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Paper 45
Entered: July 30, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00454
Patent 11,093,417 B2

Before GEORGIANNA W. BRADEN, JON M. JURGOVAN, and KEVIN C. TROCK, *Administrative Patent Judges*.

BRADEN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed motions for joinder and petitions in IPR2023-01141 and IPR2023-01142 and have been joined as petitioners to these proceedings.

I. INTRODUCTION

In this *inter partes* review, Samsung Electronics Co., Ltd. ("Samsung"), Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") challenge the patentability of claims 1–15 of U.S. Patent No. 11,093,417 B2 ("the '417 patent," Ex. 1001), which is assigned to Netlist, Inc. ("Patent Owner").

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision, issued pursuant to 35 U.S.C. § 318(a), addresses issues and arguments raised during the trial in this *inter partes* review. For the reasons discussed below, we determine Petitioner has proven by a preponderance of the evidence that claims 1–15 of the '417 patent are unpatentable. *See* 35 U.S.C. § 316(e) (2018) ("In an inter partes review instituted under this chapter, the petitioner shall have the burden of proving a proposition of unpatentability by a preponderance of the evidence.").

A. Procedural History

Samsung filed a Petition (Paper 1, "Pet.") challenging claims 1–15 of the '417 patent on the following basis:

Claims Challenged	35 U.S.C. §	References/Basis
1–15	103(a)[2]	Perego,[3] JESD79-2[4]
1–15	103(a)	Perego, JESD79-2, Ellsberry[5]

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Petitioner applies the pre-AIA version of § 103. Pet. 5.
[3] US 7,363,422 B2, issued Apr. 22, 2008 (Ex. 1071).
[4] Joint Electron Devices Engineering Council (JEDEC) DDR2 SDRAM Specification (JESD79-2), September 2003 (Ex. 1064).
[5] US 2006/0277355 A1, published Dec. 7, 2006 (Ex. 1073).

Claims Challenged	35 U.S.C. §	References/Basis
1–15	103(a)	Perego, JESD79-2, Halbert[6]

Pet. 5. Patent Owner filed a Preliminary Response. Paper 6. With Board authorization (Ex. 3001), Samsung filed a Preliminary Reply (Paper 9) to the Preliminary Response, and Patent Owner filed a Preliminary Sur-reply (Paper 10). Trial was instituted on the asserted grounds of unpatentability. Paper 11 ("Inst. Dec."), 42. After institution, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC were joined as petitioners to this proceeding based on a petition and a motion for joinder in IPR2023-01141. Paper 26.

During the trial, Patent Owner filed a Response (Paper 22, "PO Resp."), Petitioner filed a Reply (Paper 27, "Pet. Reply"), and Patent Owner filed a Sur-reply (Paper 32, "PO Sur-reply").

Petitioner filed a motion to exclude certain evidence. Paper 35. Patent Owner opposed the motion (Paper 36), and Petitioner filed a reply in support of the motion (Paper 39).

An oral hearing was held on January 11, 2024, a transcript of which appears in the record. Paper 46 ("Tr.").

Petitioner relies on testimony from Andrew Wolfe, Ph.D. Ex. 1003. Patent Owner relies on testimony from Steven Przybylski, Ph.D. Ex. 2024. The parties have entered in the record deposition transcripts of these declarants. Ex. 2033 (Wolfe Deposition); Ex. 1095 (Przybylski Deposition).

[6] US 7,024,518 B2, issued Apr. 4, 2006 (Ex. 1078).

B. Real Parties in Interest

The identified real parties in interest on the petitioner side are the following: Samsung, Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC. Pet. 1; IPR2023-01141, Paper 2, 1.

Patent Owner identifies itself as the real party in interest. Paper 4, 1.

C. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters. Pet. 1–3; Paper 4 (Patent Owner's Mandatory Notices), 1–3; IPR2023-01141, Paper 2, 1–3. We are issuing concurrently a final decision in IPR2023-00455 involving related U.S. Patent No. 9,858,215 B1 ("the '215 patent").

D. The '417 Patent and Illustrative Claim

The '417 patent relates to memory modules having ranks of memory. Ex. 1001, code (57). Claim 1 is independent and is reproduced below with Petitioner's claim element identifiers in brackets, which do not impact our analysis. *See* Pet. xiii–xiv.

> [1.a.1] A memory module [1.a.2] operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, [1.a.3] the memory bus including address and control signal lines and data signal lines, [1.a.4] the memory module comprising:
>
> > [1.b] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
> >
> > [1.c.1] logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via

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the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, [1.c.2] the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, [1.c.3] the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, [1.c.4] wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

[1.d.1] memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, [1.d.2] wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in[7]] one respective N-bit wide rank of the plurality of N-bit-wide ranks, [1.d.3] wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

[7] The word "in" was included in an amendment under 37 C.F.R. § 1.312, which the Examiner indicated was entered. Ex. 1002, 299, 313. Thus, its omission from the issued claim appears to be the result of an error by the Office.

> [1.e.1[8]] circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, [1.e.2] the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and [1.e.3] in accordance with an overall CAS latency of the memory module;
>
> [1.f] wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

Ex. 1001, 42:7–67.

II. ANALYSIS

A. Principles of Law

"In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to Patent Owner. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (discussing the burden of proof in *inter partes* review).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

[8] In the discussion of element 1.e, Petitioner provides additional element identifiers that are not reflected in the claim listing. *See* xiii–xiv, Pet. 85–94.

subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence. *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Petitioner argues that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field" and that "[a]dditional training can substitute for educational or research experience, and vice versa." Pet. 9 (citing Ex. 1003 ¶ 48); *see* Pet. Reply 1. Petitioner argues that a person of ordinary skill in the art "would have been familiar with various standards of the day including the JEDEC [(Joint Electron Devices Engineering Council)] industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM[9] memory devices and memory modules and how they interacted with the memory controller of a computer system." Pet. 9 (citing Ex. 1003 ¶ 48). Petitioner identifies other items within the ordinarily-skilled artisan's knowledge base, including "the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs

[9] DRAM (Dynamic Random-Access Memory) operates asynchronously with slower speeds and higher latency, while SDRAM (Synchronous Dynamic Random-Access Memory) synchronizes with the system clock for faster, more efficient data transfer. Ex. 1071, 4:1–12.

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(Application-Specific Integrated Circuits) and CPLDs (Complex Programmable Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers" and

> JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity.

Id. at 9–10 (citing Ex. 1003 ¶¶ 48–50; Ex. 1001, 6:43–58, 23:23–24:22, 39:21–28; Exs. 1060, 1062, 1064, 1066).

Patent Owner "applies the skill level proposed by Petitioner with one modification"—that a person of ordinary skill in the art "would have been 'knowledgeable about the operation of standardized DRAM and SDRAM memory devices and memory modules including these commercially available devices,'" as opposed to knowledgeable about the *design and* operation of DRAM and SDRAM memory devices and modules, as in Petitioner's proposal. PO Resp. 7–8 (quoting Ex. 2024 ¶ 68).

Patent Owner's attempt to omit knowledge of memory module design is problematic because, for example, "in order to render an invention unpatentable for obviousness, the prior art must enable a person of ordinary skill to make and use the invention," *In re Kumar*, 418 F.3d 1361, 1368 (Fed. Cir. 2005), and it is not apparent how a person having no knowledge of memory module design could *make* the claimed memory module. Thus, Patent Owner's proposal, on its face, would define a level of ordinary skill that precludes an obviousness conclusion.

Patent Owner's declarant, Dr. Przybylski, appears to have a slightly different position than Patent Owner, testifying that

> the design of memory modules using semiconductor memories and the design of those semiconductor memories are two distinct areas of knowledge and a [person of ordinary skill in the art] with *an ordinary level of skill in the design of memory modules* would not possess the training, knowledge or expertise to attempt to design semiconductor memory design.

Ex. 2024 ¶ 68. Thus, Dr. Przybylski's testimony indicates that an ordinarily skilled artisan at the critical time would have been knowledgeable about the design of memory modules.

At oral argument, we addressed this topic with the parties. Tr. 11:10–13:24, 43:9–46:10, 85:16–87:9. Patent Owner agreed that memory module design was within the knowledge of a person of ordinary skill in the art. Tr. 45:13–16. The parties agreed that a person of ordinary skill in the art would have had knowledge of the operation of the memory devices that go into the memory modules but would not necessarily have needed to know how to design those memory devices. Tr. 45:17–46:6, 85:16–86:4. Ultimately, however, the parties agreed that a person of ordinary skill in the art would have had knowledge about the design and operation of memory modules and the operation of memory devices within those modules. Tr. 46:2–6 (Patent Owner's agreement), 85:16–86:2 (Petitioner's agreement).

Thus, we consider the parties' dispute to be resolved, and we adopt Petitioner's construction with two modifications. First, we adopt the parties' agreement that a person of ordinary skill in the art would have had knowledge about the design and operation of standardized DRAM and SDRAM memory modules and the operation of memory devices within those modules, omitting the Petition's proposed requirement of knowledge of the *design* of standardized DRAM and SDRAM memory devices. This

includes knowledge of JEDEC industry standards. Second, we delete the qualifier "at least" to eliminate vagueness as to the amount of experience.

Accordingly, a person of ordinary skill in the art would have had an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and three years working in the field, where additional training could substitute for educational or research experience, and vice versa. Additionally, a person of ordinary skill in the art would have had knowledge about the design and operation of standardized DRAM and SDRAM memory modules and the operation of memory devices within those modules. We consider the resulting agreed-upon definition of the level of ordinary skill in the art to be consistent with the '417 patent and the prior art of record.

C. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b). Independent claim 1 recites memory devices arranged in ranks. Petitioner argues that a "rank" is "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 26 (citing Ex. 1003 ¶ 126); Pet. Reply 1–2. Patent Owner disagrees that a rank can be a single memory device but states that "the Board need not resolve that dispute to address the parties' arguments regarding the challenged claims" because Patent Owner "applies Petitioner's proposed construction" "[s]olely for purposes of responding to this Petition." PO Resp. 8–9.

Patent Owner also apprises us of a construction of "rank" from related district court litigation. PO Resp. 8 (citing Ex. 2030, 12–15). Our Rules provide that "[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record in the inter partes review proceeding will be considered." 37 C.F.R. § 42.100(b). We have considered this construction, and we note that, like Petitioner's proposed construction, it provides that a rank can be one memory device. *See* Ex. 2030, 14 ("Accordingly, the Court concludes a 'rank' can include a single memory device.").

In our patentability analysis, we adopt the construction of "rank" applied by both parties in this proceeding, and we need not engage in any further claim construction because there are no claim construction disputes that bear on the issues before us. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Alleged Obviousness of Claims 1–15 in View of Perego and JESD79-2

Petitioner asserts that claims 1–15 are unpatentable because they would have been obvious to a person of ordinary skill in the art at the critical time in view of the combined teachings of Perego and JESD79-2. Pet. 5, 28–111. Patent Owner opposes. PO Resp. 18–39; PO Sur-reply 6–20. For reasons that follow, we determine Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable under 35 U.S.C. § 103(a).

1. Overview of the Asserted Prior Art

a. Perego (Ex. 1071)

Perego pertains to memory systems and discloses a memory module with a configurable width buffer device. Ex. 1071, code (57). One embodiment of Perego is shown in Figure 3C, reproduced below.

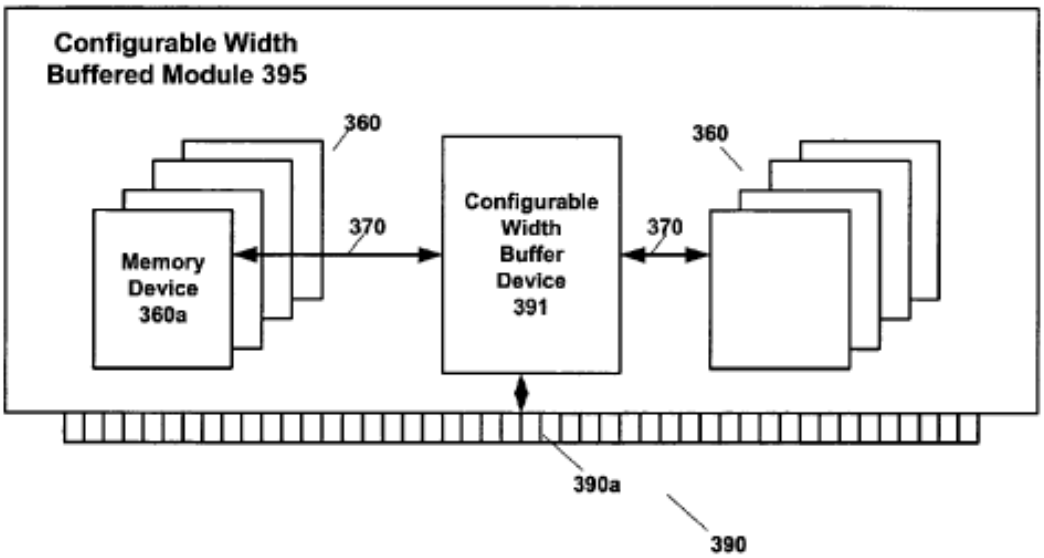

Fig. 3C

Perego's Figure 3C, above, is a block diagram illustrating a "memory module that includes a configurable width buffer device" having configurable width buffer device 391 (not shown) that is connected on the bottom to interface connections 390a in connector 390 and that is connected on the sides to memory devices 360 via channels 370. Ex. 1071, 2:43–45, 7:30–39.

Another embodiment of Perego is shown in Figure 5B, reproduced below.

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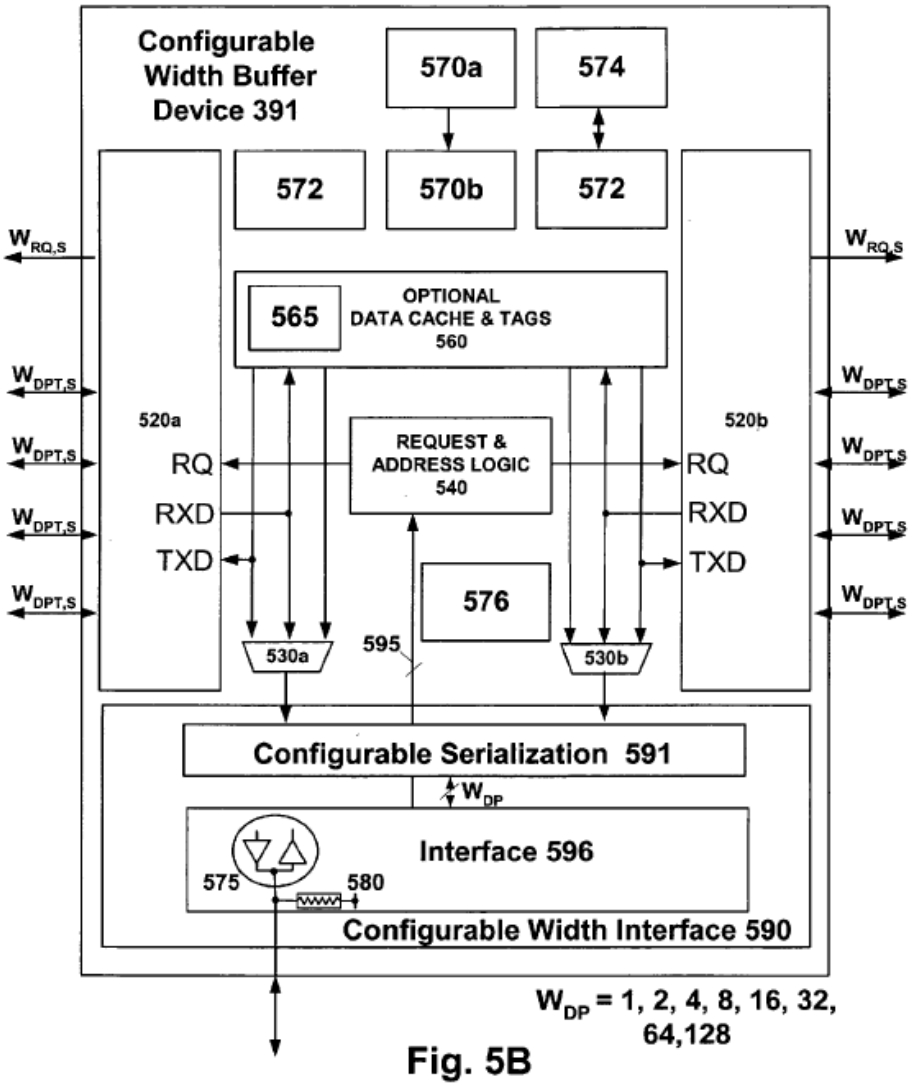

Fig. 5B

Perego's Figure 5B, above, is block diagram illustrating a configurable width buffer device 391, and we discuss this figure and the accompanying disclosure in detail in our analysis below. *See* Ex. 1071, 2:51–53, 13:6–8 ("FIG. 5B illustrates a configurable width buffer device 391 as seen in FIG. 3C in an embodiment of the present invention."). Perego also discloses that Double Data Rate 2 ("DDR2") memory devices can be used on its memory modules. *Id.* at 10:56–59.

b. JESD79-2 (Ex. 1064)

JESD79-2 is a JEDEC standard for DDR2 memory devices. Ex. 1064. It was published in September 2003 and provides industry standards for the programming and operating modes of DDR2 SDRAM. *Id.* at 12. The standard specifically addresses additive latency (AL) in the DDR2 SDRAM Extended Mode Register Set (EMRS). *Id.* at 14. Per the standard, the Read Latency (RL) is controlled by the sum of the additive latency (AL) and the CAS latency (CL). *Id.* at 24. Therefore, according to JESD79-2, if a user chooses to issue a R/W (read/write) command before the Internal RAS-CAS-Delay Time (tRCDmin), then AL (greater than 0) must be written into the EMRS(1). *Id.* The Write Latency (WL) is always defined as RL - 1 (read latency -1) where read latency is defined as the sum of additive latency plus CAS latency (RL=AL+CL). *Id.* Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section). *Id.* JESD79-2 discloses that the RL is equal to an additive latency (AL) plus CAS latency (CL), where CL is defined by the Mode Register Set (MRS), similar to the existing SDR and DDR SDRAMs, while AL is defined by the Extended Mode Register Set (1) (EMRS(1)). *Id.* at 26.

2. Analysis of Claim 1

Claim 1 recites a memory module having various components that are configured or configurable to operate in a particular manner, which we address in more detail below. To address claim 1, Petitioner relies on Perego's memory module disclosures in combination with JESD79-2's disclosures of DDR2 memory operations. Pet. 28–96. Patent Owner disputes Petitioner's contentions and argues that an ordinarily skilled artisan

at the critical time would not have had reason to alter Perego's memory modules as Petitioner suggests. PO Resp. 18.

a) Preamble (1.a.1)

The preamble of claim 1 recites the following:

> A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising.

Petitioner argues that Perego's Figures 3B, 3C, 4A, 4B, and 4C show memory modules that communicate data with a memory controller of a computer system via a bus. Pet. 33–39. Perego's Figure 4A is reproduced below.

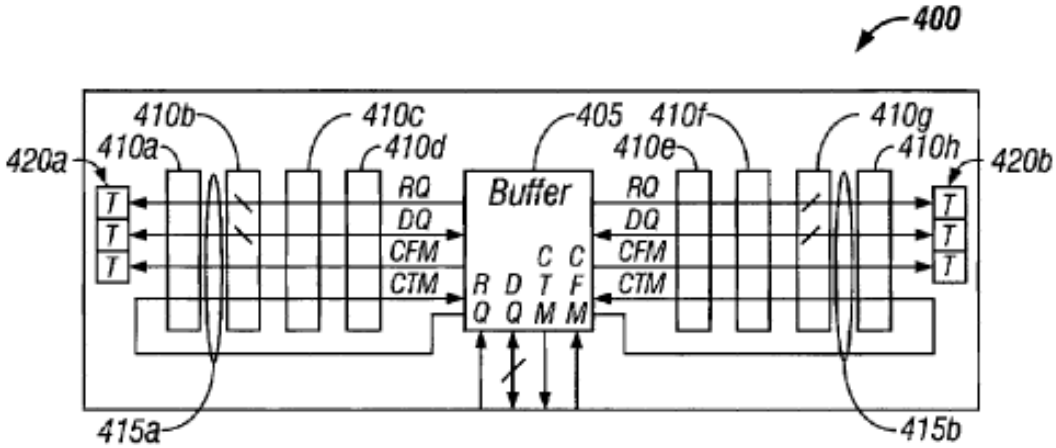

FIG. 4A

Perego's Figure 4A, above, is a diagram showing memory module 400 with buffer 405 connected to memory devices 410a–h over a pair of channels 415a and 415b. Ex. 1071, 9:26–33.

For the recited memory commands, Petitioner cites Perego's disclosure of storing and retrieving data in response to commands, and Petitioner argues that a person of ordinary skill in the art would "have

understood from their own knowledge of JEDEC standards, including JESD79-2, the specific ways to issue read and write commands to Perego's DDR2 memory devices." Pet. 39–40 (citing Ex. 1071, 6:15–25, 9:50–60, Fig. 3B; Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 216–218).

Petitioner argues that Perego discloses address and control lines and data lines on the memory bus. Pet. 40–41 (citing Ex. 1071, 5:12–15, 5:21–24, 9:43–45, 9:58–60, Figs. 3B, 4A, 4B; Ex. 1003 ¶¶ 220–224); *see* Ex. 1071, 5:12–15 ("One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n."), 5:21–24 ("In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines)."). Petitioner notes that these are the vertical RQ and DQ lines in Figure 4A. *See* Pet. 41 (parenthetical identifying "RQ and DQ lines connecting to the memory bus" in Figures 4A and 4B), 44 (noting that the address and control lines are "the vertical RQ lines coupled to the edge of the module in Figures 4A–4B").

For the "N-bit wide memory bus" recited in claim 1, Petitioner argues that Perego discloses several data width options for its memory bus, and Petitioner specifically relies on Perego's 64-bit data width. Pet. 37–38 (citing Ex. 1071, 3:12–22, 3:41–47, 3:62–4:12, 4:65–5:24, 6:15–25, 9:50–60, 11:8–12, 14:16–51, Figs. 3B, 4A, 4B, 5A, 5B; Ex. 1003 ¶¶ 208–219; Ex. 1064, 24–33, 49; Ex. 1062, 5). Perego discloses an embodiment in which the interface of its buffer has "128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391." Ex. 1071, 14:19–23. Petitioner argues that a person of ordinary skill in the art "would have

understood that a data width of W_{DP}=64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM [(dual inline memory module)]." Pet. 38 (citing Ex. 1062, 5; Ex. 1003 ¶ 215). Petitioner's declarant Dr. Wolfe testifies in support of this assertion, citing JEDEC standards showing a 64-bit DIMM. Ex. 1003 ¶ 215 (citing Ex. 1071, 2:4–6; Ex. 1062, 5). Petitioner argues that a person of ordinary skill in the art would have "been motivated to implement Perego's memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2," which would have "allow[ed] these modules to be used in JEDEC-compliant memory systems." Pet. 32–33 (citing Ex. 1003 ¶¶ 180–185).

Patent Owner does not dispute that the combination of Perego and JESD79-2 teaches the subject matter recited in the preamble, but does dispute Petitioner's contentions regarding implementing Perego's module as a JEDEC-compliant DIMM. PO Resp. 18–24 (citing Ex. 2024 ¶¶ 128–134). Based on Petitioner's persuasive contentions and evidence, summarized and cited above, we find that the combination of Perego and JESD79-2 teaches the subject matter recited in the preamble. In view of this finding, we need not decide whether the preamble is limiting.

We address the parties' dispute about a JEDEC-compliant module below in our discussion of the "input chip select signals" subject matter of claim 1.

b) Printed circuit board (1.b)

Claim 1 recites "a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding

plurality of contacts of a module slot of the computer system." Petitioner argues that Perego's disclosure of including memory modules on printed circuit boards (PCBs) with connectors (such as connectors 390a in Figure 3C) teaches this subject matter. Pet. 42–43 (citing Ex. 1071, 5:56–6:11, 7:39–41, Figs. 3B, 3C; Ex. 1003 ¶¶ 228–233); *see, e.g.*, Ex. 1071, 5:60–62 (disclosing that "memory subsystems are incorporated onto individual substrates (e.g., PCBs)").

Patent Owner does not dispute this contention. *See generally* PO Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitation 1.b.

Petitioner also argues that a person of ordinary skill in the art would have understood that Perego's memory modules could be implemented in a standard dual in-line memory module (DIMM), which would use a PCB with edge connections. Pet. 43 (citing Ex. 1071, 3:25–28, 6:34–43; Ex. 1069, 2; Ex. 1062, 29, 66; Ex. 1003 ¶ 232). Patent Owner disputes Petitioner's contentions about implementing Perego's module as a JEDEC-compliant DIMM, and we address this dispute below in our discussion of the "input chip select signals" subject matter of claim 1.

c) Input chip select signals (1.c.1, 1.c.2)

Claim 1 recites

> logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,

> the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value.

As recited in the preamble, the "address and control signal lines" are on the memory bus that connects the memory module with the memory controller of the computer. Thus, the recited "input chip select signals" are signals that the module receives from the memory controller.

(1) Petitioner's Arguments

Petitioner contends that Perego's buffer devices have logic that receives input address and control signals for a memory command from a memory controller via signal lines, specifically the vertical control lines labeled "RQ" in Figures 4A and 4B. Pet. 43–48 (citing Ex. 1071, 4:3–6, 9:43–60, Figs. 4A, 4B, 5A, 5B; Ex. 1003 ¶¶ 234–243). As Petitioner points out (Pet. 48), Perego discloses "control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column) information." Ex. 1071, 9:50–53. Perego discloses that control and address information is "contained in packets" in one embodiment, but it then discloses that, "[i]n alternate embodiments, control lines (RQ) may comprise *individual control lines*, for example, row address strobe, column address strobe, etc., and address lines." Ex. 1071, 9:50–60 (emphasis added). We further discuss Perego's disclosure of individual control lines below when we address the parties' disputes about input chip select signals.

Petitioner also contends that JESD79-2 discloses that "read and write commands include both address signals (e.g., BA0–BA2, A0–A15) and control signals (e.g., CS chip select, RAS, CAS, WE)." Pet. 48 (citing

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Ex. 1064, 6, 49; Ex. 1003 ¶ 238). Petitioner argues that it "would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module" where the signals correspond to multiple ranks of memory devices and where one of the signals is active to select the target rank and the other signals are inactive. *Id.* at 57–58 (citing Ex. 1062, 6; Ex. 1066, 6–7; Ex. 1003 ¶¶ 251–252); *see also id.* at 52–54 (explaining that chip select signal (CS) is active low).

Petitioner then contends that Perego is consistent with JESD79-2's disclosure of selecting particular groups of memory devices because "Perego discloses that its module includes multiple sets of memory devices (e.g., 'ranks,' . . .), each of which can be a target of a memory read or write command, and each of which acts together in response to a memory read or write command." Pet. 54–57 (citing Ex. 1071, 6:12–24, 15:37–45, Figs. 3C, 4A, 4B, 4C; Ex. 1003 ¶¶ 249–250).

According to Petitioner, a person of ordinary skill in the art would have had reason to combine the teachings of Perego and JESD79-2 because Perego discloses that its memory modules can use DDR2 memory devices and "the JEDEC standard for DDR2 memory devices is JESD79-2." Pet. 30 (citing Ex. 1071, 3:62–4:12, 8:1–4, 10:54–67; Ex. 1064); *see also id.* at 30–33 (further explaining rationale to combine). Petitioner then asserts that a person of ordinary skill in the art would have been motivated to make Perego's memory modules JEDEC-compliant "to allow these modules to be used in JEDEC-compliant memory systems, such as those using DIMM

modules of the format described by JESD21-C." *Id.* at 33 (citing Ex. 1003 ¶ 185).

Petitioner further argues that a person of ordinary skill in the art would have understood that "Perego's buffer device 'register[s]' address and control signals similar to a JEDEC-compliant conventional registered DIMM." Pet. 49–50 (citing Ex. 1071, 6:15–30, 13:54–59, Fig. 5C; Ex. 1062, 12; Ex. 1003 ¶¶ 239–240).

(2) Patent Owner's Arguments

Patent Owner argues that a JEDEC-compliant module that receives chip select signals "is fundamentally at odds with" Perego's architecture, which Patent Owner asserts is "a Rambus-style point-to-point topology." PO Resp. 9 (citing Ex. 1071, code (57), 4:38–45, 5:35–55, 8:10–17, 8:20–26), 23. According to Patent Owner, "Perego discloses Rambus-style modules that employ a point-to-point architecture and configurable bit-width interfaces that are fundamentally different than the conventional memory bus required by JEDEC module standards and do not include chip-select lines or otherwise convey chip-select signals." *Id.* at 1. Patent Owner further argues that "Perego repeatedly and consistently emphasizes the benefits of its point-to-point architecture over a conventional JEDEC-style bus." *Id.* at 9–10 (citing Ex. 1071, 3:47–56, 4:65–5:1, 5:6–15, 5:32–55, 6:15–19, 13:49–59, 21:46–50, Figs. 3A/3B, Fig. 5A). Patent Owner explains that "in contrast to a conventional registered DIMM ('RDIMM'), in Perego's architecture, control/address information is transmitted to the module via packets and multiplexed with data in order to be transmitted via the point-to-point links." *Id.* at 10 (citing Ex. 1071, 13:49–59).

Patent Owner's declarant, Dr. Przybylski, testifies that "Perego specifically refers to a dynamic point-to-point topology to connect the memory controller to the memory subsystem/module" and that a person of ordinary skill in the art, "being familiar with the Rambus XDR architecture, would recognize this terminology as being specific to the XDR architecture." Ex. 2024 ¶ 96 (citing Ex. 1071, 3:41–47, 5:32–35, 6:57–7:29, 8:1–9; Ex. 2009, 10–12, 15, 17).

The assignee of the Perego patent is Rambus, Inc. (Ex. 1071, code (73)), and there is no dispute that Perego discloses features that are consistent with Rambus's point-to-point architecture. And, it may be true that a person of ordinary skill in the art would have understood Perego's point-to-point terminology to refer to the Rambus XDR architecture, and Perego mentions Rambus XDR memory devices. Ex. 1071, 8:1–9. But, as explained below, Perego's disclosures are not limited to that architecture. For example, Perego discloses that "one or more busses *or* a plurality of point-to-point links may be used to couple one or more buffer devices to a master (e.g., a controller or microprocessor device)" and that a "dynamic point-to-point link topology *or* any combination of point-to-point links or busses may be used to interface the master device and a corresponding buffer device." *Id.* at 3:41–47 (emphasis added). Thus, Perego discloses that a bus, as an alternative to point-to-point links, may be used to connect the module to the memory controller.

Dr. Przybylski further explains that

> Perego's memory system (300 or 305) is built with a plurality of point-to-point buses (320) connecting a memory controller (310) with memory subsystems (330). Ex. 1071, Figure 3A, 3B, 4:63–5:15. These memory subsystems can be inserted into sockets (380) and in these embodiments comprise

> modules (340, 400). Though several embodiments of buses 320 are disclosed they are all point-to-point with one end connected to the memory controller and the other to the memory subsystem. Ex. 1071, Figures 3A, 3B, 6A, 6B, 7, 8A, 8B, 8C, 4:63–5:15, 20:48–64, 20:65–21:3, 21:39–22:9. The point to point links are used to convey read and write data, and address and control information can be multiplexed with data or be transported on their own buses. Ex. 1071, Figures 5A, 5B, 5:16–31, 8:10–19, 13:49–59.

Ex. 2024 ¶ 95. Here, Dr. Przybylski refers to the elements labeled 320 in Perego as "point-to-point buses," but Perego does not use this terminology. Rather, Perego refers to every instance of element 320 as "point-to-point link[s]." *See* Ex. 1071, 4:66–67, 5:14–15, 5:56, 5:63–64, 6:11, 6:17, 6:23–24, 7:1, 7:3, 7:8–9, 8:20, 8:42, 8:48–49, 8:67, 9:8, 9:48, 11:9, 11:12, 11:22, 11:27–28, 11:40, 12:14–15, 12:41. Indeed, Perego discloses that "[s]ignaling over point-to-point links 320a–320n *or alternatively*, over bussed topologies, may incorporate different modulation methods." *Id.* at 8:42–47 (emphasis added). Perego goes on to explain the difference between a "point-to-point link" and a bus. *Id.* at 8:51–65. Thus, Perego discloses busses as an alternative to the point-to-point topology that Dr. Przybylski says is indicative of Rambus XDR.

Data width is another indicator that Perego is not limited to a Rambus architecture. Dr. Przybylski relies on Exhibit 2009 to explain Rambus XDR technology. *See* Ex. 2024 ¶ 96 (citing Exhibit 2009 to explain that "point-to-point" refers to Rambus XDR). The largest module data width disclosed in that exhibit is 36 bits. Ex. 2009, 10 (disclosing a 32-bit module data width, which may be 36-bits wide with ECC). Perego, however, discloses a module data width of up to 128 bits (Ex. 1071, 14:16–23), which is further

evidence that Perego's disclosure encompasses more than just Rambus XDR.

Perego also discloses that the buffer can be configured with a data width of 64 bits. Ex. 1071, 14:19–23 ("In an embodiment of the present invention, interface 596 includes 128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391."). Petitioner asserts, with supporting testimony from Dr. Wolfe, that a person of ordinary skill in the art "would have understood that a data width of W_{DP}=64 corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module." Pet. 38 (citing Ex. 1003 ¶ 215; Ex. 1062, 5); *see* Ex. 1062 (Jan. 2002 JESD21-C RDIMM Specification), 5 (providing DIMM organization of "x72 ECC, x64").

Dr. Przybylski's testimony confirms that a 64-bit width was a JEDEC width. For example, Dr. Przybylski testifies that a person of ordinary skill in the art "would recognize the x64 and x72-wide memory modules mentioned in the '417 Patent, 2:47–53, as referencing JEDEC-standard compliant memory modules." Ex. 2024 ¶ 72 (citing Ex. 1066, 4). Dr. Przybylski also testifies that a person of ordinary skill in the art would have understood that, as of January 2005, a "disclosed DIMM module has a 64-bit data bus, just as all the JEDEC-standardized SDRAM-based DIMMs of the day." *Id.* ¶ 82.

Thus, the evidence shows that a 64-bit data width is a JEDEC-compliant module width and is not limited to a Rambus XDR module width, supporting Petitioner's contention that Perego's disclosure suggests a module that can be configured to have a JEDEC interface. *See* Pet. 38. We do not agree with Patent Owner's suggestion that Perego's configurable

buffer width makes it unsuitable to be implemented as an RDIMM, which has a fixed buffer width. *See* PO Resp. 23 ("Furthermore, the RDIMM relied on by Petitioners has a fixed buffer width (EX2003, 43:12–20; EX1064, 1–6, EX2024, ¶ 24), whereas configurable width buffer devices are central to Perego." (citing Ex. 1071, Abstract, Title, Figs. 3C, 4A, 5A, 5B, 13:6–17, 13:49–59, 14:52–15:6, 15:31–45, 17:22–33). We see no incompatibility where Perego discloses the RDIMM width along with other widths.

Petitioner also relies on Perego's disclosure of using individual control lines. Pet. 41 (citing Ex. 1071, 9:43–45, 9:58–60). Perego discloses an alternative to a packetized signaling approach in which "control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines." Ex. 1071, 9:50–60. Petitioner argues that individual control lines are indicative of a JEDEC-style memory bus. Pet. Reply 6–7 (citing Ex. 1071, 9:58–60, 10:54–59, Fig. 4A; Ex. 1064, 6; Ex. 2025, 3; Ex. 1003 ¶¶ 217–218; Ex. 2033, 141:6–145:24, 148:18–149:6).

Patent Owner counters that, "[e]ven when Perego discusses providing 'individual control lines,' it never mentions a chip-select signal line (or any of the other signal lines characteristic of a JEDEC-style RDIMM, such as CKE, DQS, etc.)." PO Resp. 22 (citing Ex. 1071, 9:58–60; Ex. 2024 ¶¶ 129, 139; Ex. 1066, 6; Ex. 1069, 12; Ex. 2001, 20–23). Although this passage of Perego does not mention chip select signals, it mentions "row address strobe, column address strobe, etc., and address lines" as exemplary individual control lines. Ex. 1071, 9:58–60. The evidence shows that row address strobe (RAS) and column address strobe (CAS) are JEDEC module input

signals and not Rambus signals. Ex. 1066, 6 (RDIMM pins for RAS and CAS); Ex. 1062, 6 (same); Ex. 1095, 235:1–236:25 (Dr. Przybylski's testimony in which he agrees that a Rambus direct DRAM does not have pins for RAS and CAS signals as in DDR devices).

Dr. Przybylski also testifies that

> [a]nother of the essential aspects of Direct RDRAMs that differentiate them from all of the JEDEC-defined SDRAMs is the encoding of the 8-bit RQ control bus. Instead of presenting the entire command and address at once on 24 signal lines, captured by a single clock edge, the Direct RDRAM RQ bus has only 8 transmission lines. In addition, instead of 1 command spread across 24 signal lines, row commands with their row addresses are gathered into a packet and sent over 8 bit periods on only 3 lines. Column commands are sent with the column addresses, data masking and precharge indicators over 5 metal traces in the same 8 bit period.

Ex. 2024 ¶ 46. This testimony shows that individual address lines as disclosed in Perego are not characteristic of Rambus-type memories. Thus, contrary to Patent Owner's argument above, Perego expressly discloses "signal lines characteristic of a JEDEC-style RDIMM." *See* PO Resp. 22.

Patent Owner also argues that Perego's disclosure of individual lines "relates to secondary channel signal lines," i.e., those between the buffer and the memory devices, and not the primary channel between the memory controller and the memory module. PO Sur-reply 9 (citing Ex. 1071, 9:43–60). Perego's disclosure of using "individual control lines" appears in a discussion of Figure 4A (reproduced above in § II.D.2.a), in which Perego discloses that "[s]ignal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM)." Ex. 1071, 9:43–45. Channels 415a and 415b are the channels between the buffer and the memory devices, so Perego's disclosure of individual lines certainly pertains

to the secondary channels, as asserted by Patent Owner. Figure 4A, however, shows that the primary channel has the same signals lines—RQ, DQ, CTM, and CFM (shown vertically). In view of Perego's other disclosures suggesting non-Rambus module interfaces, discussed above, we do not understand Perego's disclosure that "control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines" to be limited only to the RQ lines between the buffer and the memory devices. Rather, we find that this disclosure, read in light of Perego as a whole, at least suggests individual control lines on the primary channel as well.

Furthermore, other evidence also suggests that Perego is not limited to a Rambus-style architecture at the module interface. For example, Perego discloses that "the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of *possible module configurations* in the system." Ex. 1071, 3:25–28 (emphasis added). This indicates that Perego's disclosure is concerned with more than just one type of memory module, such as a Rambus module.

Perego further discloses that its buffered module provides flexibility because "new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." Ex. 1071, 6:34–43. In this context, it makes sense that Perego would leave the option open to use a bus on the interface between the module and the controller and not be limited to a point-to-point system, which would limit the ability to interface with a system that uses a bus, such as a JEDEC system. Indeed, Perego states:

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> However, using conventional signaling schemes, the bussed approaches lend efficiency towards resource utilization of a system and permits module interfacing for upgradeability.
>
> There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

Ex. 1071, 2:22–29. Thus, Perego discloses that upgradeability was a goal and that busses permit such action.

Based on the foregoing discussion, we find that Perego's disclosure suggests a JEDEC-compliant interface to a memory controller.

Furthermore, the evidence shows that JEDEC-compliant modules were dominant in the market at the relevant time. For example, Dr. Przybylski testifies that,

> in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a [person of ordinary skill in the art] the use of JEDEC-standard compliant SDRAM devices or modules.

Ex. 2024 ¶ 72. Petitioner asserts that the dominance of JEDEC-compliant modules "provid[es] additional motivation for the proposed combination." Pet. Reply 5–6. Patent Owner counters that the "mere fact that JEDEC-standardized modules dominated the market at the time of the invention also does not provide motivation to modify Perego." PO Sur-reply 11 (citing *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882 (Fed. Cir. 2024). We agree with Petitioner on this point. In the case relied on by Patent Owner, the Federal Circuit stated that "*KSR* did not do away with the

requirement that there must exist a motivation to combine various prior art references in order for a skilled artisan to make the claimed invention," and the court reversed the Board's conclusion of obviousness finding that there was "no evidence of a design need or market pressure." *Virtek*, 97 F.4th at 887–88. Here, Patent Owner's own expert explains that JEDEC was a driving market force at the relevant time.

Patent Owner also argues that modification of Perego's architecture and memory system with a JEDEC-compatible bus would make it non-functional. PO Resp. 29–30, 23–24 ("JEDEC-complaint, chip-select-dependent RDIMM architecture defined in JESD21-C is fundamentally at odds with the Rambus point-to-point topology and variable bit width interfaces of Perego."). But Patent Owner's "proposed" modifications would make Perego's system non-functional for Rambus, not for JEDEC, which was the dominant memory module style in the market. Given JEDEC as the standard, an ordinarily skilled artisan would have reason to pursue such a known option.

Patent Owner also argues that "Perego contrasts its memory modules with 'conventional DIMM module designs.'" PO Resp. 23–24 (quoting Ex. 1071, 6:27–33; citing Ex. 1071, 1:31–49, 2:15–30). Perego, however, draws a distinction based on the lack of buffered data lines in a conventional DIMM:

> In this embodiment, memory subsystems 330a-330n are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system 100).

Ex. 1071, 6:25–33. This passage shows that Perego discloses data buffering on the memory module, which was not present in DIMMs of that time. *See* Ex. 2024 ¶ 32 ("The two most common styles of JEDEC-standardized modules are called Unbuffered DIMMs (or UDIMMS), which contain principally just SDRAMs, and Registered DIMMs, which also include a register device for buffering the address and command buses (but not the data bus)."). We do not read Perego's disclosure of the lack of data buffering on DIMMs of the time as discounting all DIMM teachings.

We find that Perego suggests a JEDEC-compliant interface with its disclosure of a 64-bit module width, and we further find that a person of ordinary skill in the art would have been motivated to make a module JEDEC-compliant based on JEDEC's dominance in the market at the time. *See* Ex. 1003 ¶ 183 (Dr. Wolfe's testimony that a person of ordinary skill in the art "would have been motivated to implement Perego's memory modules in a registered DIMM format that fits into the DIMM connectors of the time and uses the input and output signals of a DIMM module according to the relevant JEDEC standards, including JESD21-C.").

Patent Owner also argues that Petitioner's reliance on JESD21-C (Exs. 1062, 1066) for details of a JEDEC-compliant memory module is improper because JESD21-C is not part of any challenge in the Petition. PO Resp. 24–25. Rather, Patent Owner notes, JESD79-2 is the relied-upon JEDEC standards reference, and it relates to memory devices, not memory modules. *Id.* at 1, 20. Thus, Patent Owner argues that the asserted combination of references does not teach the recited "input chip select signals," which are inputs to the module, not to individual memory devices. *Id.* at 31.

We see no impropriety in Petitioner's reference to JESD21-C as support for its "input chip select signals" contentions. As an initial matter, Patent Owner argues that "chip-select signals . . . are a hallmark of JEDEC-compliant bus architecture." PO Resp. 21 (citing Ex. 2024 ¶ 129; Ex. 1069, 2). Patent Owner's cited support states that "the chip-select bus[] is essential in a JEDEC-style memory system." Ex. 1069, 2. This is the type of knowledge that the parties agree a person of ordinary skill in the art would have had. *See* Pet. 9 (asserting that a person of ordinary skill in the art "would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard"); PO Resp. 8 (asserting that a person of ordinary skill in the art would have been "knowledgeable about the operation of *standardized* DRAM and SDRAM memory devices and memory modules" (emphasis added)); *id.* at 43 (arguing what a person of ordinary skill in the art would have understood "based on knowledge of the art and contemporaneous JEDEC standards"); Ex. 2024 ¶ 72 (Dr. Przybylski "not[ing] that in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a [person of ordinary skill in the art] the use of JEDEC-standard compliant SDRAM devices or modules").

As discussed above, we find that Perego suggests a JEDEC-compliant interface with its disclosure of a 64-bit module width and that a person of ordinary skill in the art would have been motivated to make a module JEDEC-compliant based on JEDEC's dominance in the market at the time.

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Once a module is JEDEC-compliant, a person of ordinary skill in the art would have known that it would be "configurable to receive . . . a plurality of input chip select signals," which would be sent by a separate memory controller that is not claimed, based on the knowledge of JEDEC standards, including JESD21-C. *See* Ex. 1062, 6 (identifying "SDRAM chip select lines" for DIMMs), *cited in* Pet. 57–58.

Furthermore, Patent Owner argues that "[c]hip-select signals are used to select ranks." PO Resp. 21–24 (citing Ex. 2031, 7 ("Rank: any DRAMs connected to the same CS")). Exhibit 2031's header ("JEDEC Standard No. 21-C") indicates that the exhibit pertains to JESD21-C, which is the module standard, and the exhibit states that it "describes the serial presence detects for the DDR2 version of the synchronous DRAM *modules*." Ex. 2031, 1 (emphasis added). The page cited by Patent Owner pertains to a field that "describes the number of ranks (Rank: any DRAMs connected to same physical CS) and package on the SDRAM module, and module height." *Id.* at 7. As Petitioner points out, JESDS79-2 discloses that "Chip Select . . . provides for external Rank selection on systems with multiple Ranks" and that chip select "is considered part of the command code." Ex. 1064, 6; *see* Pet. Reply 4–5. Thus, JESD79-2, which is part of the asserted grounds, discloses that chip select signals are received at the module for "external Rank selection" consistent with Patent Owner's cited evidence, which pertains to the module.

d) Registered address and control signals (1.c.3)

Claim 1 recites

> the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and

> other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value.

Petitioner argues that JESD79-2 discloses read and write commands that include a chip select signal to identify the target rank of memory devices using an active low signal with non-active ranks receiving a high signal. Pet. 58–59 (citing Ex. 1064, 6, 24–33, 49; Ex. 1003 ¶¶ 255–263). Petitioner argues that Perego is consistent with this because it "teaches that only the targeted rank of memory devices would participate in the read or write operation, while the other memory devices would 'remain in a ready or standby state until called upon to perform memory access operations.'" *Id.* at 59–60 (quoting Ex. 1071, 21:16–20; citing Ex. 1071, 15:40–45; Ex. 1003 ¶¶ 257–260). Petitioner argues that a person of ordinary skill in the art "would have known that under the JEDEC standards it was standard for a memory module to use registered chip-select signals to target one rank of memory devices for a read or write operation." *Id.* at 60 (citing Ex. 1064, 6; Ex. 1062, 12–13; Ex. 1066, 10, 12–13, Ex. 1069, 2–3; Ex. 1003 ¶ 259).

Patent Owner does not separately address this limitation, apart from its arguments about chip select signals, which we discuss above. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. We note, however, that Patent Owner disputes Petitioner's contentions that the combination of Perego and JESD79-2 teaches ranks, and we address this below.

Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, we find that Perego discloses limitation 1.c.3.

e) Data buffer control signals (1.c.4)

Claim 1 recites "wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command." Petitioner argues that a person of ordinary skill in the art

> would have understood that Perego's buffer device includes logic that outputs data buffer control signals to transceivers (e.g., 575, included in interface 520a, 520b, 510, and 590), multiplexing/demultiplexing circuits 597, and to input/output latches 597f-m, to selectively activate these circuit elements of the "buffer" according to the targeted rank and direction of the read and write operation.

Pet. 63 (citing Ex. 1071, 14:62–15:6, 15:34–37, 17:41–44, 17:61–62, Figs. 5A, 5B; Ex. 1003 ¶¶ 270–271).

Patent Owner does not dispute Petitioner's contentions for this limitation. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. Based on the entire trial record, we agree with Petitioner's analysis and we credit Dr. Wolfe's testimony supporting Petitioner's position. Accordingly, find that Perego discloses limitation 1.c.4.

f) Ranks (1.d.1, 1.d.2, 1.d.3)

Claim 1 recites

> memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices [in] one respective N-bit wide rank of the plurality of N-bit-wide

> ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command.

Petitioner argues that Perego teaches memory circuits arranged in ranks by disclosing groups of memory devices that are accessed together in a memory operation. Pet. 64–73 (citing Ex. 1071, 2:4–6, 3:62–4:3, 4:19–22, 6:12–24, 8:1–4, 10:56–58, 14:10–40, 15:37–45, 17:22–28, 21:16–20, Figs. 3C, 4A, 4B, 4C, 5A, 5B; Ex. 1003 ¶¶ 274–296). For example, Perego discloses "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Ex. 1071, 15:37–45, *quoted in* Pet. 67.

Petitioner also argues that "it would have been obvious to a [person of ordinary skill in the art] to arrange Perego's DDR memory devices into '*ranks*,' and a [person of ordinary skill in the art] would have been motivated to do so, in light of the JEDEC standards." Pet. 72 (citing Ex. 1064, 6; Ex. 1062, 13, 26–28; Ex. 1003 ¶¶ 287–289). Petitioner relies on JESD79-2's disclosure of chip select signals for ranks. *Id.* at 72 (citing Ex. 1064, 6; Ex. 1003 ¶¶ 287–289; Ex. 1062, 13).

Patent Owner disagrees with Petitioner, arguing that Perego does not disclose ranks. PO Resp. 33–36. Patent Owner specifically argues that "Rambus memory devices are incompatible with the concept of ranks because they are each accessed individually and thus do not 'act together' as proposed by Petitioner." *Id.* at 33 (citing, *inter alia*, Ex. 2024 ¶¶ 162–175).

We do not agree with Patent Owner that Perego is incompatible with ranks. Perego expressly discloses the use of DDR2 SDRAM memory devices on the module. Ex. 1071, 56–59. Dr. Przybylski testifies that, in

Perego, "the memory system can include modules that include either Direct RDRAMs, which are not organized into ranks as, for example, DDR2 SDRAMs are." Ex. 2024 ¶¶ 113. Thus, Patent Owner's own evidence shows that DDR2s would be organized in ranks. Based on this evidence, we find that a person of ordinary skill in the art at the critical time would have arranged Perego's DDR2 memory devices into ranks because that is how DDR2s are organized. *See* Pet. 72 (asserting that ranks would have been obvious); Ex. 1062, 29, 35 (illustrating DDR SDRAM devices "surface mounted" on both sides of a PCB in a DIMM format); Ex. 1071, 2:4–6 ("DIMM"); Ex. 1003 ¶ 278.

Because we agree with Petitioner's obviousness assertions and Patent Owner's admission that DDR2s would be in ranks, we need not address the parties' contentions whether Perego alone discloses ranks, including whether Perego's disclosure at column 15, lines 37–45 teaches ranks. *See* PO Resp. 35 (citing Ex. 2003, 202:8–202:10); *see also* Paper 35 (Petitioner's Motion to Exclude, 1 (seeking to exclude Exhibit 2003, 202:8–202:10)).

Patent Owner also argues that "it is not clear that any such rank would 'read or write the full bit-width of the memory module' as required by Petitioner's construction." PO Resp. 35 (citing Ex. 2024 ¶¶ 173–175). Dr. Przybylski explains that, "[i]f the Board finds that Figures 4A, 4B, and 4C show memory devices 410 that can be DDR2 SDRAMs as Petitioner asserts, then the rank elements of claim 1 of the '417 patent are still not present in Perego" because "the two interface units 520a and 520b operate together and so if indeed each of these collections offers a 64-bit data path to the buffer device, the structure that is disclosed is a 128-bit rank not two 64-bit ranks." Ex. 2024 ¶ 175.

Dr. Przybylski appears to be referring to Perego's disclosure of bandwidth concentration, which is described in the following passage:

> According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer). The concept of bandwidth concentration involves combining the (smaller) bandwidth of each channel in a multiple channel embodiment to match the (higher) overall bandwidth utilized in a smaller group of channels. This approach typically utilizes multiplexing and demultiplexing of throughput between the multiple channels and smaller group of channels. In an embodiment, buffer device 405 utilizes the combined bandwidth of interfaces 520a and 520b to match the bandwidth of interface 510.

Ex. 1071, 11:56–12:2. Perego further explains the bandwidth concentration embodiment as follows:

> Referring to FIG. 4B, buffer device 405 may operate in a bandwidth concentrator approach. By employing quad channels 415a 415d on each of modules 450a 450d, bandwidth in each module may be concentrated from all quad channels 415a 415d on each module to corresponding point-to-point links 620a 620d. In this embodiment, throughput on each of point-to-point links 620a 620d is concentrated to four times the throughput achieved on each of quad channels 415a 415d. Here, each of channels 415a 415d transfers information between one or more respective memory devices on each channel and buffer device 405 simultaneously.

Id. at 21:4–15.

We agree with Dr. Przybylski that Perego discloses that interface units 520a and 520b can operate together. The bandwidth concentration disclosure, however, is one embodiment, and Perego follows this disclosure by explaining that "[a]ny number of channels 415a 415d, for example; two

channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." Ex. 1071, 21:16–20. Thus, Perego's disclosure is not limited to the bandwidth concentration embodiment, as Patent Owner's arguments and Dr. Przybylski's testimony suggest.

Additionally, Perego discloses an embodiment in which "individual device select lines 633a and 633b are employed to perform device selection." Ex. 1071, 9:64–67. These are essentially chip select signals as required by the challenged claims.

Accordingly, based on the entirety of the trial record, we find that Perego teaches the required ranks and chip select signals.

g) Latency (1.e.1, 1.e.2, 1.e.3, 1.f)

Claim 1 recites

> circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module,
>
> wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

Petitioner argues that Perego discloses circuitry in the buffer devices of Figures 5A and 5B that is coupled between the data signal lines in the memory bus and corresponding data pins of memory devices in each of the ranks. Pet. 85–88 (citing Ex. 1071, 4:38–42, 6:12–15, 7:30–34, 10:59–67,

11:1–7, 13:6–10, 13:18–24, 14:65–15:2, 17:61–63, 18:65–19:3, Figs. 5A, 5B, 5C; Ex. 1003 ¶¶ 324–333). Petitioner argues that Perego's data bursts are routed through the buffer device between the targeted rank of memory and the memory controller and that a person of ordinary skill in the art would have understood that buffer control signals are used "to activate only the channel transferring the data burst between the memory controller and the targeted rank" and "to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operations." *Id.* at 90–91 (citing Ex. 1071, 6:15–25, 11:56–61, 12:9–12, 13:54–59, 14:62–15:6, 15:34–40, 17:41–44, 17:61–62, 21:16–20, Figs. 5A, 5B; Ex. 1003 ¶¶ 338–342).

As to the "CAS latency" recitations, Petitioner argues that the data are transferred according to an overall CAS latency of the memory module, citing Perego's disclosure of "access latency values" and JESD79-2's disclosure of CAS latency values. Pet. 92–94 (citing Ex. 1071, 12:20–34, Fig. 5B; Ex. 1064, 12, 14, 26, 28, Fig. 26; Ex. 1062, 68 n.1; Ex. 1003 ¶¶ 344–353). Petitioner argues that the data transfers in Perego are registered using latches 597f–m in Figure 5C. *Id.* at 95–96 (citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362). Petitioner also argues that, "[u]nder the JEDEC standards, 'an additional clock cycle' is added to the 'CAS latency' of the memory devices to leave enough time for the register on the memory module to perform its functions." *Id.* at 95 (citing Ex. 1062, 68 n.1; Ex. 1064, 12, 14; Ex. 1003 ¶¶ 359–362). Petitioner argues that it would have been obvious to a person of ordinary skill in the art to add an additional clock cycle in Perego "so that the memory module complies with the timing of the JEDEC standards, and

so the '*circuitry*' has enough time to perform its functions (including '*register[ing]*' the data signals for interfaces 520a/b with latches 597f-m . . .) using 'internal' clock circuit 570a-b." *Id.* (brackets by Petitioner; citing Ex. 1071, 12:65–13:5, 17:61–63, 18:65–19:3, Figs. 5B–5C; Ex. 1003 ¶¶ 359–362).

Patent Owner disputes Petitioner's contentions regarding the overall CAS latency. PO Resp. 36–39. We find Petitioner's contentions persuasive.

First, Perego discloses that "buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360." Ex. 1071, 6:12–15. This is similar to the '417 patent's disclosure "to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20." *Id.* at 22:46–49. Thus, Perego expressly discloses buffering data and its benefit—isolating the memory devices from the memory controller.

Second, the evidence shows that there would be some delay with a data buffer. *See* Ex. 1095, 132:20–133:6 (Dr. Przybylski's testimony that, with a buffer on the data line of a memory module, "[i]nevitably, there's some delay, depending on the type of buffer and its characteristics internally").

Third, a person of ordinary skill in the art would have understood that CAS latency is measured in clock cycles. *See* Ex. 1095, 251:20–252:7 (Dr. Przybylski's testimony, referring to Exhibit 1064, that "[in DDR2, the latency is measured in clock cycles"); *see also* Pet. 18 n.5 (Petitioner's citation to DDR2 RDIMM for whole clock cycle delays).

Patent Owner argues that Petitioner's contention about the data buffer necessarily adding delay "is an entirely new rationale, relying on new and different evidence, which is not permitted in Reply." PO Sur-reply 18. We disagree because for limitation 1.e.3 Petitioner contends that a person of ordinary skill in the art "would have understood that any scheduled data transfer to or from the memory module must account for the latency of the entire module . . . including the latency of the memory devices . . . combined with the latency added by the buffer device (e.g., 1 clock cycle for the buffer device . . .)." Pet. 94. Thus, the Petition sets forth Petitioner's contention that the buffer adds delay.

Accordingly, based on the entirety of the trial record, we agree with Petitioner and find that Perego teaches the coupled circuitry and CAS latency as recited by the challenged claim.

h) Objective evidence of non-obviousness

Patent Owner does not present objective evidence of non-obviousness other than to respond to Petitioner's assertion of evidence of "simultaneous invention." PO Resp. 55. As discussed, the combination of Perego and JESD79-2 teaches or renders obvious all of the limitations of claim 1, and there is no objective evidence of non-obviousness in the record.

i) Conclusion for Claim 1

We have considered the full trial record, and, for the reasons discussed above and based on Petitioner's contentions and evidence, we conclude that claim 1 would have been obvious to a person of ordinary skill in the art based on the combined teachings of Perego and JESD79-2.

3. Dependent Claims 2–15

Below we summarize Petitioner's contentions for claims 2–15, which Patent Owner does not dispute apart from its arguments for claim 1.

Claim 2 depends from claim 1 and recites "wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus." Petitioner argues that Perego's buffer device, and particularly latches 597f–m within the buffer device, isolate the load of the memory devices from the memory bus. Pet. 97 (citing Ex. 1071, 4:38–45, 6:12–15, 6:44–46, 17:61–63; Ex. 1003 ¶¶ 379–385); *see* Ex. 1071, 6:12–15 (disclosing that "buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360").

Claim 3 depends from claim 1 and recites "wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals." Petitioner argues that a person of ordinary skill in the art "would have understood from JESD79-2 that DDR2 memory devices transmit or receive data in 'bursts,'" which "are timed in accordance with latencies . . . so that the data communication between the memory controller and the memory module is properly synchronized." Pet. 98–100 (citing Ex. 1064, 12–14, 24–32; Ex. 1003 ¶¶ 386–394). Petitioner contends that it would have been obvious for the data buffer control signals to control the routing to comply with JESD79-2 timing. *Id.* at 98 (citing Ex. 1064, 12–14; Ex. 1003 ¶ 391).

Claim 4 depends from claim 1 and recites "wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs." Petitioner cites JESD79-2's disclosure of "x4" DDR2 memory devices and notes that 16 or 18 such devices would be used, respectively, for widths of 64 and 72 bits, the latter accounting for error correction. Pet. 100 (citing Ex. 1071, 10:48–53 (noting use of error correction code (ECC)); Ex. 1064, 7–8; Ex. 1062, 5–6, 15–16; Ex. 1066, 4, 6; Ex 1003 ¶¶ 395–400); *see* Ex. 1062, 5 (disclosing "DIMM organization" of "x72 ECC, x64").

Claim 5 depends from claim 1 and recites "wherein the memory devices are organized in four ranks and the set of input address and control signals include four chip select signals, one for each of the four ranks." Petitioner cites to its contentions for claim 1 and refers to Perego's Figure 4B showing "each memory interface 415a-415d can correspond to a single rank, and the set of input address and control signals include four chip select signals, one for each of the four ranks "consistent with the JEDEC standards." Pet. 101 (citing Ex. 1071, 64–73, 51–58; Ex. 1062, 6 ("Physical banks"); Ex. 1066, 6–7, 16–17; Ex. 1003 ¶¶ 401–406) (emphasis omitted).

Claim 6 depends from claim 1 and recites "wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry." Petitioner cites Perego's disclosure of a "scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections" (Ex. 1071, 18:49–54), and Petitioner argues that a person of ordinary skill in the art would have understood that such routing would "include '*logic pipelines*' to enable the '*data transfers*' through the

'*circuitry*,' all in response to control signals that enable the data transfer." Pet. 101–03 (citing Ex. 1064, 23–25, 49; Ex. 1071, 13:49–59, 17:22–18:9, 18:48–54, Figs. 5B, 5C; Ex. 1003 ¶¶ 407–415).

Claim 7 depends from claim 1 and recites "wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller." Petitioner argues that a person of ordinary skill in the art "would have been motivated to report latency parameters during initialization, including reporting '*the overall CAS latency*' of the module, 'to properly configure the memory devices upon boot of the system' and to ensure proper timing of commands from the memory controller." Pet. 104 (quoting Ex. 1071, 12:32–34; citing Ex. 1071, 12:20–27, 12:35–42, 12:45–50; Ex. 1003 ¶¶ 419–420, 422); *see* Ex. 1071, 12:20–23 ("A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, *access latency values*, vendor specific functions or calibration." (emphasis added)).

Claim 8 depends from claim 1 and recites "wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate." Petitioner argues Perego discloses that the same clock signals are used between the buffer and the memory devices as are used between the buffer and the memory controller and that a person of ordinary skill in the art would have understood that the same specified data rate is used on both of these interfaces of the buffer. Pet. 104–05 (citing Ex. 9:43–49, 10:5–13, Figs. 4A, 4B; Ex. 1003 ¶¶ 425–430).

Claim 9 recites, "The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined[10] amount of time delay is at least one clock cycle time delay." Petitioner argues that Perego's buffer device's clock circuit "implements the functionality of a 'PLL' driver to generate clock signals for the module, phase aligned with the clock signals received from the memory controller." Pet. 106–07 (citing Ex. 1071, 12:52–64; Ex. 1069, 11; Ex. 1073 ¶¶ 30, 48, Figs. 2–6, 10–13); *see* Ex. 1071, 12:52–55 ("Clock circuit 570a–b may include clock generator circuit (e.g., Direct Rambus[] Clock Generator), which may be incorporated onto buffer device 405 and thus may eliminate the need for a separate clock generating device."). For the delay being at least one clock cycle, Petitioner refers to its contentions for limitation 1.f. Pet. 106–07.

Claim 10 depends from claim 9 and recites

> wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

Petitioner argues that Perego's disclosure of using DDR2 SDRAM devices in combination with JESD79-2's disclosure that DDR2's transfer data on both edges of a complementary set of data strobes teaches this subject matter. Pet. 107–08 (citing Ex. 1071, 4:6–12, 10:58–59; Ex. 1060;

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[10] Claim limitation 1.f recites "an amount of delay," not a "predetermined amount of delay." Like Petitioner, we presume claim 9 refers to the "amount of delay" in claim 1. *See* Pet. 107 n.6.

Ex. 1064, 24–32; Ex. 1069; Ex. 1003 ¶¶ 438–441); *see* Ex. 1071, 4:6–12 (disclosing that a "memory device includes a transceiver for transmitting and receiving data" and that a "transceiver includes a transmitter circuit to output data synchronously with respect to rising and falling edges of a clock signal as well as a receiver circuit"), 10:56–59 (disclosing that DDR2 DRAMs and SDRAMs may be used on module 400).

Claim 11 depends from claim 1 and recites "wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths." Petitioner argues that Perego discloses data paths "for selectively coupling the memory bus, on one hand, to the rank of memory devices targeted by the buffer device for a read or write command, on the other hand," and Petitioner refers to its contentions for relevant limitations of claim 1. Pet. 108–10 (citing Ex. 1071, 15:34–37; Ex. 1003 ¶¶ 442–448).

Claim 12 depends from claim 11 and recites "wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry." Petitioner argues that this subject matter would have been obvious "to avoid collisions and save power, and because there is no reason to enable them." Pet. 110 (citing Ex. 1003 ¶¶ 449–452; Ex. 1071, 15:40–43, 21:16–28; Ex. 1068, 89–90, 132–33); *see* Ex. 1071, 16–20 (disclosing that memory devices can be "in a ready or standby state until called upon to perform memory access operations").

For claims 13, 14, and 15, each of which depends from claim 12, Petitioner refers to its contentions for claims 2, 8, and 3, respectively, which recite similar subject matter but are dependent from claim 1. Pet. 111.

Other than its arguments for independent claim 1, which we address above in § II.D.2, Patent Owner does not raise additional arguments for these claims. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware*, 800 F.3d at 1378. We have reviewed Petitioner's arguments and evidence, summarized above, and we find them persuasive. Therefore, having considered the full record developed during the trial, we conclude that claims 2–15 are unpatentable as having been obvious over the combined teachings of Perego and JESD79-2.

E. Remaining Challenges

Because we determine that all challenged claims are unpatentable as discussed above, we need not separately assess the challenges to patentability based on the combination of Perego, JESD79-2, and Ellsberry and the combination of Perego, JESD79-2, and Halbert. 35 U.S.C. § 318(a) ("If an inter partes review is instituted and not dismissed under this chapter, the Patent Trial and Appeal Board shall issue a final written decision with respect to the patentability of any patent claim challenged by the petitioner and any new claim added under section 316(d)."); *Bos. Sci. Scimed, Inc. v. Cook Grp. Inc.*, 809 F. App'x 984, 990 (Fed. Cir. 2020) (nonprecedential) ("We agree that the Board need not address issues that are not necessary to the resolution of the proceeding.").

III. PETITIONER'S MOTION TO EXCLUDE

Petitioner filed a Motion to Exclude Exhibit 2010 and portions of Exhibit 2003. Paper 35. Patent Owner relies on Exhibit 2010 to challenge Petitioner's combination of Perego and Ellsberry. PO Resp. 51; PO Sur-reply 24. We do not reach this ground and, therefore, do not rely on Exhibit 2010 in a manner adverse to Petitioner. We have considered the cited

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portions of Exhibit 2003 in our analysis above and do not rely on this testimony in a manner adverse to Petitioner.

Therefore, we dismiss the Motion to Exclude as moot.

IV. CONCLUSION[11]

For the reasons discussed above, we determine that Petitioner has proven, by a preponderance of the evidence, that claims 1–15 of the '417 patent are unpatentable, as summarized in the following table:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1–15	103(a)	Perego, JESD79-2	1–15	
1–15	103(a)	Perego, JESD79-2, Ellsberry[12]		
1–15	103(a)	Perego, JESD79-2, Halbert		
Overall Outcome			1–15	

[11] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

[12] As explained above, because we determine that the challenged claims are unpatentable based on the combination of Perego and JESD79-2, we decline to address the remaining grounds.

V. ORDER

Accordingly, it is

ORDERED that claims 1–15 of the ’417 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner’s Motion to Exclude (Paper 35) is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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