

Ultra Low-Supply Voltage Reference Generator

with Low Sensitivity to PVT Variations

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Abstract—Majority of trim-less PVT insensitive voltage reference generators are limited to minimum supply voltage above 0.7 V. This delimits use of energy harvesting techniques in CMOS circuits and systems. This paper proposes a low-cost CMOS voltage reference, which steps up the supply voltage by charge-pump based voltage booster. The raised voltage helps to drive a traditional parasitic BJT based bandgap voltage reference. The proposed voltage reference scheme is analyzed theoretically and compared with other methods. The circuit is designed and simulated in standard 180 nm mixed mode CMOS technology. The minimum required supply voltage is 400 mV. A worst case temperature coefficient of 4 ppm/°C is achieved over 0-100°C temperature range. The reference voltage exhibits mean value of 169.37 mV with worst case deviation of ± 1.35 mV across process corners and temperature range of 0-100°C. Achieved PSRR at 100 Hz and 1 MHz is -86 dB and -30 dB, respectively.

I. INTRODUCTION

Nowadays, energy harvesting from variety of resources available in the ambient is viewed as a practical approach for powering autonomous hand-held low-power systems [1][2]. On the other hand nanoscale CMOS technologies increase speed at the expense of increasing power density. To reduce power density of large digital ICs the supply voltage has been scaled down from 0.3 V to 0.5 V [3]. Combined growth in energy harvesting and CMOS technologies leads to applications such as self-powered sensor nodes which require ultra low voltage mixed-signal circuits [4]. Energy harvesting can also be used to empower applications such as picoradio and biomedical implantable devices [5]. For these autonomous systems to be successful, we need to develop a high-efficiency energy storage, power optimized circuits and robust power management systems.

Deployment of robust power management sub-system inherently requires PVT (Process, Supply voltage and Temperature) insensitive reference voltage circuit. However, reference voltage should be scaled down with supply voltage. Therefore, controlling deviation of reference voltage from its mean value due to process variations is becoming a concern.

Designing a process invariant voltage reference at low supply voltage is a challenge to many designers. To solve this problem Kinget et al. have proposed Schottky diode based approach, but it requires additional modifications in standard CMOS technology [6]. Annema demonstrated high performance references operating down to 0.85 V supply voltage, using Dynamic Threshold MOS Transistors (DTMOST) devices

[7]. Ugajin et al. presented a voltage reference circuit using enhancement and depletion mode devices in a process called fully depleted MOS/Separation by IMplantation of OXYgen (SIMOX) operating at a supply down to 0.6 V [8]. However, such designs are not compatible with standard CMOS technology. A specialized technique for realization of high precision reference voltage includes floating-gate design by Ahuja et al. [9]. However it requires special devices and each reference needs to be programmed after fabrication. Additionally, increasing gate leakage effects make such structures less compatible with nano scale CMOS processes. Jing et al. [10] and Seok et al. [11] designed voltage references with 0.5 V supply voltage in a standard CMOS technology, but the reported temperature coefficient (TC) is not convincing.

This paper presents a voltage reference circuit using standard CMOS technology. The proposed circuit steps up the supply voltage by connecting six stages of ‘voltage booster’ in series. Each voltage booster stage comprises of a charge-pump, analog multiplexer and low pass filter (LPF). The raised supply voltage becomes a driver for traditional parasitic bipolar junction transistor (BJT) based bandgap voltage reference. Section II illustrates the concept of the voltage reference circuit. Detailed discussion of circuit realization of the technique is mentioned in Section III. Experimental results are presented in Section IV. Section V presents comparison of the proposed architecture with recently published works. Section VI discusses the applicability of the technique. Finally, Section VII concludes the paper.

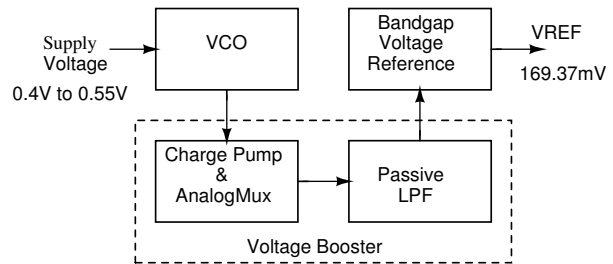


Fig. 1: Block diagram of proposed CMOS voltage reference architecture

II. PRINCIPLE OF OPERATION

In CMOS technology, a parasitic vertical BJT is often used in voltage reference circuits. These voltage references exhibit one of the best PVT insensitivities without any trimming network. For proper functionality of the reference circuit, it typically needs a supply voltage larger than 1.4 V. This requirement of supply voltage limits usage of BJT based voltage reference to low supply voltage regime. To solve this problem, we present a charge-pump based voltage boosting technique. Fig. 1 shows the block diagram of the proposed technique. VCO operates at ultra low supply voltage of 400 mV and its output is given to the rectifier and voltage booster. Output of voltage booster acts like a supply voltage for bandgap voltage reference.

VCO uses current starved topology for gaining power advantage over conventional VCO [12]. Process, temperature and supply voltage variations change the oscillation frequency, which changes only the settling time of the reference voltage without affecting the steady state reference value. In other words DC reference voltage is unchanged in-spice of PVT variations in the current starved VCO. This feature is discussed in Section IV.

III. CIRCUIT CONFIGURATION

The proposed architecture of voltage reference circuit is shown in Fig. 2.

A. Charge-pump based voltage booster

Charge-pump based voltage boosting is needed to raise the low input voltage (here VDD). Charge-pump circuit consists of two back to back source coupled NMOS transistors 'Mc1' and 'Mc2' with capacitors 'Cc' connected to source. These circuits are driven by inverted and non-inverted oscillator outputs. Two outputs of the charge pump are used as inputs as well as select lines for the analog multiplexer. Analog switches are designed with minimum size transistors to minimize charge injection effect. Passive resistor-capacitor based LPF is used with cut-off frequency much less than the oscillator frequency to produce

ripple free supply voltage of bandgap reference circuit (node Vx in Fig. 2.)

B. Bandgap Voltage Reference

The principle of the bandgap voltage reference is to balance the negative TC (temperature coefficient) of a PN junction with the positive TC of the thermal voltage $V_T = kT/q$. Due to process, voltage and temperature variations, voltage at node 'Vx' i.e. supply node for bandgap reference circuit (Fig. 2) varies significantly. The AC component of 'Vx' is due to non-zero cut-off frequency of LPF and its limited roll off. The effect of AC voltage on reference voltage is minimized by designing the circuit for high PSRR. Since DC component of 'Vx' also varies, the reference voltage circuit must also have a good line insensitivity.

Sub-1V bandgap voltage reference is shown in Fig. 2. BJTs are suitable devices for achieving process insensitive reference generator based on bandgap voltage. 'ME' and 'MF' are identical in area with equal gate voltages and drain voltages. The latter is forced by the operational amplifier. Operational amplifier comprises of MOSFETs 'Ma' to 'Md' i.e. tail transistor-less op-amp (operational-amplifier) [12]. The voltage difference between two pn junctions of BJTs, operated at different current densities, is used to generate a proportional to absolute temperature (PTAT) current in resistor 'R3'. The base-emitter voltages of BJTs are complementary to absolute temperature (CTAT) and hence the current flowing through 'R1' and 'R2' is also CTAT. Op-amp gain is large enough to ensure that the two currents 'IE' and 'IF' are identical. Considering 'R1'='R2', then the currents 'IE' and 'IF' are given by

$$IE = IF = \frac{V_T \ln(N)}{R3} + \frac{V_{BE}(1)}{R1} \quad (1)$$

Current 'IE' is mirrored and passed through resistor 'R4'. It gives reference voltage as given below,

$$V_{REF} = \frac{R4}{R3} \cdot V_T \ln(N) + \frac{R4}{R1} \cdot V_{BE}(1) \quad (2)$$

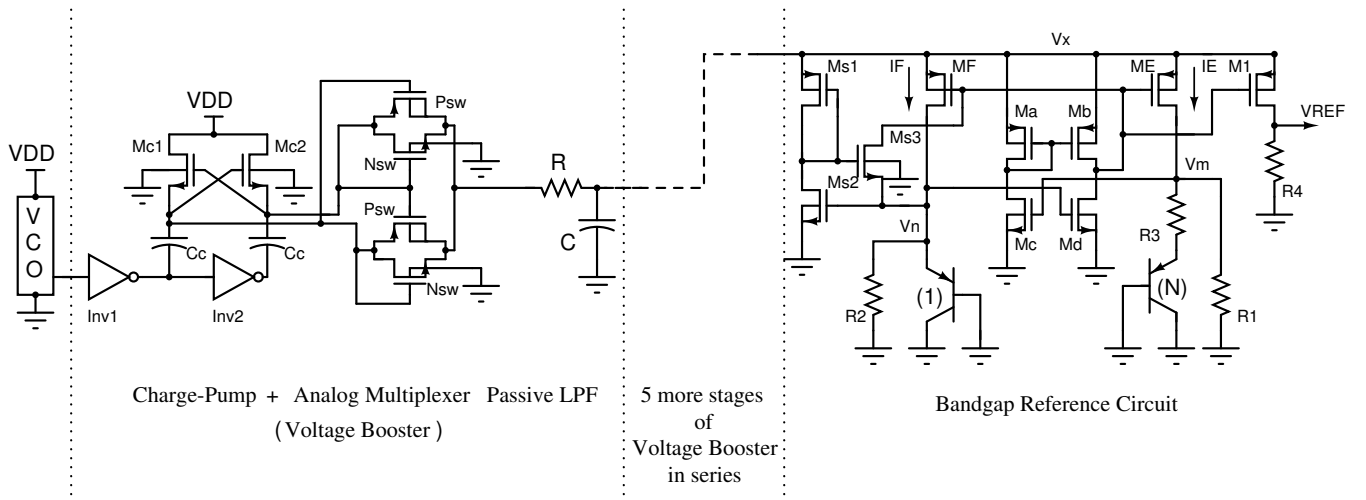


Fig. 2: CMOS voltage reference architecture

Ratios of resistors is chosen in such a way that the first order effects of the temperature dependency of reference voltage are cancelled out. Moreover, resistor ratios ensure a process insensitive behavior of the reference voltage.

IV. SIMULATION RESULTS

The voltage reference has been designed in standard 180nm mixed mode CMOS process and simulated using Spectre using foundry models. The voltage reference maximally deviates from its mean value in slow-slow (SS) and fast-fast (FF) corners for MOSFETs and min-max corners for poly resistors. Fig. 3 and Fig. 4 display the value of reference voltage after turning power on at two extremes of operating temperatures i.e. 0°C and 100°C, respectively. Fig. 3 and Fig. 4 also indicate the difference in settling time for stabilizing the reference voltage. This is due to deviation of oscillation frequency of VCO with the process. VCO oscillates at its minimum frequency at SS process corner with resistor-Min at 0°C operating temperature. This corner leads to maximum settling time of charge pump output and reference voltage. Reference

voltage values reported in Fig. 3 and Fig. 4 confirm that the maximum deviation is only ± 1.35 mV from mean reference voltage across all the process corners. Fig. 5.A shows variation of optimized voltage reference at TT process corner over temperature range of 0°C to 100°C for a low supply of 400 mV. As shown in the figure the mean reference voltage of 169.37 mV with total variation of 68 μ V is achieved. The dependency of reference voltage on temperature, i.e. TC, is 4 ppm/°C. Fig. 5.B presents the power supply rejection ratio (PSRR) of the reference generator. Achieved PSRR without any filtering capacitor is -86 dB and -30 dB at 100 Hz and 1 MHz, respectively at TT process corner and 50°C temperature. Same set of experiments has been performed for supply voltage of 550 mV. The results are quite identical to the results obtained with supply voltage of 400 mV.

V. COMPARISON

Only standard CMOS process implementations are considered for comparison. There is a trade off between the reference voltage value and the reference voltage TC (Table I). Our

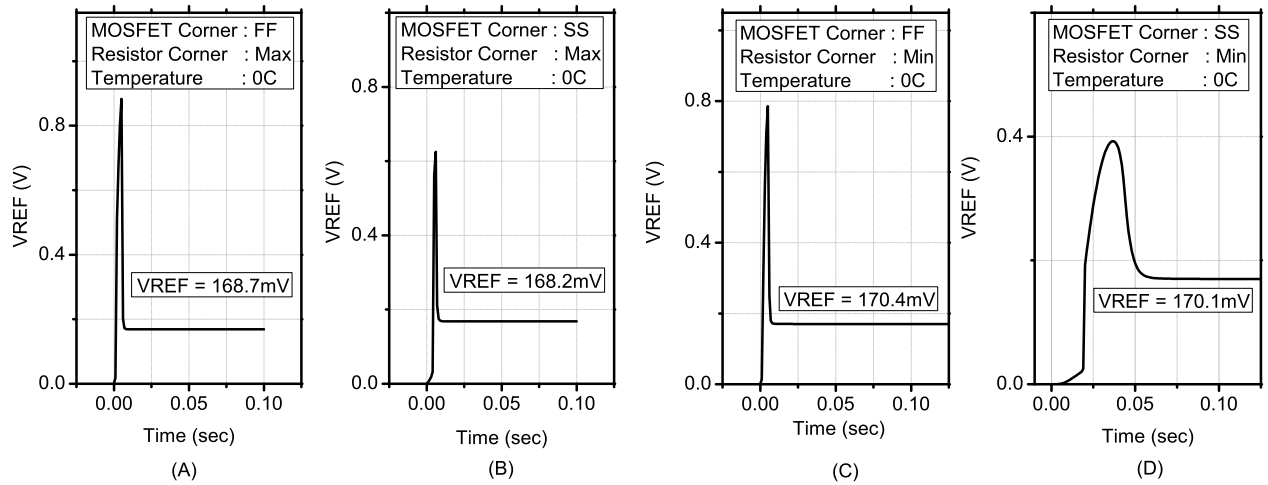


Fig. 3: Reference voltage for 400 mV supply voltage and 0°C temperature

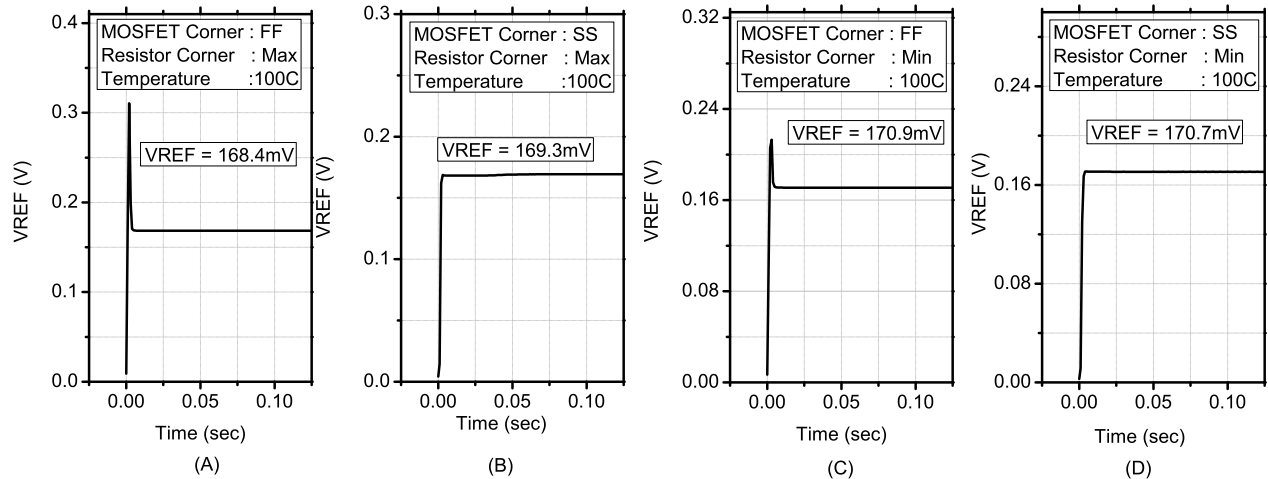


Fig. 4: Reference voltage for 400 mV supply voltage and 100°C temperature

TABLE I: Performance Comparison

Parameter	This Work	Ref.[13]	Ref.[10]	Ref.[14]	Ref.[11]	Ref.[6]	Ref.[15]
Technology (μm)	0.18	0.13	0.13	0.13	0.13	0.09	0.35
VDD (V)	0.4-0.55	0.75	0.5-1.2	0.7-1.8	0.5-3.3	0.5-1.0	0.9-2.5
V_{REF} (mV)	169.37	256	85.5	502	175.5	241.5	190.1
TC (ppm/ $^{\circ}\text{C}$)	4 [0:100]	40 [-20:85]	52.5 [0:100]	29.3 [-50:130]	19.4 [-20:80]	160 [5:100]	16.9 [-20:120]
PSRR $\leq 100\text{Hz}$ (dB)	-86.35	-70	-70.41	-	-70	-	-41
@1MHz (dB)	-30.26	-67	-98	-	-67	-	-28
Worst Case							
ΔV_{REF} (mV)	$\pm 1.35@15$ corners	-	$\pm 1.6@3$ corners	-	-	$\pm 4.25@16$ Samples	-
Power	4.75 μW	0.17 μW	1.5 nW	0.21 μW	2.2 pW	547 μW	0.25 μW

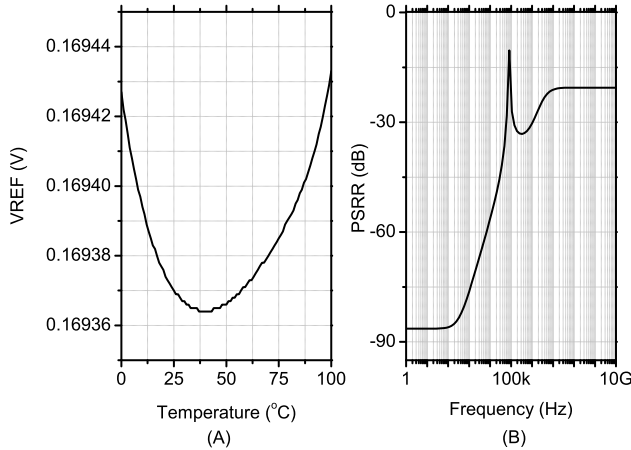


Fig. 5: (A) Reference voltage vs temperature @ TT corner, supply voltage = 400 mV (B) PSRR @ TT corner, supply voltage = 0.4 V and Temperature = 50 $^{\circ}\text{C}$

topology achieves lower TC for a lower value of reference voltage. The low frequency PSRR is almost identical to the mentioned architectures. Minimum workable supply voltage is lowest among the mentioned topologies. But, maximum value of workable supply voltage is also lower. The limitation on upper value of supply voltage is implied by the charge-pump. Charge pump boosts supply voltage value beyond 3.3 V for VDD higher than 0.55 V. The area of this architecture is more due to presence of lower cut-off frequency of low pass filter.

VI. DISCUSSION

The trim-less PVT voltage reference is accurate as well as functions efficiently with low supply voltage. Self-powered energy-harvesting systems which are used for applications like wireless sensors and biomedical implants can use our topology for generating precise voltage reference. Moreover, trim-less feature of designed voltage reference reduces product cost in terms of silicon and time to market. To reduce the effect of mismatch on reference voltage larger size transistors are used in design.

VII. CONCLUSION

In this paper, ultra low voltage and PVT insensitive CMOS voltage reference is proposed and simulated. The simulation is performed with standard 180 nm mixed mode CMOS process.

A ± 1.35 mV variation in reference voltage is achieved across corners and supply voltage range of 0.4 V to 0.55 V, over 0-100 $^{\circ}\text{C}$ temperature. Simulation results show that the presented voltage reference circuit provides a precise reference voltage with high PSRR response.

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