

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, DC**

**Before The Honorable MaryJoan McNamara
Administrative Law Judge**

In the Matter of

**CERTAIN DYNAMIC RANDOM ACCESS
MEMORY (DRAM) DEVICES,
PRODUCTS CONTAINING THE SAME,
AND COMPONENTS THEREOF**

Investigation No. 337-TA-1472

**SAMSUNG RESPONDENTS' SECOND SUPPLEMENTAL
OBJECTIONS AND RESPONSES TO COMPLAINANT
NESTLIST INC.'S FIRST SET OF INTERROGATORIES (NOS. 1-38)**

Pursuant to the United States International Trade Commission's Rules of Practice and Procedure, 19 C.F.R. §§ 210.27 and 210.29, and the ALJ's Ground Rules (Order No. 2), Respondents Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively, "Samsung" or "Respondents"), by counsel, hereby submit their second supplemental responses and objections to Complainant Netlist, Inc.'s ("Netlist's" or "Complainant's") First Set of Interrogatories (Nos. 1-38) to Samsung. As Samsung's investigation in this matter is continuing, Samsung reserves the right to amend and/or supplement these responses in accordance with the Commission's Rules, the Ground Rules, and the Procedural Schedule.

GENERAL STATEMENT AND OBJECTIONS

The Responses and Objections provided here are submitted on behalf of Samsung and reflect Samsung's continuing investigation of facts and discovery of information and documents relating to the claims and defenses at issue in this Investigation. Accordingly, Samsung's responses to these Interrogatories are based only upon Samsung's current knowledge and reasonable belief.

Netlist EX2132
Samsung v. Netlist
IPR2025-01431

[illegible]

INTERROGATORY NO. 32:

RESPONSE TO INTERROGATORY NO. 32 (JANUARY 22, 2026):

In addition to and without limiting the foregoing General Objections, which are incorporated by reference as though fully set forth herein, Samsung objects to this Interrogatory to the extent it seeks information protected from discovery by the attorney-client privilege, attorney work product doctrine, or any other applicable privilege or immunity. Samsung objects to this Interrogatory to the extent it requires legal conclusions and/or expert analysis regarding interpretation of claim terms and characterization of the accused products, features, and/or functionalities. Samsung objects to this Interrogatory to the extent it seeks premature disclosure of expert opinions or contentions, in advance of the date when such disclosure is required by any Procedural Schedule entered in this Investigation. Samsung further objects to this Interrogatory to the extent it seeks Samsung's contentions in a specific format.

Subject to and without waiving any general or specific objections, Samsung responds as follows: Samsung will provide its contentions responsive to this Interrogatory on a date to be agreed between the parties for exchange of contentions.

Samsung states that it is continuing to investigate the subject matter of this Interrogatory and reserves the right to supplement its response to the extent it locates any non-privileged, relevant documents or information responsive to this Interrogatory in accordance with the procedures and timetables established by the Commission's Rules of Practice and Procedure, the Ground Rules, and the Procedural Schedule entered in this Investigation, and after Samsung has been afforded an adequate opportunity to investigate Complainant's allegations through discovery in this Investigation.

[REDACTED]

FIRST SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 32 (MARCH 25, 2026):

Subject to and without waiving the specific objections and general objections, Samsung responds as follows:

Netlist has accused hundreds of Samsung products of infringement. *See* Samsung's Resp. to Interrogs. Nos. 1, 12 (Mar. 25, 2026). To the extent Netlist arguably presents evidence specific to one Samsung product, its deficient contentions fail to show that the allegations and cited evidence are applicable to any other Accused Product(s) or that any one product is representative of any other Accused Product(s).

Samsung's investigation is ongoing, and Samsung reserves the right to further supplement its response to this Interrogatory as discovery progresses.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[illegible]

5. '731 Patent

The Accused Products do not infringe the asserted claims of the '731 Patent (claims 1-3 and 6-18) for at least the reasons explained below. Netlist's contentions are deficient, and Netlist has not demonstrated that any Accused Products practice the asserted claims of the '731 Patent.

Nor has Netlist shown that any asserted claim is infringed under the doctrine of equivalents. Netlist's contentions regarding infringement under the doctrine of equivalents consist of a bare recitation of the legal test for the doctrine of equivalents. *See, e.g.*, '731 Chart at 55. Nor has Netlist shown that Samsung has indirectly infringed any asserted claim of the '731 Patent, either contributorily or through inducement. Netlist's contentions regarding indirect infringement consist of a bare recitation of the legal test for contributory infringement and inducement. *See* '731 Chart at 1. Samsung reserves all rights to respond to any updates by Netlist that purport to identify hardware that allegedly implements one or more limitations of the asserted claims of the 731 Patent or otherwise purport to change or clarify any of Netlist's infringement contentions.

(a) Claim 1

The Accused Products do not infringe claim 1 of the '731 Patent. For example, the Accused Products with a single-memory rank—including without limitation M321R2GA3EB0, M321R2GA3EB2, M321R2GA3PB0, M321R2GA3PB2, M321R3GA3PB0, M321R4GA0EB0, M321R4GA0EB2, M321R4GA0PB0, M321R4GA0PB2, M321R6GA0PB0, M321R6GA0PB2, M323R1GB4PB0, M323R2GA3EB0, M323R2GA3PB0, M324R2GA3PB0, M425R1GB4PB0, M425R2GA3EB0, M425R2GA3PB0, and M426R2GA3PB0—do not include “a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.” Netlist acknowledges that “[a]s stated on Samsung's web site, Samsung supports ‘up to 2 ranks per DIMM’ for its DDR5 SDRAMs.” '731 Chart at 83 (citing NETLIST-ITC-0069523 at -525). Therefore, the Accused Products that only have a single rank of memory devices do not have “multiple ranks.”

For those Accused Products that only have a single rank of memory devices, Netlist contends that because “DDR5 modules have also adopted a dual channel configuration, each channel having its own independent set of control/address signals and data/strobe signals,” ’731 Chart at 83, “the SDRAMs in what Samsung calls a ‘rank’ may also be viewed as consisting of two independent groups” that “may also be viewed as meeting the traditional definition of a ‘rank,’” *id.* at 85-86. A subchannel does not meet the plain and ordinary meaning of “rank.” Consistent with plain and ordinary meaning, the ’731 Patent explains that a rank “can be accessed by the memory controller to access the full bit-width of the memory bus of the memory module.” ’731 Patent at 6:3-5; *see also* IPR2025-01431, Paper No. 1 (Petition) at 7 (“In JEDEC-style memory systems, a ‘rank’ (sometimes called a ‘bank’) is an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module.”). For instance, if the full bit-width of the memory bus is 64 bits (x64), then each “rank” must be 64 bits wide. *See* ’731 Patent at 6:5-7. Netlist’s infringement contentions are contrary to the plain and ordinary meaning, alleging, for instance, that “ranks” can be 32 bits wide when the “full bit-width of the memory bus of the memory module” is 64 bits wide. *See, e.g.,* ’731 Chart at 84-85 (citing NETLIST-ITC-0067149 at -150 (“DDR5 splits the memory module into two independent 32-bit addressable subchannels . . . The data width of the DDR5 module is still 64-bit.”)). Indeed, documents Netlist cites from Samsung, Renesas, Rambus, and Montage consistently use the term “channel” or “subchannel” to refer to something distinct from “rank.” *See* ’731 Chart at 83-85.

Regardless of Netlist’s proffered “traditional definition,” each subchannel does not “comprise[] an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.” Netlist contends that “if each

communication channel is considered to be x32-x40 (*i.e.*, the width of channel A and channel B), then a group of devices corresponding to a channel as described above is accessed by the system memory controller to access the x32-x40 width of the memory bus.” ’731 Chart at 86. But as Netlist states, “a memory bus ‘refers to the data pathway between the central processing unit (CPU) and the computer’s main memory (RAM).’” ’731 Chart at 86. And the “width of the data bus” is measured by “how much data can be transferred in a single operation,” NETLIST-ITC-0062014 at -2019, not how much data can be accessed by some subset of memory devices. In other words, a “memory bus” with “a full bit-width” of 64 bits (*i.e.*, x64) does not become a “memory bus” with “a full bit-width” of 32 bits (*i.e.*, x32) by virtue of using a dual-channel configuration. *See* ’731 Chart at 83-84 (citing NETLIST-ITC-0061564 at -573 (acknowledging that “the data width is the same (64-bits total) even when there are two subchannels)). This is confirmed by Samsung’s datasheets. *See, e.g.*, NETLIST-ITC-0069421 at -442-45 (describing a dual-channel configuration where each subchannel comprises 40 bits as an “x80 DIMM” “[p]opulated as 1rank”).

Further for example, the Accused Products do not include “at least one circuit coupled between the at least one connector and the plurality of memory devices.” Netlist contends that “the plurality of memory devices” are “the memory cores of DDR5 SDRAMs devices.” ’731 Chart at 90. However, the plain and ordinary meaning of “memory devices,” confirmed by the ’731 Patent specification, is the entire physical SDRAM chip, not some undefined “memory core” sub-circuitry therein. *See also*, IPR2025-01431, Paper No. 1 (Petition) at 62-64 (discussing “a plurality of memory devices”). For instance, the ’731 Patent explains that “[m]emory devices compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro[] BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). ’731 Patent at 7:4-9. “Memory

[REDACTED]

devices” are physical SDRAM packages, not sub-circuitry within SDRAM packages. Furthermore, the ’731 Patent describes “memory devices” as being “mounted on the PCB,” ’731 Patent at 10:26-27, further confirming the “memory devices” are physical packages. Internal sub-circuits are not “mounted on the PCB.” Under the proper understanding of “memory devices,” the alleged “at least one circuit” resides on “the plurality of memory devices,” because the accused ODT and/or DFE circuits are located on the SDRAM chips. Therefore, the “at least one circuit” is not “coupled between the at least one connector and the plurality of memory devices.” *See, e.g.,* Samsung_1472_00532209 (Samsung SODIMM Datasheet) at -236 (showing [REDACTED] [REDACTED]); Samsung_1472_00532301 (Samsung UDIMM Datasheet) at -328 (same); Samsung_1472_00533229 (Samsung RDIMM Datasheet) at -270 (same); Samsung_1472_00533823 (Samsung MRDIMM Datasheet) at -855 (same). Netlist also takes an inconsistent position in its infringement contentions for the ’366 Patent. Specifically, for the claim limitation “a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices,” Netlist points to the entire SDRAM chip. *See* ’366 Chart at 190-91 (citing NETLIST-ITC-0069421 at Figs. 10 and 17).

Further for example, the Accused Products do not include “at least one circuit coupled between the at least one connector and the plurality of memory devices, the at least one circuit comprising a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices.” Netlist points to multiple, independent circuits that each connect to a single DRAM, not all the DRAMs as required by the claims. *See* ’731 Chart at 111.

[REDACTED]

Netlist also contends that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]. But any circuitry on the RCD or MRCD does not also “further compris[e] a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections.” Data signals do not pass through RCDs or MRCDs, and therefore those components do not make corrections in such “signals transmitted.” *See, e.g.,* ’731 Patent at 7:42-44 (“The bi-directional ports correspond to the data signal ports, for example, of the plurality of memory devices.”) and 8:39-43 (“In certain embodiments, the switching sub-circuit can pass signals (e.g., information such as the data signals described above) from one port of the second set of ports to an operatively coupled port of the first seat of ports and vice versa.”).

Further for example, the Accused Products do not include “a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices.” First, Netlist alleges that “data ports on the host side” are “a first set of port connections” that are “coupled to respective ones of the plurality of edge connections.” ’731 Chart at 110. Netlist points to schematics allegedly showing DRAM pins. *See* ’731 Chart at 112-17 (citing SAMSUNG_1472_00458230 at -232, 236, 238). However, Netlist does not specify whether the alleged “first set of port connections” labeled in its illustration, *see* ’731 Chart at 111, are the DRAM pins in the schematics, or some other alleged nodes in between the DRAM pins and “the least one circuit.” Second, Netlist alleges that “data ports on the DRAM side” are “a second set of port connections,” and points to “Samsung technical documents

[REDACTED]

show[ing] [REDACTED]

[REDACTED] '731 Chart at 112-17 (citing SAMSUNG_1472_00458230 at -232, -236, -238). For Accused Products without RCDs, Netlist similarly points to Samsung schematics allegedly showing [REDACTED]

[REDACTED] '731 Chart at 117 (citing SAMSUNG_1472_00458259 and SAMSUNG_1472_00458248). But as discussed above, Netlist contends “the plurality of memory devices” are “memory cores” of the DRAMs, not the DRAMs themselves. Thus, the alleged port connections, if they exist, must be internal to the DRAM under Netlist’s infringement theory. Therefore, any alleged pin connections on the DRAM package itself cannot be “a second set of port connections coupled to the plurality of memory devices” under Netlist’s infringement theory.

Further for example, Netlist accuses DFE circuits as being “a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between” certain “port connections,” and further “including at least one programmable impedance matching circuit.” '731 Chart at 152 (alleging “[e]ach correction circuit includes the DFE equalization circuitry to make corrections to one input signal on one DQ pin and the programmable RTT connected to DQ line”). However, DFE circuits do not perform impedance matching at least because they operate to reduce inter-symbol interference by subtracting known values of previous channel outputs to estimate present channel outputs, not by performing impedance matching. *See, e.g.,* '731 Chart at 125-28 (citing SAMSUNG_1472_00509877 at 44-45, 51 ([REDACTED])).

Further for example, the Accused Products do not include “control circuitry configured to receive the address and control signals from the system memory controller and to control the

[REDACTED]

plurality of memory devices in response to the address and control signals.” Netlist accuses the RCD or MRCD as controlling the plurality of memory devices in response to the address and control signals as claimed. *See*, Chart at 168. But RCDs and MRCDs do not perform a control function. [REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]); *compare to* IPR2025-01431, Paper No. 1 (Petition) at 39-41 and 73-74 (discussing “control circuitry”). This language tracks that used by the JEDEC standard for DDR5 RCDs (JEDEC Standard No. 82-511). *See* Samsung_1472_00550265 at -287. Indeed, Netlist points to, for instance, a “Samsung technical document showing and describing [REDACTED]

[REDACTED]

[REDACTED]’731 Chart at 169 (citing SAMSUNG_1472_00509823 at 3). Netlist also points to documentation from third-party RCD suppliers, such as Renesas, which use similar language to describe [REDACTED]. *See, e.g.*, ’731 Chart at 193-94 (citing NETLIST-ITC-0062600 at -601 regarding Renesas RCD) and 198 (citing RENESAS_NETLIST000542 at -542 regarding Renesas MRCD). Netlist itself characterizes the role of the RCD as “transmitting corresponding QCA signals to the DRAM.” ’731 Chart at 168.

For Accused Products without RCDs or MRCDs, Netlist accuses “the control/address circuit on SDRAMs” as meeting this limitation. ’731 Chart at 168. But the SDRAMs in the Accused Products are controlled by the system memory controller. *See, e.g.*,

[REDACTED]

Samsung_1472_00531272 (Samsung SODIMM Datasheet) at -278-79 (showing [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]); Samsung_1472_00531355 (Samsung UDIMM Datasheet) at -360-361 (same). In support, Netlist points to Samsung SODIMM and UDIMM datasheets that allegedly show [REDACTED]

[REDACTED] '731 Chart at 176-77. Netlist contends that “the control and address signals received from the memory controller, whether transmitted via RCD or directly, are received by the control/address signal input circuit of an SDRAM on the memory module.” '731 Chart at 214. Netlist further contends that “[i]n either case . . . the C/A and CS signals received by the memory device control the operation of the memory device.” '731 Chart at 215. Merely “receiving” control/address and chip select signals does not constitute “control” over the “plurality of memory devices in response to the address and control signals.” Rather, as Netlist itself contends, it is the address and control signals that “control the operation of the memory device.” '731 Chart at 215. Those address and control signals are generated by the system memory controller, not by any “control circuitry” on the Accused Products.

Further, for example, the Accused Products do not include “control circuitry . . . wherein the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals.” Claim 1 of the '731 Patent requires that this “dynamic[] control” of the “programmable impedance matching circuit[s]” be exercised by the same “control circuitry” discussed above with respect to controlling “the plurality of memory

[REDACTED]

devices in response to the address and control signals.” Therefore, Netlist must show that the “dynamic[] control” is performed by “the control/address circuit on SDRAMs and where available, the RCD or MRCD” under the infringement theory identified in its operative infringement contentions. *See* ’731 Chart at 168. But Netlist has failed to show the existence of any “control circuitry” on any of the Accused Products “configured to dynamically control the at least one programmable impedance matching circuit,” let alone “based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals.” In support, Netlist contends that “dynamic configuration is . . . facilitated based on CA/CS/CK signals sent from the RCD to the DRAMs corresponding to a specific rank, subchannel, or combination thereof.” ’731 Chart at 222-223. As discussed above, the RCD’s role is to buffer these signals received from the off-DIMM system memory controller. Therefore, the RCD is not configured “to dynamically control” any impedance matching circuits. Moreover, Netlist acknowledges that “in DDR5 systems, ODT control is encoded into the CS signal received from the memory controller to target a specific rank on the DDR5 DIMMs.” ’731 Chart at 227. In other words, the alleged “programmable impedance matching circuit[s]” are allegedly “dynamically control[led]” by the system memory controller, which is not part of the Accused Products. *See* ’731 Chart at 103-104 (citing SAMSUNG_1472_00464586 at -617-18 [REDACTED]).

[REDACTED]

[REDACTED]).

Netlist contends that “the RCD together with the command decoding and control circuitry on the SDRAMs (an example of a control circuitry) controls the operation of the SDRAMs, including affecting the value of the RTT for the specific rank.” ’731 Chart at 227-28. However, even under Netlist’s own infringement theory, this circuitry only “decode[s] the input

[REDACTED]

control/address signals,” “output[s] two copies,” and “direct[s] the two copies of the C/A and C/S outputs to the respective memory devices.” ’731 Chart at 227. Netlist fails to show how decoding and transmitting signals received from the system memory controller constitutes “control,” let alone “dynamic[] control” “based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals.”

Furthermore, the alleged “ranks” are not “selected to communicate data with the system memory controller in response to the address and control signals.” For example, the alleged “ranks” are not selected in response to address signals. *See, e.g., Samsung_1472_00532118* at - 126 [REDACTED]

[REDACTED]

(b) Claim 2

The Accused Products do not infringe claim 2 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 2 depends from claim 1 and the Accused Products do not infringe claim 2 at least for the same reasons that they do not infringe claim 1.

(c) Claim 3

The Accused Products do not infringe claim 3 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 3 depends from claim 1 and the Accused Products do not infringe claim 3 at least for the same reasons that they do not infringe claim 1.

(d) Claim 6

The Accused Products do not infringe claim 6 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim

[REDACTED]

6 depends from claim 1 and the Accused Products do not infringe claim 6 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any Accused Products that “the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit further includes a delay circuit that is configured to generate delayed versions of the signals transmitted between the respective port connection of the first set of port connections and the corresponding port connection in the second set of port connections.” Netlist contends “the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes a DFE circuit associated with a DQ line.” ’731 Chart at 276. Yet, Netlist points to “Samsung technical documents [that purportedly] show and describe [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Netlist also fails to show that the accused “DFE circuit associated with a DQ line” meets the requirements of claim 6 in any of the Accused Products, citing instead to an Intel document discussing decision feedback equalization and a web article published on “allaboutcircuits.com.” ’731 Chart at 290-91 (citing NETLIST-ITC-0062649 and NETLIST-ITC-0061518).

(e) Claim 7

The Accused Products do not infringe claim 7 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 7 depends from claim 1 and the Accused Products do not infringe claim 7 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any Accused Products that “the number of port connections in the first set of port connections corresponds to a bit width of the memory bus.” For instance, Netlist contends that “the number of DQ port connections in the first set of port connections correspond to 32 or 36 bits for each subchannel in a SODIMM/UDIMM” and “36 or 40 bits for each subchannel in an RDIMM or MRDIMM.” ’731 Chart at 301. For the same reasons discussed previously for claim 1, the number of bits in a subchannel does not correspond to the “bit width of the memory bus.” As such, Netlist fails to show that single-rank Accused Products practice the additional limitations of claim 7.

(f) Claim 8

The Accused Products do not infringe claim 8 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 8 depends from claim 1 and the Accused Products do not infringe claim 8 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the at least one circuit comprises multiple physically separate integrated circuit packages each having a data width corresponding to a data width of one of the plurality of memory devices.” For instance, as discussed previously, Netlist contends that the “at least one circuit” comprises ODT circuitry on each SDRAM chip. Therefore, the alleged “at least one circuit” does not comprise “physically separate integrated circuit packages,” as the “at least one circuit” is built into the SDRAM chip packages.

(g) Claim 9

The Accused Products do not infringe claim 9 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim

9 depends from claim 1 and the Accused Products do not infringe claim 9 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the at least one circuit comprises multiple physically separate integrated circuit packages.” For the same reasons discussed with respect to claim 8, the alleged “at least one circuit” does not comprise “physically separate integrated circuit packages,” as the “at least one circuit” is built into the SDRAM chip packages.

Further for example, Netlist has not shown for any of the Accused Products that the alleged “multiple physically separate integrated circuit packages each ha[s] a data width corresponding to a data width of multiple memory devices of the plurality of memory devices.” Under its analysis of claim 8, Netlist contends that the “data width of one of the plurality of memory devices” corresponds to the bit width of the SDRAM package. *See* ’731 Chart at 307 (“Each of the physically separate IC packages has a data width . . . that corresponds to a data width of the memory device within the package (x4, x8 or x16 respectively).”). But under claim 9, Netlist takes the inconsistent position that the same alleged “multiple physically separated integrated circuit packages” of claim 8 also have data widths that “correspond[] to a data width of the multiple memory devices within the package (also x4 or x8 respectively), because the data width of the package is the same as the data width of each of the memory device in the package.” ’731 Chart at 311. But claim 9 does not claim a package having a data width corresponding to each memory device, it claims a package “having a data width corresponding to a data width of multiple memory devices.” In other words, the data width of the package must correspond to the sum of the data widths of the “multiple memory devices.” Notably, Netlist takes the sum of the bit-widths of the “multiple memory devices” when analyzing MDBs under this claim. *See* ’731 Chart at 312 (“When

[REDACTED]

the MDBs each interface with x4 DDR5 memory devices, the physically separate IC packages for the 10 MDBs each have a x8 data width corresponding to a data width of multiple memory devices (e.g., two x4 DDR5 memory devices) of the plurality of memory devices.”).

(h) Claim 10

The Accused Products do not infringe claim 10 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 10 depends from claim 1 and the Accused Products do not infringe claim 10 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the control circuitry is configured to activate signal paths in the each circuit of the at least one circuit in response to the address and control signals.” Netlist points to the same “control circuitry” previously discussed and contends that “DQ signal paths and the corresponding DFE and ODT/RTT circuits for memory operations are activated if the value of the [chip select] signal is low.” '731 Chart at 314. However, Netlist does not explain how allegations that chip select signals activate signal paths shows that the alleged “control circuitry” (i.e., “the control/address circuit on SDRAMs and where available, the RCD or MRCD”) also activates signal paths. As discussed previously with respect to claim 1 (incorporated herein by reference), and as outlined in Netlist’s analysis of claim 10, RCDs buffer the chip select signals that are received from the host controller. *See, e.g.*, '731 Chart at 317-18 (citing SAMSUNG_1472_00509823 at 3). Therefore, the host controller is configured “to activate signal paths,” not the alleged “control circuitry.” The foregoing similarly applies to Netlist’s contentions that DIMMs without RCDs or MRCDs allegedly infringe claim 10.

Netlist also contends that “the direction of the data flow, and hence the activation and deactivation of Rx versus Tx of the DQ signal paths will depend on whether the memory operation

[REDACTED]

is a read or write operation, which are in response to the address and control signals.” ’731 Chart at 336. As just discussed, Netlist does not explain how allegations that address and control signals activate signal paths shows that the alleged “control circuitry” (i.e., “the control/address circuit on SDRAMs and where available, the RCD or MRCD”) also activates signal paths. Rather, because address and control signals are controlled by the host controller, at most the host controller is configured “to activate signal paths,” not the alleged “control circuitry.”

Furthermore, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Netlist alleges that “the direction of the data flow . . . will depend on whether the memory operation is a read or write operation, which are in response to the address and control signals.” ’731 Chart at 336-37 (citing NETLIST-ITC-0061561 at -562). However, [REDACTED]

[REDACTED]

[REDACTED].

(i) Claim 11

The Accused Products do not infringe claim 11 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 11 depends from claim 1 and the Accused Products do not infringe claim 11 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the control circuitry is configured to send at least one control signal to the at least one circuit in response to the address and control signals.” Netlist contends that “[t]he output address/control

decoder on the SDRAM provides input to various control blocks, including to the ODT control block. The output of the ODT control block, ODTCTL, provides an input to corresponding correction circuits in the at least one circuit.” ’731 Chart at 343. However, Netlist does not provide any analysis of Samsung’s circuitry. Moreover, Netlist does not show that the alleged “at least one control signal” is actually sent to the alleged “at least one circuit.” For instance, according to Netlist’s annotated illustration, the alleged “at least one control signal” (“control/address and CS signals,” notated as “CS and CA[0:13]”) is first sent to a “command decoder.” ’731 Chart at 344. Netlist alleges that “[t]he output of the address/control decoder on the SDRAM provides input to various control blocks, including to the ODT control block.” ’731 Chart at 343-44 (highlighting the alleged output going from the “COMMAND DECODER” to “OE/ODT CONTROL” via another functional block labeled “PR DLL”). However, what Netlist identifies as the “output” of the decoder is actually an input clock signal that is sent to both the “decoder” and the “ODT control block.” *See* NETLIST-ITC-0067137 at -139. The line Netlist highlighted green has arrows pointing to each of the decoder and ODT control block, indicating these are inputs. *Id.* Moreover, the lines highlighted green originate from signals labeled “CK_t” and “CK_c.” *Id.* Furthermore, the lines highlighted green are labeled “ICKL<0:3>” and “ICLK DLL <0:3>” and are marked as four bits wide (in contrast to the 1-bit CS signal and 14-bit CA bus). *Id.*

Next, Netlist contends that “[t]he output of the ODT control block, ODTCTL, provides an input to corresponding correction circuits in the at least one circuit.” ’731 Chart at 343-44 (annotating the alleged pathway in a dashed green line). But as the illustration shows, the input to the alleged “at least one circuit” is “ODTCTL,” which is not one of the CS or CA[0:13] signals Netlist accuses as the “at least one control signal.” Rather, as shown in Fig. 10 of the article Netlist cites, the output of the ODT control functional block is an effective termination resistance (RTT)

[REDACTED]

value (e.g., RTT_PARK). *See* NETLIST-ITC-0067137 at -141-42 (“Fig. 10 shows the . . . block diagram for ODT control . . . If the command is the write command the signal output will be WTT_WR value . . . If there is no command, the output will be RTT_PARK value.”). Therefore, the alleged “control circuitry” does not send any signals to the alleged “at least one circuit,” let alone “at least one control signal . . . in response to the address and control signals.” Furthermore, the alleged “control circuitry” does not send control signals in response to address signals for at least the reasons explained with respect to claim 10, which are incorporated herein by reference.

(j) Claim 12

The Accused Products do not infringe claim 12 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 12 depends from claim 1 and the Accused Products do not infringe claim 12 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit includes one or more circuit elements, and wherein the control circuitry is configured to activate the one or more circuit elements in response to the address and control signals.” Netlist contends the “circuit elements” consist of “comparators/gain adjustors, resistors for ODT, and DFE circuit.” '731 Chart at 367. With respect to ODT resistors, Netlist contends that “dynamic ODT/RTT configuration” is “facilitated based on CA/CS/CK signals sent from the RCD to the DRAMs corresponding to a specific rank.” '731 Chart at 367. For reasons already discussed with respect to claims 1 and 10 (incorporated herein by reference), this does not show that the alleged “control circuitry is configured to activate the one or more circuit elements,” as opposed to the system memory controller. The foregoing similarly applies to Accused Products without RCDs or MRCDs. Furthermore, Netlist does not explain how the ODT resistors are allegedly activated “in

[REDACTED]

response to the address and control signals,” as opposed to simply being adjusted. For instance, according to Netlist’s contentions, “there are five RTT values: RTT_disable, RTT_WT, RTT_NOM_RD, RTT_WR, and RTT_PARK.” ’731 Chart at 378-79 (citing NETLIST-ITC-0069421 at -494-96). With respect to “comparators/gain adjustors” and “DFE circuit,” Netlist does not provide any explanation nor citations to documents describing how either alleged “circuit element” is allegedly “activate[d] . . . in response to the address and control signals.” Furthermore,

[REDACTED] for at least the reasons explained with respect to claim 10, which are incorporated herein by reference. Netlist contends that “[t]he use of the specific RTT and hence the turning on and off of the corresponding resistor or resistor network is controlled by the C/A and CS signals.” ’731 Chart at 387. However, the JEDEC standard makes clear that “[t]he ODT control is encoded into the chip selects,” not address signals. *See* ’731 Chart at 387-88 (citing NETLIST-ITC-0066438 at -476).

(k) Claim 13

The Accused Products do not infringe claim 13 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 13 depends from claim 1 and the Accused Products do not infringe claim 13 at least for the same reasons that they do not infringe claim 1.

(l) Claim 14

The Accused Products do not infringe claim 14 of the ’731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 14 depends from claim 1 and the Accused Products do not infringe claim 14 at least for the same reasons that they do not infringe claim 1.

(m) Claim 15

[REDACTED]

The Accused Products do not infringe claim 15 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 15 depends from claim 1 and the Accused Products do not infringe claim 15 at least for the same reasons that they do not infringe claim 1.

(n) Claim 16

The Accused Products do not infringe claim 16 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 16 depends from claim 1 and the Accused Products do not infringe claim 16 at least for the same reasons that they do not infringe claim 1.

(o) Claim 17

The Accused Products do not infringe claim 17 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 17 depends from claim 1 and the Accused Products do not infringe claim 17 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown for any of the Accused Products that “the at least one circuit includes signal paths, wherein the control circuitry is configured to activate a subset of the signal paths in response to the address and control signals.” For at least the reasons discussed above with respect to claim 10, Netlist has not shown nor explained how the alleged “control circuitry,” as opposed to the system memory controller, is “configured to activate” signal paths, or a subset thereof, “in response to the address and control signals.” Furthermore, [REDACTED]
[REDACTED] for at least the reasons explained with respect to claim 10, which are incorporated herein by reference.

(p) Claim 18

[REDACTED]

The Accused Products do not infringe claim 18 of the '731 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 18 depends from claim 17 and the Accused Products do not infringe claim 18 at least for the same reasons that they do not infringe claim 17.

[REDACTED]

[REDACTED]

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Respectfully Submitted,

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