

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

NETLIST, INC.,
Patent Owner

Case IPR2025-01431
U.S. Patent No. 10,025,731

PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120

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PATENT OWNER'S UPDATED EXHIBIT LIST

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2003	Senior Secured Convertible Promissory Note, November 18, 2015
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2007	Release of Assignment, Reel No. 065629, Frame No. 0330, November 20, 2023
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2010	Median time to trial statistics for the International Trade Commission, Docket Navigator report generated October 6, 2025)
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2013	First Amended Complaint, <i>Netlist Inc. v. Samsung Electronics Co., Ltd.</i> , Case No. 2:25-cv-00557 (E.D. Tex.), July 8, 2025
2014	Verdict Form, <i>Netlist, Inc. v. Samsung Electronics Co. et al.</i> , Case No. 2:21-cv-00463-JRG (E.D. Tex.), April 21, 2023
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2113	Netlist, Inc. Form 8-K, April 5, 2021
2114	Netlist Form 10-Q for the Quarterly Period Ended April 2, 2022
2115	Netlist Form 10-Q for the Quarterly Period Ended October 1, 2022
2116	Netlist, Inc. Report, Roth Capital Partners, April 8, 2021
2117	Netlist, Inc. Report, Craig-Hallum Capital Group LLC, April 8, 2021

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2118	Netlist, Inc. Form 10-K for the Fiscal Year Ended January 2, 2016
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Exhibit No.	Description
2129	Email from Michel A. Pearson titled “Stipulation re: PGR2025-00071 (U.S. Patent No. 12,308,087); IPR2025-01431 (U.S. Patent No. 10,025,731); and PGR2026-00001, IPR2026-00018 (U.S. Patent No. 12,373,366)” (March 3, 2026)
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I. INTRODUCTION

This *inter partes* review of claims 1-18 of U.S. Patent No. 10,025,731 (“the ’731 patent”) should be terminated. First, the Petition fails to name two real parties in interest (RPIs): Samsung Electronics America, Inc. (SEA) and Avnet, Inc., both of which have preexisting, established relationships with Petitioner and have a clear interest in and would benefit from this IPR. Indeed, both parties represented to an Article III court that they have standing and a present stake in the ’731 patent dispute. Second, Samsung advances inconsistent claim constructions across parallel proceedings, which is prohibited under current Office guidance.

Samsung also fails to prove the challenged claims were obviousness. First, the combinations fail to show key elements of the only independent claim. Second, a POSA would not have combined the art as asserted by Samsung. Third, secondary considerations confirm that the ’731 patent claims are not obvious. Two of the three most dominant players in the relevant market took a license to the ’731 patent and its family members but Samsung’s Petition simply ignores this highly relevant fact. The patentability of the challenged claims should be confirmed.

II. THE ’731 PATENT

The ’731 patent describes a memory module that reduces signal noise and reflections caused by impedance mismatches between the transmission lines and circuits that receive the signals. *See* EX1001, 2:2-14, 4:39-43, 9:55-10:29.

Specifically, that '731 patent describes a memory module that includes memory devices arranged in multiple ranks and programmable impedance matching circuits that are dynamically controlled based on which of the multiple ranks is selected to communicate data with an external system memory controller. *See* EX1001, 5:65-6:28, 10:59-11:17.

Figure 3, reproduced below, illustrates an external memory controller 106 that communicates with a memory module 100 that includes memory devices 110. EX1001, 5:14-21. The memory module 100 may also include a circuit 112 that “comprises a correction circuit 150 (see, e.g., FIG. 4) which reduces noise in one or more signals” EX1001 5:22-40.

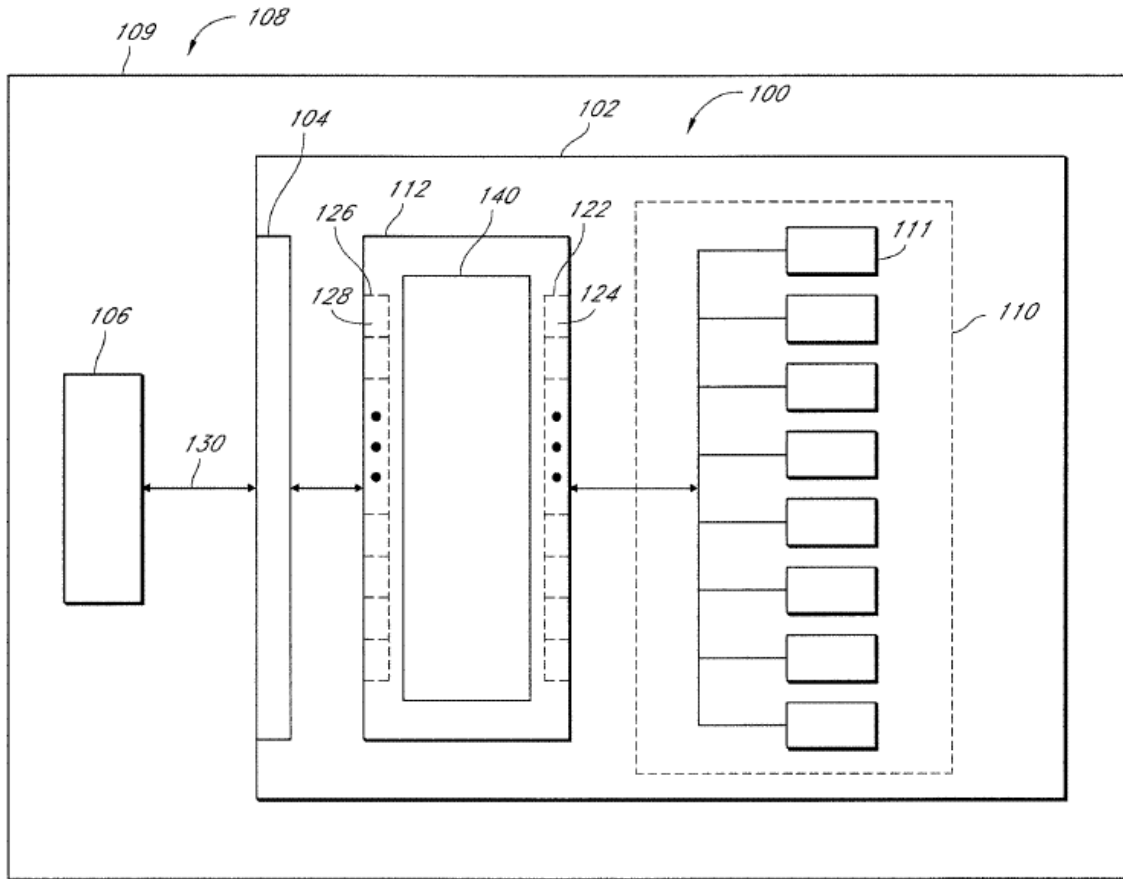


FIG. 3

EX1001, FIG. 3.

“Referring to FIG. 4, ... the correction circuit 150 includes one or more elements to provide for coarse correction of signal noise due to impedance matches (e.g., discontinuity regions) in the system. The at least one coarse correction element 152 comprises at least one programmable impedance matching circuit.”

EX1001, 10:40-46, FIG. 4 (reproduced below).

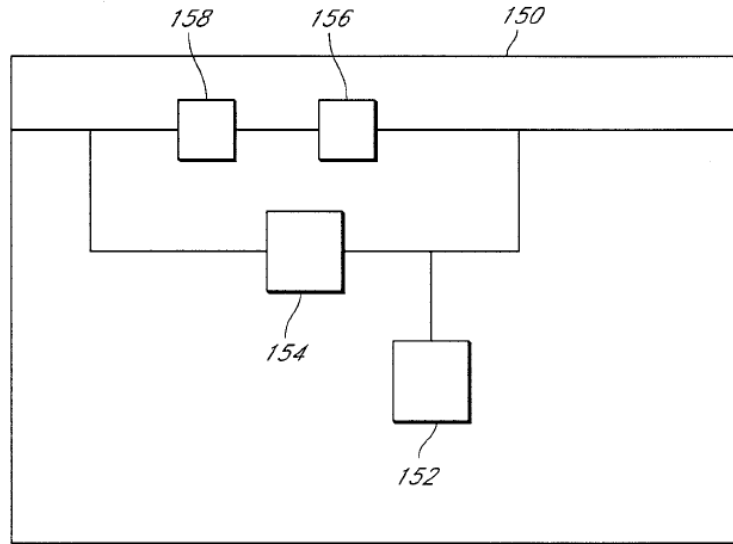


FIG. 4

EX1001, FIG. 4.

The '731 patent explains that “impedance values of the coarse correction element 152 may be dynamically controllable, configurable, and/or programmable, so as to match the characteristic impedances of the transmission lines (e.g., signal paths) in the system. The values of these impedances may differ (e.g., may be programmed differently) based on which particular signal path is activated.”

EX1001, 10:66-11:5. And, “[d]uring operation, one or more ranks of a memory module 100 may be selected or activated from the plurality of ranks by control signals that are received from a component of the system (e.g., a system memory controller 106 or a local memory controller of the memory module 100). Examples of such control signals include, but are not limited to rank-select signals, also

called chip-select signals.” EX1001, 6:20-28, FIG. 3 (reproduced above).

The ’731 patent thus describes a memory module that includes signal correction circuits, each including at least one programmable impedance matching circuit, to correct signals transmitted to and from the module’s memory devices, and control circuitry configured to dynamically control the at least one programmable impedance matching circuit. *See* EX1001, 9:9-13, 9:55-62. The claimed correction circuitry can reduce signal noise due to impedance mismatch in the system, enabling the claimed memory modules to provide stable, reliable signals at high data rates. *See* EX1001, 4:30-67. The claimed control circuitry can dynamically control impedance values of the programmable impedance matching circuit based on selection or activation of a rank of memory devices. *See* EX1001, 6:20-28; 10:66-11:6.

III. THE PETITION FAILS TO NAME TWO RPIs.

This proceeding should be terminated because the Petition fails to name all real parties in interest (RPIs). “A petition filed under section 311 may be considered *only if* ... the petition identifies all real parties in interest.” 35 U.S.C. § 312(a)(2) (emphasis added); *see also* 37 C.F.R. §§ 42.8(b)(1), 42.104. A petition that fails to name all RPIs cannot be considered. *Corning Optical Commc’ns RF, LLC v. PPC Broadband, Inc.*, IPR2014-00440, Paper 68 at 23-24 (PTAB Aug. 18, 2015) (precedential except § II.E.1); EX2024, 1. Such incomplete petitions “will

not be accorded a filing date until the petition satisfies all of the ... requirements.”

37 C.F.R. § 42.106; 35 U.S.C. § 312; *Corning*, Paper 68 at 24-25; *Yangtze Memory Techs. Co., Ltd. v. Micron Tech., Inc.*, IPR2025-00098, Paper 38 at 6 (PTAB Jan. 15, 2026) (informative) (“*YMTC*”) (“Petitioner’s failure to provide clarity as to its actual identity is fatal to its petitions.”).

The Petition names Petitioner Samsung Electronics Co., Ltd. (“SEC”) and Samsung Semiconductor, Inc. (“SSI”) as the only real parties-in-interest. Pet., 1. However, Samsung Electronics America, Inc. (“SEA”) and Avnet, Inc. (“Avnet”) are both additional RPIs that should have been identified in the Petition. Although both SEA and Avnet are RPIs, the panel need only find that one is an unnamed RPI to terminate this proceeding.

Samsung should be not permitted to correct its RPI listing at this late stage. Under current Office policy, adding a new RPI requires according the Petition a new filing date. *See Corning*, Paper 68 at 23-25; *Curium US LLC v. Universität Heidelberg*, IPR2025-01582, Paper 11 at 3 (Squires Feb. 25, 2026) (informative) (“*Curium*”) (“Petitioner’s amendment of its RPI disclosures results in according the Petition a new filing date.”). Netlist first raised this issue in the POPR on December 9, 2025, and Samsung has made no attempt to correct its RPI listing in response. In these circumstances, allowing a petitioner to correct its RPI listing at

this stage of the proceeding would encourage gamesmanship.¹ Accordingly, the proceeding should be terminated.

A. Relevant Litigation History

In May 2025, Netlist filed suits against SEC; SEA, and SSI (25-cv-00557) and Micron (25-cv-00558) in EDTX. EX2127, 1; EX2128, 1. In July 2025, Netlist amended its Samsung complaint to assert the '731 patent and add Samsung's customer Avnet as a defendant. EX2013. Also in July 2025, the same three Samsung entities (SEC, SEA, and SSI) filed a proposed amended complaint in the District of Delaware (DDE) for declaratory judgment of non-infringement of the '731 patent and added Avnet as a fourth DJ plaintiff.² EX2025.

In September 2025, Netlist filed an ITC complaint against the three Samsung entities (SEC, SEA, and SSI) and certain of its customers asserting six patents, including the '731 patent. EX2015. In the ITC, the three Samsung entities

¹ Additionally, SEA and Avnet will become time-barred under 35 U.S.C. § 315(b) on July 8, 2026 and July 13, 2026, respectively, because SEA and Avnet were each served with a complaint alleging infringement of the '731 patent, respectively on July 8, 2025 and July 11, 2025 (July 11, 2026 is a Saturday). *See* EX2127, 2 (Dkt. Nos. 15 and 23).

² Samsung filed the Petition in this IPR on August 29, 2025.

jointly filed a stipulation that “for any proceedings above [(including this IPR)] that are instituted by the PTAB ... Samsung will not pursue an invalidity defense in the ITC or any district court action.” EX2129. With this stipulation, the three Samsung entities jointly chose the PTAB as the preferred forum to challenge validity, confirming they are acting in concert.

B. Legal Standards

“Determining whether a non-party is a ‘real party in interest’ ... takes into account both equitable and practical considerations, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner.” *Applications in Internet Time, LLC v. RPX Corp.*, 897 F.3d 1336, 1351 (Fed. Cir. 2018) (“*AIT*”). “[A] patent owner must produce some evidence that tends to show that a particular third party should be named a real party in interest.” *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1244 (Fed. Cir. 2018). But after the RPI issue is placed in dispute, the petitioner has the burden “to bring forth evidence or arguments demonstrating that it named all RPIs.” *YMTC*, Paper 38 at 8 (citing *Worlds*, 903 F.3d at 1242). Indeed, Petitioner “bear[s] the burden of persuasion” to show that it has named all RPIs. *Worlds*, 903 F.3d at 1242; *Tianma Microelectronics Co., Ltd. v. LG Display Co., Ltd.*, IPR2025-01579, Paper 12 at 9-10 (Squires Mar. 18, 2026) (precedential).

RPI has an “expansive formulation.” *AIT*, 897 F.3d at 1351. Whether an

unnamed party is an RPI “is a highly fact-dependent question,” which may be shown through “direct or circumstantial” evidence. *Corning*, Paper 68 at 14-15; *Taylor v. Sturgell*, 553 U.S. 880 (2008). “[A] nonparty to an IPR can be a real party in interest even without entering into an express or implied agreement with the petitioner to file an IPR petition.” *AIT*, 897 F.3d at 1354; *RPX Corp. v. Applications in Internet Time, LLC*, IPR2015-01750, Paper 128 at 25 (PTAB Oct. 2, 2020) (precedential) (“*RPX*”). Board precedent and guidance identifies several factors to be considered in determining whether an unnamed party is an RPI, including: (i) nature of the entity filing the petition (i.e., petitioner’s business model); (ii) petitioner’s explanation of its own interest in the IPRs; (iii) whether petitioner takes the unnamed party’s interest into account when determining whether to file the petition; (iv) relationship between the petitioner and the unnamed party; (v) unnamed party’s relationship to the petition itself; (vi) unnamed party’s “interest in” and “benefit from” the IPR; (vii) whether petitioner can be said to be representing that interest; (viii) whether the unnamed party desired review of the patent; (ix) degree to which the unnamed party “exercised or could have exercised control over” the petition; and (x) whether the unnamed party funds, directs, or controls the petition. *See RPX*, Paper 128 at 10-11 ; *Corning*,

Paper 68 at 14-16; PTAB Trial Practice Guide (“TPG”)³, § D.1. “[A]t a general level, the ‘real party-in-interest’ is the party that desires review of the patent.” TPG, § D.1.

C. SEA is an unnamed RPI.⁴

A “non-party to an IPR can be a real party in interest even without entering into an express or implied agreement with the petitioner to file an IPR petition.” *AIT*, 897 F.3d at 1354; *RPX*, Paper 128 at 25. The RPI factors demonstrate that SEA is an unnamed RPI to this proceeding.

**1. SEA “has a preexisting, established relationship with”
Petitioner SEC and RPI SSI.**

“[W]hen it comes to evaluating the relationship between a party bringing a suit and a non-party, the common law seeks to ascertain who, from a ‘practical and equitable’ standpoint, will benefit from the redress that the chosen tribunal might provide.” *AIT*, 897 F.3d at 1349. This analysis is done “with an eye toward

³ <https://www.uspto.gov/patents/ptab/trial-practice-guide>

⁴ On May 28, 2026, the panel authorized Netlist to file a Motion for Additional Discovery related to RPI issues. *See* EX3105. This motion is due June 5, 2026. Should the Board grant Netlist’s motion, Netlist reserves the right to address any evidence produced in its PO Sur-reply or to request authorization to file a Motion to Terminate.

determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner.” *Id.* at 1351; *RPX*, Paper 128 at 20-21.

SEA admittedly has a preexisting, established relationship with both Petitioner SEC and named RPI SSI. SSI is a wholly-owned subsidiary of SEA, which is a wholly-owned subsidiary of SEC (SEC→SEA→SSI). EX2027, 1; EX2046, 2; EX2130, 17 (consolidated financial statement for “Samsung Electronics Co., Ltd. and its subsidiaries”). SEA’s relationship with SEC is far greater than that of the party who the Director found to be unnamed RPI in *Aylo Freesites Ltd. v. Dish Techs. LLC*, IPR2024-00940, Paper 75 (Squires Feb. 3, 2026) (“*Aylo*”). There, the Director de-instituted review because the petition failed to name a mere “services affiliate of Petitioner and co-defendant in parallel district court litigation.” *Aylo*, 2. SEA, by contrast, is a corporate entity in the middle of petitioner SEC and RPI SSI (SEC→SEA→SSI).

Further, this relationship is specifically tied to Samsung’s validity challenge of the ’731 patent. Indeed, Netlist alleges that SEA and SSI, “collectively with SEC, operate[] the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of” products that infringe the ’731 patent. EX2013, 2-3 (¶¶4-5).

2. SEA has a clear “interest in” and would “benefit from” this IPR, and desires review of the ’731 patent.

“[T]he focus of the real-party-in-interest inquiry is on the patentability of the

claims challenged in the IPR petition, bearing in mind who will benefit from having those claims canceled or invalidated.” *AIT*, 897 F.3d at 1348; *RPX*, Paper 128 at 23. The Board must consider whether SEA “has an interest in and will benefit from” this IPR. *AIT*, 897 F.3d at 1353; *RPX*, Paper 128 at 15. SEA would plainly benefit from review and invalidation of the ’731 patent.

SEA is a respondent in the ITC investigation and a co-defendant in the EDTX litigation. EX2015, 2 (¶5); EX2013, 1. As a named defendant in the EDTX litigation and in the ITC investigation, SEA faces the same infringement exposure as SEC and SSI. Invalidating the ’731 patent through this IPR would immediately benefit SEA by eliminating liability and foreclosing injunctive relief in the parallel fora.

Critically, Samsung *itself* confirmed SEA’s concrete interest in the ’731 patent by naming SEA as a co-plaintiff in its DJ action against the ’731 patent. EX2025, 1. In that complaint, Samsung affirmatively alleged that a “substantial, immediate, and real controversy” exists between Netlist and SEA regarding infringement of the ’731 patent. EX2025, 44 (¶146); *see id.*, 5 (¶17). Having represented to an Article III court that SEA has standing and a present stake in the ’731 patent dispute, Samsung cannot now credibly claim that SEA is only a peripheral entity with no RPI status in this IPR.

SEA’s involvement in *three* co-pending litigations demonstrates it has a

significant stake and would benefit from a favorable outcome here. *RPX*, Paper 128 at 24-25 (“[B]ecause of the pending litigation, the invalidation of the challenged patents would provide a benefit to [unnamed party].”). Indeed, even Samsung’s own expert in this IPR, Dr. Wolfe, conceded that SEA could benefit if the IPR is successful. *See* EX2060, 103:4-105:2, 107:4-108:12.

And SEA’s interest and participation in the litigation with Netlist is far greater than that of the party who the Board found to be unnamed RPI in *Aylo*. Here, SEA has affirmatively invoked standing in Delaware to participate in Samsung’s DJ action. If the affiliate in *Aylo*—a mere “services affiliate of Petitioner and co-defendant in parallel district court litigation,” *Aylo*, 2—was an RPI, SEA necessarily is as well.

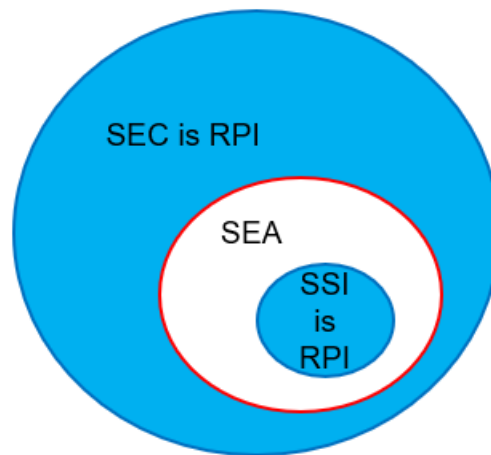
Further, SEA desires review of the ’731 patent claims and, thus, has an interest in this IPR. Indeed, SEA has challenged the validity of the ’731 patent claims in district court. *See* EX2016. And SEA’s *Sotera* stipulation, EX2129, demonstrates that SEA desires review of the ’731 patent, and has *affirmatively selected* the PTAB as its preferred forum.

3. SEC and SSI are representing SEA’s interests.

The Board also must consider “whether, and under what circumstances, [Petitioner] takes a particular client’s [or customer’s] interests into account when determining whether to file IPR petitions.” *AIT*, 897 F.3d at 1353; *RPX*, Paper 128

at 17. The Board must further consider whether SEC and SSI “can be said to be representing [SEA’s] interest” in filing this IPR. *AIT*, 897 F.3d at 1353; *RPX*, Paper 128 at 25. Again, the answer is yes. SEC (as parent) and SSI (as subsidiary) are plainly representing the interests of SEA.

All three entities are accused of infringing the ’731 patent. And this IPR represents the interests of all three—in particular, the interest in avoiding liability for infringement by attempting to invalidate the asserted patent. *See RPX*, Paper 128 at 27. In these circumstances it is nonsensical that both parent SEC and subsidiary SSI would be RPIs, but SEA—sandwiched in the middle as shown below—would not be.



Samsung’s decision to name SEA as a co-plaintiff in its DJ action further demonstrates that SEC (as the parent company) is representing SEA’s interest in challenging the validity of the ’731 patent in this IPR.

Significantly, nowhere in its pre-institution argument does SEC provide any

evidence, or even a clear statement, that it is *not* representing SEA's interest in avoiding liability for infringement by challenging the validity of the '731 patent in this IPR. *See Sun Pharm. Indus., Inc. v. Biofrontera Inc.*, PGR2026-00021, Paper 12 at 2-3 (Squires May 26, 2026) (denying institution due to unnamed RPI; determining a parent with 100% ownership of subsidiary has *ability* to control proceeding and it was Petitioner's burden to show otherwise).

4. There is apparent collaboration between SEC, SEA, and SSI in defending against the '731 patent, suggesting both that the parties are working in concert and that SEA had control (or the opportunity to control) this IPR.

Another "common consideration [in determining whether a non-party is an RPI] is whether the non-party exercised or could have exercised control over a party's participation in a proceeding." TPG, § D.1. Even if SEC, SEA, and SSI "did not directly discuss filing an IPR, the discussions of litigation are naturally tied to possible defenses, of which an IPR challenge is one." *RPX*, Paper 128 at 30 (explaining that "[s]uch communications need not expressly involve a request by [unnamed RPI] Salesforce for [petitioner] RPX to file an IPR petition," and that "[t]he discussion of pending litigation by [patent owner] AIT against Salesforce ... [would] weigh[] in favor of finding that Salesforce was an interested party.").

First, the parties' joint stipulation in the ITC to forgo any invalidity challenge there in favor of this PTAB challenge, provides substantial evidence of collaboration between all three entities in defending against the '731 patent.

And the asserted grounds in the IPR include the very same combinations (Ellsberry, Dour, and/or Abadeer) that SEC, SEA, and SSI jointly present in their invalidity contentions in the EDTX litigation. EX2016, 184-185, 201-262. This suggests a coordinated strategy between SEC, SEA, and SSI for challenging the validity of the '731 patent in defense of Netlist's infringement claims. *See Volkswagen Grp. of Am., Inc. v. Arigna Tech. Ltd.*, IPR2021-01263, Paper 16 at 15-16 (PTAB Jan. 21, 2022). At minimum, as a co-defendant in the EDTX litigation, SEA *could have exercised control* over the development of these invalidity positions presented in the Petition. *Sun Pharm.*, PGR2026-00021, Paper 12 at 2-3 (only the *ability* to control proceeding, such as via a 100% parent/subsidiary relationship—as opposed to *actual* control—is required to be considered an RPI).

5. SEC's business model and reasons for filing Petition.

The Board must also consider the nature of Petitioner and Petitioner's own interest in the IPR. *AIT*, 897 F.3d at 1353-54; *RPX*, Paper 128 at 10. These factors do not affect the analysis here. SEC's business model does not implicate the factors discussed in *AIT* or *RPX*, which focused on RPX's status as membership organization whose purpose is to "protect its members from the threat of patent litigation." *RPX*, Paper 128 at 11-15. And SEC's own reasons for filing an IPR do not undermine SEA's status as an RPI. *AIT*, 897 F.3d at 1347 (noting that Congress

did not intend for there to be only one interested party per case “even where the petitioning party might separately have its own interest in initiating an IPR”); *id.* at 1353 (RPI inquiry “is not an either-or proposition.”).

6. Samsung’s venue arguments in the EDTX litigation are irrelevant to the RPI question here.

Samsung’s motion to dismiss SSI and SEA from the EDTX case for alleged improper venue, *see* EX2026⁵, does not change the RPI analysis. The issues of whether venue is proper in EDTX and whether SEA is an RPI to this proceeding are different legal and factual analyses. *See* 28 U.S.C. § 1400(b); *AIT*, 897 F.3d at 1351. The RPI analysis is not limited to a specific district court venue, such as EDTX. And thus, even if venue is not properly sited for a given defendant, it does not follow that the defendant fails to qualify as an RPI.

SEA is a perfect example. In its motion to dismiss, Samsung raises three arguments: (1) neither SSI nor SEA resides in Texas, (2) SSI has no regular and established place of business in EDTX, and (3) Netlist fails to plausibly allege an

⁵ In pre-institution briefing, Samsung accuses Netlist of concealing declarations Samsung used to support its EDTX venue motion. POPR Reply (Paper 15), 2. But Netlist submitted the motion itself, which contains the same alleged facts, *see* EX2026, 3-4, which are irrelevant here because venue and RPI turn on different legal tests, POPR, 8-10.

act of infringement by SEA in EDTX. EX2026, 6-11. Even if Samsung were to prevail on *all* three arguments, which it should not, SEA is still an RPI here. Arguments (1) and (2) are geographically limited to Texas (and thus have no bearing on the RPI inquiry); argument (3) is limited to *SEA*'s alleged non-infringement. Even if SEA does not infringe in EDTX, which Netlist does not concede, Samsung's argument does not extend to SEC and SSI. Because SEA has preexisting, established relationships with both, the RPI inquiry is still at issue in light of the EDTX case against SEC and SSI. And, if there were any doubt, the Delaware DJ action and the ITC case confirm that SEA is an unnamed RPI.

Finally, Samsung is the leading petitioner in AIA challenges and has named SEA as an RPI on close to 800 petitions. EX2020, 48; EX2028. Samsung knew or should have known the requirement for naming all RPIs and has no excuse for failing to do so here.

* * *

For these reasons, SEA is an unnamed RPI to this proceeding and, therefore, the proceeding should be terminated.

D. Avnet is an unnamed RPI.

The RPI demonstrate that Avnet also is an unnamed RPI to this proceeding.

1. Avnet “has a preexisting, established relationship with the petitioner” SEC and RPI SSI.

Avnet indisputably has a preexisting, established relationship with Petitioner

SEC and RPI SSI. *AIT*, 897 F.3d at 1351. Indeed, Samsung has acknowledged that Avnet is Samsung's customer. EX2025, 2. But more than that, Avnet is a distributor of Samsung's memory products, EX2047, EX2048, and, as such, is a co-defendant in the EDTX litigation, EX2013, 1.

2. Avnet has a clear “interest in” and would “benefit from” this IPR, and desires review of the '731 patent.

Avnet is a defendant in the EDTX litigation. EX2013, 1. And in the Delaware DJ action—again, where the plaintiffs had control over the parties to name—Avnet certified *collectively* with Samsung that it has an “immediate, real, and justiciable controversy” as to whether it infringes the '731 patent and made no attempt to establish its own, separate reasons for standing. EX2025, 5. Avnet has a clear “interest in” and “benefit from” this IPR (avoiding liability for alleged infringement). *RPX*, Paper 128 at 24-25.

3. SEC and SSI are representing Avnet's interests.

Petitioner, as Avnet's supplier, is representing Avnet's interest. At minimum, Samsung's attempt to shield its customer from infringement liability in the EDTX litigation at least “strongly suggest[s] that [petitioner] filed the Petition, at least in part, on [Avnet's] behalf.” *See Ventex Co., Ltd. v. Columbia Sportswear N. Am., Inc.*, IPR2017-00651, Paper 148 at 8-9 (PTAB Jan. 24, 2019) (precedential).

4. Ongoing discovery may further show Avnet's opportunity to control these proceedings.

Discovery is ongoing. Netlist is seeking additional discovery regarding, among other things, indemnification and manufacturing/supply agreements between SEC and Avnet related to the accused products. *See* EX3105. Indemnity or defense obligations for SEC on behalf of Avnet included in these agreements would tend to show Avnet's opportunity to control this proceeding, at least sufficient to put Samsung's identification of RPIs in dispute and shift the burden to Samsung to show that Avnet is not an RPI. *See Worlds*, 903 F.3d at 1246.

5. SEC's business model and reasons for filing Petition.

SEC's business model and its own interest in the IPRs do not affect the analysis here. *See* Section III.C.5.

* * *

For these reasons, Avnet is an unnamed RPI to this proceeding and, therefore, the proceeding should be terminated.

E. Samsung should not be permitted to correct its RPI listing at this stage of the proceeding.

Samsung should be not permitted to correct its RPI listing at this late stage. Netlist first raised this issue in the POPR on December 9, 2025, and Samsung has made no attempt to correct its RPI listing in response. Allowing Samsung to correct its petition in these circumstances would circumvent the statute and invite gamesmanship. Congress stated a petition may only be considered if the petition

identifies all real parties in interest, which is echoed in the PTAB regulations. 35 U.S.C. § 312(a)(2); 37 C.F.R. § 42.104. The policy for this requirement is not limited to concerns about identifying any § 315(b) time-bar but also ensures that sufficiently related third parties are bound by § 315(e)'s IPR estoppel provision. *See RPX*, Paper 128 at 9 (quoting *AIT*, 897 F.3d at 1350). Allowing Samsung to add an unnamed RPI months after the issue was raised by Netlist would impart no real consequence for its failure to follow these statutory and regulatory requirements.

Worse yet, to change the filing date and restart the proceeding (as in *Curium*) would be grossly unfair to Netlist, because it would allow Samsung to see all of Netlist's arguments before the proceeding was restarted. That is, it would permit Samsung a second bite at the apple and open the door to road mapping based on all the arguments that Netlist included in its pre- and post-institution briefing. Further, it would be grossly inefficient, driving up costs and wasting the Board's resources. And here, trial in the ITC case is scheduled to begin at the end of November 2026—months before the projected FWD date of February 18, 2027. EX2131, 6. A clock reset would push the projected FWD date well past both the ITC trial and the May 3, 2027 projected date for the ITC's initial determination and clearly be contrary to the purpose of the AIA's objective to provide an effective and efficient alternative to litigation. *Id.*; *Accord NHK Spring Co., Ltd. v. Intri-*

Plex Techs., Inc., IPR2018-00752, Paper 8 at 20 (PTAB Sept. 12, 2018)

(precedential).

IV. SAMSUNG PRESENTS INCONSISTENT CLAIM CONSTRUCTIONS

Samsung presents inconsistent claim constructions regarding the term “control circuitry configured to ... control the plurality of memory devices in response to the address and control signals.” At the Board, Samsung argues that receiving memory addresses and command information from the DIMM interface, buffering in a register, and sending to all memory banks teaches this element. Pet., 73. But at the ITC, Samsung argues that an RCD (a type of control circuitry on the memory module) does “not perform a control function,” EX2132, 126, because an “RCD’s role is to buffer [address and control] signals received from the off-DIMM system memory controller,” EX2132, 129.

V. THE CLAIMS ARE VALID AND NON-OBVIOUS

Samsung presents two Grounds of unpatentability alleging claims 1-18 of the ’731 patent would have been obvious based on (1) the combination of Ellsberry and Dour and (2) the combination of Ellsberry, Dour, and Abadeer. Both Grounds fail; they do not teach or render obvious all the claim elements, and secondary considerations (including Samsung’s own licensing activities) confirm that the claims were non-obvious.

A. Ellsberry

Ellsberry describes a capacity-expanding memory device. EX1005, Title. As background, Ellsberry describes a conventional memory system. EX1005, ¶¶2-5. A memory module, such as a dual in-line memory module or “DIMM,” may include dynamic random-access memory (“DRAM”) chips that store information. EX1005, ¶¶2-3. The memory module is inserted into “a slot” on a “computer motherboard,” enabling information to be exchanged between the memory module and a “system memory controller” via a memory bus on the motherboard. EX1005, ¶¶2-5.

In conventional systems, the system memory controller knows the configuration of the memory module(s) that it communicates with. *See* EX1005, ¶4. The system memory controller typically obtains the memory module’s configuration information by reading it from a Serial Presence Detect (“SPD”) chip that is on the memory module. *See* EX1005, ¶34; EX2060, 32:17-33:11. And because the system memory controller knows the memory module’s configuration, the system memory controller can *access* memory locations on the memory module: “To *access* locations in memory devices, such as DRAM, a memory location is typically specified by the system over an address bus. This address is decoded to *access* the correct memory device.” EX1005, ¶4.

Ellsberry recognized that electronic devices were becoming “more sophisticated” and there was a “need for greater storage or memory increases.”

EX1005, ¶5. And because “many electronic applications are restricted by industry standards and physical limitations,” it was “undesirable and impractical” to increase the size of the memory bus on the system’s motherboard. EX1005, ¶5. Ellsberry thus sought to “expand[] the memory capacity of a memory module without increasing the bus size.” EX1005, ¶26; *see also* EX1005, ¶10.

Ellsberry’s solution was a memory module in which smaller-capacity memory devices “emulate” a single, higher capacity memory device, EX1005, ¶¶10, 26, while making the underlying architecture of the memory module “transparent” to the rest of the system, EX1005, ¶¶1, 27. For example, “two separate SDRAM DDR devices” can “appear as a single higher-capacity SDRAM DDR device to” the system memory controller while the actual configuration of the memory module is hidden to the system memory controller. EX1005, ¶26. Importantly, Ellsberry organizes the memory devices on the memory module into “banks” but does not share this information with the system memory controller. EX1005, ¶¶27, 30.

To hide the memory module’s architecture from the system memory controller, Ellsberry implemented additional logic on the memory module that “intercepts and modifies communication from the host computer.” EX1003, ¶51; *see also* EX2060, 42:18-43:5 (Dr. Wolfe explaining that “the system cannot tell logically or electrically that there is ranked multiplication going on, because

there's an intermediate circuit that isolates the multiple memory banks from the memory controller and performs all of the translations that -- that take place.”). Specifically, Ellsberry’s “capacity-expanding feature ... is accomplished by a combination of a control unit 204 and one or more memory bank switches 206 & 208,” which are shown in Figure 2 below.

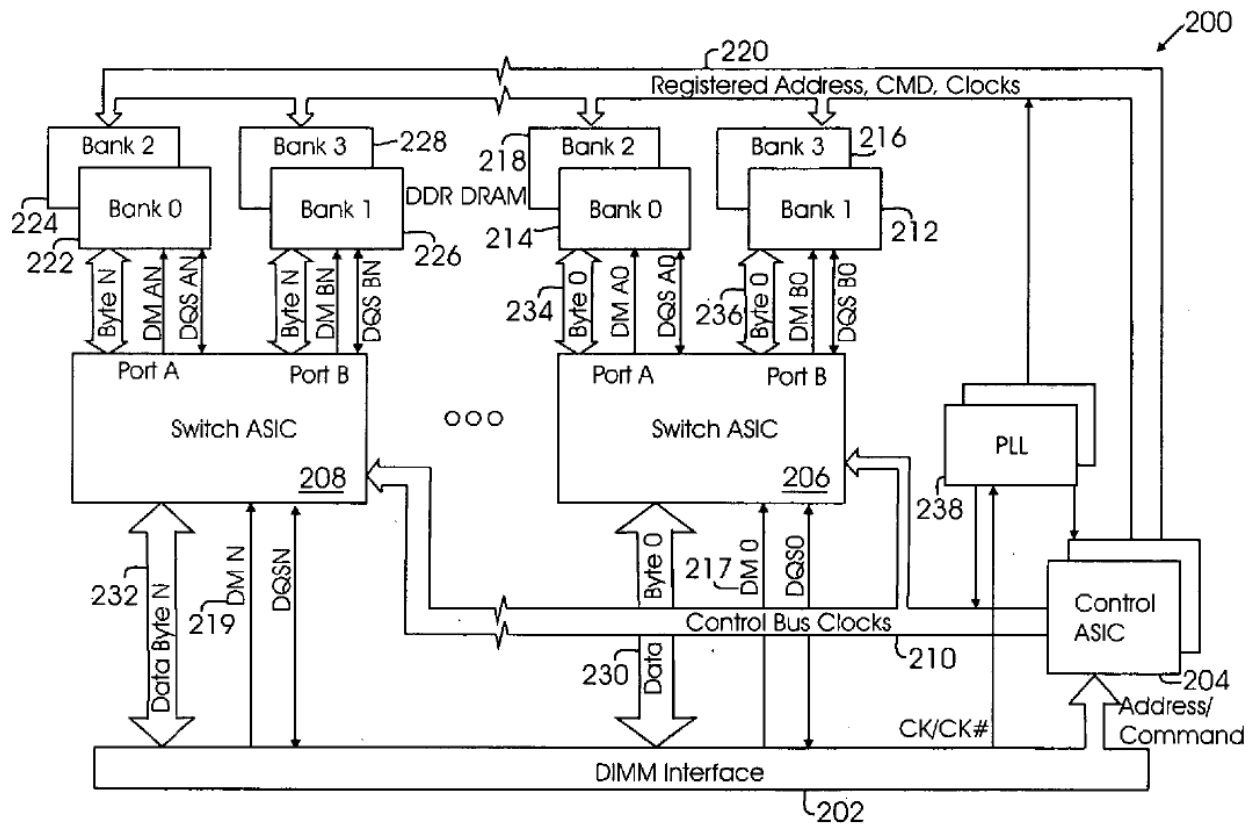


Fig. 2

EX1005, FIG. 2.

Figure 2 depicts an embodiment of Ellsberry’s capacity-expanding memory system. EX1005, ¶28. “The DIMM interface 202 may be coupled to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted.” EX1005, ¶28. Ellsberry explains that

“control unit 204 receives memory addresses and commands over the DIMM interface 202” and the “memory bank switches 206 & 208 receive data information from the DIMM interface 202 via data buses 230 & 232, respectively.” EX1005, ¶29. “Each memory bank switch 206 & 208 is communicatively coupled to a plurality of memory banks that may have one or more memory devices (e.g., dynamic random access memory (DRAM)).” EX1005, ¶30.

Ellsberry explains that the control unit 204 performs address space translation to identify which banks and memory locations to access. EX1005, ¶¶31, 35, 37, 39; FIG. 7; *see also* EX2060, 42:18-43:5. Because the memory module’s architecture is transparent, the system memory controller provides an address in a “primary space” that the control unit 204 maps or translates into a “secondary space.” EX1005, ¶¶35 (“The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the switches 206 and 208.”), 37 (“[A] primary space address received by the control unit 204 is mapped to a secondary space address corresponding to the memory banks.”). In particular, “the control unit 204 decodes a memory address received over the DIMM interface 202, determines to which memory bank the received address corresponds, and causes the memory bank switch 206 and 208 to activate the correct memory bank.” EX1005, ¶31.

B. Dour

Dour is directed to programmable on-die termination (“ODT”) for properly terminating signals that travel on buses between components on a computer system’s main board (or motherboard). EX2058, ¶39. Dour teaches that “[c]omputer system components include processors” and “memory modules” that “communicate with one another over a set of buses.” EX1018, 1:15-18. “Buses are typically communication signals laid out on a printed circuit board such as the main board of a computer system.” EX1018, 1:30-32.

Figure 2 of Dour is reproduced below and illustrates communication line 205 (red) between a memory controller 213 and a memory module 211. EX1018, 2:42-44, FIG. 2. “Communication line 205 may be part of a system bus such as a front side bus, a memory bus, or similar communication line.” EX1018, 2:54-56.

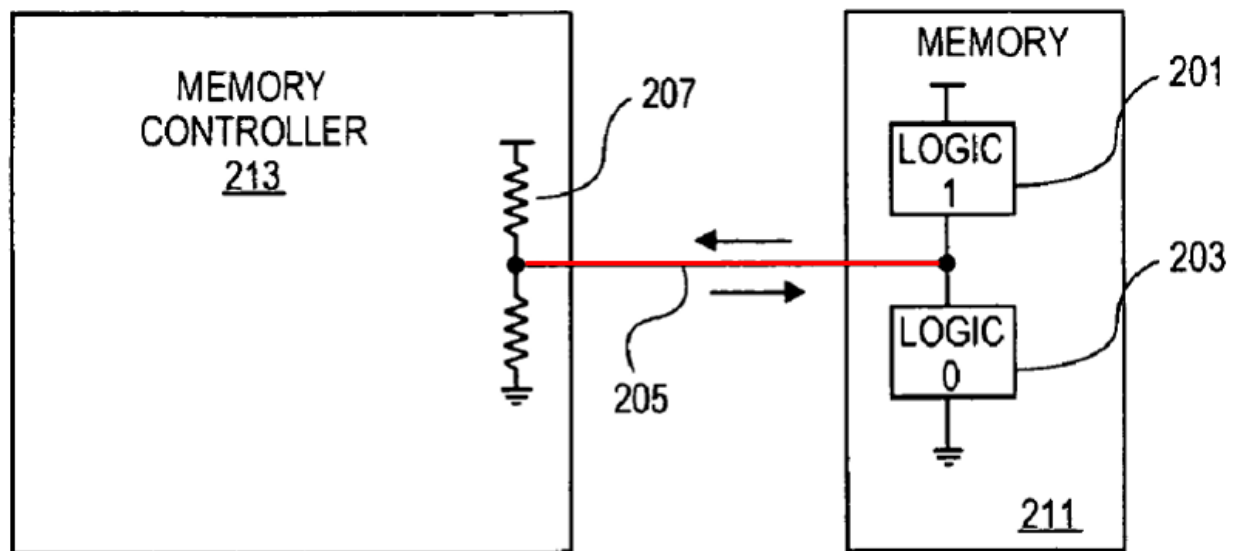


FIG. 2

EX1018, FIG. 2 (annotated).

Dour explains that “memory module 211 may be a dynamic random access memory [(DRAM)] module” that is “packaged as a dual in line memory module (DIMM).” EX1018, 2:46-49. Dour further explains that “[m]emory module 211 may be a double data rate (DDR) module” EX1018, 2:50-51. But other than describing the memory module as a DDR DRAM packaged as a DIMM, Dour provides no further details of the memory module. Relevant here, Dour does not disclose that the memory module is a multi-rank memory module. EX2060, 77:7-10. Nor does Dour suggest ODT is used to terminate signals that are transmitted within a memory module itself.

Dour teaches programming the ODT based on certain conditions *in the device* that receives a signal (such as a memory controller), not based on the length of the communication line that carries the signal. EX2058, ¶42 (citing EX1018, 3:60-65, 4:4-7, 4:7-11, 4:11-15, 4:17-20, 4:21-22, 5:20-23, 6:50-53). Specifically, figure 4 of Dour is reproduced below and shows a memory controller that includes a “testing circuit 401 to determine conditions *in the device*.” EX1018, 3:60-61.

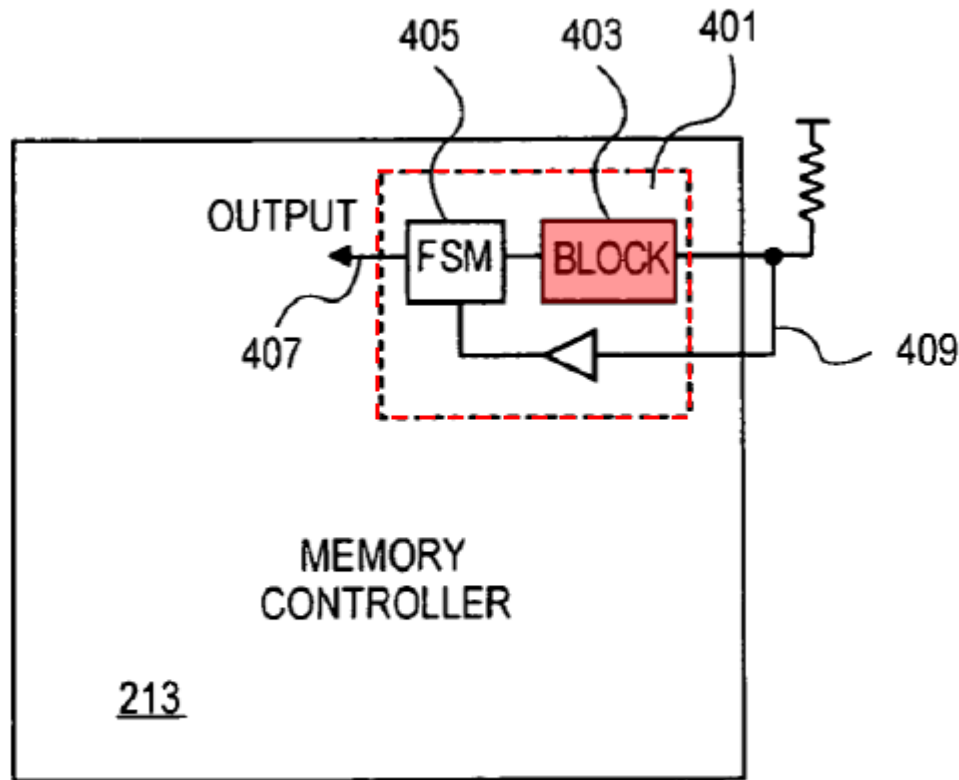


FIG. 4

EX1018, FIG. 4 (annotated).

Testing circuit 401 includes a circuit block 403, a finite state machine (“FSM”) 405, and a feedback loop 409. EX1018, 3:65-4:3. Dour teaches that the FSM 405 encodes the “conditions of circuit block 403” into a signal that is used to adjust the ODT. EX1018, 4:4-20. Dour explains that these “conditions ... include the effects of the physical characteristics of the device, such as quality and type of manufacture, materials and similar physical characteristics, temperature, voltage and similar device conditions have on [sic] the signal processed by circuit block 403.” EX1018, 4:7-12; *see also* EX1018, 4:12-15 (“In one embodiment, finite state

machine 405 may encode the impedance of signals in block 403 based on the physical characteristics, voltage levels, and temperatures (PVT) *of block 403.*”), 6:50-53 (“a testing circuit or similar component detects the physical conditions, voltage conditions and temperature conditions (PVT) *of the component or on die termination circuit* (block 701).”), FIG. 7. Nowhere does Dour teach or suggest that the ODT is adjusted based on the length of the communication line or bus that carries the signal to be terminated. EX2058, ¶43.

C. Abadeer

Abadeer is “directed to automatic driver/transmission line/receiver impedance matching circuitry.” EX1039, ¶1. Samsung did not rely on Abadeer to address the claim elements discussed below, and thus a detailed discussion of Abadeer is omitted.

D. Claim 1

Grounds 1 and 2 fail to demonstrate claim 1 was obvious because: (1) Ellsberry’s memory controller cannot access an independent set of memory devices (e.g., a bank) on Ellsberry’s memory module (element 1.c), (2) the combination of Ellsberry and Dour does not teach or render obvious dynamically controlling an impedance matching circuit based on which rank of a multi-rank memory module is selected (element 1.f.2), and (3) a POSA would not have implemented Dour’s ODT in Ellsberry’s switch ASIC.

1. Ellsberry’s memory controller cannot access an independent set of memory devices on the memory module (element 1.c).

Element 1.c requires a “plurality of memory devices” that are “arranged in multiple ranks” in which “each rank compris[es] an independent set of memory devices *that can be accessed by the system memory controller* to access a full bit-width of the memory bus.” The plain and ordinary meaning of this claim language is that the memory controller must be able to access each rank (i.e., each independent set of memory devices that form a rank) of a multi-rank memory module. EX2058, ¶48.

Samsung relies on Ellsberry for element 1.c. Pet., 62-64; EX1003, ¶¶128-130; EX2060, 22:4-10. Neither Dour nor Abadeer disclose a memory module that includes ranks. EX2060, 77:7-10 (testifying Dour does not disclose ranks), 24:13-18 (testifying Abadeer does not disclose ranks). So Ellsberry is the only reference in Grounds 1 and 2 that is relevant to element 1.c.

But Ellsberry intentionally hides the bank arrangement and architecture of the memory module from the host system (including the system memory controller). Namely, Samsung alleges that Ellsberry’s “processing unit 102” is the claimed “memory controller” and that Ellsberry’s physical banks on the memory module are the claimed “ranks.” Pet., 58, 62-64. But Ellsberry teaches that the details of the memory module—particularly, the arrangement of its physical

banks—are transparent to the processing unit (or system memory controller).

Because Ellsberry’s banks are intentionally hidden from the rest of the system (including the processing unit, operating system, memory controller, etc.),

Ellsberry’s system memory controller cannot access each of the individual banks of the memory module, as required. EX2058, ¶50.

a. Memory controllers typically access ranks of a multi-rank DIMM using rank-select or chip-select signals.

The ’731 patent explains that the memory controller can access a specific rank on the multi-rank memory module using specific control signals, such as rank-select or chip-select signals. Specifically, “[d]uring operation, one or more ranks of a memory module 100 may be selected or activated from the plurality of ranks by control signals that are received from a component of the system (e.g., a system memory controller 106 or a local memory controller of the memory module 100).” “[S]uch control signals include, but are not limited to, rank-select signals, also called chip-select signals.” EX1001, 6:20-26; *see also* EX1001, 2:25-27; EX2058, ¶51.

The ’731 patent’s description of how memory controllers can access a rank on a multi-rank DIMM is consistent with contemporary industry standards. EX2058, ¶52; EX1003, ¶51 (explaining that “a ‘rank’ (sometimes called a ‘bank’) is an independent set of one or more memory devices on a memory module that act together in response to command signals, including *chip select signals*, to read or

write the full bit-width of the memory module.”). For example, the JEDEC specification for DDR SDRAM Registered DIMM Design provides the pinout of standard memory module (DIMM) during the relevant timeframe. EX1010, 6-9; *see also* EX2060, 27:8-33:21. The DIMM includes pins, shown below, that are described as “chip select lines” that receive commands sent by a system memory controller to select physical banks on the DIMM. EX1010, 6; EX2060, 30:9-31:4, 32:2-16.

$\overline{S}0 - \overline{S}3$	SDRAM chip select lines (Physical. banks 0, 1, 2, and 3)
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EX1010, 6.

In typical systems, the memory controller reads configuration information from a Serial Presence Detect (SPD) chip on the DIMM, which may include the number of physical banks on the DIMM. EX2060, 32:17-33:11; EX1010, 68. The JEDEC specification for DDR SDRAM Registered DIMM Design provides the example below, which shows an SPD that includes 256 bytes of configuration information. EX1010, 68. Byte 5 indicates that the “Number of Physical Banks” on this example DIMM is “2.” *Id.* The memory controller can use this information to access specific banks on the DIMM via chip select signals. EX2058, ¶53; *see also* EX2060, 32:17-33:11.

Serial Presence Detect Example Raw Card Version ‘A’ (Part 1 of 3)

64M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total number of bytes in Serial PD Device	256	08	
2	Fundamental Memory Type	SDRAM DDR	07	
3	Number of Row Addresses on Assembly	13	0D	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of Physical Banks on DIMM	2	02	

EX1010, 68 (reproduced in-part and annotated).

By contrast, Ellsberry intentionally hides the memory module’s bank-related information from the memory controller, emphasizing that the capacity-expanding aspects of its memory module are “transparent” to the rest of the system. EX1005, ¶¶1, 27. Indeed, Ellsberry discloses that the memory module may include an SPD but discloses only that the SPD contains information about the capacity of the memory module, not details of the bank arrangement. EX1005, ¶34. Specifically, Ellsberry teaches that the SPD contains information about “the total module memory capacity and data width along with the individual emulated memory device capacity that is formed by two or more small-capacity memory devices.” *Id.* Nowhere does Ellsberry state that information about the banks is included on the SPD. *Id.*; EX2058, ¶54. Given Ellsberry’s emphasis on transparency, a POSA would have understood that Ellsberry’s SPD does not contain information about the memory banks. EX2058, ¶54.

b. Because Ellsberry's banks are "transparent" to the memory controller, the memory controller cannot access the independent banks.

Ellsberry does not disclose a memory controller that can access each rank (i.e., each independent set of memory devices that form a rank) in a multi-rank memory module. EX2058, ¶55. Instead, Ellsberry discloses that such details of the memory module are "transparent" to the memory controller. EX1005, ¶¶1 ("a controller and architecture that permits transparent bank switching of memory devices"); 27 ("the capacity-expanding memory device 108 is compatible with existing system architectures and transparent to the rest of the system (e.g., microprocessor, operating system, etc.)"). Ellsberry's control unit 204 of Figure 2 (or controller 510 of Figure 5), not the external processing unit/memory controller, accesses the specific banks on the memory module following address translation.

Samsung and Dr. Wolfe acknowledge that Ellsberry teaches "transparent" bank switching of memory devices. Pet., 29; EX1003, ¶92. They allege that Ellsberry's disclosure that "the operating system addresses a single logical memory bank which is mapped by the controller 510 to the physical banks of memory devices" teaches a memory controller that can access individual ranks. Pet., 62; EX1003, ¶128. That is wrong; Ellsberry's teaches the opposite.

The crux of Ellsberry is that the "rest of the system" (host system, operating system, system memory controller, etc.) does not know that the memory devices on

the memory module are organized into banks. EX1005, ¶¶1, 10, 26-27; EX2058, ¶57; EX2060, 42:11-43:5 (“the system cannot tell logically or electronically that there is ranked multiplication going on”), 98:13-99:8. In other words, Ellsberry’s memory controller does not even know that the banks exist. Those details are left to and handled by the logic on the memory module (e.g., the control unit 204 and memory bank switch 206 & 208 of Figure 2). EX1005, ¶¶28-31; EX2058, ¶57; EX2060, 42:11-43:5 (“there’s an intermediate circuit that isolates the multiple memory banks from the memory controller and performs all of the translations that -- that take place”). And because these details are transparent to the rest of Ellsberry’s system, the system memory controller cannot and does not access an “independent set of memory devices” that form an individual, physical bank. EX2058, ¶57. Instead, Ellsberry’s host system sends an address in a primary address space that the logic on the memory module translates into a secondary address space and determines which bank the logic should access. EX1005, ¶¶31, 37, 39-40, FIG. 7.

On cross-examination, Dr. Wolfe confirmed this operation in Ellsberry. Specifically, he confirmed that (1) Ellsberry’s external memory controller “cannot tell logically or electronically” that the memory module includes multiple banks and (2) Ellsberry’s control unit 204 (“an intermediate circuit”) performs address translations in order to access the memory banks:

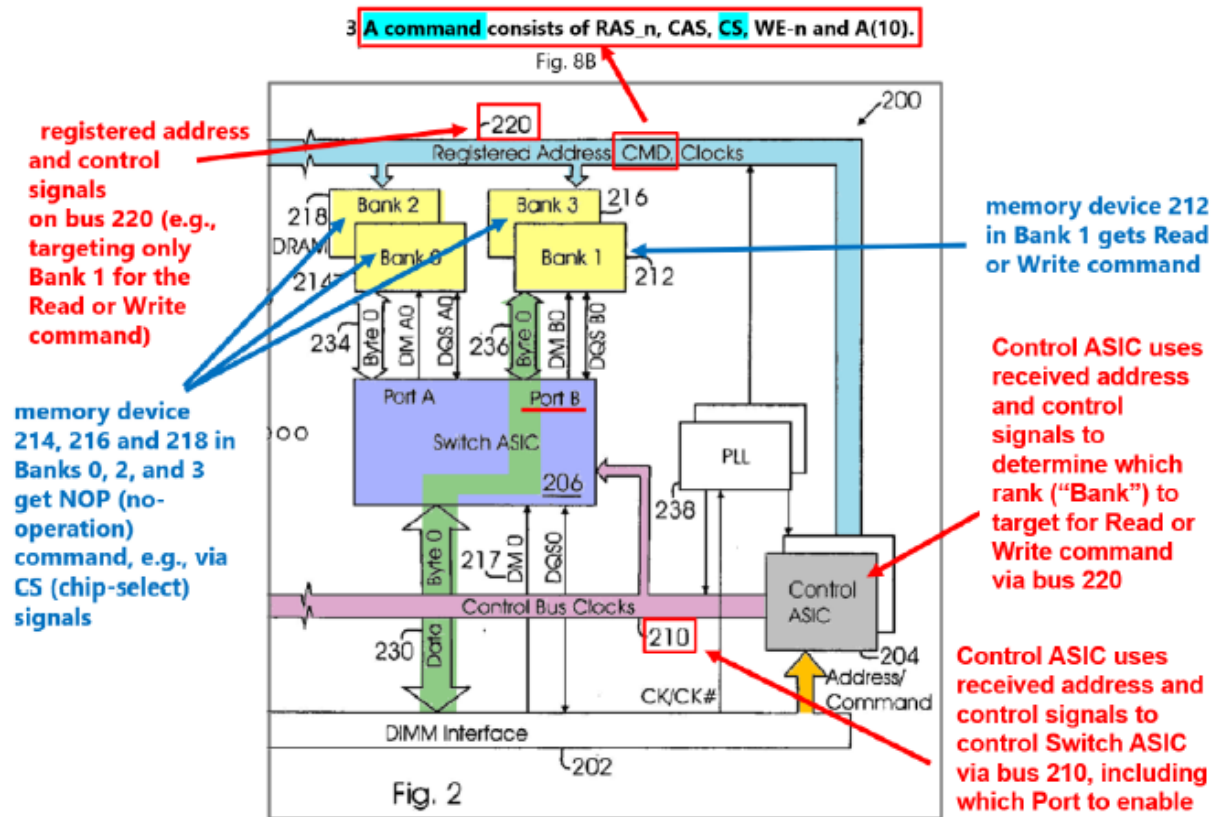
Q. What does Ellsberry mean that the capacity-expanding memory device is transparent to the rest of the system?

A. It means that *the system cannot tell logically or electrically* that there is ranked multiplication going on because *there's an intermediate circuit that isolates the multiple memory banks from the memory controller and performs all of the translations* that -- that take place.

EX2060, 42:18-43:5.

Dr. Wolfe's annotations to Ellsberry's Figure 2 (reproduced below) and his corresponding discussion of how Ellsberry's system operates further confirm that Ellsberry's system memory controller cannot access each of the independent banks. EX1003, ¶139; EX2060, 98:13-99:8 (discussing figure on page 101 of his declaration). As shown, Ellsberry's control unit 204 (labeled "Control ASIC") receives address and command signals from the DIMM interface 202. EX1003, ¶139. The received address is an address in a primary address space that corresponds to the overall capacity of the memory module and thus corresponds to all of memory banks. EX1005, ¶¶37, 39, FIG. 7A (2nd column); EX2058, ¶59. The Control ASIC uses the primary address "to determine which rank ("Bank") to target for Read or Write command[s] via bus 220," then generates and sends chip select signals ("CS" highlighted in blue) via the bus 220 (annotated in blue) to access an independent bank. EX1003, ¶139 (quote in annotated figure); EX2060, 98:20-22 ("...so the command that comes into the control ASIC is not necessarily

the command that gets sent out. It generates new commands.”).



EX1003, ¶139 (p. 101).

Ellsberry's system memory controller thus sends address signals using a primary address space that corresponds to the overall capacity of the memory module defined by the sum of the capacity of the individual banks. The system memory controller cannot access the banks individually. Only logic on Ellsberry's memory module can access banks individually via chip select signals that are generated by the logic on the memory module. EX2058, ¶60.

c. None of the previous Board decisions determined that Ellsberry discloses element 1.c.

Samsung and Dr. Wolfe are incorrect that the Board has already determined that Ellsberry discloses Element 1.c. Pet., 23, 64; EX1003, ¶¶86, 129. Each of the previous final written decisions they rely on evaluated a patent from a different family than the '731 patent that had a different disclosure and different claims. Element 1.c is materially different from other claim elements that the Board evaluated, and thus the previous decisions do not control. EX2058, ¶¶61-64.

The final written decisions in IPR2018-00362 and IPR2018-00363 evaluated U.S. 9,606,907 (“the '907 patent”). EX1062. The '907 patent is not in the '731 patent family, *see* EX1001, (63), and does not recite the term “rank” nor that “each rank compris[es] an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.” *See* EX1062, 17, 19-21.

'731 patent, element 1.c	'907 patent, cited elements of claim 1
“a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-	“A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and $N=M \times n$ ”

'731 patent, element 1.c	'907 patent, cited elements of claim 1
width of the memory bus”	“a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command”

The final written decision in IPR2022-00639 evaluated U.S. 10,949,339 (“the ’339 patent”). EX1066. The ’339 patent is not in the ’731 patent family, *see* EX1001, (63), and does not recite that “each rank compris[es] an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.” *See* EX1066, 33.

'731 patent, element 1.c	'339 patent, cited elements of claim 1
“a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in	“double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in

'731 patent, element 1.c	'339 patent, cited elements of claim 1
multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus”	multiple N-bit-wide ranks”

The final written decision in IPR2022-00615 evaluated U.S. 7,619,912 (“the ’912 patent). EX1078. The ’339 patent is not in the ’731 patent family, *see* EX1001, (63), and does not recite that “each rank compris[es] an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus.” *See* EX1078, 38-39.

'731 patent, element 1.c	'912 patent, cited elements of claim 16
“a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus”	“a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks”

Accordingly, none of the prior Board decisions evaluated whether Ellsberry

“banks” satisfy the “ranks” that are described and claimed in the ’731 patent.

2. The combination of Ellsberry and Dour does not render obvious dynamically controlling an impedance matching circuit on a multi-rank memory module based on which rank is selected (element 1.f.2).

Element 1.f.2 recites “wherein *the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit based on which of the multiple ranks is selected to communicate data with the system memory controller* in response to the address and control signals.”

Samsung does not allege that any of the references in Grounds 1 and 2 teach dynamically controlling an impedance matching circuit on a multi-rank memory module based on which rank is selected. *See* Pet., 74-77; EX1003, ¶¶137-140; EX2060, 23:12-17, 76:10-15. Indeed, Dr. Wolfe confirmed that neither Ellsberry nor Dour nor Abadeer discloses this feature. EX2060, 76:16-77:6 (alleging that Ellsberry “suggests” performing impedance calibration “because of the variation in wiring characteristics in the DIMM...”), 77:7-10 (confirming that Dour does not discuss ranks), 24:13-25:1 (confirming that Abadeer does not discuss ranks). So none of the references discloses a key element of the claimed invention: the ability to dynamically control impedance based on the specific rank that is selected.

Rather, Samsung alleges the combination of Ellsberry and Dour renders

obvious element 1.f.2. Pet., 74-77; EX1003, ¶¶137-140; EX2060, 23:12-17, 76:10-15. Specifically, Samsung posits that (1) it would have been obvious to implement “Dour’s ‘programmable on die termination circuit’ ... in Ellsberry’s ‘bidirectional signal drivers 402 & 404,’” Pet., 74, and (2) this combination would be further modified to dynamically calibrate impedance because of “variation of the surrounding conditions of incoming data signals” depending on which of Ellsberry’s banks is selected. Pet., 76-77.

Samsung’s basis for the latter modification is that Dour allegedly discloses dynamic impedance control based on the length of the communication line that carries the signal to be terminated, which, according to Samsung, corresponds to which of Ellsberry’s banks is selected. Pet., 75-76 (alleging that “data lines to Bank 0/1 may be shorter than data lines to Bank 2/3, which results in smaller loads for the shorter data lines”); EX2060, 76:16-77:20 (unable to find any discussion of “wire lengths” in Dour and relying instead on “physical characteristics of the device”), 79:4-83:18 (discussing “PVT” in Dour). But Samsung misinterprets and mischaracterizes Dour’s teachings, and thus a POSA would not have been motivated to make Samsung’s proposed further modification. EX2058, ¶68.

Dour does not teach dynamic impedance control (or programmable ODT) based on wire length. *See* EX2060, 77:7-20. Rather, Dour teaches programming the ODT based on certain conditions *in the device* that receives and terminates the

incoming signal (e.g., a memory controller). EX2058, ¶69 (citing EX1018, 3:60-65, 4:4-7, 4:7-11, 4:11-15, 4:17-20, 4:21-22, 5:20-23, 6:50-53); EX2060, 78:3-10, 80:4-11, 81:1-4. Specifically, Figure 4 of Dour is reproduced below and shows a memory controller that includes a “testing circuit 401 to determine conditions *in the device*.” EX1018, 3:60-61. Testing circuit 401 includes a circuit block 403, a finite state machine (“FSM”) 405, and a feedback loop 409. EX1018, 3:65-4:3.

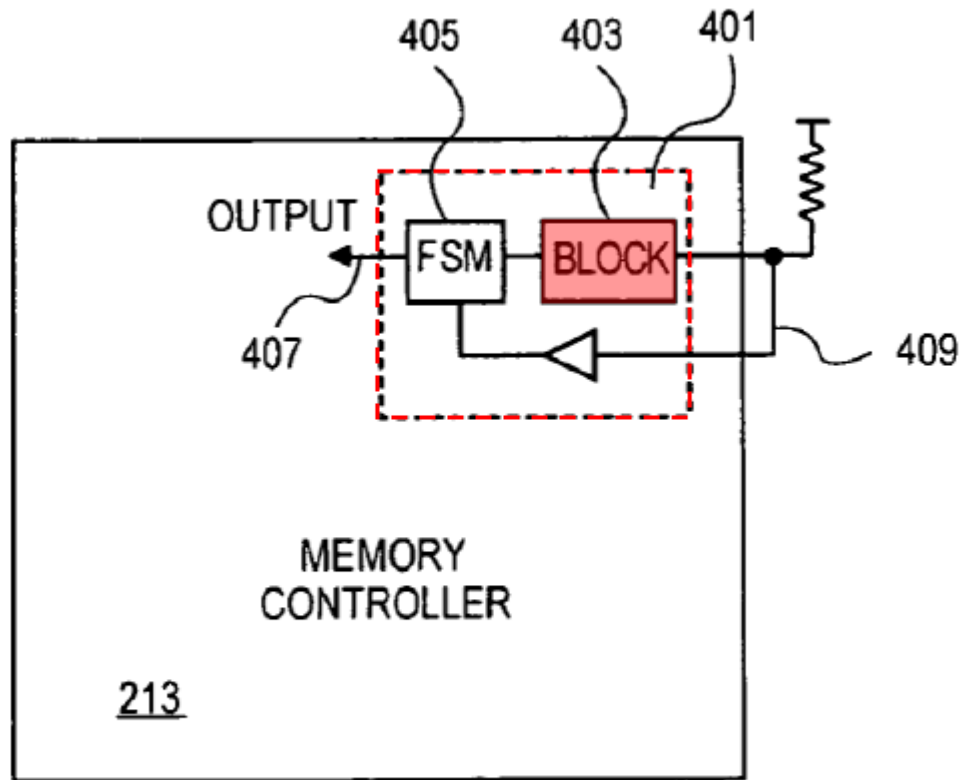


FIG. 4

EX1018, FIG. 4 (annotated).

Dour teaches that the FSM 405 encodes the “conditions of *circuit block 403*” into a signal that is used to adjust the ODT. EX1018, 4:4-20; *see* EX2060, 79:7-

81:4. Dour explains these “conditions ... include the effects of the physical characteristics *of the device*, such as quality and type of manufacture, materials and similar physical characteristics, temperature, voltage, and similar *device conditions* have on [sic] the signal processed by block 403.” EX1018, 4:7-12; *see also* EX1018, 4:12-15 (“In one embodiment, finite state machine 405 may encode the impedance of signals in block 403 based on the physical characteristics, voltage levels, and temperatures (PVT) *of block 403*.”), 6:50-53 (“a testing circuit or similar component detects the physical conditions, voltage conditions and temperature conditions (PVT) *of the component or on die termination circuit* (block 701).”), FIG. 7.

Nowhere does Dour teach or suggest that the ODT is adjusted based on the length of the communication line that carries the signal to be terminated or other characteristics of the communication line. EX2058, ¶¶70-71. Dr. Wolfe confirmed during cross-examination that Dour does not disclose programmable ODT based on “wire length.” *See* EX2060, 77:7-20. Instead, he speculated that Dour’s disclosure of “environmental conditions” and “physical characteristics” include characteristics of the communication line 205 (i.e., the communication line on the motherboard between the memory controller and the memory module). EX2060, 78:11-16, 79:19-80:3 (“...I think it includes the characteristics of the communication line 205”). But when confronted with the relevant disclosures in

Dour, he confirmed that these disclosures are directed to “the device” that terminates the signal. EX2060, 78:3-10, 80:4-11, 81:1-4.

The concept of PVT had an established meaning in the industry and a POSA would have understood Dour’s teachings to be consistent with this meaning. EX2058, ¶¶72-76. Specifically, PVT is used to refer to the process, voltage, and temperature of a device or circuit. *Id.* Process refers to the process used to fabricate the device, which dictates the device’s physical characteristics. *Id.* Voltage and temperature refer to the supply voltage and the operating temperature of the device, which are environmental or operating conditions of the device. *Id.* Accordingly, Dour’s teachings regarding PVT relate to the terminating device not the communication line that carries the signal to be terminated. *Id.*

Moreover, even if Dr. Wolfe was correct (which he is not) that the “physical characteristics” that Dour mentions is of the communication line 205, that is the communication line between the external memory controller and the memory module, as shown in Figure 2 of Dour below. EX1018, FIG. 2. Applied to Ellsberry, Dour’s teaching corresponds to the communication line between the system memory controller and Ellsberry’s control ASIC (for address and command signals) or Ellsberry’s switch ASIC (for data signals), not the communication line between the switch ASIC and the memory devices/banks. EX2058, ¶¶77-78.

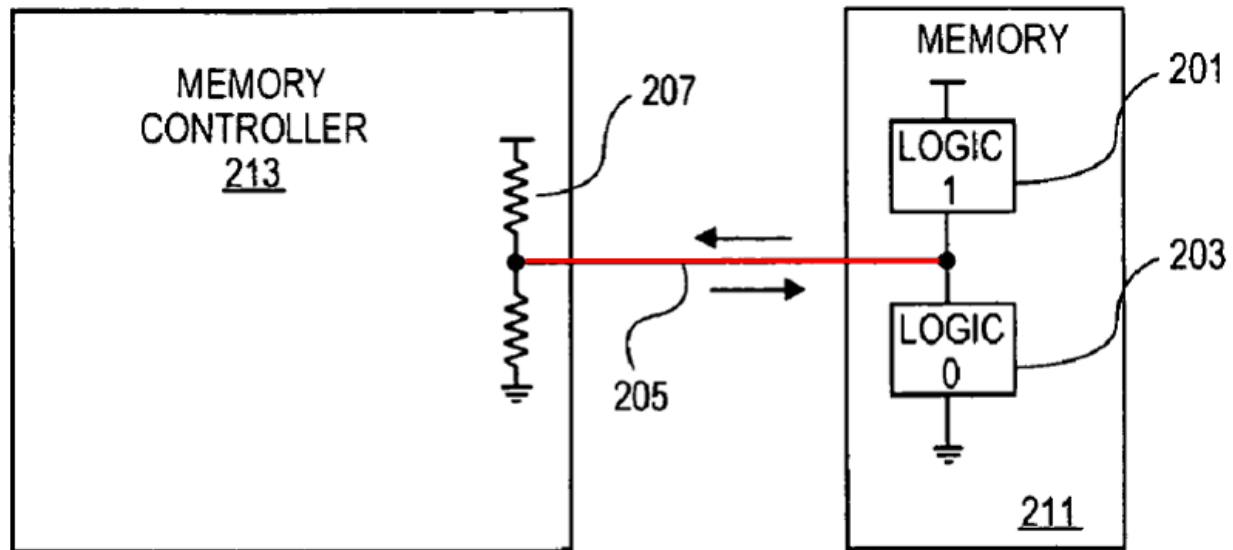


FIG. 2

EX1018, FIG. 2 (annotated).

3. A POSA would not have implemented Dour's ODT in Ellsberry's switch ASIC.

a. Dour's ODT circuitry is too slow.

Samsung argues that increases in the operating speed of memory devices would have motivated a POSA to implement Dour's ODT circuitry in Ellsberry's switch ASICs. *See, e.g., Pet.*, 47 (“a POSITA would have understood the importance of proper signal termination as the speed of memory operations increases”), 49 (“in order to provide reliable data transmission at the higher transmission speeds expected in 2008”), 52 (“To achieve such ‘higher communication speeds,’ a POSITA would have been motivated to use Dour's ODT functionality in Ellsberry's Switch ASICs.”), 75 (addressing element 1.f.2 and

arguing that switching between Ellsberry's banks "requires accurate, dynamic termination, especially at a high operating speed"). Specifically, Samsung proposes implementing (1) Dour's programmable ODT circuit in Ellsberry's bidirectional signal drivers 402 & 404 *and* (2) Dour's testing circuit 402 in Ellsberry's Control Block of Figure 4 (which Samsung colors gray). Pet., 71-72.

Although operating speed increased over time, Samsung is wrong that a POSA would have implemented Dour's ODT circuitry in Ellsberry's switch ASICs because Dour's ODT circuitry would have been too slow to handle high operating speeds. EX2058, ¶¶80-81. Dour's testing circuit 401 includes a circuit block 403, a finite state machine ("FSM") 405, and a feedback loop 409. EX1018, 3:65-4:3. Dour teaches that the FSM 405 encodes the "conditions of circuit block 403" into a signal that is used to adjust the ODT. EX1018, 4:4-20. These "conditions ... include the effects of the physical characteristics of the device, such as quality and type of manufacture, materials and similar physical characteristics, temperature, voltage, and similar device conditions have on [sic] the signal processed by block 403." EX1018, 4:7-12; *see also* EX1018, 4:12-15 ("In one embodiment, finite state machine 405 may encode the impedance of signals in block 403 based on the physical characteristics, voltage levels, and temperatures (PVT) of block 403."), 6:50-53 ("a testing circuit or similar component detects the physical conditions, voltage conditions and temperature conditions (PVT) of the component or on die

termination circuit (block 701).”), FIG. 7.

A POSA would have understood that the PVT characteristics of a device typically change slowly. EX2058, ¶82. Accordingly, a POSA would have known that Dour’s teaching of tracking and encoding PVT conditions into a driver signal that controls the programmable impedance circuit 500 does not have fast response. *Id.* To start, the feedback loop 409 that iterates toward a final value includes the finite state machine 405, which is a clocked circuit that nominally takes at least one clock cycle to determine its output. *Id.* The feedback loop 409 also includes the test block and two chip boundary crossings, which would have added additional latency. EX1018, FIG. 5. Further, Figure 6 shows the flowchart for the disclosed process for programming an on-die termination circuit. This flow chart includes a multiplier 601, which is an intrinsically complex operation. EX2058, ¶82 (citing EX1018, 5:45-63). And Figure 7 illustrates the disclosed process for programming an ODT circuit to adjust for conditions in a device. *Id.* (citing EX1018, 6:48-56). Figure 7 confirms that Dour’s ODT circuit that may take multiple clock cycles to reach step 707 with a new stable termination value. *Id.*

At bottom, Dour’s ODT circuitry was designed to identify and react to PVT conditions that change much slower than the high-speed bank switching required by Ellsberry. Accordingly, a POSA would not have been motivated to implement Dour’s ODT circuitry in Ellsberry’s switch ASICs, as Samsung proposes. EX2058,

¶83. Indeed, the significant delay that would be introduced by Dour's ODT circuitry would have dissuaded a POSA from making this combination. *Id.*

b. Ellsberry's lines are too short.

A POSA would not have been motivated to include Dour's ODT circuitry in Ellsberry's switch ASICs to terminate signals transmitted between Ellsberry's switch ASICs and memory devices because the length of the wires between the switch ASICs and memory devices is too short to be negatively affected by impedance mismatch. EX2058, ¶84. The '731 patent explains that signal wires should be considered "transmission lines" that require proper termination if the length of the wire is greater than or equal to a fraction of the wavelength of the signal, such as 1/2, 1/8, or 1/10 of the wavelength. EX1001, 9:63-10:6. This teaching was well-known "rule of thumb" in the industry that a POSA would have known about and followed. EX2058, ¶84.

Ellsberry discloses that "the control unit and bank switch combination may support SDRAM DDR1 and DDR2 specifications (incorporated herein by reference) with memory capacities of 256 Mb, 512 Mb, and 1 Gb in speed grades of 200/266/333/400 Mbps in DDR1 and capacities of 256 Mb, 512 Mb, 1 Gb, and 2 Gb in speed grades of 400/533 Mbps in DDR2." EX1005, ¶46. Accordingly, the highest operating speed that Ellsberry contemplates is 533 Mbps (Mbps means megabits per second per pin). EX2058, ¶85. Because the DRAMs are double data

rate (DDR), the clock frequency is half 533 Mbps, or 266.5 Mhz. EX2058, ¶85.

The wavelength of a 266.5 Mhz signal is about .55 m or 550 mm. EX2058, ¶85.

And 1/10 of this wavelength (the smallest that the '731 suggests would require signal termination) is 55 mm. EX2058, ¶85.

Dr. Wolfe testified that the length of the longest wire between Ellsberry's switch ASIC and DRAM chips would be about 30 mm. EX2060, 58:18-59:8. Specifically, he indicated that the wire shown in red below would be about 15 mm, and the wire shown in blue below would be about 30 mm. *Id.* Because 30 mm is less than 55 mm (or 1/10 the wavelength of a signal at Ellsberry's fastest operating speed), a POSA would have understood that no signal termination is required between Ellsberry's switch ASICs and memory devices and would not have been motivated to add additional, unnecessary circuitry to Ellsberry. EX2058, ¶85. For this additional reason, a POSA would not have been motivated to modify Ellsberry as Samsung proposes.

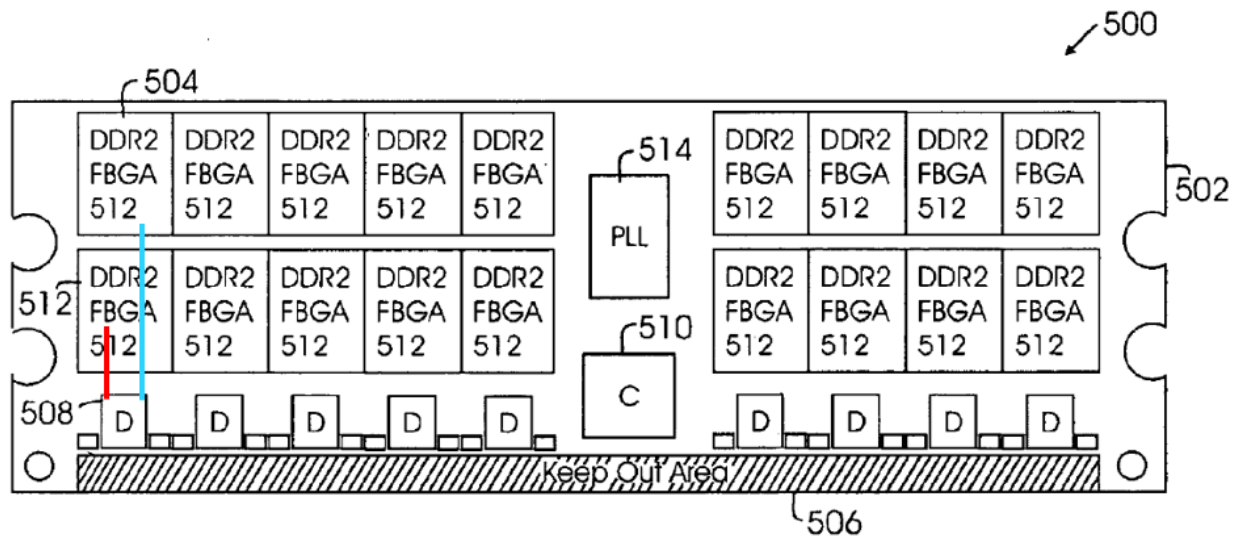


Fig. 5

EX1005, FIG. 5 (annotated).

E. Claim 6

Claim 1 recites “at least one circuit coupled between the at least one connector and the plurality of memory devices.” This at least one circuit “compris[es] a set of correction circuits” each of which “include[es] at least one programmable impedance matching circuit.” Claim 6 further recites that “each correction circuit ... includes *a delay circuit* that is configured to generate delayed versions of the signals transmitted between the respective port connection of the first set of port connections and the corresponding port connection in the second set of port connections.” Claim 6 thus requires that each “correction circuit” includes a “programmable impedance matching circuit” and a “delay circuit.”

Samsung relies on Ellsberry for claim 6. Pet., 83-86. Specifically, Samsung

alleges that Ellsberry's bidirectional signal drivers 402 & 404 are the claimed "delay circuit." Pet., 86. This argument fails for two reasons.

First, Ellsberry does not disclose that signal drivers 402 & 404 are a delay circuit. Indeed, Ellsberry's entire disclosure of the signal drivers is limited to part of a single sentence stating that "bidirectional signal drivers 402 & 404 ... transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks." EX1005, ¶45. Ellsberry says nothing more about them.

On cross-examination, Dr. Wolfe could not identify a "delay circuit." EX2060, 68:12-69:5. He testified that Ellsberry describes "latency extension circuitry" that is allegedly "in the switch ASIC." EX2060, 68:12-20. But when asked "[w]here in the switch ASIC would it be?" he replied, "*Oh, I don't know. As I said, it's described ... functionally as being part of the switch ASIC. ... I think it's in Elements 402 and 404 and controlled by the control block in Figure 4.*" EX2060, 68:21-69:5. Paired with Ellsberry's lack of disclosure, Dr. Wolfe's inability to identify any delay circuit confirms claim 6 is non-obvious.

Second, Samsung's theory primarily relies on two prior Board decisions involving materially different claims that recited "a latency parameter," not "a delay circuit." Pet., 83-86. Critically, neither decision found that Ellsberry's bidirectional signal drivers 402 & 404 are "a delay circuit," as recited in claim 6.

The Board in IPR2022-00639 analyzed a claim element of the '339 patent

that recited “a latency parameter.” EX1066, 37. It credited the petitioner’s expert, who testified that Ellsberry’s data buffers (i.e., switch ASICs) add some latency as compared to systems that do not include data buffers, and, to offset this latency, the latency of SDRAM chips is reduced by one clock cycle. EX1066, 46 (“Dr. Subramanian states that Ellsberry’s note should be understood as meaning that one cycle has been added to account for propagation delay through the data buffer so one cycle should be subtracted from the overall latency so that the system memory controller encounters the same delay it would have in the absence of the data buffer.”). The Board did not find that Ellsberry’s bidirectional signal drivers 402 & 404 are “a delay circuit.” EX1066, 43-47.

Similarly, the Board in IPR2018-00362 evaluated certain dependent claims in the ’907 patent that recited “a latency parameter.” EX1062, 62-63. Here, the Board simply held that “Posted CAS_n” in Ellsberry is a latency parameter but provided no further analysis of Ellsberry with respect to the relevant claims. *Id.* Again, the Board did not find that Ellsberry’s bidirectional signal drivers 402 & 404 are “a delay circuit.” *Id.*

In sum, Samsung fails to prove that Ellsberry discloses the “delay circuit” recited in claim 6 and the Board has not evaluated this feature in its prior decisions.

F. Secondary considerations confirm the claims are nonobvious.

“[E]vidence of secondary considerations may often be the most probative

and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not.” *Apple Inc. v. Samsung Elecs. Co., Ltd.*, 839 F.3d 1034, 1052-53 (Fed. Cir. 2016) (en banc) (quoting *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538-59 (Fed. Cir. 1983)). Evidence of secondary considerations “must be considered in every case where present,” *Apple*, 839 F.3d at 1048, and may be “crucial in avoiding the trap of hindsight ...,” *Leo Pharm. Prods., Ltd. v. Rea.*, 726 F.3d 1346, 1358 (Fed. Cir. 2013).

Licensing is an important secondary consideration that weighs on the obviousness inquiry. *Ancora Techs., Inc. v. Roku, Inc.*, 140 F.4th 1351, 1360 (Fed. Cir. 2025). “Actual licenses to the patented technology are highly probative ... because such actual licenses most clearly reflect the economic value of the patented technology in the marketplace.” *Ancora*, 140 F.4th at 1362 (quoting *LaserDynamics, Inc. v. Quanta Comput., Inc.*, 694 F.3d 51, 79 (Fed. Cir. 2012)). Here, two of the three most dominant players in the HBM market, RDIMM market, and the broader DRAM market—Samsung and SK hynix—took a license to the ’731 patent and its family members. EX2073, 2-3; EX2064, 2-3; EX2071, 6-7; EX2072, 6-7; EX2083, 2-3. Samsung fails to address these license agreements that it indisputably knew about prior to filing its Petition. *See generally* Pet. These licensing activities demonstrate the substantial value of ’731 patented technology

and support that the challenged claims are patentable.

1. Samsung’s license of the ’731 patent and Netlist’s patent portfolio proves the claims are valid and non-obvious.

a. Licensing activity between Netlist and Samsung

On November 12, 2015, Netlist and Samsung entered into a Joint Development and License Agreement (“JDLA”) under which Netlist granted Samsung a license to its intellectual property, including patents (e.g., U.S. Patent No. 8,154,901 (“’901 patent”), the earliest non-provisional in the ’731 family), continuations, and pending applications in the ’731 family (e.g., U.S. Application No. 13/715,491 (“’491 Application”), the application leading to the ’731 patent, which was pending at the time the JDLA was signed). EX2001, 1-2, 8; *see also* EX2006, 15 (expressly listing the ’491 Application). The JDLA enabled Samsung to use Netlist’s technology to develop DRAM memory products that are critical to current high-performance computing and AI applications, such as double data rate, 5th generation (DDR5) memory.

Netlist and Samsung concurrently entered into an agreement for convertible note financing (“Purchase Agreement”) under the terms of the JDLA, EX2001, 1, which was executed by Samsung’s “venture investment arm”: Samsung Venture Investment Corporation (SVIC). EX2005; EX2022, 2. The Purchase Agreement included a number of sub-agreements, including: (1) a Stock Purchase Warrant; (2) a Senior Secured Convertible Promissory Note (“Promissory Note”); (3) a Security

Agreement; and (4) an “Intellectual Property Security Agreement.” EX2002; EX2003; EX2004; EX2006, 5-16.

Under the JDLA and these ancillary agreements, Samsung provided significant value to Netlist: (1) a \$15 million loan collateralized by Netlist’s IP portfolio, (2) a payment of \$8 million for engineering fees, and (3) an agreement to supply DRAM and other memory to Netlist (“supply agreement”). Specifically, the Promissory Note provided Netlist with a \$15 million loan collateralized by Netlist’s IP portfolio. EX2003, 0001; EX2004, 2; EX2006, 0005. The Intellectual Property Security Agreement granted Samsung a security interest in Netlist’s patents and patent applications, including “divisions, continuations,” and “continuations-in-part.” EX2006, 0005. EX2004. The 78 individually identified assets spanned only 20 patent families and included the members of the ’731 patent family, including the pending application that led to the ’731 patent. EX2006, 15-16 (listing the ’491 Application and the ’901 patent, as well as U.S. Patent Nos. 8,782,350 and 9,037,809). The agreement required that Netlist “[p]rotect, defend, and maintain the validity and enforceability” of the assets. EX2004, 8. Thus, Samsung recognized the importance and value of Netlist’s patents (and relied on their validity) by requiring them as loan collateral.

Samsung also agreed to pay Netlist \$8 million in non-refundable, non-recurring engineering (NRE) fees, and to “supply NAND and DRAM products to

Netlist on Netlist's request at a competitive price." EX2001, 5-6. Samsung's agreement to supply Netlist with these products represented immense value given supply uncertainty expected in the market. EX2061, ¶¶17-19, 24-44.

In short, as a result of the November 2015 technology partnership, Samsung acquired a license to and a security interest in Netlist's IP portfolio (including the '731 patent and its family members), and provided significant value to Netlist for those rights. The value of Samsung's license is discussed further below.

b. Samsung's licensing activities evidence that the challenged claims were not obvious.

Typically, "to be accorded substantial weight in the obviousness analysis, the evidence of secondary considerations must have a 'nexus' to the claims." *Ancora*, 140 F.4th at 1361 (quoting *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1332 (Fed. Cir. 2019)). But "[u]nlike products, which may incorporate numerous features beyond those claimed or described in a patent and therefore may require careful parsing to establish a nexus, *actual licenses to the subject patent do not demand the same, as they are, by their nature, directly tied to the patented technology.*" *Ancora*, 140 F.4th at 1362 (emphasis added). That is because "actual licenses most clearly reflect the economic value of the patented technology in the marketplace." *Ancora*, 140 F.4th at 1362 (quoting *LaserDynamics*, 694 F.3d at 79).

In *Ancora*, the Federal Circuit considered licenses taken by other parties to

the subject patent as part of secondary indicia of non-obviousness. *Ancora*, 140 F.4th at 1362-64. The court instructed that “our case law does not require a parsing of specific claims for licenses.” *Id.* at 1363. Moreover, the court explained, a license to the patent “necessarily conveys a right to all of the challenged claims.” *Id.* “That other patents may have also been part of the license,” the court further noted, “does not detract from the nexus inquiry.” *Id.* at 1364. Therefore, the court found that the “evidence supports a nexus finding,” and that substantial weight should be accorded to those licenses. *Id.* at 1363. The same principles set out in *Ancora* apply to Samsung’s license to Netlist’s patent portfolio and strongly support the patentability of the challenged claims.

i. Samsung’s license to the ’731 patent should be accorded substantial weight.

Samsung licensed the ’731 patent and its parents as part of the JDLA. EX2001, 1-3, 8; EX2006, 15-16. *Ancora*, 140 F.4th at 1362-64. Samsung further recognized the value of that technology, taking a license to all patents, “including originals or divisions, continuations, [and] continuations-in-part,” “having an effective first filing date on or prior to” November 12, 2020. EX2001, 1-3.

Samsung’s voluntary participation in the JDLA further supports that substantial weight should be accorded to Samsung’s licensing activities. *See Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling USA, Inc.*, 699 F.3d 1340, 1349 (Fed. Cir. 2012) (“[L]icenses with companies under no apparent

threat of litigation” more likely “reflect the value of the claimed invention”); *Fox Factory Inc. v. SRAM LLC*, IPR2017-00472, Paper 64 at 45). Samsung entered into

the JDLA [REDACTED]

[REDACTED], which Samsung believed was [REDACTED] EX2080, 1 [REDACTED]

[REDACTED]. And [REDACTED]

[REDACTED]. EX2081, 1 [REDACTED].

Samsung’s recognition of the ’731 patent’s technology thus supports the patentability of the challenged claims. *Cirrus Logic, Inc. v. Greenthread, LLC*, IPR2024-00016, Paper 110 at 39-40 (finding nexus between a license to the patent application leading to the subject patent and the challenged claims); *Ancora*, 140 F.4th at 1362-64; *see also id.* at 1363 (recognizing “that which is disclosed could be the subject of a separate patent, such that a licensee might consider it prudent to take a license under both patents,” supports a finding of nexus); *Stratoflex*, 713 F.2d at 1539. Capitalizing on the technology disclosed in the ’731 patent, Samsung is one of the top producers of DRAM products. EX2073, 3; EX2071, 6-7; EX2072, 6-7; EX2083, 2-3; *Stratoflex*, 713 F.2d at 1539 (“Recognition and acceptance of the patent by competitors who take licenses under it to avail themselves of the merits of the invention is evidence of nonobviousness.”).

ii. The value of the license agreement is strong secondary indicia of non-obviousness.

Samsung's commitments to Netlist in return for patent licenses emphasize "the economic value of the patented technology in the marketplace." *Ancora*, 140 F.4th at 1362. Those commitments included an agreement to "supply NAND and DRAM products to Netlist on Netlist's request at a competitive price" during the term of the JDLA, \$8 million in non-recurring engineering (NRE) fees, and a collateralized loan in the amount of \$15 million. EX2001, 5-6; EX2002, 1; EX2004, 1. Samsung agreed that the collateral would include a security interest in and to all of Netlist's "patents, patent applications," and well as "divisions, continuations, ... and continuations-in-part of the same"—including the '731 patent and its family members. EX2006, 0005, 0012-0016; EX2004, 1.

As Netlist's expert Mr. Kennedy testifies, Samsung's agreement to supply Netlist with NAND and DRAM products during the term of the JDLA provided value substantially above the monetary payments made to Netlist. EX2061, ¶¶24-44. The supply agreement provided Netlist steady supply of NAND and DRAM products at competitive pricing, even in times of supply uncertainty. EX2061, ¶¶24-26. As Netlist's employees noted in the year after signing the JDLA, "we continue to benefit from the unique access we have [] to certain Samsung products in the enterprise space," including "high-density DRAM modules," which allowed Netlist to reach "customers not previously accessible." EX2061, ¶26 (citing

EX2076, 6; EX2077, 5-6).

From the first quarter of 2016 to the second quarter of 2017, Netlist's sales associated with purchase of Samsung products totaled approximately [REDACTED]. Netlist's [REDACTED] [REDACTED]. EX2061, ¶¶27-28.

In 2017, Samsung breached its supply agreement. EX2009, 1; EX2078, 15. Had Samsung continued to honor its supply agreement, however, Netlist's profits over the next five years (through 2022) resulting from that agreement would have totaled approximately [REDACTED]. EX2061, ¶¶29-41. And expected profits through 2027 would have totaled almost [REDACTED]. *Id.*

These benefits conferred to Netlist came at substantial cost to Samsung. EX2061, ¶¶42-43. The supply agreement “unambiguously create[d] a *mandatory obligation* on Samsung to supply certain types of products to Netlist *on request*,” and “to fulfill Netlist's requests for NAND and DRAM products *at a competitive price*”—regardless of the market demand or supply. EX2078, 7-8, 11 (emphasis added). Thus, Samsung was obligated to provide products to Netlist at a competitive price even in times of low supply or high demand, forgoing price increases and profit that it would have otherwise been able to achieve in the market. EX2061, ¶¶42-43.

Accordingly, the value conferred by Samsung for its license in Netlist's

intellectual property, including the '731 patent and its family members, amounted to at least \$23 million in monetary payments and [REDACTED] more in value resulting from Samsung's supply agreement. As in *Ancora*, these benefits provided to Netlist in exchange for patent licenses demonstrate the value placed on Netlist's patented technology. *Ancora*, 140 F.4th at 1362. Samsung's licensing activities, therefore, evidence the high "economic value of the patented technology in the marketplace" and should be accorded substantial weight in the Board's obviousness analysis. *Id.* (quoting *LaserDynamics*, 694 F.3d at 79).

2. SK hynix's license of the '731 patent supports the patentability of the challenged claims.

a. Background of licensing activity between Netlist and SK hynix

SK hynix's license to Netlist's patents further supports a non-obviousness finding. On April 5, 2021, Netlist and SK hynix entered into a licensing agreement under which Netlist granted SK hynix a license to its patent portfolio, including the '731 patent. EX2063, 1-2; EX2113, 2. Specifically, Netlist granted a term license to "any and all valid Patents owned or controlled by Netlist or any of its Subsidiaries at any time during the Term License Period," which ran through April 5, 2026. EX2063, 1-2; EX2113, 2. Those licensed patents included the '731 patent and its parents, which issued prior to execution of the license. EX2063, 1-2; EX2113, 2; EX1001, Cover (45), (63). In return for a license to the '731 patent,

among other patents in Netlist’s portfolio, SK hynix agreed to pay Netlist \$40,000,000—a number representing the high value SK hynix placed on Netlist’s patented technology. EX2063, 2.

Further in return for its patent license, SK hynix—like Samsung—entered into a supply agreement in which it agreed to “supply, or cause its Subsidiaries to supply, OEM-grade ... DRAM and NAND wafers, components, and finished products, as well as associated technical support, to Netlist.” EX2063, 2; EX2113, 2. The supply agreement “entitle[d] Netlist to purchase up to \$600,000,000 of SK hynix memory products during the term” of the agreement (five years). EX2113, 2. After announcement of this supply agreement, analysts commented that they saw “considerable value to the supply agreement to [Netlist], both supporting its current/future products for years,” and expected “re-sales revenues to ramp up over the next few quarters and boost existing re-sale revenue” due to the supply agreement. EX2061, ¶¶45-49 (citing EX2116, 1; EX2117, 1).

The value placed by SK hynix on licensing the technology in the ’731 patent and its family members is further confirmed by SK hynix’s success. SK hynix is one of the two leading suppliers of DRAM products globally. EX2073, 1-2; *see also* EX2072, 6-7 (showing SK hynix as one of the top players in the RDIMM market); EX2089, 3, 5 (showing SK hynix as the second-largest DRAM producer). In the first quarter of FY 2025 alone, SK hynix reported revenue of \$9.1 billion in

the United States, with much of that revenue attributable to DRAM-based memory. EX2015, 28; EX2065, 16 (showing 80% of revenue attributable to DRAM products). And SK hynix was forecasted “to reach \$49.6 billion” in DRAM revenue in 2025, demonstrating the value SK hynix placed on Netlist’s patented technology. EX2066, 2.

Under these facts, SK hynix’s decision to take a license to Netlist’s patent portfolio—including the ’731 patent—provides strong objective evidence that the challenged claims were not obvious.

b. SK hynix’s license strongly evidences that the challenged claims were not obvious.

Similar to *Ancora*, SK hynix—one of the dominant suppliers of DRAM products—took a direct license to the ’731 patent and its family members. EX2063, 1-3, 5-6; *Stratoflex*, 713 F.2d at 1539. Moreover, SK hynix’s significant \$40,000,000 payment for the licenses, along with its commitment to supply Netlist with DRAM and NAND products, emphasize “the economic value of the patented technology in the marketplace,” *Ancora*, 140 F.4th at 1362, as confirmed by the massive revenues generated through SK hynix’s DRAM sales. EX2066, 1; EX2067, 1; EX2065, 2-3. These facts demonstrate the industry’s desire for access to the technology covered by the ’731 patent.

Indeed, SK hynix itself touted its DDR5 DIMM development during the license term. For example, in September 2023, SK hynix announced publication of

a white paper “reveal[ing] that its DDR5 server DRAM applied to Intel’s CPUs demonstrated industry-leading performance levels.” EX2067, 1; *see also* EX2069, 2 (“SK hynix's DDR5 delivers an outstanding performance per watt[] and carbon emissions reduction effect to server customers ... while boosting performance by 70% or more.”). SK hynix further promoted its DDR5 RDIMM as one of the products “that garnered the most interest,” which SK hynix stated “offers outstanding performance” and “support[s] unprecedented transfer speeds.” EX2070, 3. And, SK hynix’s sales of DRAM products in the coming years reflect that value. *See* EX2015, 28; EX2065, 16; EX2066, 2.

The license agreement was reached as years-long litigation between the parties settled, including litigation in the Western District of Texas set for trial a mere two months after the license agreement was reached. *See* EX2068, 17. As in *Ancora*, SK hynix’s payment of \$40,000,000 and commitment to supply DRAM and NAND components to Netlist far exceeds the cost of typical patent litigation—and, more importantly, the remaining litigation costs—underscoring the value of the license to SK hynix. EX2061, ¶¶47-49; EX2079, 119 (in 2019, “the cost to litigate a patent in the United States average[d] about \$3.5 million”); *Ancora*, 140 F.4th at 1363 (“[C]lear evidence that substantial license fees were paid for licenses to a specific patent late in a litigation should be given the significance that their magnitude deserves. And while it is often cheaper to take licenses than to defend

infringement suits, ... that is certainly not the case here.”) (internal citations omitted).

* * *

Samsung knew of both SK hynix’s and its own licensing activities with Netlist. EX2039, 689:10-24 (testimony regarding SK hynix’s license taken on April 18, 2023, in prior litigation between Netlist and Samsung); *see also* EX2060, 87:7-15 (Samsung’s expert testifying that he “was aware that [Samsung] had licensed a large portfolio” of Netlist’s patents). Yet, Samsung and its expert wholly ignore this evidence in its Petition. As in *Ancora*, the Board should accord substantial weight to these licenses in its obviousness analysis and find the challenged claims patentable.

G. Samsung’s challenge to certain claims/claim elements is based solely on unsupported attorney argument because Exhibit 1093 is not sworn testimony that complies with Rule 42.53(a).

Samsung’s expert, Dr. Wolfe, addresses only a subset of the claim elements in his Declaration. EX1003, ¶125 (“In the paragraphs below, I focus on providing context and technical explanations related to specific limitations.”); EX2060, 16:1-17:20, 18:4-16. Instead of addressing all elements, he refers to Exhibit 1093, which is a 53-page, unsigned “claim chart” for both Grounds presented in the Petition. EX1003, ¶125; EX2060, 9:15-10:6. Dr. Wolfe mentions the chart only once (in ¶125) and does not even attempt to incorporate it by reference into his Declaration.

The Director and the Board should give no weight to Exhibit 1093. Rule 42.53(a) requires that “[u]ncompelled direct testimony must be submitted in the form of an affidavit.” 37 C.F.R. § 42.53(a). Exhibit 1093 is not in the form of an affidavit or declaration. More critically, it lacks a perjury statement and is unsigned. Therefore, it is not evidence in the form of sworn testimony that could support Samsung’s obviousness challenges.

Samsung’s challenge to certain claim elements is thus based solely on attorney argument—which “is not evidence.” *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017). Addressing claim 1, for example, Samsung alleges that Ellsberry *renders obvious* elements 1.b, 1.d, and 1.f.1. Pet., 60-61, 64-65, 73-74. But Dr. Wolfe does not address claim elements 1.b, 1.d, and 1.f.1 in his Declaration, even though the challenge relies on an obviousness analysis for these limitations. Nor does he address dependent claims 5, 8-9, 11-13, and 17. Accordingly, Samsung’s arguments with respect to these elements and claims amount to nothing more than attorney argument, which is insufficient to show that the claims are obvious.

VI. CONCLUSION

Samsung fails to meet its burden of persuasion. The Board should reject the Petition and find all of the challenged claims not unpatentable.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner Response complies with the type-volume limitation of 14,000 words, comprising 13,958 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).
2. This Patent Owner Response complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER RESPONSE**
UNDER 37 C.F.R. § 42.120 and Exhibits 2058-2132 were served in their
entireties on June 3, 2026, upon the following parties via electronic mail:

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