

Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment

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Abstract—A critical review is presented of the theories proposed in the literature to explain the current gain enhancement of polysilicon emitter bipolar transistors. From these theories a simplified analytical formulation is chosen which models the blocking properties of the interface, including tunneling through the interfacial oxide, reduced grain boundary mobility at the polysilicon/silicon interface, and the potential barrier created by segregated dopant, which can all give rise to an enhanced current gain. Also modeled are the mechanisms which limit the extent of any gain enhancement, such as recombination in the single-crystal emitter, in the bulk of the polysilicon, and at the polysilicon/silicon interface. This model is then applied in an original manner to a selection of experimental data in an effort to identify the dominant current gain mechanisms in polysilicon emitter transistors as a function of a given set of fabrication conditions.

For devices with a deliberately grown oxide layer at the polysilicon/silicon interface, an *oxide tunneling model* can fully explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. For devices without a deliberately grown interfacial oxide layer, two distinct types of behavior are observed. First, for low concentrations of arsenic in the polysilicon ($< 10^{20} \text{ cm}^{-3}$) and/or high anneal temperatures ($\geq 1000^\circ\text{C}$), recombination of carriers via interface states at the polysilicon/silicon interface dominates the base current. This results in a current gain which is degraded below that of an extended emitter device. Secondly, for higher concentrations of arsenic in the polysilicon ($1\text{--}2 \times 10^{20} \text{ cm}^{-3}$) and anneal temperatures around 900°C , the increased segregation of arsenic to the grain boundaries pacifies the interface states, resulting in an enhancement of gain compared to that for an extended emitter device. Pseudo-two-dimensional modeling of the discontinuous interfacial layer in these devices is undertaken, which shows that the base current flows primarily through those areas of the interface that are free from oxide. The base current is therefore controlled by the fraction of the interface which is oxide-free.

I. INTRODUCTION

SINCE the discovery of polysilicon emitters in the 1970's [1]–[3], they have moved from being a laboratory curiosity to become a vital part of many high-speed

bipolar [4], [5] and BiCMOS [6]–[8] production processes. The main reason for their success is that they provide a simple means of achieving the reductions in junction depth which are necessary when lateral device geometries are scaled. This co-ordinated scaling of lateral and vertical dimensions is important in order to provide an emitter structure in which the peripheral component of the emitter/base capacitance is maintained at a reasonable level. An important feature of polysilicon emitter technology is that reduced junction depths can be obtained without the degradation in gain which is obtained with conventional ion-implanted emitters [9]. On the contrary, an improvement in gain can be obtained, ranging from a factor of 3 [9] to 30 [10], with the size of the improvement depending upon the fabrication conditions used to produce the polysilicon emitter [11].

In spite of their widespread application, there is still considerable controversy over the precise mechanisms which control the current gain of a polysilicon emitter. Three physical mechanisms have been proposed to explain the improved gains of polysilicon emitter transistors. The first is termed the “*oxide tunneling model*” [3], [12] and explains the improved gains by tunneling through a thin oxide layer at the polysilicon/silicon interface. This model predicts not only a reduction in base current, and hence an improved gain, but also an increase in emitter resistance. The second is termed the “*grain boundary mobility model*” [9], [13], [14] and explains the improved gain by reduced mobility at the grain boundaries in the polysilicon and at the pseudo-grain boundary at the polysilicon/silicon interface. This model predicts a reduction in base current when the density of interface states at the grain boundaries is small, but an increase when the interface state density is high [14]. The third is termed the “*segregation model*” [15]–[17] and explains the improved gain by the presence of a potential barrier at the polysilicon/silicon interface due to the segregation of dopant. This model predicts a reduction in base current, with the amount of reduction depending upon the concentration of segregated arsenic at the interface. However, the “*segregation model*” predicts no change in emitter resistance. These three mechanisms can all be described as blocking mechanisms, since they are capable of giving an enhancement in gain compared with comparable con-

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ventional metal-contacted bipolar transistors. In order to fully explain the behavior of polysilicon emitters, it is necessary to also consider mechanisms which limit the extent of the gain improvement. These are mainly recombination mechanisms and include recombination at grain boundaries [14], recombination at the polysilicon/silicon interface [14], and recombination in the single-crystal emitter [18].

Since the publication of the above theoretical work, a large amount of experimental data has been gathered [19], which has greatly extended the understanding of the physical structure of the polysilicon emitter. High-resolution electron microscopy has been extensively used to study the polysilicon/silicon interface in detail, and has shown that a thin native oxide layer is invariably present [20]. The structure of the interfacial oxide depends critically upon the surface treatment carried out prior to polysilicon deposition [10], [20], with oxidizing chemical treatments giving a continuous oxide of approximately 14-Å thickness, and HF treatments giving a discontinuous oxide ranging in thickness from zero to around 8 Å. In oxide-free regions of the interface, epitaxial regrowth of the polysilicon occurs, extending typically a few hundred Angstroms into the polysilicon. In extreme cases, complete epitaxial regrowth of the polysilicon can occur [21] leading to a device with an extended single-crystal emitter [22]. The interfacial oxide structure also depends critically on annealing schedules [10], with oxide breakup being more likely for higher temperatures and thinner oxides.

Polysilicon emitter transistors and a variety of test structures have been fabricated in order to assess the importance of key processing parameters on the base current [3], [9]–[11], [23]–[41] and emitter resistance [29], [30], [42]–[48], and to obtain an insight into the mechanisms which control the device behavior. Specifically, the influence of the interface treatment [11], [45], the annealing temperature [10], the polysilicon thickness [28], [31], [37], dopant segregation [24], [28], and hydrogen passivation [28], [35] have all been studied. Many of the processing parameters have been shown to have a large influence on the device behavior, giving rise to changes in current gain by more than an order of magnitude.

In spite of this large amount of experimental and theoretical work, there is still considerable controversy over the precise mechanisms which control the base current of a polysilicon emitter transistor. Some of this controversy arises because of the different types of polysilicon emitter transistors which have been studied and the different fabrication conditions used to produce the devices. Another cause is the large number of competing mechanisms which can occur at the polysilicon/silicon interface and the resulting complexity of the device modeling. This paper will address these problems by first reviewing the competing theories for current gain enhancement, which will lead to a simple unified model for the base current of a polysilicon emitter transistor. The wide range of experimental data on polysilicon emitters will then be briefly reviewed,

and then re-assessed using this unified theory in an original manner. This approach will allow the identification of the mechanisms which control the current gain for a given set of fabrication conditions.

II. TYPES OF POLYSILICON EMITTER

Several types of polysilicon emitter have been studied in the literature, as illustrated in Fig. 1. In the first type (Fig. 1(a)), the n^+ dopant is confined to the polysilicon so that the metallurgical emitter/base junction coincides with the polysilicon/silicon interface. This structure is analogous to the MIS tunnel device [49], [50], and is therefore referred to here as a SIS emitter. Very high current gains have been reported for this structure [51]–[53], although the base characteristic is very nonideal, and is often accompanied by a “kink” at high emitter/base voltages. These disadvantages, and its poor current carrying capability [54], make it unsuitable for realizing high-speed circuits. This structure will therefore not be discussed in this paper, although, it should be pointed out that SIS behavior can be obtained in polysilicon emitters if the emitter/base junction is too shallow.

The second type of structure (Fig. 1(b)) is a polysilicon emitter in which the n^+ dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitter/base junction. The emitter/base depletion region therefore resides entirely in the single-crystal silicon, which leads directly to very ideal base characteristics. In order to obtain enhanced gain, the emitter/base junction depth must be shallower than the hole diffusion length in the single-crystal emitter, otherwise the gain is dominated by recombination in the single-crystal emitter. The crucial part of this structure is the polysilicon/silicon interface which can have a large effect on the base current of the transistor.

The third type of structure illustrated (Fig. 1(c)) is an extended emitter in which the n^+ polysilicon is replaced by single-crystal silicon. This can arise in practice if complete epitaxial regrowth of the polysilicon is induced during the emitter drive-in [21], [22]. The current gain is therefore unaffected by the interface, and hence it behaves like a conventional bipolar transistor. For the purposes of this paper this is a useful structure to consider, since a comparison of the gain of a polysilicon emitter with that of an identical extended emitter gives a measure of the gain enhancement or reduction resulting from the presence of the polysilicon/silicon interface.

Finally, the last structure shown (Fig. 1(d)) is that of a conventional metal-contacted emitter. In this type of device the emitter is formed by direct ion implantation into the silicon substrate, followed by a high-temperature anneal which is designed to activate the emitter dopant. When the emitter junction depth is scaled in such a device a reduction of current gain results because the emitter is transparent to the injected minority-carrier current [9]. This severe disadvantage precludes the use of metal-contacted emitters in high-speed bipolar processes.

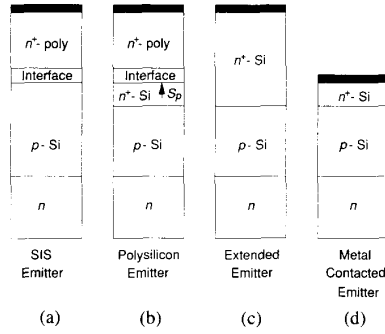


Fig. 1. Schematic diagrams of (a) an SIS emitter, (b) a polysilicon emitter, (c) an extended emitter, and (d) a metal contacted emitter.

III. EFFECTIVE RECOMBINATION VELOCITY

In this paper the polysilicon/silicon interface is modeled by using an effective recombination velocity S_p , which defines the recombination velocity at the lower side of the polysilicon/silicon interface, as shown in Fig. 1(b). In order to relate the effective recombination velocity to the base current, it is necessary to model recombination in the single-crystal emitter region. For a shallow emitter which is quasi-transparent, the base current can be modeled using the approach of del Alamo *et al.* [18]

$$J_{BO} = \frac{qn_{io}^2}{G_{\text{eff}}(W_E) + N_{D\text{eff}}(W_E)/S_p} \cdot \left[1 + \int_0^{W_E} \frac{G_{\text{eff}}(W_E) - G_{\text{eff}}(x)}{\tau_p(x)N_{D\text{eff}}(x)} dx + \frac{N_{D\text{eff}}(W_E)}{S_p} \int_0^{W_E} \frac{dx}{\tau_p(x)N_{D\text{eff}}(x)} \right] \quad (1)$$

where G_{eff} is the effective emitter Gummel number, $N_{D\text{eff}}$ is the “effective” doping concentration in the emitter, τ_p is the hole lifetime in the emitter, while $x = 0$ is defined to be the edge of the emitter/base depletion region, and $x = W_E$ is the position of the polysilicon/silicon interface.

The term in brackets in (1) represents a first-order correction for recombination in the single-crystal emitter, although, for the vast majority of devices analyzed in this paper recombination in the single-crystal emitter is negligible. The only notable exception to this is for devices with thick interfacial oxide layers. In order to calculate predicted values of base current to compare with reported experimental values in the literature, (1) is used together with measured emitter profiles, where available. In cases where the emitter profile is not given, a Gaussian profile is assumed in the single-crystal emitter, the Gaussian being constructed using estimates of the emitter/base junction depth and the doping concentration at the interface.

IV. CURRENT GAIN THEORIES

The general model to be used in this study to calculate the effective recombination velocity S_p follows from the unified model of Yu *et al.* [14], and is shown schemati-

cally in Fig. 1(b). It is assumed that the polysilicon layer consists of only one crystalline grain separated from the monosilicon substrate by an interfacial region of finite thickness, which will be described in detail further on. A density of interface traps is also assumed to exist at the two interfaces between the interface region and the polysilicon grain and the monosilicon substrate.

The effective recombination velocity S_p can be expressed as [14]

$$S_p = S_I + \left(\frac{1}{T_{\text{block}}} + \frac{1}{S_I + S_g} \right)^{-1} \quad (2)$$

where S_I models the recombination of minority carriers via traps at the interface, and is given by

$$S_I = \frac{1}{2} N_{it} c_p v_{th} \quad (3)$$

and N_{it} is the total density of interface traps per unit area, c_p is the capture cross section, and v_{th} is the thermal velocity. The factor of $1/2$ arises in (3) from interface traps being equally distributed between the upper and lower sides of the interface.

The parameter S_g describes the recombination of minority carriers in the bulk of the polysilicon grain, and is given by [14]

$$S_g = a_g - \frac{b_g^2}{a_g + S_M} \quad (4)$$

where

$$a_g = \frac{D_g}{L_g} \coth \left(\frac{W_p}{L_g} \right) \quad (5)$$

$$b_g = \frac{D_g}{L_g} \text{csch} \left(\frac{W_p}{L_g} \right)$$

D_g and L_g are the diffusivity and diffusion length, respectively, of minority carriers in the grain, S_M is the effective recombination velocity at the metal contact, and W_p is the polysilicon thickness.

The term T_{block} in (2) describes the blocking action of the polysilicon/silicon interface, and the expression used to calculate T_{block} is determined by the dominating mechanism. The three competing mechanisms are tunneling, reduced mobility in the pseudo-grain boundary at the interface, and thermionic emission over a segregation barrier. These will now each be considered in turn.

The *oxide tunneling model* was first proposed by de Graaff *et al.* [3], and later modified by Eltoukhy *et al.* [12]. The model assumes that a thin tunneling oxide is present at the polysilicon/silicon interface. Holes injected from the base into the emitter are forced to tunnel through the interfacial oxide layer, thereby blocking minority carrier flow into the polysilicon and hence producing a reduction in base current. The expression that will be used for T_{block} in the *oxide tunneling model* is summarized in Table I. Similarly, the majority-carrier electrons which flow from the polysilicon into the silicon must also tunnel

TABLE I
ANALYTICAL EXPRESSIONS USED FOR T_{block} IN THE THREE BLOCKING
MECHANISMS IN THIS STUDY

($b_h = 4\pi\delta/h\sqrt{2m_p^*}\chi_h$, $c_h = 2\pi\delta/h\sqrt{2m_i^*}/\chi_h$, χ_h is the barrier height to holes, m_p^* is the effective mass of holes in silicon, m_i^* is the effective mass of holes in the oxide, δ is the interfacial oxide thickness, μ_{pgb} is the minority-carrier mobility in the pseudo-grain boundary, Δ is the thickness of the pseudo-grain boundary, N_E is the electrically active doping density in the emitter, and N_{int} is the electrically active doping density of segregated dopant at the interface.)

Blocking Model	Expression Used for T_{block}
Oxide tunneling model	$T_{\text{block}} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{\exp(-b_h)}{1 - c_h kT}$ (6)
Pseudo grain-boundary mobility model	$T_{\text{block}} = \frac{kT}{q} \frac{\mu_{pgb}}{\Delta}$ (7)
Segregation model	$T_{\text{block}} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{N_E}{N_{\text{int}}}$ (8)

through the oxide. This limits the maximum current carrying capability of the device, since it gives rise to a series emitter resistance [43]–[45].

The *grain boundary mobility model* was first proposed by Ning *et al.* [9], who used it to explain electrical results obtained on transistors with conventional implanted emitters on top of which a layer of arsenic *in situ* doped polysilicon was deposited. A gain enhancement of a factor of 3 was achieved for the polysilicon emitters, compared to conventional metal-contacted emitters, which was attributed to a lower minority-carrier mobility in the polysilicon, when compared to single-crystal silicon. Eltoukhy *et al.* [13] extended the above simple two-region model to take into account the effect of grain boundaries on the minority carriers, which they assumed were infinitely thin, and characterized by a large concentration of interface states. Alternatively, Yu *et al.* [14] modeled the grain boundaries by assuming that they have a finite thickness, in which the minority-carrier mobility is reduced with respect to that in the bulk of the grain. Recombination is assumed to occur only at the interface between the grain and grain boundary, but not actually in the grain boundary. Furthermore, recombination at the polysilicon/silicon interface was also modeled. The grain boundaries can effect minority-carrier transport in two ways. First, if the density of interface states is large enough ($>10^{14} \text{ cm}^{-2}$) then they will act as efficient recombination centers, and no improvement in current gain will result over that for a metal-contacted emitter. However, for low densities of interface states ($\leq 10^{12} \text{ cm}^{-2}$), recombination at the grain boundary interface becomes negligible, and the minority-carrier transport is dominated by the reduced carrier mobility in the grain boundaries. This has the overall effect of lowering the minority-carrier mobility in the polysilicon layer, and so reducing the base current.

In this paper the polysilicon layer is assumed to consist of only one crystalline grain, although the disordered interfacial region will be treated as a pseudo-grain boundary

with a corresponding reduction in carrier mobility. This model will be termed the “*pseudo-grain boundary mobility model*,” and the expression used for the blocking recombination velocity T_{block} is summarized in Table I. A value for the pseudo-grain boundary thickness Δ will be chosen as 7 Å [55], which is consistent with the approximate thickness of a grain boundary in the bulk of the polysilicon. Typical values for the minority-carrier mobility in the pseudo-grain boundary μ_{pgb} can be several orders of magnitude less than the hole mobility in single-crystal silicon [56].

The *segregation model* was proposed by Ng *et al.* [15] to explain the observation that the current gain of polysilicon emitter transistors is dependent upon the amount of arsenic which segregates to the interface [24], [28]. Typically, the concentration of arsenic at the polysilicon/silicon interface can be a factor of two or three larger than the concentration of arsenic in the bulk of the grains. Ng *et al.* [15] argued that if the segregated arsenic is electrically active then this could form a low-high-low barrier, although the model will not predict any increase in emitter resistance. The expression that will be used for T_{block} in the *segregation model* is summarized in Table I [15].

It should be pointed out that the doping densities in (8) (see Table I) should strictly be effective doping densities, which include the effects of bandgap narrowing [57]. Since effective doping densities tend to saturate to a constant value as the doping concentration increases [58], this implies that the segregation barrier will be smaller than predicted in [15]. For example, for this mechanism to dominate the base current, the barrier created by the segregated dopant must be greater than about $2kT$. For a typical emitter doping concentration of 10^{20} cm^{-3} , this means that the segregated doping concentration must be greater than around $8 \times 10^{20} \text{ cm}^{-3}$ if the electrically active arsenic concentration is used, or greater than $10^{23} - 10^{24} \text{ cm}^{-3}$ if the effective doping concentration is used.

In order to obtain accurate predictions of effective recombination velocity and base current from doping profiles, it is necessary to take into account heavy doping effects, which influence parameters such as hole lifetime τ_p , hole mobility μ_p , and bandgap narrowing ΔE_g^{app} . Values for these parameters, as a function of doping, are taken from the work of del Alamo *et al.* [58]. Finally, it is necessary to assume values for some parameters for which measured values are not available. These are summarized in Table II, and the given values have been used throughout this paper unless otherwise stated.

V. EXPERIMENTAL RESULTS

Over the past ten years or so, a considerable amount of experimental results on polysilicon emitter transistors have been published in the literature [19]. In this section, approximately eight or so key papers have been chosen which are representative of a broad cross section of important experimental results. The results of these papers will be quoted in the form of raw experimental data (for

TABLE II
PARAMETER VALUES USED IN THIS STUDY

Parameter	Value	Reference
Hole effective mass in silicon (m_p^*)	$0.66m_0$	[12]
Hole effective mass in the interfacial oxide layer (m_i^*)	$0.42m_0$	[12]
Interface trap capture cross section $\times$ thermal velocity ($c_p v_{th}$)	$2 \times 10^{-9} \text{ cm}^3 \cdot \text{s}^{-1}$	[54]
Grain boundary thickness (Δ)	$7 \text{ \AA}$	[55]
Recombination velocity at metal contact (S_M)	$10^6 \text{ cm} \cdot \text{s}^{-1}$	[14]

example, measured current densities and resistances, etc.), and then *all* subsequent modeling will be performed in an original manner using the simplified analytical equations outlined in Section IV. This will allow a consistent comparison to be made between the predictions of the three blocking mechanisms and the reported experimental results.

A. Devices with Interfacial Oxides

1) *Effect of an Interface Anneal*: The analysis will begin by considering experimental results from devices with an interfacial oxide layer, which is generally grown using an oxidizing chemical treatment. It has been well documented in the literature that such an interface treatment gives a significant improvement in the current gain. For example, Ashburn *et al.* [11] have shown that devices given an RCA clean prior to polysilicon deposition had gains five times higher than those given an HF etch. A more detailed characterization of the influence of the interfacial oxide on the current gain was carried out by Wolstenholme *et al.* [10]. In this experiment, an interface anneal was carried out after polysilicon deposition, but prior to emitter implant, to thermally stress the interfacial oxide. In this way, a range of interfacial oxide structures was obtained without significantly altering the emitter and base doping profiles. The results are shown in Fig. 2 for devices given an RCA clean prior to polysilicon deposition. It is evident that a factor of 100 increase in base current is obtained as the temperature of the interface anneal is increased from 800 to 1100°C. These electrical results were correlated with high-resolution TEM observations of the polysilicon/silicon interface which showed that an interfacial oxide was present, which broke up by increasing amounts as the interface anneal temperature was increased.

High-resolution TEM showed that for interface anneal temperatures of 900°C or below, the interfacial oxide was continuous and uniform, with a thickness of $14 \pm 2 \text{ \AA}$. It is therefore possible to apply the *oxide tunneling model* unambiguously to these results. Fig. 2 shows the modeled values of base current (using (6) of Table I and the parameters in Table II) for different values of oxide barrier height, assuming that the devices are tunneling-dominated (i.e., $S_i = 0$ and $T_{\text{block}} \ll S_g$). It is evident that these devices can be modeled by an oxide barrier height

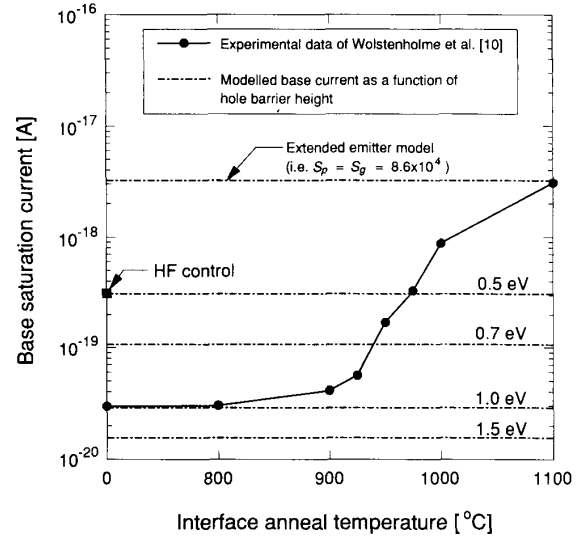


Fig. 2. Experimental data of Wolstenholme *et al.* [10] showing base saturation current as a function of interface anneal for devices with a deliberately grown interfacial oxide layer. The base current has been modeled by assuming that the dominant blocking mechanism is tunneling through the interfacial oxide layer (i.e., *oxide tunneling model* with $\delta = 14 \text{ \AA}$, and $S_i = 0$). Also shown is the modeled base current using the *extended emitter model* ($T_{\text{block}} = \infty$, and $S_i = 0$).

of 1.0 eV. Also modeled in Fig. 2 is the base current of an extended emitter device, in which no blocking or recombination at the interface is assumed to occur (i.e., $T_{\text{block}} = \infty$ and $S_i = 0$). As can be seen, a good fit to the 1100°C interface anneal device is achieved, which implies that the interface has no effect on the base current of this device. This conclusion is consistent with the TEM analysis, which showed that the interfacial oxide had completely “balled-up,” such that 97% of the interface was oxide-free. These experimental results show that the interfacial oxide plays a dominant role in controlling the current gain of polysilicon emitter transistors with deliberately grown interfacial oxide layers.

Rutherford backscattering (RBS) analysis has been used by Wolstenholme [57] to investigate the distribution of arsenic at the interface for the devices reported in Fig. 2. The results of this analysis are shown in Fig. 3, and indicate that the concentration of arsenic at the polysilicon/silicon interface remains unchanged for interface anneals up to a temperature of 1000°C. Applying the *segregation model* to the barriers produced in Fig. 3 for the RCA control device, produces a blocking recombination velocity of either $7.9 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$ (no bandgap narrowing), or $1.2 \times 10^6 \text{ cm} \cdot \text{s}^{-1}$ (with bandgap narrowing). This compares with an extracted T_{block} of $3.2 \times 10^2 \text{ cm} \cdot \text{s}^{-1}$ for the control device in Fig. 2, which therefore implies that the *segregation model* cannot explain the experimental results in either Figs. 2 or 3.

2) *Temperature Dependence of Current Gain*: Further evidence supporting the *oxide tunneling model* is obtained from measurements of the temperature dependence of cur-

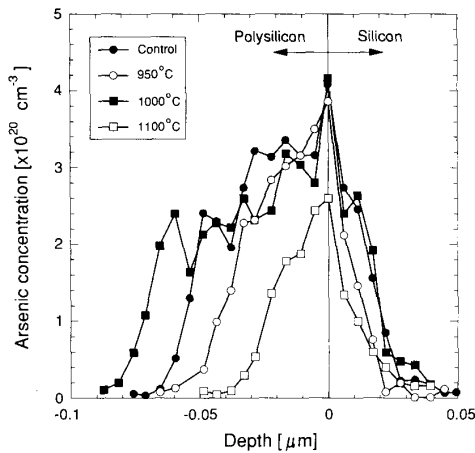


Fig. 3. Experimental data of Wolstenholme [57] showing Rutherford backscattering (RBS) arsenic profiles of the polysilicon/silicon interface for devices with a deliberately grown interfacial layer, subjected to various interface anneals.

rent gain. Several authors [2], [3], [11] have reported that polysilicon emitter transistors with a chemically grown interfacial oxide have a gain which varies less strongly with temperature than observed for conventional metal-contacted transistors. Fig. 4 shows the current gain, as a function of inverse temperature, from the work of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11]. Also shown in Fig. 4 is the temperature dependence of current gain for a conventional metal-contacted transistor (whereby the temperature dependence of the current gain is determined by the difference in bandgap narrowing in the base and emitter). It can be seen, especially for temperatures above 300 K, that the current gain becomes less sensitive to temperature than in conventional metal-contacted transistors. In fact, the results from de Graaff *et al.* [3] even show a negative temperature coefficient. Ashburn *et al.* [11] modeled the temperature dependence of gain, and showed that the *oxide tunneling model* could explain the observed results for the whole temperature range in Fig. 4.

3) *Emitter Resistance*: The presence of a deliberately grown oxide layer at the polysilicon/silicon interface has been shown to block majority-carrier flow, leading to an increase in emitter resistance [43]–[45]. Measurements of specific interfacial resistivity for devices with deliberately grown interfacial oxide layers typically range from 200 to 500 $\Omega \cdot \mu\text{m}^2$ [43]–[45]. This compares with generally far lower values of 10 to 200 $\Omega \cdot \mu\text{m}^2$ [29], [43], [45] for devices without deliberately grown interfacial oxide layers. By applying the *oxide tunneling model* to the devices with interfacial layers, assuming an average oxide thickness of 14 Å [10] and an electrically active polysilicon doping level of $5 \times 10^{19} \text{ cm}^{-3}$ [10], implies a barrier height to electrons of around 0.3 eV (using the analytical expression for emitter resistance derived in [30]). Comparing this value with the barrier height for holes, which is around 1 eV (Fig. 2), it can be clearly seen that there

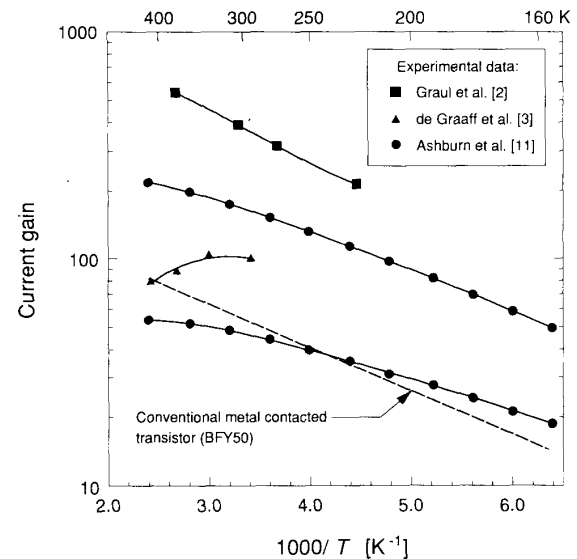


Fig. 4. Experimental data of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices with a deliberately grown interfacial oxide layer. It can be clearly seen that the temperature dependence of current gain is less than that for a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

exists an asymmetry in oxide barrier heights for electrons and holes.

Wolstenholme *et al.* [45] have performed experiments on the “balling-up” of the interfacial oxide from interface anneals, and then correlated this with measurements of emitter resistance, as shown in Fig. 5. Also shown in Fig. 5 are the base current data from Fig. 2. Some important differences can be seen in the variation of the base current and emitter resistance with interface anneal temperature. Most notable is a substantial reduction in emitter resistance for the device given a 900°C interface anneal, compared to the control device, even though the TEM analysis showed that the interfacial layer for both devices was continuous and unbroken. Two-dimensional modeling by Hamel *et al.* [59], as shown in Fig. 6, has recently shown that this result can be explained if a limited number of widely spaced small gaps in the oxide layer are produced in the 900°C interface anneal, even though nearly 99% of the oxide remains continuous (and so therefore these gaps would be difficult to observe by TEM). Since a large proportion of the interface remains intact, a reduction in base current is still obtained, as observed in Fig. 2. These results show that it is possible to produce a device with both a high gain and a low emitter resistance [60].

Measurement and modeling of the temperature dependence of emitter resistance for devices with deliberately grown interfacial oxide layers has been conducted by Yung *et al.* [46]. They found that the *oxide tunneling model* could fit the observed temperature dependence, although the shape of the tunneling barrier had to be

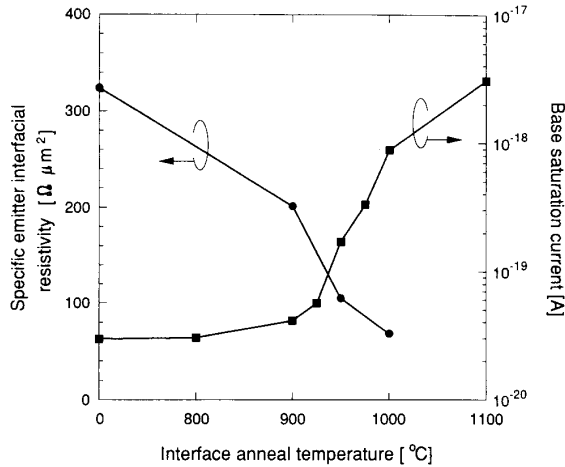


Fig. 5. Experimental data of Wolstenholme *et al.* [10], [45] showing the specific emitter resistivity and base saturation current as a function of interface anneal temperature for devices with a deliberately grown interfacial oxide layer.

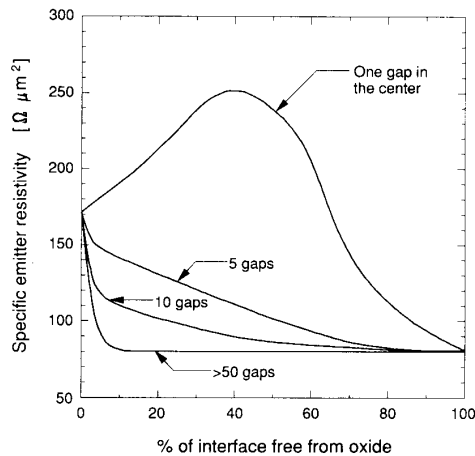


Fig. 6. Modeled specific emitter resistivity as a function of the percentage of the interface which is oxide-free for a device with a HF interfacial treatment, from the work of Hamel *et al.* [59]. It can be clearly seen that not only the amount of oxide, but its distribution along the interface can dramatically effect the emitter resistance.

changed from rectangular to triangular. Yung *et al.* [46] speculated that dopant pileup at the interface was the physical cause of this change in barrier shape.

4) *p-n-p Polysilicon Emitter Transistors*: As an aid to understanding the physics of polysilicon emitter transistors it is worthwhile here to examine the experimental results from p-n-p polysilicon emitter transistors [61]–[63]. The extracted values of barrier height ($\chi_h = 1.0$ eV and $\chi_e = 0.3$ eV) from measurements on n-p-n polysilicon emitter transistors imply that p-n-p transistors should have a high emitter resistance and a small gain improvement. In practice, however, this is found not to be the case. Reported values of current gains for p-n-p polysilicon emitter transistors with deliberately grown interfacial ox-

ide layers, are between a factor of 2 [61] and 10 [63] times higher than for devices without a deliberately grown interfacial layer. Furthermore, the emitter resistance of p-n-p polysilicon emitter transistors, with an interfacial oxide layer, are only approximately a factor of 2–3 [61]–[63] higher than for the corresponding devices without a deliberately grown interfacial layer. If the *oxide tunneling model* is used to extract oxide barrier heights to holes and electrons, the values of barrier height of $\chi_h = 0.3$ eV and $\chi_e = 1.0$ eV [63] are seen to be inconsistent with those obtained from measurements on n-p-n transistors. Further work is therefore needed on the *oxide tunneling model* to explain this discrepancy.

B. Devices Without an Interfacial Oxide Layer

For commercial applications, devices without a deliberately grown interfacial oxide layer are generally preferred because of the emitter resistance problem described above. However, it should be pointed out that an interfacial layer is invariably present at the polysilicon/silicon interface, even in devices given an HF etch prior to polysilicon deposition [10].

1) *Segregation of Dopant to the Interface*: Confirmation of the role of the interface in controlling the gain comes from the work of Neugroschel *et al.* [24], who have fabricated bilayer polysilicon diodes by first depositing undoped polysilicon and then capping the device with *in situ* arsenic-doped polysilicon. Drive-in conditions were carefully chosen so that the amount of arsenic segregated to the polysilicon/silicon interface could be varied. A long low-temperature drive-in (e.g., 64 h at 800°C) was used to preferentially diffuse the arsenic along the grain boundaries, and dope the grain boundaries and interface to a concentration of around $5 \times 10^{20} \text{ cm}^{-3}$. However, the temperature of the drive-in was not high enough to diffuse arsenic into the bulk of the grains [64], which remained at a low concentration of $\leq 10^{18} \text{ cm}^{-3}$. This device was then compared to both an unannealed bilayer device (with a low arsenic concentration of $\leq 10^{18} \text{ cm}^{-3}$ in the grains and at the interface), and to a control device with a single *in situ* doped polysilicon layer (with an arsenic concentration of $\sim 10^{21} \text{ cm}^{-3}$ at the interface and around $5 \times 10^{20} \text{ cm}^{-3}$ in the grains).

Fig. 7 shows the current–voltage characteristics for the annealed and unannealed bilayer devices, and the *in situ* doped monolayer polysilicon control device. Also shown is the characteristic for a metal-contacted control with no polysilicon layer. It can be seen from Fig. 7 that the current from the annealed bilayer device is nearly identical to the monolayer control. However, these two devices have *different* doping concentrations in the bulk polysilicon ($\sim 10^{18} \text{ cm}^{-3}$ and $5 \times 10^{20} \text{ cm}^{-3}$, respectively), but have *similar* concentrations of arsenic at the polysilicon/silicon interface (5×10^{20} – 10^{21} cm^{-3}). It can thus be concluded that the *concentration* of arsenic at the polysilicon/silicon interface is important in controlling the hole current. In addition, the hole current from the metal-con-

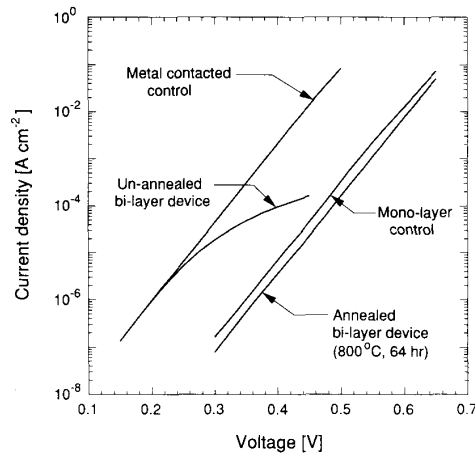


Fig. 7. Current-voltage characteristics of the diodes as analyzed by Neugroschel *et al.* [24]. The devices shown are the metal-contacted control, the single-layer polysilicon control, and the annealed and unannealed bi-layer devices.

tacted control is almost identical to that of devices with low arsenic concentrations at the interface, which implies the density of interface states is so large as to recombine all the minority holes at the interface. An interface state density of $6 \times 10^{14} \text{ cm}^{-2}$ can be calculated by using (1), assuming that the hole current is entirely dominated by recombination at the interface (i.e., $T_{\text{block}} = \infty$, and $S_f \gg S_g$ so that $S_p = 2S_f$ in (2)).

For the devices with a high arsenic concentration at the interface, a dramatic reduction of hole current by a factor of 600 is obtained. Assuming that the hole current is again dominated by recombination at the interface ($T_{\text{block}} \approx 0$, so that $S_p = S_f$ in (2)) then an upper limit of $2 \times 10^{11} \text{ cm}^{-2}$ can be obtained for the interface state density. The increase of segregated arsenic from 10^{18} to $5 \times 10^{20} \text{ cm}^{-3}$ at the interface has therefore reduced the interface state density by over a factor of 3000.

The above results demonstrate the importance of recombination via states at the polysilicon/silicon interface, and also its relationship to the segregated arsenic concentration. Patton *et al.* [28] have also shown that recombination at the interface cannot be ignored, particularly when the doping concentration in the polysilicon is low. Fig. 8 shows the measured base current as a function of polysilicon doping level for various emitter drive-in conditions. Nearly all the devices have large base currents at low polysilicon doping levels ($3 \times 10^{19} \text{ cm}^{-3}$), which fall to minimum values around $1\text{--}2 \times 10^{20} \text{ cm}^{-3}$ and then rise for increased doping levels up to $5 \times 10^{20} \text{ cm}^{-3}$. Also shown in Fig. 8 is the modeled base current from the extended emitter model (i.e., $T_{\text{block}} = \infty$ and $S_f = 0$, so that $S_p = S_g$ in (2)), which can qualitatively explain the increase in base current at high values of doping ($2\text{--}5 \times 10^{20} \text{ cm}^{-3}$) by increased Auger recombination in the bulk polysilicon. However, the extended emitter model cannot explain either the sharp increase in base current at the low polysilicon doping levels of $3 \times 10^{19} \text{ cm}^{-3}$, or the reduc-

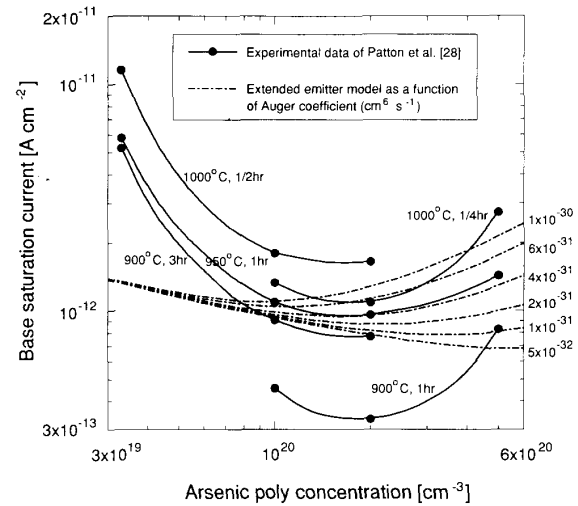


Fig. 8. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for various emitter anneals. Also shown is the modeled base current as a function of Auger coefficient in the polysilicon, assuming that no blocking or recombination mechanisms exists at the interface (i.e., the extended emitter model with $T_{\text{block}} = \infty$, $S_f = 0$). The polysilicon is assumed to be 40% electrically active and consisting of only one crystalline grain.

tion in base current for the devices annealed at 900°C for 1 h. It can therefore be concluded that a recombination mechanism is dominating at low polysilicon doping levels, while a blocking mechanism is dominating the 900°C 1-h devices.

Fig. 9 shows the modeled values of base current as a function polysilicon doping for various interface state densities, assuming no blocking action at the interface (i.e., $T_{\text{block}} = \infty$, so that $S_p = 2S_f + S_g$ from (2)). The case for $N_{it} = 0$ is that for the extended emitter model (i.e., $S_p = S_g$). The modeling clearly demonstrates that a constant value of interface state density cannot model the base current, especially at low arsenic concentrations. Patton *et al.* [28] argued that the arsenic segregation could lower the trap density at the interface. Fig. 10 models the base current of the device annealed at 950°C for 1 h, by the combined contribution of recombination via interface states (for interface densities as a function of arsenic concentration) and minority-carrier transport in the bulk polysilicon (assuming no blocking action at the interface, i.e., $T_{\text{block}} = \infty$). A reasonable fit to the measured base current can result, if it is assumed that the interface state density reduces from 2×10^{14} to $1.4 \times 10^{13} \text{ cm}^{-2}$, as the arsenic concentration increases from 3×10^{19} to $2 \times 10^{20} \text{ cm}^{-3}$.

Fig. 11 shows the fitted interface state density, as a function of polysilicon doping, for all the drive-in conditions in Fig. 9. Also shown are the modeled results from Neugroschel *et al.* [24], who used low-temperature drive-ins of 800°C , and the modeled results from Meister *et al.* [37] who used rapid thermal annealing at 1050°C . The most immediate trend visible is that of a dramatic reduction in interface state density for increases in arsenic con-

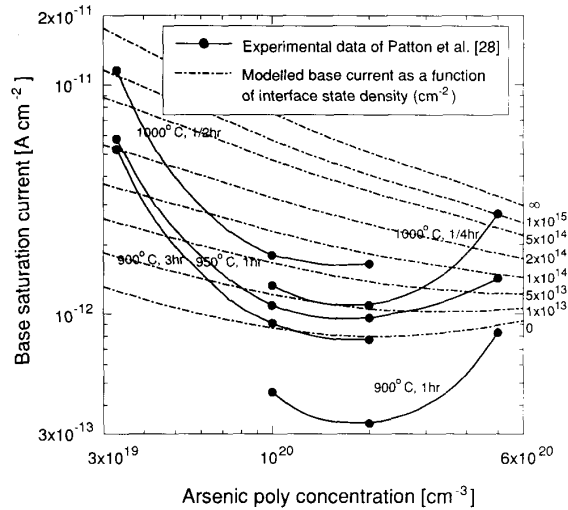


Fig. 9. Experimental data of Patton *et al.* [28]. Also shown is the modeled base current as a function of interface state density, assuming no blocking at the interface (i.e., $T_{\text{block}} = \infty$). The modeled base current for a metal-contacted control is also shown (i.e., $N_H = \infty$). The polysilicon is assumed to be 40% electrically active.

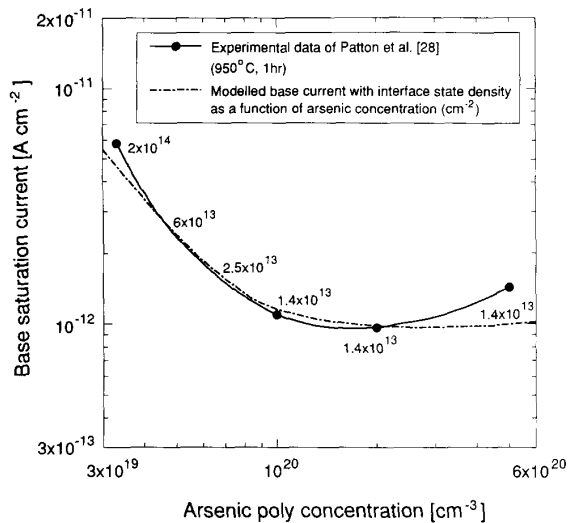


Fig. 10. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 950°C for 1 h. Also shown is the modeled base current as a function of interface state density, assuming that the interface state density varies with arsenic concentration in the polysilicon. No blocking action is assumed to occur at the interface (i.e., $T_{\text{block}} = \infty$), and the polysilicon is assumed to be 40% electrically active.

centration from 3×10^{19} to 10^{20} cm^{-3} . This behavior can be explained by the passivation of the interface states due to segregation of arsenic to the interface. There is, however, a second trend in the results of Fig. 11, which reveals that in most cases the largest interface state densities are obtained for the highest anneal temperatures. This result is consistent with the findings of Mandurah *et al.* [65], who found that arsenic segregation to grain boundaries

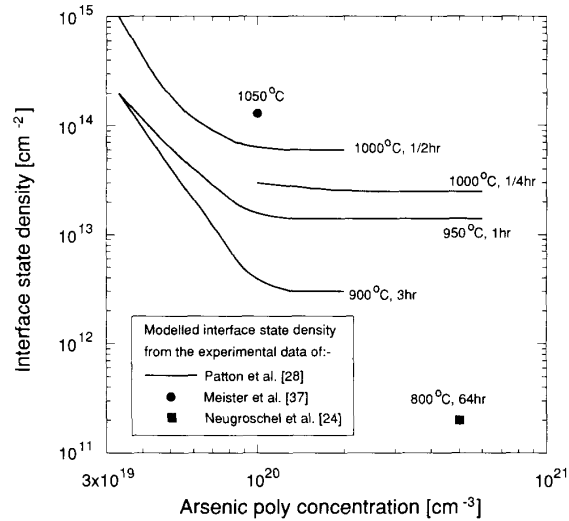


Fig. 11. Modeled interface state density as a function of arsenic concentration in the polysilicon, and polysilicon anneal, for devices with no deliberately grown interfacial oxide layers. Experimental data are from Patton *et al.* [28], Neugroschel *et al.* [24], and Meister *et al.* [37].

increases as the anneal temperature is reduced. If it is assumed that the segregation properties of grain boundaries are similar to those for the pseudo-grain boundary at the polysilicon/silicon interface, then this can explain the reduction of interface state density with anneal temperature.

Turning now to the 900°C device annealed for 1 h, the base current shows a reduction by a factor of 2.5 (for polysilicon doping concentrations of $1\text{--}2 \times 10^{20} \text{ cm}^{-3}$) from the *extended emitter model* (Fig. 8), which suggests that a blocking mechanism at the interface is controlling the base current. Fig. 12 shows the experimental data and the modeled base current as a function of the effective recombination velocity S_p . An effective recombination velocity of $2.7 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$ can be fitted to the base current for polysilicon concentrations of $1\text{--}2 \times 10^{20} \text{ cm}^{-3}$. Assuming that the effective recombination velocity is dominated by a blocking mechanism at the interface (i.e., $S_l = 0$ and $T_{\text{block}} \ll S_g$), then the *pseudo-grain boundary mobility model* can be used to model this fitted value of recombination velocity. This results in a minority hole interface mobility $\mu_{p\text{rgb}}$ of $0.1 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, which is a reduction in hole mobility by a factor of 1500 compared with the mobility in the bulk emitter.

The *segregation model* predicts a barrier to minority carriers of around $0.9 kT$ (using the SIMS analysis in [28]) for the devices annealed at 1000°C, if the segregated arsenic at the interface is electrically active. Assuming a similar barrier exists for devices annealed at 900°C, then this barrier yields a recombination velocity of $7.5 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$ (no bandgap narrowing), or $8.1 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$ (with bandgap narrowing). These values of blocking recombination velocity are clearly too large to model the extracted recombination velocity, and so the *segregation model* cannot account for the reduction in base current in Fig. 12.

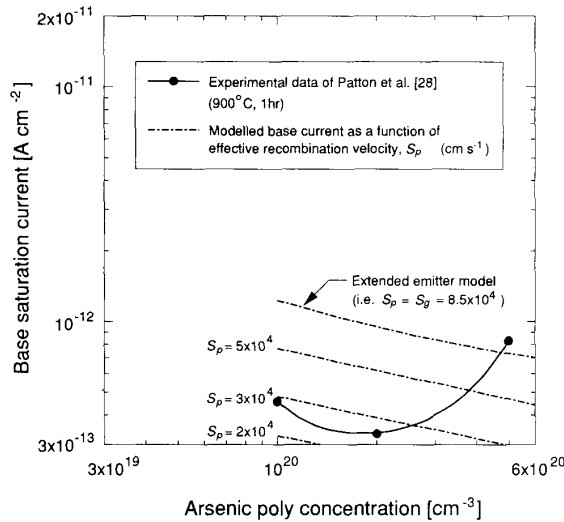


Fig. 12. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 900°C for 1 h. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the *extended emitter model* (i.e., with $T_{\text{block}} = \infty$ and $S_I = 0$). The polysilicon is assumed to be 10% electrically active.

2) *Polysilicon Thinning*: The influence of the polysilicon layer on the current gain has been studied by several authors [28], [37] who have made measurements on polysilicon emitter transistors in which the polysilicon layer has been thinned after the emitter drive-in. The results of Meister *et al.* [37] are typical and are shown in Fig. 13. It can be seen that the base current remains constant down to a thickness of less than 10 nm, which shows that the base current is dominated by the blocking/recombination properties of the polysilicon/silicon interface, even in devices without a deliberately grown interfacial oxide layer. Also shown in Fig. 13 is the modeled base currents as a function of polysilicon thickness. Equation [1] was used to convert the modeled effective recombination velocity into a base current, and the emitter Gummel number was extracted from the metal contacted control. The device was first modeled by the *extended emitter model* (i.e., curve 1 with $T_{\text{block}} = \infty$ and $S_I = 0$), and as can be clearly seen it is impossible to model both the metal-contacted control and the variation of base current with polysilicon thickness. Decreasing T_{block} to $5 \times 10^5 \text{ cm} \cdot \text{s}^{-1}$ (curve 2, with $S_I = 0$) enables the base current of the metal-contacted control and the polysilicon emitter device with an emitter thickness of 90 nm to be both modeled. However, for polysilicon thickness between 0 and 90 nm the model cannot be fitted to the base current. Further reductions in T_{block} to $1 \times 10^5 \text{ cm} \cdot \text{s}^{-1}$ (curve 3), allows the constant base current with polysilicon thickness to be modeled, but at the expense of being unable to model the absolute value of base current. The only way to remedy this situation is for the interface state recombination velocity (S_I) to take values other than zero. Curve 4 in Fig. 13 shows that an excellent fit to the experimental data can

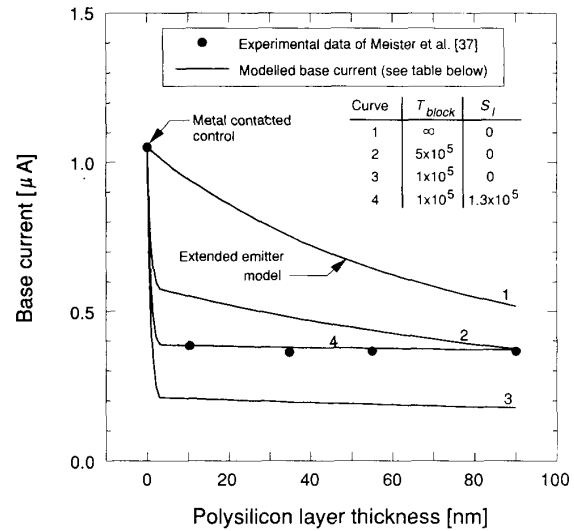


Fig. 13. Experimental data of Meister *et al.* [37] showing base current ($V_{be} = 0.66 \text{ V}$ and $A_E = 15.5 \times 15.5 \mu\text{m}^2$) as a function of polysilicon thickness. Also shown is a metal-contacted control with zero polysilicon thickness. The modeled base current is shown as a function of interface state density and blocking recombination velocity. Also shown is the modeled base current using the *extended emitter model* (i.e., $T_{\text{block}} = \infty$, $S_I = 0$). S_M is taken to be equal to infinity, and S_g is a function of polysilicon thickness.

be made with $T_{\text{block}} \leq 10^5 \text{ cm} \cdot \text{s}^{-1}$, and $S_I \geq 1.3 \times 10^5 \text{ cm} \cdot \text{s}^{-1}$, which corresponds to an interface state density which must be greater than $1.3 \times 10^{14} \text{ cm}^{-2}$.

3) *Temperature Dependence of Current Gain*: The temperature dependence of the current gain for devices without a deliberately grown interfacial layer has been experimentally measured by Ashburn *et al.* [11], and is shown in Fig. 14(a) and (b). They found that the temperature sensitivity of the current gain was *greater* than that of conventional metal-contacted transistors, especially at higher temperatures. This temperature dependence differs markedly to that of devices with deliberately grown interfacial oxide layers (i.e., dominated by tunneling), which show a far *lower* temperature sensitivity at higher temperatures. Fig. 14(a) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *oxide tunneling model*. It is clear that the model cannot explain the observed temperature dependence (especially at higher temperatures), and so it can be concluded tunneling is not the dominant mechanism in devices without deliberately grown interfacial oxide layers.

Fig. 14(b) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *pseudo-grain boundary mobility model*. If it is assumed that the interface hole mobility is temperature-independent, then the temperature dependence of the current gain is controlled by the difference in the bandgap narrowing between the base and emitter, as in a conventional metal-contacted device (shown as the $n = 0$ curve in Fig. 14(b)). However, a fit cannot be made to the measured current gain, which implies that the hole mobility must be tem-

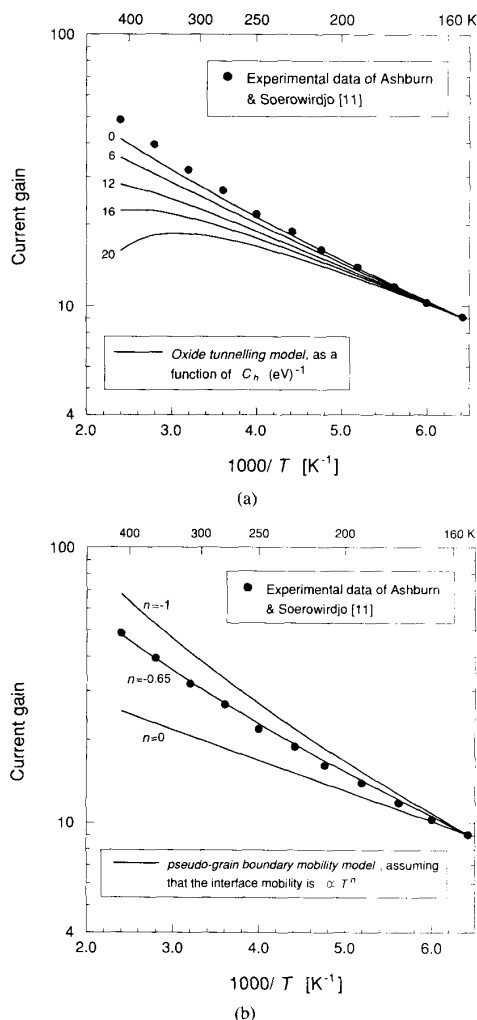


Fig. 14. (a) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the oxide tunnelling model (assuming $S_i = 0$, and $T_{block} \ll S_g$), as a function of the parameter c_h (in (6)). (b) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the pseudo-grain boundary mobility model (assuming $S_i = 0$, and $T_{block} \ll S_g$). The interface mobility (μ_i) is assumed to be proportional to T^{-n} . The $n = 0$ case corresponds to the temperature dependence of a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

perature-dependent. If it is assumed that the interface hole mobility has a dependence of the form $\mu_i = AT^{-n}$ (where A is a temperature-independent constant), then an excellent fit to the experimental data can be achieved for $n = -0.65$.

4) *Effect of an Interface Anneal:* Wolstenholme *et al.* [10] have performed the same interface anneal experiments with HF devices as with RCA devices, and the results are shown in Fig. 15. These results show that the base current increases by a factor of 5.5 as the interface

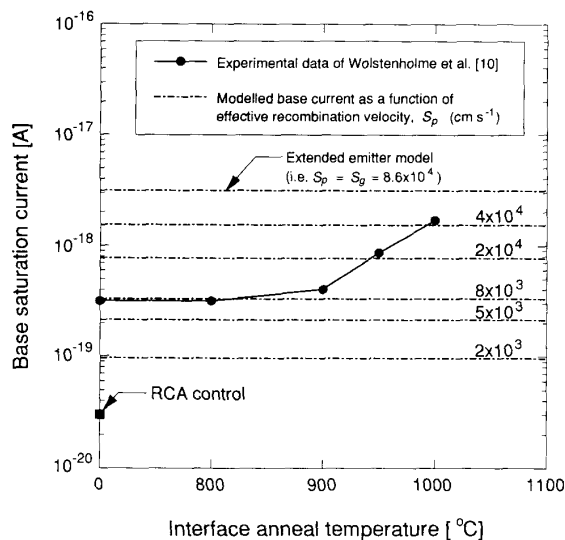


Fig. 15. Experimental data of Wolstenholme *et al.* [10] showing the base saturation current as a function of interface anneal for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the extended emitter model (i.e., with $T_{block} = \infty$ and $S_i = 0$).

anneal temperature is increased from 800 to 1000 $^{\circ}C$. Also shown in Fig. 15 is the modeled base current as a function of effective recombination velocity S_p , and the modeled base current using the extended emitter model. Transmission electron microscopy (TEM) reveals that a dip-etch in hydrofluoric acid (HF) prior to polysilicon deposition (which is designed to remove any interfacial oxide), nevertheless produces a uniform oxide of approximately 4-Å thickness. After typical anneals at 900 $^{\circ}C$, thermal stressing causes the thin HF oxide to break up, leading to a discontinuous layer varying in thickness from 0 to 8 Å, and with approximately 30% of the interface oxide-free. This compares with the 1000 $^{\circ}C$ interface anneal device, in which 90% of the interface is oxide-free. These results clearly indicate that the interfacial oxide controls the base current in a HF device. It is tempting to conclude, therefore, that tunneling through the interfacial oxide is the dominant mechanism, even in HF devices. However, as already shown in Fig. 14(a), this conclusion is inconsistent with the measured temperature dependence of the current gain, which is markedly stronger for the HF devices than for the RCA devices. In order to explain this apparent inconsistency, it is necessary to consider how a discontinuous interfacial oxide can be modeled in two dimensions.

C. Modeling a Discontinuous Interfacial Layer

Very little has been published on the two-dimensional modeling of the polysilicon/silicon interface, although Hamel *et al.* [59] have simulated the majority carrier flow in a polysilicon emitter as a function of oxide breakup. Their simulations revealed that the majority-carrier cur-

rent flow had a large lateral component, which was required to explain the observed decrease in emitter resistance with oxide breakup [45]. Recent attempts to model the minority-carrier flow at the polysilicon/silicon interface in two dimensions [66] have shown that the current flow is primarily through those regions of the interface free from oxide. Hence the lateral component of the minority-carrier flow can be largely ignored, and this is the approach followed in this paper.

The effect of a broken up interfacial oxide layer on the base current is modeled by assuming that the emitter can be treated as two polysilicon emitter transistors connected in parallel, one with an interfacial oxide layer and the other without. The area of the interface which is oxide-covered is denoted by A_{ox} , and that which is oxide-free by A_{nox} . Each of these areas of the interface can then be described by an effective recombination velocity S_{pox} (dominated by the *oxide tunneling model*) and S_{ppgb} (dominated by the *pseudo-grain boundary mobility model*). The overall recombination velocity S_p can then be calculated as a weighted mean of these two contributions

$$S_p = S_{pox} \left(1 - \frac{A_{nox}}{A_{EW}} \right) + S_{ppgb} \left(\frac{A_{nox}}{A_{EW}} \right) \quad (9)$$

where A_{EW} is the total emitter window area. Wolstenholme [57] and Gold [67] have used (9) to model the base current of polysilicon emitters as a function of the fraction of interface which is oxide-free, and the results are shown in Fig. 16 for devices with a deliberately grown interfacial oxide layer. Also shown are some of the modeled recombination velocities from the experimental results in Figs. 2 and 15. The value of S_{pox} used in Fig. 16 for the situation of no oxide breakup has been fitted from the base current of the RCA control device. As the oxide breaks up, high-resolution TEM has shown [10], [67] that it becomes thicker in some regions and thinner in others, with the overall oxide volume remaining constant. In order to model the tunneling current through the oxide-covered regions (the first term in (9)), S_{pox} has been calculated for each of the RCA devices, assuming an initial oxide thickness of 14 Å and a constant oxide volume. The result of these calculations is shown as the dashed line in Fig. 16. It is clear that, apart from the very early stages of oxide breakup ($A_{nox}/A_{EW} \leq 0.1$), the overall recombination velocity S_p is dominated by the second term in (9). This means that the majority of the hole current in a device with a broken up interfacial oxide flows through the oxide-free regions. Thus the factor of a 100 increase in base current of the RCA device with an interface anneal of 1100°C compared to the control (Fig. 2), can be partly explained as simply the increase in area of those portions of the interface which are free from oxide.

Another factor which is likely to influence S_p is the epitaxial regrowth of the polysilicon through the holes in the interfacial oxide [10], [67]. This regrowth is likely to affect the value of the pseudo-grain boundary recombination velocity S_{ppgb} , since the grain boundary moves further

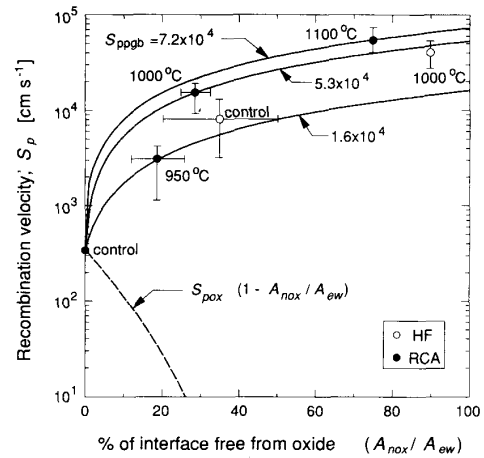


Fig. 16. Modeled recombination velocity S_p as a function of the fraction of the interfacial layer which is oxide free, for devices with a deliberately grown interfacial oxide layer (using (9)). Also shown is a selection of the modeled experimental base currents from Figs. 2 and 15. The modeled recombination velocity is only strictly relevant for those devices with a deliberately grown interfacial oxide layer (RCA). The dashed line corresponds to only the first term in (9).

into the polysilicon as the oxide breaks up. Extra recombination in the single-crystal emitter would therefore be expected, which would be seen as an increase in S_{ppgb} . The effect of a change in the value of S_{ppgb} is illustrated in Fig. 16, whereby to model the base currents of the RCA devices, S_{ppgb} has to increase from 1.6×10^4 to $7.2 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$ as the interface breaks up and the polysilicon epitaxially regrows. This corresponds to an increase in pseudo-grain boundary mobility from 0.043 to $0.195 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$.

Turning now to the devices without deliberately grown interfacial layers (HF devices), the modeling is somewhat complicated since there exists no "control" device (i.e., a device with a uniform 4 Å oxide at the interface). Nevertheless, if it is assumed that the value of S_{pox} used in (9) is much less than S_{ppgb} , then the modeled curves in Fig. 16 are still valid for the HF devices. The difference in recombination velocity between the control HF device and the 1000°C interface anneal device is a factor of 5.5, while the difference in the oxide-free area at the interface is only a factor of 3. The fact that the base current increases more than predicted by the difference in areas of the oxide-free regions of the interface can be explained by an increase in the value of the pseudo-grain boundary recombination velocity, S_{ppgb} from 2.4×10^4 to $4.4 \times 10^4 \text{ cm} \cdot \text{s}^{-1}$. This therefore corresponds to an increase in pseudo-grain boundary mobility by a factor of only 1.8 from 0.065 to $0.12 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. It can therefore be seen that the increase in base current of an HF device subjected to an interfacial anneal is determined mostly by the increase in the fraction of the interface which is oxide-free, though there is also a small contribution (a factor of 1.8 compared with a factor of 3) from an increase in the pseudo-grain boundary recombination velocity, S_{ppgb} due

to the epitaxial regrowth of the polysilicon. Moreover, the base current of the HF control device is dominated by current flow through the gaps in the interfacial oxide, with the result that the dominant mechanism is the reduced minority-carrier mobility at the interface, which is in agreement with the temperature dependence of current gain in Fig. 14(b).

VI. CONCLUSIONS

This paper has critically reviewed theories in the literature on the current gain enhancement of polysilicon emitter bipolar transistors, and then applied these theories in a consistent manner to the published experimental data. In this way, it has been possible to identify the dominant physical mechanisms for a given set of fabrication conditions. In devices fabricated with a deliberately grown interfacial oxide layer, tunneling through the interfacial oxide layer can explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. In devices fabricated without a deliberately grown interfacial oxide layer, two distinct regions of device behavior have been identified. First, for low concentrations of arsenic in the polysilicon ($<10^{20} \text{ cm}^{-3}$) and/or high anneal temperatures ($>1000^\circ\text{C}$), recombination of carriers via interface states at the polysilicon interface dominates the base current. This results in a current gain which is lower than that for an extended emitter device. Secondly, for arsenic concentrations of $1\text{--}2 \times 10^{20} \text{ cm}^{-3}$ and anneals around 900°C (as used in many commercial processes), the increased segregation of arsenic to the interface pacifies the interface states. These devices exhibit a gain enhancement compared with an extended emitter device. In order to fully explain this gain enhancement, it is necessary to model the discontinuous interfacial oxide in two dimensions. The use of a simple pseudo-two-dimensional model shows that the oxide covered regions of the interface are opaque to minority carriers, so that most of the current flows through the gaps in the oxide. The base current is therefore determined primarily by the fraction of the interface which is oxide-free, and hence is very sensitive to the detailed structure of the interfacial oxide. The dominant base current mechanism is thus reduced minority-carrier mobility in the pseudo-grain boundary at the polysilicon/silicon interface.

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