

An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations

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A comparison is made between the results of high-resolution electron microscope observations and the electrical characteristics of polycrystalline silicon emitter bipolar transistors. Devices are fabricated with and without a deliberately grown interfacial oxide layer, and the thermal stability of this oxide layer is investigated by carrying out a preanneal at temperatures between 800 and 1100 °C after polysilicon deposition, but prior to emitter implant and 900 °C drive-in. The electron microscope observations show that the deliberately grown interfacial oxide is of uniform thickness ~ 14 Å, but breaks up when annealed at ~ 950 °C and above, with "balling-up" occurring at ~ 1100 °C. This correlates with a transistor gain that decreases from ~ 1400 to ~ 40 . The electron microscopy also shows that a thin interfacial oxide layer is present even when not deliberately grown. This oxide breaks up when annealed at ~ 900 °C and above, with "balling-up" occurring at ~ 1000 °C. This correlates with a transistor gain that decreases from ~ 240 to ~ 50 . Calculations of the effect that such interfacial oxide layers will have on the characteristics of polysilicon emitter bipolar transistors are made, and these predictions correlate well with the measured characteristics.

I. INTRODUCTION

Polycrystalline silicon ("polysilicon") is now widely used in bipolar technology as a means of making contact to the emitter and base of the transistor¹ and this can lead to a dramatic improvement in both switching speed and packing density.^{2,3} An additional advantage of using a polysilicon emitter is that an improvement in gain by a factor of between 3 and 30 can be obtained compared with conventional transistors.⁴ This improvement in gain can be partly attributed to the transport properties of the polysilicon⁵ although this mechanism can only explain an improvement by a factor of ~ 3 . The much larger gain improvements are obtained when a thin interfacial oxide layer is deliberately introduced between the polysilicon and single-crystal silicon.^{4,6,7} In this case the gain improvement can be attributed to tunneling through this oxide layer.⁸ Eltoukhy and Roulston,^{9,10} and later Yu *et al.*,¹¹ have published unified theories that incorporate both these mechanisms, the former giving a solution suitable for numerical implementation, the latter a versatile analytical solution.

If high-gain polysilicon emitter transistors incorporating an interfacial oxide layer are to be used in commercial integrated circuit processes, it is important that the oxide layer is fully characterized in terms of thickness and uniformity, and that it is stable during subsequent high-temperature processing. Our previous structural studies¹²⁻¹⁶ showed

that the oxide layer progressively breaks up during high-temperature heat treatments. In order to investigate this behavior in more detail and to relate it directly to device performance, we have carried out a detailed comparison of electrical results on polysilicon emitter transistors with structural results from high-resolution transmission electron microscopy. The thermal stability of the oxide layer was investigated by carrying out preanneals at temperatures between 800 and 1100 °C immediately after polysilicon deposition but prior to emitter implant and drive-in at 900 °C. In this way, the oxide layer could be subjected to a high-temperature heat treatment without significantly affecting the rest of the emitter structure, and therefore changes in gain could be correlated directly with changes in the structure of the oxide layer.

II. EXPERIMENT

Two types of polysilicon emitter bipolar transistor were fabricated using identical standard processing up to the surface treatment of the (100) silicon slices prior to polysilicon deposition. For the first type (RCA treatment), the slice was given a dip in buffered HF followed by an RCA clean⁴ ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ as 1:1:5 for 10 min; $\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ as 1:1:6 for 10 min) to produce a surface oxide layer of nominal thickness ~ 15 Å. For the second type (HF treatment), the slice was given a dip in buffered HF with the intention of

removing any native oxide which might have been present.⁴ These surface layer treatments were immediately followed by the deposition of a $\sim 0.4\text{-}\mu\text{m}$ -thick layer of undoped LPCVD polysilicon at $\sim 610^\circ\text{C}$. One of each type of slice was given a 10 min preanneal in dry nitrogen at one of several temperatures in the range $800\text{--}1100^\circ\text{C}$ in order to breakup the interfacial oxide layer to different extents. The emitters of the transistors were then formed by implanting $1 \times 10^{16}\text{-cm}^{-2}$, 70-keV As^+ into the polysilicon and driving it in at 900°C in wet oxygen for 30 min. The active emitter area was $20\text{ }\mu\text{m}$ by $18\text{ }\mu\text{m}$. The aluminium contact to the emitter was remote from the active emitter area, being made a via polysilicon track $60\text{ }\mu\text{m}$ in length.

Detailed electrical measurements were carried out on the transistors including measurements of collector and base current as a function of base/emitter voltage. Unpatterned check slices which had been given identical base and emitter processing were used for the TEM studies. Cross sections were prepared corresponding to the $(01\bar{1})$ plane of the (100) single-crystal silicon slice by grinding, polishing, and argon ion-beam thinning. These were examined using a JEOL 200CX TEM with the electron beam aligned parallel to the $[01\bar{1}]$ direction of the single-crystal silicon. High-resolution electron microscopy (HREM) was performed to give lattice images using conventional procedures. All of the specimens examined (except for that of Fig. 6) corresponded to the final processed slices and so the observed TEM structures could be directly correlated with the device results. Large numbers of micrographs were taken of each specimen in order to determine its characteristic structure. The micrographs of Figs. 1–6 are typical of those obtained, but do not show all the features described in the text.

III. TEM RESULTS

For specimens given in an RCA treatment, a 900°C preanneal and full processing (As^+ implant and 900°C drive-in), cross-section micrographs of the interface region showed the single-crystal silicon with the characteristic (111) , $(\bar{1}\bar{1}1)$, and (200) lattice planes clearly delineated (Fig. 1). The individual polysilicon grains only showed lattice planes when the grains were favorably oriented with respect to the electron beam, e.g., as at A. When such planes were observed in the individual polysilicon grains, they were in general not aligned with the planes present in the silicon.

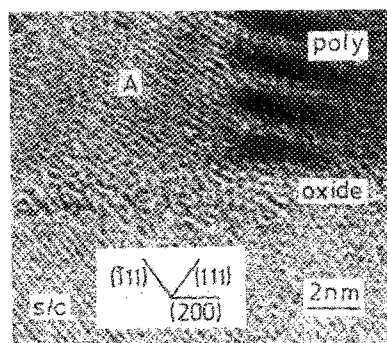


FIG. 1. HREM micrograph of a fully processed specimen given an RCA treatment and a 900°C preanneal. Note the interfacial oxide layer and the polysilicon grain A. s/c—single-crystal silicon; oxide—interfacial oxide layer; poly—polysilicon layer.

The interfacial oxide layer was seen as a thin bright band separating the silicon from the polysilicon. The band exhibited a random wormlike contrast in the lattice-image micrographs, this being the characteristic behavior for an amorphous material. The oxide layer was continuous and uniform with a thickness of $\sim 14 \pm 1 \text{ \AA}$ and it followed the undulations of the surface of the silicon slice with an “amplitude” of $\sim 6\text{--}9 \text{ \AA}$ (perpendicular to the interface) and a “wavelength” of $\sim 200\text{--}400 \text{ \AA}$ (parallel to the interface). The good uniformity of the oxide layer indicates that its structure had been little changed by the subsequent 900°C preanneal and 900°C drive-in, and so Fig. 1 shows it in effect as it was when initially produced by the RCA treatment. The directly measured oxide layer thickness of $14 \text{ \AA}$ is in good agreement with the values of $13\text{--}15 \text{ \AA}$ obtained from ellipsometry,¹⁷ and $10\text{--}15 \text{ \AA}$ obtained from Auger spectroscopy profiles,¹⁸ for silicon slices given an RCA treatment. The TEM results are summarized in Table I.

For specimens given an RCA treatment, a 950°C preanneal and full processing, the interfacial oxide layer was non-uniform (Fig. 2). Some regions had increased in thickness to a maximum of $19 \text{ \AA}$, some regions were thinner, and in some regions holes (B) were present in the layer. Small areas (C) of the polysilicon had been regrown through such holes to become single-crystal material with the same crystallographic orientation as the underlying silicon, this being deduced from the micrograph contrast and the alignment of

TABLE I. Summary of results.

Silicon slice surface treatment	Preanneal temperature (°C)	Interfacial oxide layer		Polysilicon			Transistor gain
		Geometry	Maximum thickness (Å)	Fraction of interface regrown	Grain size (Å)		
					Surface	Bulk	
RCA	900	continuous	~ 14	0	1200	400	1400
RCA	950	broken up	~ 19	0.3	1200	600	350
RCA	1000	broken up	~ 22	0.7	1200	1000	90
RCA	1100	balled up	~ 55	0.97	2000	1000	40
HF	None	broken up	~ 8	0.2	1200	400	240
HF	1000	balled up	~ 50	0.95	1200	1000	50

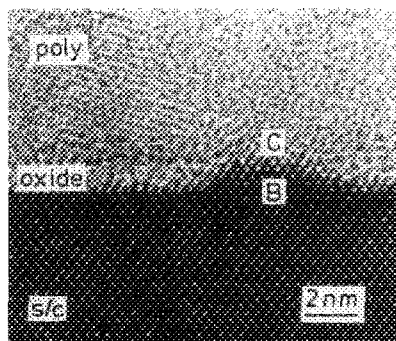


FIG. 2. HREM micrograph of a fully processed specimen given an RCA treatment and a 950 °C preanneal. Note the hole B in the interfacial oxide layer and the regrown polysilicon area C.

the lattice planes. The regrown areas had often spread out laterally in the polysilicon and so were sometimes wider than the holes in the oxide layer through which they had been grown. Individual areas extended typically 35 Å along the interface and 35 Å into the polysilicon. When the individual lengths of the regrown areas of the polysilicon were measured along the interface and added together, this represented ~ 0.3 of the total length of the interface.

For the specimens given an RCA treatment, a 1000 °C preanneal and full processing (micrograph not included), the breakup of the interfacial oxide layer was more pronounced. Some regions had increased in thickness to a maximum of 22 Å, and more holes were present in the layer. However, no substantial "balling-up" of the layer had occurred. Individual regrown areas of the polysilicon extended typically 120 Å along the interface and 40 Å into the polysilicon. The fraction of the length of the interface that had regrown was ~ 0.7 .

For specimens given an RCA treatment, a 1100 °C preanneal and full processing, the breakup of the interfacial oxide layer was almost complete (Fig. 3), the layer now consisting mainly of balls of oxide (D) up to 55 Å in diameter or worms $\sim 30 \times 100$ Å across. Individual regrown areas of the polysilicon overlapped to give almost complete coverage of the interface with the regrowth extending typically 170 Å into the polysilicon. The large difference between the

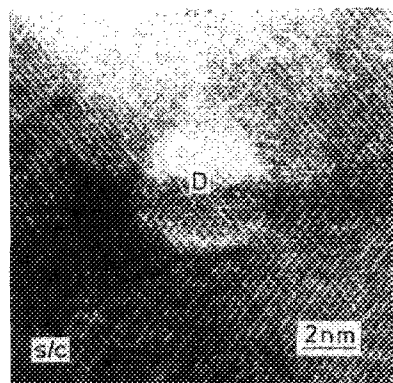


FIG. 3. HREM micrograph of a fully processed specimen given an RCA treatment and an 1100 °C preanneal. Note the balled-up oxide D.

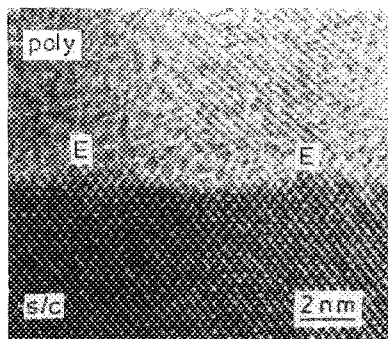


FIG. 4. HREM micrograph of a fully processed specimen given an HF treatment and no preanneal. Note the regrown polysilicon areas E.

oxide layer in the specimens given the 950, 1000, and 1100 °C preanneals, and the specimen given the 900 °C preanneal, indicates that the breakup of the oxide in the 950, 1000, and 1100 °C specimens occurred during the preanneals.

For specimens given an HF treatment, no preanneal and full processing, an interfacial oxide layer was present but it was not continuous (Fig. 4). In some regions it was up to a maximum thickness of 8 Å, in other regions it was thinner, and in some regions there were holes. Small areas (E) of the polysilicon had regrown through the holes, individual areas extending typically 25 Å along the interface and 25 Å into the polysilicon. The fraction of the interface that had been regrown was ~ 0.2 .

For specimens given an HF treatment, a 1000 °C preanneal and full processing, the breakup of the interfacial oxide layer was severe, the layer consisting mainly of balls of oxide up to 50 Å diameter (Fig. 5). Individual areas (F) of regrown polysilicon extended typically 300 Å along the interface and 150 Å into the polysilicon, each area often covering several oxide balls (G) and holes (H). The fraction of the length of the interface that had regrown was ~ 0.95 . The

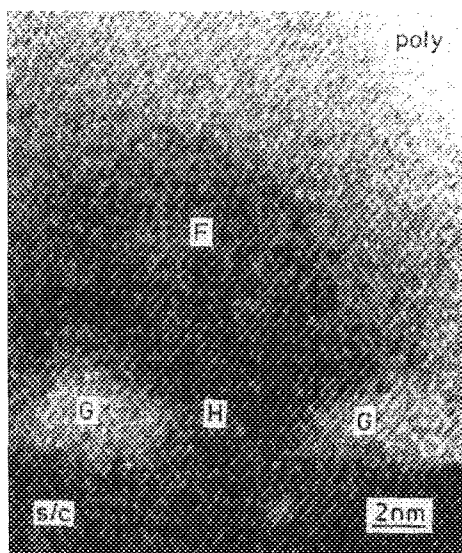


FIG. 5. HREM micrograph of a fully processed specimen given an HF treatment and a 1000 °C preanneal. Note the regrown polysilicon area F, the balled-up oxide G, and the holes in between H.

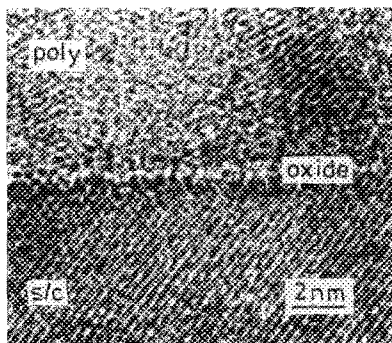


FIG. 6. HREM micrograph of a specimen given an HF treatment, but no preanneal, implant, or drive-in.

large difference between the oxide layers in the specimen given the 1000 °C preanneal, and the specimen given no preanneal, indicates that the "balling-up" of the oxide in the 1000 °C specimen mainly occurred during the preanneal.

In order to obtain further information concerning the interfacial oxide layer that was present after an HF treatment, additional specimens were examined that corresponded to an HF treatment and polysilicon deposition, but no further processing. A white band was seen at the interface (Fig. 6) but this was extremely thin, and so the oxide thickness could not be directly measured accurately. The interface was very uniform, and in a few places adjacent to the interface small areas of the polysilicon were of the same crystallographic orientation as the single-crystal silicon. These areas could have arisen by either direct epitaxial growth through holes initially present in the oxide layer or regrowth through holes created initially present in the oxide layer during the deposition of the polysilicon at 610 °C. The results indicate that an extremely thin and mainly continuous oxide layer was present immediately after the polysilicon deposition. The results also indicate that for the specimens that were given an HF treatment, no preanneal and full processing, the significant breakup of the oxide layer that was observed occurred during the 900 °C drive-in.

In our previous TEM studies¹³ of the breakup of an analogous interfacial oxide layer formed by a sulfuric acid/hydrogen peroxide surface chemical treatment, it was shown that the volume of the oxide present after complete balling-up of the layer corresponded closely to the volume of the ~ 10 -Å-thick uniform oxide layer that was present initially. This suggested that the breakup of the oxide layer occurred mainly by a local diffusion mechanism. Application of this principle to the present work gives the following results. For the specimens given an HF treatment, a 1000 °C preanneal, and full processing, the balled-up oxide corresponded to an approximately planar array of spheres of mean diameter 40 Å and mean spacing 100 Å. Calculation shows that this is equivalent to an initial uniform oxide layer of thickness ~ 4 Å, a result which is consistent with the TEM observations for the specimens given an HF treatment and polysilicon deposition, but no further processing (Fig. 6). For the specimens given an RCA treatment, an 1100 °C preanneal, and full processing, a similar calculation showed that the balled-up oxide layer is equivalent to an initial uniform oxide layer

of thickness ~ 15 Å. This result is in good agreement with the TEM value of ~ 14 Å for the specimens given an RCA treatment, preannealed at 900 °C, and fully processed (Fig. 1).

Present evidence indicates that there are genuine differences in the thickness of oxide layers formed on silicon slices by the HF treatments of different organizations. These differences may depend on the HF solution, the dip procedure, or the elapsed time prior to the subsequent deposition of the polysilicon. Our TEM examinations of silicon specimens given nominally the same HF treatment, and subsequently processed, by different organizations have shown differences in the behavior of the oxide layer which we attribute to differences in its initial thickness.¹⁹ Furthermore, measurements by different organizations of the thickness of oxide layers present on silicon slices after HF treatments have given markedly different values, e.g., 8–9 Å from ellipsometry¹⁷ and ~ 3 Å from Auger spectroscopy.¹⁸

The above TEM results show that the interfacial oxide layers break up faster when they are heated at higher temperatures, and when they are initially thinner. Thus, for the oxide layers arising from the HF treatment, which were initially ~ 4 Å thick, breakup had already occurred during a heat treatment at 900 °C (drive-in), while for oxide layers arising from the RCA treatment, which were initially ~ 14 Å thick, breakup only began to occur during a treatment at 950 °C (preanneal). These present results are consistent with our previous TEM results^{14,16} which indicated that an initially ~ 10 -Å-thick oxide layer was just beginning to break up at 900 °C. The results are also consistent with the TEM results of Schaber *et al.*²⁰ which showed that for an oxide layer ~ 30 Å thick, breakup did not occur at 950 °C. However, some caution is required when making comparisons of such results obtained by different organizations because the precise behavior depends on a number of factors, e.g., it has been shown that such oxide layers break up more rapidly when the arsenic concentration is higher.^{15,16}

Grain sizes for the polysilicon layers in fully processed specimens were determined from TEM cross-section micrographs taken at lower magnifications. For individual specimens, the grain size near the polysilicon layer surface was in general larger than in the remainder of the polysilicon layer. This was because the upper portion of the polysilicon layer had been made amorphous by the arsenic implant. Consequently, during the drive-in at 900 °C, larger grains had formed in this portion of the layer by regrowth from amorphous material than in the remainder of the layer by regrowth from fine grains. For the grains in the main portion of the layer, i.e., away from the layer surface, the results showed that the mean grain size was typically 400, 600, 1000, and 1000 Å for preanneal temperatures of 900, 950, 1000, and 1100 °C, respectively. Conversely, for the grains near the surface, the mean grain size was typically 1200 Å for all of these preanneal temperatures, except for 1100 °C when it was typically 2000 Å.

IV. ELECTRICAL RESULTS

Figures 7 and 8 show Gummel plots for the RCA- and HF-treated devices, respectively, that were given preanneals

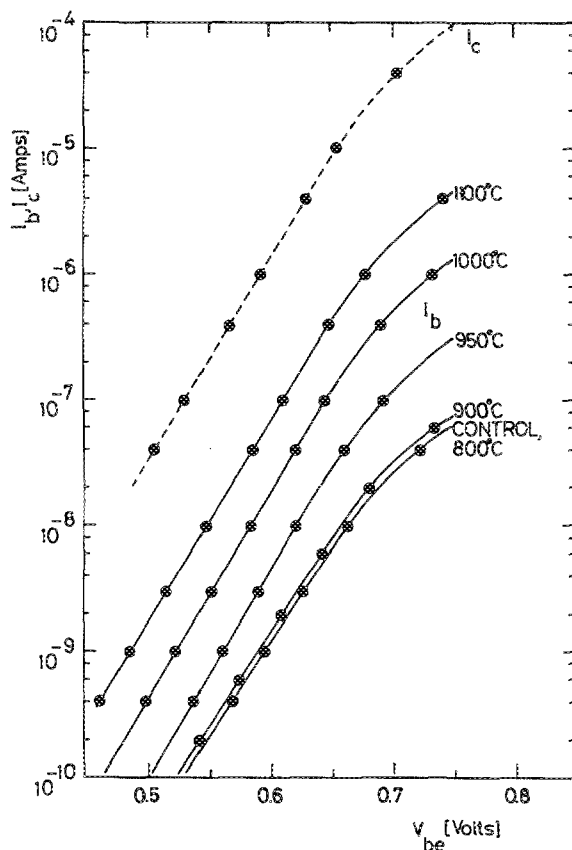


FIG. 7. Gummel plots of devices given an RCA treatment and preanneals in the range 800–1100 °C.

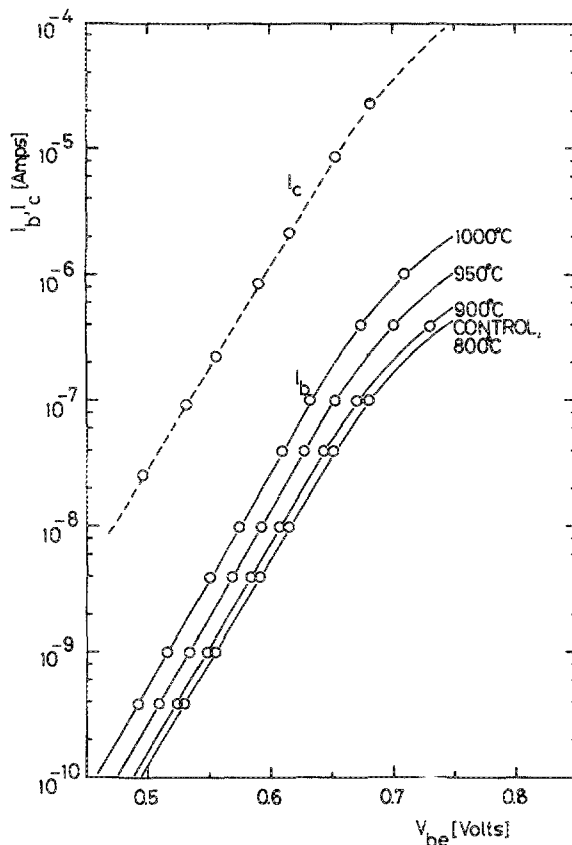


FIG. 8. Gummel plots of devices given an HF treatment and preanneals in the range 800–1000 °C.

between 800 and 1100 °C. The collector characteristics for both the HF- and RCA-treated devices are all ideal over at least three orders of collector current (60 mV/decade). Similarly the base characteristics of the HF-treated devices are also ideal, although the base characteristics of the RCA-treated devices are slightly nonideal (70 mV/decade) corresponding to an ideality parameter of $n = 1.12$. To show the effect of the preanneal on the electrical characteristics of the RCA- and HF-treated devices, I_{b0} and I_{c0} have been plotted against the preanneal temperature in Fig. 9. Because of the nonideality of the base current characteristics of the RCA-treated devices, the values of I_{b0} were calculated from the ideal collector characteristics and maximum current gain β_{max} using the relationship²¹ $I_{b0} = I_{c0}/\beta_{max}$.

For the RCA-treated devices, Figs. 7 and 9 show that the collector current is relatively unaffected by a preanneal. Conversely, the base current is strongly affected with the electrical results falling into two distinct regimes. Below ~ 900 °C, the base current is approximately constant. In this regime, the 900 °C drive-in is the dominant process as far as the interfacial oxide layer is concerned. Above ~ 900 °C, the base current increases rapidly with preanneal temperature. In this regime, the preanneal is the dominant process as far as the oxide layer is concerned. For example, the base current increases after a 950 °C preanneal by $\sim 6\times$, after a 1000 °C preanneal by $\sim 28\times$, and after a 1100 °C preanneal by $\sim 100\times$. This trend correlates well with the TEM results. Thus, after a 900 °C preanneal, the oxide layer is uniform and continuous (Fig. 1) and the gain is not significantly affected by the preanneal. After a 950 °C preanneal, the oxide layer begins to break up (Fig. 2) and a large increase in

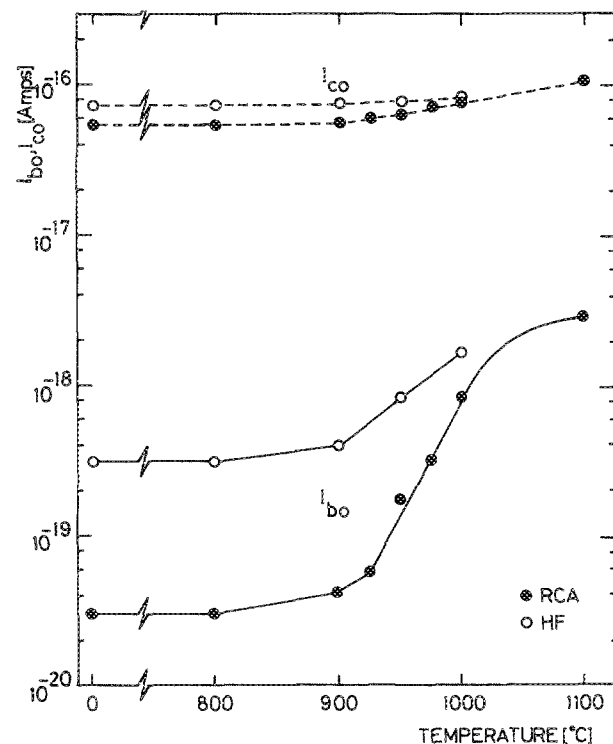


FIG. 9. I_{b0} and I_{c0} vs preanneal temperature for devices given RCA and HF treatments.

the base current occurs. As the preanneal temperature is further increased, the breaking up of the oxide layer continues (Fig. 3) and this corresponds to a continuing increase in the base current. Over the preanneal temperature range of 800–1100 °C, the transistor gain decreases from ~1800 to ~40.

For the HF-treated devices, Figs. 8 and 9 show a similar but less pronounced trend to that of the RCA-treated devices. Thus, the collector current is relatively unaffected by a preanneal. For the base current, after a preanneal below ~900 °C, no significant increase occurs. After a 950 °C preanneal it increases ~3×, and after a 1000 °C preanneal it increases ~5.5×. This increase in the base current again correlates with a progressive increase in the breaking up of the interfacial oxide layer (Figs. 4 and 5), although it should be noted that some polysilicon grain growth also occurs (Table I). Over the pre-anneal temperature range of 800–1000 °C, the transistor gain decreases from ~240 to ~50.

A comparison of the RCA- and HF-treated devices shows the following. After a preanneal below ~900 °C, the base current for the RCA-treated devices is ~10× less than for the HF-treated devices. This difference correlates with the former devices having a relatively thick, continuous oxide layer, and the latter devices having a thin broken-up oxide layer. After a preanneal at 1000 °C, the base current for the RCA-treated devices is ~2× less than for the HF-treated devices. This difference correlates with the former devices having a broken-up oxide layer, and the latter devices having a completely balled-up oxide layer.

V. INTERPRETATION OF ELECTRICAL RESULTS

The larger gain that occurs for polysilicon emitter bipolar transistors when a thin interfacial oxide layer is incorporated in the emitter can be explained qualitatively in terms of tunneling through the oxide layer as follows. For *n-p-n* transistors, the collector current I_c is determined mainly by the flow of electrons through the emitter to the base and collector. Considerable evidence has shown that the potential barrier to electrons χ_e associated with the oxide layer is small, the tunnelling probability is high, and so the electron flow is little reduced. Conversely, the base current I_b is determined mainly by the flow of holes from the base into the emitter. The potential barrier to holes χ_h associated with the oxide layer is high, the tunneling probability is low, and so the hole flow is significantly reduced. The current gain is the ratio I_c/I_b and so the gain is increased.

We shall now try to interpret our device results more quantitatively. Yu *et al.*¹¹ in their theoretical analysis of polysilicon emitter bipolar transistors which incorporated a thin uniform oxide layer within the emitter, obtained the following equation for the base current density J_b :

$$J_b = [qS_{\text{eff}} n_{ie}^2 / N_d(w)] \exp(qV_{be}/kT), \quad (1)$$

where V_{be} is the base/emitter applied voltage, $N_d(w)$ is the emitter carrier concentration at the base/emitter depletion region edge, n_{ie} is the intrinsic carrier concentration of the emitter taking into account band-gap narrowing effects, and S_{eff} is an effective recombination velocity which incorporates the various recombination processes occurring for the

holes injected from the base into the emitter. It can be seen that J_b depends directly on S_{eff} , and also on the emitter dopant profile through the parameters n_{ie} and $N_d(w)$. Earlier work²² showed that an interfacial oxide layer can retard the emitter dopant diffusion, and hence change the final dopant profile. However, for the oxide layer thicknesses considered here, this effect is very small. We shall therefore assume that n_{ie} and $N_d(w)$ are constant, and so variations in J_b can be predicted from changes in the value of S_{eff} .

A simplification of the analysis occurs if carrier recombination in the single-crystal part of the emitter located below the interfacial oxide layer is ignored. In the present work this assumption is justified, partly because the emitter/base junction is only ~100 Å below the oxide layer,¹ and partly because we shall only be considering the change in J_b , rather than its absolute value. The equation for S_{eff} then reduces to¹¹

$$S_{\text{eff}} = S_i + \{ (1/T_i) + [1/(S_i + S_p)] \}^{-1}, \quad (2)$$

where S_i is the recombination velocity for holes at the oxide layer/single-crystal silicon interface, T_i is an effective recombination velocity corresponding to the tunnelling of holes through the oxide layer, and S_p is an effective recombination velocity for holes in the polysilicon.

The parameter T_i depends on the oxide layer thickness Δ and is given by¹¹

$$T_i = (kT/2\pi m_h^*)^{1/2} (e^{-b_h}) (1 - c_h kT)^{-1}, \quad (3)$$

where

$$b_h = (4\pi\Delta/h) (2m_h^* \chi_h)^{1/2},$$

$$c_h = (2\pi\Delta/h) (2m_h^* / \chi_h)^{1/2},$$

and χ_h is the potential barrier for holes and m_h^* is the effective mass for holes.

To gain a clear insight into the relative importance of the three components of S_{eff} , curves showing the relationship between S_{eff} and Δ were calculated using Eqs. (2) and (3) (Fig. 10). A value for S_p of $1.5 \times 10^5 \text{ cm s}^{-1}$ was used, this being calculated by the method of Yu *et al.*¹¹ for a grain size of 1000 Å using the data listed in Table II. This value may be compared with the range of values of $\sim 8 \times 10^4$ to $2 \times 10^5 \text{ cm s}^{-1}$ obtained by Yu *et al.*¹¹ for similar polysilicon layers with various thicknesses and grain sizes. A value for S_i of $1.5 \times 10^3 \text{ cm s}^{-1}$ was assumed, again following Yu *et al.*¹¹ In order to calculate T_i , a value of χ_h is required. Measurements of χ_h by Ng and Card²⁷ for oxide layers in the thickness range ~20 to ~26 Å gave values of ~1.0 eV, i.e., considerably less than for thick oxide layers where $\chi_h \approx 3.0 \text{ eV}$. In the absence of any experimental values of χ_h for oxide layers of thickness < 20 Å, three values have been chosen for our calculations, namely, $\chi_h = 0.5, 1.0$, and 1.5 eV . It was also assumed that $m_h^* = m_0$, the free electron mass.

From Fig. 10 it can be seen that there are three distinct regions of device operation for a polysilicon emitter transistor. For large Δ , $S_{\text{eff}} \approx S_i$ and is determined mainly by recombination at the oxide layer/single-crystal silicon interface. Other mechanisms such as recombination in the single-crystal part of the emitter and recombination in the base may also contribute to the base current in this region of

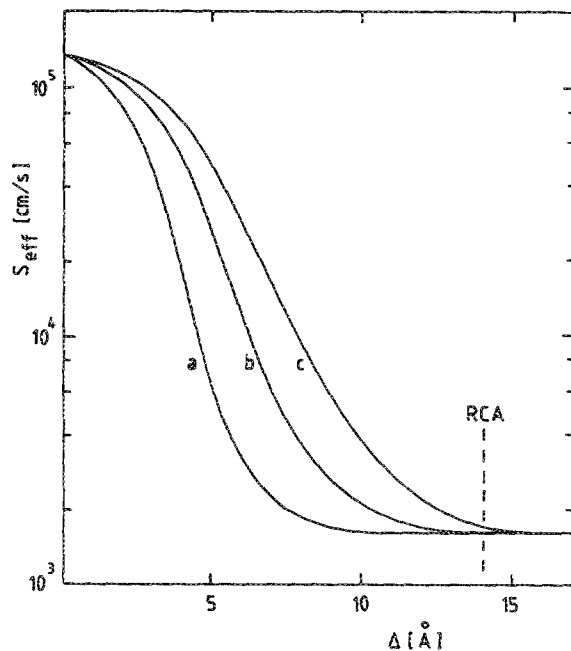


FIG. 10. Theoretical plots of effective recombination velocity (S_{eff}) vs interfacial oxide layer thickness (Δ) for hole potential barriers (χ_h) associated with the oxide of (a) 1.5, (b) 1.0, and (c) 0.5 eV.

operation.²² For small Δ , most holes tunnel through the oxide layer, $S_{\text{eff}} \approx S_p$ and is determined mainly by transport and recombination in the polysilicon. For intermediate Δ , tunneling through the oxide layer is the dominant mechanism, and S_{eff} is extremely sensitive to small changes in Δ .

Let us initially consider the effect of the interfacial oxide layer on the device operation by comparing the $\sim 10\times$ difference in base current between the RCA- and HF-treated devices given no preanneal, as shown in Fig. 9, with that predicted by Fig. 10. For the RCA-treated devices, the oxide layer is uniform and of thickness ~ 14 Å. Consequently, Fig. 10 predicts that $S_{\text{eff}} \approx S_i \approx 1.5 \times 10^3$ cm s⁻¹, and this value does not depend significantly on the precise value of χ_h . For the HF-treated devices, S_{eff} should then be $10\times$ larger, i.e., $\sim 1.5 \times 10^4$ cm s⁻¹. Figure 10 predicts that this

would correspond to a uniform oxide layer of thickness ~ 4 to ~ 8 Å, the range arising because of the uncertainty in the value of χ_h . This prediction is in reasonable agreement with the observation of a uniform oxide layer of thickness ~ 4 Å immediately after polysilicon deposition, and a broken up oxide layer of maximum thickness ~ 8 Å after no preanneal, but a 900 °C drive-in.

Let us now consider the effect of the interfacial oxide layer on the devices by comparing the $\sim 100\times$ difference in base current between the RCA-treated devices given no preanneal with those given a 1100 °C preanneal. For no preanneal, the oxide layer is continuous and uniform, and $S_{\text{eff}} \approx S_i \approx 1.5 \times 10^3$ cm s⁻¹. For a 1100 °C preanneal, the oxide layer is balled-up. If it is assumed that such a balled-up oxide layer has little effect on the flow of holes through the interface, then S_{eff} will correspond to the value for $\Delta = 0$, i.e., to $S_{\text{eff}} \approx S_p \approx 1.5 \times 10^5$ cm s⁻¹ (Fig. 10). Hence, an increase in base current of $\sim 100\times$ is predicted, in good agreement with the experimental value of $\sim 100\times$ (Fig. 9).

With regard to the effect of the interfacial oxide layer on the RCA-treated devices as the preanneal temperature is progressively increased, comparison of the device results and TEM observations suggest the following behaviors. On going from no preanneal to ~ 800 °C, I_b is constant and is determined mainly by recombination of holes at the oxide-layer/single-crystal silicon interface (mechanism A). From ~ 800 to ~ 925 °C, I_b increases slowly and is determined by mechanism A, together with tunnelling of holes through the thinner portions of the oxide layer (mechanism B). From ~ 925 to ~ 975 °C, I_b increases rapidly and is determined by mechanism B, together with an increasing contribution from the flow of holes through the penetrated regions of the oxide layer and the transport properties in the polysilicon layer (mechanism C). From ~ 975 to ~ 1100 °C, I_b continues to increase and then approaches a constant value, and is determined mainly by mechanism C, the constant value arising when the oxide layer is completely balled up.

An additional factor that could contribute to the increase in the base current as the preanneal temperature increases is the progressive coarsening of the polysilicon grains that occurs. The grain size for the part of the layer adjacent to the interfacial oxide layer increases from ~ 400 to ~ 1000 Å on going from no preanneal to both 1000 to 1100 °C preanneals (Table I). Such coarsening could change S_p , and this would change S_{eff} if Δ were small. The calculations of Yu *et al.*¹¹ indicate a maximum change in S_p due to this effect of ~ 2 or $\sim 3\times$. However, such a change in S_p would have no effect on the $\sim 100\times$ difference in I_b calculated above for the RCA-treated devices on going from no preanneal to a 1100 °C preanneal. This is because for no preanneal, the value of $S_{\text{eff}} \approx S_i$ used is appropriate for a grain size of ~ 400 Å (S_i corresponds to mechanism A and is independent of grain size), and for a 1100 °C preanneal, the value of $S_{\text{eff}} \approx S_p$ used is appropriate for a grain size of ~ 1000 Å (S_p was calculated from the data of Table II). However, the coarsening of the grains could slightly affect the shape of the curve of Fig. 9 for the RCA-treated devices on going from no preanneal to a 1100 °C preanneal because mechanisms B and C both depend on the transport properties in the polysilicon layer.

TABLE II. Summary of parameter values used to calculate S_p .

Parameter	Value	Reference
Doping concentration $N_d(w)$	5×10^{19} cm ⁻³	1
Diffusion length of holes, L_p	0.7 μm	21
Grain size	0.1 μm	
Hole mobility at grain boundary, μ_{gb}	2 cm ² V ⁻¹ s ⁻¹	23
Thickness of grain boundary, δ	10 Å	24
Grain boundary interface recombination velocity, S_{gb}	7.5×10^4 cm s ⁻¹	25,26
Length of polysilicon emitter track	Large with respect to L_p	

Let us now consider the effect of the interfacial oxide layer on the devices by comparing the $\sim 5.5\times$ difference in base current between the HF-treated devices given no preanneal with those given a 1000 °C preanneal. It is more difficult to calculate the behavior in this case because the oxide layer is already broken up for no preanneal. Comparison of the device results and TEM observations suggests that on going from no preanneal to ~ 900 °C, I_b is determined by mechanisms B and C; and on going from ~ 900 to ~ 1000 °C, I_b is determined mainly by mechanism C.

In this case the progressive coarsening of the grains could make a contribution to the increase in I_b of $\sim 5.5\times$. This is because over the whole range from no preanneal to a 1000 °C preanneal, the transport properties in the polysilicon layer play a role. The experimental results of Ning and Isaac,⁵ performed on what were in effect HF-treated devices, showed that on going from bipolar silicon transistors with polysilicon emitters to analogous devices with single-crystal emitters, the device gain decreased by $\sim 3\times$. These results suggest that in our case, i.e., for polysilicon emitter bipolar transistors given an HF treatment, some of the increase in I_b of $\sim 5.5\times$ is due to the coarsening of the grains and some to the continued breaking up of the oxide layer.

From the above results it might be expected that all devices with oxide layers thicker than ~ 10 Å would give the same best performance. However, although all such devices would possess the same lowest value of S_{eff} , and as a result J_b , the oxide layers introduce a series emitter resistance which increases rapidly with increasing oxide thickness.^{11,28} This is detrimental to device and circuit performance, and so in practice a compromise between increased gain and increased emitter resistance needs to be made.

As far as the breakup and eventual balling-up of the thin interfacial oxide layer is concerned, the main driving force is considered to be a significant reduction in the total amount of energy associated with the oxide layer/silicon interface^{13,15} (analogous to the well-known Oswald ripening effect that occurs in metallurgical systems). Thus, on going from a continuous uniform oxide layer to a balled-up oxide layer, the interfacial area decreases by typically ~ 5 to $\sim 10\times$ (deduced from TEM examinations). However, the presence of the As dopant can also have an effect. For example, in our work^{15,16} on similar specimens post-annealed at 900 °C, the breakup of the oxide layer was found to proceed more rapidly when the As⁺ implantation dose was increased from 5×10^{15} to 2×10^{16} cm⁻². This result suggests¹⁵ that the As dopant can either enhance the local oxide diffusion rate or change the oxide/silicon interfacial energy.

VI. CONCLUSIONS

A detailed comparison of the electrical and TEM results has revealed that there is a strong correlation between the high gain of polysilicon emitter bipolar transistors and the existence of a continuous, thin, interfacial oxide layer between the single-crystal silicon and the polysilicon. For RCA-treated devices, an initial high gain of ~ 1400 occurs due to the presence of an ~ 14 -Å-thick oxide layer. On annealing at temperatures up to 1100 °C, the gain progressively decreased to ~ 40 due mainly to the breaking up of the oxide

layer. For HF-treated devices, an initial gain of ~ 240 occurs due to the presence of a thinner and already partly broken up oxide layer. On annealing at temperatures up to 1000 °C, the gain decreases to ~ 50 due to further breaking up of the oxide layer together with a coarsening of the polysilicon grains. The decrease in gain observed with increasing anneal temperature is explained using a theoretical model in which tunneling through the interfacial oxide is an important mechanism. As demonstrated by other authors,^{11,28} if the oxide layer is too thick, it contributes a significant series resistance to the emitter structure. Therefore, in order to obtain the optimum device, it is necessary to produce an extremely thin continuous oxide layer, and to prevent it from breaking up during the device fabrication. The thinner the oxide layer, the more readily it breaks up, and the more critical the device processing procedures become.

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