

Highly Reliable High-Voltage Transistors by Use of the SIPOS Process

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Abstract—The n-p-n and p-n-p high-voltage transistors showing high reliabilities have been developed by using semi-insulating polycrystalline-silicon (SIPOS) films for the surface passivation. SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms. The films employed for the surface passivation of high-voltage transistors are composed of triple layers, which are oxygen-doped SIPOS films of 0.5- μm thickness to stabilize the silicon interface, nitrogen-doped SIPOS films of 0.15- μm thickness to prevent water or sodium ions from reaching the silicon surface, and silicon dioxide films to prevent dielectric breakdown of the SIPOS films under very high-voltage operation.

The n-p-n and p-n-p SIPOS transistors rated at 800 and 2500 V have been produced in planar-like structures with field-limiting rings. These transistors showed highly reliable characteristics, because the passivating SIPOS layer provides a good protection against ionic contamination and externally applied electric fields. Furthermore, 10-kV n-p-n SIPOS transistors with multiple rings have been fabricated and found that operation is stable.

I. INTRODUCTION

THE PLANAR technology minimizes and stabilizes various surface effects since planar junctions are covered by a thermally grown silicon dioxide layer, and therefore results in better control of device characteristics [1]. Instability due to the drift of sodium ions in silicon dioxide film can be suppressed by forming a phospho-silicate glass [2] or silicon nitride film over the silicon dioxide film [3]. However, there are still some problems in the planar process. The first problem of the planar technology is that a fixed positive charge appears in the silicon dioxide layer near its interface with the underlying silicon substrate. This positive charge tends to cause accumulation of electrons in n-type silicon and an inversion layer in p-type silicon, respectively, which makes it difficult to produce high-voltage planar transistors of IC's [1].

The second problem is that planar devices, passivated with an insulating layer like silicon dioxide film, may not be protected from accumulated electronic charges or ionic contamination on the passivating layer. The electric charges induce charges of opposite polarity near the surface region of a silicon substrate and modulate its conductivity.

The third problem is that degradation of characteristics of planar devices occurs by avalanching p-n junctions. Degradation of low current h_{FE} due to avalanche breakdown of the emitter-base junction of a silicon planar

transistor is caused by an increase in surface recombination velocity within the vicinity of the emitter-base metallurgical junction [4]. Walk-out phenomena of breakdown voltages in p-n junctions under a reverse bias are due to the memory effects of hot carriers which are injected into insulating films like silicon dioxide and may stay long inside the films and modulate the conductivity of the surface region of devices [5].

The oxygen-doped polycrystalline-silicon film applied to the surface passivation of silicon devices has solved these problems, because the film is semi-insulating and almost electrically neutral [6]–[8]. The polycrystalline-silicon layer doped with oxygen is employed as a replacement for the silicon dioxide layer of planar devices. An oxygen-doped polycrystalline-silicon film can be used for the surface passivation of p-type silicon substrates as well as n-type silicon, since it is electrically neutral [8]. When the surface of silicon devices is directly passivated with a semi-insulating layer like oxygen-doped polycrystalline-silicon films, charges of opposite polarity induced near the silicon surface by contaminating ions on top of the passivating layer drift into the passivating layer. Then, the induced charges either neutralize the charges on the outer surface or otherwise form a space-charge region within the passivating layer, which electrostatically shields the surface region of a silicon substrate from the outer charges. On the other hand, there is no memory effects due to hot carriers injected into the passivating layer by avalanche breakdown of a p-n junction, because hot carriers may not stay long within the semi-insulating layer.

Furthermore, a nitrogen-doped polycrystalline-silicon film known as silicon-rich nitride and a silicon dioxide film have been introduced on the oxygen-doped polycrystalline-silicon layer. The former acts to prevent water or sodium ions from reaching the silicon surface and the latter to prevent dielectric breakdown of the nitrogen-doped polycrystalline-silicon film in the region of very high-voltage operation, since the silicon-rich nitride has lower resistivities than stoichiometric silicon nitride (Si_3N_4).

Thus a device passivated by a triple layer system composed of an oxygen-doped polycrystalline-silicon film, a nitrogen-doped polycrystalline-silicon film and a silicon dioxide film can be operated stably, even if it is exposed to ionic contamination, dipolarly polarized resin, or externally applied electric fields.

The employment of a triple layer system for the surface passivation of silicon devices has brought about a fundamental solution to the weakness of the planar method and

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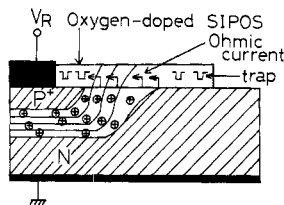


Fig. 1. Potential distribution in the depletion region of p^+-n diode passivated with an oxygen-doped SIPOS film.

results in devices with high performance and high reliability. Since the technology is based on the semi-insulating polycrystalline-silicon layer, it is named the "SIPOS" process.

II. PASSIVATING PROPERTIES OF SIPOS FILMS

The passivating properties of oxygen-doped SIPOS films, deposited directly on the surface of a silicon device by a chemical vapor deposition technique, were examined for various oxygen concentrations and compared with a silicon dioxide passivating layer used in the planar technology. We first look into the passivating effects of oxygen-doped SIPOS films in the vicinity of reversely biased p^+-n junction.

SIPOS films are semi-insulating and contain deep-lying centers in themselves as described elsewhere [6]–[8]. The voltage–current characteristics of SIPOS films obey Ohm's law in the low-voltage region in resistivity measurements. When a p^+-n junction diode passivated with a SIPOS film is reversely biased, the bias voltage is also applied to the SIPOS film and an ohmic current flows through the SIPOS film, as shown in Fig. 1, although the magnitude of the current is less than the surface generation current in p^+-n junction. The negative potential of p^+ -type region is transmitted to the surface region of the n -type substrate through the SIPOS film. Therefore, electrons near the surface of the n -type substrate can be depleted as shown in Fig. 1, and the surface electric field of the n -type substrate is modulated and relaxed. Thus the breakdown voltages of the devices will increase, if they are limited by the surface breakdown. However, the field relaxation effect is lessened, as the resistivities of the SIPOS film increase and become as high as that of a silicon dioxide. That is, the potential drop within the SIPOS film near p^+-n metallurgical junction will increase due to currents from the n -type substrate and increasing resistance of the SIPOS film, which reduces the transmitting distance of the negative potential of the p^+ -type region to the n -type substrate.

Fig. 2 shows the junction breakdown voltages of p^+-n diodes having cylindrical junction passivated with a SIPOS film of $0.5\text{-}\mu\text{m}$ thickness or a thermal oxide of $1\text{-}\mu\text{m}$ film, where the resistivity of n -type substrate is $50\text{ }\Omega\text{-cm}$ and the diffusion depth of p^+ -type region is $25\text{ }\mu\text{m}$. The reverse voltage–current characteristics of p^+-n diodes showed hard-breakdown characteristics. The junction breakdown voltages decrease with increasing oxygen concentration in SIPOS films up to 8 at. percent, but tend to approach a certain value with increasing oxygen concentration as

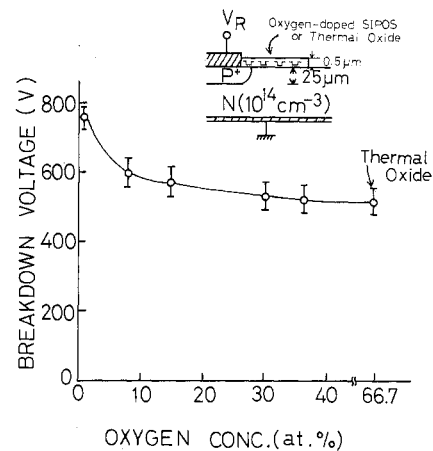


Fig. 2. Junction breakdown voltages of p^+-n diodes as a function of oxygen concentration in SIPOS films and a diode passivated with a thermally grown oxide film.

shown in Fig. 2. Since the theoretical breakdown voltage is about 550 V in the case of planar junctions with diffusion depth of $25\text{ }\mu\text{m}$, SIPOS passivated junctions seem to show a higher breakdown voltage than the theoretical one. This is due to the relaxation effect of the surface electric field by the SIPOS passivation. When oxygen concentration of SIPOS films increases, however, the relaxation effect is lessened by increase of the resistivities of SIPOS films and the breakdown voltages decrease.

The reverse leakage current I_R of SIPOS passivated junctions is given by

$$I_R = I_{\text{gen},s} + I_{\text{gen},b} + I_{\text{diff}} + I_{\text{ohmic}}$$

where $I_{\text{gen},s}$, $I_{\text{gen},b}$, I_{diff} , and I_{ohmic} are the surface generation current, the generation current within the space-charge region, the diffusion current outside the space-charge region and the ohmic current flowing through SIPOS films, respectively. If the resistance of a SIPOS layer is not large enough, I_{ohmic} becomes dominant. Furthermore, $I_{\text{gen},s}$ may become large, if the density of the surface generation centers near the surface of a silicon substrate is high. Fig. 3 shows both the reverse current I_R of p^+-n diodes, of which peripheral junction length is 0.12 cm , passivated with a SIPOS film of $0.5\text{-}\mu\text{m}$ thickness and a thermal oxide film of $1\text{ }\mu\text{m}$ and the resistivities of SIPOS films as a function of oxygen concentration. When only 8 at. percent oxygen is doped, I_R drastically decreases as compared with I_R of a p^+-n diode passivated by a film not containing oxygen atoms, namely undoped polycrystalline-silicon film. However, I_R tends to be settled at a certain value less than 10^{-9} A , although the resistivities of the films become higher when the films contain more than 15 at. percent oxygen. It indicates that oxygen atoms doped into polycrystalline-silicon films lessen the ohmic current and the surface generation current in the reverse current of p^+-n diode, but oxygen atoms more than 15 at. percent in SIPOS films do not contribute to reduce the density of the surface generation centers any more. The surface recombination velocity of a diode passivated with SIPOS films with more than 15 at. percent oxygen is about 200 cm/s , which is calculated by the assumption that the

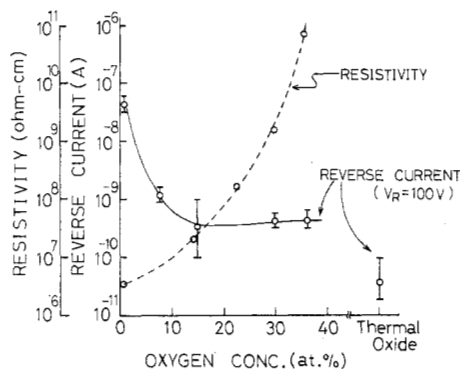


Fig. 3. Reverse leakage currents of p^+-n diodes passivated with SIPOS films as a function of oxygen concentration in SIPOS films as compared with that of p^+-n planar diode, and resistivities of SIPOS films as a function of oxygen concentration.

measured value of I_R is equal to the surface generation current $I_{gen,s}$. The leakage current of SIPOS passivated diodes is one order of magnitude larger than that of good planar diodes but is not harmful for most of the devices in practical use.

Fig. 4 shows the common-emitter current gain h_{FE} as a function of collector current. h_{FE} increases with increasing oxygen concentration. It is concluded that SIPOS films with 15 to 35 at. percent oxygen have the optimum passivating properties for silicon devices, because a SIPOS film with less than 15 at. percent oxygen shows a lower h_{FE} and a larger reverse current, and a SIPOS film with more than 35 at. percent oxygen becomes a good insulator, like a silicon dioxide film, and tends to exhibit some problems as described previously.

We shall next consider the passivating properties of a triple layer system composed of an oxygen-doped SIPOS film, a nitrogen-doped SIPOS film, and a silicon dioxide film. This system can be used for the surface passivation of p-type silicon substrates as well as n-type silicon, since an oxygen-doped SIPOS film, in which ionic charges do not exist is directly deposited on the silicon substrate. Furthermore, it can be protected from penetration of water or sodium ions, because there is a nitrogen-doped SIPOS film. It can be applied to the surface passivation of very high-voltage devices, because silicon dioxide as the top layer of the system prevents dielectric breakdown of the SIPOS films in the region of very high-voltage operation.

III. HIGH-VOLTAGE TRANSISTORS

The SIPOS passivation process has been applied to high-voltage n-p-n and p-n-p transistors. These transistors have planar-like structures with field-limiting rings on silicon substrates, as shown in Fig. 5 [9]. Fig. 5(a) shows a p-n-p transistor passivated by a triple layer system. If the planar method is employed, thermally grown silicon dioxide induces an inversion layer in lightly doped p-type substrates and bridges the base region and the field-limiting ring as shown in Fig. 5(b), which makes the field-limiting ring ineffective. Moreover, these structures are generally sensitive to electronic or ionic charges on the passivating layers, because positive charges on the layer, for example, induce negative mobile charges near the sil-

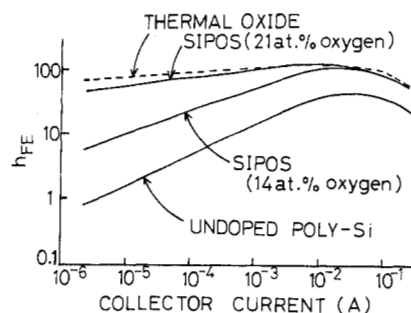


Fig. 4. Common-emitter current gains of n-p-n transistors as a function of collector current.

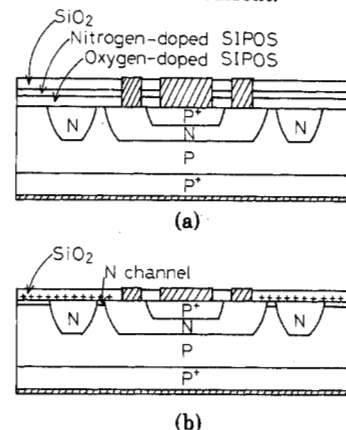


Fig. 5. (a) Cross-sectional view of a p-n-p high-voltage transistor passivated with triple layers composed of an oxygen-doped SIPOS film, a nitrogen-doped SIPOS film and a silicon dioxide film. (b) Cross-sectional view of a p-n-p transistor passivated with a thermally grown oxide film.

icon surface, which cause the potential change of the field-limiting rings and results in degradation of device characteristics. By employing the SIPOS process, however, these structures become insensitive to an externally applied field, which leads to highly reliable devices.

A SIPOS bipolar transistor is fabricated by standard planar processes until emitter regions are diffused as shown in Fig. 6. Instead of opening windows for the ohmic-contact metallization, the entire silicon dioxide layer on the surface of the device is etched away. Then, a triple layer system, which consists of an oxygen-doped SIPOS film of $0.5\text{-}\mu\text{m}$ thickness containing 20 at. percent oxygen, a nitrogen-doped SIPOS film of $0.15\text{ }\mu\text{m}$ with 52 at. percent nitrogen and a silicon dioxide film of $1\text{ }\mu\text{m}$, is successively deposited onto devices at 650°C by chemical-vapor deposition. Prior to the deposition, a natural oxide layer must be etched away, because the memory effect takes place when a rather thick natural oxide layer exists. An oxygen-doped SIPOS film is deposited from the $SiH_4\text{-}N_2O\text{-}N_2$ system and a nitrogen-doped SIPOS film is deposited from the $SiH_4\text{-}NH_3\text{-}N_2$ system at the same temperature [6]. A new etchant which is a mixture of H_2O_2 , HF, and NH_4F has been developed for etching SIPOS films. The etching rate is about $2000\text{ }\text{\AA}/\text{min}$ for oxygen-doped SIPOS films of 20 at. percent oxygen, $100\text{ }\text{\AA}/\text{min}$ for nitrogen-doped SIPOS films of 52 at. percent nitrogen at 25°C and infinitesimal for silicon substrate, when an etchant consists of $6H_2O_2$, HF, and $10\text{ }NH_4F$ in volume ra-

FABRICATION OF SIPOS TRANSISTOR

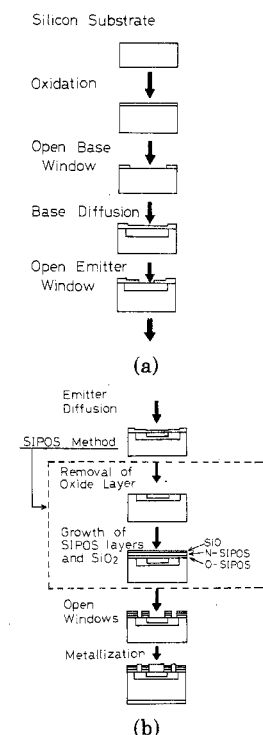


Fig. 6. Fabrication process of a SIPOS transistor.

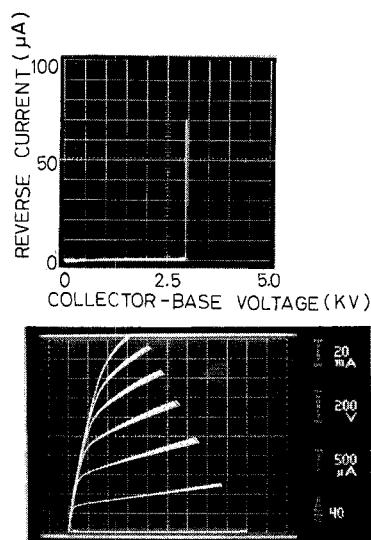


Fig. 7. Typical characteristics of a 2500-V p-n-p SIPOS transistor.

tios. Accordingly, windows for the ohmic contact of devices passivated with SIPOS films can be opened by using conventional photoresist and this etchant. After etching, metal electrodes are formed onto the devices.

The n-p-n and p-n-p transistors rated at 800 and 2500 V have been produced by using the triple layers. The resistivities of the substrates for each high-voltage transistor are 50 Ω·cm for 800-V n-p-n, 150 Ω·cm for 800-V p-n-p, 250 Ω·cm for 2500-V n-p-n, and 750 Ω·cm for 2500-V p-n-p. Typical characteristics of a 2500-V p-n-p transistor are shown in Fig. 7. These transistors show highly reliable characteristics. For example, characteristics of 800-V n-p-n and p-n-p SIPOS transistors did not show any degradation

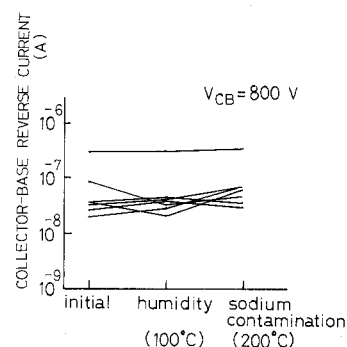


Fig. 8. Changes of collector-base reverse currents of p-n-p SIPOS transistors when they are exposed to water vapor and sodium contamination.

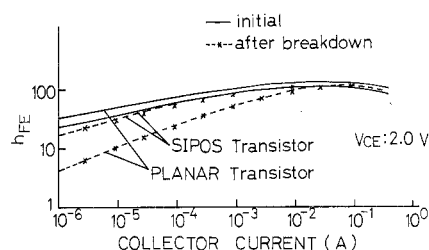


Fig. 9. Changes of current gains due to the avalanche breakdown of emitter-base junctions.

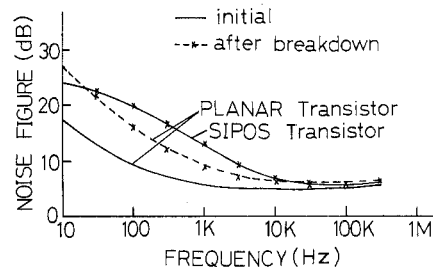


Fig. 10. Changes of noise characteristics due to the avalanche breakdown of emitter-base junctions.

under a bias-temperature stress test (dc 800 V and 120°C) for 1008 h. On the other hand, 800-V n-p-n planar transistors did not operate stably under the reliability tests of the same conditions for only 24 h and p-n-p planar transistors rated at more than 500 V have not been fabricated anywhere yet. Furthermore, the collector-base reverse currents of 800-V p-n-p transistors with the emitter open at 800 V did not increase even after the chips were exposed to water vapor at 100°C for 1 h and sodium contamination at 200°C for 2 h, as shown in Fig. 8. Because of the good protection afforded by SIPOS films, SIPOS devices can be packaged in inexpensive molded resin rather than costly metal cans. When high-voltage rating but not high dissipating rating is required, dip coating which is usually used for capacitors can be used, which eliminates expensive packaging and reduces the final size of the unit.

SIPOS transistors showed little degradation of h_{FE} and noise figure after avalanche breakdown of the emitter-base junctions, but the planar transistors exhibited much decrease of h_{FE} and much increase of noise figure, as shown in Figs. 9 and 10. Furthermore, breakdown voltages of SIPOS transistors did not show walk-out phenomena due

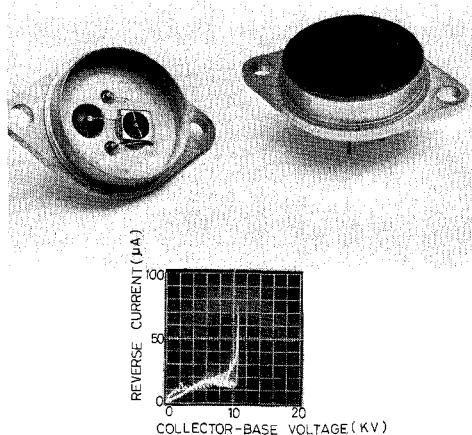


Fig. 11. The top view and collector-base reverse current of a SIPOS transistor withstanding 10 kV.

TABLE I
Characteristics of High-Voltage SIPOS Transistors

	800 V _{nnp}	800 V _{ppp}	2500 V _{nnp}	2500 V _{ppp}	10 kV _{nnp}
BV _{CBO}	800 V	800 V	2500 V	2500 V	10 kV
BV _{CEO}	500 V	500 V	1500 V	1500 V	9 kV
I _{CBO}	0.03 μA	0.4 μA	0.3 μA	10 μA	10 μA
I _{CEO}	0.2 μA	0.4 μA	0.8 μA	70 μA	50 μA
V _{CE(sat)}	5 V	10 V	15 V	35 V	15 V
I _{C max}	150 mA	50 mA	150 mA	50 mA	10 mA
h _{FE}	60	50	40	40	10 ~ 50
f _T	8 MHz	8 MHz	9 MHz	5 MHz	10 MHz
C _{cbp}	10 pF	10 pF	14 pF	14 pF	8 pF

to avalanche breakdown of junctions. Thus SIPOS transistors are protected against the stress within the devices such as avalanche breakdown.

10-kV n-p-n SIPOS transistors with multiple rings on both the surfaces of silicon substrates have also been fabricated [10], [11] and operation of the transistors was found to be stable. The top view and the collector-base leakage current of a 10-kV transistor are shown in Fig. 11. The characteristics of the high-voltage SIPOS transistors are shown in Table I.

IV. CONCLUSION

The n-p-n and p-n-p high-voltage transistors rated at 800 and 2500 V have been produced in planar-like structures with field-limiting rings by using the SIPOS films for

the surface passivation. These transistors showed highly reliable characteristics, because the passivating SIPOS layer provided a good protection against ionic contamination and externally applied electric fields, which makes it possible to use low-cost molded resin and then to miniaturize package. Furthermore, 10-kV n-p-n SIPOS transistors with multiple rings have been fabricated and it has been found that operation is stable.

SIPOS transistors did not show walk-out phenomena of I - V characteristics of p-n junctions, degradation of h_{FE} , and increase of noise figure by the avalanche breakdown of p-n junctions, which allows the maximum ratings of devices to increase.

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