

BORON AND PHOSPHORUS DIFFUSION THROUGH AN SiO_2 LAYER FROM A DOPED POLYCRYSTALLINE Si SOURCE UNDER VARIOUS DRIVE-IN AMBIENTS†

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Abstract—The diffusion of boron and phosphorus into thermally grown SiO_2 from a doped polycrystalline Si source has been found to be dependent on drive-in ambients and to be especially fast in an H_2 ambient. Diffusion coefficients have been calculated by the two boundary diffusion model. It was found that the diffusion coefficient of boron in SiO_2 is about two orders of magnitude larger than that of phosphorus. This fact is very important for Si gate processes. For P -channel Si gate transistors, boron diffused in the gate SiO_2 film from the doped polycrystalline Si gate electrode causes new types of instabilities in transistor characteristics.

1. INTRODUCTION

One of the most serious problems in Si gate processes [1] is the impurity penetration into a gate SiO_2 film from a doped polycrystalline Si gate electrode. With a P -channel Si gate transistor, in particular, it gives rise to new types of instabilities in transistor characteristics. Faggin, Forsythe and Klein [2] have reported that P -channel Si gate transistors exhibit rapid and substantial threshold shift and breakdown voltage degradation when stressed at room temperature with a positive gate bias and that these shifts are consistent with H^+ ion movement through the gate insulator film. In order to examine the causes behind these phenomena, the dependence of instabilities on boron drive-in ambients has been studied. In consequence, the magnitude of instabilities such as threshold voltage shift by a positive gate bias at room temperature and the increase of drain leakage current and surface state density, were found to be strongly dependent on the boron drive-in ambients. An H_2 ambient, especially, has brought out the largest instabilities. As the instabilities were considered to be related to the boron penetration depths in the gate insulator films, experiments have been conducted to study the diffusion of boron in polycrystalline Si and in SiO_2 under various drive-in ambients. In polycrystalline Si, no difference in diffusion depths was found among samples treated in various drive-in ambients. However, the diffusion coefficient of boron in SiO_2 was found to be dependent on the drive-in ambients corresponding to the instabilities in transistor characteristics and was calculated to be 10^{-16} – 10^{-15} cm^2/sec at 1100°C by the two boundary [3] diffusion model. Similarly, the diffusion of phosphorus in SiO_2 , which is closely related to an N -channel Si gate process, has been studied. It was found that the diffusion coefficient of phosphorus in SiO_2 also depends on the drive-in ambients. The diffusion coefficient of phosphorus in SiO_2 , however, is about two orders of magnitude smaller than that of boron.

First, this paper describes the instabilities of P -channel

Si gate transistors caused by boron penetration in the gate SiO_2 films. Then, the diffusion of boron in polycrystalline Si and the diffusion of boron and phosphorus in thermally grown SiO_2 in various drive-in ambients are described. Finally, the diffusion coefficients of boron and phosphorus in SiO_2 , calculated by the two boundary diffusion model [3], are shown.

2. EXPERIMENTAL PROCEDURE

The substrates used for P -channel Si gate transistors were N -type Si wafers of $4\sim6\ \Omega\text{ cm}$ resistivity. For a gate electrode, $5000\ \text{\AA}$ polycrystalline Si was deposited from $\text{SiH}_4\text{--N}_2$ mixture at 650°C on a $1000\ \text{\AA}$ steam oxidized gate film. As a result of the boron predeposition process, using a BCl_3 source at 1000°C for 20 minutes, drain and source junctions were formed and the Si gate electrode was heavily doped with boron. Then, the subsequent drive-in stage was carried out in an N_2 or O_2 ambient for 1 hr at 1050°C , in a steam ambient for 10 min at 1000°C , or in an H_2 ambient at 850°C . In the next step, $5000\ \text{\AA}$ SiO_2 layer was deposited onto the entire surface by low temperature ($\sim 400^\circ\text{C}$) oxidation of SiH_4 . After opening windows for the contact areas, aluminum was evaporated by electron-beam method and was defined by the conventional photo-resist process. Finally, the wafers were alloyed in an N_2 ambient at 450°C . Most of the experimental transistors were of a stripe type with a channel length of $10\ \mu$, channel width of $3000\ \mu$ and drain area of $5.65 \times 10^4\ \mu^2$. The substrates used for the study of boron diffusion into thermally grown SiO_2 were N -type Si wafers which were oxidized in a steam ambient at 950°C . The thicknesses of oxide films were measured by an ellipsometer. Then the $5000\ \text{\AA}$ polycrystalline Si film was deposited on the wafer, which was subjected to boron deposition for 10 min at 1080°C by a BCl_3 source. Immediately after the boron deposition process, a CVD SiO_2 film $5000\ \text{\AA}$ thick was deposited on the wafer to prevent the out-diffusion of boron from the polycrystalline Si surface.

The drive-in stage was carried out at 1100°C in an N_2 , O_2 , steam or H_2 ambient. After the drive-in operation, all

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the layers on the single crystalline Si were removed. The $P-N$ junction depth in the single crystalline Si was measured by the spherical grooving method and the sheet resistivity was measured by the standard 4-point probe method. Similarly, the diffusion of phosphorus in thermally grown SiO_2 was studied in N_2 and H_2 ambients at 1150°C and 1200°C . The diffusion was carried out into single crystalline Si through a thermally grown SiO_2 film from phosphorus doped polycrystalline silicon layers of two different concentration levels. The impurity concentration in the polycrystalline Si can be estimated by a direct diffusion of the impurity into single crystalline Si from the doped polycrystalline Si. In this case, the impurity concentration in the polycrystalline Si is assumed to be homogeneously equal to the measured concentration at the single crystalline Si surface. After the diffusion process, the polycrystalline Si layer was etched away by an $\text{HF-HNO}_3\text{-CH}_3\text{COOH}$ mixture and the surface concentration was calculated from the measured sheet resistivity and junction depth of the impurity in the single crystalline Si. In this procedure, the end point of etching time for the polycrystalline Si was judged from the etch-off time for the polycrystalline Si deposited on an SiO_2 layer.

3. EXPERIMENTAL RESULTS

3.1. New types of P-channel Si gate transistor instabilities

By a positive gate bias at room temperature, the threshold voltage shifts to a larger value and reaches the saturation state in about 1 min of biasing. This shift recovers almost to the initial value by the subsequent application of a negative gate bias. However, this type of shift doesn't appear in case of negative gate biasing. Figure 1 shows the threshold voltage shift after 1 min of a positive gate bias at room temperature. From this figure, it can be understood that the shift depends on the drive-in ambients. A larger shift appears with the sample treated in the steam ambient, even though the drive-in temperature is lower and the drive-in time is shorter. There is a small shift with the O_2 -treated sample and there is no shift with the N_2 -treated and no-drive-in samples. Figure 2 also shows the threshold voltage shift of samples which were subjected to the drive-in operation for 5 min and 30 min in an H_2 ambient at 850°C . In case of an H_2 ambient, the shift appears even at relatively lower temperatures and the

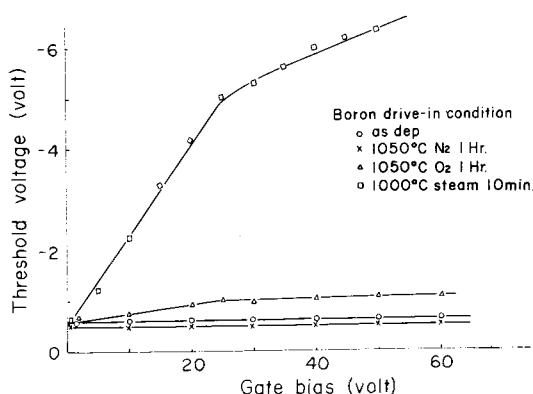


Fig. 1. Threshold voltage shift with a positive gate bias at room temperature.

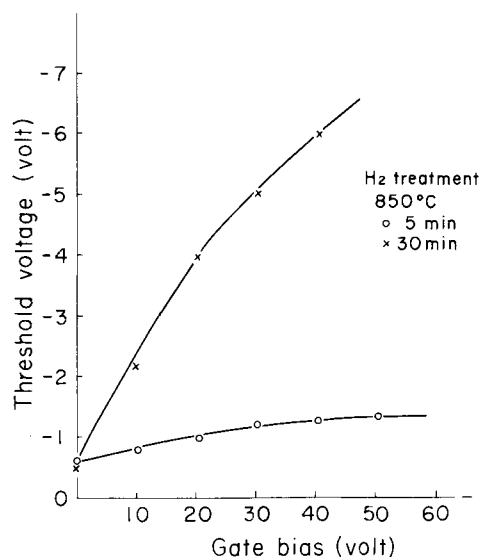


Fig. 2. Threshold voltage shift with a positive gate bias at room temperature.

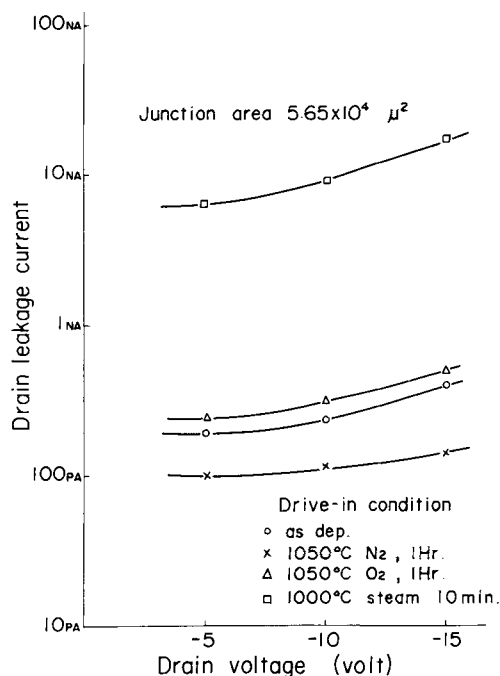


Fig. 3. Drain junction leakage current as a function of drain voltage.

shift increases with the treatment period. Figure 3 shows the drain leakage current of the transistors. The drain leakage current was measured as a function of drain voltage with the gate, the source and the substrate electrode grounded. The drain leakage current also depends on the drive-in ambients, as much as the threshold voltage shift does. This figure shows that the no-drive-in sample has a larger leakage current than the N_2 treated sample. However, the no-drive-in sample has a shallow junction depth, which might presumably account for this result. Table 1 shows the threshold voltage and the

Table 1. Threshold voltage and surface mobility under various drive-in ambients

drive ambient	050°C N ₂ 60 min	050°C CO ₂ 60 min	000°C steam 10 min
V _T (R·temp)	0.6 V	0.6 V	0.4 V
V _T (77°K)	1.1 V	1.1 V	1.4 V
ΔV _T (77°K-Rt)	0.5 V	0.5 V	1.0 V
μ _{MAX} (R·temp)	260 cm ² /v sec	265 cm ² /v sec	125 cm ² /v sec
μ _{MAX} (77°K)	1270 cm ² /v sec	1340 cm ² /v sec	300 cm ² /v sec
μ _{MAX} 77°K / μ _{MAX} Rt	4.88	5.05	2.4

maximum value of the surface mobility, which was measured as a function of gate voltage under small drain voltage ($V_D = 0.01$ volt) at room temperature and at 77°K. Generally speaking, the change of threshold voltage by variation of temperature and the maximum value of surface mobility depend on the surface states. According to this table, the steam treated sample shows a larger variation of the threshold voltage and a smaller surface mobility, especially at 77°K. Therefore, it can be concluded that this sample has a larger surface state density.

In an attempt to explain why the new types of instabilities, such as the threshold voltage shift by a positive gate bias at room temperature and the increase of drain leakage current, occur in a *P*-channel Si gate transistor, the following model was proposed. At first it was considered that these instabilities are caused by the motion of positive ions in the gate insulator. Hofstein[4] has found similar instabilities in metal gate MOS devices and reported that the instabilities correspond to the motion of H⁺ ions in a thermally grown, undoped SiO₂ layer. However, in his report, no measurable shifts were observed at room temperature. In the present work, instabilities occur even at below room temperature. As an explanation of this point, the model was proposed as shown in Fig. 4. By the boron diffusion into the gate SiO₂ film during the boron drive-in process, the boron doped SiO₂ layer is formed on the pure SiO₂ layer. The depth of the boron doped SiO₂ layer depends on the drive-in ambients. In the boron doped SiO₂ layer, if H⁺ ions can move easily at room temperature, H⁺ ions, initially located near the gate electrode, move into the boron doped SiO₂ layer due to a positive gate bias at that

temperature and are stored at the boundary of the boron doped SiO₂ layer and the pure SiO₂ layer. If one now considers the possibility of a volume charge distribution $P(x)$ within the boron doped SiO₂ layer, the effective threshold voltage shift becomes [5]

$$\frac{1}{X_0 C_0} \int_0^{X_0} X P(x) dx \quad (1)$$

where X_0 is the thickness of the gate insulator. C_0 is the capacitance per unit area of the insulating layer. X_D is the thickness of the boron doped SiO₂. Accordingly, changes in the positive charge distribution within the boron doped SiO₂ can be observed from the threshold voltage shift. By applying a gate bias for various lengths of time at various temperatures, one can study the kinetics of the positive charge ion migration process. In the case of Na⁺ and Li⁺, the activation energy of the diffusion coefficients in SiO₂ is obtained from this method [5]. In consequence therefore, the activation energy of the positive charge can be estimated in the typical sample. The dependence of the threshold voltage shift on biasing time and temperature is shown in Fig. 5 for an applied gate bias of +20 volts. In this figure, the shift is plotted against the square root of biasing time with temperature as a parameter. The

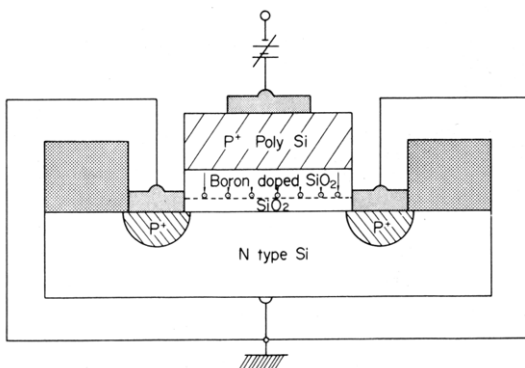


Fig. 4. Proposed threshold voltage shift model using stored positive charges.

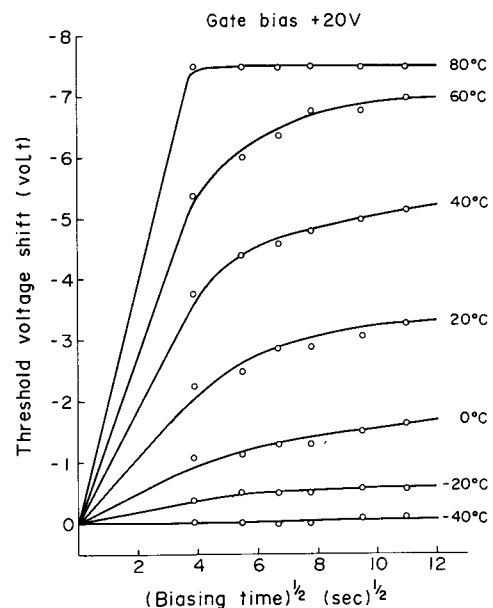


Fig. 5. Threshold voltage shift dependence on biasing time and temperature for +20 volt applied gate bias.

temperature dependence of the threshold voltage shift is analyzed by plotting the logarithm of the gradient of the straight line portion in Fig. 5 versus $1/T$. The plot is shown in Fig. 6, where a straight line corresponding to an activation energy of 0.26 eV is obtained. The proposed model by Snow *et al.* [5], shows that the activation energy for the diffusion coefficient of the positive charge is twice this value, viz. 0.52 eV. As described in the proposed model, it seems that the obtained value is the activation energy of the diffusion coefficient of H^+ ions in the boron doped SiO_2 , which is considered to be introduced during the heat treatment at 450°C [2,6] by the chemical reaction of aluminum with minute amount of water on the outer surface. However, no definite relation is found between the results of H^+ ion induced instabilities and those of H^+ ions induced reduction of fast surface state densities [6]. Comparing the activation energy of 1.35~1.40 eV for Na^+ ions in SiO_2 [5], that of H^+ ions in the boron doped SiO_2 is much smaller. Drain leakage current also increases due to the positive charges stored on the P^+N drain junction edge by the electric field between the drain and gate electrode. Though the detailed mechanism about the drain leakage current is not clear from these experiments, it seems to be probable that this increased current flows through the field-induced junction between the inversion layer formed on the P^+ region near the P^+N junction edge and the underlying P^+ region as proposed by Grove *et al.* [7]. These charges are stored at the boundary of the boron doped SiO_2 and the pure SiO_2 . Therefore, the closer the boundary is to the Si surface, the larger the threshold voltage shift and drain leakage current shift become.

3.2. Diffusion of boron in polycrystalline Si and single crystalline Si in various drive-in ambients

As the next step, studies were made on the diffusion of boron in polycrystalline Si and single crystalline Si under various drive-in ambients. Figure 7 shows the diffusion depths of boron into polycrystalline Si and single crystalline Si under N_2 , O_2 and steam drive-in ambients at

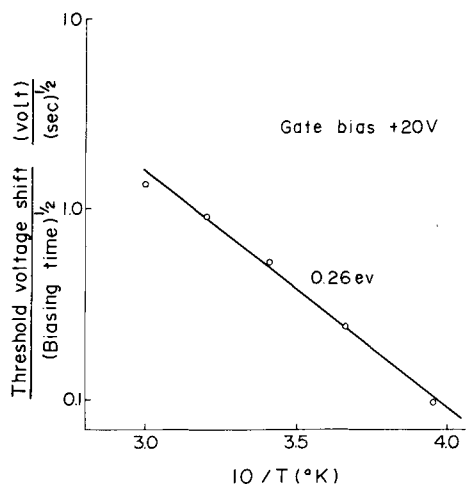


Fig. 6. Temperature dependence of the slopes of the straight line portions of the curves in Fig. 5.

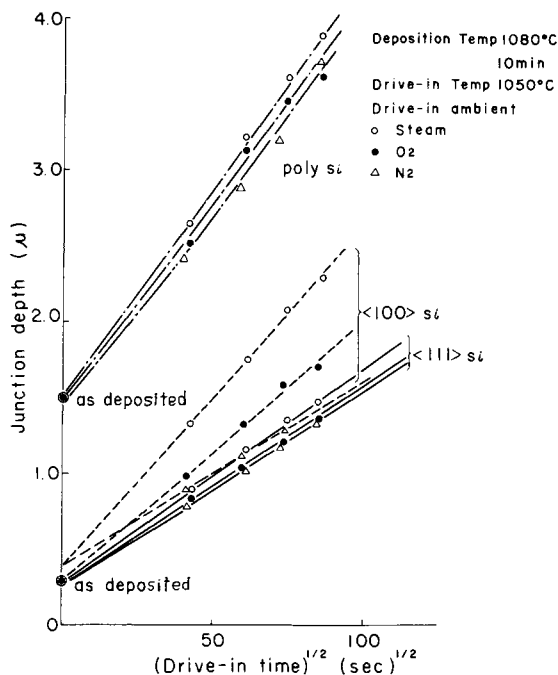


Fig. 7. Junction depths of boron in polycrystalline Si and single crystalline Si in various drive-in ambients.

1050°C after the boron predeposition process at 1080°C. In this figure, it can be recognized that there is almost no difference in junction depth among the three polycrystalline samples, just like the (111) plane single crystal samples, and that the diffusion depth of the former is about three times as large as that of the latter at 1050°C.

However, among the (100) plane single crystalline samples, there is a large dependence of the junction depth on the drive-in ambients, as reported previously [8] by Allen and Arand.

3.3. Diffusion of boron in SiO_2 in various drive-in ambients

Figure 8 shows the P - N junction depths formed in single crystalline Si by boron penetration through the SiO_2 films from doped polycrystalline Si. This figure shows that the diffusion of boron in SiO_2 films is strongly dependent on the drive-in ambients. It is particularly fast in an H_2 ambient. Figure 9 shows the surface concentrations of

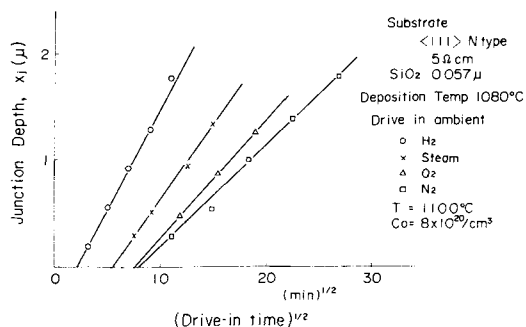


Fig. 8. Junction depths resulting from diffusion of boron into substrate Si through the SiO_2 layer from the doped polycrystalline Si in various drive-in ambients.

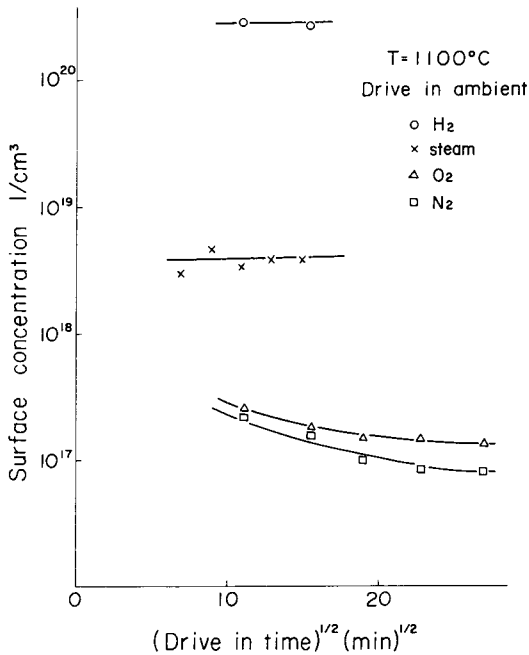


Fig. 9. Surface concentration of boron diffused into the Si substrate as a function of the square root of drive-in time.

boron in the substrates obtained from the Irvin's curves[9], using the measured sheet resistivity and junction depth.

3.4. Diffusion of phosphorus in SiO₂ in an H₂ and an N₂ ambient

Similarly, *P-N* junction depths formed in single crystalline Si substrates are shown in Fig. 10. Diffusion was carried out through an SiO₂ film from the phosphorus doped polycrystalline Si source of two different concentration levels in H₂ and N₂ ambients at 1150°C. This figure shows that the diffusion of phosphorus in SiO₂ is also dependent on the drive-in ambients, like boron. However, in case of the diffusion of phosphorus in SiO₂ in an N₂ ambient from a high concentration source, abnormally rapid diffusion is observed. It is considered that this phenomenon is attributed to the "melt through diffusion" which results

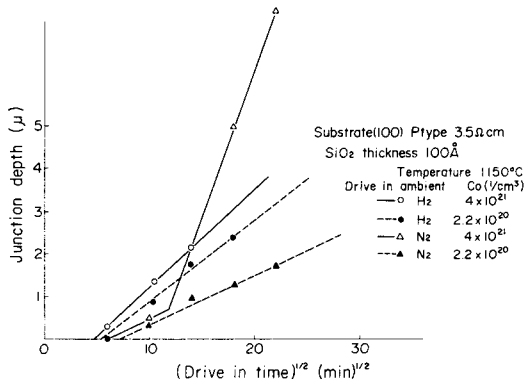


Fig. 10. Junction depths resulting from diffusion of phosphorus into substrate Si through the SiO₂ layer from the doped polycrystalline Si in H₂ and N₂ ambients.

from the formation of glassy compounds by a reaction of phosphorus with SiO₂. Figure 11 shows stained *P-N* junction patterns in the single Si substrate under the "normal solid diffusion" and the "melt through diffusion" conditions. In case of the "melt through diffusion", a disturbed *P-N* junction boundary is observed. Figure 12 shows the phosphorus surface concentrations on substrates of samples which were subjected to drive-in operation in an N₂ ambient at 1150°C. This figure shows that, under the "melt through diffusion", the surface concentration amounts to a very high value.

4. DISCUSSION

In order to estimate the diffusion coefficients of boron and phosphorus in SiO₂, the two boundary diffusion model[3] was applied. By this modelling, the specimen structure is simplified into a slab of medium 1 (SiO₂) of finite thickness X_0 on a semi-infinite block of medium 2 (single crystalline Si substrate). The boundary between the two media is taken to be $x = 0$. The concentration of the diffusant species, as a function of distance x and time t , is denoted as $C_1(x, t)$ in region 1 and as $C_2(x, t)$ in region 2. The concentration of diffusant species in polycrystalline Si is assumed to be held constant at C_0 . The value of C_0 can be obtained from the direct diffusion into single crystalline Si from the doped polycrystalline Si. m is the segregation constant of diffusant at the interface of Si substrate and SiO₂ and also m is used as the segregation constant at the interface of polycrystalline Si and SiO₂.

The diffusion equations for this case become,

$$D_1 \frac{\partial^2 C_1(x, t)}{\partial x^2} = \frac{\partial C_1(x, t)}{\partial t} \quad -X_0 < x < 0. \quad (2)$$

$$D_2 \frac{\partial^2 C_2(x, t)}{\partial x^2} = \frac{\partial C_2(x, t)}{\partial t} \quad 0 < x < \infty. \quad (3)$$

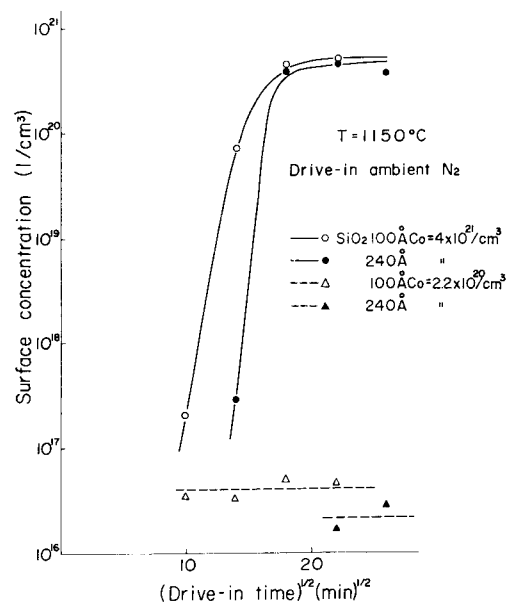


Fig. 12. Surface concentration of phosphorus diffused into the Si substrate as a function of the square root of drive-in time.

The initial and boundary conditions are:

$$\left. \begin{aligned} C_1 &= C_2 & x > -X_0 \text{ and } t = 0 \\ C_1(-X_0, t) &= C_0/m & t > 0 \\ C_2(0, t) &= mC_1(0, t) = C_s(t) & t > 0 \\ D_1 \frac{\partial C_1}{\partial x} &= D_2 \frac{\partial C_2}{\partial x} & \text{at } x = 0 \text{ and } t > 0 \\ C_2(x, t) &\rightarrow 0 & \text{as } x \rightarrow \infty \end{aligned} \right\} \quad (4)$$

In consequence of standard treatments, the solutions obtained are

$$C_2(x, t) = \frac{2mkC_0}{(m+k)m} \sum_{n=0}^{\infty} \left(\frac{m-k}{m+k} \right)^n \operatorname{erfc} \left[\frac{(2n+1)X_0}{2\sqrt{D_1 t}} + \frac{x}{2\sqrt{D_2 t}} \right] \quad (0 < x < \infty) \quad (5)$$

$$K \equiv \sqrt{D_1/D_2} \quad (6)$$

$$C_B \approx \left(\frac{2k}{m+k} \right) C_0 \operatorname{erfc} \left[\frac{X_0}{2\sqrt{D_1 t}} + \frac{X_j}{2\sqrt{D_2 t}} \right] \quad \left(\frac{X_0}{2\sqrt{D_1 t}} \geq 1 \right) \quad C_2(X_j, t) = C_B \quad (7)$$

Diffusion coefficient D_1 associated with SiO_2 can be determined in the following way. The bulk concentration is just compensated for at the interface ($x=0$) with certain diffusion time t^M and SiO_2 thickness X_0^M . At this critical situation, eqn (7) can be written as:

$$C_B \approx \frac{2k}{m+k} C_0 \operatorname{erfc} \left(\frac{X_0^M}{2\sqrt{D_1 t^M}} \right). \quad (8)$$

From eqn (8), D_1 can be calculated as:

$$D_1 = \frac{(X_0^M)^2}{4t^M} \frac{1}{\arg^2 \left[\operatorname{erfc} \left(\frac{m+k}{2k} \frac{C_B}{C_0} \right) \right]}. \quad (9)$$

Estimation of k can be made by varying the diffusion time and measuring the change of the junction depth, with other factors being kept constant. Under such conditions, eqn (7) reduces to:

$$\frac{X_0}{\sqrt{t}} + k \frac{X_j}{\sqrt{t}} = \text{constant}. \quad (10)$$

Figure 13 is a graphic representation of eqn (10) for boron. The values of k can be obtained from the gradients in Fig. 13. The segregation constant value was 0.3 for boron and 10 for phosphorus, from the values given by Grove *et al.* [10] and Deal *et al.* [11]. Finally, by applying these obtained values, the diffusion coefficient of boron in SiO_2 can be calculated. The results of calculation are shown in Table 2. From this table, it can be determined that the magnitude of diffusion coefficient of boron in SiO_2 at 1100°C ranges from $10^{-16} \text{ cm}^2/\text{sec}$ to $10^{-15} \text{ cm}^2/\text{sec}$ and that the value in the H_2 ambient is one order larger than in the other ambients.

Similarly, the diffusion coefficient of phosphorus in SiO_2 was calculated for the "normal solid diffusion". Figure 14 shows the temperature dependence of the diffusion coefficient of phosphorus in SiO_2 in H_2 and N_2 ambients. From this figure, it can be seen that the diffusion coefficient of phosphorus also depends on drive-in ambients, as boron. However, the values are about two orders of magnitude smaller than that of boron.

5. SUMMARY AND CONCLUSION

New types of instabilities in a P -channel Si gate transistor, such as threshold voltage shift by a positive gate bias at room temperature and the increase of drain leakage current are connected with the depth of boron penetration into the gate SiO_2 film and the motion of H^+ ions in that layer. The diffusion coefficient of boron in SiO_2 film, calculated by using the two boundary diffusion model, is dependent on the drive-in ambients. The value in

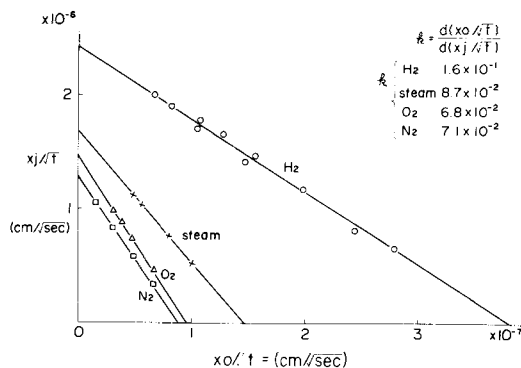


Fig. 13. Determination of k by eqn (11).

Table 2. Diffusion coefficients of boron in SiO_2 under various drive-in ambients

	$C_0 = 8 \times 10^{10}/\text{cm}^3$	$C_B = 10^{15}/\text{cm}^3$	$x_0 = 0.057 \mu$	$T = 1100^\circ\text{C}$
ambient	$\sqrt{t^M}$ (min) ^{1/2}	k ($-dx_0/dx_j$)	$\sqrt{D_1}$ ($\mu/\text{min}^{1/2}$)	D_1 (cm^2/sec)
H_2	2.1	1.6×10^{-1}	4.13×10^{-3}	2.84×10^{-15}
Steam	5.5	8.7×10^{-2}	1.56×10^{-3}	4.05×10^{-16}
O_2	7.5	6.8×10^{-2}	1.16×10^{-3}	2.24×10^{-16}
N_2	8.0	7.1×10^{-2}	1.08×10^{-3}	1.94×10^{-16}

NORMAL "SOLID DIFFUSION" "MELT THROUGH DIFFUSION"

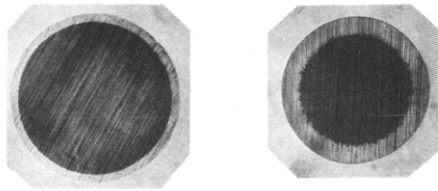


Fig. 11. Stain $P-N$ junction boundary patterns caused by phosphorus diffusion under the "normal solid diffusion" and the "melt through diffusion".

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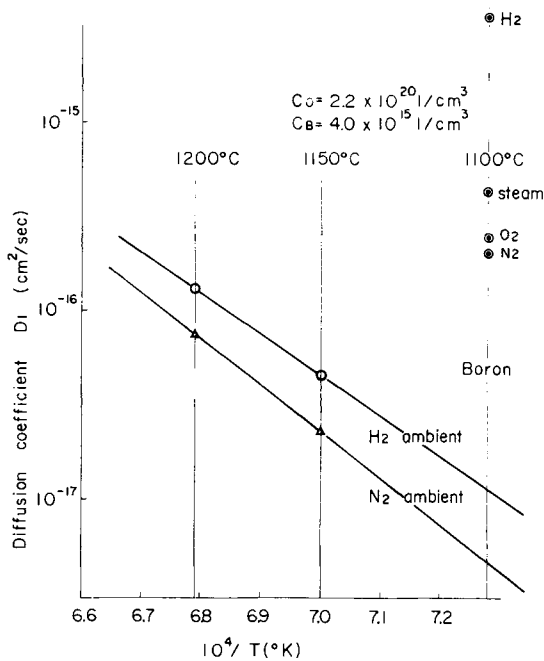


Fig. 14. Temperature dependence of the diffusion coefficient of phosphorus in SiO₂ in H₂ and N₂ ambients. Boron diffusion coefficient at 1100°C is also shown.

an H₂ ambient is one order larger than in the other ambients. Similarly, the diffusion coefficient of phos-

phorus in SiO₂ film depends on the drive-in ambients. From the view point of the fact that the diffusion coefficient of phosphorus in SiO₂ films is about two orders of magnitude smaller than that of boron, the *N*-channel Si gate process has an advantage over the *P*-channel Si gate process.

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