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Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment

Ian R. C. Post, *Member, IEEE*, Peter Ashburn, *Member, IEEE*, and Graham R. Wolstenholme, *Member, IEEE*

***Abstract*—A critical review is presented of the theories proposed in the literature to explain the current gain enhancement of polysilicon emitter bipolar transistors. From these theories a simplified analytical formulation is chosen which models the blocking properties of the interface, including tunneling through the interfacial oxide, reduced grain boundary mobility at the polysilicon/silicon interface, and the potential barrier created by segregated dopant, which can all give rise to an enhanced current gain. Also modeled are the mechanisms which limit the extent of any gain enhancement, such as recombination in the single-crystal emitter, in the bulk of the polysilicon, and at the polysilicon/silicon interface. This model is then applied in an original manner to a selection of experimental data in an effort to identify the dominant current gain mechanisms in polysilicon emitter transistors as a function of a given set of fabrication conditions.**

For devices with a deliberately grown oxide layer at the polysilicon/silicon interface, an *oxide tunneling model* can fully explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. For devices without a deliberately grown interfacial oxide layer, two distinct types of behavior are observed. First, for low concentrations of arsenic in the polysilicon ($<10^{20}$ cm^{-3}) and/or high anneal temperatures ($\geq 1000°$C), recombination of carriers via interface states at the polysilicon/silicon interface dominates the base current. This results in a current gain which is degraded below that of an extended emitter device. Secondly, for higher concentrations of arsenic in the polysilicon (1–2×10^{20} cm^{-3}) and anneal temperatures around 900°C, the increased segragation of arsenic to the grain boundaries pacifies the interface states, resulting in an enhancement of gain compared to that for an extended emitter device. Pseudo-two-dimensional modeling of the discontinuous interfacial layer in these devices is undertaken, which shows that the base current flows primarily through those areas of the interface that are free from oxide. The base current is therefore controlled by the fraction of the interface which is oxide-free.

I. Introduction

SINCE the discovery of polysilicon emitters in the 1970's [1]–[3], they have moved from being a laboratory curiosity to become a vital part of many high-speed bipolar [4], [5] and BiCMOS [6]–[8] production processes. The main reason for their success is that they provide a simple means of achieving the reductions in junction depth which are necessary when lateral device geometries are scaled. This co-ordinated scaling of lateral and vertical dimensions is important in order to provide an emitter structure in which the peripheral component of the emitter/base capacitance is maintained at a reasonable level. An important feature of polysilicon emitter technology is that reduced junction depths can be obtained without the degradation in gain which is obtained with conventional ion-implanted emitters [9]. On the contrary, an improvement in gain can be obtained, ranging from a factor of 3 [9] to 30 [10], with the size of the improvement depending upon the fabrication conditions used to produce the polysilicon emitter [11].

In spite of their widespread application, there is still considerable controversy over the precise mechanisms which control the current gain of a polysilicon emitter. Three physical mechanisms have been proposed to explain the improved gains of polysilicon emitter transistors. The first is termed the *"oxide tunneling model"* [3], [12] and explains the improved gains by tunneling through a thin oxide layer at the polysilicon/silicon interface. This model predicts not only a reduction in base current, and hence an improved gain, but also an increase in emitter resistance. The second is termed the *"grain boundary mobility model"* [9], [13], [14] and explains the improved gain by reduced mobility at the grain boundaries in the polysilicon and at the pseudo-grain boundary at the polysilicon/silicon interface. This model predicts a reduction in base current when the density of interface states at the grain boundaries is small, but an increase when the interface state density is high [14]. The third is termed the *"segregation model"* [15]–[17] and explains the improved gain by the presence of a potential barrier at the polysilicon/silicon interface due to the segregation of dopant. This model predicts a reduction in base current, with the amount of reduction depending upon the concentration of segregated arsenic at the interface. However, the *"segregation model"* predicts no change in emitter resistance. These three mechanisms can all be described as blocking mechanisms, since they are capable of giving an enhancement in gain compared with comparable con-

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ventional metal-contacted bipolar transistors. In order to fully explain the behavior of polysilicon emitters, it is necessary to also consider mechanisms which limit the extent of the gain improvement. These are mainly recombination mechanisms and include recombination at grain boundaries [14], recombination at the polysilicon/silicon interface [14], and recombination in the single-crystal emitter [18].

Since the publication of the above theoretical work, a large amount of experimental data has been gathered [19], which has greatly extended the understanding of the physical structure of the polysilicon emitter. High-resolution electron microscopy has been extensively used to study the polysilicon/silicon interface in detail, and has shown that a thin native oxide layer is invariably present [20]. The structure of the interfacial oxide depends critically upon the surface treatment carried out prior to polysilicon deposition [10], [20], with oxidizing chemical treatments giving a continuous oxide of approximately 14-Å thickness, and HF treatments giving a discontinuous oxide ranging in thickness from zero to around 8 Å. In oxide-free regions of the interface, epitaxial regrowth of the polysilicon occurs, extending typically a few hundred Angstroms into the polysilicon. In extreme cases, complete epitaxial regrowth of the polysilicon can occur [21] leading to a device with an extended single-crystal emitter [22]. The interfacial oxide structure also depends critically on annealing schedules [10], with oxide breakup being more likely for higher temperatures and thinner oxides.

Polysilicon emitter transistors and a variety of test structures have been fabricated in order to assess the importance of key processing parameters on the base current [3], [9]–[11], [23]–[41] and emitter resistance [29], [30], [42]–[48], and to obtain an insight into the mechanisms which control the device behavior. Specifically, the influence of the interface treatment [11], [45], the annealing temperature [10], the polysilicon thickness [28], [31], [37], dopant segregation [24], [28], and hydrogen passivation [28], [35] have all been studied. Many of the processing parameters have been shown to have a large influence on the device behavior, giving rise to changes in current gain by more than an order of magnitude.

In spite of this large amount of experimental and theoretical work, there is still considerable controversy over the precise mechanisms which control the base current of a polysilicon emitter transistor. Some of this controversy arises because of the different types of polysilicon emitter transistors which have been studied and the different fabrication conditions used to produce the devices. Another cause is the large number of competing mechanisms which can occur at the polysilicon/silicon interface and the resulting complexity of the device modeling. This paper will address these problems by first reviewing the competing theories for current gain enhancement, which will lead to a simple unified model for the base current of a polysilicon emitter transistor. The wide range of experimental data on polysilicon emitters will then be briefly reviewed, and then re-assessed using this unified theory in an original manner. This approach will allow the identification of the mechanisms which control the current gain for a given set of fabrication conditions.

II. Types of Polysilicon Emitter

Several types of polysilicon emitter have been studied in the literature, as illustrated in Fig. 1. In the first type (Fig. 1(a)), the n^+ dopant is confined to the polysilicon so that the metallurgical emitter/base junction coincides with the polysilicon/silicon interface. This structure is analogous to the MIS tunnel device [49], [50], and is therefore referred to here as a SIS emitter. Very high current gains have been reported for this structure [51]–[53], although the base characteristic is very nonideal, and is often accompanied by a "kink" at high emitter/base voltages. These disadvantages, and its poor current carrying capability [54], make it unsuitable for realizing high-speed circuits. This structure will therefore not be discussed in this paper, although, it should be pointed out that SIS behavior can be obtained in polysilicon emitters if the emitter/base junction is too shallow.

The second type of structure (Fig. 1(b)) is a polysilicon emitter in which the n^+ dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitter/base junction. The emitter/base depletion region therefore resides entirely in the single-crystal silicon, which leads directly to very ideal base characteristics. In order to obtain enhanced gain, the emitter/base junction depth must be shallower than the hole diffusion length in the single-crystal emitter, otherwise the gain is dominated by recombination in the single-crystal emitter. The crucial part of this structure is the polysilicon/silicon interface which can have a large effect on the base current of the transistor.

The third type of structure illustrated (Fig. 1(c)) is an extended emitter in which the n^+ polysilicon is replaced by single-crystal silicon. This can arise in practice if complete epitaxial regrowth of the polysilicon is induced during the emitter drive-in [21], [22]. The current gain is therefore unaffected by the interface, and hence it behaves like a conventional bipolar transistor. For the purposes of this paper this is a useful structure to consider, since a comparison of the gain of a polysilicon emitter with that of an identical extended emitter gives a measure of the gain enhancement or reduction resulting from the presence of the polysilicon/silicon interface.

Finally, the last structure shown (Fig. 1(d)) is that of a conventional metal-contacted emitter. In this type of device the emitter is formed by direct ion implantation into the silicon substrate, followed by a high-temperature anneal which is designed to activate the emitter dopant. When the emitter junction depth is scaled in such a device a reduction of current gain results because the emitter is transparent to the injected minority-carrier current [9]. This severe disadvantage precludes the use of metal-contacted emitters in high-speed bipolar processes.

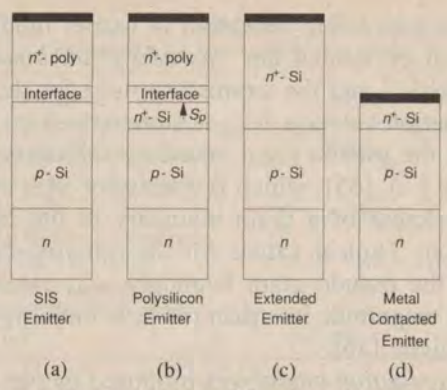

Fig. 1. Schematic diagrams of (a) an SIS emitter, (b) a polysilicon emitter, (c) an extended emitter, and (d) a metal contacted emitter.

III. Effective Recombination Velocity

In this paper the polysilicon/silicon interface is modeled by using an effective recombination velocity S_p, which defines the recombination velocity at the lower side of the polysilicon/silicon interface, as shown in Fig. 1(b). In order to relate the effective recombination velocity to the base current, it is necessary to model recombination in the single-crystal emitter region. For a shallow emitter which is quasi-transparent, the base current can be modeled using the approach of del Alamo *et al.* [18]

$$J_{BO} = \frac{qn_{io}^2}{G_{\text{eff}}(W_E) + N_{D\text{eff}}(W_E)/S_p} \cdot \left[1 + \int_0^{W_E} \frac{G_{\text{eff}}(W_E) - G_{\text{eff}}(x)}{\tau_p(x) N_{D\text{eff}}(x)} dx + \frac{N_{D\text{eff}}(W_E)}{S_p} \int_0^{W_E} \frac{dx}{\tau_p(x) N_{D\text{eff}}(x)}\right] \quad (1)$$

where G_{eff} is the effective emitter Gummel number, $N_{D\text{eff}}$ is the "effective" doping concentration in the emitter, τ_p is the hole lifetime in the emitter, while $x = 0$ is defined to be the edge of the emitter/base depletion region, and $x = W_E$ is the position of the polysilicon/silicon interface.

The term is brackets in (1) represents a first-order correction for recombination in the single-crystal emitter, although, for the vast majority of devices analyzed in this paper recombination in the single-crystal emitter is negligible. The only notable exception to this is for devices with thick interfacial oxide layers. In order to calculate predicted values of base current to compare with reported experimental values in the literature, (1) is used together with measured emitter profiles, where available. In cases where the emitter profile is not given, a Gaussian profile is assumed in the single-crystal emitter, the Gaussian being constructed using estimates of the emitter/base junction depth and the doping concentration at the interface.

IV. Current Gain Theories

The general model to be used in this study to calculate the effective recombination velocity S_p follows from the unified model of Yu *et al.* [14], and is shown schematically in Fig. 1(b). It is assumed that the polysilicon layer consists of only one crystalline grain separated from the monosilicon substrate by an interfacial region of finite thickness, which will be described in detail further on. A density of interface traps is also assumed to exist at the two interfaces between the interface region and the polysilicon grain and the monosilicon substrate.

The effective recombination velocity S_p can be expressed as [14]

$$S_p = S_I + \left(\frac{1}{T_{\text{block}}} + \frac{1}{S_I + S_g}\right)^{-1} \quad (2)$$

where S_I models the recombination of minority carriers via traps at the interface, and is given by

$$S_I = \tfrac{1}{2} N_{it} c_p v_{\text{th}} \quad (3)$$

and N_{it} is the total density of interface traps per unit area, c_p is the capture cross section, and v_{th} is the thermal velocity. The factor of $1/2$ arises in (3) from interface traps being equally distributed between the upper and lower sides of the interface.

The parameter S_g describes the recombination of minority carriers in the bulk of the polysilicon grain, and is given by [14]

$$S_g = a_g - \frac{b_g^2}{a_g + S_M} \quad (4)$$

where

$$a_g = \frac{D_g}{L_g} \coth\left(\frac{W_p}{L_g}\right)$$

$$b_g = \frac{D_g}{L_g} \operatorname{csch}\left(\frac{W_p}{L_g}\right) \quad (5)$$

D_g and L_g are the diffusivity and diffusion length, respectively, of minority carriers in the grain, S_M is the effective recombination velocity at the metal contact, and W_p is the polysilicon thickness.

The term T_{block} in (2) describes the blocking action of the polysilicon/silicon interface, and the expression used to calculate T_{block} is determined by the dominating mechanism. The three competing mechanisms are tunneling, reduced mobility in the pseudo-grain boundary at the interface, and thermionic emission over a segregation barrier. These will now each be considered in turn.

The *oxide tunneling model* was first proposed by de Graaff *et al.* [3], and later modified by Eltoukhy *et al.* [12]. The model assumes that a thin tunneling oxide is present at the polysilicon/silicon interface. Holes injected from the base into the emitter are forced to tunnel through the interfacial oxide layer, thereby blocking minority carrier flow into the polysilicon and hence producing a reduction in base current. The expression that will be used for T_{block} in the *oxide tunneling model* is summarized in Table I. Similarly, the majority-carrier electrons which flow from the polysilicon into the silicon must also tunnel

TABLE I
ANALYTICAL EXPRESSIONS USED FOR T_{block} IN THE THREE BLOCKING MECHANISMS IN THIS STUDY

($b_h = 4\pi\delta/h\sqrt{2m_l^*\chi_h}$, $c_h = 2\pi\delta/h\sqrt{2m_l^*/\chi_h}$, χ_h is the barrier height to holes, m_p^* is the effective mass of holes in silicon, m_l^* is the effective mass of holes in the oxide, δ is the interfacial oxide thickness, μ_{pgb} is the minority-carrier mobility in the pseudo-grain boundary, Δ is the thickness of the pseudo-grain boundary, N_E is the electrically active doping density in the emitter, and N_{Int} is the electrically active doping density of segregated dopant at the interface.)

Blocking Model	Expression Used for T_{block}	
Oxide tunneling model	$T_{block} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{\exp(-b_h)}{1 - c_h kT}$	(6)
Pseudo grain-boundary mobility model	$T_{block} = \frac{kT}{q} \frac{\mu_{pgb}}{\Delta}$	(7)
Segregation model	$T_{block} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{N_E}{N_{Int}}$	(8)

through the oxide. This limits the maximum current carrying capability of the device, since it gives rise to a series emitter resistance [43]–[45].

The *grain boundary mobility model* was first proposed by Ning *et al.* [9], who used it to explain electrical results obtained on transistors with conventional implanted emitters on top of which a layer of arsenic *in situ* doped polysilicon was deposited. A gain enhancement of a factor of 3 was achieved for the polysilicon emitters, compared to conventional metal-contacted emitters, which was attributed to a lower minority-carrier mobility in the polysilicon, when compared to single-crystal silicon. Eltoukhy *et al.* [13] extended the above simple two-region model to take into account the effect of grain boundaries on the minority carriers, which they assumed were infinitely thin, and characterized by a large concentration of interface states. Alternatively, Yu *et al.* [14] modeled the grain boundaries by assuming that they have a finite thickness, in which the minority-carrier mobility is reduced with respect to that in the bulk of the grain. Recombination is assumed to occur only at the interface between the grain and grain boundary, but not actually in the grain boundary. Furthermore, recombination at the polysilicon/silicon interface was also modeled. The grain boundaries can effect minority-carrier transport in two ways. First, if the density of interface states is large enough ($>10^{14}$ cm^{-2}) then they will act as efficient recombination centers, and no improvement in current gain will result over that for a metal-contacted emitter. However, for low densities of interface states ($\leq 10^{12}$ cm^{-2}), recombination at the grain boundary interface becomes negligible, and the minority-carrier transport is dominated by the reduced carrier mobility in the grain boundaries. This has the overall effect of lowering the minority-carrier mobility in the polysilicon layer, and so reducing the base current.

In this paper the polysilicon layer is assumed to consist of only one crystalline grain, although the disordered interfacial region will be treated as a pseudo-grain boundary with a corresponding reduction in carrier mobility. This model will be termed the *"pseudo-grain boundary mobility model,"* and the expression used for the blocking recombination velocity T_{block} is summarized in Table I. A value for the pseudo-grain boundary thickness Δ will be chosen as 7 Å [55], which is consistent with the approximate thickness of a grain boundary in the bulk of the polysilicon. Typical values for the minority-carrier mobility in the pseudo-grain boundary μ_{pgb} can be several orders of magnitude less than the hole mobility in single-crystal silicon [56].

The *segregation model* was proposed by Ng *et al.* [15] to explain the observation that the current gain of polysilicon emitter transistors is dependent upon the amount of arsenic which segregates to the interface [24], [28]. Typically, the concentration of arsenic at the polysilicon/silicon interface can be a factor of two or three larger than the concentration of arsenic in the bulk of the grains. Ng *et al.* [15] argued that if the segregated arsenic is electrically active then this could form a low–high–low barrier, although the model will not predict any increase in emitter resistance. The expression that will be used for T_{block} in the *segregation model* is summarized in Table I [15].

It should be pointed out that the doping densities in (8) (see Table I) should strictly be effective doping densities, which include the effects of bandgap narrowing [57]. Since effective doping densities tend to saturate to a constant value as the doping concentration increases [58], this implies that the segregation barrier will be smaller than predicted in [15]. For example, for this mechanism to dominate the base current, the barrier created by the segregated dopant must be greater than about $2kT$. For a typical emitter doping concentration of 10^{20} cm^{-3}, this means that the segregated doping concentration must be greater than around 8×10^{20} cm^{-3} if the electrically active arsenic concentration is used, or greater than 10^{23}–10^{24} cm^{-3} if the effective doping concentration is used.

In order to obtain accurate predictions of effective recombination velocity and base current from doping profiles, it is necessary to take into account heavy doping effects, which influence parameters such as hole lifetime τ_p, hole mobility μ_p, and bandgap narrowing ΔE_g^{app}. Values for these parameters, as a function of doping, are taken from the work of del Alamo *et al.* [58]. Finally, it is necessary to assume values for some parameters for which measured values are not available. These are summarized in Table II, and the given values have been used throughout this paper unless otherwise stated.

V. EXPERIMENTAL RESULTS

Over the past ten years or so, a considerable amount of experimental results on polysilicon emitter transistors have been published in the literature [19]. In this section, approximately eight or so key papers have been chosen which are representative of a broad cross section of important experimental results. The results of these papers will be quoted in the form of raw experimental data (fo

TABLE II
PARAMETER VALUES USED IN THIS STUDY

Parameter	Value	Reference
Hole effective mass in silicon (m_p^*)	$0.66m_o$	[12]
Hole effective mass in the interfacial oxide layer (m_i^*)	$0.42m_o$	[12]
Interface trap capture cross section × thermal velocity ($c_p v_{th}$)	2×10^{-9} cm^3 · s^{-1}	[54]
Grain boundary thickness (Δ)	7 Å	[55]
Recombination velocity at metal contact (S_M)	10^6 cm · s^{-1}	[14]

example, measured current densities and resistances, etc.), and then *all* subsequent modeling will be performed in an original manner using the simplified analytical equations outlined in Section IV. This will allow a consistent comparison to be made between the predictions of the three blocking mechanisms and the reported experimental results.

A. Devices with Interfacial Oxides

1) Effect of an Interface Anneal: The analysis will begin by considering experimental results from devices with an interfacial oxide layer, which is generally grown using an oxidizing chemical treatment. It has been well documented in the literature that such an interface treatment gives a significant improvement in the current gain. For example, Ashburn *et al.* [11] have shown that devices given an RCA clean prior to polysilicon deposition had gains five times higher than those given an HF etch. A more detailed characterization of the influence of the interfacial oxide on the current gain was carried out by Wolstenholme *et al.* [10]. In this experiment, an interface anneal was carried out after polysilicon deposition, but prior to emitter implant, to thermally stress the interfacial oxide. In this way, a range of interfacial oxide structures was obtained without significantly altering the emitter and base doping profiles. The results are shown in Fig. 2 for devices given an RCA clean prior to polysilicon deposition. It is evident that a factor of 100 increase in base current is obtained as the temperature of the interface anneal is increased from 800 to 1100°C. These electrical results were correlated with high-resolution TEM observations of the polysilicon/silicon interface which showed that an interfacial oxide was present, which broke up by increasing amounts as the interface anneal temperature was increased.

High-resolution TEM showed that for interface anneal temperatures of 900°C or below, the interfacial oxide was continuous and uniform, with a thickness of 14 ± 2 Å. It is therefore possible to apply the *oxide tunneling model* unambiguously to these results. Fig. 2 shows the modeled values of base current (using (6) of Table I and the parameters in Table II) for different values of oxide barrier height, assuming that the devices are tunneling-dominated (i.e., $S_I = 0$ and $T_{block} << S_g$). It is evident that these devices can be modeled by an oxide barrier height

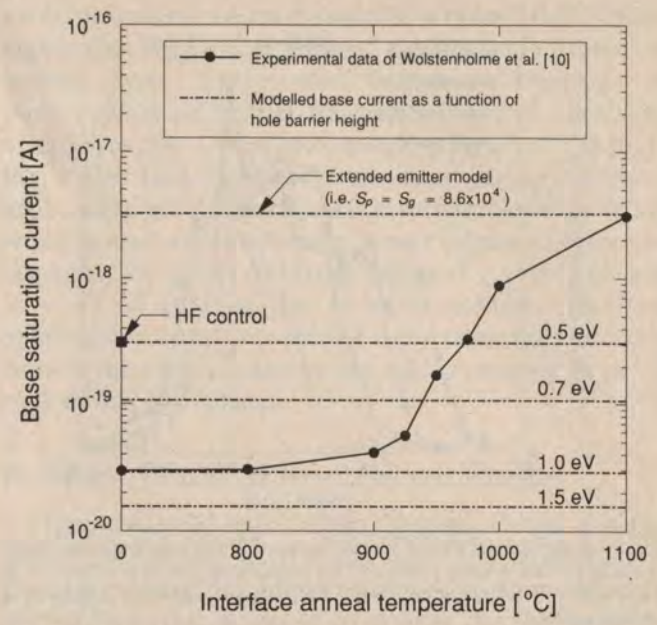

Fig. 2. Experimental data of Wolstenholme *et al.* [10] showing base saturation current as a function of interface anneal for devices with a deliberately grown interfacial oxide layer. The base current has been modeled by assuming that the dominant blocking mechanism is tunneling through the interfacial oxide layer (i.e., *oxide tunneling model* with $\delta = 14$ Å, and $S_I = 0$). Also shown is the modeled base current using the *extended emitter model* ($T_{block} = \infty$, and $S_I = 0$).

of 1.0 eV. Also modeled in Fig. 2 is the base current of an extended emitter device, in which no blocking or recombination at the interface is assumed to occur (i.e., $T_{block} = \infty$ and $S_I = 0$). As can be seen, a good fit to the 1100°C interface anneal device is achieved, which implies that the interface has no effect on the base current of this device. This conclusion is consistent with the TEM analysis, which showed that the interfacial oxide had completely "balled-up," such that 97% of the interface was oxide-free. These experimental results show that the interfacial oxide plays a doiminant role in controlling the current gain of polysilicon emitter transistors with deliberately grown interfacial oxide layers.

Rutherford backscattering (RBS) analysis has been used by Wolstenholme [57] to investigate the distribution of arsenic at the interface for the devices reported in Fig. 2. The results of this analysis are shown in Fig. 3, and indicate that the concentration of arsenic at the polysilicon/silicon interface remains unchanged for interface anneals up to a temperature of 1000°C. Applying the *segregation model* to the barriers produced in Fig. 3 for the RCA control device, produces a blocking recombination velocity of either 7.9×10^4 cm · s^{-1} (no bandgap narrowing), or 1.2×10^6 cm · s^{-1} (with bandgap narrowing). This compares with an extracted T_{block} of 3.2×10^2 cm · s^{-1} for the control device in Fig. 2, which therefore implies that the *segregation model* cannot explain the experimental results in either Figs. 2 or 3.

2) Temperature Dependence of Current Gain: Further evidence supporting the *oxide tunneling model* is obtained from measurements of the temperature dependence of cur-

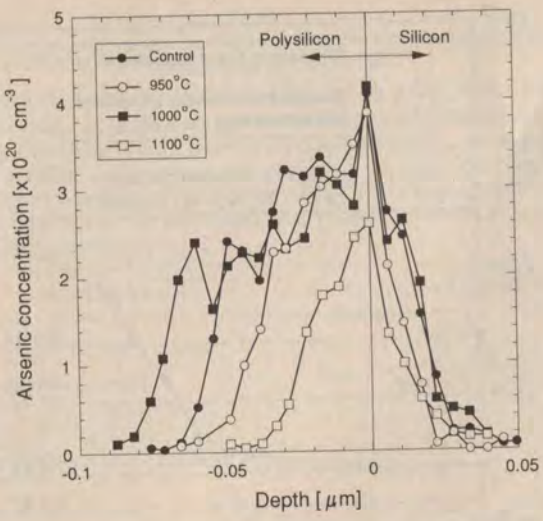

Fig. 3. Experimental data of Wolstenholme [57] showing Rutherford backscattering (RBS) arsenic profiles of the polysilicon/silicon interface for devices with a deliberately grown interfacial layer, subjected to various interface anneals.

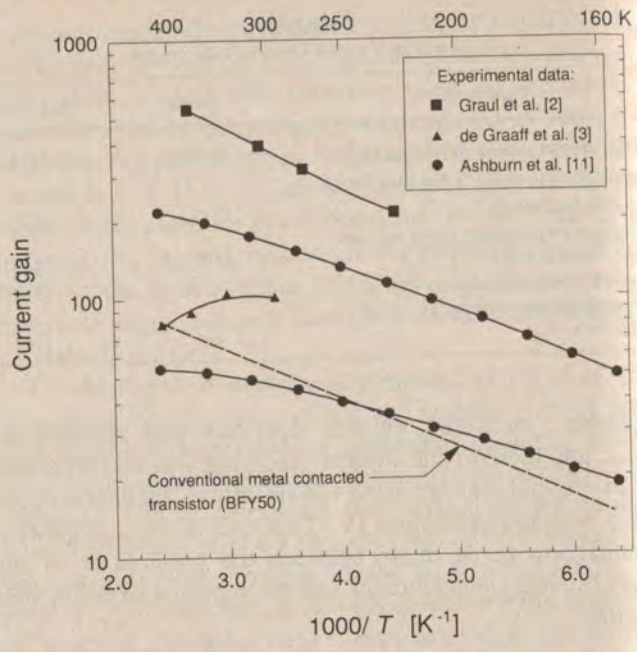

Fig. 4. Experimental data of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices with a deliberately grown interfacial oxide layer. It can be clearly seen that the temperature dependence of current gain is less than that for a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

rent gain. Several authors [2], [3], [11] have reported that polysilicon emitter transistors with a chemically grown interfacial oxide have a gain which varies less strongly with temperature than observed for conventional metal-contacted transistors. Fig. 4 shows the current gain, as a function of inverse temperature, from the work of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11]. Also shown in Fig. 4 is the temperature dependence of current gain for a conventional metal-contacted transistor (whereby the temperature dependence of the current gain is determined by the difference in bandgap narrowing in the base and emitter). It can be seen, especially for temperatures above 300 K, that the current gain becomes less sensitive to temperature than in conventional metal-contacted transistors. In fact, the results from de Graaff *et al.* [3] even show a negative temperature coefficient. Ashburn *et al.* [11] modeled the temperature dependence of gain, and showed that the *oxide tunneling model* could explain the observed results for the whole temperature range in Fig. 4.

3) Emitter Resistance: The presence of a deliberately grown oxide layer at the polysilicon/silicon interface has been shown to block majority-carrier flow, leading to an increase in emitter resistance [43]–[45]. Measurements of specific interfacial resistivity for devices with deliberately grown interfacial oxide layers typically range from 200 to 500 $\Omega \cdot \mu m^2$ [43]–[45]. This compares with generally far lower values of 10 to 200 $\Omega \cdot \mu m^2$ [29], [43], [45] for devices without deliberately grown interfacial oxide layers. By applying the *oxide tunneling model* to the devices with interfacial layers, assuming an average oxide thickness of 14 Å [10] and an electrically active polysilicon doping level of 5×10^{19} cm^{-3} [10], implies a barrier height to electrons of around 0.3 eV (using the analytical expression for emitter resistance derived in [30]). Comparing this value with the barrier height for holes, which is around 1 eV (Fig. 2), it can be clearly seen that there exists an asymmetry in oxide barrier heights for electrons and holes.

Wolstenholme *et al.* [45] have performed experiments on the "balling-up" of the interfacial oxide from interface anneals, and then correlated this with measurements of emitter resistance, as shown in Fig. 5. Also shown in Fig. 5 are the base current data from Fig. 2. Some important differences can be seen in the variation of the base current and emitter resistance with interface anneal temperature. Most notable is a substantial reduction in emitter resistance for the device given a 900°C interface anneal, compared to the control device, even though the TEM analysis showed that the interfacial layer for both devices was continuous and unbroken. Two-dimensional modeling by Hamel *et al.* [59], as shown in Fig. 6, has recently shown that this result can be explained if a limited number of widely spaced small gaps in the oxide layer are produced in the 900°C interface anneal, even though nearly 99% of the oxide remains continuous (and so therefore these gaps would be difficult to observe by TEM). Since a large proportion of the interface remains intact, a reduction in base current is still obtained, as observed in Fig. 2. These results show that it is possible to produce a device with both a high gain and a low emitter resistance [60].

Measurement and modeling of the temperature dependence of emitter resistance for devices with deliberately grown interfacial oxide layers has been conducted by Yung *et al.* [46]. They found that the *oxide tunneling model* could fit the observed temperature dependence, although the shape of the tunneling barrier had to be

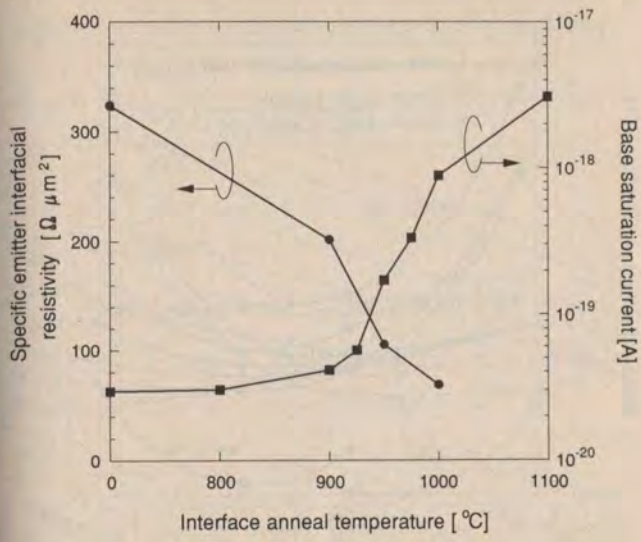

Fig. 5. Experimental data of Wolstenholme *et al.* [10], [45] showing the specific emitter resistivity and base saturation current as a function of interface anneal temperature for devices with a deliberately grown interfacial oxide layer.

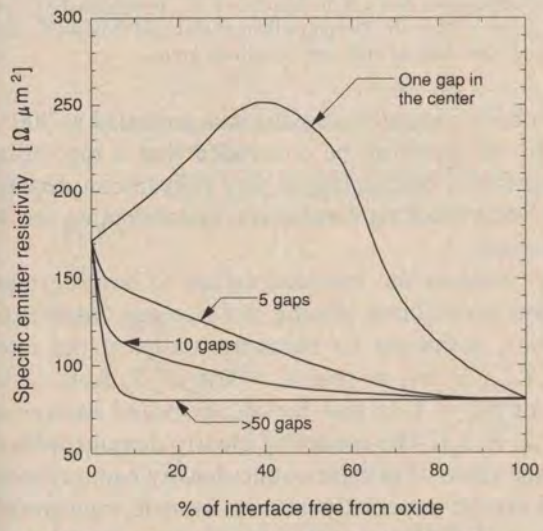

Fig. 6. Modeled specific emitter resistivity as a function of the percentage of the interface which is oxide-free for a device with a HF interfacial treatment, from the work of Hamel *et al.* [59]. It can be clearly seen that not only the amount of oxide, but its distribution along the interface can dramatically effect the emitter resistance.

changed from rectangular to triangular. Yung *et al.* [46] speculated that dopant pileup at the interface was the physical cause of this change in barrier shape.

4) p-n-p Polysilicon Emitter Transistors: As an aid to understanding the physics of polysilicon emitter transistors it is worthwhile here to examine the experimental results from p-n-p polysilicon emitter transistors [61]–[63]. The extracted values of barrier height (χ_h = 1.0 eV and χ_e = 0.3 eV) from measurements on n-p-n polysilicon emitter transistors imply that p-n-p transistors should have a high emitter resistance and a small gain improvement. In practice, however, this is found not to be the case. Reported values of current gains for p-n-p polysilicon emitter transistors with deliberately grown interfacial oxide layers, are between a factor of 2 [61] and 10 [63] times higher than for devices without a deliberately grown interfacial layer. Furthermore, the emitter resistance of p-n-p polysilicon emitter transistors, with an interfacial oxide layer, are only approximately a factor of 2–3 [61]–[63] higher than for the corresponding devices without a deliberately grown interfacial layer. If the *oxide tunneling model* is used to extract oxide barrier heights to holes and electrons, the values of barrier height of χ_h = 0.3 eV and χ_e = 1.0 eV [63] are seen to be inconsistent with those obtained from measurments on n-p-n transistors. Further work is therefore needed on the *oxide tunneling model* to explain this discrepancy.

B. Devices Without an Interfacial Oxide Layer

For commercial applications, devices without a deliberately grown interfacial oxide layer are generally preferred because of the emitter resistance problem described above. However, it should be pointed out that an interfacial layer is invariably present at the polysilicon/silicon interface, even in devices given an HF etch prior to polysilicon deposition [10].

1) Segregation of Dopant to the Interface: Confirmation of the role of the interface in controlling the gain comes from the work of Neugroschel *et al.* [24], who have fabricated bilayer polysilicon diodes by first depositing undoped polysilicon and then capping the device with *in situ* arsenic-doped polysilicon. Drive-in conditions were carefully chosen so that the amount of arsenic segregated to the polysilicon/silicon interface could be varied. A long low-temperature drive-in (e.g., 64 h at 800°C) was used to preferentially diffuse the arsenic along the grain boundaries, and dope the grain boundaries and interface to a concentration of around 5×10^{20} cm^{-3}. However, the temperature of the drive-in was not high enough to diffuse arsenic into the bulk of the grains [64], which remained at a low concentration of $\leq 10^{18}$ cm^{-3}. This device was then compared to both an unannealed bilayer device (with a low arsenic concentration of $\leq 10^{18}$ cm^{-3} in the grains and at the interface), and to a control device with a single *in situ* doped polysilicon layer (with an arsenic concentration of $\sim 10^{21}$ cm^{-3} at the interface and around 5×10^{20} cm^{-3} in the grains).

Fig. 7 shows the current–voltage characteristics for the annealed and unannealed bilayer devices, and the *in situ* doped monolayer polysilicon control device. Also shown is the characteristic for a metal-contacted control with no polysilicon layer. It can be seen from Fig. 7 that the current from the annealed bilayer device is nearly identical to the monolayer control. However, these two devices have *different* doping concentrations in the bulk polysilicon ($\sim 10^{18}$ cm^{-3} and 5×10^{20} cm^{-3}, respectively), but have *similar* concentrations of arsenic at the polysilicon/silicon interface (5×10^{20}–10^{21} cm^{-3}). It can thus be concluded that the *concentration* of arsenic at the polysilicon/silicon interface is important in controlling the hole current. In addition, the hole current from the metal-con-

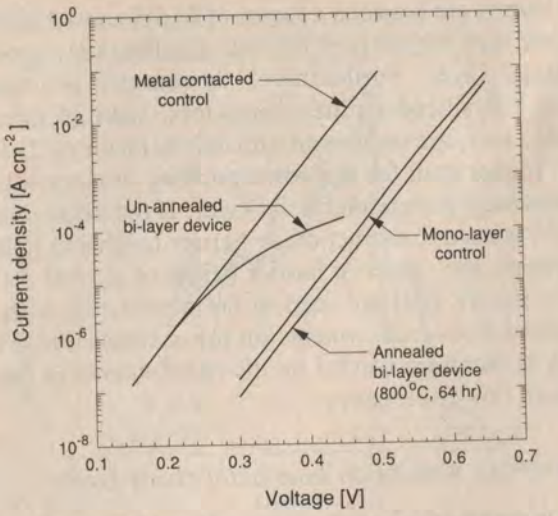

Fig. 7. Current–voltage characteristics of the diodes as analyzed by Neugroschel *et al.* [24]. The devices shown are the metal-contacted control, the single-layer polysilicon control, and the annealed and unannealed bi-layer devices.

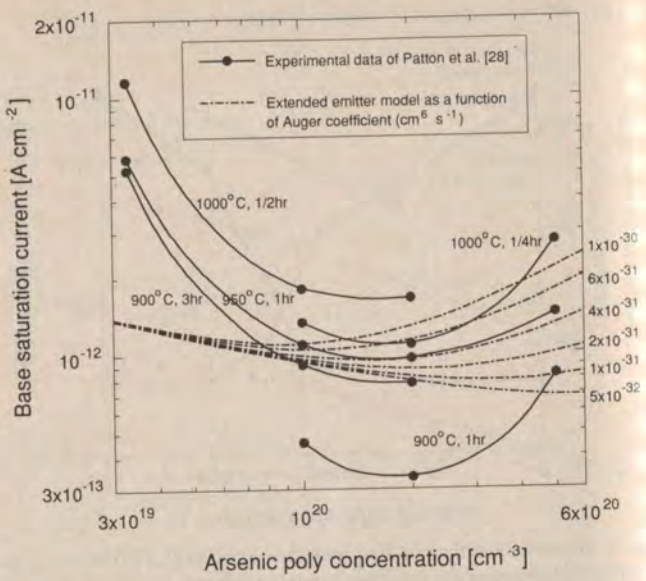

Fig. 8. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for various emitter anneals. Also shown is the modeled base current as a function of Auger coefficient in the polysilicon, assuming that no blocking or recombination mechanisms exists at the interface (i.e., the *extended emitter model* with $T_{\text{block}} = \infty$, $S_I = 0$). The polysilicon is assumed to be 40% electrically active and consisting of only one crystalline grain.

tacted control is almost identical to that of devices with low arsenic concentrations at the interface, which implies the density of interface states is so large as to recombine all the minority holes at the interface. An interface state density of 6×10^{14} cm^{-2} can be calculated by using (1), assuming that the hole current is entirely dominated by recombination at the interface (i.e., $T_{\text{block}} = \infty$, and $S_I >> S_g$ so that $S_p = 2S_I$ in (2)).

For the devices with a high arsenic concentration at the interface, a dramatic reduction of hole current by a factor of 600 is obtained. Assuming that the hole current is again dominated by recombination at the interface ($T_{\text{block}} \approx 0$, so that $S_p = S_I$ in (2)) then an upper limit of 2×10^{11} cm^{-2} can be obtained for the interface state density. The increase of segregated arsenic from 10^{18} to 5×10^{20} cm^{-3} at the interface has therefore reduced the interface state density by over a factor of 3000.

The above results demonstrate the importance of recombination via states at the polysilicon/silicon interface, and also its relationship to the segregated arsenic concentration. Patton *et al.* [28] have also shown that recombination at the interface cannot be ignored, particularly when the doping concentration in the polysilicon is low. Fig. 8 shows the measured base current as a function of polysilicon doping level for various emitter drive-in conditions. Nearly all the devices have large base currents at low polysilicon doping levels (3×10^{19} cm^{-3}), which fall to minimum values around 1–2 $\times 10^{20}$ cm^{-3} and then rise for increased doping levels up to 5×10^{20} cm^{-3}. Also shown in Fig. 8 is the modeled base current from the extended emitter model (i.e., $T_{\text{block}} = \infty$ and $S_I = 0$, so that $S_p = S_g$ in (2)), which can qualitatively explain the increase in base current at high values of doping (2–5 $\times 10^{20}$ cm^{-3}) by increased Auger recombination in the bulk polysilicon. However, the extended emitter model cannot explain either the sharp increase in base current at the low polysilicon doping levels of 3×10^{19} cm^{-3}, or the reduction in base current for the devices annealed at 900°C for 1 h. It can therefore be concluded that a recombination mechanism is dominating at low polysilicon doping levels, while a blocking mechanism is dominating the 900°C 1-h devices.

Fig. 9 shows the modeled values of base current as a function polysilicon doping for various interface state densities, assuming no blocking action at the interface (i.e., $T_{\text{block}} = \infty$, so that $S_p = 2S_I + S_g$ from (2)). The case for $N_{it} = 0$ is that for the *extended emitter model* (i.e., $S_p = S_g$). The modeling clearly demonstrates that a constant value of interface state density cannot model the base current, especially at low arsenic concentrations. Patton *et al.* [28] argued that the arsenic segregation could lower the trap density at the interface. Fig. 10 models the base current of the device annealed at 950°C for 1 h, by the combined contribution of recombination via interface states (for interface densities as a function of arsenic concentration) and minority-carrier transport in the bulk polysilicon (assuming no blocking action at the interface, i.e., $T_{\text{block}} = \infty$). A reasonable fit to the measured base current can result, if it is assumed that the interface state density reduces from 2×10^{14} to 1.4×10^{13} cm^{-2}, as the arsenic concentration increases from 3×10^{19} to 2×10^{20} cm^{-3}.

Fig. 11 shows the fitted interface state density, as a function of polysilicon doping, for all the drive-in conditions in Fig. 9. Also shown are the modeled results from Neugroschel *et al.* [24], who used low-temperature drive-ins of 800°C, and the modeled results from Meister *et al.* [37] who used rapid thermal annealing at 1050°C. The most immediate trend visible is that of a dramatic reduction in interface state density for increases in arsenic con-

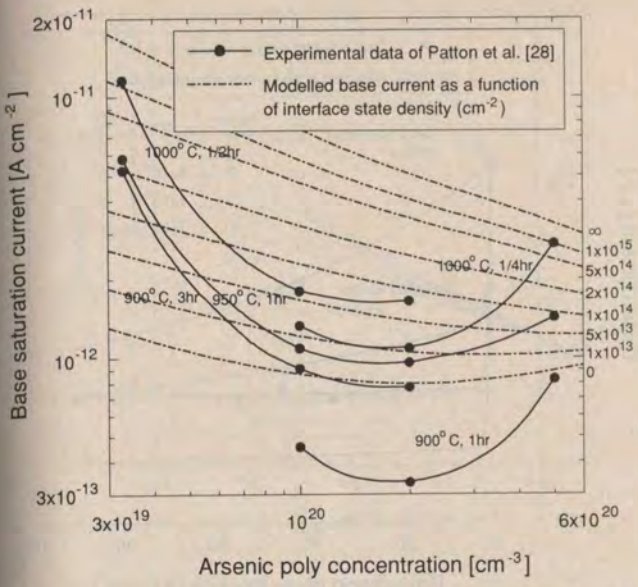

Fig. 9. Experimental data of Patton *et al.* [28]. Also shown is the modeled base current as a function of interface state density, assuming no blocking at the interface (i.e., $T_{\text{block}} = \infty$). The modeled base current for a metal-contacted control is also shown (i.e., $N_{it} = \infty$). The polysilicon is assumed to be 40% electrically active.

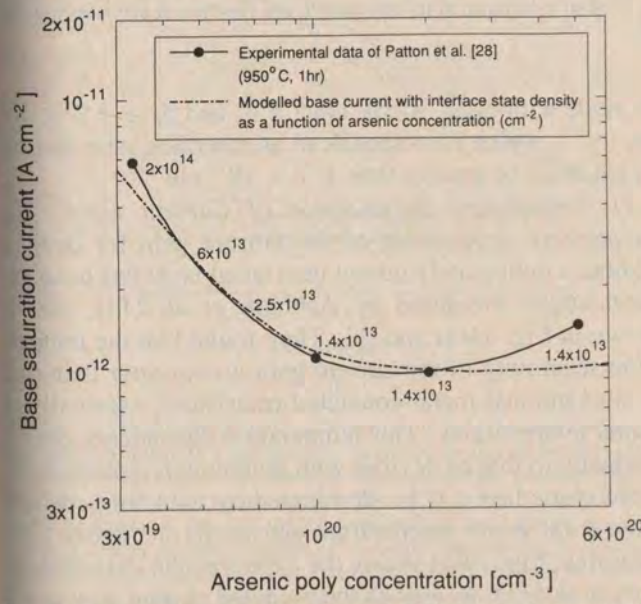

Fig. 10. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 950°C for 1 h. Also shown is the modeled base current as a function of interface state density, assuming that the interface state density varies with arsenic concentration in the polysilicon. No blocking action is assumed to occur at the interface (i.e., $T_{\text{block}} = \infty$), and the polysilicon is assumed to be 40% electrically active.

centration from 3×10^{19} to 10^{20} cm^{-3}. This behavior can be explained by the passivation of the interface states due to segregation of arsenic to the interface. There is, however, a second trend in the results of Fig. 11, which reveals that in most cases the largest interface state densities are obtained for the highest anneal temperatures. This result is consistent with the findings of Mandurah *et al.* [65], who found that arsenic segregation to grain boundaries

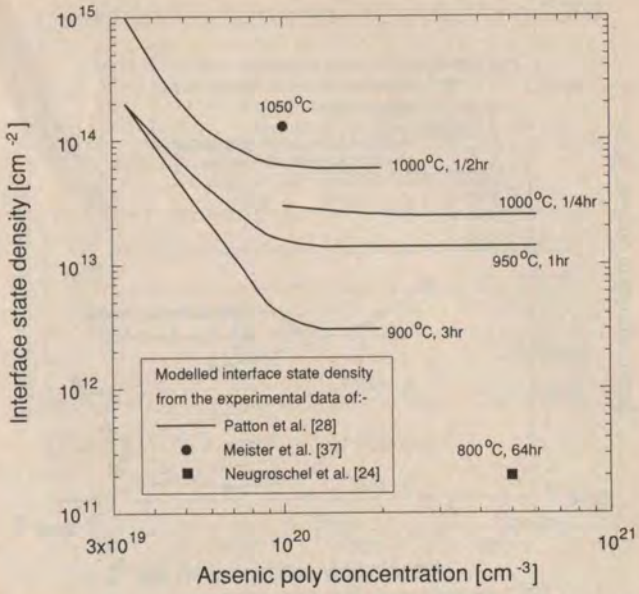

Fig. 11. Modeled interface state density as a function of arsenic concentration in the polysilicon, and polysilicon anneal, for devices with no deliberately grown interfacial oxide layers. Experimental data are from Patton *et al.* [28], Neugroschel *et al.* [24], and Meister *et al.* [37].

increases as the anneal temperature is reduced. If it is assumed that the segregation properties of grain boundaries are similar to those for the pseudo-grain boundary at the polysilicon/silicon interface, then this can explain the reduction of interface state density with anneal temperature.

Turning now to the 900°C device annealed for 1 h, the base current shows a reduction by a factor of 2.5 (for polysilicon doping concentrations of 1–2 $\times$ 10^{20} cm^{-3}) from the *extended emitter model* (Fig. 8), which suggests that a blocking mechanism at the interface is controlling the base current. Fig. 12 shows the experimental data and the modeled base current as a function of the effective recombination velocity S_p. An effective recombination velocity of 2.7×10^4 cm $\cdot$ s^{-1} can be fitted to the base current for polysilicon concentrations of 1–2 $\times$ 10^{20} cm^{-3}. Assuming that the effective recombination velocity is dominated by a blocking mechanism at the interface (i.e., $S_I = 0$ and $T_{\text{block}} << S_g$), then the *pseudo-grain boundary mobility model* can be used to model this fitted value of recombination velocity. This results in a minority hole interface mobility μ_{pgb} of 0.1 cm^2 $\cdot$ V^{-1} $\cdot$ s^{-1}, which is a reduction in hole mobility by a factor of 1500 compared with the mobility in the bulk emitter.

The *segregation model* predicts a barrier to minority carriers of around 0.9 kT (using the SIMS analysis in [28]) for the devices annealed at 1000°C, if the segregated arsenic at the interface is electrically active. Assuming a similar barrier exists for devices annealed at 900°C, then this barrier yields a recombination velocity of 7.5×10^4 cm $\cdot$ s^{-1} (no bandgap narrowing), or 8.1×10^4 cm $\cdot$ s^{-1} (with bandgap narrowing). These values of blocking recombination velocity are clearly too large to model the extracted recombination velocity, and so the *segregation model* cannot account for the reduction in base current in Fig. 12.

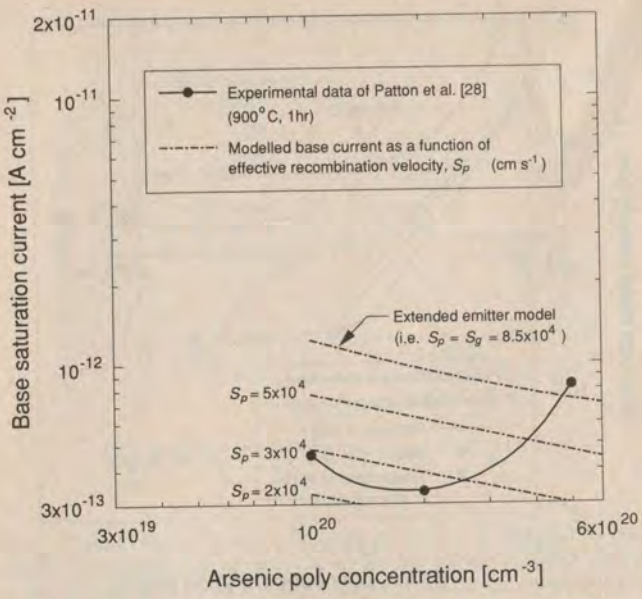

Fig. 12. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 900°C for 1 h. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the *extended emitter model* (i.e., with $T_{\text{block}} = \infty$ and $S_I = 0$). The polysilicon is assumed to be 10% electrically active.

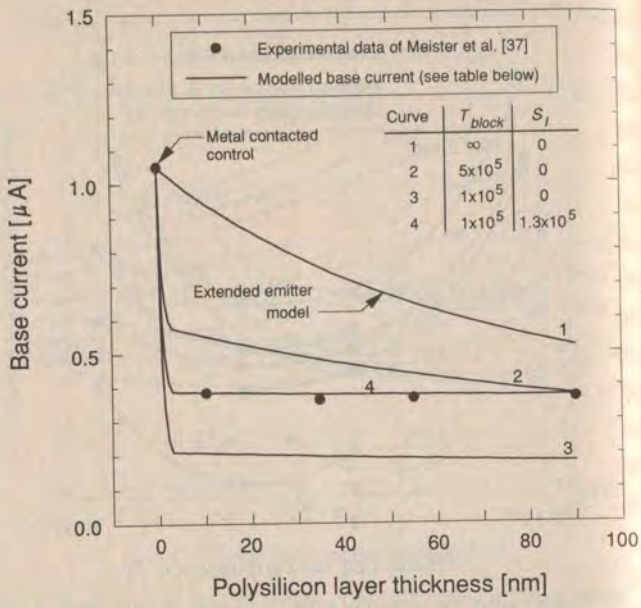

Fig. 13. Experimental data of Meister *et al.* [37] showing base current ($V_{be} = 0.66$ V and $A_E = 15.5 \times 15.5\ \mu\text{m}^2$) as a function of polysilicon thickness. Also shown is a metal-contacted control with zero polysilicon thickness. The modeled base current is shown as a function of interface state density and blocking recombination velocity. Also shown is the modeled base current using the *extended emitter model* (i.e., $T_{\text{block}} = \infty$, $S_I = 0$). S_M is taken to be equal to infinity, and S_g is a function of polysilicon thickness.

2) Polysilicon Thinning: The influence of the polysilicon layer on the current gain has been studied by several authors [28], [37] who have made measurements on polysilicon emitter transistors in which the polysilicon layer has been thinned after the emitter drive-in. The results of Meister *et al.* [37] are typical and are shown in Fig. 13. It can be seen that the base current remains constant down to a thickness of less than 10 nm, which shows that the base current is dominated by the blocking/recombination properties of the polysilicon/silicon interface, even in devices without a deliberately grown interfacial oxide layer. Also shown in Fig. 13 is the modeled base currents as a function of polysilicon thickness. Equation [1] was used to convert the modeled effective recombination velocity into a base current, and the emitter Gummel number was extracted from the metal contacted control. The device was first modeled by the *extended emitter model* (i.e., curve 1 with $T_{\text{block}} = \infty$ and $S_I = 0$), and as can be clearly seen it is impossible to model both the metal-contacted control and the variation of base current with polysilicon thickness. Decreasing T_{block} to 5×10^5 cm $\cdot$ s^{-1} (curve 2, with $S_I = 0$) enables the base current of the metal-contacted control and the polysilicon emitter device with an emitter thickness of 90 nm to be both modeled. However, for polysilicon thickness between 0 and 90 nm the model cannot be fitted to the base current. Further reductions in T_{block} to 1×10^5 cm $\cdot$ s^{-1} (curve 3), allows the constant base current with polysilicon thickness to be modeled, but at the expense of being unable to model the absolute value of base current. The only way to remedy this situation is for the interface state recombination velocity (S_I) to take values other than zero. Curve 4 in Fig. 13 shows that an excellent fit to the experimental data can be made with $T_{\text{block}} \leq 10^5$ cm $\cdot$ s^{-1}, and $S_I \geq 1.3 \times 10^5$ cm $\cdot$ s^{-1}, which corresponds to an interface state density which must be greater than 1.3×10^{14} cm^{-2}.

3) Temperature Dependence of Current Gain: The temperature dependence of the current gain for devices without a deliberately grown interfacial layer has been experimentally measured by Ashburn *et al.* [11], and is shown in Fig. 14(a) and (b). They found that the temperature sensitivity of the current gain was *greater* than that of conventional metal-contacted transistors, especially at higher temperatures. This temperature dependence differs markedly to that of devices with deliberately grown interfacial oxide layers (i.e., dominated by tunneling), which show a far *lower* temperature sensitivity at higher temperatures. Fig. 14(a) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *oxide tunneling model*. It is clear that the model cannot explain the observed temperature dependence (especially at higher temperatures), and so it can be concluded tunneling is not the dominant mechanism in devices without deliberately grown interfacial oxide layers.

Fig. 14(b) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *pseudo-grain boundary mobility model*. If it is assumed that the interface hole mobility is temperature-independent, then the temperature dependence of the current gain is controlled by the difference in the bandgap narrowing between the base and emitter, as in a conventional metal-contacted device (shown as the $n = 0$ curve in Fig. 14(b)). However, a fit cannot be made to the measured current gain, which implies that the hole mobility must be tem-

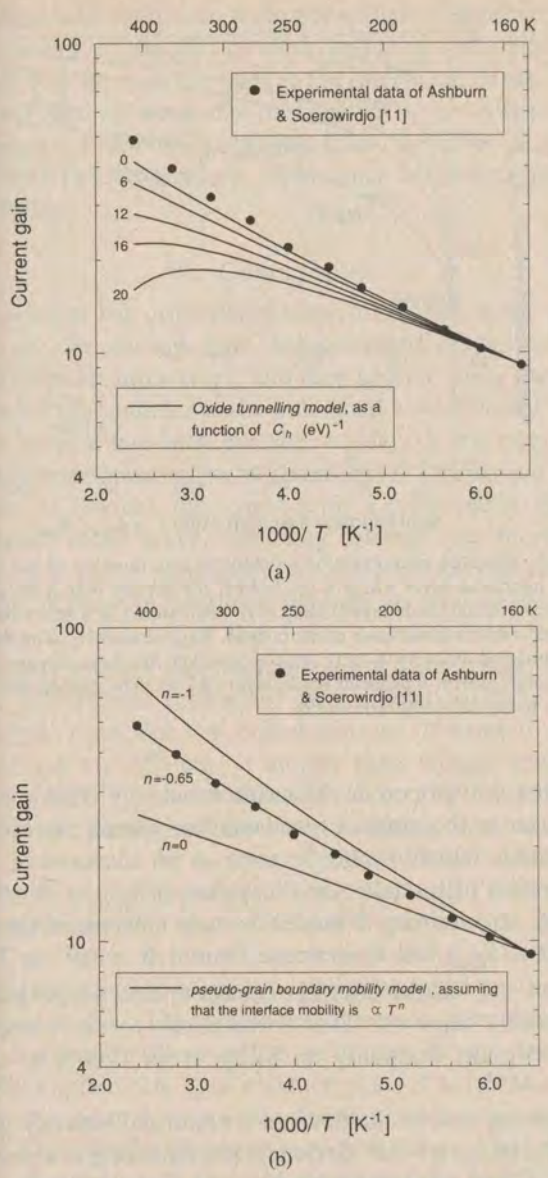

Fig. 14. (a) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the *oxide tunneling model* (assuming $S_I = 0$, and $T_{\text{block}} \ll S_g$), as a function of the parameter c_h (in (6)). (b) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the *pseudo-grain boundary mobility model* (assuming $S_I = 0$, and $T_{\text{block}} \ll S_g$). The interface mobility (μ_I) is assumed to be proportional to T^{-n}. The $n = 0$ case corresponds to the temperature dependence of a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

perature-dependent. If it is assumed that the interface hole mobility has a dependence of the form $\mu_I = AT^{-n}$ (where A is a temperature-independent constant), then an excellent fit to the experimental data can be achieved for $n = -0.65$.

4) Effect of an Interface Anneal: Wolstenholme *et al.* [10] have performed the same interface anneal experiments with HF devices as with RCA devices, and the results are shown in Fig. 15. These results show that the base current increases by a factor of 5.5 as the interface

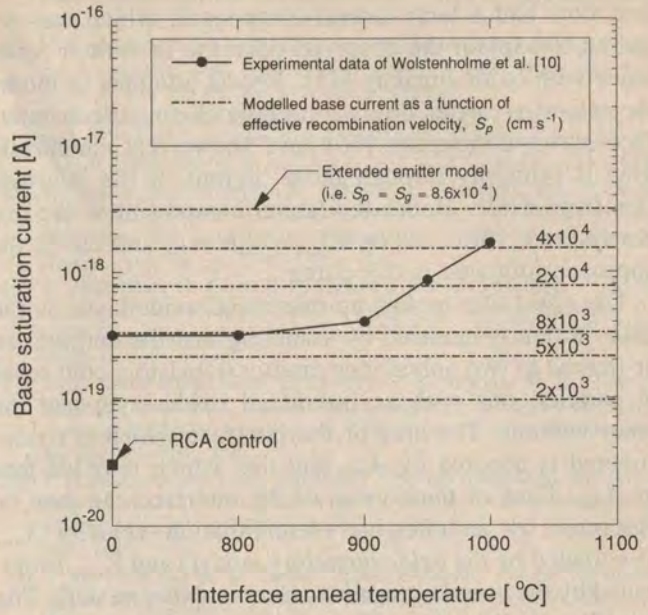

Fig. 15. Experimental data of Wolstenholme *et al.* [10] showing the base saturation current as a function of interface anneal for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the *extended emitter model* (i.e., with $T_{\text{block}} = \infty$ and $S_I = 0$).

anneal temperature is increased from 800 to 1000°C. Also shown in Fig. 15 is the modeled base current as a function of effective recombination velocity S_p, and the modeled base current using the *extended emitter model*. Transmission electron microscopy (TEM) reveals that a dip-etch in hydrofluoric acid (HF) prior to polysilicon deposition (which is designed to remove any interfacial oxide), nevertheless produces a uniform oxide of approximately 4-Å thickness. After typical anneals at 900°C, thermal stressing causes the thin HF oxide to break up, leading to a discontinuous layer varying in thickness from 0 to 8 Å, and with approximately 30% of the interface oxide-free. This compares with the 1000°C interface anneal device, in which 90% of the interface is oxide-free. These results clearly indicate that the interfacial oxide controls the base current in a HF device. It is tempting to conclude, therefore, that tunneling through the interfacial oxide is the dominant mechanism, even in HF devices. However, as already shown in Fig. 14(a), this conclusion is inconsistent with the measured temperature dependence of the current gain, which is markedly stronger for the HF devices than for the RCA devices. In order to explain this apparent inconsistency, it is necessary to consider how a discontinuous interfacial oxide can be modeled in two dimensions.

C. Modeling a Discontinuous Interfacial Layer

Very little has been published on the two-dimensional modeling of the polysilicon/silicon interface, although Hamel *et al.* [59] have simulated the majority carrier flow in a polysilicon emitter as a function of oxide breakup. Their simulations revealed that the majority-carrier cur-

rent flow had a large lateral component, which was required to explain the observed decrease in emitter resistance with oxide breakup [45]. Recent attempts to model the minority-carrier flow at the polysilicon/silicon interface in two dimensions [66] have shown that the current flow is primarily through those regions of the interface free from oxide. Hence the lateral component of the minority-carrier flow can be largely ignored, and this is the approach followed in this paper.

The effect of a broken up interfacial oxide layer on the base current is modeled by assuming that the emitter can be treated as two polysilicon emitter transistors connected in parallel, one with an interfacial oxide layer and the other without. The area of the interface which is oxide-covered is denoted by A_{ox}, and that which is oxide-free by A_{nox}. Each of these areas of the interface can then be described by an effective recombination velocity $S_{p\,ox}$ (dominated by the *oxide tunneling model*) and S_{ppgb} (dominated by the *pseudo-grain boundary mobility model*). The overall recombination velocity S_p can then be calculated as a weighted mean of these two contributions

$$S_p = S_{p\,ox}\left(1 - \frac{A_{nox}}{A_{EW}}\right) + S_{ppgb}\left(\frac{A_{nox}}{A_{EW}}\right) \tag{9}$$

where A_{EW} is the total emitter window area. Wolstenholme [57] and Gold [67] have used (9) to model the base current of polysilicon emitters as a function of the fraction of interface which is oxide-free, and the results are shown in Fig. 16 for devices with a deliberately grown interfacial oxide layer. Also shown are some of the modeled recombination velocities from the experimental results in Figs. 2 and 15. The value of $S_{p\,ox}$ used in Fig. 16 for the situation of no oxide breakup has been fitted from the base current of the RCA control device. As the oxide breaks up, high-resolution TEM has shown [10], [67] that it becomes thicker in some regions and thinner in others, with the overall oxide volume remaining constant. In order to model the tunneling current through the oxide-covered regions (the first term in (9)), $S_{p\,ox}$ has been calculated for each of the RCA devices, assuming an initial oxide thickness of 14 Å and a constant oxide volume. The result of these calculations is shown as the dashed line in Fig. 16. It is clear that, apart from the very early stages of oxide breakup ($A_{nox}/A_{EW} \leq 0.1$), the overall recombination velocity S_p is dominated by the second term in (9). This means that the majority of the hole current in a device with a broken up interfacial oxide flows through the oxide-free regions. Thus the factor of a 100 increase in base current of the RCA device with an interface anneal of 1100°C compared to the control (Fig. 2), can be partly explained as simply the increase in area of those portions of the interface which are free from oxide.

Another factor which is likely to influence S_p is the epitaxial regrowth of the polysilicon through the holes in the interfacial oxide [10], [67]. This regrowth is likely to affect the value of the pseudo-grain boundary recombination velocity S_{ppgb}, since the grain boundary moves further

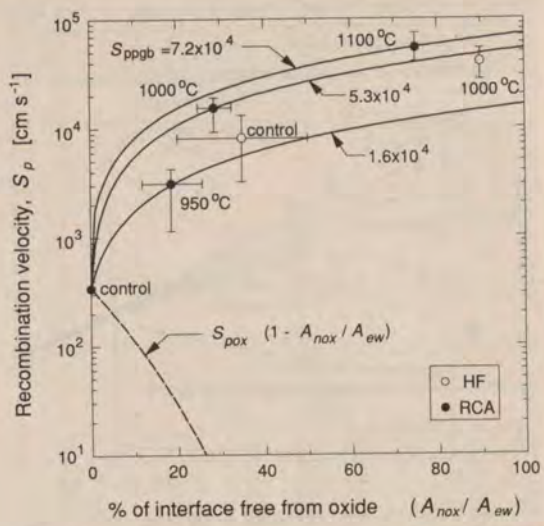

Fig. 16. Modeled recombination velocity S_p as a function of the fraction of the interfacial layer which is oxide free, for devices with a deliberately grown interfacial oxide layer (using (9)). Also shown is a selection of the modeled experimental base currents from Figs. 2 and 15. The modeled recombination velocity is only strictly relevant for those devices with a deliberately grown interfacial oxide layer (RCA). The dashed line corresponds to only the first term in (9).

into the polysilicon as the oxide breaks up. Extra recombination in the single-crystal emitter would therefore be expected, which would be seen as an increase in S_{ppgb}. The effect of a change in the value of S_{ppgb} is illustrated in Fig. 16, whereby to model the base currents of the RCA devices, S_{ppgb} has to increase from 1.6×10^4 to 7.2×10^4 cm · s^{-1} as the interface breaks up and the polysilicon epitaxially regrows. This corresponds to an increase in pseudo-grain boundary mobility from 0.043 to 0.195 cm^2 · V^{-1} · s^{-1}.

Turning now to the devices without deliberately grown interfacial layers (HF devices), the modeling is somewhat complicated since there exists no "control" device (i.e., a device with a uniform 4 Å oxide at the interface). Nevertheless, if it is assumed that the value of $S_{p\,ox}$ used in (9) is much less than S_{ppgb}, then the modeled curves in Fig. 16 are still valid for the HF devices. The difference in recombination velocity between the control HF device and the 1000°C interface anneal device is a factor of 5.5, while the difference in the oxide-free area at the interface is only a factor of 3. The fact that the base current increases more than predicted by the difference in areas of the oxide-free regions of the interface can be explained by an increase in the value of the pseudo-grain boundary recombination velocity, S_{ppgb} from 2.4×10^4 to 4.4×10^4 cm · s^{-1}. This therefore corresponds to an increase in pseudo-grain boundary mobility by a factor of only 1.8 from 0.065 to 0.12 cm^2 · V^{-1} · s^{-1}. It can therefore be seen that the increase in base current of an HF device subjected to an interfacial anneal is determined mostly by the increase in the fraction of the interface which is oxide-free, though there is also a small contribution (a factor of 1.8 compared with a factor of 3) from an increase in the pseudo-grain boundary recombination velocity, S_{ppgb} due

to the epitaxial regrowth of the polysilicon. Moreover, the base current of the HF control device is dominated by current flow through the gaps in the interfacial oxide, with the result that the dominant mechanism is the reduced minority-carrier mobility at the interface, which is in agreement with the temperature dependence of current gain in Fig. 14(b).

VI. Conclusions

This paper has critically reviewed theories in the literature on the current gain enhancement of polysilicon emitter bipolar transistors, and then applied these theories in a consistent manner to the published experimental data. In this way, it has been possible to identify the dominant physical mechanisms for a given set of fabrication conditions. In devices fabricated with a deliberately grown interfacial oxide layer, tunneling through the interfacial oxide layer can explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. In devices fabricated without a deliberately grown interfacial oxide layer, two distinct regions of device behavior have been identified. First, for low concentrations of arsenic in the polysilicon ($<10^{20}$ cm^{-3}) and/or high anneal temperatures ($>1000°$C), recombination of carriers via interface states at the polysilicon interface dominates the base current. This results in a current gain which is lower than that for an extended emitter device. Secondly, for arsenic concentrations of $1\text{–}2 \times 10^{20}$ cm^{-3} and anneals around 900°C (as used in many commercial processes), the increased segregation of arsenic to the interface pacifies the interface states. These devices exhibit a gain enhancement compared with an extended emitter device. In order to fully explain this gain enhancement, it is necessary to model the discontinuous interfacial oxide in two dimensions. The use of a simple pseudo-two-dimensional model shows that the oxide covered regions of the interface are opaque to minority carriers, so that most of the current flows through the gaps in the oxide. The base current is therefore determined primarily by the fraction of the interface which is oxide-free, and hence is very sensitive to the detailed structure of the interfacial oxide. The dominant base current mechanism is thus reduced minority-carrier mobility in the pseudo-grain boundary at the polysilicon/silicon interface.

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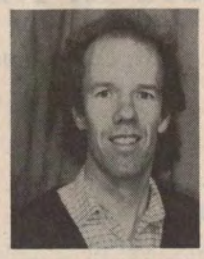

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Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment

Ian R. C. Post, *Member, IEEE*, Peter Ashburn, *Member, IEEE*, and Graham R. Wolstenholme, *Member, IEEE*

***Abstract*—A critical review is presented of the theories proposed in the literature to explain the current gain enhancement of polysilicon emitter bipolar transistors. From these theories a simplified analytical formulation is chosen which models the blocking properties of the interface, including tunneling through the interfacial oxide, reduced grain boundary mobility at the polysilicon/silicon interface, and the potential barrier created by segregated dopant, which can all give rise to an enhanced current gain. Also modeled are the mechanisms which limit the extent of any gain enhancement, such as recombination in the single-crystal emitter, in the bulk of the polysilicon, and at the polysilicon/silicon interface. This model is then applied in an original manner to a selection of experimental data in an effort to identify the dominant current gain mechanisms in polysilicon emitter transistors as a function of a given set of fabrication conditions.**

For devices with a deliberately grown oxide layer at the polysilicon/silicon interface, an *oxide tunneling model* can fully explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. For devices without a deliberately grown interfacial oxide layer, two distinct types of behavior are observed. First, for low concentrations of arsenic in the polysilicon ($< 10^{20}$ cm^{-3}) and/or high anneal temperatures ($\geq 1000°$C), recombination of carriers via interface states at the polysilicon/silicon interface dominates the base current. This results in a current gain which is degraded below that of an extended emitter device. Secondly, for higher concentrations of arsenic in the polysilicon (1–2×10^{20} cm^{-3}) and anneal temperatures around 900°C, the increased segragation of arsenic to the grain boundaries pacifies the interface states, resulting in an enhancement of gain compared to that for an extended emitter device. Pseudo-two-dimensional modeling of the discontinuous interfacial layer in these devices is undertaken, which shows that the base current flows primarily through those areas of the interface that are free from oxide. The base current is therefore controlled by the fraction of the interface which is oxide-free.

I. Introduction

SINCE the discovery of polysilicon emitters in the 1970's [1]–[3], they have moved from being a laboratory curiosity to become a vital part of many high-speed bipolar [4], [5] and BiCMOS [6]–[8] production processes. The main reason for their success is that they provide a simple means of achieving the reductions in junction depth which are necessary when lateral device geometries are scaled. This co-ordinated scaling of lateral and vertical dimensions is important in order to provide an emitter structure in which the peripheral component of the emitter/base capacitance is maintained at a reasonable level. An important feature of polysilicon emitter technology is that reduced junction depths can be obtained without the degradation in gain which is obtained with conventional ion-implanted emitters [9]. On the contrary, an improvement in gain can be obtained, ranging from a factor of 3 [9] to 30 [10], with the size of the improvement depending upon the fabrication conditions used to produce the polysilicon emitter [11].

In spite of their widespread application, there is still considerable controversy over the precise mechanisms which control the current gain of a polysilicon emitter. Three physical mechanisms have been proposed to explain the improved gains of polysilicon emitter transistors. The first is termed the *"oxide tunneling model"* [3], [12] and explains the improved gains by tunneling through a thin oxide layer at the polysilicon/silicon interface. This model predicts not only a reduction in base current, and hence an improved gain, but also an increase in emitter resistance. The second is termed the *"grain boundary mobility model"* [9], [13], [14] and explains the improved gain by reduced mobility at the grain boundaries in the polysilicon and at the pseudo-grain boundary at the polysilicon/silicon interface. This model predicts a reduction in base current when the density of interface states at the grain boundaries is small, but an increase when the interface state density is high [14]. The third is termed the *"segregation model"* [15]–[17] and explains the improved gain by the presence of a potential barrier at the polysilicon/silicon interface due to the segregation of dopant. This model predicts a reduction in base current, with the amount of reduction depending upon the concentration of segregated arsenic at the interface. However, the *"segregation model"* predicts no change in emitter resistance. These three mechanisms can all be described as blocking mechanisms, since they are capable of giving an enhancement in gain compared with comparable con-

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ventional metal-contacted bipolar transistors. In order to fully explain the behavior of polysilicon emitters, it is necessary to also consider mechanisms which limit the extent of the gain improvement. These are mainly recombination mechanisms and include recombination at grain boundaries [14], recombination at the polysilicon/silicon interface [14], and recombination in the single-crystal emitter [18].

Since the publication of the above theoretical work, a large amount of experimental data has been gathered [19], which has greatly extended the understanding of the physical structure of the polysilicon emitter. High-resolution electron microscopy has been extensively used to study the polysilicon/silicon interface in detail, and has shown that a thin native oxide layer is invariably present [20]. The structure of the interfacial oxide depends critically upon the surface treatment carried out prior to polysilicon deposition [10], [20], with oxidizing chemical treatments giving a continuous oxide of approximately 14-Å thickness, and HF treatments giving a discontinuous oxide ranging in thickness from zero to around 8 Å. In oxide-free regions of the interface, epitaxial regrowth of the polysilicon occurs, extending typically a few hundred Angstroms into the polysilicon. In extreme cases, complete epitaxial regrowth of the polysilicon can occur [21] leading to a device with an extended single-crystal emitter [22]. The interfacial oxide structure also depends critically on annealing schedules [10], with oxide breakup being more likely for higher temperatures and thinner oxides.

Polysilicon emitter transistors and a variety of test structures have been fabricated in order to assess the importance of key processing parameters on the base current [3], [9]–[11], [23]–[41] and emitter resistance [29], [30], [42]–[48], and to obtain an insight into the mechanisms which control the device behavior. Specifically, the influence of the interface treatment [11], [45], the annealing temperature [10], the polysilicon thickness [28], [31], [37], dopant segregation [24], [28], and hydrogen passivation [28], [35] have all been studied. Many of the processing parameters have been shown to have a large influence on the device behavior, giving rise to changes in current gain by more than an order of magnitude.

In spite of this large amount of experimental and theoretical work, there is still considerable controversy over the precise mechanisms which control the base current of a polysilicon emitter transistor. Some of this controversy arises because of the different types of polysilicon emitter transistors which have been studied and the different fabrication conditions used to produce the devices. Another cause is the large number of competing mechanisms which can occur at the polysilicon/silicon interface and the resulting complexity of the device modeling. This paper will address these problems by first reviewing the competing theories for current gain enhancement, which will lead to a simple unified model for the base current of a polysilicon emitter transistor. The wide range of experimental data on polysilicon emitters will then be briefly reviewed, and then re-assessed using this unified theory in an original manner. This approach will allow the identification of the mechanisms which control the current gain for a given set of fabrication conditions.

II. Types of Polysilicon Emitter

Several types of polysilicon emitter have been studied in the literature, as illustrated in Fig. 1. In the first type (Fig. 1(a)), the n^+ dopant is confined to the polysilicon so that the metallurgical emitter/base junction coincides with the polysilicon/silicon interface. This structure is analogous to the MIS tunnel device [49], [50], and is therefore referred to here as a SIS emitter. Very high current gains have been reported for this structure [51]–[53], although the base characteristic is very nonideal, and is often accompanied by a "kink" at high emitter/base voltages. These disadvantages, and its poor current carrying capability [54], make it unsuitable for realizing high-speed circuits. This structure will therefore not be discussed in this paper, although, it should be pointed out that SIS behavior can be obtained in polysilicon emitters if the emitter/base junction is too shallow.

The second type of structure (Fig. 1(b)) is a polysilicon emitter in which the n^- dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitter/base junction. The emitter/base depletion region therefore resides entirely in the single-crystal silicon, which leads directly to very ideal base characteristics. In order to obtain enhanced gain, the emitter/base junction depth must be shallower than the hole diffusion length in the single-crystal emitter, otherwise the gain is dominated by recombination in the single-crystal emitter. The crucial part of this structure is the polysilicon/silicon interface which can have a large effect on the base current of the transistor.

The third type of structure illustrated (Fig. 1(c)) is an extended emitter in which the n^+ polysilicon is replaced by single-crystal silicon. This can arise in practice if complete epitaxial regrowth of the polysilicon is induced during the emitter drive-in [21], [22]. The current gain is therefore unaffected by the interface, and hence it behaves like a conventional bipolar transistor. For the purposes of this paper this is a useful structure to consider, since a comparison of the gain of a polysilicon emitter with that of an identical extended emitter gives a measure of the gain enhancement or reduction resulting from the presence of the polysilicon/silicon interface.

Finally, the last structure shown (Fig. 1(d)) is that of a conventional metal-contacted emitter. In this type of device the emitter is formed by direct ion implantation into the silicon substrate, followed by a high-temperature anneal which is designed to activate the emitter dopant. When the emitter junction depth is scaled in such a device a reduction of current gain results because the emitter is transparent to the injected minority-carrier current [9]. This severe disadvantage precludes the use of metal-contacted emitters in high-speed bipolar processes.

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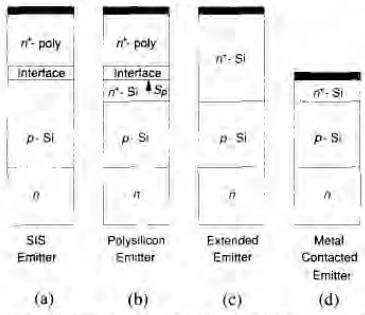

Fig. 1. Schematic diagrams of (a) an SIS emitter, (b) a polysilicon emitter, (c) an extended emitter, and (d) a metal contacted emitter.

III. Effective Recombination Velocity

In this paper the polysilicon/silicon interface is modeled by using an effective recombination velocity S_p, which defines the recombination velocity at the lower side of the polysilicon/silicon interface, as shown in Fig. 1(b). In order to relate the effective recombination velocity to the base current, it is necessary to model recombination in the single-crystal emitter region. For a shallow emitter which is quasi-transparent, the base current can be modeled using the approach of del Alamo *et al.* [18]

$$J_{BO} = \frac{qn_{io}^2}{G_{\text{eff}}(W_E) + N_{D\text{eff}}(W_E)/S_p} \cdot \left[1 + \int_0^{W_E} \frac{G_{\text{eff}}(W_E) - G_{\text{eff}}(x)}{\tau_p(x) N_{D\text{eff}}(x)}\, dx + \frac{N_{D\text{eff}}(W_E)}{S_p} \int_0^{W_E} \frac{dx}{\tau_p(x) N_{D\text{eff}}(x)}\right] \tag{1}$$

where G_{eff} is the effective emitter Gummel number, $N_{D\text{eff}}$ is the "effective" doping concentration in the emitter, τ_p is the hole lifetime in the emitter, while $x = 0$ is defined to be the edge of the emitter/base depletion region, and $x = W_E$ is the position of the polysilicon/silicon interface.

The term is brackets in (1) represents a first-order correction for recombination in the single-crystal emitter, although, for the vast majority of devices analyzed in this paper recombination in the single-crystal emitter is negligible. The only notable exception to this is for devices with thick interfacial oxide layers. In order to calculate predicted values of base current to compare with reported experimental values in the literature, (1) is used together with measured emitter profiles, where available. In cases where the emitter profile is not given, a Gaussian profile is assumed in the single-crystal emitter, the Gaussian being constructed using estimates of the emitter/base junction depth and the doping concentration at the interface.

IV. Current Gain Theories

The general model to be used in this study to calculate the effective recombination velocity S_p follows from the unified model of Yu *et al.* [14], and is shown schematically in Fig. 1(b). It is assumed that the polysilicon layer consists of only one crystalline grain separated from the monosilicon substrate by an interfacial region of finite thickness, which will be described in detail further on. A density of interface traps is also assumed to exist at the two interfaces between the interface region and the polysilicon grain and the monosilicon substrate.

The effective recombination velocity S_p can be expressed as [14]

$$S_p = S_I + \left(\frac{1}{T_{\text{block}}} + \frac{1}{S_I + S_g}\right)^{-1} \tag{2}$$

where S_I models the recombination of minority carriers via traps at the interface, and is given by

$$S_I = \tfrac{1}{2} N_{it} c_p v_{\text{th}} \tag{3}$$

and N_{it} is the total density of interface traps per unit area, c_p is the capture cross section, and v_{th} is the thermal velocity. The factor of $1/2$ arises in (3) from interface traps being equally distributed between the upper and lower sides of the interface.

The parameter S_g describes the recombination of minority carriers in the bulk of the polysilicon grain, and is given by [14]

$$S_g = a_g - \frac{b_g^2}{a_g + S_M} \tag{4}$$

where

$$a_g = \frac{D_g}{L_g} \coth\left(\frac{W_p}{L_g}\right)$$
$$b_g = \frac{D_g}{L_g} \operatorname{csch}\left(\frac{W_p}{L_g}\right) \tag{5}$$

D_g and L_g are the diffusivity and diffusion length, respectively, of minority carriers in the grain, S_M is the effective recombination velocity at the metal contact, and W_p is the polysilicon thickness.

The term T_{block} in (2) describes the blocking action of the polysilicon/silicon interface, and the expression used to calculate T_{block} is determined by the dominating mechanism. The three competing mechanisms are tunneling, reduced mobility in the pseudo-grain boundary at the interface, and thermionic emission over a segregation barrier. These will now each be considered in turn.

The *oxide tunneling model* was first proposed by de Graaff *et al.* [3], and later modified by Eltoukhy *et al.* [12]. The model assumes that a thin tunneling oxide is present at the polysilicon/silicon interface. Holes injected from the base into the emitter are forced to tunnel through the interfacial oxide layer, thereby blocking minority carrier flow into the polysilicon and hence producing a reduction in base current. The expression that will be used for T_{block} in the *oxide tunneling model* is summarized in Table I. Similarly, the majority-carrier electrons which flow from the polysilicon into the silicon must also tunnel

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TABLE I
ANALYTICAL EXPRESSIONS USED FOR T_{block} IN THE THREE BLOCKING MECHANISMS IN THIS STUDY

($b_h = 4\pi\delta/h\sqrt{2m_i^*\chi_h}$, $c_h = 2\pi\delta/h\sqrt{2m_i^*/\chi_h}$, χ_h is the barrier height to holes, m_p^* is the effective mass of holes in silicon, m_i^* is the effective mass of holes in the oxide, δ is the interfacial oxide thickness, μ_{pgb} is the minority-carrier mobility in the pseudo-grain boundary, Δ is the thickness of the pseudo-grain boundary, N_E is the electrically active doping density in the emitter, and N_{Int} is the electrically active doping density of segregated dopant at the interface.)

Blocking Model	Expression Used for T_{block}	
Oxide tunneling model	$T_{\text{block}} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{\exp(-b_h)}{1 - c_h kT}$	(6)
Pseudo grain-boundary mobility model	$T_{\text{block}} = \frac{kT}{q} \frac{\mu_{pgb}}{\Delta}$	(7)
Segregation model	$T_{\text{block}} = \sqrt{\frac{kT}{2\pi m_p^*}} \frac{N_E}{N_{\text{Int}}}$	(8)

through the oxide. This limits the maximum current carrying capability of the device, since it gives rise to a series emitter resistance [43]–[45].

The *grain boundary mobility model* was first proposed by Ning *et al.* [9], who used it to explain electrical results obtained on transistors with conventional implanted emitters on top of which a layer of arsenic *in situ* doped polysilicon was deposited. A gain enhancement of a factor of 3 was achieved for the polysilicon emitters, compared to conventional metal-contacted emitters, which was attributed to a lower minority-carrier mobility in the polysilicon, when compared to single-crystal silicon. Eltoukhy *et al.* [13] extended the above simple two-region model to take into account the effect of grain boundaries on the minority carriers, which they assumed were infinitely thin, and characterized by a large concentration of interface states. Alternatively, Yu *et al.* [14] modeled the grain boundaries by assuming that they have a finite thickness, in which the minority-carrier mobility is reduced with respect to that in the bulk of the grain. Recombination is assumed to occur only at the interface between the grain and grain boundary, but not actually in the grain boundary. Furthermore, recombination at the polysilicon/silicon interface was also modeled. The grain boundaries can effect minority-carrier transport in two ways. First, if the density of interface states is large enough ($> 10^{14}$ cm^{-2}) then they will act as efficient recombination centers, and no improvement in current gain will result over that for a metal-contacted emitter. However, for low densities of interface states ($\leq 10^{12}$ cm^{-2}), recombination at the grain boundary interface becomes negligible, and the minority-carrier transport is dominated by the reduced carrier mobility in the grain boundaries. This has the overall effect of lowering the minority-carrier mobility in the polysilicon layer, and so reducing the base current.

In this paper the polysilicon layer is assumed to consist of only one crystalline grain, although the disordered interfacial region will be treated as a pseudo-grain boundary with a corresponding reduction in carrier mobility. This model will be termed the *"pseudo-grain boundary mobility model,"* and the expression used for the blocking recombination velocity T_{block} is summarized in Table I. A value for the pseudo-grain boundary thickness Δ will be chosen as 7 Å [55], which is consistent with the approximate thickness of a grain boundary in the bulk of the polysilicon. Typical values for the minority-carrier mobility in the pseudo-grain boundary μ_{pgb} can be several orders of magnitude less than the hole mobility in single-crystal silicon [56].

The *segregation model* was proposed by Ng *et al.* [15] to explain the observation that the current gain of polysilicon emitter transistors is dependent upon the amount of arsenic which segregates to the interface [24], [28]. Typically, the concentration of arsenic at the polysilicon/silicon interface can be a factor of two or three larger than the concentration of arsenic in the bulk of the grains. Ng *et al.* [15] argued that if the segregated arsenic is electrically active then this could form a low–high–low barrier, although the model will not predict any increase in emitter resistance. The expression that will be used for T_{block} in the *segregation model* is summarized in Table I [15].

It should be pointed out that the doping densities in (8) (see Table I) should strictly be effective doping densities, which include the effects of bandgap narrowing [57]. Since effective doping densities tend to saturate to a constant value as the doping concentration increases [58], this implies that the segregation barrier will be smaller than predicted in [15]. For example, for this mechanism to dominate the base current, the barrier created by the segregated dopant must be greater than about $2kT$. For a typical emitter doping concentration of 10^{20} cm^{-3}, this means that the segregated doping concentration must be greater than around 8×10^{20} cm^{-3} if the electrically active arsenic concentration is used, or greater than 10^{23}–10^{24} cm^{-3} if the effective doping concentration is used.

In order to obtain accurate predictions of effective recombination velocity and base current from doping profiles, it is necessary to take into account heavy doping effects, which influence parameters such as hole lifetime τ_p, hole mobility μ_p, and bandgap narrowing ΔE_g^{app}. Values for these parameters, as a function of doping, are taken from the work of del Alamo *et al.* [58]. Finally, it is necessary to assume values for some parameters for which measured values are not available. These are summarized in Table II, and the given values have been used throughout this paper unless otherwise stated.

V. EXPERIMENTAL RESULTS

Over the past ten years or so, a considerable amount of experimental results on polysilicon emitter transistors have been published in the literature [19]. In this section, approximately eight or so key papers have been chosen which are representative of a broad cross section of important experimental results. The results of these papers will be quoted in the form of raw experimental data (for

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TABLE II
PARAMETER VALUES USED IN THIS STUDY

Parameter	Value	Reference
Hole effective mass in silicon (m_p^*)	$0.66m_o$	[12]
Hole effective mass in the interfacial oxide layer (m_i^*)	$0.42m_o$	[12]
Interface trap capture cross section × thermal velocity ($c_p v_{th}$)	2×10^{-9} cm$^3 \cdot$ s^{-1}	[54]
Grain boundary thickness (Δ)	7 Å	[55]
Recombination velocity at metal contact (S_M)	10^6 cm $\cdot$ s^{-1}	[14]

example, measured current densities and resistances, etc.), and then *all* subsequent modeling will be performed in an original manner using the simplified analytical equations outlined in Section IV. This will allow a consistent comparison to be made between the predictions of the three blocking mechanisms and the reported experimental results.

A. Devices with Interfacial Oxides

1) Effect of an Interface Anneal: The analysis will begin by considering experimental results from devices with an interfacial oxide layer, which is generally grown using an oxidizing chemical treatment. It has been well documented in the literature that such an interface treatment gives a significant improvement in the current gain. For example, Ashburn *et al.* [11] have shown that devices given an RCA clean prior to polysilicon deposition had gains five times higher than those given an HF etch. A more detailed characterization of the influence of the interfacial oxide on the current gain was carried out by Wolstenholme *et al.* [10]. In this experiment, an interface anneal was carried out after polysilicon deposition, but prior to emitter implant, to thermally stress the interfacial oxide. In this way, a range of interfacial oxide structures was obtained without significantly altering the emitter and base doping profiles. The results are shown in Fig. 2 for devices given an RCA clean prior to polysilicon deposition. It is evident that a factor of 100 increase in base current is obtained as the temperature of the interface anneal is increased from 800 to 1100°C. These electrical results were correlated with high-resolution TEM observations of the polysilicon/silicon interface which showed that an interfacial oxide was present, which broke up by increasing amounts as the interface anneal temperature was increased.

High-resolution TEM showed that for interface anneal temperatures of 900°C or below, the interfacial oxide was continuous and uniform, with a thickness of 14 ± 2 Å. It is therefore possible to apply the *oxide tunneling model* unambiguously to these results. Fig. 2 shows the modeled values of base current (using (6) of Table I and the parameters in Table II) for different values of oxide barrier height, assuming that the devices are tunneling-dominated (i.e., $S_I = 0$ and $T_{\text{block}} << S_g$). It is evident that these devices can be modeled by an oxide barrier height

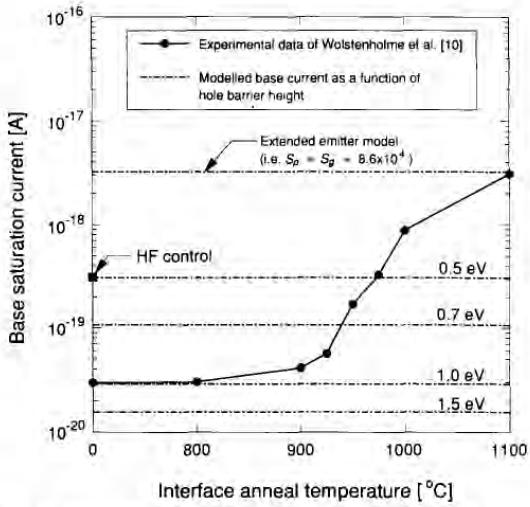

Fig. 2. Experimental data of Wolstenholme *et al.* [10] showing base saturation current as a function of interface anneal for devices with a deliberately grown interfacial oxide layer. The base current has been modeled by assuming that the dominant blocking mechanism is tunneling through the interfacial oxide layer (i.e., *oxide tunneling model* with $\delta = 14$ Å, and $S_I = 0$). Also shown is the modeled base current using the *extended emitter model* ($T_{\text{block}} = \infty$, and $S_I = 0$).

of 1.0 eV. Also modeled in Fig. 2 is the base current of an extended emitter device, in which no blocking or recombination at the interface is assumed to occur (i.e., $T_{\text{block}} = \infty$ and $S_I = 0$). As can be seen, a good fit to the 1100°C interface anneal device is achieved, which implies that the interface has no effect on the base current of this device. This conclusion is consistent with the TEM analysis, which showed that the interfacial oxide had completely "balled-up," such that 97% of the interface was oxide-free. These experimental results show that the interfacial oxide plays a doiminant role in controlling the current gain of polysilicon emitter transistors with deliberately grown interfacial oxide layers.

Rutherford backscattering (RBS) analysis has been used by Wolstenholme [57] to investigate the distribution of arsenic at the interface for the devices reported in Fig. 2. The results of this analysis are shown in Fig. 3, and indicate that the concentration of arsenic at the polysilicon/silicon interface remains unchanged for interface anneals up to a temperature of 1000°C. Applying the *segregation model* to the barriers produced in Fig. 3 for the RCA control device, produces a blocking recombination velocity of either 7.9×10^4 cm $\cdot$ s^{-1} (no bandgap narrowing), or 1.2×10^6 cm $\cdot$ s^{-1} (with bandgap narrowing). This compares with an extracted T_{block} of 3.2×10^2 cm $\cdot$ s^{-1} for the control device in Fig. 2, which therefore implies that the *segregation model* cannot explain the experimental results in either Figs. 2 or 3.

2) Temperature Dependence of Current Gain: Further evidence supporting the *oxide tunneling model* is obtained from measurements of the temperature dependence of cur-

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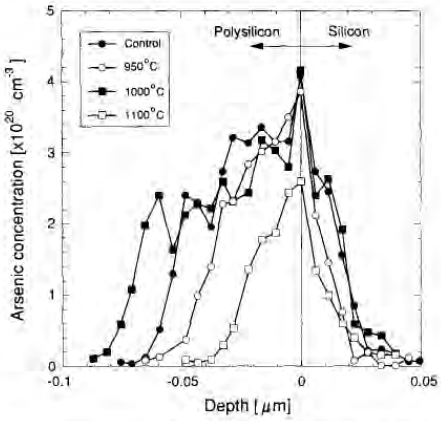

Fig. 3. Experimental data of Wolstenholme [57] showing Rutherford backscattering (RBS) arsenic profiles of the polysilicon/silicon interface for devices with a deliberately grown interfacial layer, subjected to various interface anneals.

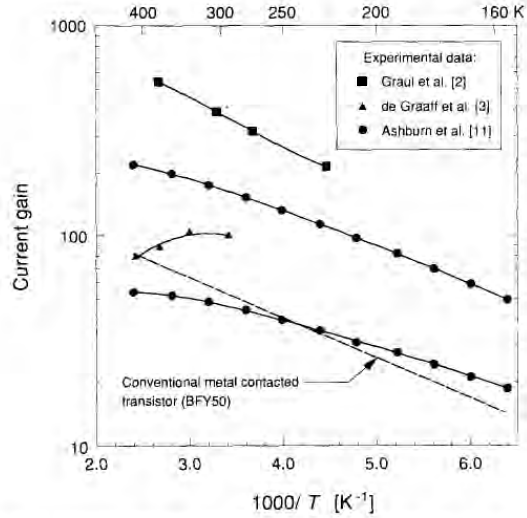

Fig. 4. Experimental data of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices with a deliberately grown interfacial oxide layer. It can be clearly seen that the temperature dependence of current gain is less than that for a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

rent gain. Several authors [2], [3], [11] have reported that polysilicon emitter transistors with a chemically grown interfacial oxide have a gain which varies less strongly with temperature than observed for conventional metal-contacted transistors. Fig. 4 shows the current gain, as a function of inverse temperature, from the work of Graul *et al.* [2], de Graaff *et al.* [3], and Ashburn *et al.* [11]. Also shown in Fig. 4 is the temperature dependence of current gain for a conventional metal-contacted transistor (whereby the temperature dependence of the current gain is determined by the difference in bandgap narrowing in the base and emitter). It can be seen, especially for temperatures above 300 K, that the current gain becomes less sensitive to temperature than in conventional metal-contacted transistors. In fact, the results from de Graaff *et al.* [3] even show a negative temperature coefficient. Ashburn *et al.* [11] modeled the temperature dependence of gain, and showed that the *oxide tunneling model* could explain the observed results for the whole temperature range in Fig. 4.

3) Emitter Resistance: The presence of a deliberately grown oxide layer at the polysilicon/silicon interface has been shown to block majority-carrier flow, leading to an increase in emitter resistance [43]–[45]. Measurements of specific interfacial resistivity for devices with deliberately grown interfacial oxide layers typically range from 200 to 500 $\Omega \cdot \mu m^2$ [43]–[45]. This compares with generally far lower values of 10 to 200 $\Omega \cdot \mu m^2$ [29], [43], [45] for devices without deliberately grown interfacial oxide layers. By applying the *oxide tunneling model* to the devices with interfacial layers, assuming an average oxide thickness of 14 Å [10] and an electrically active polysilicon doping level of 5×10^{19} cm^{-3} [10], implies a barrier height to electrons of around 0.3 eV (using the analytical expression for emitter resistance derived in [30]). Comparing this value with the barrier height for holes, which is around 1 eV (Fig. 2), it can be clearly seen that there exists an asymmetry in oxide barrier heights for electrons and holes.

Wolstenholme *et al.* [45] have performed experiments on the "balling-up" of the interfacial oxide from interface anneals, and then correlated this with measurements of emitter resistance, as shown in Fig. 5. Also shown in Fig. 5 are the base current data from Fig. 2. Some important differences can be seen in the variation of the base current and emitter resistance with interface anneal temperature. Most notable is a substantial reduction in emitter resistance for the device given a 900°C interface anneal, compared to the control device, even though the TEM analysis showed that the interfacial layer for both devices was continuous and unbroken. Two-dimensional modeling by Hamel *et al.* [59], as shown in Fig. 6, has recently shown that this result can be explained if a limited number of widely spaced small gaps in the oxide layer are produced in the 900°C interface anneal, even though nearly 99% of the oxide remains continuous (and so therefore these gaps would be difficult to observe by TEM). Since a large proportion of the interface remains intact, a reduction in base current is still obtained, as observed in Fig. 2. These results show that it is possible to produce a device with both a high gain and a low emitter resistance [60].

Measurement and modeling of the temperature dependence of emitter resistance for devices with deliberately grown interfacial oxide layers has been conducted by Yung *et al.* [46]. They found that the *oxide tunneling model* could fit the observed temperature dependence, although the shape of the tunneling barrier had to be

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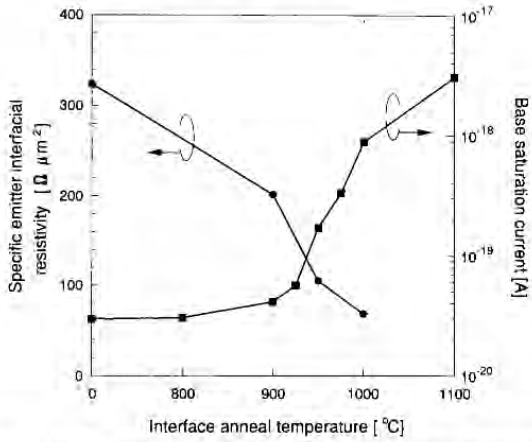

Fig. 5. Experimental data of Wolstenholme *et al.* [10], [45] showing the specific emitter resistivity and base saturation current as a function of interface anneal temperature for devices with a deliberately grown interfacial oxide layer.

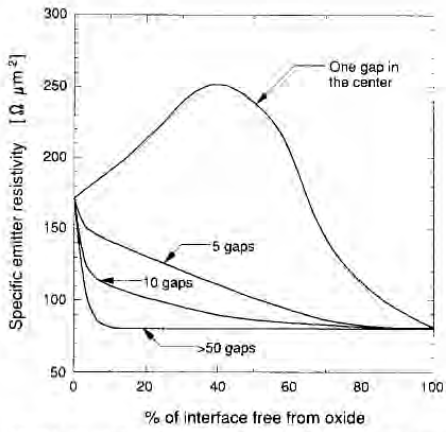

Fig. 6. Modeled specific emitter resistivity as a function of the percentage of the interface which is oxide-free for a device with a HF interfacial treatment, from the work of Hamel *et al.* [59]. It can be clearly seen that not only the amount of oxide, but its distribution along the interface can dramatically effect the emitter resistance.

changed from rectangular to triangular. Yung *et al.* [46] speculated that dopant pileup at the interface was the physical cause of this change in barrier shape.

4) p-n-p Polysilicon Emitter Transistors: As an aid to understanding the physics of polysilicon emitter transistors it is worthwhile here to examine the experimental results from p-n-p polysilicon emitter transistors [61]–[63]. The extracted values of barrier height (χ_h = 1.0 eV and χ_e = 0.3 eV) from measurements on n-p-n polysilicon emitter transistors imply that p-n-p transistors should have a high emitter resistance and a small gain improvement. In practice, however, this is found not to be the case. Reported values of current gains for p-n-p polysilicon emitter transistors with deliberately grown interfacial oxide layers, are between a factor of 2 [61] and 10 [63] times higher than for devices without a deliberately grown interfacial layer. Furthermore, the emitter resistance of p-n-p polysilicon emitter transistors, with an interfacial oxide layer, are only approximately a factor of 2–3 [61]–[63] higher than for the corresponding devices without a deliberately grown interfacial layer. If the *oxide tunneling model* is used to extract oxide barrier heights to holes and electrons, the values of barrier height of χ_h = 0.3 eV and χ_e = 1.0 eV [63] are seen to be inconsistent with those obtained from measurments on n-p-n transistors. Further work is therefore needed on the *oxide tunneling model* to explain this discrepancy.

B. Devices Without an Interfacial Oxide Layer

For commercial applications, devices without a deliberately grown interfacial oxide layer are generally preferred because of the emitter resistance problem described above. However, it should be pointed out that an interfacial layer is invariably present at the polysilicon/silicon interface, even in devices given an HF etch prior to polysilicon deposition [10].

1) Segregation of Dopant to the Interface: Confirmation of the role of the interface in controlling the gain comes from the work of Neugroschel *et al.* [24], who have fabricated bilayer polysilicon diodes by first depositing undoped polysilicon and then capping the device with *in situ* arsenic-doped polysilicon. Drive-in conditions were carefully chosen so that the amount of arsenic segregated to the polysilicon/silicon interface could be varied. A long low-temperature drive-in (e.g., 64 h at 800°C) was used to preferentially diffuse the arsenic along the grain boundaries, and dope the grain boundaries and interface to a concentration of around 5×10^{20} cm^{-3}. However, the temperature of the drive-in was not high enough to diffuse arsenic into the bulk of the grains [64], which remained at a low concentration of $\leq 10^{18}$ cm^{-3}. This device was then compared to both an unannealed bilayer device (with a low arsenic concentration of $\leq 10^{18}$ cm^{-3} in the grains and at the interface), and to a control device with a single *in situ* doped polysilicon layer (with an arsenic concentration of $\sim 10^{21}$ cm^{-3} at the interface and around 5×10^{20} cm^{-3} in the grains).

Fig. 7 shows the current–voltage characteristics for the annealed and unannealed bilayer devices, and the *in situ* doped monolayer polysilicon control device. Also shown is the characteristic for a metal-contacted control with no polysilicon layer. It can be seen from Fig. 7 that the current from the annealed bilayer device is nearly identical to the monolayer control. However, these two devices have *different* doping concentrations in the bulk polysilicon ($\sim 10^{18}$ cm^{-3} and 5×10^{20} cm^{-3}, respectively), but have *similar* concentrations of arsenic at the polysilicon/silicon interface (5×10^{20}–10^{21} cm^{-3}). It can thus be concluded that the *concentration* of arsenic at the polysilicon/silicon interface is important in controlling the hole current. In addition, the hole current from the metal-con-

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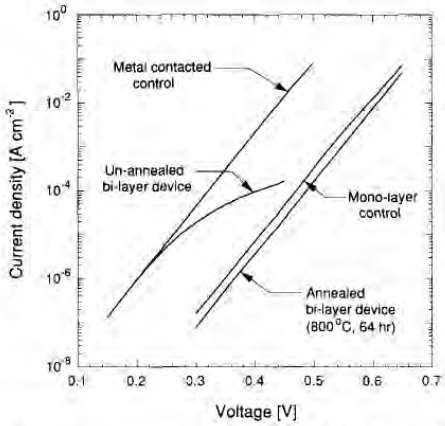

Fig. 7. Current–voltage characteristics of the diodes as analyzed by Neugroschel *et al.* [24]. The devices shown are the metal-contacted control, the single-layer polysilicon control, and the annealed and unannealed bi-layer devices.

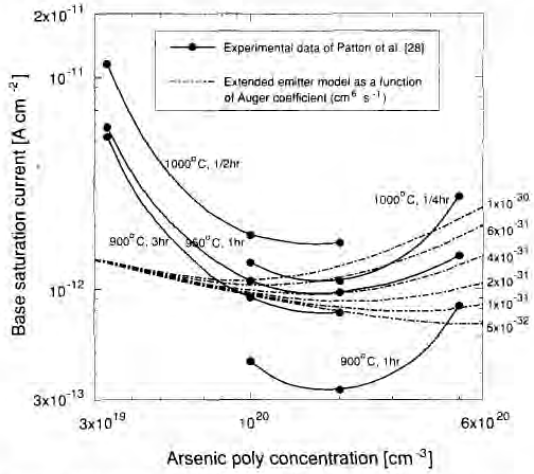

Fig. 8. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for various emitter anneals. Also shown is the modeled base current as a function of Auger coefficient in the polysilicon, assuming that no blocking or recombination mechanisms exists at the interface (i.e., the *extended emitter model* with $T_{\text{block}} = \infty$, $S_I = 0$). The polysilicon is assumed to be 40% electrically active and consisting of only one crystalline grain.

tacted control is almost identical to that of devices with low arsenic concentrations at the interface, which implies the density of interface states is so large as to recombine all the minority holes at the interface. An interface state density of 6×10^{14} cm^{-2} can be calculated by using (1), assuming that the hole current is entirely dominated by recombination at the interface (i.e., $T_{\text{block}} = \infty$, and $S_I >> S_g$ so that $S_p = 2S_I$ in (2)).

For the devices with a high arsenic concentration at the interface, a dramatic reduction of hole current by a factor of 600 is obtained. Assuming that the hole current is again dominated by recombination at the interface ($T_{\text{block}} \approx 0$, so that $S_p = S_I$ in (2)) then an upper limit of 2×10^{11} cm^{-2} can be obtained for the interface state density. The increase of segregated arsenic from 10^{18} to 5×10^{20} cm^{-3} at the interface has therefore reduced the interface state density by over a factor of 3000.

The above results demonstrate the importance of recombination via states at the polysilicon/silicon interface, and also its relationship to the segregated arsenic concentration. Patton *et al.* [28] have also shown that recombination at the interface cannot be ignored, particularly when the doping concentration in the polysilicon is low. Fig. 8 shows the measured base current as a function of polysilicon doping level for various emitter drive-in conditions. Nearly all the devices have large base currents at low polysilicon doping levels (3×10^{19} cm^{-3}), which fall to minimum values around 1–2 $\times 10^{20}$ cm^{-3} and then rise for increased doping levels up to 5×10^{20} cm^{-3}. Also shown in Fig. 8 is the modeled base current from the extended emitter model (i.e., $T_{\text{block}} = \infty$ and $S_I = 0$, so that $S_p = S_g$ in (2)), which can qualitatively explain the increase in base current at high values of doping (2–5 $\times 10^{20}$ cm^{-3}) by increased Auger recombination in the bulk polysilicon. However, the extended emitter model cannot explain either the sharp increase in base current at the low polysilicon doping levels of 3×10^{19} cm^{-3}, or the reduction in base current for the devices annealed at 900°C for 1 h. It can therefore be concluded that a recombination mechanism is dominating at low polysilicon doping levels, while a blocking mechanism is dominating the 900°C 1-h devices.

Fig. 9 shows the modeled values of base current as a function polysilicon doping for various interface state densities, assuming no blocking action at the interface (i.e., $T_{\text{block}} = \infty$, so that $S_p = 2S_I + S_g$ from (2)). The case for $N_{it} = 0$ is that for the *extended emitter model* (i.e., $S_p = S_g$). The modeling clearly demonstrates that a constant value of interface state density cannot model the base current, especially at low arsenic concentrations. Patton *et al.* [28] argued that the arsenic segregation could lower the trap density at the interface. Fig. 10 models the base current of the device annealed at 950°C for 1 h, by the combined contribution of recombination via interface states (for interface densities as a function of arsenic concentration) and minority-carrier transport in the bulk polysilicon (assuming no blocking action at the interface, i.e., $T_{\text{block}} = \infty$). A reasonable fit to the measured base current can result, if it is assumed that the interface state density reduces from 2×10^{14} to 1.4×10^{13} cm^{-2}, as the arsenic concentration increases from 3×10^{19} to 2×10^{20} cm^{-3}.

Fig. 11 shows the fitted interface state density, as a function of polysilicon doping, for all the drive-in conditions in Fig. 9. Also shown are the modeled results from Neugroschel *et al.* [24], who used low-temperature drive-ins of 800°C, and the modeled results from Meister *et al.* [37] who used rapid thermal annealing at 1050°C. The most immediate trend visible is that of a dramatic reduction in interface state density for increases in arsenic con-

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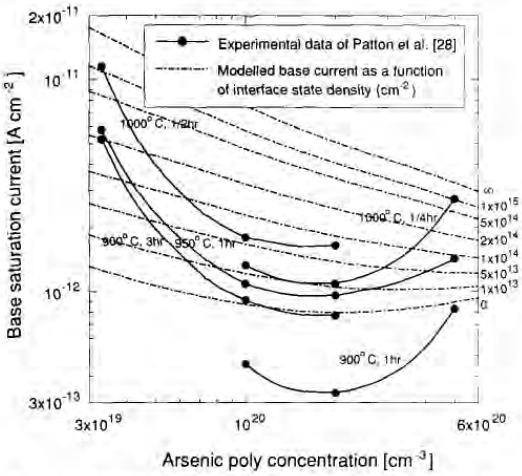

Fig. 9. Experimental data of Patton *et al.* [28]. Also shown is the modeled base current as a function of interface state density, assuming no blocking at the interface (i.e., $T_{block} = \infty$). The modeled base current for a metal-contacted control is also shown (i.e., $N_{it} = \infty$). The polysilicon is assumed to be 40% electrically active.

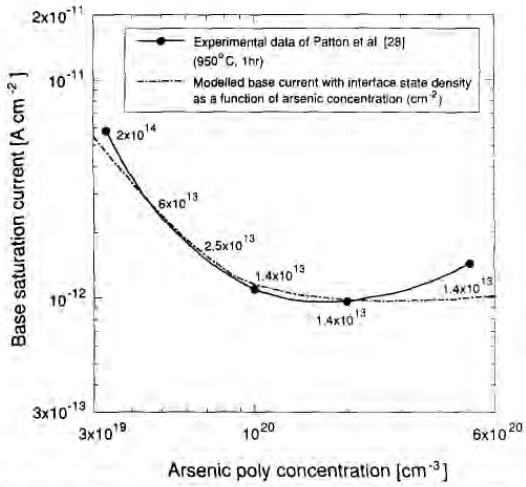

Fig. 10. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 950°C for 1 h. Also shown is the modeled base current as a function of interface state density, assuming that the interface state density varies with arsenic concentration in the polysilicon. No blocking action is assumed to occur at the interface (i.e., $T_{block} = \infty$), and the polysilicon is assumed to be 40% electrically active.

centration from 3×10^{19} to 10^{20} cm^{-3}. This behavior can be explained by the passivation of the interface states due to segregation of arsenic to the interface. There is, however, a second trend in the results of Fig. 11, which reveals that in most cases the largest interface state densities are obtained for the highest anneal temperatures. This result is consistent with the findings of Mandurah *et al.* [65], who found that arsenic segregation to grain boundaries

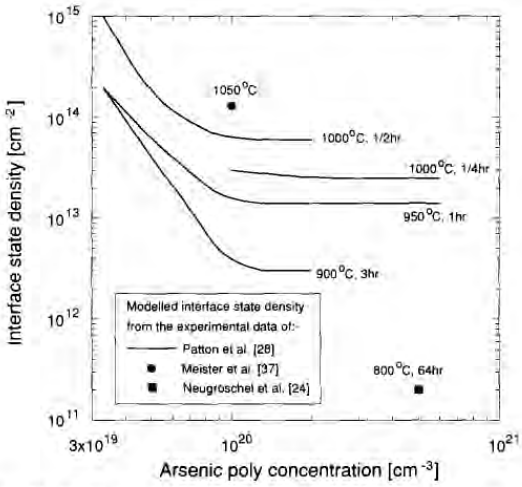

Fig. 11. Modeled interface state density as a function of arsenic concentration in the polysilicon, and polysilicon anneal, for devices with no deliberately grown interfacial oxide layers. Experimental data are from Patton *et al.* [28], Neugroschel *et al.* [24], and Meister *et al.* [37].

increases as the anneal temperature is reduced. If it is assumed that the segregation properties of grain boundaries are similar to those for the pseudo-grain boundary at the polysilicon/silicon interface, then this can explain the reduction of interface state density with anneal temperature.

Turning now to the 900°C device annealed for 1 h, the base current shows a reduction by a factor of 2.5 (for polysilicon doping concentrations of 1–2 $\times$ 10^{20} cm^{-3}) from the *extended emitter model* (Fig. 8), which suggests that a blocking mechanism at the interface is controlling the base current. Fig. 12 shows the experimental data and the modeled base current as a function of the effective recombination velocity S_p. An effective recombination velocity of 2.7×10^4 cm $\cdot$ s^{-1} can be fitted to the base current for polysilicon concentrations of 1–2 $\times$ 10^{20} cm^{-3}. Assuming that the effective recombination velocity is dominated by a blocking mechanism at the interface (i.e., $S_l = 0$ and $T_{block} << S_g$), then the *pseudo-grain boundary mobility model* can be used to model this fitted value of recombination velocity. This results in a minority hole interface mobility μ_{pgb} of 0.1 cm^2 $\cdot$ V^{-1} $\cdot$ s^{-1}, which is a reduction in hole mobility by a factor of 1500 compared with the mobility in the bulk emitter.

The *segregation model* predicts a barrier to minority carriers of around 0.9 kT (using the SIMS analysis in [28]) for the devices annealed at 1000°C, if the segregated arsenic at the interface is electrically active. Assuming a similar barrier exists for devices annealed at 900°C, then this barrier yields a recombination velocity of 7.5×10^4 cm $\cdot$ s^{-1} (no bandgap narrowing), or 8.1×10^4 cm $\cdot$ s^{-1} (with bandgap narrowing). These values of blocking recombination velocity are clearly too large to model the extracted recombination velocity, and so the *segregation model* cannot account for the reduction in base current in Fig. 12.

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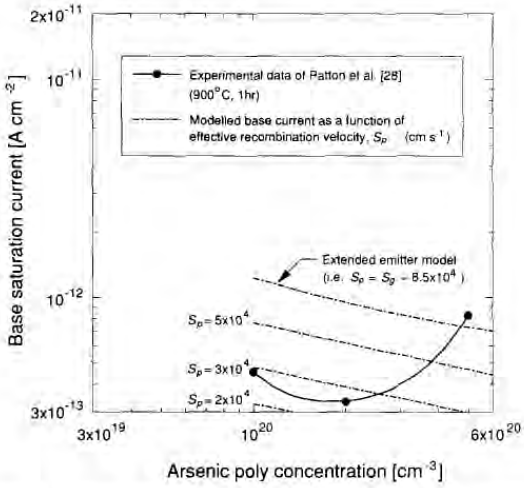
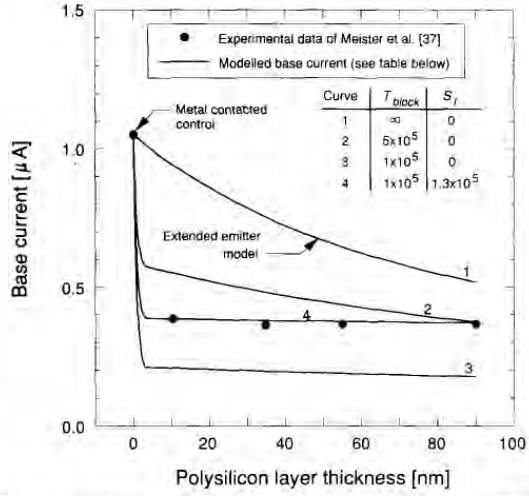


Fig. 12. Experimental data of Patton *et al.* [28] showing base saturation current as a function of arsenic concentration in the polysilicon for an emitter anneal of 900°C for 1 h. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the *extended emitter model* (i.e., with $T_{\text{block}} = \infty$ and $S_I = 0$). The polysilicon is assumed to be 10% electrically active.



Curve	T_{block}	S_I
1	∞	0
2	5×10^5	0
3	1×10^5	0
4	1×10^5	1.3×10^5

Fig. 13. Experimental data of Meister *et al.* [37] showing base current (V_{be} = 0.66 V and A_E = 15.5 × 15.5 μm^2) as a function of polysilicon thickness. Also shown is a metal-contacted control with zero polysilicon thickness. The modeled base current is shown as a function of interface state density and blocking recombination velocity. Also shown is the modeled base current using the *extended emitter model* (i.e., $T_{\text{block}} = \infty$, $S_I = 0$). S_M is taken to be equal to infinity, and S_c is a function of polysilicon thickness.

2) Polysilicon Thinning: The influence of the polysilicon layer on the current gain has been studied by several authors [28], [37] who have made measurements on polysilicon emitter transistors in which the polysilicon layer has been thinned after the emitter drive-in. The results of Meister *et al.* [37] are typical and are shown in Fig. 13. It can be seen that the base current remains constant down to a thickness of less than 10 nm, which shows that the base current is dominated by the blocking/recombination properties of the polysilicon/silicon interface, even in devices without a deliberately grown interfacial oxide layer. Also shown in Fig. 13 is the modeled base currents as a function of polysilicon thickness. Equation [1] was used to convert the modeled effective recombination velocity into a base current, and the emitter Gummel number was extracted from the metal contacted control. The device was first modeled by the *extended emitter model* (i.e., curve 1 with $T_{\text{block}} = \infty$ and $S_I = 0$), and as can be clearly seen it is impossible to model both the metal-contacted control and the variation of base current with polysilicon thickness. Decreasing T_{block} to 5×10^5 cm · s^{-1} (curve 2, with $S_I = 0$) enables the base current of the metal-contacted control and the polysilicon emitter device with an emitter thickness of 90 nm to be both modeled. However, for polysilicon thickness between 0 and 90 nm the model cannot be fitted to the base current. Further reductions in T_{block} to 1×10^5 cm · s^{-1} (curve 3), allows the constant base current with polysilicon thickness to be modeled, but at the expense of being unable to model the absolute value of base current. The only way to remedy this situation is for the interface state recombination velocity (S_I) to take values other than zero. Curve 4 in Fig. 13 shows that an excellent fit to the experimental data can be made with $T_{\text{block}} \leq 10^5$ cm · s^{-1}, and $S_I \geq 1.3 \times 10^5$ cm · s^{-1}, which corresponds to an interface state density which must be greater than 1.3×10^{14} cm^{-2}.

3) Temperature Dependence of Current Gain: The temperature dependence of the current gain for devices without a deliberately grown interfacial layer has been experimentally measured by Ashburn *et al.* [11], and is shown in Fig. 14(a) and (b). They found that the temperature sensitivity of the current gain was *greater* than that of conventional metal-contacted transistors, especially at higher temperatures. This temperature dependence differs markedly to that of devices with deliberately grown interfacial oxide layers (i.e., dominated by tunneling), which show a far *lower* temperature sensitivity at higher temperatures. Fig. 14(a) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *oxide tunneling model*. It is clear that the model cannot explain the observed temperature dependence (especially at higher temperatures), and so it can be concluded tunneling is not the dominant mechanism in devices without deliberately grown interfacial oxide layers.

Fig. 14(b) shows the experimental data of Ashburn *et al.* [11], as well as the modeled current gain using the *pseudo-grain boundary mobility model*. If it is assumed that the interface hole mobility is temperature-independent, then the temperature dependence of the current gain is controlled by the difference in the bandgap narrowing between the base and emitter, as in a conventional metal-contacted device (shown as the $n = 0$ curve in Fig. 14(b)). However, a fit cannot be made to the measured current gain, which implies that the hole mobility must be tem-

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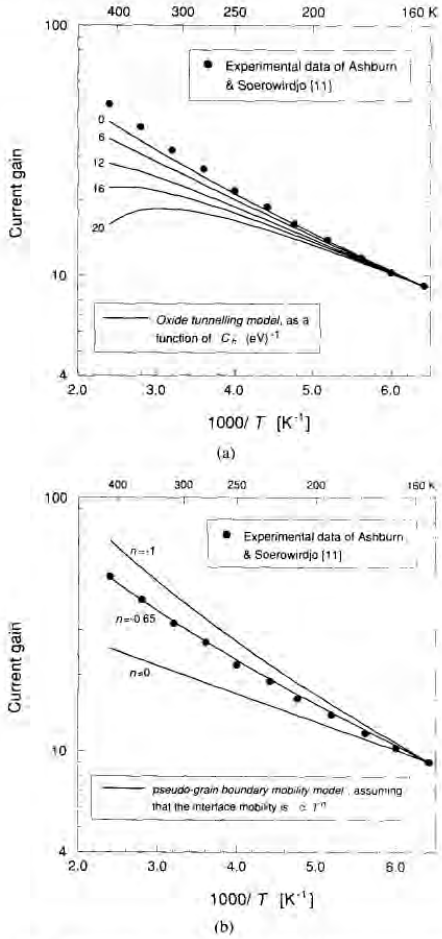

Fig. 14. (a) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the *oxide tunneling model* (assuming $S_f = 0$, and $T_{block} \ll S_e$), as a function of the parameter c_b (in (6)). (b) Experimental data of Ashburn *et al.* [11] showing current gain as a function of inverse temperature for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current, using the *pseudo-grain boundary mobility model* (assuming $S_f = 0$, and $T_{block} \ll S_e$). The interface mobility (μ_f) is assumed to be proportional to T^{-n}. The $n = 0$ case corresponds to the temperature dependence of a conventional metal-contacted bipolar transistor, whereby the temperature dependence is attributed to the difference in bandgap narrowing between the base and emitter.

perature-dependent. If it is assumed that the interface hole mobility has a dependence of the form $\mu_f = AT^{-n}$ (where A is a temperature-independent constant), then an excellent fit to the experimental data can be achieved for $n = -0.65$.

4) Effect of an Interface Anneal: Wolstenholme *et al.* [10] have performed the same interface anneal experiments with HF devices as with RCA devices, and the results are shown in Fig. 15. These results show that the base current increases by a factor of 5.5 as the interface

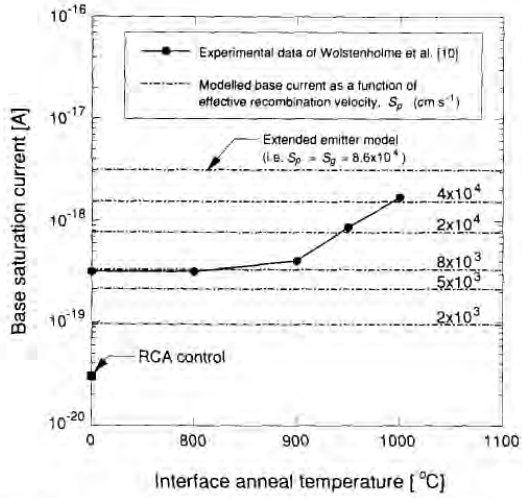

Fig. 15. Experimental data of Wolstenholme *et al.* [10] showing the base saturation current as a function of interface anneal for devices without a deliberately grown interfacial oxide layer. Also shown is the modeled base current as a function of the effective recombination velocity (S_p), and the modeled base current using the *extended emitter model* (i.e., with $T_{block} = \infty$ and $S_f = 0$).

anneal temperature is increased from 800 to 1000°C. Also shown in Fig. 15 is the modeled base current as a function of effective recombination velocity S_p, and the modeled base current using the *extended emitter model*. Transmission electron microscopy (TEM) reveals that a dip-etch in hydrofluoric acid (HF) prior to polysilicon deposition (which is designed to remove any interfacial oxide), nevertheless produces a uniform oxide of approximately 4-Å thickness. After typical anneals at 900°C, thermal stressing causes the thin HF oxide to break up, leading to a discontinuous layer varying in thickness from 0 to 8 Å, and with approximately 30% of the interface oxide-free. This compares with the 1000°C interface anneal device, in which 90% of the interface is oxide-free. These results clearly indicate that the interfacial oxide controls the base current in a HF device. It is tempting to conclude, therefore, that tunneling through the interfacial oxide is the dominant mechanism, even in HF devices. However, as already shown in Fig. 14(a), this conclusion is inconsistent with the measured temperature dependence of the current gain, which is markedly stronger for the HF devices than for the RCA devices. In order to explain this apparent inconsistency, it is necessary to consider how a discontinuous interfacial oxide can be modeled in two dimensions.

C. Modeling a Discontinuous Interfacial Layer

Very little has been published on the two-dimensional modeling of the polysilicon/silicon interface, although Hamel *et al.* [59] have simulated the majority carrier flow in a polysilicon emitter as a function of oxide breakup. Their simulations revealed that the majority-carrier cur-

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rent flow had a large lateral component, which was required to explain the observed decrease in emitter resistance with oxide breakup [45]. Recent attempts to model the minority-carrier flow at the polysilicon/silicon interface in two dimensions [66] have shown that the current flow is primarily through those regions of the interface free from oxide. Hence the lateral component of the minority-carrier flow can be largely ignored, and this is the approach followed in this paper.

The effect of a broken up interfacial oxide layer on the base current is modeled by assuming that the emitter can be treated as two polysilicon emitter transistors connected in parallel, one with an interfacial oxide layer and the other without. The area of the interface which is oxide-covered is denoted by A_{ox}, and that which is oxide-free by A_{nox}. Each of these areas of the interface can then be described by an effective recombination velocity $S_{p\,ox}$ (dominated by the *oxide tunneling model*) and S_{ppgb} (dominated by the *pseudo-grain boundary mobility model*). The overall recombination velocity S_p can then be calculated as a weighted mean of these two contributions

$$S_p = S_{p\,ox}\left(1 - \frac{A_{nox}}{A_{EW}}\right) + S_{ppgb}\left(\frac{A_{nox}}{A_{EW}}\right) \qquad (9)$$

where A_{EW} is the total emitter window area. Wolstenholme [57] and Gold [67] have used (9) to model the base current of polysilicon emitters as a function of the fraction of interface which is oxide-free, and the results are shown in Fig. 16 for devices with a deliberately grown interfacial oxide layer. Also shown are some of the modeled recombination velocities from the experimental results in Figs. 2 and 15. The value of $S_{p\,ox}$ used in Fig. 16 for the situation of no oxide breakup has been fitted from the base current of the RCA control device. As the oxide breaks up, high-resolution TEM has shown [10], [67] that it becomes thicker in some regions and thinner in others, with the overall oxide volume remaining constant. In order to model the tunneling current through the oxide-covered regions (the first term in (9)), $S_{p\,ox}$ has been calculated for each of the RCA devices, assuming an initial oxide thickness of 14 Å and a constant oxide volume. The result of these calculations is shown as the dashed line in Fig. 16. It is clear that, apart from the very early stages of oxide breakup ($A_{nox}/A_{EW} \leq 0.1$), the overall recombination velocity S_p is dominated by the second term in (9). This means that the majority of the hole current in a device with a broken up interfacial oxide flows through the oxide-free regions. Thus the factor of a 100 increase in base current of the RCA device with an interface anneal of 1100°C compared to the control (Fig. 2), can be partly explained as simply the increase in area of those portions of the interface which are free from oxide.

Another factor which is likely to influence S_p is the epitaxial regrowth of the polysilicon through the holes in the interfacial oxide [10], [67]. This regrowth is likely to affect the value of the pseudo-grain boundary recombination velocity S_{ppgb}, since the grain boundary moves further

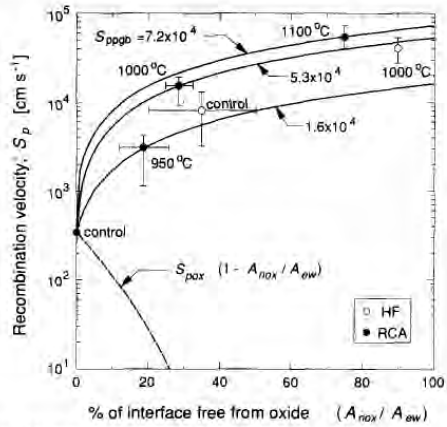

Fig. 16. Modeled recombination velocity S_p as a function of the fraction of the interfacial layer which is oxide free, for devices with a deliberately grown interfacial oxide layer (using (9)). Also shown is a selection of the modeled experimental base currents from Figs. 2 and 15. The modeled recombination velocity is only strictly relevant for those devices with a deliberately grown interfacial oxide layer (RCA). The dashed line corresponds to only the first term in (9).

into the polysilicon as the oxide breaks up. Extra recombination in the single-crystal emitter would therefore be expected, which would be seen as an increase in S_{ppgb}. The effect of a change in the value of S_{ppgb} is illustrated in Fig. 16, whereby to model the base currents of the RCA devices, S_{ppgb} has to increase from 1.6×10^4 to 7.2×10^4 cm · s^{-1} as the interface breaks up and the polysilicon epitaxially regrows. This corresponds to an increase in pseudo-grain boundary mobility from 0.043 to 0.195 cm^2 · V^{-1} · s^{-1}.

Turning now to the devices without deliberately grown interfacial layers (HF devices), the modeling is somewhat complicated since there exists no "control" device (i.e., a device with a uniform 4 Å oxide at the interface). Nevertheless, if it is assumed that the value of $S_{p\,ox}$ used in (9) is much less than S_{ppgb}, then the modeled curves in Fig. 16 are still valid for the HF devices. The difference in recombination velocity between the control HF device and the 1000°C interface anneal device is a factor of 5.5, while the difference in the oxide-free area at the interface is only a factor of 3. The fact that the base current increases more than predicted by the difference in areas of the oxide-free regions of the interface can be explained by an increase in the value of the pseudo-grain boundary recombination velocity, S_{ppgb} from 2.4×10^4 to 4.4×10^4 cm · s^{-1}. This therefore corresponds to an increase in pseudo-grain boundary mobility by a factor of only 1.8 from 0.065 to 0.12 cm^2 · V^{-1} · s^{-1}. It can therefore be seen that the increase in base current of an HF device subjected to an interfacial anneal is determined mostly by the increase in the fraction of the interface which is oxide-free, though there is also a small contribution (a factor of 1.8 compared with a factor of 3) from an increase in the pseudo-grain boundary recombination velocity, S_{ppgb} due

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to the epitaxial regrowth of the polysilicon. Moreover, the base current of the HF control device is dominated by current flow through the gaps in the interfacial oxide, with the result that the dominant mechanism is the reduced minority-carrier mobility at the interface, which is in agreement with the temperature dependence of current gain in Fig. 14(b).

VI. Conclusions

This paper has critically reviewed theories in the literature on the current gain enhancement of polysilicon emitter bipolar transistors, and then applied these theories in a consistent manner to the published experimental data. In this way, it has been possible to identify the dominant physical mechanisms for a given set of fabrication conditions. In devices fabricated with a deliberately grown interfacial oxide layer, tunneling through the interfacial oxide layer can explain both the reduction in base current and the increase in emitter resistance, as well as the temperature dependence of these two quantities. In devices fabricated without a deliberately grown interfacial oxide layer, two distinct regions of device behavior have been identified. First, for low concentrations of arsenic in the polysilicon ($<10^{20}$ cm^{-3}) and/or high anneal temperatures ($>1000°$C), recombination of carriers via interface states at the polysilicon interface dominates the base current. This results in a current gain which is lower than that for an extended emitter device. Secondly, for arsenic concentrations of 1-2 $\times$ 10^{20} cm^{-3} and anneals around 900°C (as used in many commercial processes), the increased segregation of arsenic to the interface pacifies the interface states. These devices exhibit a gain enhancement compared with an extended emitter device. In order to fully explain this gain enhancement, it is necessary to model the discontinuous interfacial oxide in two dimensions. The use of a simple pseudo-two-dimensional model shows that the oxide covered regions of the interface are opaque to minority carriers, so that most of the current flows through the gaps in the oxide. The base current is therefore determined primarily by the fraction of the interface which is oxide-free, and hence is very sensitive to the detailed structure of the interfacial oxide. The dominant base current mechanism is thus reduced minority-carrier mobility in the pseudo-grain boundary at the polysilicon/silicon interface.

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ATTACHMENT J-4

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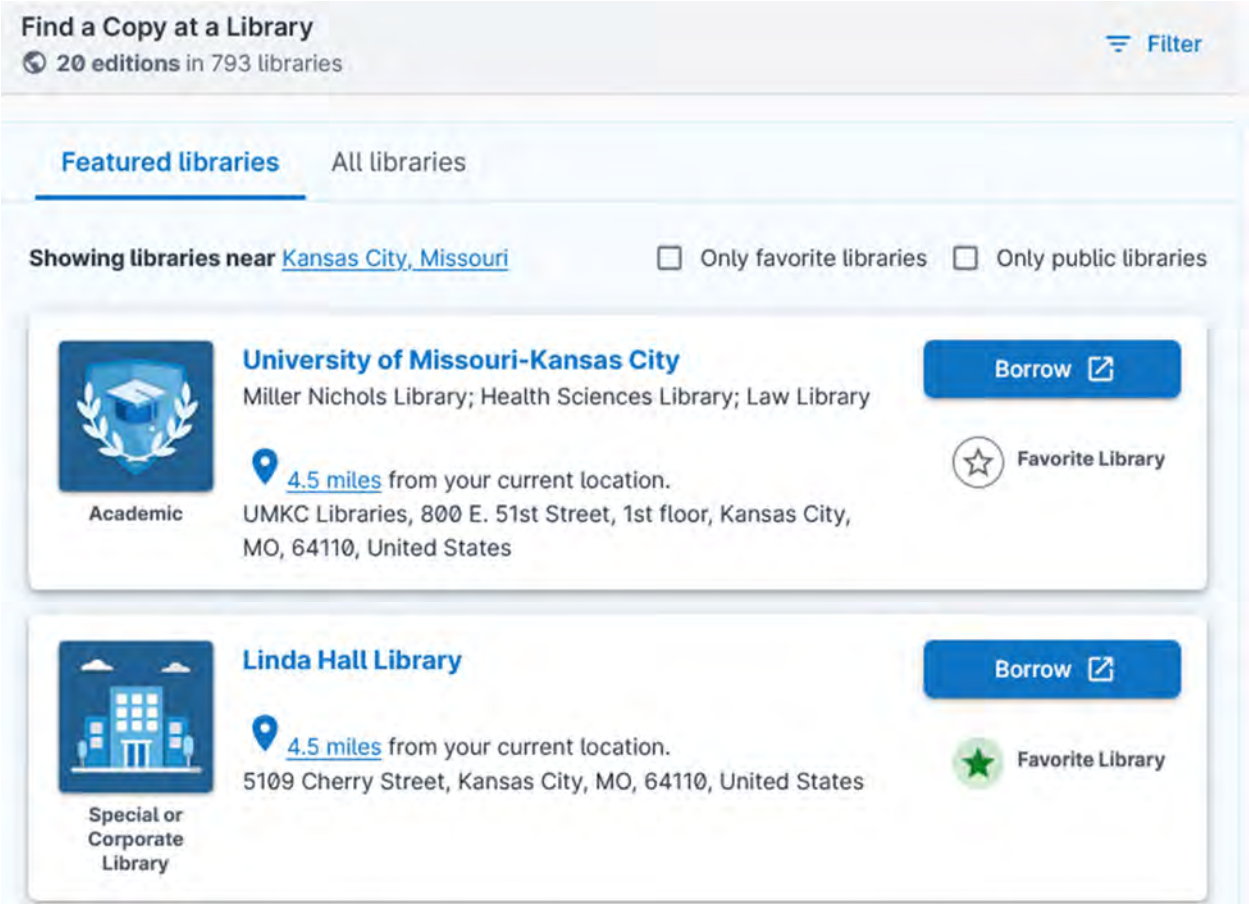

ATTACHMENT J-5

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ATTACHMENT K-1

An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations

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A comparison is made between the results of high-resolution electron microscope observations and the electrical characteristics of polycrystalline silicon emitter bipolar transistors. Devices are fabricated with and without a deliberately grown interfacial oxide layer, and the thermal stability of this oxide layer is investigated by carrying out a preanneal at temperatures between 800 and 1100 °C after polysilicon deposition, but prior to emitter implant and 900 °C drive-in. The electron microscope observations show that the deliberately grown interfacial oxide is of uniform thickness ~14 Å, but breaks up when annealed at ~950 °C and above, with "balling-up" occurring at ~1100 °C. This correlates with a transistor gain that decreases from ~1400 to ~40. The electron microscopy also shows that a thin interfacial oxide layer is present even when not deliberately grown. This oxide breaks up when annealed at ~900 °C and above, with "balling-up" occurring at ~1000 °C. This correlates with a transistor gain that decreases from ~240 to ~50. Calculations of the effect that such interfacial oxide layers will have on the characteristics of polysilicon emitter bipolar transistors are made, and these predictions correlate well with the measured characteristics.

I. INTRODUCTION

Polycrystalline silicon ("polysilicon") is now widely used in bipolar technology as a means of making contact to the emitter and base of the transistor[1] and this can lead to a dramatic improvement in both switching speed and packing density.[2,3] An additional advantage of using a polysilicon emitter is that an improvement in gain by a factor of between 3 and 30 can be obtained compared with conventional transistors.[4] This improvement in gain can be partly attributed to the transport properties of the polysilicon[5] although this mechanism can only explain an improvement by a factor of ~3. The much larger gain improvements are obtained when a thin interfacial oxide layer is deliberately introduced between the polysilicon and single-crystal silicon.[4,6,7] In this case the gain improvement can be attributed to tunneling through this oxide layer.[8] Eltoukhy and Roulston,[9,10] and later Yu *et al.*,[11] have published unified theories that incorporate both these mechanisms, the former giving a solution suitable for numerical implementation, the latter a versatile analytical solution.

If high-gain polysilicon emitter transistors incorporating an interfacial oxide layer are to be used in commercial integrated circuit processes, it is important that the oxide layer is fully characterized in terms of thickness and uniformity, and that it is stable during subsequent high-temperature processing. Our previous structural studies[12–16] showed that the oxide layer progressively breaks up during high-temperature heat treatments. In order to investigate this behavior in more detail and to relate it directly to device performance, we have carried out a detailed comparison of electrical results on polysilicon emitter transistors with structural results from high-resolution transmission electron microscopy. The thermal stability of the oxide layer was investigated by carrying out preanneals at temperatures between 800 and 1100 °C immediately after polysilicon deposition but prior to emitter implant and drive-in at 900 °C. In this way, the oxide layer could be subjected to a high-temperature heat treatment without significantly affecting the rest of the emitter structure, and therefore changes in gain could be correlated directly with changes in the structure of the oxide layer.

II. EXPERIMENT

Two types of polysilicon emitter bipolar transistor were fabricated using identical standard processing up to the surface treatment of the (100) silicon slices prior to polysilicon deposition. For the first type (RCA treatment), the slice was given a dip in buffered HF followed by an RCA clean[4] (NH_4OH:H_2O_2:H_2O as 1:1:5 for 10 min; HCl:H_2O_2:H_2O as 1:1:6 for 10 min) to produce a surface oxide layer of nominal thickness ~15 Å. For the second type (HF treatment), the slice was given a dip in buffered HF with the intention of

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removing any native oxide which might have been present.[4] These surface layer treatments were immediately followed by the deposition of a ~0.4-μm-thick layer of undoped LPCVD polysilicon at ~610 °C. One of each type of slice was given a 10 min preanneal in dry nitrogen at one of several temperatures in the range 800–1100 °C in order to breakup the interfacial oxide layer to different extents. The emitters of the transistors were then formed by implanting 1×10^{16}-cm^{-2}, 70-keV As^+ into the polysilicon and driving it in at 900 °C in wet oxygen for 30 min. The active emitter area was 20 μm by 18 μm. The aluminium contact to the emitter was remote from the active emitter area, being made a via polysilicon track 60 μm in length.

Detailed electrical measurements were carried out on the transistors including measurements of collector and base current as a function of base/emitter voltage. Unpatterned check slices which had been given identical base and emitter processing were used for the TEM studies. Cross sections were prepared corresponding to the $(01\bar{1})$ plane of the (100) single-crystal silicon slice by grinding, polishing, and argon ion-beam thinning. These were examined using a JEOL 200CX TEM with the electron beam aligned parallel to the $[01\bar{1}]$ direction of the single-crystal silicon. High-resolution electron microscopy (HREM) was performed to give lattice images using conventional procedures. All of the specimens examined (except for that of Fig. 6) corresponded to the final processed slices and so the observed TEM structures could be directly correlated with the device results. Large numbers of micrographs were taken of each specimen in order to determine its characteristic structure. The micrographs of Figs. 1–6 are typical of those obtained, but do not show all the features described in the text.

III. TEM RESULTS

For specimens given in an RCA treatment, a 900 °C preanneal and full processing (As^+ implant and 900 °C drive-in), cross-section micrographs of the interface region showed the single-crystal silicon with the characteristic (111), $(\bar{1}11)$, and (200) lattice planes clearly delineated (Fig. 1). The individual polysilicon grains only showed lattice planes when the grains were favorably oriented with respect to the electron beam, e.g., as at A. When such planes were observed in the individual polysilicon grains, they were in general not aligned with the planes present in the silicon.

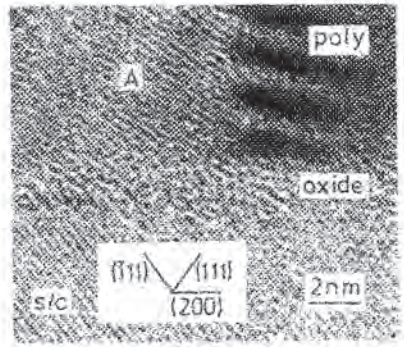

FIG. 1. HREM micrograph of a fully processed specimen given an RCA treatment and a 900 °C preanneal. Note the interfacial oxide layer and the polysilicon grain A. s/c—single-crystal silicon; oxide—interfacial oxide layer; poly—polysilicon layer.

The interfacial oxide layer was seen as a thin bright band separating the silicon from the polysilicon. The band exhibited a random wormlike contrast in the lattice-image micrographs, this being the characteristic behavior for an amorphous material. The oxide layer was continuous and uniform with a thickness of ~14 ± 1 Å and it followed the undulations of the surface of the silicon slice with an "amplitude" of ~6–9 Å (perpendicular to the interface) and a "wavelength" of ~200–400 Å (parallel to the interface). The good uniformity of the oxide layer indicates that its structure had been little changed by the subsequent 900 °C preanneal and 900 °C drive-in, and so Fig. 1 shows it in effect as it was when initially produced by the RCA treatment. The directly measured oxide layer thickness of 14 Å is in good agreement with the values of 13–15 Å obtained from ellipsometry,[17] and 10–15 Å obtained from Auger spectroscopy profiles,[18] for silicon slices given an RCA treatment. The TEM results are summarized in Table I.

For specimens given an RCA treatment, a 950 °C preanneal and full processing, the interfacial oxide layer was nonuniform (Fig. 2). Some regions had increased in thickness to a maximum of 19 Å, some regions were thinner, and in some regions holes (B) were present in the layer. Small areas (C) of the polysilicon had been regrown through such holes to become single-crystal material with the same crystallographic orientation as the underlying silicon, this being deduced from the micrograph contrast and the alignment of

TABLE I. Summary of results.

Silicon slice surface treatment	Preanneal temperature (°C)	Interfacial oxide layer: Geometry	Interfacial oxide layer: Maximum thickness (Å)	Polysilicon: Fraction of interface regrown	Polysilicon: Grain size (Å) Surface	Polysilicon: Grain size (Å) Bulk	Transistor gain
RCA	900	continuous	~14	0	1200	400	1400
RCA	950	broken up	~19	0.3	1200	600	350
RCA	1000	broken up	~22	0.7	1200	1000	90
RCA	1100	balled up	~55	0.97	2000	1000	40
HF	None	broken up	~8	0.2	1200	400	240
HF	1000	balled up	~50	0.95	1200	1000	50

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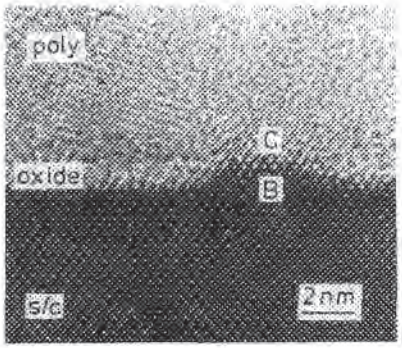

FIG. 2. HREM micrograph of a fully processed specimen given an RCA treatment and a 950 °C preanneal. Note the hole B in the interfacial oxide layer and the regrown polysilicon area C.

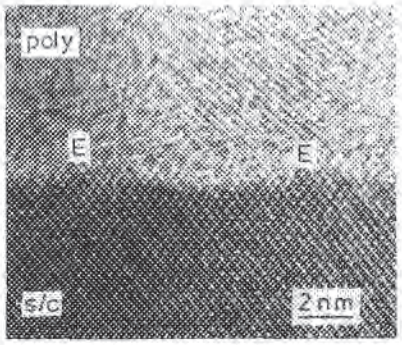

FIG. 4. HREM micrograph of a fully processed specimen given an HF treatment and no preanneal. Note the regrown polysilicon areas E.

the lattice planes. The regrown areas had often spread out laterally in the polysilicon and so were sometimes wider than the holes in the oxide layer through which they had been grown. Individual areas extended typically 35 Å along the interface and 35 Å into the polysilicon. When the individual lengths of the regrown areas of the polysilicon were measured along the interface and added together, this represented ~0.3 of the total length of the interface.

For the specimens given an RCA treatment, a 1000 °C preanneal and full processing (micrograph not included), the breakup of the interfacial oxide layer was more pronounced. Some regions had increased in thickness to a maximum of 22 Å, and more holes were present in the layer. However, no substantial "balling-up" of the layer had occurred. Individual regrown areas of the polysilicon extended typically 120 Å along the interface and 40 Å into the polysilicon. The fraction of the length of the interface that had regrown was ~0.7.

For specimens given an RCA treatment, a 1100 °C preanneal and full processing, the breakup of the interfacial oxide layer was almost complete (Fig. 3), the layer now consisting mainly of balls of oxide (D) up to 55 Å in diameter or worms ~30×100 Å across. Individual regrown areas of the polysilicon overlapped to give almost complete coverage of the interface with the regrowth extending typically 170 Å into the polysilicon. The large difference between the oxide layer in the specimens given the 950, 1000, and 1100 °C preanneals, and the specimen given the 900 °C preanneal, indicates that the breakup of the oxide in the 950, 1000, and 1100 °C specimens occurred during the preanneals.

For specimens given an HF treatment, no preanneal and full processing, an interfacial oxide layer was present but it was not continuous (Fig. 4). In some regions it was up to a maximum thickness of 8 Å, in other regions it was thinner, and in some regions there were holes. Small areas (E) of the polysilicon had regrown through the holes, individual areas extending typically 25 Å along the interface and 25 Å into the polysilicon. The fraction of the interface that had been regrown was ~0.2.

For specimens given an HF treatment, a 1000 °C preanneal and full processing, the breakup of the interfacial oxide layer was severe, the layer consisting mainly of balls of oxide up to 50 Å diameter (Fig. 5). Individual areas (F) of regrown polysilicon extended typically 300 Å along the interface and 150 Å into the polysilicon, each area often covering several oxide balls (G) and holes (H). The fraction of the length of the interface that had regrown was ~0.95. The

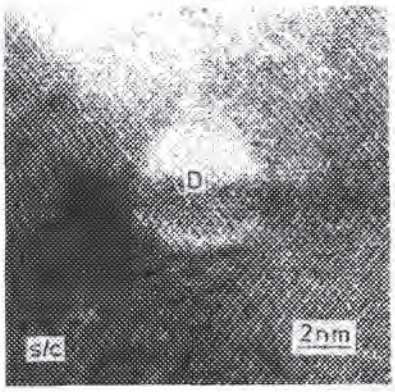

FIG. 3. HREM micrograph of a fully processed specimen given an RCA treatment and an 1100 °C preanneal. Note the balled-up oxide D.

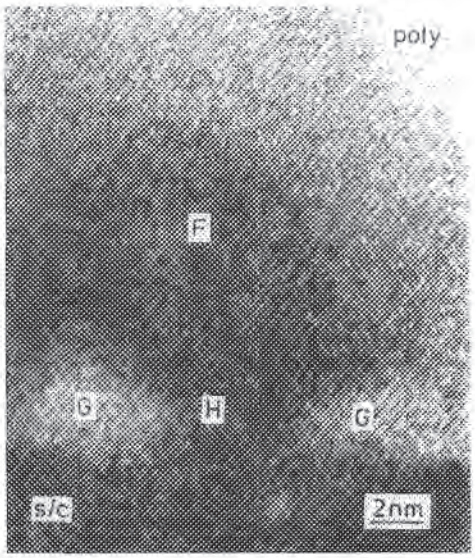

FIG. 5. HREM micrograph of a fully processed specimen given an HF treatment and a 1000 °C preanneal. Note the regrown polysilicon area F, the balled-up oxide G, and the holes in between H.

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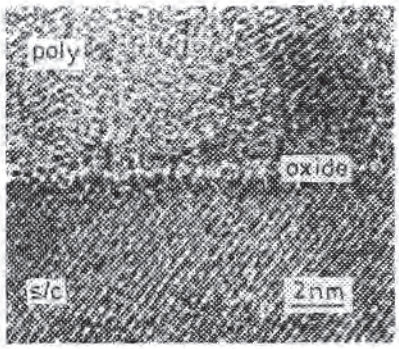

FIG. 6. HREM micrograph of a specimen given an HF treatment, but no preanneal, implant, or drive-in.

large difference between the oxide layers in the specimen given the 1000 °C preanneal, and the specimen given no preanneal, indicates that the "balling-up" of the oxide in the 1000 °C specimen mainly occurred during the preanneal.

In order to obtain further information concerning the interfacial oxide layer that was present after an HF treatment, additional specimens were examined that corresponded to an HF treatment and polysilicon deposition, but no further processing. A white band was seen at the interface (Fig. 6) but this was extremely thin, and so the oxide thickness could not be directly measured accurately. The interface was very uniform, and in a few places adjacent to the interface small areas of the polysilicon were of the same crystallographic orientation as the single-crystal silicon. These areas could have arisen by either direct epitaxial growth through holes initially present in the oxide layer or regrowth through holes created initially present in the oxide layer during the deposition of the polysilicon at 610 °C. The results indicate that an extremely thin and mainly continuous oxide layer was present immediately after the polysilicon deposition. The results also indicate that for the specimens that were given an HF treatment, no preanneal and full processing, the significant breakup of the oxide layer that was observed occurred during the 900 °C drive-in.

In our previous TEM studies[13] of the breakup of an analogous interfacial oxide layer formed by a sulfuric acid/hydrogen peroxide surface chemical treatment, it was shown that the volume of the oxide present after complete balling-up of the layer corresponded closely to the volume of the ~10-Å-thick uniform oxide layer that was present initially. This suggested that the breakup of the oxide layer occurred mainly by a local diffusion mechanism. Application of this principle to the present work gives the following results. For the specimens given an HF treatment, a 1000 °C preanneal, and full processing, the balled-up oxide corresponded to an approximately planar array of spheres of mean diameter 40 Å and mean spacing 100 Å. Calculation shows that this is equivalent to an initial uniform oxide layer of thickness ~4 Å, a result which is consistent with the TEM observations for the specimens given an HF treatment and polysilicon deposition, but no further processing (Fig. 6). For the specimens given an RCA treatment, an 1100 °C preanneal, and full processing, a similar calculation showed that the balled-up oxide layer is equivalent to an initial uniform oxide layer of thickness ~15 Å. This result is in good agreement with the TEM value of ~14 Å for the specimens given an RCA treatment, preannealed at 900 °C, and fully processed (Fig. 1).

Present evidence indicates that there are genuine differences in the thickness of oxide layers formed on silicon slices by the HF treatments of different organizations. These differences may depend on the HF solution, the dip procedure, or the elapsed time prior to the subsequent deposition of the polysilicon. Our TEM examinations of silicon specimens given nominally the same HF treatment, and subsequently processed, by different organizations have shown differences in the behavior of the oxide layer which we attribute to differences in its initial thickness.[19] Furthermore, measurements by different organizations of the thickness of oxide layers present on silicon slices after HF treatments have given markedly different values, e.g., 8–9 Å from ellipsometry[17] and ~3 Å from Auger spectroscopy.[18]

The above TEM results show that the interfacial oxide layers break up faster when they are heated at higher temperatures, and when they are initially thinner. Thus, for the oxide layers arising from the HF treatment, which were initially ~4 Å thick, breakup had already occurred during a heat treatment at 900 °C (drive-in), while for oxide layers arising from the RCA treatment, which were initially ~14 Å thick, breakup only began to occur during a treatment at 950 °C (preanneal). These present results are consistent with our previous TEM results[14,16] which indicated that an initially ~10-Å-thick oxide layer was just beginning to break up at 900 °C. The results are also consistent with the TEM results of Schaber *et al.*[20] which showed that for an oxide layer ~30 Å thick, breakup did not occur at 950 °C. However, some caution is required when making comparisons of such results obtained by different organizations because the precise behavior depends on a number of factors, e.g., it has been shown that such oxide layers break up more rapidly when the arsenic concentration is higher.[15,16]

Grain sizes for the polysilicon layers in fully processed specimens were determined from TEM cross-section micrographs taken at lower magnifications. For individual specimens, the grain size near the polysilicon layer surface was in general larger than in the remainder of the polysilicon layer. This was because the upper portion of the polysilicon layer had been made amorphous by the arsenic implant. Consequently, during the drive-in at 900 °C, larger grains had formed in this portion of the layer by regrowth from amorphous material than in the remainder of the layer by regrowth from fine grains. For the grains in the main portion of the layer, i.e., away from the layer surface, the results showed that the mean grain size was typically 400, 600, 1000, and 1000 Å for preanneal temperatures of 900, 950, 1000, and 1100 °C, respectively. Conversely, for the grains near the surface, the mean grain size was typically 1200 Å for all of these preanneal temperatures, except for 1100 °C when it was typically 2000 Å.

IV. ELECTRICAL RESULTS

Figures 7 and 8 show Gummel plots for the RCA- and HF-treated devices, respectively, that were given preanneals

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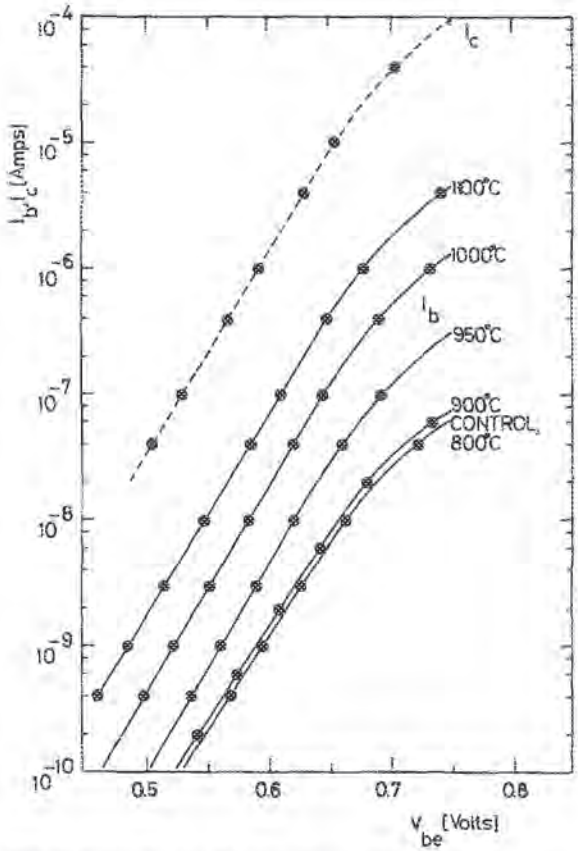

FIG. 7. Gummel plots of devices given an RCA treatment and preanneals in the range 800–1100 °C.

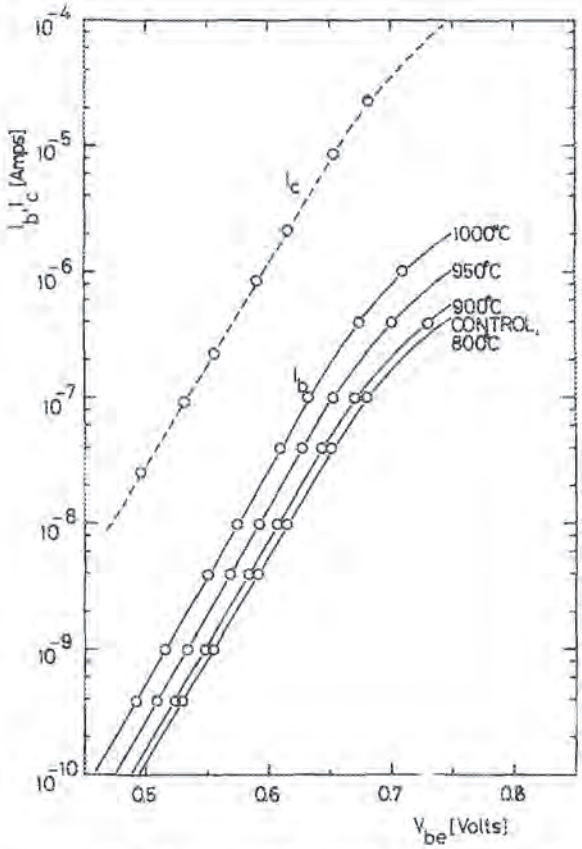

FIG. 8. Gummel plots of devices given an HF treatment and preanneals in the range 800–1000 °C.

between 800 and 1100 °C. The collector characteristics for both the HF- and RCA-treated devices are all ideal over at least three orders of collector current (60 mV/decade). Similarly the base characteristics of the HF-treated devices are also ideal, although the base characteristics of the RCA-treated devices are slightly nonideal (70 mV/decade) corresponding to an ideality parameter of $n = 1.12$. To show the effect of the preanneal on the electrical characteristics of the RCA- and HF-treated devices, I_{b0} and I_{c0} have been plotted against the preanneal temperature in Fig. 9. Because of the nonideality of the base current characteristics of the RCA-treated devices, the values of I_{b0} were calculated from the ideal collector characteristics and maximum current gain β_{max} using the relationship[21] $I_{b0} = I_{c0}/\beta_{max}$.

For the RCA-treated devices, Figs. 7 and 9 show that the collector current is relatively unaffected by a preanneal. Conversely, the base current is strongly affected with the electrical results falling into two distinct regimes. Below ~900 °C, the base current is approximately constant. In this regime, the 900 °C drive-in is the dominant process as far as the interfacial oxide layer is concerned. Above ~900 °C, the base current increases rapidly with preanneal temperature. In this regime, the preanneal is the dominant process as far as the oxide layer is concerned. For example, the base current increases after a 950 °C preanneal by ~6×, after a 1000 °C preanneal by ~28×, and after a 1100 °C preanneal by ~100×. This trend correlates well with the TEM results. Thus, after a 900 °C preanneal, the oxide layer is uniform and continuous (Fig. 1) and the gain is not significantly affected by the preanneal. After a 950 °C preanneal, the oxide layer begins to break up (Fig. 2) and a large increase in

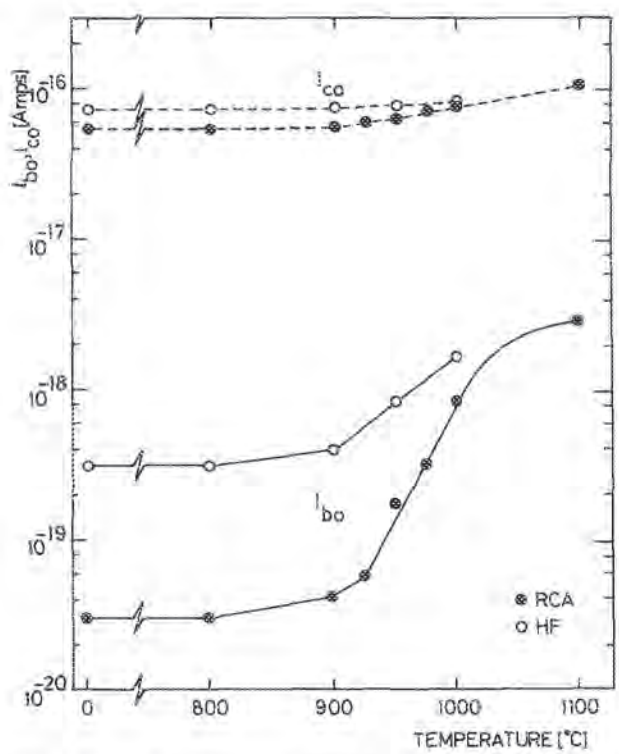

FIG. 9. I_{b0} and I_{c0} vs preanneal temperature for devices given RCA and HF treatments.

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the base current occurs. As the preanneal temperature is further increased, the breaking up of the oxide layer continues (Fig. 3) and this corresponds to a continuing increase in the base current. Over the preanneal temperature range of 800–1100 °C, the transistor gain decreases from ~1800 to ~40.

For the HF-treated devices, Figs. 8 and 9 show a similar but less pronounced trend to that of the RCA-treated devices. Thus, the collector current is relatively unaffected by a preanneal. For the base current, after a preanneal below ~900 °C, no significant increase occurs. After a 950 °C preanneal it increases ~3×, and after a 1000 °C preanneal it increases ~5.5×. This increase in the base current again correlates with a progressive increase in the breaking up of the interfacial oxide layer (Figs. 4 and 5), although it should be noted that some polysilicon grain growth also occurs (Table I). Over the pre-anneal temperature range of 800–1000 °C, the transistor gain decreases from ~240 to ~50.

A comparison of the RCA- and HF-treated devices shows the following. After a preanneal below ~900 °C, the base current for the RCA-treated devices is ~10× less than for the HF-treated devices. This difference correlates with the former devices having a relatively thick, continuous oxide layer, and the latter devices having a thin broken-up oxide layer. After a preanneal at 1000 °C, the base current for the RCA-treated devices is ~2× less than for the HF-treated devices. This difference correlates with the former devices having a broken-up oxide layer, and the latter devices having a completely balled-up oxide layer.

V. INTERPRETATION OF ELECTRICAL RESULTS

The larger gain that occurs for polysilicon emitter bipolar transistors when a thin interfacial oxide layer is incorporated in the emitter can be explained qualitatively in terms of tunneling through the oxide layer as follows. For *n-p-n* transistors, the collector current I_c is determined mainly by the flow of electrons through the emitter to the base and collector. Considerable evidence has shown that the potential barrier to electrons χ_e associated with the oxide layer is small, the tunnelling probability is high, and so the electron flow is little reduced. Conversely, the base current I_b is determined mainly by the flow of holes from the base into the emitter. The potential barrier to holes χ_h associated with the oxide layer is high, the tunneling probability is low, and so the hole flow is significantly reduced. The current gain is the ratio I_c/I_b and so the gain is increased.

We shall now try to interpret our device results more quantitatively. Yu *et al.*[11] in their theoretical analysis of polysilicon emitter bipolar transistors which incorporated a thin uniform oxide layer within the emitter, obtained the following equation for the base current density J_b:

$$J_b = [qS_{\text{eff}} n_{ie}^2/N_d(w)]\exp(qV_{be}/kT), \qquad (1)$$

where V_{be} is the base/emitter applied voltage, $N_d(w)$ is the emitter carrier concentration at the base/emitter depletion region edge, n_{ie} is the intrinsic carrier concentration of the emitter taking into account band-gap narrowing effects, and S_{eff} is an effective recombination velocity which incorporates the various recombination processes occurring for the holes injected from the base into the emitter. It can be seen that J_b depends directly on S_{eff}, and also on the emitter dopant profile through the parameters n_{ie} and $N_d(w)$. Earlier work[22] showed that an interfacial oxide layer can retard the emitter dopant diffusion, and hence change the final dopant profile. However, for the oxide layer thicknesses considered here, this effect is very small. We shall therefore assume that n_{ie} and $N_d(w)$ are constant, and so variations in J_b can be predicted from changes in the value of S_{eff}.

A simplification of the analysis occurs if carrier recombination in the single-crystal part of the emitter located below the interfacial oxide layer is ignored. In the present work this assumption is justified, partly because the emitter/base junction is only ~100 Å below the oxide layer,[1] and partly because we shall only be considering the change in J_b, rather than its absolute value. The equation for S_{eff} then reduces to[11]

$$S_{\text{eff}} = S_i + \{(1/T_i) + [1/(S_i + S_p)]\}^{-1}, \qquad (2)$$

where S_i is the recombination velocity for holes at the oxide layer/single-crystal silicon interface, T_i is an effective recombination velocity corresponding to the tunnelling of holes through the oxide layer, and S_p is an effective recombination velocity for holes in the polysilicon.

The parameter T_i depends on the oxide layer thickness Δ and is given by[11]

$$T_i = (kT/2\pi m_h^*)^{1/2}(e^{-b_h})(1 - c_h kT)^{-1}, \qquad (3)$$

where

$$b_h = (4\pi\Delta/h)(2m_h^*\chi_h)^{1/2},$$
$$c_h = (2\pi\Delta/h)(2m_h^*/\chi_h)^{1/2},$$

and χ_h is the potential barrier for holes and m_h^* is the effective mass for holes.

To gain a clear insight into the relative importance of the three components of S_{eff}, curves showing the relationship between S_{eff} and Δ were calculated using Eqs. (2) and (3) (Fig. 10). A value for S_p of 1.5×10^5 cm s^{-1} was used, this being calculated by the method of Yu *et al.*[11] for a grain size of 1000 Å using the data listed in Table II. This value may be compared with the range of values of $\sim8\times10^4$ to 2×10^5 cm s^{-1} obtained by Yu *et al.*[11] for similar polysilicon layers with various thicknesses and grain sizes. A value for S_i of 1.5×10^3 cm s^{-1} was assumed, again following Yu *et al.*[11] In order to calculate T_i, a value of χ_h is required. Measurements of χ_h by Ng and Card[27] for oxide layers in the thickness range ~20 to ~26 Å gave values of ~1.0 eV, i.e., considerably less than for thick oxide layers where $\chi_h \simeq 3.0$ eV. In the absence of any experimental values of χ_h for oxide layers of thickness <20 Å, three values have been chosen for our calculations, namely, $\chi_h = 0.5$, 1.0, and 1.5 eV. It was also assumed that $m_h^* = m_0$, the free electron mass.

From Fig. 10 it can be seen that there are three distinct regions of device operation for a polysilicon emitter transistor. For large Δ, $S_{\text{eff}} \simeq S_i$ and is determined mainly by recombination at the oxide layer/single-crystal silicon interface. Other mechanisms such as recombination in the single-crystal part of the emitter and recombination in the base may also contribute to the base current in this region of

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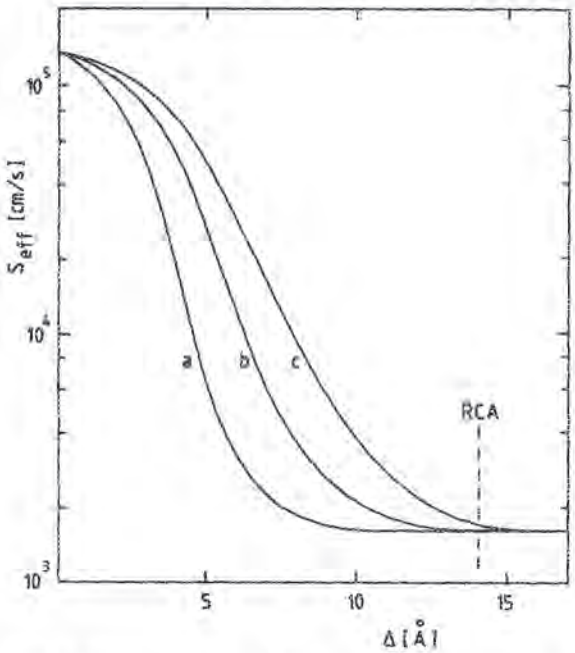

FIG. 10. Theoretical plots of effective recombination velocity (S_{eff}) vs interfacial oxide layer thickness (Δ) for hole potential barriers (χ_h) associated with the oxide of (a) 1.5, (b) 1.0, and (c) 0.5 eV.

operation.[22] For small Δ, most holes tunnel through the oxide layer, $S_{eff} \simeq S_p$ and is determined mainly by transport and recombination in the polysilicon. For intermediate Δ, tunneling through the oxide layer is the dominant mechanism, and S_{eff} is extremely sensitive to small changes in Δ.

Let us initially consider the effect of the interfacial oxide layer on the device operation by comparing the ~10× difference in base current between the RCA- and HF-treated devices given no preanneal, as shown in Fig. 9, with that predicted by Fig. 10. For the RCA-treated devices, the oxide layer is uniform and of thickness ~14 Å. Consequently, Fig. 10 predicts that $S_{eff} \simeq S_i \simeq 1.5\times10^3$ cm s^{-1}, and this value does not depend significantly on the precise value of χ_h. For the HF-treated devices, S_{eff} should then be 10× larger, i.e., ~1.5×10^4 cm s^{-1}. Figure 10 predicts that this would correspond to a uniform oxide layer of thickness ~4 to ~8 Å, the range arising because of the uncertainty in the value of χ_h. This prediction is in reasonable agreement with the observation of a uniform oxide layer of thickness ~4 Å immediately after polysilicon deposition, and a broken up oxide layer of maximum thickness ~8 Å after no preanneal, but a 900 °C drive-in.

TABLE II. Summary of parameter values used to calculate S_p.

Parameter	Value	Reference
Doping concentration $N_d(w)$	5×10^{19} cm^{-3}	1
Diffusion length of holes, L_p	0.7 μm	21
Grain size	0.1 μm	
Hole mobility at grain boundary, μ_{gb}	2 cm^2 V^{-1} s^{-1}	23
Thickness of grain boundary, δ	10 Å	24
Grain boundary interface recombination velocity, S_{gb}	7.5×10^4 cm s^{-1}	25,26
Length of polysilicon emitter track	Large with respect to L_p	

Let us now consider the effect of the interfacial oxide layer on the devices by comparing the ~100× difference in base current between the RCA-treated devices given no preanneal with those given a 1100 °C preanneal. For no preanneal, the oxide layer is continuous and uniform, and $S_{eff} \simeq S_i \simeq 1.5\times10^3$ cm s^{-1}. For a 1100 °C preanneal, the oxide layer is balled-up. If it is assumed that such a balled-up oxide layer has little effect on the flow of holes through the interface, then S_{eff} will correspond to the value for Δ = 0, i.e., to $S_{eff} \simeq S_p \simeq 1.5\times10^5$ cm s^{-1} (Fig. 10). Hence, an increase in base current of ~100× is predicted, in good agreement with the experimental value of ~100× (Fig. 9).

With regard to the effect of the interfacial oxide layer on the RCA-treated devices as the preanneal temperature is progressively increased, comparison of the device results and TEM observations suggest the following behaviors. On going from no preanneal to ~800 °C, I_b is constant and is determined mainly by recombination of holes at the oxide-layer/single-crystal silicon interface (mechanism A). From ~800 to ~925 °C, I_b increases slowly and is determined by mechanism A, together with tunnelling of holes through the thinner portions of the oxide layer (mechanism B). From ~925 to ~975 °C, I_b increases rapidly and is determined by mechanism B, together with an increasing contribution from the flow of holes through the penetrated regions of the oxide layer and the transport properties in the polysilicon layer (mechanism C). From ~975 to ~1100 °C, I_b continues to increase and then approaches a constant value, and is determined mainly by mechanism C, the constant value arising when the oxide layer is completely balled up.

An additional factor that could contribute to the increase in the base current as the preanneal temperature increases is the progressive coarsening of the polysilicon grains that occurs. The grain size for the part of the layer adjacent to the interfacial oxide layer increases from ~400 to ~1000 Å on going from no preanneal to both 1000 to 1100 °C preanneals (Table I). Such coarsening could change S_p, and this would change S_{eff} if Δ were small. The calculations of Yu *et al.*[11] indicate a maximum change in S_p due to this effect of ~2 or ~3×. However, such a change in S_p would have no effect on the ~100× difference in I_b calculated above for the RCA-treated devices on going from no preanneal to a 1100 °C preanneal. This is because for no preanneal, the value of $S_{eff} \simeq S_i$ used is appropriate for a grain size of ~400 Å (S_i corresponds to mechanism A and is independent of grain size), and for a 1100 °C preanneal, the value of $S_{eff} \simeq S_p$ used is appropriate for a grain size of ~1000 Å (S_p was calculated from the data of Table II). However, the coarsening of the grains could slightly affect the shape of the curve of Fig. 9 for the RCA-treated devices on going from no preanneal to a 1100 °C preanneal because mechanisms B and C both depend on the transport properties in the polysilicon layer.

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Let us now consider the effect of the interfacial oxide layer on the devices by comparing the $\sim 5.5\times$ difference in base current between the HF-treated devices given no preanneal with those given a 1000 °C preanneal. It is more difficult to calculate the behavior in this case because the oxide layer is already broken up for no preanneal. Comparison of the device results and TEM observations suggests that on going from no preanneal to ~ 900 °C, I_b is determined by mechanisms B and C; and on going from ~ 900 to ~ 1000 °C, I_b is determined mainly by mechanism C.

In this case the progressive coarsening of the grains could make a contribution to the increase in I_b of $\sim 5.5\times$. This is because over the whole range from no preanneal to a 1000 °C preanneal, the transport properties in the polysilicon layer play a role. The experimental results of Ning and Isaac,[5] performed on what were in effect HF-treated devices, showed that on going from bipolar silicon transistors with polysilicon emitters to analogous devices with single-crystal emitters, the device gain decreased by $\sim 3\times$. These results suggest that in our case, i.e., for polysilicon emitter bipolar transistors given an HF treatment, some of the increse in I_b of $\sim 5.5\times$ is due to the coarsening of the grains and some to the continued breaking up of the oxide layer.

From the above results it might be expected that all devices with oxide layers thicker than ~ 10 Å would give the same best performance. However, although all such devices would possess the same lowest value of S_{eff}, and as a result J_b, the oxide layers introduce a series emitter resistance which increases rapidly with increasing oxide thickness.[11,28] This is detrimental to device and circuit performance, and so in practice a compromise between increased gain and increased emitter resistance needs to be made.

As far as the breakup and eventual balling-up of the thin interfacial oxide layer is concerned, the main driving force is considered to be a significant reduction in the total amount of energy associated with the oxide layer/silicon interface[13,15] (analogous to the well-known Oswald ripening effect that occurs in metallurgical systems). Thus, on going from a continuous uniform oxide layer to a balled-up oxide layer, the interfacial area decreases by typically ~ 5 to $\sim 10\times$ (deduced from TEM examinations). However, the presence of the As dopant can also have an effect. For example, in our work[15,16] on similar specimens post-annealed at 900 °C, the breakup of the oxide layer was found to proceed more rapidly when the As^+ implantation dose was increased from 5×10^{15} to 2×10^{16} cm^{-2}. This result suggests[15] that the As dopant can either enhance the local oxide diffusion rate or change the oxide/silicon interfacial energy.

VI. CONCLUSIONS

A detailed comparison of the electrical and TEM results has revealed that there is a strong correlation between the high gain of polysilicon emitter bipolar transistors and the existence of a continuous, thin, interfacial oxide layer between the single-crystal silicon and the polysilicon. For RCA-treated devices, an initial high gain of ~ 1400 occurs due to the presence of an ~ 14-Å-thick oxide layer. On annealing at temperatures up to 1100 °C, the gain progressively decreased to ~ 40 due mainly to the breaking up of the oxide layer. For HF-treated devices, an initial gain of ~ 240 occurs due to the presence of a thinner and already partly broken up oxide layer. On annealing at temperatures up to 1000 °C, the gain decreases to ~ 50 due to further breaking up of the oxide layer together with a coarsening of the polysilicon grains. The decrease in gain observed with increasing anneal temperture is explained using a theoretical model in which tunneling through the interfacial oxide is an important mechanism. As demonstrated by other authors,[11,28] if the oxide layer is too thick, it contributes a significant series resistance to the emitter structure. Therefore, in order to obtain the optimum device, it is necessary to produce an extremely thin continuous oxide layer, and to prevent it from breaking up during the device fabrication. The thinner the oxide layer, the more readily it breaks up, and the more critical the device processing procedures become.

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