

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANADIAN SOLAR (USA) INC.,

Petitioner,

v.

FIRST SOLAR, INC.

Patent Owner.

Patent No. 9,130,074

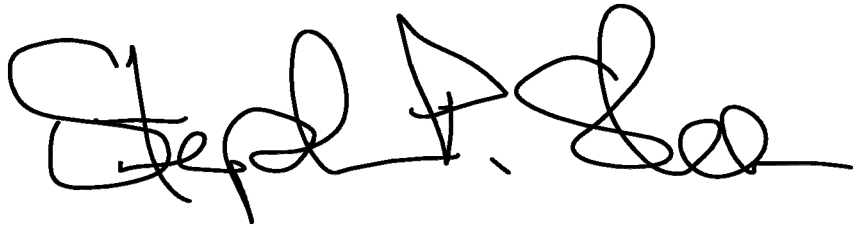
Title: High-Efficiency Solar Cell Structures and Methods of Manufacture

Inter Partes Review No. IPR2025-01432

**DECLARATION OF STEPHEN SHEA REGARDING
U.S. PATENT NO. 9,130,074**

I, Stephen Shea, do hereby declare and state that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 22, 2025

A handwritten signature in black ink, appearing to read 'Stephen P. Shea', with a stylized, cursive script.

Stephen P. Shea, Ph.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
A.	Engagement	1
B.	Background and Qualifications	1
C.	Compensation and Prior Testimony	4
D.	Information Considered.....	4
II.	LEGAL STANDARDS FOR PATENTABILITY	5
A.	Anticipation	7
B.	Obviousness.....	8
III.	THE 074 PATENT.....	14
A.	Effective Filing Date of the 074 Patent.....	14
B.	Person of Ordinary Skill in the Art	14
C.	Overview of the 074 Patent	15
D.	The Prosecution History	22
E.	The 074 Patent Claims	26
F.	Claim Construction	27
IV.	BACKGROUND OF THE TECHNOLOGY.....	28
A.	Basic Solar Cell Configuration	28
B.	Solar Cell Operation.....	33
C.	Doping Methods	35
D.	State of the Art	38
V.	DETAILED OVERVIEW OF THE PRIOR ART	40
A.	Yablonovitch (EX1005)	40
B.	Kwark (EX1006)	47
C.	Froitzheim (EX1008)	52
D.	Neville (EX1009)	55
E.	Sasaki (EX1010).....	56

VI.	CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM AND YABLONOVITCH.....	58
A.	The Combination of Froitzheim and Yablonovitch	58
B.	Modifying Froitzheim with SIPOS and Interfacial Oxide Layer.....	61
C.	Reasonable Expectation of Success	67
D.	Froitzheim and Yablonovitch Disclose All Claim Limitations	71
1.	Claim 1(a) – Preamble	71
2.	Claim 1(b) – Central Substrate.....	72
3.	Claim 1(c) – Interface Passivation Layer.....	74
4.	Claim 1(d) – Conductive and Passivating Layer	78
5.	Claim 1(e) – Thermal Treatment	83
6.	Claim 1(f) – Metallization.....	89
7.	Claim 2 – Antireflective Layer	100
8.	Claim 4 – Perforation.....	104
9.	Claim 5 – Crystallization	107
10.	Claim 6 – Transmissivity	109
11.	Claim 7 – Dopant Activation	112
12.	Claim 8 – PN Junction	114
VII.	CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, YABLONOVITCH, AND NEVILLE.....	116
VIII.	CLAIM 2 IS UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, YABLONOVITCH, AND SASAKI.....	118
A.	The Combination of Froitzheim, Yablonovitch, and Sasaki.....	118
B.	Sasaki Discloses the Method Step of Claim 2	119
C.	Motivation to Combine Froitzheim and Yablonovitch with Sasaki’s ITO Film	121
D.	Reasonable Expectation of Success	124
IX.	CLAIMS 1-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM AND KWARK	125
A.	The Combination of Froitzheim and Kwark	125

B.	Modifying Froitzheim with SIPOS/Polysilicon and Interfacial Oxide Layer	127
C.	Reasonable Expectation of Success	134
D.	Froitzheim and Kwark Disclose All Claim Limitation	139
1.	Claim 1(a) – Preamble	139
2.	Claim 1(b) – Central Substrate.....	139
3.	Claim 1(c) – Interface Passivation Layer.....	140
4.	Claim 1(d) – Conductive and Passivating Layer	143
5.	Claim 1(e) – Thermal Treatment	147
6.	Claim 1(f) – Metallization.....	153
7.	Claim 2 – Antireflective Layer	158
8.	Claim 3 – Separation.....	160
9.	Claim 4 – Perforation.....	164
10.	Claim 5 – Crystallization	168
11.	Claim 6 – Transmissivity	171
12.	Claim 7 – Dopant Activation	174
13.	Claim 8 – PN Junction	176
X.	CLAIMS 1-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, KWARK, AND NEVILLE	178
XI.	CLAIM 2 IS UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, KWARK, AND SASAKI.....	179
A.	The Combination of Froitzheim, Kwark, and Sasaki.....	180
B.	Sasaki Discloses the Method Step of Claim 2	181
C.	Motivation to Combine Froitzheim and Kwark with Sasaki’s ITO Film.....	182
D.	Reasonable Expectation of Success	184
XII.	OBJECTIVE FACTORS.....	185

Attachment A. Materials Relied On

I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Petitioner Canadian Solar (USA) Inc. (“Petitioner”) as an expert witness in the above-captioned proceeding. I have been asked to provide my opinions about the state of the art of the technology related to U.S. Patent 9,130,074 (the “074 Patent”) (EX1001) and on the patentability of claims 1-8 of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I have summarized in this Section my educational background, career history, and other relevant qualifications. A full and accurate description of my educational background, professional experience, and qualifications is set forth more fully in my curriculum vitae, which is attached to this Declaration as EX1004.

3. I received a Bachelor of Science degree in Engineering Science and a Bachelor of Arts degree in English Literature from Swarthmore College. I then received a Master of Electrical Engineering degree, and subsequently obtained my Ph.D. in Applied Sciences-Electrical Engineering from the University of Delaware. My research for both the Masters and the Ph.D. was on thin film photovoltaic cells.

4. I have worked in the solar PV field since 1981, working for several large solar cell, panel and system manufacturers as an engineer, manager, and

executive. During my 40+ year career, I have worked in and managed many facets of the solar cell and module manufacturing processes, including research and development, manufacturing process development, factory construction, launch, expansion and upgrade, engineering, and operations management, as well as system performance modeling and design.

5. For example, I worked for nearly ten years at Suniva Inc., where I served as Vice President, Chief Engineering Officer and Vice President of Manufacturing. While I was at Suniva (2007-2016), it became a leading American manufacturer of high-efficiency solar cells and modules. While there, I was responsible for guiding the company's next generation technology, from the research and development in the laboratory all the way through the manufacturing process. This included the design and construction of the manufacturing facility and the creation and management of the manufacturing organization itself. I also designed a complete factory renovation that expanded Suniva's production to triple the existing capacity and transition to next-generation Passivated Emitter, Rear Contact (PERC) process technology.

6. Prior to my time at Suniva, I worked for Solarex which became, via merger, BP Solar, for 20 years. I began, shortly after finishing my Ph.D., as a Staff Scientist, responsible for development and deployment of new PV cell technology into manufacturing, leading the transition of the manufacturing process from a

highly expensive technology adapted from processes used for satellite power systems to the far less expensive screen printed metal contact technology still used today. In my twenty years at Solarex/BP Solar I advanced through various roles in Process Development, Process Engineering and Technology Development, ultimately serving as the Directory of Technology for crystalline silicon worldwide. In this role I was responsible for all advanced technology and new product development and deployment for the Crystalline Division of the new company, including factories in: Frederick, Maryland; Sydney, Australia; Bangalore, India; and several sites in Madrid, Spain. My responsibilities at Solarex/BP Solar included all aspects of R&D, process deployment, manufacturing and equipment engineering and large-scale manufacturing process management and control.

7. I also worked for another solar start-up company, Beamreach Solar, as the Vice President, Cell Engineering and Operations. As an executive at Beamreach, I oversaw R&D, facilities and operations groups, leading the development of a proprietary, manufacturable, low-cost interdigitated back contact (IBC) cell structure.

8. I have also done extensive R&D work with a wide variety of thin-film materials through doctoral and later work at the University of Delaware's Institute of Energy Conversion and have experience in materials characterization using

scanning electron microscopy (SEM); secondary ion mass spectrometry (SIMS); xray diffraction (EDS/EDAX).

9. I am the author of over 20 papers and several patents and applications in the field of photovoltaics.

C. Compensation and Prior Testimony

10. I am being compensated at a rate of \$450.00-\$500.00 per hour for my time spent on this matter. I am also being reimbursed for reasonable and customary expenses associated with my work in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

11. I have previously provided expert testimony before the US International Trade Commission and in other Inter Partes Review, as listed in my CV, EX1004.

D. Information Considered

12. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this declaration and those listed as exhibits in Attachment A to this declaration.

13. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional

documents and information in forming any necessary opinions—including documents that may not yet have been provided to me.

14. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

15. I am not a lawyer and am not providing any legal opinions. In providing my opinions in this declaration, I am relying upon certain basic legal principles that have been explained to me by counsel as summarized below.

16. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

17. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

18. I understand that in this proceeding the Petitioner has the burden of proving that the claims are anticipated by or obvious from the prior art by a

preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

19. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. In particular, I understand that claims must be interpreted in view of the teachings of the specification and that the prosecution history can inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, thus making the claim scope narrower. The claims after being construed in this manner are then to be compared to the information in the prior art.

20. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

21. I understand that there are various ways in which prior art may render a patent claim unpatentable based on prior art patents and printed publications. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. My understanding of the legal standards is set forth below.

A. Anticipation

22. I understand that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art.

23. I have applied these standards in my evaluation of whether the claims would have been anticipated by the prior art.

24. I understand that the “prior art” includes patents and printed publications that existed before the earliest filing date (the “effective filing date”) of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

25. I understand that, for a patent claim to be “anticipated” by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are “inherent” to the thing or process being described in the prior art. I understand that a limitation can be “inherent” if that limitation is necessarily present in or the natural result of the elements explicitly disclosed by the prior art.

26. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

27. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

28. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

29. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)¹) as follows:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

30. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my

¹ I understand from counsel that the pre-America Invents Act (“AIA”) versions of 35 U.S.C. §§ 102 & 103 apply to these proceedings.

evaluation of whether the claims would have been considered obvious as of the priority date of the patent.

31. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

32. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

33. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this

evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention.

34. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I understand that when the prior art does not expressly disclose a claim limitation, inherency may also supply a missing claim limitation in an obviousness analysis. I understand that inherency is established in the context of obviousness when the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

35. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other

device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

36. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

37. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents/publications; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

38. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that KSR confirms that any motivation that would have been

known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined. However, I understand that the mere fact that two elements are known in the prior art does not mean that the combination is obvious; there must still be a motivation to combine these elements.

39. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents/publications together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

40. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

41. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or leads away from the line of inquiry disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (e.g., because it would not work or explicit statements saying the combination should not be made).

42. I understand that a person of ordinary skill is also a person of ordinary creativity.

43. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem

and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 074 PATENT

A. Effective Filing Date of the 074 Patent

44. The 074 Patent, titled “High-Efficiency Solar Cell Structures and Methods of Manufacture,” was filed on April 21, 2010. EX1001. Based on the information on the face of the 074 Patent, it claims priority to a provisional patent application filed April 21, 2009. I have been instructed by Petitioner’s counsel to assume that April 21, 2009, is the earliest effective filing date of the 074 Patent for purposes of this proceeding.

B. Person of Ordinary Skill in the Art

45. From my review of the 074 Patent specification and claims 1-8, and based on my experience in the field and the information disclosed in the 074

Patent, I believe that a person of ordinary skill in the art in the 074 Patent's field of solar cell design or manufacture in April 2009 ("Skilled Artisan") would have been someone with an master's degree involving the disciplines of electrical engineering, physics, chemistry, or materials science, or a degree in an equivalent field, and at least two years of experience designing, developing, or researching in the field of solar cell design and manufacture. Alternatively, that person would have had a bachelor's degree in electrical engineering, physics, or materials science, and at least four years of experience designing, developing, or researching in the field. By that definition, I qualify as a Skilled Artisan before April 21, 2009, the earliest effective filing date of 074 Patent.

C. Overview of the 074 Patent

46. The 074 Patent discloses a method of manufacturing a solar cell, like the cell depicted in Fig. 6.

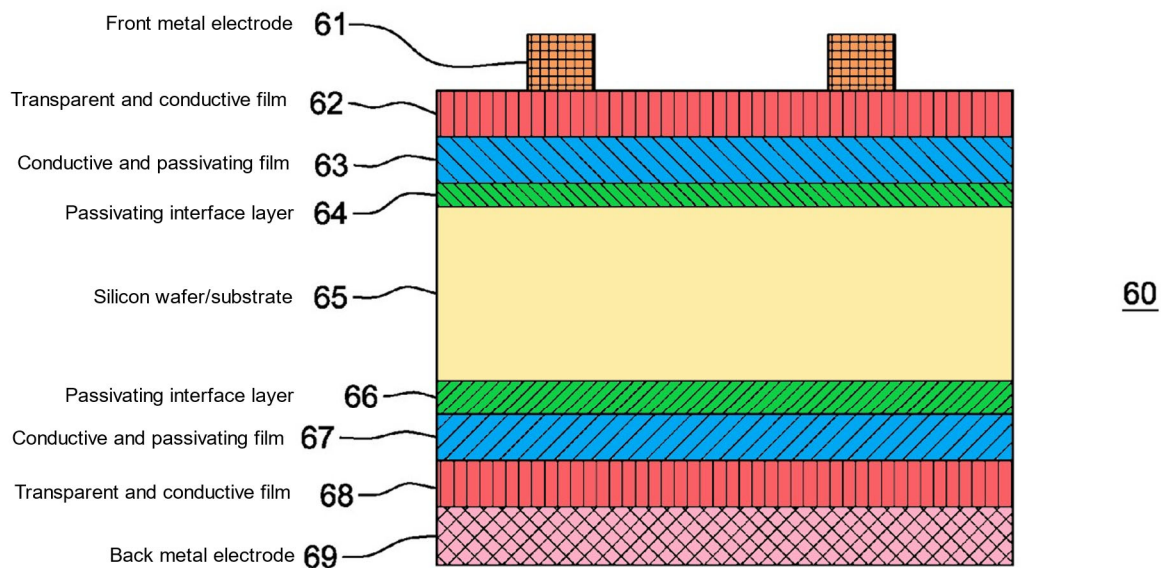


FIG. 6

47. The solar cell of Fig. 6 has “an n-type front, n- or p-type wafer, and p-type back.” EX1001, 074 Patent at 5:14-15. An n- or p-type crystalline silicon wafer forms the cell’s substrate. *Id.* at 5:62-65. On either side of the substrate are “electrically passivating interface layers” 64 and 66, which are less than 10nm thick. *Id.* at 5:56-61, 5:66-6:4. The 074 Patent identifies silicon oxide, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon, aluminum oxide, aluminum nitride, phosphorus nitride, and titanium nitride as possible materials for the “electrically passivating interface layers.” *Id.* at 5:56-61, 5:66-6:4.

48. Next, “electrically passivating and conductive films” 63 and 67 are formed on the electrically passivating interface layers 64 and 66, respectively. *Id.* at 5:42-55, 6:5-17. In the embodiment shown in Fig. 6, electrically passivating and conductive film 63 is highly n-doped and can be made of several materials, including: “amorphous or polycrystalline silicon carbides; “amorphous or polycrystalline silicon;” or “amorphous or poly-crystalline diamond-like carbon.” *Id.* at 5:45-53. In addition, any of these materials can include oxygen or hydrogen, e.g., “n-doped $\text{SiC}_x\text{O}_y\text{H}_z$; n-doped $\text{SiN}_x\text{O}_y\text{H}_z$ ”. *Id.* at 5:54-55. Electrically passivating and conductive film 67 is highly p-doped but can otherwise be made of the same materials as film 63. *Id.* at 6:5-17.

49. After that, “transparent and conductive films” 62 and 68 are formed on electrically passivating and conductive films 63 and 67, respectively. *Id.* at 5:32-41, 6:16-24. The transparent and conductive films 62 and 68 can be made of various exemplary “transparent conductive oxides,” such as indium tin oxide. *Id.* at 5:37-41, 6:20-24. The ’074 Patent elsewhere states that the formation of transparent and conductive films 62 and 68 may include “a low reflective index layer for a good internal mirror on the back—refractive index basically smaller than 3.0, smaller than 2.6, smaller than 2.0, smaller than 1.5.” *E.g., id.* at 15:22-35.

50. On the front transparent conductive film 62, a front metal electrode 61 is formed. *Id.* at 5:31. As shown in Fig. 6, the front metal electrode 61 is localized

and does not cover the entire front surface of the solar cell. On the back transparent conductive film 68, a back metal electrode 69 is formed. *Id.* at 6:25. Unlike the front electrode, the back electrode is shown covering the entire back surface of the solar cell in Fig. 6. According to the 074 Patent, metal electrodes 61 and 69 “ha[ve] the benefit that the metal does not need to penetrate underlying layers before it contacts the wafer.” *Id.* at 5:16-19.

51. The 074 Patent describes a process for forming the solar cell in Fig. 6 above, though I discuss only certain aspects here. *See id.* at 15:5-21. First, the 074 Patent notes that most of the layers above can be formed from any of a number of well-known formation techniques (15:54-56):

Most layers within the solar cell structures described above can be deposited or grown with methods such as PECVD, APCVD, LPCVD, PVD, plating etc.

52. Second, the 074 Patent describes a “thermal treatment” process at “500°C or more” which causes amorphous silicon layers to crystallize into polycrystalline silicon (*id.* at 16:3-29):

In the described cell structures, amorphous silicon layers can be turned into polycrystalline silicon layers by thermal treatment. This also holds true for doped amorphous silicon layers or compounds of amorphous silicon carbides, etc. This crystallization negatively affects the passivation quality of the silicon/amorphous silicon interface layer (if it exists in the cell structure). However, layers xx4 and xx6 buffer the wafer surface from the crystallized polysilicon layer. Therefore, the interface is

still passivated after the thermal treatment and the layer systems are stable at the thermal-treatment temperature.

In accordance with the present invention, during the crystallization process many properties of the layer change: Donors or acceptors get activated, the optical transmission increases, hydrogen effuses from the layer. The thermal treatment may activate doping atoms in the compound and result in diffusion of dopant atoms into a substrate wafer to provide a high-low junction or a p-n junction....

Thermal treatment at 500° C. or more therefore comprises an aspect of the present invention.

The 074 Patent further explains that during the thermal treatment, oxygen incorporated into a deposited amorphous silicon layer migrates towards the interface with the silicon substrate, forming a thin oxide layer (*id.* at 16:38-42):

If the layer composition is chosen correctly, a layer deposited in a single process can split into two (or more) layers. The incorporated oxygen in the amorphous deposited layer migrates toward the silicon interface and a thin oxide can be grown.

53. The 074 Patent also discusses the trajectory of current flow in various solar cell configurations:

In a front junction cell the minority carriers (in the case of a p-type wafer these are electrons) are collected on the side of illumination. In a back junction cell the minority carriers are collected at the side opposed to the illumination. Current flow patterns are shown generally in the partial cross-sectional solar cell views of FIGS. 2-5 for p-type and n-type wafers.

Id at 4:29-35.

54. For example, “FIG. 4 [reproduced below] shows carrier flow for a solar cell 40, in which minority carriers (solid lines) flow to front electrodes 41 from an n-type wafer 45 having a front junction.” *Id.* at 4:52-54. According to the 074 Patent, the minority carriers (holes) “need to use the lateral flow [red solid lines] within the thin p-type emitter, 42 to reach the electrodes 41,” and this lateral flow determines resistive losses. *Id.* at 4:54-57. By contrast, the majority carriers (electrons) “can use the shortest geometrical path to the full area back electrode 49,” shown by the dashed blue lines. *Id.*

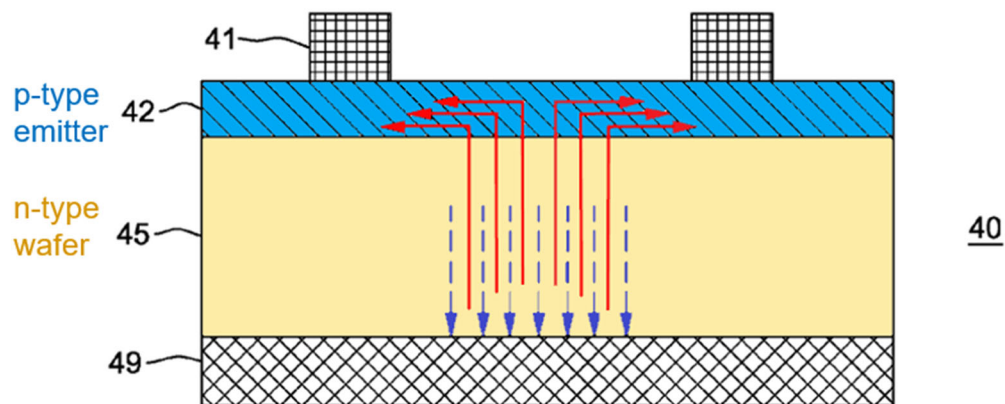


FIG. 4

The full paragraph describing Fig. 4 is reproduced here (*id.* at 4:52-59):

FIG. 4 shows carrier flow for a solar cell 40, in which minority carriers (solid lines) flow to front electrodes 41 from an n-type wafer 45 having a front junction. The holes need to use lateral flow within the thin p-type emitter 42 to reach the electrodes 41, and the lateral conductivity of the emitter determines the resistive losses. The majority carriers (dashed lines) can use the shortest geometrical path to the full area back electrode 49.

55. By contrast, Fig. 5 shows the carrier flow for an n-type wafer with a back junction. *Id.* at 4:60-61. According to the 074 Patent, the “[t]he majority carriers [electrons] (dashed lines) can use the entire wafer conductivity to reach the front electrodes 51.” *Id.* at 4:61-63. In addition, the minority carriers (holes) “can use the shortest geometrical path to reach the rear p-type emitter 58,” such that their trajectory is mostly vertical instead of lateral, reducing resistance due to lateral motion. *Id.* at 3:63-67. Eliminating the lateral flow thus shortens the carrier flow path.

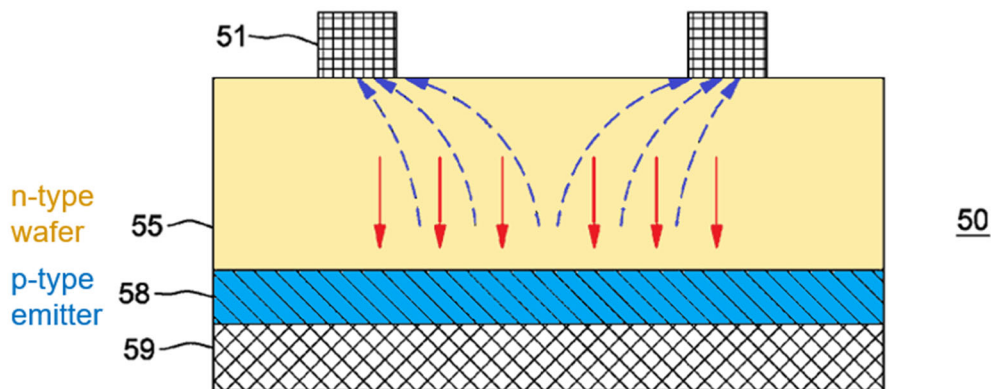


FIG. 5

The full paragraph describing Fig. 5 is reproduced here (*id.* at 4:60-67):

FIG. 5 shows carrier flow for a solar cell 50 from an n-type wafer 55 having a back junction. The majority carriers (dashed lines) can use the entire wafer conductivity to reach the front electrodes 51. The minority carriers (solid lines) can use the shortest geometrical path to reach the rear p-type emitter 58, and their transport within the emitter is vertical instead of mainly lateral. This back junction structure reduces the requirements for lateral conductivity of the emitter layer.

56. Comparing the solar cells in Fig. 4 and Fig. 5, the '074 Patent explains that the back junction cell in Fig. 5 is advantageous over the front junction cell in Fig. 4 because the *minority carriers* (electrons) can flow directly vertically to reach the rear contact, instead of horizontally, reducing path resistance (*id.* at 5:1-1) (emphasis added):

A back junction cell with a full area back contact has the advantage that the minority carriers do not have to flow laterally through the emitter to reach the contacts, their transport within the emitter is mainly vertical. This reduces the losses associated with the lateral transport of the minority carriers within the emitter. Since the **full contact area coverage is a requirement to benefit from this property** of the structure, a shielded contact is important, e.g., **since the metal contacts the layer everywhere (“full area contact coverage”)**, there is no need for the minority carriers to flow laterally toward the nearest contact, like they do within the emitter in, e.g., FIG. 4.

The 074 Patent further observes that “full contact area coverage is a requirement” for a solar cell to achieve this benefit of reduced resistance. *Id.* In other words, without a rear electrode covering the entire back surface of a back junction solar cell, minority charge carriers do not follow the shortest charge carrier path.

D. The Prosecution History

57. I have also reviewed the prosecution history of the 074 Patent to understand what the Examiner had considered during prosecution and the reasons

why the claims were allowed. I recite below a summary of the prosecution history of the 074 Patent. During prosecution, claim 1 initially recited:

A method of fabricating a solar cell, comprising:

providing a wafer as a central substrate;

depositing or growing at least one interface passivation layer over the substrate;

depositing at least one conductive layer over the passivation layer(s);

providing thermal treatment; and

providing metallization as electrodes.

EX1002 at 125.

58. The Examiner initially rejected the claims as anticipated by WO2008/115814 (“Carlson”) and also by US6,821,875 (“Wenham”). *Id.*, 274. In response, the Applicant amended claim 1:

- First, the amended claim required the “conductive layer” to *also* have a “passivating” function, and to “comprise a dopant.”
- Second, the amended claim required the thermal treatment to be at 500°C or higher and to render two effects: “crystallizing, at least in part, the at least one conductive and passivating layer” and “facilitating diffusion of the dopant through the at least one interface passivation layer.”
- Third, the amended claim required the metallization as electrodes to be “over the at least one conductive and passivating layer”.

Id. at 367.

59. With these modifications, the Applicant argued that the “at least one conductive and passivating layer comprising a dopant deposited on at least one interface passivating layer over a substrate” is “itself believed to be novel.”

EX1002 at 371. The Applicant further argued that “[a] layer combining both conductive and passivating functions/features does not appear in the applied art” and this layer “provides both electrical conductivity to allow current flow as well as surface passivation to prevent carrier recombination.” *Id.*

60. As to the thermal treatment, the Applicant argued that this also “distinguish[es] amended claim 1 over the applied art.” *Id.* at 372. The thermal treatment, according to the Applicant, “preserves or improves the passivating qualities of the conductive and passivating layer through its crystallization ... and at the same time allows the dopant diffusion out of the conductive and passivating layer through the interface passivation layer(s).” *Id.*

61. Finally, regarding metallization, the Applicant argued that the claimed method allows the metal electrodes to be “provided over the conductive and passivating layer ... without the need for a protective dielectric layer, or the need to create openings or firing holes through multiple layers of the solar cell to permit contact between metal electrodes and semiconductor substrate.” EX1002 at 373. That is, the metal “can be deposited directly on the conductive and passivating

layer(s)” or “additional conductive layers can optionally be placed over the conductive and passivating layer with metallization provided over the additional conductive layers.” *Id.*

62. After this response, the Examiner issued a Final Office Action rejecting the amended claims as obvious over Wenham in view of US2009/0235972 (“Fukushima”)², and as further obvious over US6,210,991 (“Wenham II”) in view of Fukushima. *Id.* at 415, 417. In response, the Applicant further amended Claim 1. *Id.* at 466-67.

63. In the remarks accompanying the amendment, the Applicant continued to argue that Wenham “nowhere discloses providing a conductive and passivating layer comprising a dopant on an interface passivation layer.” *Id.* at 469. The Applicant further argued that Wenham and Wenham II “do not disclose providing thermal treatment to crystallize a conductive and passivating layer and facilitate diffusion of a dopant from a conductive and passivating layer throughout an interface passivation layer.” *Id.* at 470. In addition, the Applicant argued that its method of diffusing the dopant from the conductive and passivating layer through the interface passivating layer “enable[s] charge carrier flow paths through the conductive and passivating layer and the interface layer” resulting in the substrate

² The Fukushima publication was used as a translation for WO 2007/125903.

and the electrodes “having direct electrical connectivity flow paths through the intervening layers of the solar cell via the diffused dopant.” *Id.* at 472. This allows for the “metallization as electrodes” to be formed after the thermal treatment, without the metal material needing “to penetrate through one or more other layers of the solar cell to make contact with the solar cell substrate.” *Id.* at 471.

64. Based on these comments, the Examiner accepted the Applicant’s arguments and initiated an interview to suggest certain amendments that “would bring the application into condition for allowance.” *Id.* at 483. In the Notice of Allowance, the Examiner made no mention of Wenham, Wenham II, or Fukushima, but instead discussed two additional references—a publication by Bau and US Patent No. 7,202,143 to Naseem. *Id.* at 485-86 The Examiner stated, “there is no teaching or motivation to provide metallization as electrodes which directly contact the conductive and passivation layer, as that layer supports a layer which forms the absorbing portion of the solar cell.” *Id.* at 485.

E. The 074 Patent Claims

65. Claim 1 of the 074 Patent recites:

Claim Element	Claim Language
[1.a]	A method of fabricating a solar cell, comprising;
[1.b]	providing a wafer as a central substrate;

[1.c]	depositing or growing at least one amorphous interface passivation layer over the substrate;
[1.d]	depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant;
[1.e]	providing thermal treatment at a temperature of about 500° C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and
[1.f]	providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.

F. Claim Construction

66. For purposes of my opinions in this proceeding, I applied each claim term's ordinary and customary meaning to the Skilled Artisan read in light of the specification and prosecution history.

IV. BACKGROUND OF THE TECHNOLOGY

A. Basic Solar Cell Configuration

67. A solar cell is a device that turns sunlight into electrical current. A solar cell typically has multiple layers of silicon and other materials, each of which serves a particular purpose. The side of a solar cell that faces the sun is conventionally referred to as the front side of the solar, and the side of the solar cell that faces away from the sun is the back or rear side.

68. The most part, or “bulk” of a solar cell is the base layer of silicon, known as the wafer or substrate, on which the other layers are formed. Two variants of silicon are commonly used for the substrate: (i) silicon that has a monocrystalline lattice; and (ii) multicrystalline silicon, in which there are many regions of crystalline silicon that are not aligned to each other.

69. Impurities called “dopants,” usually boron or phosphorus, can be introduced into silicon to alter the silicon’s conductive properties in a process known as “doping.” EX1018-Quirk, 34-38. When a boron atom replaces a silicon atom in a crystalline lattice of silicon, for example, the boron atom has one fewer valence electron than does the silicon atom it replaces, thus leaving behind a positively charged vacancy or “hole” in the crystal lattice at that point. *Id.*, 36-37. Because a hole represents the absence of an electron, a hole is often modeled as a positively charged “virtual” particle. Although the hole is not an actual particle but

is rather a positively charge vacancy that is fixed in one place and into which an electron can flow, it conveniently behaves mathematically exactly like a positively charged particle whose “flow” can be modelled mathematically with the same equations used for electron flow, but with slightly different effective mass and opposite (positive) charge. The equations for electron and “hole” flow are complementary. As free electrons migrate out of one vacancy and into another, this behavior looks as if the positively charged vacancy is actually moving in the opposite direction. For this reason, silicon doped with boron is known as a positive-type or “p-type” semiconductor material, a material in which electrical current is carried by these virtual P-Type carriers. *Id.* Conversely, phosphorus has one more valence electron per phosphorus atom than does silicon, and in silicon doped with phosphorus electrical current is carried by these actual, negatively charged carriers as it would be in a metallic conductor. Phosphorus doped silicon is therefore known as an “n-type” material or negative-type material. *Id.*, 36.

Techniques for doping silicon and polysilicon layers were well established by the late 20th century.

70. When n-type and p-type layers or regions are adjacent to one another, they form a “pn junction.” EX1019 (Luque) at 83. As excess electrons migrate (or “diffuse”) from the n-type region across the pn junction to the p-type region, they become trapped in holes in the p-type region, and vice versa. *Id.* The region where

the holes and electrons become trapped is known as the “depletion region,” as it is “depleted” of free carriers of either type. As a result of these fixed charges, a voltage develops across the pn junction that can be used to drive current through a connected circuit. *Id.* In solar cells, the pn junction is often created by doping the bulk of the substrate to be either uniformly p- or n-type, (known as the base or “absorption region”), and forming an “emitter” layer or region with the opposite dopant type either on or within the bulk region. *Id.* The figure from Luque (EX1019) below depicts a basic schematic of a solar cell with a pn junction formed from a p-type base region on the right, and an n⁺-doped³ emitter on the left. *Id.*

³ The n⁺ nomenclature refers to an n-type region that is *heavily* doped with n-type dopants compared to the base doping concentration.

EX1019, Luque Fig. 3.13

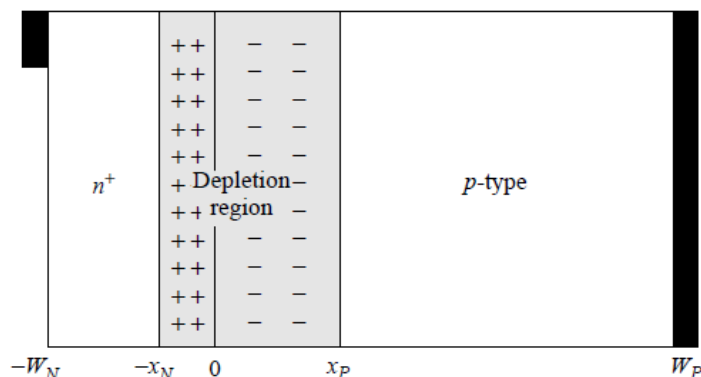


Figure 3.13 Simple solar cell structure used to analyze the operation of a solar cell. Free carriers have diffused across the junction ($x = 0$) leaving a space-charge or depletion region practically devoid of any free or mobile charges. The fixed charges in the depletion region are due to ionized donors on the n -side and ionized acceptors on the p -side

71. While the figure above from EX1019 (Luque) depicts a p -type base region and an n -type emitter layer, the polarity of a solar cell can be reversed because of the complementarity of the electron and hole physics discussed just above. In other words, a solar cell like the one above from Luque could instead have an n -type base region and a p -type emitter. For example, the figure below comes from a 1995 textbook and shows various types of solar cell configurations, including the highlighted cell with a pn junction on the back of the solar cell. EX1009-Neville at 200. As shown, for each configuration there are two possible arrangements: (1) the solar cell can have a p -type base and an n -type emitter, or (2) a n -type base and a p -type emitter. *Id.*

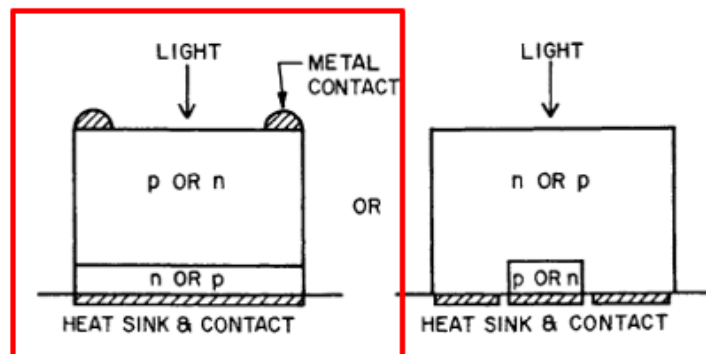
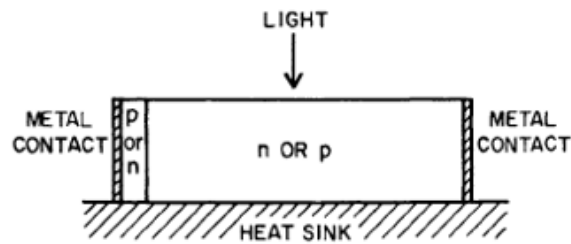
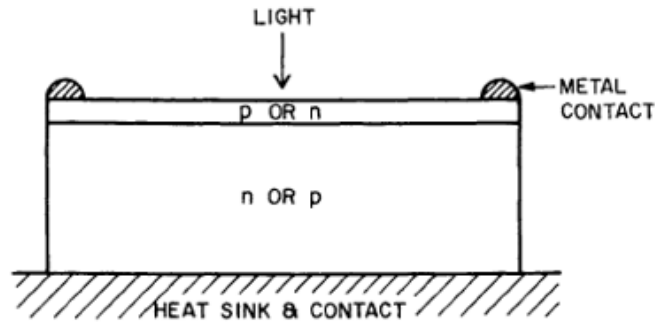


Figure VI.1. PN and heterojunction solar cell-light configurations.

In general, whether to implement a solar cell with a p-type base substrate and an n-type emitter, or vice versa, always represents a limited universe of options that would have been well known to Skilled Artisans researching and designing solar cells.

72. In addition to an emitter, a solar cell can be fabricated with a thin “surface field,” which is a layer or region that has the *same* dopant type as the adjacent silicon layer, but is more heavily doped. EX1019-Luque at 88. Using Figure 3.13 from Luque above as an example, a surface field could be formed on the right side of the substrate by forming a p^+ -type layer. Since in this figure the surface field would be on the side of the solar cell deployed opposite the sun, this layer would be called a Back Surface Field (BSF). In some solar cell configurations, A Front Surface Field (FSF) is also possible.

B. Solar Cell Operation

73. When solar radiation reaches a solar cell, photons with energy greater than a critical energy level known as the bandgap can excite valence electrons, which are relatively lightly bound to atoms, enough to free the electrons. The location vacated by a freed electron now becomes a hole, and this phenomenon is said to create an electron/hole pair. In a P-Type material, the freed electrons are called “minority” carriers, since the majority of electrical current is carried by the dopant holes, and in an N-Type material, the freed electrons in motion are modeled as the motion of the virtual holes, which are in this case the minority carrier. The freed electrons and holes are mobile and move through the silicon randomly until they either meet an opposite carrier and again become bound by a local atom or until they reach the high electric field of the depletion region surrounding the PN

junction, in which case minority electrons from the P-Type region are swept by the electric field into the N-Type Region (where they are now majority carriers), while minority holes from the N-Type region are swept by the electric field into the P-Type region (where they are also now majority carriers). Because of the potential difference across the pn junction, if an external conductive circuit is provided connecting the N-Type and P-Type regions the electrons flow out of the n-region into one or more electrodes and the holes flow out of the p-region into one or more electrodes resulting in the flow of electrical current.

74. It is a common goal of solar cell designers to increase solar cell efficiency. The more electrons and holes that are able to reach the respective electrodes relative to the amount of light the cell receives, the greater the total current generated and the more efficient the solar cell. However, when a free electron or hole meets a fixed charge of the opposite type before reaching the depletion region, it will again become bound to a local atom and no longer contribute to electrical conduction. This process is known as “recombination,” because the free actual electron fills the fixed virtual hole and both seem to disappear as far as electrical conduction is concerned, and reduce the photo-generated current. EX1019-Luque at 74.

75. Various mechanisms can lead to increased electron/hole recombination. Because dissimilar materials can have different crystalline

structures, the interface where two dissimilar materials meet may have crystalline defects that are more prone to recombination, for example. *See id.* at 77. Surfaces are inherently disordered, as a surface is where the crystal structure ends, leaving unsatisfied atomic bonds that facilitate recombination. Such “surface recombination” is a highly studied phenomenon, and various methods have been developed to reduce the level of surface recombination that occurs across the material interfaces in a solar cell. For example, “surface passivation” is a strategy in which particular materials are chosen in such a way that the crystalline mismatch across interfaces is smoothed over, such as by forming silicon dioxide SiO₂ on silicon to reduce dangling silicon bonds. EX1018-Quirk at 227. “Passivation” thus reduces recombination, which impacts solar cell efficiency. Because a solar cell is a very thin device with a high surface to volume ratio, the minimization of surface recombination is always a critical feature of device design.

C. Doping Methods

76. Dopants can be driven into silicon using a variety of methods. For example, silicon can be doped via thermal diffusion by exposing a silicon wafer/substrate to a dopant vapor at a high temperature, which causes the dopants in the gas to diffuse into the silicon, as shown below in a figure from a textbook by Quirk and Serda. EX1018-Quirk, 478, Fig. 17.3 (reproduced below). Another

method of doping is ion implantation, which involves bombarding a substrate with high energy dopants. *Id.* at 475.

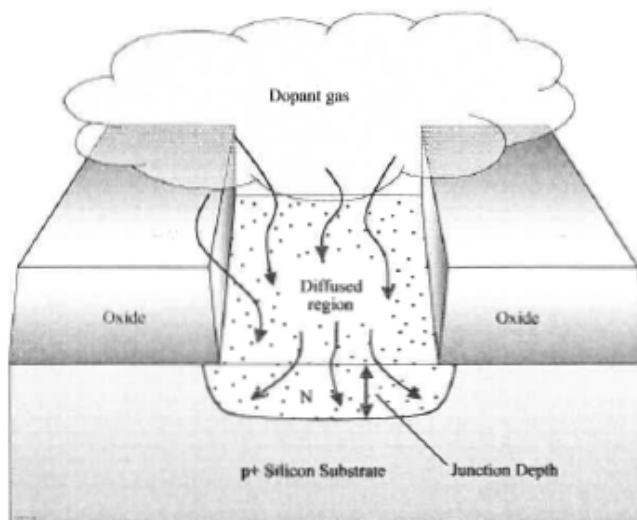


FIGURE 17.3 Doped Region in a Silicon Wafer

77. For chemical vapor deposition of silicon layers, doping can be achieved by adding the dopant into the mixture of gases used in the deposition. In turn, another technique for driving dopants into a silicon wafer/substrate known years before the 2009 effective filing date of the 074 Patent involves forming or placing a highly doped silicon layer material (e.g., doped polysilicon) onto a substrate and heating the cell up such that dopants' thermal energy causes them to outdiffuse from the silicon layer and into the substrate. This process is described, for example, in a 1992 article published in the IEEE journal Transactions on Electron Devices:

Several types of polysilicon emitter have been studied in the literature, as illustrated in Fig. 1.... The second type of structure (Fig. 1(b)) is a polysilicon emitter in which the n+

dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitted base junction.

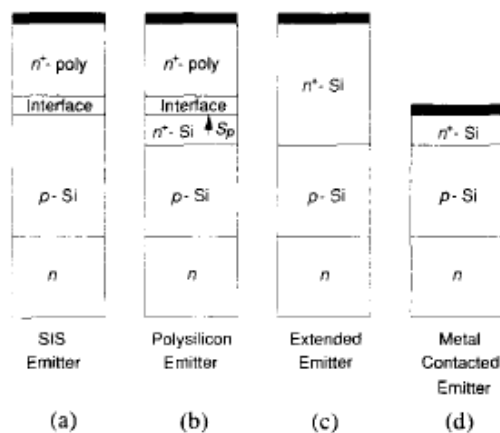


Fig. 1. Schematic diagrams of (a) an SIS emitter, (b) a polysilicon emitter, (c) an extended emitter, and (d) a metal contacted emitter.

EX1016-Post at 1718, Fig. 1. The “outdiffusion” method of doping by thermally driving dopants from one layer into the substrate was known even years earlier than 1992. *See, e.g.*, EX1006-Kwark at 743 (“emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction”) (1984); EX1020-Lindholm at 363 (“Outdiffusion from the doped polysilicon into the base occurring during the emitter diffusion creates a crystalline low-high junction of thickness $<200 \text{ \AA}$.”) (1985); EX1007-Kwark II at 1123 (“In addition, emitters of type C with no prediffusion were fabricated. These relied solely on outdiffusion from the in-situ doped SIPOS or polysilicon to provide sufficient surface doping concentration.”) (1987).

D. State of the Art

78. The 074 Patent identifies doped polycrystalline silicon (with or without oxygen) as an exemplary material for the “electrically passivating and conductive film,” EX1001 at 5:42-55, 6:5-15, and silicon oxide as an exemplary material for the “electrically passivating interface layer”, *id.* at 5:56-6:4.

79. Long before 2009, those skilled in the art already recognized that polycrystalline silicon (also known as “polysilicon”) films, either by itself or mixed with small amount of oxygen (known as “SIPOS”), could reduce solar cell recombination by passivating the silicon substrate and improve solar cell efficiency. An interfacial oxide layer was also known to enhance this improvement by the polysilicon film. An “interfacial oxide layer” refers to a thin layer of silicon oxide in between the substrate and the polysilicon layer.

80. Deposited polysilicon emitters with an interfacial oxide layer were first used to improve the performance of bipolar transistors in 1984. EX1027, Ashburn 1984. Then in 1985, Yablonovitch et al. showed that n- or p-type doped “SIPOS” films (i.e. polycrystalline silicon mixed with oxygen) together with the interfacial oxide layer reduces recombination (as measured by the saturation current density, J_o , discussed more below in the overview of Yablonovitch) by one to two orders of magnitude compared to conventional dopant diffused layers. EX1005 (Yablonovitch). SIPOS films “were pioneered at Sony [and] found initial

application in their intrinsic form to the passivation of high voltage devices.”

EX1007 at 1121. Yablonovitch states that its findings with the use of SIPOS films with solar cells “suggests that crystalline solar cells can be much more efficient than had been suspected.” *Id.* at Abstract, *see also* EX1028 at 597 (“There have been a considerable number of reports recently on improved bipolar transistor emitters made of polycrystalline silicon or of SIPOS.... Such heterojunctions are valuable not only for emitter efficiency in bipolar transistors, **but also for solar cells**”).

81. Subsequently in 1987, another publication modeled the projected efficiencies of what would be possible incorporating “SIPOS” emitters versus diffused emitters and showed a more than one percent absolute increase in efficiency for the solar cell. EX1029, 2122.

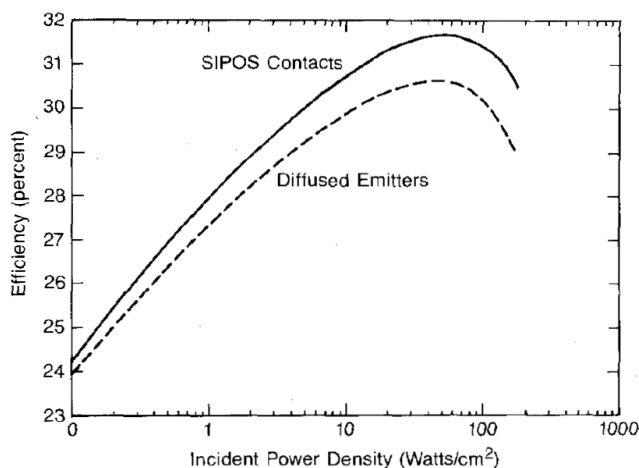


Fig. 9. A comparison of the projected efficiencies possible for a cell incorporating SIPOS emitters (solid curve), compared to projections for diffused emitters as used to date (dashed curve).

82.

83. Around the same time, Kwark extended the findings with SIPOS and interfacial oxide layer to the use of relatively oxygen-free polysilicon with interface oxide layer, recognizing that “incorporation of these films into emitter structure ... translates into potential improvements of energy conversion efficiency for solar cells” EX1006, 742.

84. By 2008, it was well recognized that “[g]reater improvements in open-circuit voltage and efficiency can be achieved from polysilicon contact solar cells in devices with a deliberately grown interfacial oxide with thin polysilicon layer whatever the grain width and cell thickness.” EX1030 (Zouari), 322. By this time, others had also published and filed patent applications describing front and back junction solar cells with the polysilicon emitter structure deposited on an interfacial oxide layer formed over the substrate. EX1032 (Cousins), 2:28-31, 2:58-58, Fig. 1; EX1036 (Borden), 1149.

V. DETAILED OVERVIEW OF THE PRIOR ART

A. Yablonovitch (EX1005)

85. “A 720 mV open circuit voltage $\text{SiO}_x:\text{cSi}:\text{SiO}_x$ double heterostructure solar cell” (“Yablonovitch”) (EX1005) is an article authored by E. Yablonovitch and T. Gmitter published in the journal Applied Physics Letters, Vol. 47 at 1211, in 1985. I understand from Petitioner’s counsel this makes Yablonovitch prior art to the 074 Patent.

86. Yablonovitch discloses the fabrication and testing of “SIPOS-crystalline silicon-SIPOS double heterostructure solar cells.” *Id.* As explained by Yablonovitch, “SIPOS” stands for “semi-insulating polycrystalline silicon,” which is a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1005 at 1211. The SIPOS was formed using chemical vapor deposition using a mixture of silane, dopant (phosphine), and oxygen, which when treated with a thermal annealing process, forms small grains of polycrystalline silicon embedded in a layer of SiO₂. In the art, SIPOS films are also known as “deposited silicon films doped with oxygen.” EX1007 (Kwark II) at 1121; EX1035 (Matsushita) at abstract (“SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.”).

87. From the studies, Yablonovitch concluded that “crystalline silicon solar cells can be much more efficient than had been suspected” by using a SIPOS emitter layer on a crystalline silicon substrate. *Id.* In particular, Yablonovitch suggested replacing existing homojunction-type solar cells, in which the emitter layer is formed by diffusing a portion of the solar cell’s substrate with the opposite dopant type, with heterojunctions, in which the emitter is made of SIPOS, which has a different bandgap compared to the base silicon substrate. *See e.g.*, EX1005 at abstract, 1211:

The processing of these solar cells gives insights into the truly outstanding performance of the n⁺-SIPOS: p-Si

heterojunction which has a forward saturation current coefficient $J_o=10^{-14}$ A/cm², or equivalently an “emitter Gummel number” $G_e=3.3 \times 10^{15}$ s/cm⁴....

The solar cell should be built in the form of a double heterostructure. In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping.

The parameter “ J_o ” is called “saturation current density” and is a global indicator of the quality of a solar cell PN junction, bulk silicon layer and surfaces (a function of overall electron/hole recombination in the device). A lower value is better.⁴

88. Yablonovitch reported much lower J_o with the SIPOS emitters compared to diffused emitters for both n-type and p-type SIPOS emitters. EX1005 at 1211. In particular, Yablonovitch reported that “n⁺-type SIPOS heterocontacts on p-Si [p-type silicon substrate]” showed forward saturation current J_o “two orders of magnitude superior to a conventional homojunction.” *Id.* And although Yablonovitch’s article focused on n-type SIPOS, Yablonovitch further tested and reported that p-type SIPOS on n-type substrates were also “superior to that of a

⁴ Specifically, J_o is directly proportional, among other attributes, to the “observed surface recombination velocity” S . EX1005 at 1212 (“ $J_o=qn_i^2S/p^b$ ”)

homojunction.” EX1005 at 1211. The SIPOS heterocontacts studied by Yablonovitch exhibited “excellent surface passivation”. EX1005 at 1212.

89. Yablonovitch also described the method for manufacturing the studied SIPOS solar cells Yablonovitch used. This process is set forth at a high level in Table II of Yablonovitch, below.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

90. Steps 6-9 are particularly relevant to the 074 Patent. First, in step 6, Yablonovitch oxidized the “thin silicon wafers” with oxygen, O_2 , for five minutes to grow a layer of silicon oxide on the surface of the silicon wafer. EX1005 at 1212, Table II (step 6). According to Yablonovitch, this step was crucial to the improved results observed by Yablonovitch:

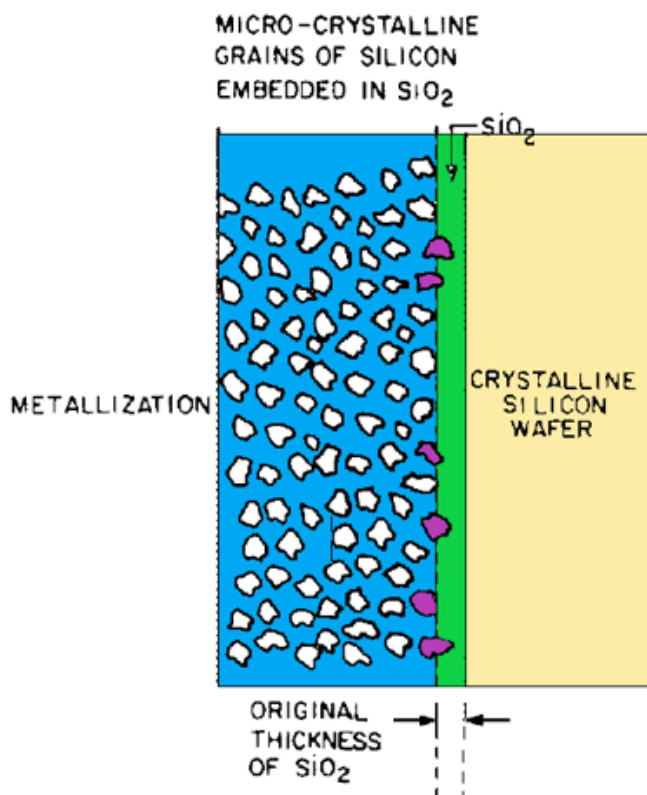
Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step

the “emitter Gummel number”⁵ figure of merit degrades by almost an order of magnitude. We found that purging with high-purity cylinder gas (< 0.5 ppm O₂ and H₂O) helps to reproducibly control this oxidation step. In some published results on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is necessary toward achieving the most favorable figure of merit. Dewar nitrogen gas is notoriously unreliable in regard to oxygen concentration and was avoided. Likewise it was helpful to load the silicon into a cold furnace to prevent inadvertent oxidation. [*Id.* at 1212(citations omitted).]

Yablonovitch also noted that even when the oxidization step is not performed intentionally, oxidation nevertheless occurs “inadvertently.” *Id.* Yablonovitch’s intentional oxidation step resulted in a thin layer of silicon oxide (SiO₂) as the

⁵ “Emitter Gummel number” reflects the total majority carrier charge in the emitter region. EX1026 (Streetman) at 378 (“We can similarly write the base electron current flow back into the emitter as [a function of Q_E], where Q_E is the integrated majority carrier charge in the emitter, known as the *emitter Gummel number*.”).
The Gummel number was a figure of merit used in analyzing bipolar junction transistors, for which a higher number was generally better.

oxygen reacts with the silicon on the surface of the wafer, which I have colored green in the portion of Fig. 3 of Yablonovitch reproduced below. EX1005, Fig. 3⁶.



91. Next, in step (7), Yablonovitch formed the SIPOS layer, colored blue in the figure above. EX1005 at 1213, Table II (step 7). In particular, Yablonovitch deposited a chemical gaseous mixture of SiH₄ (silane), PH₃ (phosphine), and O₂ (oxygen) to form the as-deposited SIPOS. *Id.* The phosphine allows the SIPOS to

⁶ Throughout my report, I have added colored annotations to various figures to assist in my explanations. Unless otherwise noted, it should be understood that the colorations are added.

become doped with phosphorus *in situ*, as the SIPOS is being formed. The SIPOS mixture was then heated at 900°C for fifteen minutes, a process called annealing, in order to crystallize the silicon in the SIPOS and activate the dopant:

The annealing step (9) follows SIPOS deposition. **This step is necessary to precipitate microcrystalline silicon grains within the material and to activate the phosphorus dopant.** In addition during this step the phosphorus diffuses about 20-50 Å into the silicon wafer as measured by secondary ion mass spectrometry. [*Id.* at 1212, Table II (steps 8 & 9).]

Yablonovitch further noted that during the annealing step “phosphorus diffuses about 20-50 Å [i.e., 2-5 nanometers] into the silicon wafer” through the thin oxide layer, a process commonly known as “outdiffusion.” *Id.* at 1212. Moreover, as a result of heating, the micro-crystalline silicon grains “protrude into the oxide as shown in Fig. 3,” which I have colored purple in the figure above, such that “electrical contact [between the wafer and the SIPOS layer] is via thin spots and pinholes in the SiO₂.” *Id.* at 1213. In other words, as small grains of crystalline silicon, which is more conductive than the silicon oxide (an insulator) push through pinholes in the thin oxide layer, these grains form electrical pathways for current to pass through the oxide, which is too thick for tunneling:

Oxide thickness between 25 and 40 Å [i.e., 2.5-4 nanometers] was found to be equally favorable with respect to the "emitter Gummel number." Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because over part of this range the oxide is too thick for electron tunneling. **We**

believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO₂. [*Id.* at 1213.]

B. Kwark (EX1006)

92. “SIPOS Heterojunction Contacts to Silicon,” is a conference paper presented at the International Electron Devices Meeting (1984): 742-745 (“Kwark”), authored by Y. Kwark and others, and was published in Technical Digest, pp. 742-745, IEEE in 1985. I understand from counsel this makes Kwark prior art to the 074 Patent.

93. Kwark reported on testing of both SIPOS *and* polysilicon films with and without an intervening chemically grown oxide layer, referred to as a “chemox,” across annealing temperatures ranging from 800-1000°C. EX1006, 742, Fig. 4. For polysilicon emitters, and in particular for *outdiffused* polysilicon emitters (“emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction”), Kwark found that the chemox layer decreased emitter saturation current J_{oe} .⁷ EX1006, 742. Specifically, Kwark reported that the addition of a polysilicon emitter (labelled “POLY”) without a chemox does not

⁷ In this context, J_{oe} is one of several components of total J_o with the additional “e” to indicate it is the component arising from the “emitter”.

affect J_{oe} (the emitter saturation current) as much as would have been expected (though it was still lower than the “Al contact” control shown below). EX1006, 743. On the other hand, Kwark reported that when chemox was added, J_{oe} was greatly decreased with the polysilicon emitter compared to the “Al contact” control shown below. EX1006, 743. The “Al contact” control was a conventional, in-substrate diffused emitter formed with a pre-diffusion of the dopant into the substrate before the formation of the aluminum contact. *Id.*⁸ The “Al contact” control did not have either the polysilicon or SIPOS layer.

94. Kwark’s observations with respect to the impact of chemox on outdiffused polysilicon emitters are summarized in Figure 4, reproduced here.

⁸ See also, EX1007 (Kwark II) at 1123 (“The test devices had two diffused emitters of different junction depth, emitters A and B, that were either contacted with aluminum, as a control, or contacted with in-situ doped SIPOS or polys-silicon.”).

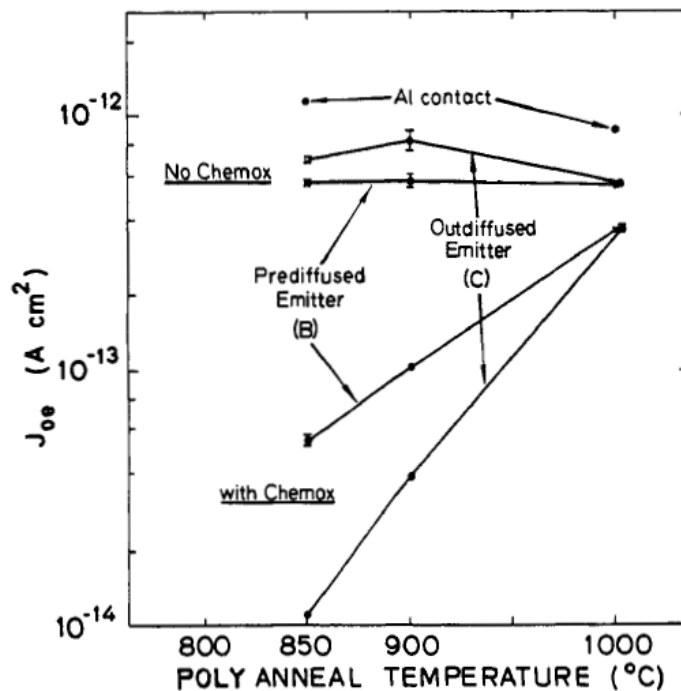


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

95. As for SIPOS emitters, Kwark observed that for SIPOS emitters *without* an intentional chemox layer “[t]he behavior above 850°C strongly resembles the POLY case with chemox,” whereas the SIPOS layers with chemox exhibited slightly better J_{oe} at higher temperatures (*id.* at 743):

In Fig. 5, J_{oe} for a $7 = 0$ SIPOS film (which recall has several at% oxygen) without the chemox is shown. The behavior above 850°C strongly resembles the POLY case with chemox. Addition of the chemox to the SIPOS contact structure does not greatly affect the lowest values of J_{oe} attained. However, the increase in J_{oe} at higher temperatures is not as severe as for the devices in Fig. 4 and 5.

Figures 5 and 6 showing Kwark's results for SIPOS with and without chemox are reproduced below. From this data, Kwark postulated that high temperature annealing of SIPOS causes a thin interfacial oxide to form at the interface of the SIPOS and silicon substrate, whether or not an intentional chemox layer is added (*id.*):

That there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases. **Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent with the observed similarities in J_{oe} .** The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.

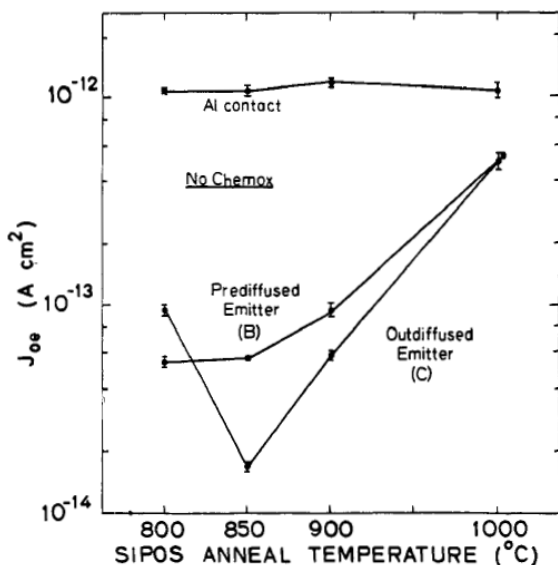


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

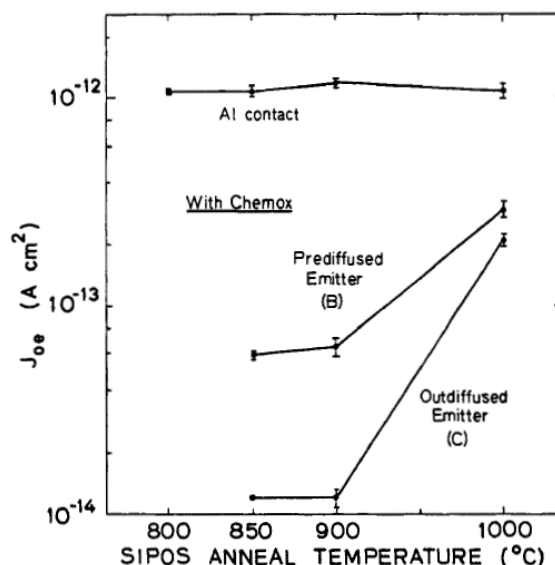


Fig. 6: emitter saturation current vs. anneal temperature for SIPOS contacts with a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

96. The formation of the interface oxide as a result of the annealing process is depicted in Figure 3 of Kwark. *Id.* at 743. In Figure 3, “as-deposited” SIPOS is shown crystallizing into small grains of “XTAL Si” (crystal silicon) embedded in silicon oxide SiO_2 , along with a thin interfacial oxide, as a result of the annealing process.

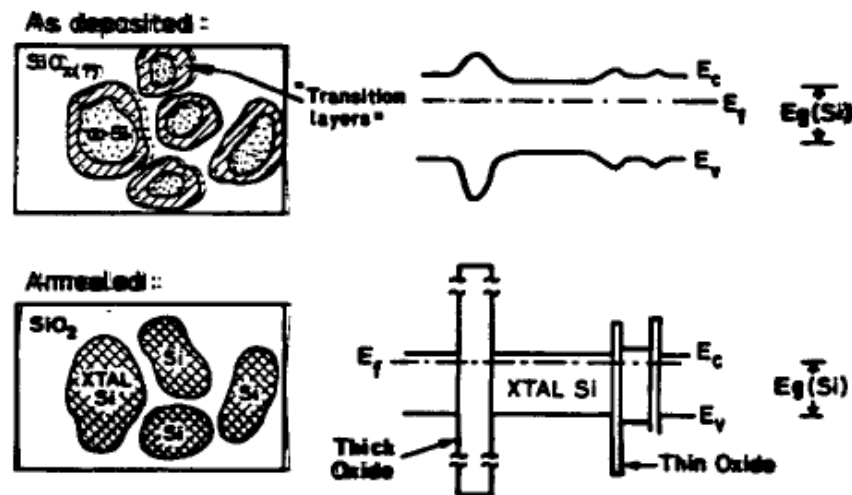


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

97. Another paper authored by Y. Kwark and R. Swanson that was published a few years after Kwark (EX1006), N-type SIPOS and Poly-Silicon Emitters, Solid-State Electronics, Vol. 30, No. 11, pp. 1121-1125 (1987) (“Kwark II”) (EX1007) reproduced much of the same data presented in Kwark, but also provided additional details regarding the configuration of the test structures, details

of the experiments on polysilicon and SIPOS emitters, and conclusions Kwark drew from the results of the experiments. Regarding the oxide layer formed with the SIPOS film without the added chemox, Kwark II explained that “[s]uch an oxide could form, for example, during the anneal as oxygen segregates from the SIPOS.” EX1007 at 1125.

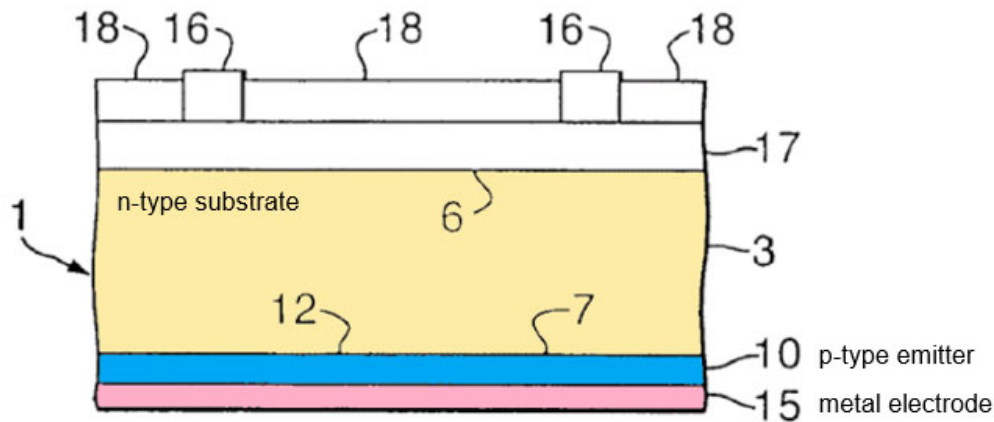
C. Froitzheim (EX1008)

98. European Patent Application Publication EP1732142A1 (EX1008) to Froitzheim (“Froitzheim”) was published on December 13, 2006. EX1008, face. I understand from counsel this makes Froitzheim prior art to the 074 Patent.

99. According to Froitzheim, in conventional solar cells the emitter layer is placed at the front of the cell to form a frontside pn junction with an oppositely doped p-type substrate. EX1008, ¶2. Froitzheim instead proposed forming the pn junction on the rear of the solar cell, thus creating a backside pn junction solar cell. EX1008, ¶8. As shown in Figure 1 of Froitzheim below, solar cell 1 has an n-type body layer or substrate 3 (yellow) with a front side 6 and a rear side 7. EX1008, ¶24. A p-type doped emitter layer 10 (blue) is placed on the rear side of the cell, thus forming the pn junction on the rear side of the solar cell. EX1008, ¶25. A contact 15 (pink) is formed on the back of the emitter layer 10 and covers substantially all of the rear side of the solar cell. EX1008, ¶27 (“The rear side

contact is shown covering a large part or substantially all of the rear side of the cell.”).

Fig. 1.

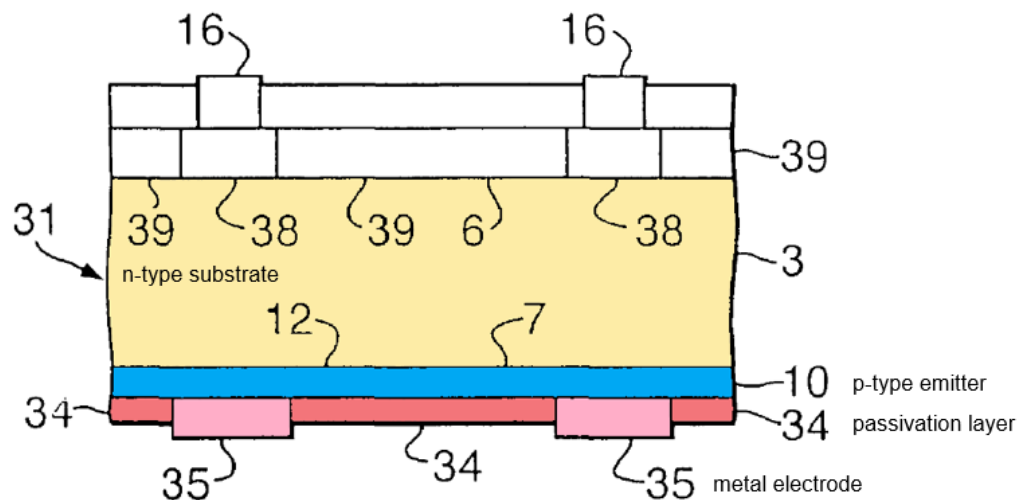


100. Froitzheim also discloses a method for fabricating the solar cell above. First, Froitzheim forms the n-type silicon substrate from a wafer in a <100> crystalline orientation doped with phosphorus. EX1008, ¶¶38-39. The substrate’s rear surface is then diffused with boron, a p-type dopant, using one of several known diffusion techniques, including the gas and solid diffusion techniques I described in Section IV.C above. EX1008, ¶40. In particular, Froitzheim suggests forming a boron-doped diffusion source layer onto the back of the substrate and thermally driving dopants from the diffusion source layer into the substrate. EX1008, ¶40 (“The diffusion source layer is one that contains boron and out of which the boron is thermally driven.”). The diffused p-type doped layer 10 thus forms an emitter layer on the back of the n-side substrate because of the

opposite dopant types. Phosphorus is diffused onto the front surface of the substrate to form an n-type front surface field. EX1008, ¶¶43-44. After the formation of the rear p-type emitter and front n-type surface field, passivation and anti-reflection coating are applied “using known methods,” and front and rear metal contacts are applied. EX1008, ¶¶48-50, 60.

101. Although the embodiment in Figure 1 of Froitzheim has a rear electrode that covers the entire back surface of the solar cell, Froitzheim also discloses another embodiment in Figure 3 reproduced below that has a metal electrode 35 (pink) that is arranged in a “finger structure covering only part of the rear side” deposited by “screen-printing.” EX1008, ¶¶33, 48-50. The finger electrodes contact the p-type emitter layer 10 at specific points through openings in a passivation layer 34 (red). EX1008, ¶33.

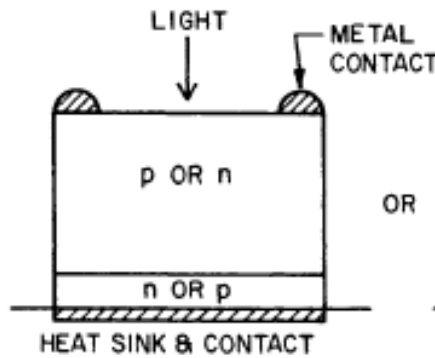
Fig.3.



D. Neville (EX1009)

102. Solar Energy Conversion, The Solar Cell, Second Ed. (Elsevier Science B.V.) (EX1009) (“Neville”), is a textbook published in 1995. I understand from counsel this makes Neville prior art to the 074 Patent.

103. As I discussed above in Paragraph 71, a Skilled Artisan would have known around the time the 074 Patent was filed (and years before then) that the polarity of a solar cell—whether to make the base substrate p-type and the emitter n-type, or vice versa—could be reversed. This basic observation is demonstrated by Neville, which depicts a simple schematic of a back junction solar cell showing that the substrate can be either p- or n-type, and the emitter layer would then have the opposite dopant type (n- or p-type). EX1009 at 199-200. While a Skilled Artisan building a solar cell may ultimately choose one of those two possible options after weighing various manufacturing and efficiency concerns, the Skilled Artisan would nevertheless know that both basic options are available and would be able to implement either option when designing a solar cell.



E. Sasaki (EX1010)

104. H. Sasaki, et al., Light Trapping for Thin-Film Silicon Solar Cells Fabricated on Insulator, Jpn. J. Appl. Phys. Vol. 33 (1994) pp. 3389-3392 (“Sasaki”) (EX1010), is a paper published in the Japanese Journal of Applied Physics at least by 1994. I understand from counsel this makes Neville prior art to the 074 Patent.

105. Sasaki’s article explores light trapping schemes for thin-film solar cells to improve the efficiency of existing cells. EX1010-Sasaki at 3389. One such strategy investigated by Sasaki was to increase the light internally reflected at the rear of the solar cell. *Id.* at 3390. In particular, Sasaki sought to improve over existing solar cells that used aluminum rear metal contacts by using silver contacts and/or a transparent conductive indium tin oxide (“ITO”) film (*id.*):

In order to realize reflectivity higher than that of conventional aluminum (Al) metal, we have adopted silver (Ag) metal and a transparent conductive indium tin oxide (ITO) film inserted between the thin Si film and Ag layer.

Figure 2 of Sasaki reproduced below depicts, at a high level, the configurations Sasaki tested. *Id.* In Figure 2 below, the silicon substrate is colored blue, the ITO film is colored orange, and the aluminum/silver contacts are colored pink. The internal reflection of light coming in through the front of the solar cell and reflecting at the back surface of the substrate is depicted by the arrows.

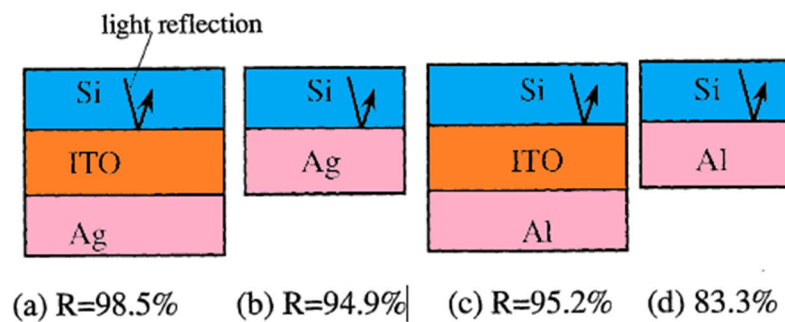


Fig. 2. Calculated reflectances for four different conditions of rear reflectors at opening.

106. Sasaki observed that by including an ITO film between the silicon substrate and a silver electrode, the internal reflectivity of the solar cell went up from 94.9% to 98.5% compared to a solar cell with a silver contact and no ITO film. *Id.* Even for cheaper solar cells with aluminum contacts, adding the ITO layer between the substrate and the contact increased internal reflectivity from 83.3% to 95.2% (*id.*):

Comparing the result obtained using only Al film (R=83.3%), the Ag film can increase the reflectance to R=94.9%. Furthermore, insertion of the ITO film between Si and Ag makes it possible to obtain a sufficiently high reflectance of R=98.5%.... On the other hand, for low-cost

fabrication (using the less-expensive Al electrode), insertion of the ITO film can improve the reflectance from R=83.3% to R=95.2%.

VI. CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM AND YABLONOVITCH

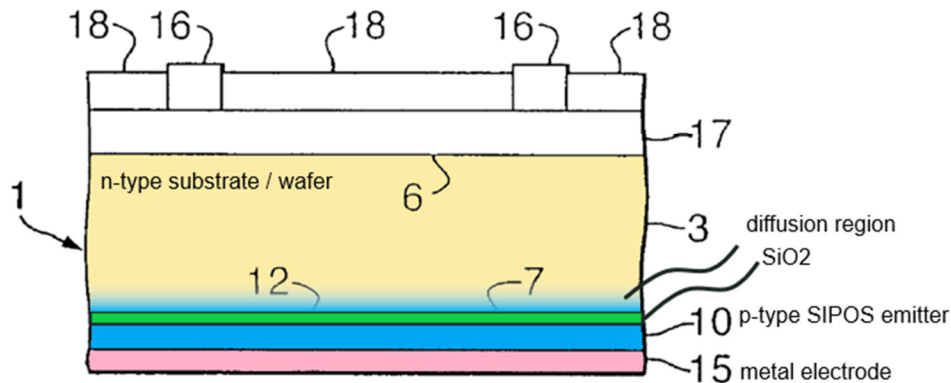
107. In my opinion, the combination of Froitzheim and Yablonovitch rendered obvious claims 1, 2, and 4-8 of the 074 Patent.

A. The Combination of Froitzheim and Yablonovitch

108. In my opinion, it would have been obvious to a Skilled Artisan to modify Froitzheim's method of forming a solar cell by replacing the formation of the diffused emitter of Froitzheim with Yablonovitch's formation of a SIPOS emitter and interfacial oxide, based on Yablonovitch's teachings that doing so would reduce J_o and increase efficiency, as discussed more below. An exemplary device made using this combined method is illustrated in the figure below, in which Froitzheim's in-substrate emitter 10 is replaced with Yablonovitch's SIPOS emitter (blue), SiO₂ oxide layer (green), and a dopant diffusion region (blue) in the substrate.

Combination of Froitzheim and Yablonovitch

Fig. 1.



109. Though I have depicted the combination as having an n-type substrate and p-type SIPOS for simplicity, the combination could instead have a p-type substrate and n-type SIPOS, as discussed in more detail below in paragraphs ¶¶123-126 below. The figure above is not intended to limit the dopant types of the combination to just those labelled.

110. In addition, I have primarily used the embodiment shown in Figure 1 of Froitzheim to explain the combined teachings of Yablonovitch and Froitzheim. The embodiment in Figure 1 has a metal contact that covers substantially the entire backside of the solar cell, just like the embodiment depicted in Figures 5 and others of the 074 Patent. EX1008 (Froitzheim), ¶27 (“The rear side contact is shown covering a large part or substantially all of the rear side of the cell.”); EX1001 (074 Patent) at Fig. 5, 4:60-5:11. However, a Skilled Artisan could instead combine the

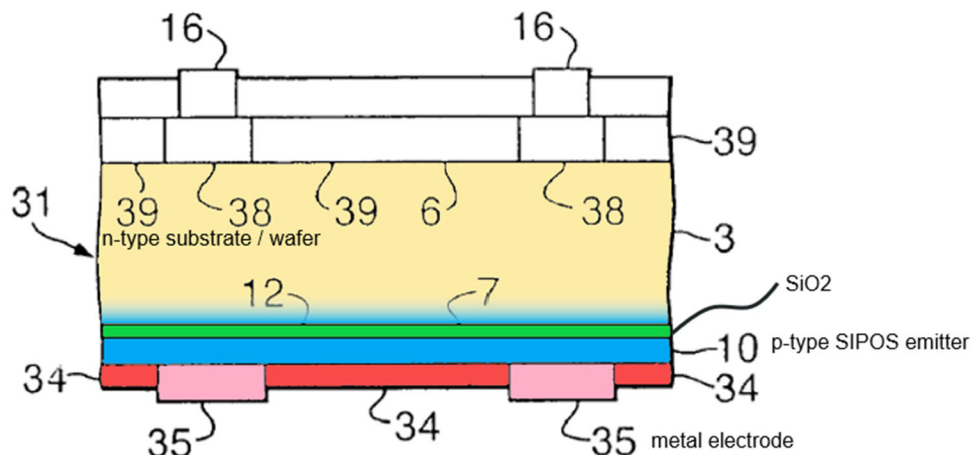
embodiment in, e.g., Figure 3 of Froitzheim with Yablonovitch in the same manner. That combination is depicted below. Unlike Figure 1, which has a contact covering the entire backside of the solar cell, Figure 3 has a series of rear finger contacts 35 (pink) separated by a passivation layer 34 (red), but which is otherwise the same as the Figure 1 in relevant respects discussed below:

Reference is made to Figure 3 showing a second embodiment of a solar cell 31 according to the invention. Cell 31 differs from cell 1 of Figure 1 in that the rear contacts 35 are arranged in a finger structure covering only part of the rear side, e.g. similar to that of Figure 2.

Accordingly, it should be understood that my discussions below pertain to both possible combinations, even though I use the combination with Figure 1 for simplicity.

Second Combination of Froitzheim and Yablonovitch

Fig.3.



B. Modifying Froitzheim with SIPOS and Interfacial Oxide Layer

111. Froitzheim and Yablonovitch are analogous art, because they are both in the same field of solar cell design and fabrication. EX1008, Abstract, ¶¶1,9; EX1005, Abstract, 1211-12. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1008, Abstract, ¶¶1,9; EX1005, Abstract, 1211.

112. In my opinion, by April 2009, the Skilled Artisan would have been motivated to replace the diffused emitter of Froitzheim's back junction solar cell with a SIPOS emitter as taught by Yablonovitch, because as Yablonovitch disclosed, SIPOS emitters form heterojunctions with silicon, which was known to improve the quality and efficiency of the solar cell compared to conventional homojunction solar cells. For example, Yablonovitch observed that:

We have found rather good performance in **SIPOS-crystalline silicon-SIPOS double heterostructure solar cells**, where SIPOS=SiOx. The processing of these solar cells gives insights into the truly outstanding performance **of the n⁺-SIPOS: p-Si heterojunction** which has a forward saturation current coefficient $J_0=10^{-14}$ A/cm², or equivalently an "emitter Gummel number" $G_e=3.3 \times 10^{15}$ s/cm⁴....

It has been recognized for some time that the structure of an ideal solar cell should resemble that of a semiconductor laser. **The solar cell should be built in the form of a double heterostructure.** In this configuration a narrow band-gap active layer is sandwiched between two

wide band-gap layers of opposite doping. [EX1005 at abstract, 1211.]

Indeed, others before Yablonovitch had already reported on the superiority of SIPOS heterojunctions over homojunctions in the context of bipolar transistors: “The first indication of a superior quality heterojunction using SIPOS came in the pioneering work at Sony. Matsushita *et al.* showed that SIPOS heterojunction emitters incorporated as part of a bipolar transistor structure showed greatly enhanced current gains.” *Id.* at 1211.

113. Yablonovitch was thus interested in analyzing “[a] more direct measure of heterojunction quality i[n] the forward saturation current J_o ” for solar cells. *Id.* at 1211. For both n- and p-type SIPOS emitters, Yablonovitch saw improvement in the forward saturation current J_o over conventional homojunction solar cells:

As a result of the fabrication sequence to be discussed below we now routinely produce $J_o = 10^{-14}$ A/cm² for **n⁺-SIPOS heterocontacts** on p-Si (or equivalently $G_e = 3.3 \times 10^{15}$ s/cm⁴). **This is about two orders of magnitude superior to a conventional homojunction.** Unfortunately we have been unable thus far to achieve a correspondingly good figure of merit for p-type SIPOS. Our best value of forward saturation current on **p-type SIPOS** is $J_o = 8 \times 10^{-14}$ A/cm², **which is nevertheless superior to that of a homojunction.** [EX1005 at 1211.]

114. A homojunction is a junction (in this context, e.g., a pn junction) in which the two sides of the junction have the *same* bandgap energy such as the

junction formed within a single semiconductor material. EX1026 at 234 (“Thus far we have discussed p-n junctions formed within a single semiconductor (*homojunctions*)....”). Thus, for example, a pn junction formed by doping the silicon substrate with p-type dopants, and the one side of the same substrate with n-type dopants (or vice versa), would form a homojunction, because the same bandgap is reflected on both sides of the pn-junction.

115. By contrast, a heterojunction is formed from two materials that have *different* bandgaps. *Id.* (“The third important class of junctions consist of those between two lattice-matched semiconductors with different band gaps (*heterojunctions*).”). A SIPOS film, being composed of silicon and oxygen, is a different material than the crystalline silicon and has a different bandgap than the crystalline silicon. A SIPOS on crystalline silicon junction thus forms a heterojunction. See EX1005 (Yablonovitch) at 1211 (“Due to its larger band gap, the heterocontact material may be disordered and of poor quality and still be able to support the voltage generated in the active layer”); EX1007 (Kwark II) at 1123-24 (“It has been postulated that the improvement that SIPOS emitters obtain is because SIPOS has a larger band gap than crystalline silicon....”).

116. Froitzheim’s emitter forms a homojunction. As Froitzheim explains, the p-type doped emitter region is formed in the n-type substrate “by a process which introduces dopant, preferably boron, only by diffusion into the rear surface

of the body layer.” EX1008, ¶¶39-40. Because the emitter in Froitzheim is formed by diffusing p-type dopants directly into the substrate, the emitter region and the substrate body region have the same bandgap, thus comprising a homojunction.

117. Although the embodiment in Figure 1 of Froitzheim is described as having an n-type substrate, and Yablonovitch preferentially used an n-type SIPOS emitter, in my opinion, a Skilled Artisan would be motivated to combine Froitzheim and Yablonovitch because Yablonovitch also suggested that p-type SIPOS was also “superior to that of a homojunction” and could also be used. EX1005 at 1211. (“Our best value of forward saturation current on *p-type* SIPOS is $J_0 = 8 \times 10^{-14}$ A/cm², which is nevertheless superior to that of a homojunction.”). The Skilled Artisan would understand that a J_0 of 8×10^{-14} A/cm² is still more an order of magnitude lower than the recombination of a conventional diffused emitter and therefore advantageous to replace the diffused emitter. See e.g., EX1012 (Gan) at 245 (“For silicon solar cells operated under high concentrated sunlight, the emitter recombination is one of the main recombination that limit the solar cell performance. This is because the diffused emitter, which is formed with dopant diffusion into the base (substrate), has high J_0 ($=4.5 \times 10^{-13}$ A/cm²). Consequently, the cell performance can be improved if the diffused-emitter is replaced with the polysilicon emitter, of which the J_0 is less than 4.5×10^{-13} A/cm² and the ρ_c is low enough.”) Indeed, Yablonovitch also filed a patent (US

4,525,593) in 1984 in which he discloses that although illustrated with p-doped crystalline silicon and n-doped SIPOS, “it is understood that the doping types may be interchanged.” EX1011 at 2:16-19.

118. Accordingly, a Skilled Artisan would have been motivated to improve Froitzheim’s solar cell by replacing the diffused in-substrate *homojunction* emitter layer with Yablonovitch’s deposited *heterojunction* SIPOS emitter layer, because Yablonovitch specifically suggested that doing so would reduce recombination as seen from the decreased forward saturation current J_0 .

119. A Skilled Artisan would also have been motivated to incorporate Yablonovitch’s interfacial oxide layer when replacing Froitzheim’s diffused emitter with Yablonovitch’s SIPOS emitter, because Yablonovitch understood and instructed that this layer was “critical” to the benefits of using Yablonovitch’s SIPOS emitter:

Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step the "emitter Gummel number" figure of merit **degrades by almost an order of magnitude**. We found that purging with high-purity cylinder gas (< 0.5 ppm O₂ and H₂O) helps to reproducibly control this oxidation step. In some published results on SIPOS heterojunction emitters and polysilicon emitters this step has been omitted, but we believe that oxidation frequently occurs inadvertently and is **necessary toward achieving the most favorable figure of merit**. [EX1005 at 1212.]

The SIPOS emitter and interfacial oxide would otherwise function the same as the emitter in Froitzheim, but with a reduced recombination, as taught by Yablonovitch.

120. It was also well known in the art by 2009 that back junction solar cells—in which the emitter layer and pn junction are formed on the back of the solar cell—could be more efficient than front junction solar cells. This fact was recognized in, for example, US Patent No. 4,667,060 (“Spitzer”) (EX1034), which was issued in 1987. Spitzer disclosed “[a] solar cell of novel construction... featuring the formation of a p-n junction at its rear surface,” in contrast to conventional solar cells, which “comprise a standard p-n junction formed at the front surface.” EX1034 at abstract, 1:10-17. Spitzer taught that placing the pn junction on the rear side of the solar cell “decouples the junction design from the front grid pattern design. In this way, the junction and the grid may be independently optimized to achieve both low series resistance and high open circuit voltage.” *Id.* at 3:12-17. Forming the emitter on the back of the solar cell is beneficial because when the emitter is on the front side--where sunlight enters the solar cell--there is a high concentration of photons that are absorbed in the emitter, but many of the free electrons recombine quickly in the highly doped emitter region before they can diffuse to the metal contacts because of the short minority

carrier lifetimes and diffusion lengths, leading to loss of efficiency. This problem is not seen in a properly designed back junction cell.

C. Reasonable Expectation of Success

121. Replacing the backside diffused emitter layer of Froitzheim with a SIPOS emitter and interfacial oxide layer, as formed by the oxidation and SIPOS deposition steps of Yablonovitch, would have been well within the level of the Skilled Artisan by 2009. It would have been a simple substitution of two known elements for another to obtain predictable results. Yablonovitch provided detailed instruction explaining how the oxidation and deposition of the SIPOS occurred, and would constitute applying standard, known techniques to a known device ready for improvement to yield predictable results. EX1005, Table II, 1212-13.

122. Specifically, instead of introducing the dopant by diffusion at the rear side of the substrate (for example, as described in paragraphs 40-41 of Froitzheim), the Skilled Artisan would grow the interfacial oxide layer by oxidizing the substrate in oxygen, then deposit the SIPOS from a mixture of SiH_4 , PH_3 , and O_2 , followed by annealing at 900°C to form the crystalline SIPOS grains. EX1005 (Yablonovitch) at Table II. Moreover, the Skilled Artisan would have recognized that the steps in fabricating the solar cell could be optimized such that the front and back sides of the solar cell are doped differently without impacting the layers applied to the other side of the solar cell. This would have been within the skill of

the Skilled Artisan before 2009. For example, various techniques such as masking, selective etching, or single sided etching were all available and within the routine skill of the Skilled Artisan before 2009 to be able to process and dope the front and backside of the solar cell differently. See e.g., EX1020 at 363 (“During the polysilicon deposition and the emitter diffusion, CVD-SiO₂ protected the other side of the sample”); EX1044 (US20080041526) (Abstract: “A method of single-sided etching is disclosed”); EX1045 (Arumughan) at 705 (describing an “automated inline etching system” in which “[t]he wafers are transported through an acidic etching solution in a way that only [one] side comes in contact with the chemical bath. As the wafers do not need any stacking, handling becomes much easier and the risk of wafer damage is reduced.”); EX1036 at 1150 (Figure 2) (showing different doping of front and back in a polysilicon emitter solar cell); EX1032 at Figs. 4a-4m, 3:47-5:61. See also, EX1019 at 291 (silicon nitride “serves as a masking layer for heavy phosphorus diffusion and plating, and also performs as an antireflection coating and surface passivator.”) EX1018 at 228 (“Silicon dioxide can be used as an effective barrier to selectively introduce dopants into the silicon surface”). And knowing that the interfacial oxide layer would break up during high temperature annealing, the Skilled Artisan would also have known that the formation of the side with the interfacial oxide layer and the SIPOS layer could be ordered after the dopant diffusion of the other side such that

the interfacial oxide would be exposed only to a single high temperature annealing step. See e.g., EX1036 at (Figure 2) (showing a process where high temperature diffusion of one side ordered first before the formation of the tunnel oxide and polysilicon layers and subsequent annealing).

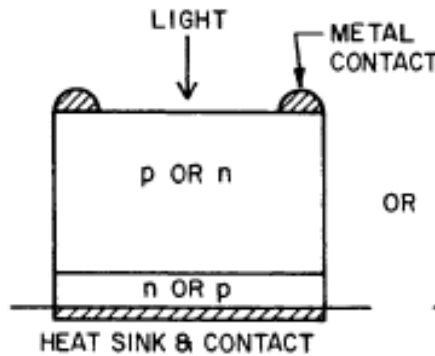
123. The Skilled Artisan in 2009 would also have a reasonable expectation of success in reversing the dopant type of Yablonovitch's n-type SIPOS and using a p-type SIPOS film. For one thing, Yablonovitch expressly created and disclosed using p-type SIPOS. EX1005 at 1211. This is a matter of simple substitution of phosphine (PH_3) in Yablonovitch's SIPOS deposition step 7 mixture with diborane (B_2H_6). Because diborane consists of boron atoms (a p-type dopant) instead of phosphorus (an n-type dopant), this substitution would result in p-type SIPOS. It was well within the level of ordinary skill in 2009 to make this substitution when forming an emitter, as demonstrated by the Quirk, Luque, and Streetman textbooks. See, e.g., EX1018 (Quirk) at 276 ("The polysilicon film is usually doped in situ during the deposition process by adding arsine (AH_3), phosphine (PH_3), or diborane (B_2H_6) to the gas mixture."); EX1019 (Luque) at 528 ("As discussed in Section 12.2.6, a-Si can be doped n-type by mixing phosphine (PH_3) with the gas mixture or doped p-type by mixing diborane (B_2H_6), BF_3 , or trimethylboron [TMB , $\text{B}(\text{CH}_3)_3$] with the gas mixture during deposition."); EX1026 at 450 ("Alternatively, the LPCVD polysilicon film may also be in situ

doped during the deposition itself by flowing in an appropriate dopant gas such as phosphine or diborane.”).

124. Moreover, it was well understood by 2009 that the polarity of a solar cell substrate and emitter could be reversed. In other words, it was well established that a solar cell could be formed either with an n-type substrate and a p-type emitter, or conversely with a p-type substrate and an n-type emitter.

125. That the dopant type of the substrate can be reversed is evident, for example, in the Neville textbook (EX1009), Figure VI.1, which depicts a variety of possible solar cell configurations including a back junction cell like Froitzheim, which has a substrate that is either “p or n” type and a backside emitter that is either “n or p” type. EX1009 at Fig. VI.1, 199-200; see also Paragraphs 102-103 above. The Spitzer patent also observed that for a back junction cell, the wafer (i.e., substrate) “may be formed of an n-type or p-type silicon.” EX1034 at 3:66-68. Froitzheim even alludes to this possibility of reversing the polarity of the substrate and emitter layer. EX1008, ¶7. Thus, alternatively, the Skilled Artisan would understand that Froitzheim could be reversed to have a p-type substrate and used with Yablonovitch’s n-type SIPOS.

Neville, Fig. VI.1



126. Thus, the combination of Froitzheim and Yablonovitch would simply have been the combination of prior art elements according to known methods to yield predictable results. Likewise, substituting Froitzheim's in-substrate emitter with a deposited SIPOS emitter and interfacial oxide layer according to the steps described by Yablonovitch would be simple substitution of one known element for another to obtain predictable results. It would further constitute use of a known technique (depositing SIPOS emitters with an interfacial oxide layer) to improve similar devices (Froitzheim's back junction solar cell) in the same way. It would also constitute applying a known technique to a known device ready for improvement to yield predictable results.

D. Froitzheim and Yablonovitch Disclose All Claim Limitations

1. Claim 1(a) – Preamble

127. The preamble to claim 1 recites: "*A method of fabricating a solar cell.*"

128. Froitzheim and Yablonovitch both disclose methods of fabricating a solar cells. For example, Froitzheim discloses “[t]he method of manufacturing a solar cell according to [Froitzheim’s] invention,” which includes the embodiments in Figures 1 and 3. EX1008, ¶¶38-50. Yablonovitch likewise disclosed the method used to create the heterojunction solar cell Yablonovitch studied, summarized in Table II:

Yablonovitch, Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

2. Claim 1(b) – Central Substrate

129. The first step of claim 1 recites: “*providing a wafer as a central substrate.*”

130. Both Froitzheim and Yablonovitch satisfy this step. In Froitzheim’s fabrication method, a silicon body is formed out of a wafer. EX1008, ¶38 (“A

silicon body layer of n-type bulk doping, typically a wafer in <100> orientation that was sawed from a Cz grown and Phosphorous doped crystal, is provided.”). Likewise, the first step of Yablonovitch’s method starts by submerging silicon wafers in aqueous KOH. EX1009 at Table II, 1212.

Yablonovitch, Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2.
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2.
7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

The silicon wafers in Froitzheim and Yablonovitch serve “*as a central substrate*” because the other layers of the solar cells are subsequently deposited or formed on the wafers. For example, EX1008 (Froitzheim), ¶41 (“a diffusion source layer... is applied, e.g. spun, only onto the back of the n- doped silicon wafer”); EX1005 (Yablonovitch) at 1212 (“The silicon wafers, which were coated on both faces with 1000 Å of n^+ -SIPOS, were fabricated into devices as shown in Fig. 2.”).

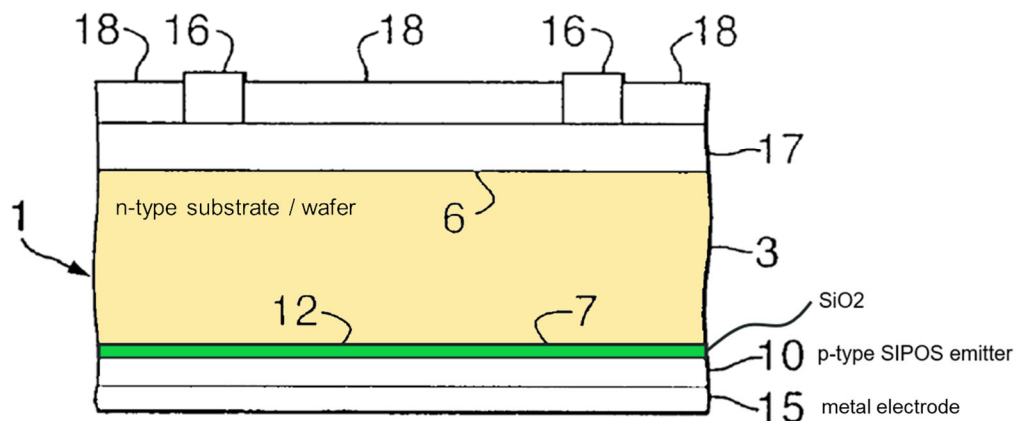
3. Claim 1(c) – Interface Passivation Layer

131. The next step of claim 1 is: “*depositing or growing at least one amorphous interface passivation layer over the substrate.*”

132. The combination of Froitzheim and Yablonovitch, depicted below, has an SiO₂ silicon oxide layer (green) that is an “*amorphous interface passivation layer*” formed on the substrate.

Combination of Yablonovitch and Froitzheim

Fig.1.



133. This step of the claim is found in Yablonovitch. In particular, in step 6, Yablonovitch discloses oxidizing the silicon wafer in O₂:

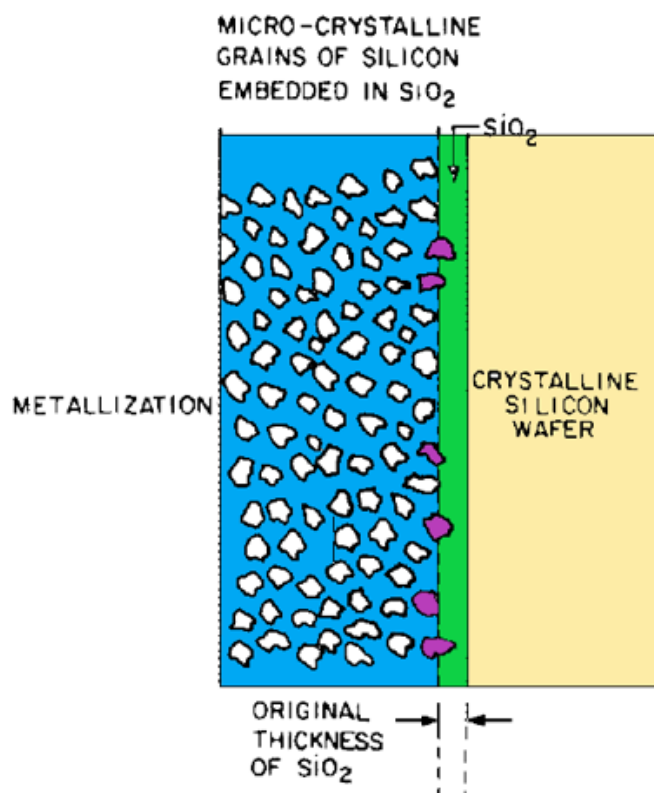
Yablonovitch, Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Oxidizing the wafer grows a layer of silicon oxide on the wafer as the oxygen reacts with the silicon on the surface of the wafer, which is depicted in Figure 3 of Yablonovitch.

Yablonovitch, Fig. 3



134. Yablonovitch's SiO₂ layer is passivating. According to Yablonovitch, the outstanding results of Yablonovitch's studied solar cells was enabled by the quality of the silicon wafer and the passivation of the SIPOS contact with the wafer. EX1005 at 1212 ("This outstanding voltage performance is made possible both by the excellent bulk quality of the crystalline silicon and the excellent surface passivation of the n⁺-SIPOS heterocontact."). Yablonovitch further recognized that "[o]f critical importance in achieving this performance level is the oxidation step (6)." *Id.* In other words, Yablonovitch recognized that the passivating quality of the interfacial oxide layer contributed to the positive results Yablonovitch overserved. And in general, silicon oxide was known in the art prior

to the 074 Patent to have passivating qualities. See, e.g., EX1018 (Quirk) at 227 (“A major benefit from thermally grown SiO₂ is the reduction in the surface-state density of silicon that occurs by tying up dangling silicon bonds. This action is referred to as surface passivation, which prevents the deterioration of the electronic properties.”). The 074 Patent itself also lists silicon oxide as an example of a passivating interface layer. EX1001 at 5:56-61, 5:66-6:4.

135. Yablonovitch’s SiO₂ layer is also amorphous. In Yablonovitch, the SiO₂ layer is thermally grown on the crystalline silicon wafer. Silicon oxide thermally grown on crystalline silicon was known in the art to be amorphous before the 074 Patent. For example, this fact was observed by K Matsumura, et al, in “Residual order within thermally grown amorphous SiO₂ on crystalline silicon,” Phys. Rev. B 69, 085212 (2004) (EX1021) (“Matsumura”). According to Matsumura, “[t]hree models of SiO₂ on Si(001), Si(111), and Si(113) were formed by introducing oxygen atoms in crystalline Si from the surfaces in an atom-by-atom manner. The SiO₂ structures are classified as being amorphous in conventional characterizations....” EX1021 at abstract, 085212-1 (“The thermally grown SiO₂ on crystalline Si (c-Si) is an almost perfect insulator, primarily responsible for the predominance of silicon in the microelectronics industry. The structure of the thermal oxide is amorphous as far as one can see by using electron diffraction and infrared absorption spectrum.”) (citations omitted).

136. In the combination of Froitzheim and Yablonovitch, the formation of the diffused emitter in Froitzheim is replaced with the thermal oxidization and deposition of doped SIPOS layer, as taught by Yablonovitch. EX1005 at 1212.

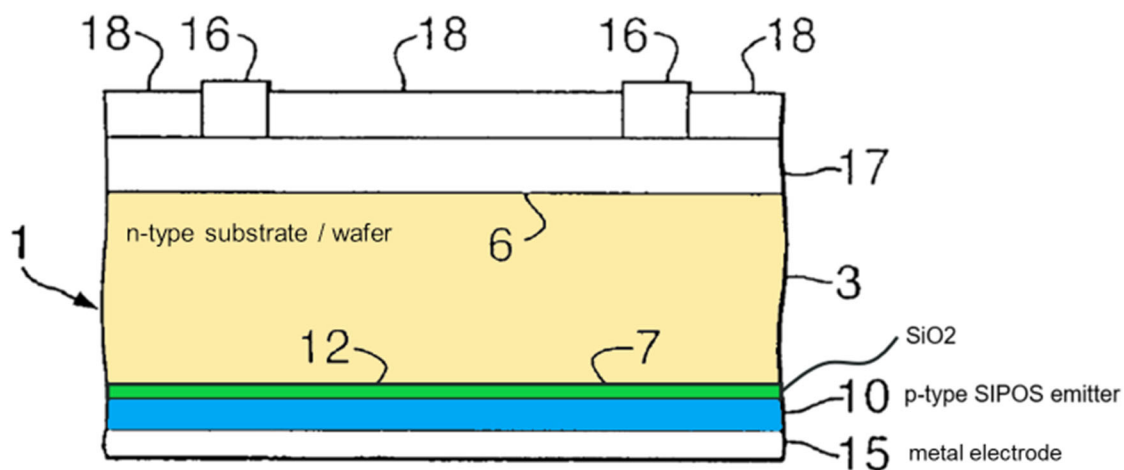
4. Claim 1(d) – Conductive and Passivating Layer

137. The next step of claim 1 is: “*depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant.*”

138. The combination of Froitzheim and Yablonovitch, depicted below, has an p- or n-type SIPOS layer (blue) that is a “*conductive and passivating layer*” formed on the green SiO₂ layer (*interface passivation layer*).

Combination of Yablonovitch and Froitzheim

Fig. 1.



139. This step of the claim is found in Yablonovitch. In particular, in step 7, Yablonovitch discloses depositing SIPOS from a mixture of silane (SiH_4), phosphine (PH_3) and oxygen (O_2), followed by thermal treatment/annealing:

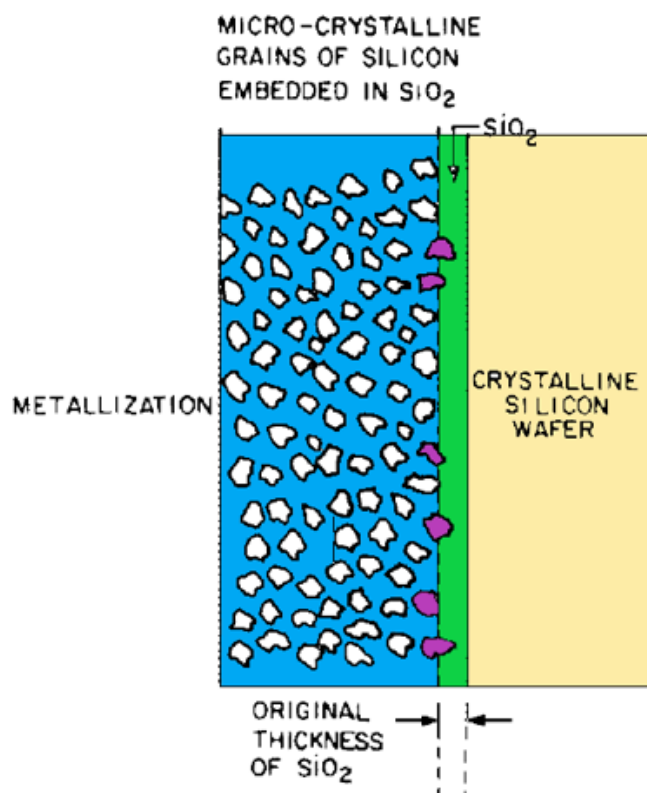
Yablonovitch, Table II

TABLE II. Processing sequence.

- | |
|--|
| <ol style="list-style-type: none">1. Thin silicon wafers to $50\ \mu\text{m}$ in aqueous KOH.2. Getter in an oxidation furnace containing substantial chlorine.3. Strip gettering oxide in HF acid.4. Immediately load into cold APCVD furnace while purging with N_2.5. Ramp up to $650\ ^\circ\text{C}$ while maintaining N_2 purge.6. Oxidize for 5 min with 100 ppm O_2.7. Deposit SIPOS from 1000 ppm SiH_4, 50 ppm PH_3, and 10 ppm O_2.8. Ramp furnace to $900\ ^\circ\text{C}$.9. Anneal for 15 min.10. Ramp furnace down to $450\ ^\circ\text{C}$.11. Anneal in forming gas for 2 h.12. Pull wafers from cold furnace. |
|--|

140. The SIPOS deposition step (once annealed) forms a layer of crystalline silicon grains on the wafer embedded in silicon oxide SiO_2 , which is depicted in Figure 3 of Yablonovitch.

Yablonovitch, Fig. 3



141. Yablonovitch's doped SIPOS layer is conductive. As Yablonovitch explains, "the majority-carrier electrical contact is by individual microcrystalline grains, which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO₂." EX1005 at 1213. The silicon grains in the SIPOS that protrude into the interfacial oxide (colored purple) are sufficiently conductive to allow electrical current to pass through the oxide, which is otherwise too thick for the charge carriers to tunnel through. EX1005 at 1213 ("The individual contacts provide more than enough conductivity for majority- carrier electrons, but the small fractional contact area acts to block minority-carrier holes from recombining in the SIPOS."); *see also id.* at 1212-13

(“Therefore, differential tunneling between electrons and holes does not appear to be playing a major role because over part of this range the oxide is too thick for electron tunneling.”).

142. Even outside of Yablonovitch, the fact that doped SIPOS was conductive was well known in the art before the 074 Patent. For example, US Patent 7,851,336 to Poplavskyy (“Poplavskyy”) which was filed March 13, 2008, and issued December 14, 2010,⁹ cited to the Yablonovitch paper and observed that doped SIPOS generally has a high conductivity:

SIPOS materials are generally prepared by a variety of chemical vapor deposition (CVD) methods, and can include silicon nanocrystals embedded within a matrix of SiO₂. **Such a structure may be doped to have high conductivity (e.g., 10³ S/cm)**, and with a larger band gap than silicon. [EX1022 at 3:16-24.]

143. Yablonovitch’s SIPOS layer is also passivating. As Yablonovitch explains, “**[t]he interface states between SIPOS and crystalline silicon (c-Si) seem to be passivated** as well as the high quality interface between thermally grown SiO₂ and c-Si.” EX1005 at 1211. Indeed, that SIPOS was passivating was well known in the art well before the 074 Patent. In a 1994 article published in the

⁹ I understand from counsel that the filing date makes Poplavskyy prior art to the 074 Patent.

Journal of Materials Research, G. Compagnini and others observed that “[s]emi-insulating polycrystalline silicon (SIPOS) is widely used as a passivation layer.” EX1014 at 885. Kwarik II also discloses that “these films, pioneered at Sony, found initial application in their intrinsic form to the passivation of high voltage devices.” EX1007 at 1121. See also, EX1015 (Pan) at 589 (SIPOS “has been used in a variety of electronic devices ... as excellent surface passivation films in semiconductor devices”).

144. The 074 Patent itself provides further evidence that doped SIPOS is conductive and passivating. In particular, the 074 Patent specification identifies exemplary materials for fabricating an “electrically passivating and conductive film” of either p- or n-types. EX1001 at 5:49-55, 6:5-17. Some of the recited examples include “amorphous or polycrystalline silicon carbides,” “amorphous or polycrystalline silicon,” and “amorphous or poly-crystalline diamond-like-carbon.” EX1001 at 5:49-55, 6:5-15. Importantly, the 074 Patent further notes that “[a]ny of the above listed examples may include oxygen.” EX1001 at 5:54-55, 6:16-17. As Yablonovitch and others recognized, SIPOS is a combination of polycrystalline silicon and oxygen. *See, e.g.*, EX1005 (Yablonovitch) (“SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x).”);

EX1035 (Matsushita) at abstract (“SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.”).

145. Lastly, Yablonovitch’s SIPOS layer “*compris[es] a dopant.*” For example, Yablonovitch discloses a process for forming n-type SIPOS using a mixture of silane, phosphine, and oxygen, which results in SIPOS *in situ* doped with phosphorus. EX1005 at Table II, 1212 (discussing the formation of “n⁺-SIPOS” layers and noting the annealing step “activate[s] the phosphorus dopant”). Phosphorus is a common n-type dopant. EX1018 (Quirk) at 36. However, Yablonovitch also discloses that the SIPOS can be p-type instead, which also exhibited qualities superior to the conventional homojunction cells Yablonovitch studied, even though they were less so than the n-type SIPOS cells. EX1005 at 1211 (“Our best value of forward saturation current on p-type SIPOS is J_0 8×10^{-14} A/cm² which is nevertheless superior to that of a homojunction.”). P-type SIPOS would have, e.g., boron as a dopant instead of phosphorus, because boron is a p-type dopant. EX1018 (Quirk) at 36.

5. Claim 1(e) – Thermal Treatment

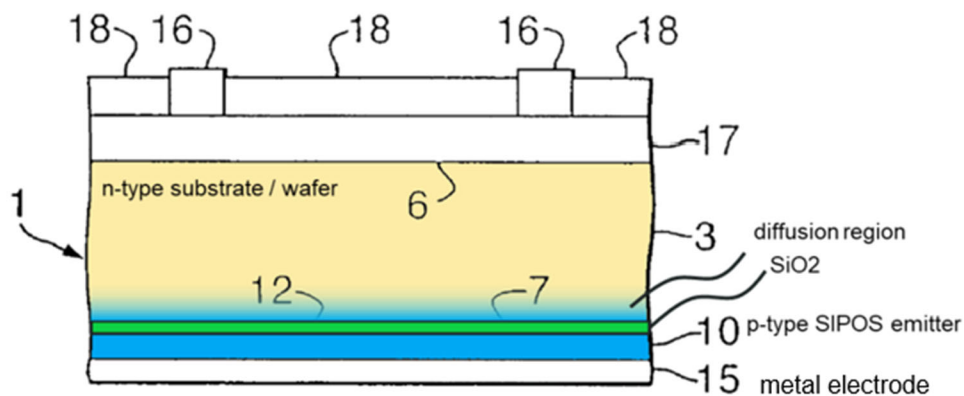
146. The next step of claim 1 is: “*providing thermal treatment at a temperature of about 500°C or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion*”

of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer.”

147. In the combination of Froitzheim and Yablonovitch, depicted below, the annealing step (*thermal treatment*) of Yablonovitch crystallizes the blue SIPOS emitter (*conductive and passivating layer*) and facilitates diffusion of dopants through the green SiO₂ layer (*interface passivation layer*).

Combination of Yablonovitch and Froitzheim

Fig.1.



148. This step of the claim is found in Yablonovitch. In particular, in steps 8 and 9 Yablonovitch discloses annealing the silicon wafer and SIPOS layer at 900°C for fifteen minutes (*“thermal treatment at a temperature of about 500°C or higher”*):

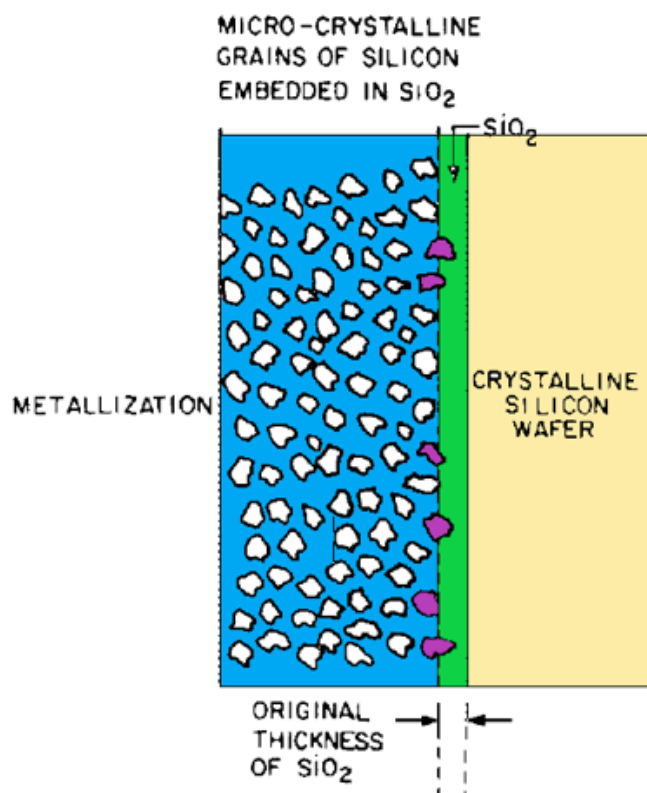
Yablonovitch, Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

149. Yablonovitch's annealing step "*crystalliz[es], at least in part, the at least one conductive and passivating layer.*" In particular, the annealing step turns the as-deposited SIPOS layer into a layer of crystalline silicon grains on the wafer embedded in silicon oxide SiO_2 , which is depicted in Figure 3 of Yablonovitch.

Yablonovitch, Fig. 3



Explaining the effect of the annealing step, Yablonovitch observed that the annealing step causes the silicon in the SIPOS to crystallize into grains:

The annealing step (9) follows SIPOS deposition. **This step is necessary to precipitate microcrystalline silicon grains** within the material and to activate the phosphorus dopant. [EX1005 at 1212.]

150. In general, annealing is a common technique used to crystallize, for example, amorphous silicon into polycrystalline silicon. EX1018 (Quirk) at 499-501 (“Annealing heats the implanted silicon substrate to repair crystalline damage and electrically activate dopants by moving the atoms into crystal lattice sites.... Crystal damage repair is done at about 500°C....”); EX1026 (Streetman), 160-61

(“However, most of this damage can be removed in Si by heating the crystal after the implantation. This process is called *annealing*.”). The annealing step in Yablonovitch is no different and is needed to crystallize the silicon in the SIPOS, because the as-deposited SIPOS is amorphous. E.g., EX1013 (Fussel) at abstract (“As-deposited [SIPOS] layers are predominantly amorphous...”); EX1025 (Kwark III) (“SIPOS films prepared at 650°C are amorphous;”); EX1005 (Yablonovitch) at 1211 (“In its **annealed** form [SIPOS] is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x).”).

151. Yablonovitch’s annealing step also “*facilitat[es] diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer.*” In particular, Yablonovitch observed that the annealing step causes phosphorus to diffuse from the as-deposited phosphorus-doped SIPOS through the SiO₂ interfacial oxide layer into the wafer:

The annealing step (9) follows SIPOS deposition.... In addition **during this step the phosphorus diffuses about 20-50 Å into the silicon wafer** as measured by secondary ion mass spectrometry. This produces **a very shallow n + accumulation layer** which is transparent to minority carriers; i.e., the holes from the bulk “see” the Si-SiO₂ interface. [EX1005 at 1212.]

In order for the phosphorus to diffuse 20-50 angstroms into the wafer, it must pass from the SIPOS layer into the wafer through the interfacial oxide, which separates the wafer from the SIPOS emitter, as seen in Figure 3 of Yablonovitch above. This

is apparent, because the only source of phosphorus in Yablonovitch's manufacturing process is the deposition of the SIPOS; there is no phosphorus introduced into the wafer or interfacial oxide prior to the SIPOS deposition. See EX1005 (Yablonovitch) at Table II. This phenomenon was well understood by the Skilled Artisan, as observed in Post, "in which the n⁺ dopant is diffused from the polysilicon into the underlying single-crystal silicon" through an interfacial oxide "to form a very shallow emitter/base junction." EX1016 (Post) at 1718, Fig. 1.

152. Yablonovitch's annealing step would also cause diffusion of boron through the interfacial oxide into the wafer when using Yablonovitch's p-type SIPOS. See, e.g., EX1036 (Borden) at Fig. 4 (depicting the diffusion of boron dopants from p-type polysilicon through a tunnel oxide into an n-type substrate and into about 50 nm of the substrate); EX1039 (Shimakura) §3.3, Fig. 8 ("Figure 8 shows the P-N junction depths formed in single crystalline Si by boron penetration through the SiO₂ films from doped polycrystalline Si. This figure shows that the diffusion of boron in SiO₂ films is strongly dependent on the drive-in ambients."). In fact, boron has a greater diffusivity than phosphorus in SiO₂ films such that the Skilled Artisan would expect that boron would readily diffuse into the substrate through the 2.5 to 5 nanometer, thin interfacial oxide layer of Yablonovitch. *Id.* at Abstract ("It was found that the diffusion coefficient of boron in SiO₂ is about two orders of magnitude larger than that of phosphorus."); EX1031 (Fair) at 712, Fig. 9

(diffusivity of boron greatly increases through SiO₂ for oxide thickness below 8 nanometers); EX1005 (Yablonovitch) at 1212 (“Oxide thickness between 25 and 40 Å was found to be equally favorable to the ‘emitter Gummel number.’”).

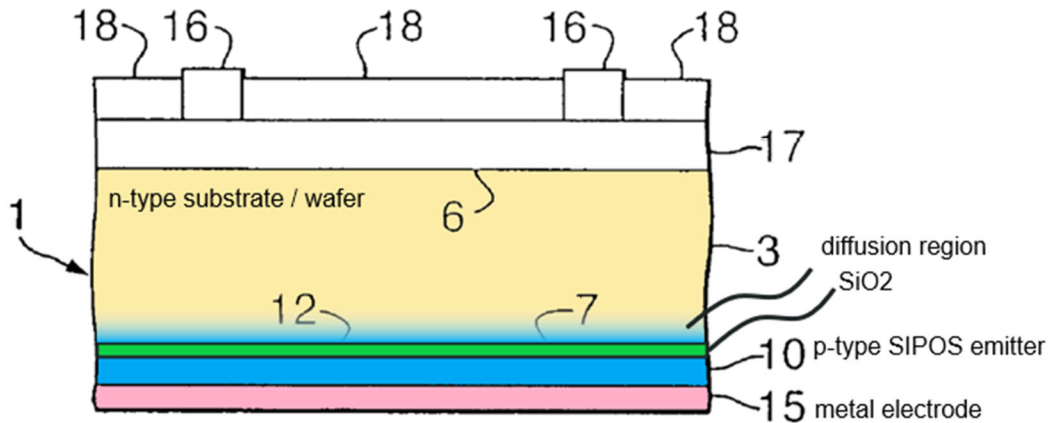
6. Claim 1(f) – Metallization

153. The next step of claim 1 is: “*providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

154. The combination of Froitzheim and Yablonovitch, depicted below, has an electrode formed from metallization (pink) that “*directly contact[s] the at least one conductive and passivating layer,*” i.e., the blue SIPOS emitter layer.

Combination of Yablonovitch and Froitzheim

Fig.1.



155. This step of the claim is found in Froitzheim. In particular, after Yablonovitch's steps of annealing the SIPOS layer (which supplanted Froitzheim's step of forming the in-substrate diffused emitter), Froitzheim discloses "*providing metallization as electrodes*" as shown in the "rear side contact 15" in Figure 1:

A rear side contact 15 is arranged in electrical connection with the p-doped layer 10. The rear side contact is shown covering a large part or substantially all of the rear side of the cell. [EX1008, ¶27.]

The Skilled Artisan would understand that the rear side contact is made of metal and acts as an electrode. Froitzheim explains that the front and rear side contacts function to "withdraw a photocurrent" or charge carriers, confirming their role as electrodes. EX1008, ¶¶2, 18, and 32. Further, in describing the rear contact of the additional embodiment in Figure 3 (in which the rear side contact 35 only covers

the rear partially), Froitzheim states that “less material such as Ag [silver] or Al [aluminum] is required for the contacts,” which indicates that the full backside contact 15 is also made of either metal. *Id.*, ¶¶20, 33.

156. Yablonovitch likewise discloses using a silver electrode. EX1005 at 1212. In general, a Skilled Artisan would know that electrodes could be made using either aluminum or silver, among other metals. Aluminum and silver were both well known materials for making contacts, with tradeoffs for better efficiency (silver) versus lower costs (aluminum). *See, e.g.*, EX1032 (Cousins) at 5:52-55 (“The metal contact 110 may comprise silver... Other metals may also be used as a metal contact 110, such as aluminum, for example.”); EX1010 (Sasaki) at 3390, Fig. 2 (comparing solar cells with silver and aluminum contacts).

157. In addition, the electrode directly contacts the SIPOS emitter (i.e., “*directly contact[ing] the at least one conductive and passivating layer*”) in the combination of Froitzheim and Yablonovitch. EX1008 (Froitzheim), ¶27 (“A rear side contact 15 is arranged **in electrical connection** with the p-doped layer 10.”).

158. As discussed in paragraphs 151-152, the annealing step in Yablonovitch (steps 8-9) also diffuses the dopant through the interfacial oxide layer and thus, also satisfies the limitation of “*the dopant diffused through the at least one interface passivation layer*” in this part of the claim.

159. As I discuss below, the combination of Froitzheim and Yablonovitch also satisfies the limitation of “*provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

160. **Combination Using Figure 1 of Froitzheim:** The combination of Yablonovitch and Froitzheim Figure 1 meets the above “*shortened charge carrier flow paths*” limitation to the same extent that (and in the same manner as) the embodiment of Figure 5 of the 074 Patent satisfies this limitation.

161. According to the 074 Patent, Figure 5 depicts a back junction solar cell with a rear contact that fully covers the back of the solar cell:

FIG. 5 shows carrier flow for a solar cell 50 from an n-type wafer 55 having **a back junction**. The majority carriers (dashed lines) can use the entire wafer conductivity to reach the front electrodes 51. **The minority carriers (solid lines) can use the shortest geometrical path to reach the rear p-type emitter 58,** and their transport within the emitter is vertical instead of mainly lateral. This back junction structure reduces the requirements for lateral conductivity of the emitter layer.

A back junction cell with a full area back contact has the advantage that the minority carriers do not have to flow laterally through the emitter to reach the contacts, their transport within the emitter is mainly vertical. This reduces the losses associated with the lateral transport of the minority carriers within the emitter. **Since the full contact area coverage is a requirement to benefit from this property of the structure, a shielded contact is important, e.g., since the metal contacts the layer everywhere (“full area contact coverage”), there is no**

need for the minority carriers to flow laterally toward the nearest contact, like they do within the emitter in, e.g., FIG. 4. [EX1001 at 4:60-5:11.]

The combination using Froitzheim Figure 1 and Yablonovitch has the same configuration as Figure 5 of the 074 Patent.¹⁰ As the embodiment in Figure 1 of Froitzheim depicts, the electrode covers substantially all of the backside of the solar cell. EX1008, Fig. 1, ¶27 (“The rear side contact is shown covering a large part or substantially all of the rear side of the cell.”). In particular, the combination of Yablonovitch and Froitzheim Figure 1 also forms a back junction solar cell with a rear p-type emitter and metal electrode that fully covers the back of the solar cell:

074 Patent, Figure 5

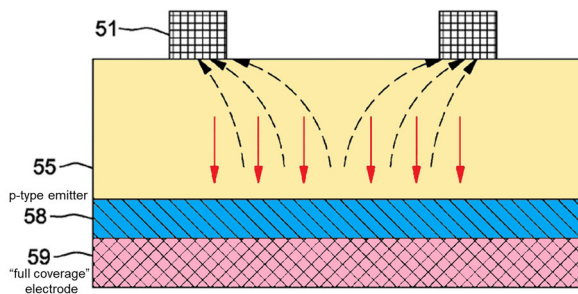
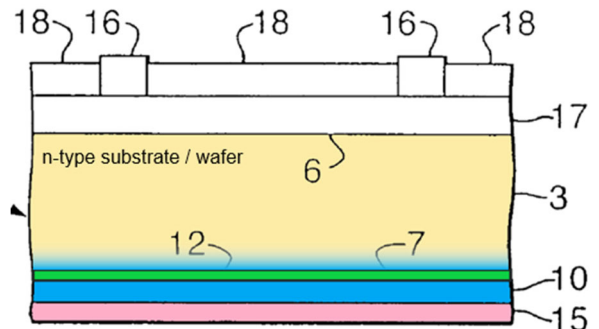


FIG. 5

Yablonovitch and Froitzheim, Fig. 1



¹⁰ Figure 3 of the 074 Patent is the same as Figure 5, but with the polarities of the substrate and emitter reversed (i.e., a p-type substrate and an n-type emitter).

EX1001 at 4: 44-51. Thus, this discussion equally applies to the combination of Froitzheim and Yablonovitch that has a p-type substrate and n-type SIPOS emitter.

162. According to the 074 Patent, the back junction configuration in Figure 5 with a full rear metallization causes the charge carrier flow paths (colored red) to be shortened, because the minority carriers (i.e., electrons in the case of Figure 5) can propagate directly vertically to the emitter and electrode without having to traverse horizontally:

FIG. 5 shows carrier flow for a solar cell 50 from an n-type wafer 55 having a back junction. The majority carriers (dashed lines) can use the entire wafer conductivity to reach the front electrodes 51. **The minority carriers (solid lines) can use the shortest geometrical path to reach the rear p-type emitter 58,** and their transport within the emitter is vertical instead of mainly lateral. This back junction structure reduces the requirements for lateral conductivity of the emitter layer.

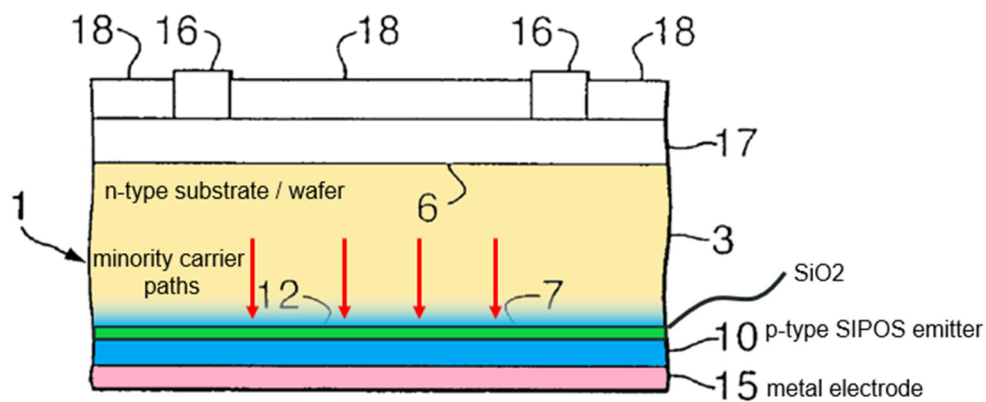
A back junction cell with a full area back contact has the advantage that the minority carriers do not have to flow laterally through the emitter to reach the contacts, their transport within the emitter is mainly vertical. This reduces the losses associated with the lateral transport of the minority carriers within the emitter. Since the full contact area coverage is a requirement to benefit from this property of the structure, a shielded contact is important, e.g., **since the metal contacts the layer everywhere (“full area contact coverage”), there is no need for the minority carriers to flow laterally toward the nearest contact,** like they do within the emitter in, e.g., FIG. 4. [EX1001 at 4:60-5:11.]

163. Accepting the 074 Patent’s description of Figure 5, the combination of Yablonovitch and Froitzheim Figure 1 would thus have shortened charge carrier

paths using the same reasoning.¹¹ That is, because the combination using Figure 1 has a back junction emitter and a full area backside contact, minority carriers in the substrate can flow directly vertically through the SIPOS emitter to the electrode, thus allowing for shortened current flow paths, as depicted below:

Combination of Yablonovitch and Froitzheim Fig. 1

Fig. 1.

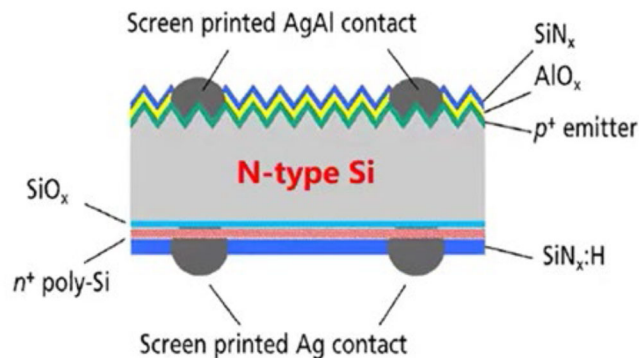


164. Thus, to the extent Figure 5 (or Figure 3) of the 074 Patent satisfies this limitation of claim 1, the combination of Yablonovitch and Figure 1 of Froitzheim would do so as well.

¹¹ I understand that Patent Owner appears to assert that Figure 5 of the 074 Patent does in fact practice the “*shortened charge carrier paths*” limitation in the district court complaint. EX1024 ¶81.

165. **Combination Using Figure 3 of Froitzheim:** I understand that in its district court complaint, the Patent Owner has taken the position that localized metal contact that does not cover substantially all of the backside of Petitioner’s accused solar cells nevertheless “provide metallization as electrodes” such that there are “shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer”. EX1024 (Complaint), ¶¶79-81. Under Patent Owner’s infringement rationale in its complaint, the combination of Yablonovitch and Froitzheim Figure 3 would also meet limitation 1(f) of claim 1.

166. In particular, I understand that in its district court complaint, Patent Owner alleges that:



The phosphorus dopant that is diffused from the conductive and passivating layer (the “n+ poly-Si” layer) in the Canadian Solar TOPCon solar cell through the interface passivation layer (the “SiO_x” layer) provides shortened charge flow paths between the substrate (the “N-type Si” layer) and the electrodes through the conductive and passivating layer (the “n+ poly-Si” layer)

and interface passivation layer (the “SiOx” layer). This is reflected in the smooth transition of phosphorus levels shown in the graph above, resulting in higher conductivity near the back surface of the substrate compared to an assembly that does not have dopant diffused through the interface passivation layer. This causes charge flow paths to curve toward the electrodes, shortening them as illustrated in concept in Figure 5 of the ’074 Patent and described above. Thus, Canadian Solar practices the method of Claim 1 of the ’074 Patent. [EX1024, ¶81.]

167. According to the image above from Patent Owner’s complaint, the silver “screen printed Ag contact” on the back of the solar cell do not cover the entire back surface of the cell, they are localized and only cover small portions of the back surface of the solar cell.

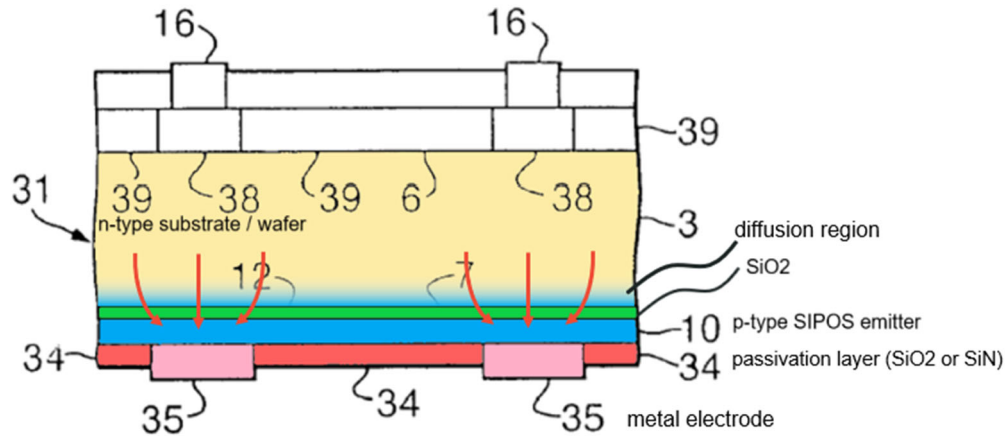
168. I have not analyzed Petitioner’s accused solar cells and thus do not opine on the charge carrier paths or the nature of any dopant diffusion in Petitioner’s accused products, nor have I been asked to do so. Nevertheless, accepting Patent Owner’s allegations in its complaint, the combination of Yablonovitch and Froitzheim Figure 3 also meets the “*shortened charge carrier flow paths*” limitations using the Patent Owner’s reasoning.

169. In particular, the combination of Froitzheim Figure 3 and Yablonovitch, depicted below, has a series of finger electrodes formed from metallization (pink) on only part of the rear side that “*directly contact the at least*

one conductive and passivating layer,” i.e., the blue SIPOS emitter layer, through the red passivation layer 34.

Combination of Yablonovitch and Froitzheim Fig. 3¹²

Fig.3.



170. The Patent Owner’s district court complaint explains that the “curved path between the electrodes and the substrate as represented by the dashed lines in Figure 5” of the 074 Patent represents “shortened” flow path. EX1024, ¶57. And a shortening “similar in concept to that which is shown in Figure 5” occurs, according to Patent Owner’s complaint, when “[t]he area where the dopant ... is incorporated into the interface passivation layer and ... the substrate makes the silicon in those areas more conductive and forms low resistance pathways through

¹² According to Patent Owner’s allegations in the district court complaint (EX1024) at ¶¶79-81.

those layers along which electrons can more easily travel.” EX1024, ¶58. Patent Owner states that “the diffusion of dopant into these layers thus increases the conductivity of the solar cell near the back surface of the silicon substrate ... such that that its conductivity is more similar to the conductivity of the conductive and passivating layer.” *Id.* “As a result, [the Patent Owner explains that] charges take a more direct route from the substrate toward the electrodes affixed to the back of the solar cell than they would otherwise without the diffusion of the dopant, similar in concept to that which is shown in Figure 5.” *Id.* The Patent Owner further expands that the diffusion of the dopant through the interface passivation layer “result[s] in higher conductivity near the back surface of the substrate compared to an assembly that does not have dopant diffused through the interface passivation layer. This causes charge flow paths to curve toward the electrodes, shortening them as illustrated in concept in Figure 5 of the 074 Patent.” *Id.* ¶81. Assuming Patent Owner’s contention and reasoning as true, the combination of Yabonovitch with FIG. 3 of Froitzheim similarly satisfies this limitation of claim 1 because the dopant similarly diffuses from the SIPOS into the substrate through the interfacial oxide layer, creating higher conductivity in the back surface of the substrate, thus resulting in this shortened, curve flow path similar to concept to what occurs in the front portion of FIG. 5 of the 074 Patent, based on Patent Owner’s explanation.

7. Claim 2 – Antireflective Layer

171. Claim 2 depends from claim 1 and adds the additional step: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

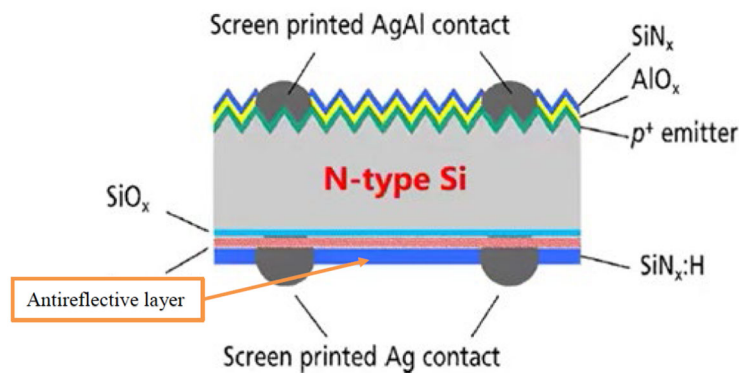
172. I understand that, in Patent Owner’s district court complaint, the Patent Owner asserted that

[m]etal electrodes are added to the cells such that they directly contact the conductive and passivating layer to form an electrical connection thereto. The diagram below shows that the electrodes (the “Screen printed Ag contact”) directly contact the orange-colored n^+ poly-Si layer. As shown in the diagram below, **the antireflective layer (or coating) deposited on the back of the Canadian Solar TOPCon cells is silicon nitride (the “SiN_x:H” layer). SiN_x is an electrical insulator, so the electrodes of the Canadian Solar TOPCon solar cells must make direct contact with the conductive and passivating layer to allow an electric current to pass through that layer.** Otherwise, the antireflective layer would restrict the flow of electricity between the electrodes and the conductive and passivating layer.

...

The manufacture of Canadian Solar’s TOPCon solar cells includes depositing at least one antireflective layer, **a silicon nitride antireflective coating (the blue “SiN_x:H” layer in the image below),** on the back of the solar cell. The antireflective layer is used to increase absorption, and minimize reflection, of light energy that hits the solar cell from the back (because the device is bifacial and accepts light from both the front and back sides of the device). Silicon nitride has a refractive index (a measurement of how much light bends when entering a material) well below 3.0 and therefore forms a good internal mirror on the inside surface of the antireflective layer, such that light

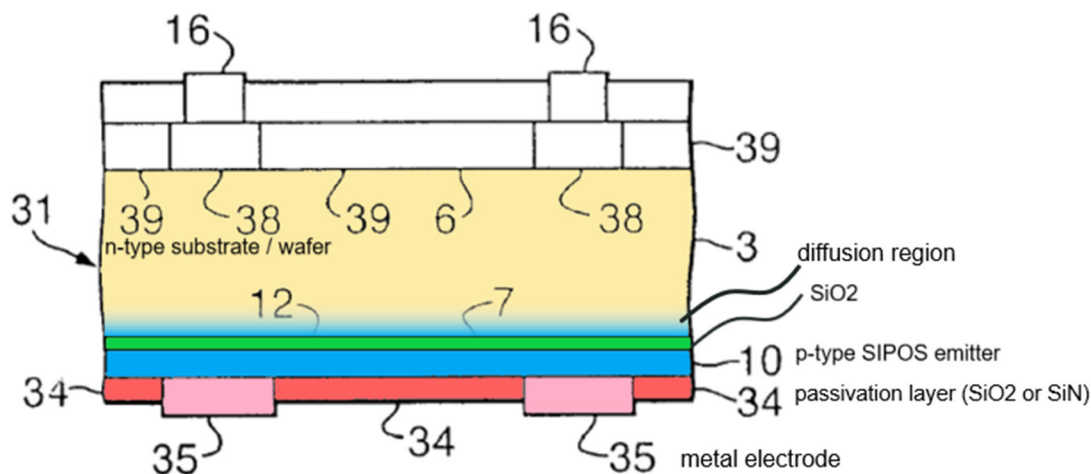
that passes through the solar cell from the front is reflected by the antireflective layer back into the cell so as to excite additional electrons. **In this way, the antireflective layer is akin to a one-way mirror allowing light from the back side to pass through, while reflecting light from the front side back into the cell.** [EX1024 ¶¶79, 82.]



174. According to Patent Owner’s theory, the combination of Yablonovitch and Figure 3 of Froitzheim, depicted below, has a red passivation layer made of silicon nitride (SiN) or silicon oxide (SiO₂) that is an “*antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

Second Combination of Yablonovitch and Froitzheim Fig. 3¹³

Fig.3.



175. Assuming the Patent Owner’s theory in district court, this step of the claim is also found in Froitzheim, in which Froitzheim discloses that the “[p]assivation and antireflection coating can be applied using known methods, before or after contact formation.” EX1008, ¶50. According to Froitzheim, the passivation layer 18 on the *front* of the solar cell can be made of “an oxide such as SiO₂, [or] a nitride such as SiN,” formed “using methods known in the art.” EX1008, ¶30. Then, “[b]etween the [rear] fingers a passivation layer 34 is arranged, for which the same type of layers can be used as for the front side.”

¹³ According to Patent Owner’s allegations in the district court complaint (EX1024) at ¶82.

EX1008, ¶33. That is, the rear passivation layer 34 in Froitzheim can also be made of either SiN or SiO₂. In reporting on his testing, Froitzheim further discloses that silicon nitride “SiN was used in all cases as antireflection as well as surface coating for n- and p-type silicon.” EX1008, ¶60.

176. As discussed above, Patent Owner contends that a SiN layer satisfies claim 2 in the district court complaint. EX1024, ¶82 (“Silicon nitride has a refractive index (a measurement of how much light bends when entering a material) well below 3.0 and therefore forms a good internal mirror....”). Assume for purposes here that Patent Owner is correct, then the SiN passivation layer 34 in the combination of Yablonovitch and Figure 3 of Froitzheim would also be *“antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell,”* since it is the exact same material: silicon nitride.

177. Separately, the 074 Patent also identifies silicon nitride and silicon oxide as example of antireflective layers with indices of refraction between 1.4 and 3. EX1001 at 6:47-50. This is further evidence that the passivation layer 34 in the combination of Yablonovitch and Froitzheim, which can be either silicon nitride or silicon oxide, satisfies claim 2 under Patent Owner’s theory in the district court complaint. EX1008 (Froitzheim), ¶30.

8. Claim 4 – Perforation

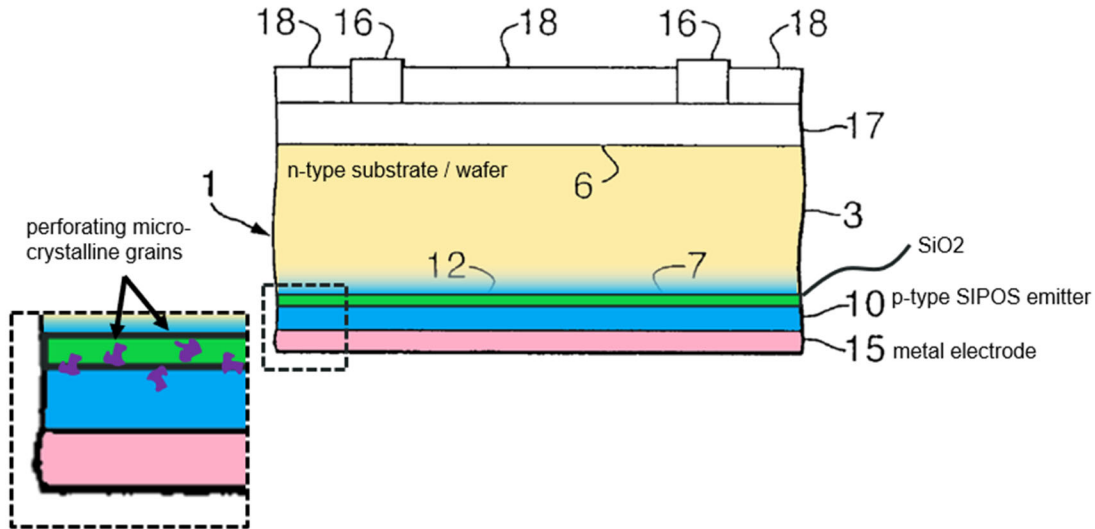
178. Claim 4 depends from claim 1 and adds the additional step: “*wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.*”

179. As noted above, during prosecution, the patent applicant made repeated arguments to the examiner to overcome rejections appearing to disclaim from the scope of the claims any fabrication process that requires boring through other layers of the solar cell to enable electrical contact between the electrode and the substrate. *See above* §III.D.

180. Nevertheless, to the extent Patent Owner contends there is no such disclaimer, the combination of Yablonovitch and Froitzheim, depicted below, has grains of microcrystalline silicon (purple) that protrude (*perforate*) into the green SiO₂ interfacial oxide (*interface passivation layer*) as a result of the annealing process (*thermal treatment*) to enable current to pass through the interfacial oxide (*to allow carrier transport therethrough*).

Combination of Yablonovitch and Froitzheim

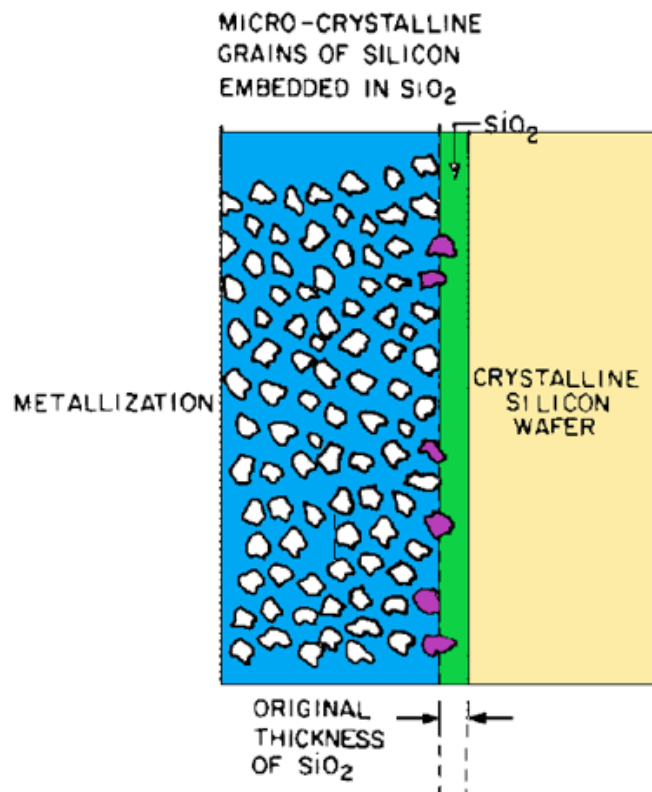
Fig.1.



181. This step of the claim is found in Yablonovitch, in particular, in the annealing steps 8 and 9 of Yablonovitch. EX1005, Table II. As Figure 3 of Yablonovitch depicts (below), some microcrystalline grains (colored purple) penetrate into the SiO₂ layer as a result of the annealing step. EX1005 at Fig. 3. Yablonovitch explains that these silicon grains enable charge carriers to pass through the SiO₂ layer: “We believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO₂.” EX1005 at 1213, Fig. 3 (“Electron conduction is thought to proceed via the microcrystalline grains which protrude into the thin oxide layer.”). According to

Yablonovitch's experiments, "[t]he individual [silicon grain] contacts provide more than enough conductivity for majority-carrier electrons." EX1005 at 1213.

Yablonovitch, Fig. 3



182. Silicon oxide is an insulator that under normal operating conditions does not conduct current. EX1018 (Quirk) at 34 ("SiO₂ is a high-quality, stable electrical insulator..."). Moreover, Yablonovitch explains that the thickness of the interfacial oxide, 25-40Å, means that the oxide layer is too thick to allow electron tunneling to occur through the oxide.

Oxide thickness between 25 and 40 Å was found to be equally favorable with respect to the 'emitter Gummel number.' Therefore, differential tunneling between electrons and holes does not appear to be playing a major

role because **over part of this range the oxide is too thick for electron tunneling.** [EX1005 at 1212-13.]

Because the interfacial oxide is electrically insulating and too thick to allow electron tunneling, at least in portions, the *only* way for electrons or other charge carriers to pass from the substrate through the interfacial oxide to the SIPOS layer is by conducting through the microcrystalline silicon grains protruding into the interfacial oxide layer.

9. Claim 5 – Crystallization

183. Claim 5 depends from claim 1 and adds the additional step: “*wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.*”

184. The SIPOS layer (*conductive and passivating layer*) in the combination of Froitzheim and Yablonovitch “*comprises an amorphous, silicon containing compound.*” SIPOS stands for “semi-insulating polycrystalline silicon” that is formed in Yablonovitch’s SIPOS deposition step by a mixture of silane (SiH₄), phosphine (PH₃), and oxygen (O₂). EX1005 at Table II, 1211. Silane contains silicon (Si), such that as-deposited SIPOS also contains silicon and is a “*silicon containing compound*”.

185. In addition, Yablonovitch’s as-deposited SIPOS layer, deposited at 650°C, is amorphous. E.g., EX1013 (Fussel) at abstract (“As-deposited [SIPOS]

layers are predominantly amorphous....”), 355 (“The results shown in fig. 1 indicate a predominantly amorphous structure for the as-deposited [SIPOS] layers with a very low density of Si microcrystallites....”); EX1007 (Kwark II) at 1121 (“As deposited, SIPOS is usually amorphous.”); EX1025 (Kwark III) (“SIPOS films prepared at 650°C are amorphous;”). As Yablonovitch explains, annealing at 900°C (*thermal treatment*) is needed to crystalize the as-deposited amorphous SIPOS into microcrystalline silicon grains:

The annealing step (9) follows SIPOS deposition. **This step is necessary to precipitate microcrystalline silicon grains** within the material and to activate the phosphorus dopant. [EX1005 at 1212.]

Elsewhere, Yablonovitch observes that “[i]n its annealed form [SIPOS] is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x).”

EX1005 at 1211.

186. Finally, the crystalline grains formed as a result of the annealing step in Yablonovitch are *polycrystalline*, such that Yablonovitch’s annealing step converts the amorphous SIPOS layer into a “*polycrystalline film*.” This is disclosed by Yablonovitch, which notes that SIPOS stands for “semi-insulating polycrystalline silicon.” EX1005 at 1211. Others in the art also characterized SIPOS as polycrystalline. *E.g.*, EX1035 (Matsushita) at abstract (“SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.”). As was known in the art prior to the 074 Patent, SIPOS is essentially a

material somewhere between the limiting cases of pure polysilicon¹⁴, on the one hand, and pure SiO₂, on the other hand, depending on the oxygen content. EX1007 (Kwark II) at 1121 (“SIPOS, for Semi-Insulating Poly-crystalline Silicon, has become the generic acronym for deposited silicon films doped with oxygen.... Indeed, normal poly-silicon and SiO, can be thought of as the limiting cases of no oxygen and full oxidation.”).

10. Claim 6 – Transmissivity

187. Claim 6 depends from claim 1 and adds the additional step: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and [b] increases the optical transmissivity.*”

188. Part [a] of claim 6 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer.*” I discussed how the combination of Froitzheim and Yablonovitch satisfies this limitation in Paragraphs 183-186 above.

¹⁴ Polysilicon is a common shorthand for polycrystalline silicon.

189. As for part [b], in the combination of Froitzheim and Yablonovitch, Yablonovitch's annealing step (*thermal treatment*) further "*increases the optical transmissivity*" of the SIPOS layer (*conductive and passivating layer*). In particular, Yablonovitch disclosed depositing the SIPOS layer at 650°C and then annealing the SIPOS layer at 900°C to form microcrystalline silicon grains. EX1005 at Table II, 1212-13 ("This [annealing] step is necessary to precipitate microcrystalline grains within the [SIPOS] material...."). Yablonovitch explains that the particular chemical mixture Yablonovitch uses to form the SIPOS layer results in "5% oxygen incorporation." Yablanovitch at 1213.

190. SIPOS annealed at 900°C with 5% oxygen is more transmissive than SIPOS as-deposited at 650°C. For example, Pan et al. investigated the "optical absorption characteristics of SIPOS." EX1015 ("Pan"), §1. In the study Pan prepared "SIPOS films deposited at 650°C," and observed that "[a]nnealing at different temperatures has modified the optical absorption of the films." *Id.* §§2.1, 3. The relationship between annealing temperature and optical absorption for SIPOS films with 8% oxygen content is graphed in Figure 4 of Pan, reproduced with annotations below. *Id.* §3, Fig. 4. As shown, the optical absorption was greater for the as-deposited SIPOS films than for films annealed at 900°C.

Pan, Fig. 4

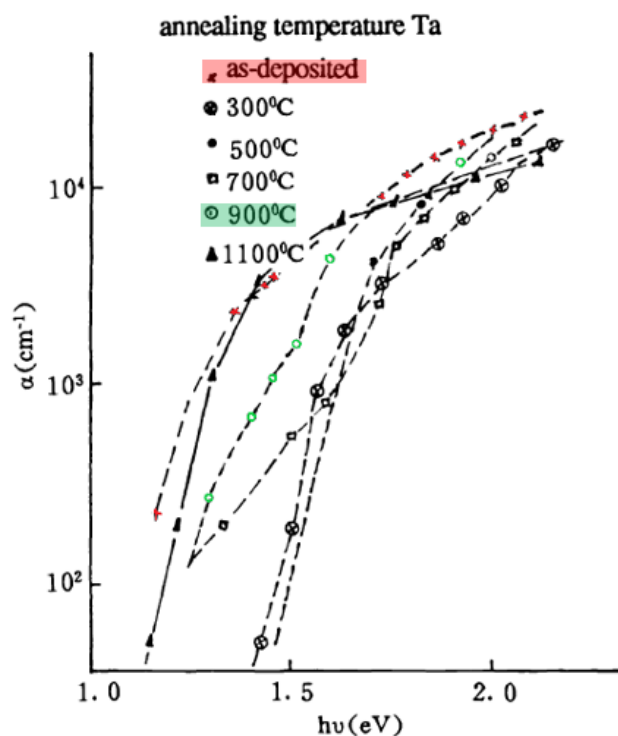


Fig. 4 Changes in optical absorption of SIPOS films (8 at.%) with annealing temperature T_a .

191. Optical absorption is the inverse of transmissivity. That is, the more light that is absorbed by a SIPOS layer, the less light that is transmitted through the layer. Accordingly, Pan shows that SIPOS crystallized at 900°C has greater optical transmissivity than amorphous SIPOS deposited at 650°C. Similar results have been obtained by others. For example, Compagnini discloses that the optical transmission increases when SIPOS films are annealed, and the transmittance increases with increasing anneal temperature. EX1014 at 886 (Figure 1) and at 890 (Figure 8).

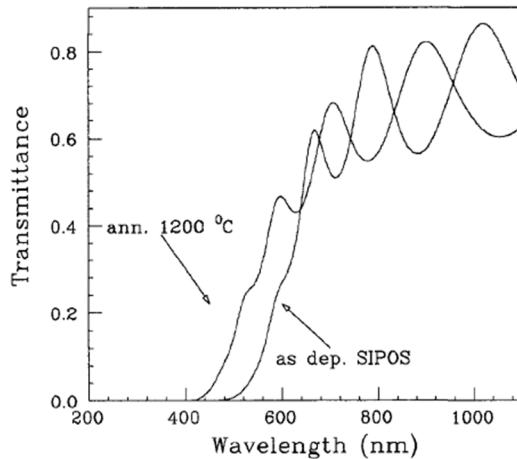


FIG. 1. Transmission curves in the fundamental absorption region for as-deposited and 1200 °C samples.

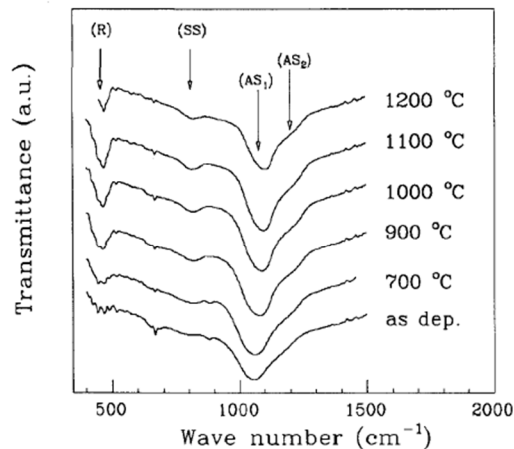


FIG. 8. Infrared absorption data in the region of the Si-O allowed vibrations.

And in general, crystallized silicon is more optically transmissive than amorphous, as-deposited silicon. For example, as reported by Janai et al., when silicon crystallizes as a result of annealing, “the absorption profile shifts back to higher energies and approaches that of single-crystal silicon.” EX1037, at 16, Fig. 1. In other words, the transmissivity of the polysilicon goes up across a broad spectrum of wavelengths.

192. The annealed SIPOS layer of Yablonovitch, therefore, has greater optical transmissivity (and less absorption) than the as-deposited SIPOS layer, such that the thermal treatment annealing of Yablonovitch increased the optical transmissivity.

11. Claim 7 – Dopant Activation

193. Claim 7 depends from claim 1 and adds the additional step: “*wherein* [a] *the at least one conductive and passivating layer comprises an amorphous,*

silicon containing compound, and [b] wherein the thermal treatment activates doping atoms in the compound.”

194. Part [a] of claim 7 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound.*” I discussed how the combination of Froitzheim and Yablonovitch satisfies this limitation in Paragraphs 183-186 above.

195. As for part [b], in the combination of Froitzheim and Yablonovitch, Yablonovitch’s annealing step (*thermal treatment*) further activates phosphorus, an n-type dopant, in the SIPOS layer (“*activates doping atoms in the compound*”). In particular, Yablonovitch disclosed:

The annealing step (9) follows SIPOS deposition. **This step is necessary** to precipitate microcrystalline silicon grains within the material and **to activate the phosphorus dopant.** [EX1005 at 1212.]

The SIPOS layer in Yablonovitch was doped with phosphorus in situ during the SIPOS deposition step, which included deposition of phosphine (PH₃). EX1005, Table II.

196. The dopant activation process is further explained by Quirk, EX1018. As Quirk explains, “[d]opants are useful to form semiconductor silicon only if they are activated dopants, meaning they are part of the silicon lattice structure.” EX1018 at 480. Dopants become activated when thermal energy, for example, energy imparted as a result of annealing, moves a dopant into a regular crystal site.

Id. (“Thermal energy moves dopants into the regular crystal sites, a process known as crystal activation.”). This dopant activation process works the same for both p-type and n-type dopants. *Id.* (“An activated dopant can act as a donor or acceptor of electrons and is an n-type or p-type dopant with respect to silicon.”). Thus, Yablonovitch’s anneal step would also activate p-type dopants (boron) in p-type SIPOS in the same manner as the phosphorus activation disclosed in Yablonovitch.

12. Claim 8 – PN Junction

197. Claim 8 depends from claim 1 and adds the additional step: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.*”

198. Part [a] of claim 8 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound.*” I discussed how the combination of Froitzheim and Yablonovitch satisfies this limitation in Paragraphs 183-186 above.

199. As for part [b], in the combination of Froitzheim and Yablonovitch, Yablonovitch’s annealing step (*thermal treatment*) results in the “*diffusion of dopant atoms into the substrate*”. In particular, Yablonovitch disclosed:

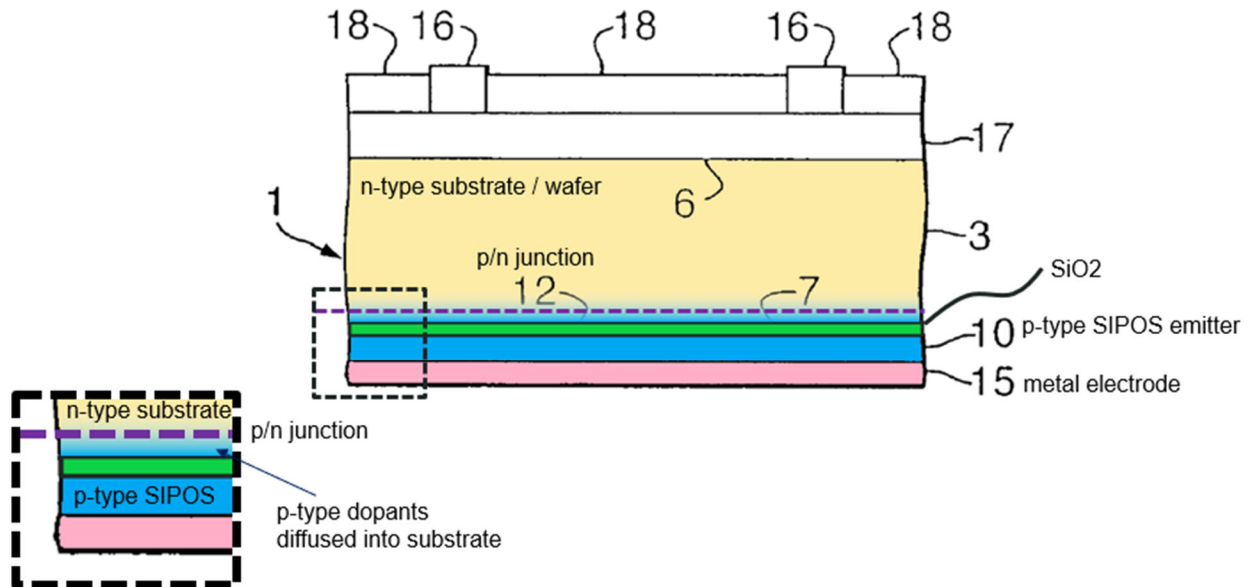
The annealing step (9) follows SIPOS deposition.... In addition **during this step the phosphorus diffuses about**

20-50 Å into the silicon wafer as measured by secondary ion mass spectrometry. [EX1005 at 1212.]

200. The same result would occur when annealing a p-type SIPOS layer, in that the p-type dopants (boron) would likewise outdiffuse through the interfacial oxide layer and into the substrate, as I discussed in paragraphs 152 above. In the combination of Froitzheim and Yablonovitch, depicted below, the diffusion of p-type dopants into the n-type substrate forms “*a p-n junction*”. Froitzheim expressly disclose that the formation of a p-type diffused emitter on the back of an n-type substrate results in a pn junction. EX1008, ¶¶7, 25. Replacing Froitzheim’s diffused in-substrate emitter with Yablonovitch’s SIPOS emitter and interfacial oxide does not change that. Moreover, whether the combination of Froitzheim and Yablonovitch is made using an n-type wafer and a p-type SIPOS emitter, or a p-type wafer and an n-type SIPOS emitter, either way the diffusion of the dopants from the emitter into the substrate results in a junction where p- and n-type dopant regions come together, thus forming a pn junction. EX1019 (Luque) at 83.

Combination of Yablonovitch and Froitzheim

Fig.1.



VII. CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, YABLONOVITCH, AND NEVILLE

201. In my opinion, the combination of Froitzheim and Yablonovitch in further view of Neville rendered obvious claims 1, 2, and 4-8 of the 074 Patent.

202. I understand that Petitioner is asserting two distinct but similar grounds in the Petition, Ground I consisting of Froitzheim and Yablonovitch and Ground II consisting of Froitzheim, Yablonovitch, and Neville. As I explained in Section VI above, the combination of Froitzheim and Yablonovitch discloses each and every limitation of claims 1, 2, and 4-8, and render these claims obvious.

203. Nevertheless, to the extent Patent Owner might argue that Yablonovitch does not disclose a p-type SIPOS emitter, Neville makes clear that the Skilled Artisan would understand that the dopant type of Yablonovitch's n-type SIPOS, or Froitzheim's p-type substrate, could be reversed. In particular, Figure VI.1 of Neville depicts a variety of possible solar cell configurations including a back junction cell like Froitzheim, which has a substrate that is either "p or n" type and a backside emitter that is either "n or p" type. EX1009 at Fig. VI.1, 199-200; see also Paragraphs 102-103 above. The use of p-type substrate was well within the skill of the Skilled Artisan because p-type silicon substrates were so widely used before 2008.

204. Neville thus merely confirms that the Skilled Artisan would have no difficulty in combining Froitzheim and Yablonovitch, for example, because the Skilled Artisan would understand that Froitzheim's substrate can be readily reversed from n-type to p-type. Confirmation that the reversing the dopant of the substrate and SIPOS emitter was well known is also evidenced by the Spitzer and Yablonovitch patents. EX1034 (Spitzer) (disclosing that for a back junction cell, the wafer (i.e., substrate) "may be formed of an n-type or p-type silicon."); EX1011 (Yablonovitch patent) at 2:16-19 ("The solar cell of the present invention shall be illustrated and described by a cell with p doped crystalline silicon and n-doped SIPOS. It is to be understood that the doping types may be interchanged.").

Making this modification is well within the skill of the Skilled Artisan who would have reasonably expected to be able to make such a modification and to use a p-type substrate with an n-type SIPOS emitter.

205. The combination of Froitzheim, Yablonovitch, and Neville, thus further renders obvious claims 1, 2, and 4-8, for the same reasons as discussed above in Section VI.

VIII. CLAIM 2 IS UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, YABLONOVITCH, AND SASAKI

206. In my opinion, the combination of Froitzheim, Yablonovitch (and Neville), in further view of Sasaki (EX1010) further rendered obvious claim 2 of the 074 Patent.

A. The Combination of Froitzheim, Yablonovitch, and Sasaki

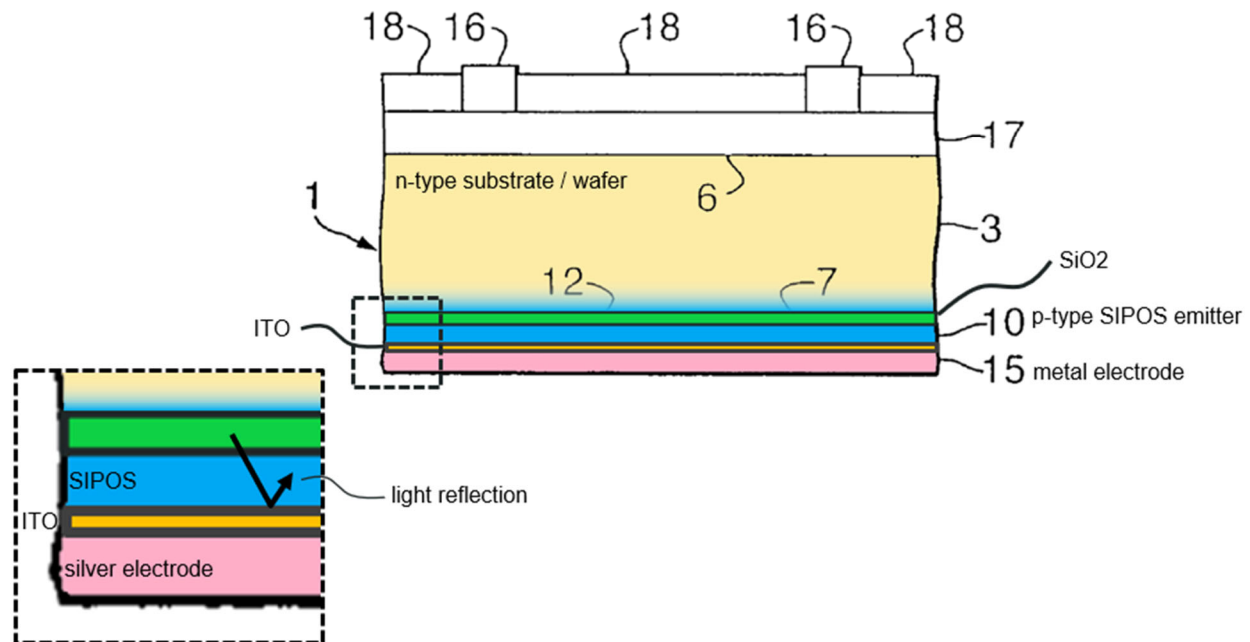
207. As discussed in more detail in the next section, Sasaki discloses inserting a transparent conductive indium tin oxide (ITO) film between an aluminum or silver contact and a silicon substrate in a solar cell. EX1010 at 3390.

208. In my opinion, it would have been obvious to a Skilled Artisan to further modify the combination of Froitzheim and Yablonovitch by inserting the additional step of forming an ITO film as taught by Sasaki between the steps of forming the SIPOS emitter and forming the metal electrode, based on Sasaki's teachings that doing so would increase efficiency, as discussed more below. An exemplary device made using this combined method is illustrated in the figure

below, in which Sasaki's ITO film (orange) is inserted between Yablonovitch's SIPOS emitter (blue) and Froitzheim's rear electrode (pink).

Combination of Froitzheim, Yablonovitch, and Sasaki

Fig. 1.



B. Sasaki Discloses the Method Step of Claim 2

209. Claim 2 depends from claim 1 and adds the additional step: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

210. Even if Patent Owner were to argue that the combination of Froitzheim and Yablonovitch does not disclose the claim 2 step of depositing an antireflective layer to form a good internal mirror, Sasaki also discloses this step.

211. In particular, Sasaki sought to improve over existing solar cells that used aluminum rear metal contacts by using silver contacts with a transparent conductive indium tin oxide (ITO) film:

In order to realize reflectivity higher than that of conventional aluminum (Al) metal, we have adopted silver (Ag) metal and **a transparent conductive indium tin oxide (ITO) film inserted between the thin Si film and Ag layer.** [EX1010 at 3390.]

In Figure 2 below, the silicon substrate is colored blue, the ITO film is colored orange, and the aluminum/silver contacts are colored pink. The internal reflection of light coming in through the front of the solar cell and reflecting at the back surface of the substrate is depicted by the arrows.

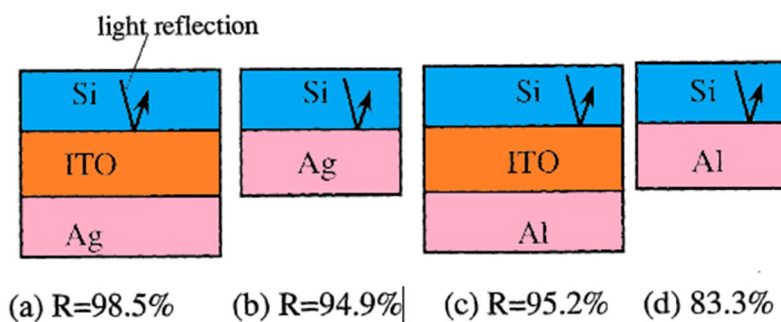


Fig. 2. Calculated reflectances for four different conditions of rear reflectors at opening.

212. Sasaki discloses that by including an ITO film between the silicon substrate and a silver electrode, the internal reflectivity of the solar cell went up from 94.9% to 98.5% compared to a solar cell with a silver contact and no ITO film. *Id.* Even for cheaper solar cells with aluminum contacts, adding the ITO

layer between the substrate and the contact increased internal reflectivity from 83.3% to 95.2%. *Id.* Sasaki's ITO film thus "*form[s] a good internal mirror on a back of the solar cell,*" because it increases the internal reflectivity of solar cells having either aluminum or silver contacts.

213. Moreover, the 074 Patent identifies that the "transparent and conductive film" is used as a "a low reflective index layer good internal mirror on the back," and indium tin oxide (the same material as Sasaki's ITO film) is an example of such transparent and conductive film. EX1001 at 6:18-24; 15:31-35. This is further evidence that the ITO film in Sasaki meets the limitation of claim 2, because the ITO film is an "*a low reflective index layer forming a good internal mirror on a back of the solar cell*" according to the 074 Patent. See also, *id.*, at 18:24-28.

C. Motivation to Combine Froitzheim and Yablonovitch with Sasaki's ITO Film

214. Sasaki, Froitzheim, and Yablonovitch are analogous art because each is in the same field of endeavor—solar cell design. EX1008 (Froitzheim), Abstract, ¶¶1, 9; EX1005 (Yablonovitch), Abstract, 1211-12; EX1010 (Sasaki) at abstract, 3389. Each is reasonably pertinent to the problems of efficiency and cost-effectiveness of solar cell designs. EX1008 (Froitzheim), Abstract, ¶¶1, 9; EX1005 (Yablonovitch), Abstract, 1211; EX1010 (Sasaki) at abstract, 3389.

215. In my opinion, by April 2009, the Skilled Artisan would have been motivated to insert Sasaki's ITO film between the SIPOS emitter as taught by Yablonovitch and the rear metal electrode as taught by Froitzheim, because Sasaki disclosed that the ITO film would improve the internal reflectivity of the back surface of the solar cell for both silver and aluminum electrodes, and thus the quality and efficiency of the solar cell compared to those that lacked the ITO film. In particular, Sasaki observed that by including an ITO film between the silicon substrate and a silver electrode, the internal reflectivity of the solar cell went up from 94.9% to 98.5%, and adding the ITO layer between the substrate and an aluminum contact increased internal reflectivity from 83.3% to 95.2%. EX1010 at 3390.

216. Increasing the internal reflectivity of the rear surface of the solar cell is important and advantageous because it increases the number of photons that are converted into energy in the solar cell. Not every photon is absorbed and results in the generation of an electron/hole pair on the first pass through the solar cell. Once a photon passes completely through a solar cell, it is no longer available to form an electron/hole pair, and thus generate electrical current. However, by increasing the internal reflectivity at the back surface of a solar cell, some of photons of sunlight that enter the front of solar cell and pass unabsorbed through the substrate may get reflected at the back surface, rather than exiting the solar cell. Upon reflection, the

photons then pass back through the solar cell, effectively doubling the probability that the photons will be absorbed. Internal reflectivity is therefore one way to increase a solar cell's efficiency in converting photons into electrical current.

217. Although Sasaki discloses the use of transparent and conductive oxide films in a thin-film solar cell, the Skilled Artisan would understand and be motivated to equally apply this to the Froitzheim/Yablonovitch solar cell made from crystalline solar wafers. Even before 2008, these films were well known and have been used with heterojunction solar cells made from crystalline solar wafers, which have a very similar structure to the proposed combination. EX1019 at 289 (Fig. 7.14) (“On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed” on top of the TCO layers; “Mass production of HIT cells started in 1997”).

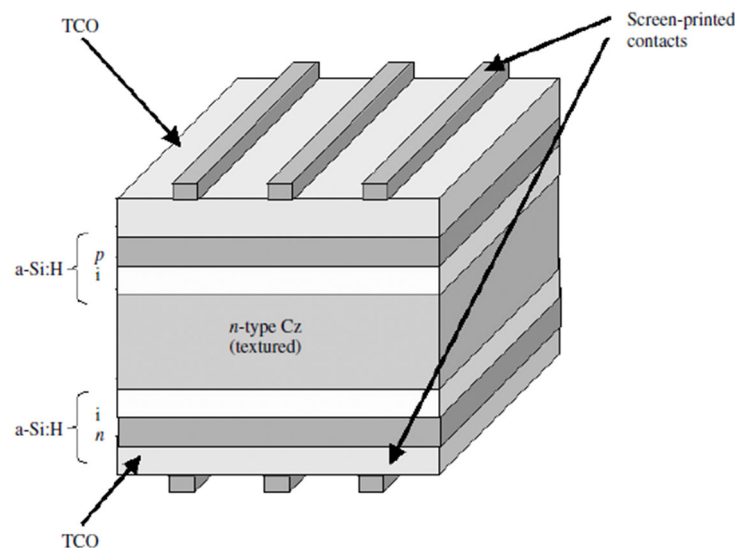


Figure 7.14 Structure of the HIT cell

D. Reasonable Expectation of Success

218. Inserting the ITO film of Sasaki between the SIPOS emitter layer and rear metal electrode in the combination of Yablonovitch and Froitzheim, would have been well within the level of the Skilled Artisan by 2009. It would have been a simple addition of a known element for another to obtain predictable results.

219. Specifically, after completing Yablonovitch's steps of depositing the SIPOS emitter and annealing the solar cell, EX1005 at Table II (steps 7-12), the Skilled Artisan would perform the step of depositing the ITO layer as taught by Sasaki, EX1010 at 3390, before proceeding to Froitzheim's step of forming the rear metal contacts, EX1008, ¶¶48-49. The result would be a solar cell with increased internal reflectivity at the rear surface, as reported by Sasaki. EX1010 at 3390. Such a modification would further constitute use of a known technique (depositing and ITO film) to improve similar devices (Froitzheim's back junction solar cell) in the same way. It would also constitute applying a known technique to a known device ready for improvement to yield predictable results.

220. Combining Froitzheim/Yablonovitch with Sasaki as described here would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished with a reasonable expectation of success. Even before 2008, forming a TCO layer on top of deposited doped layers were well known and well within the skill of the

Skilled Artisan. See EX1019 at 289 (Fig. 7.14) (“On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed” on top of the TCO layers). The combinations would simply have been the combination of prior art elements according to known methods to yield predictable results, namely, the straightforward deposition of an indium tin oxide layer according to standard, well-known deposition techniques.

IX. CLAIMS 1-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM AND KWARK

221. In my opinion, the combination of Froitzheim and Kwark would have rendered obvious claims 1-8 of the 074 Patent.

A. The Combination of Froitzheim and Kwark

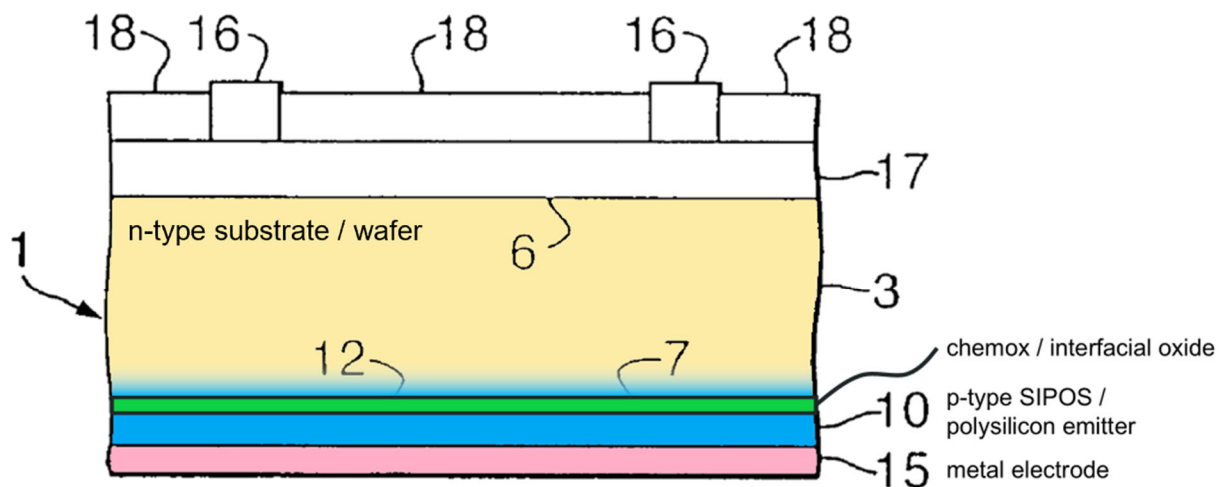
222. The combination of Froitzheim and Kwark is very similar to the combination of Froitzheim and Yablonovitch discussed above.

223. In my opinion, it would have been obvious to a Skilled Artisan to modify Froitzheim’s method of forming a solar cell by replacing the step of forming the emitter of Froitzheim with Kwark’s steps for forming a SIPOS/polysilicon emitter and interfacial oxide, based on Kwark’s teachings that doing so would reduce recombination and increase efficiency, as discussed more below. An exemplary device made using this combined method is illustrated in the figure below, in which Froitzheim’s in-substrate emitter 10 is replaced with

Kwark's SIPOS/polysilicon emitter (blue), interfacial oxide (green), and a dopant diffusion region (blue) in the substrate.

Combination of Froitzheim and Kwark

Fig.1.



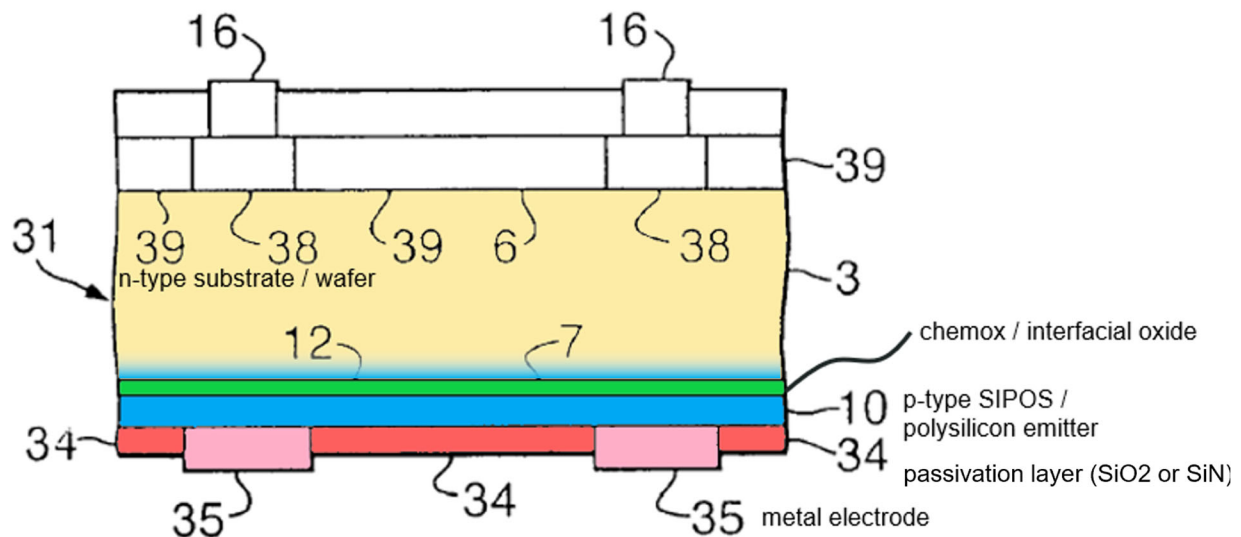
224. Though I have depicted the combination as having an n-type substrate and p-type SIPOS/polysilicon emitter for simplicity, the combination could instead have a p-type substrate and n-type SIPOS/polysilicon, as discussed in more detail below in paragraphs ¶¶236-240. The figure above is not intended to limit the dopant types of the combination to just those labelled.

225. In addition, just as for the combination between Froitzheim and Yablonovitch, I have primarily used the embodiment shown in Figure 1 of Froitzheim to explain the combined teachings of Kwerk and Froitzheim. However, a Skilled Artisan could also combine the embodiment in Figure 3 of Froitzheim,

for the same reasons discussed above in Paragraph 110. Accordingly, it should be understood that my discussions below pertain to both possible combinations, even though I mostly depict the combination with Figure 1 for simplicity.

Second Combination of Froitzheim and Kwark

Fig.3.



B. Modifying Froitzheim with SIPOS/Polysilicon and Interfacial Oxide Layer

226. Froitzheim and Kwark are analogous art because each is in the same field of endeavor—solar cell design. EX1006 (Kwark) at 742; EX1008 (Froitzheim), abstract, ¶1, 9. Thus, each reference is reasonably pertinent to the problems of solar cell efficiency. EX1008 (Froitzheim), Abstract, ¶¶1,9; Kwark, 742.

227. In my opinion, a Skilled Artisan would have looked to Kwark when designing solar cells, even though Kwark is discusses bipolar transistors, as it was

common in the art to consult references regarding bipolar transistors when researching solar cell design. Kwark expressly taught that the benefits of these SIPOS/polysilicon emitter films “translates into potential improvements of energy conversion efficiency for solar cells and enhanced high frequency performance of bipolar structures.” EX1006 at 742.

228. Furthermore, other references taught the same thing that the Skilled Artisan would look to bipolar transistors art and apply its teachings to solar cells. For example, Lindholm (EX1020) reported on “the first use of a (silicon)/(heavily doped polysilicon)/(metal)” configuration in solar cells, and compared his measurements of the effective surface recombination velocity S to “past findings for bipolar transistors.” EX1020, 363. Yablonovitch also sought to capture current gains in bipolar transistors structures observed and reported by others to heterostructure solar cells. EX1028, 597. Likewise, in a 1990 article, Gan (EX1012) reported on his studies of solar cells using polysilicon emitters “because of their important applications in high speed bipolar transistors, [which] have been widely studied.” EX1012, 245. A few years later, in 1996 Silvestre (EX1038) observed that polysilicon emitter technology “widely used in high speed bipolar transistors for VLSI circuits” was being studied for uses “in polysilicon emitter contacted solar cells.” EX1038, 497. As these examples show, it is thus expected

that a Skilled Artisan would consider articles regarding bipolar transistors when researching and designing solar cells.

229. In my opinion, by April 2009, the Skilled Artisan would have been motivated to replace the diffused emitter of Froitzheim's back junction solar cell with a SIPOS/polysilicon emitter and interfacial oxide as taught by Kwark, because as Kwark disclosed, that these film reduce recombination as measured by reduced emitter saturation current (J_{oe}), which can translate into improved solar cell efficiency. EX1006 at 745. For example, Kwark observed that:

Deliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties... The addition of a dopant species converts these films from semi-insulating to a form that can be made sufficiently conductive after annealing to make them interesting for electronic applications (2). Incorporation of these films into the emitter structure of an NPN bipolar transistor had been found to **reduce the emitter saturation current fifty fold (3); this translates into potential improvements of energy conversion efficiency for solar cells** and enhanced high frequency performance of bipolar structures. [EX1006 at 742.]

230. Kwark conducted a "set of experiments investigated the effect of varying the oxygen content [of deposited SIPOS emitters] on J_{oe} ," the emitter saturation current that is related to recombination, including comparing the results

to a control set of emitters “relatively oxygen free film, [*i.e.*,] POLY¹⁵ films doped in-situ.” EX1006, 742-43. Kwark also compared the results of the tested SIPOS/polysilicon emitters with and without an intentionally added interfacial oxide, known as a “chemox.” EX1006 at 743. Kwark’s experiments revealed that, for polysilicon emitters with an intentionally added chemox, the emitter saturation current J_{oc} was orders of magnitude lower (*i.e.*, better) than “a conventional emitter structure with a metallic contact” (designated “Al contact” with no SIPOS/polysilicon emitter, as depicted in Figure 4 below. EX1006 at 742.

¹⁵ Here, Kwark is using POLY as a shorthand for polysilicon, *i.e.*, the limiting case of SIPOS without any oxygen.

Kwark, Fig. 4

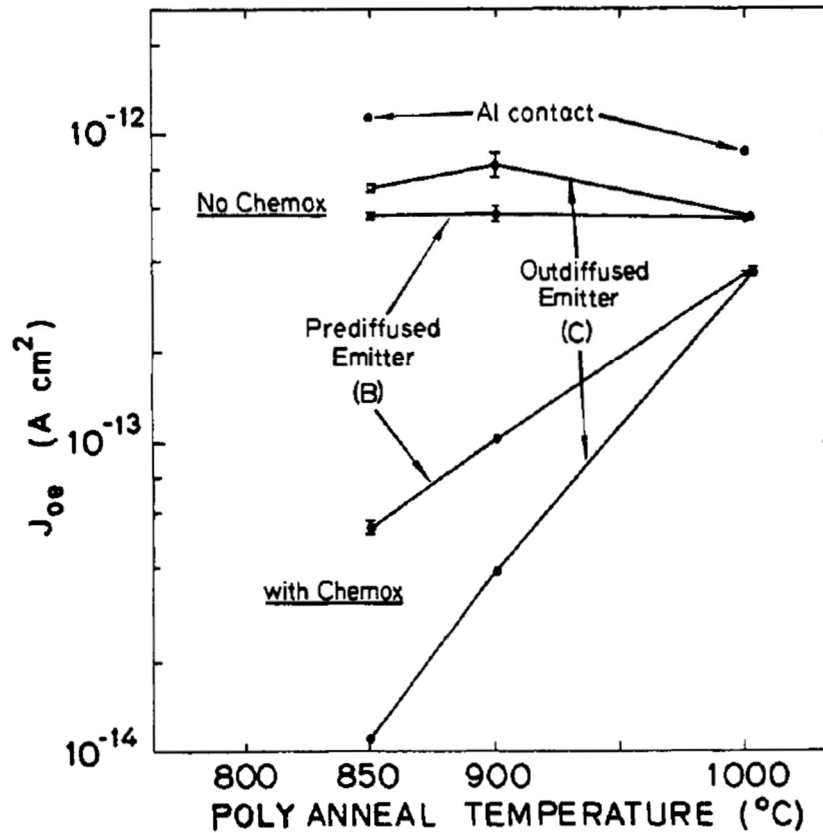


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

231. Moreover, the emitter saturation current J_{oe} was also better for SIPOS emitters with or without the intentionally added chemox, compared to the “Al contact” control, as shown in the two graphs below (for the “outdiffused emitter (C)). EX1006 at 743, Figs. 5-6.

Kwark, Figs. 5-6

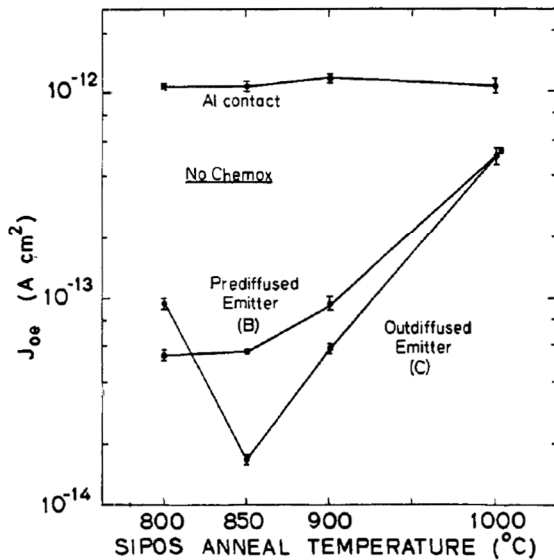


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

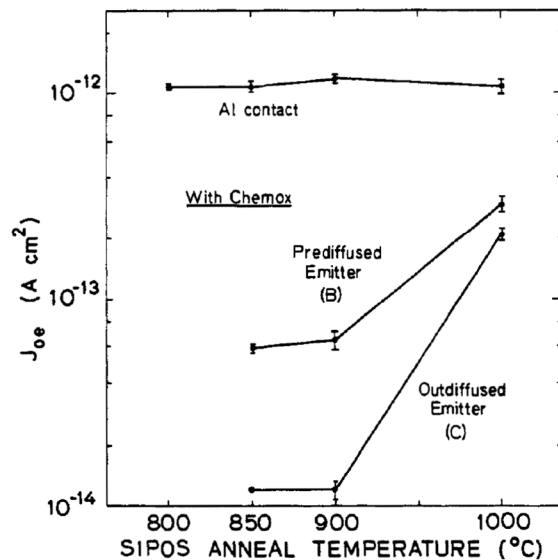


Fig. 6: emitter saturation current vs. anneal temperature for SIPOS contacts with a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

232. Accordingly, a Skilled Artisan would have been motivated to improve Froitzheim's solar cell by replacing the diffused in-substrate emitter layer with Kwark's deposited SIPOS/polysilicon emitter layer, because Kwark specifically instructed that doing so would improve the emitter saturation current. Although Kwark discloses use of n-type SIPOS and polysilicon, the Skilled Artisan would have recognized that p-type SIPOS and polysilicon would also be beneficial. As discussed in paragraph 117, Yablonovitch taught that p-type SIPOS emitter is superior to diffused-emitters, even though it has slightly higher J_o than n-type SIPOS. EX1005 at 1121. Likewise, Gan discloses that p-type polysilicon also has lower J_o than diffused emitters and low specific contact resistivity ρ_c as well.

EX1012 at 248-249 (Table 1 and Figure 6) (“The data shown in Fig. 6 are quite useful for silicon solar cells”).

233. In fact, prior to the 074 Patent, others in the art have made the proposed combination of Froitzheim and Kwark above, which further supports my opinion that a Skilled Artisan would be motivated to do so. In particular, U.S. Patent No. 8,222,516 (“Cousins”)¹⁶ explicitly disclosed a solar cell with “an N-type silicon substrate 101” and “a backside junction formed by a P-type doped polysilicon emitter 108,” separated by “a tunnel oxide layer 107.” EX1032 at 2:28-31, 2:57-58, cl. 1; *see also* cl. 9 (which allows the substrate to be p-type and the polysilicon emitter to be n-type). The p-type polysilicon emitter is formed directly on the tunnel oxide layer from a variety of different deposition techniques (i.e., rather than diffused directly into the substrate), and then annealed. EX1032 at 2:57-62. Cousins touted this solar cell configuration “relatively efficient and cost-effective,” particularly for “power plants and other applications where power generation is the main concern.” EX1032 at 1:34-42. Cousins is thus additional

¹⁶ The patent application that issued as the Cousins patent was filed February 20, 2008, about 13 months before the effective filing date of the 074 Patent in April 2009. EX1032, at face. I understand this makes Cousins prior art to the 074 Patent.

evidence that a Skilled Artisan would have been motivated to (and did) combine Kwark and Froitzheim to arrive at the proposed combination described above, in which Froitzheim's solar cell is modified to have a backside SIPOS emitter (thus forming a backside p-n junction), separated from the substrate by an interfacial oxide, according to Kwark.

C. Reasonable Expectation of Success

234. Replacing the backside diffused emitter layer of Froitzheim with a SIPOS/polysilicon emitter and interfacial oxide layer and/or chemox, as taught by Kwark, would have been well within the level of the Skilled Artisan by 2009. It would have been a simple substitution of two known elements for another to obtain predictable results. Methods for forming SIPOS layers and intentional oxide layers on substrates were well known (as demonstrated by Yablonovitch and Kwark II, for example), and Kwark further explained that an unintentional interfacial oxide is formed at the SIPOS/silicon interface as a byproduct of the annealing process. E.g., EX1005 (Yablonovitch), Table II; EX1006 (Kwark) at 743 (formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step); EX1007 (Kwark II) (explaining that chemox is formed as “the result of omitting the final HF dip after an RCA clean”). In addition, methods for forming polysilicon emitters, including on an oxide layer, were also known. E.g., EX1032 (Cousins), 2:28-31, 2:58-58.

235. Specifically, instead of introducing the dopant by diffusion at the rear side of the substrate (for example, as described in paragraphs 40-41 of Froitzheim), the Skilled Artisan would perform Kward's steps for forming a chemox on the substrate, then depositing the SIPOS/polysilicon, followed by annealing at 800-1000°C to form the crystalline SIPOS grains or to crystallize the polysilicon. EX1006 (Kward) at 743, Figs. 4-6. Moreover, the Skilled Artisan would have recognized that the steps in fabricating the solar cell could be optimized such that the front and back sides of the solar cell are doped differently without impacting the layers applied to the other side of the solar cell. This would have been within the skill of the Skilled Artisan before 2009. For example, various techniques such as masking, selective etching, or single sided etching were all available and within the routine skill of the Skilled Artisan before 2009 to be able to process and dope the front and backside of the solar cell differently. See e.g., EX1020 at 363 ("During the polysilicon deposition and the emitter diffusion, CVD-SiO₂ protected the other side of the sample"); EX1044 (US20080041526) (Abstract: "A method of single-sided etching is disclosed"); EX1045 (Arumughan) at 705 (describing an "automated inline etching system" in which "[t]he wafers are transported through an acidic etching solution in a way that only [one] side comes in contact with the chemical bath. As the wafers do not need any stacking, handling becomes much easier and the risk of wafer damage is reduced."); EX1036 at 1150 (Figure 2)

(showing different doping of front and back in a polysilicon emitter solar cell); EX1032 at Figs. 4a-4m, 3:47-5:61. See also, EX1019 at 291 (silicon nitride “serves as a masking layer for heavy phosphorus diffusion and plating, and also performs as an antireflection coating and surface passivator.”) EX1018 at 228 (“Silicon dioxide can be used as an effective barrier to selectively introduce dopants into the silicon surface”). And knowing that the interfacial oxide layer would break up during high temperature annealing, the Skilled Artisan would also have known that the formation of the side with the interfacial oxide layer and the SIPOS layer could be ordered after the dopant diffusion of the other side such that the interfacial oxide would be exposed only to a single high temperature annealing step. See e.g., EX1036 at (Figure 2) (showing a process where high temperature diffusion of one side ordered first before the formation of the tunnel oxide and polysilicon layers and subsequent annealing).

236. The Skilled Artisan in 2009 would also have a reasonable expectation of success in reversing the dopant type of Kwark’s n-type SIPOS/polysilicon and using a p-type SIPOS/polysilicon. For one thing, Yablonovitch had already expressly created and disclosed using p-type SIPOS around the time of Kwark’s publication. EX1005 (Yablonovitch) at 1211.

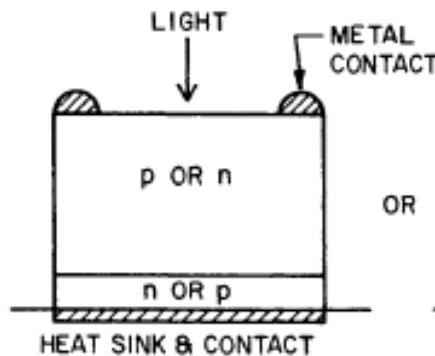
237. This would be matter of simple substitution of phosphine (PH_3) in Yablonovitch’s SIPOS deposition mixture with diborane (B_2H_6). Because

diborane consists of boron atoms (a p-type dopant) instead of phosphorus (an n-type dopant), this substitution would result in p-type SIPOS. It was well within the level of ordinary skill in 2009 to make this substitution when forming an emitter, as demonstrated by the Quirk, Luque, and Streetman textbooks. *See, e.g.*, EX1018 (Quirk) at 276 (“The polysilicon film is usually doped in situ during the deposition process by adding arsine (AsH_3), phosphine (PH_3), or diborane (B_2H_6) to the gas mixture.”); EX1019 (Luque) at 528 (“As discussed in Section 12.2.6, a-Si can be doped n-type by mixing phosphine (PH_3) with the gas mixture or doped p-type by mixing diborane (B_2H_6), BF_3 , or trimethylboron [TMB, $\text{B}(\text{CH}_3)_3$] with the gas mixture during deposition.”); EX1026 at 450 (“Alternatively, the LPCVD polysilicon film may also be in situ doped during the deposition itself by flowing in an appropriate dopant gas such as phosphine or diborane.”).

238. Moreover, it was well understood by 2009 that the polarity of a solar cell substrate and emitter could be reversed. *E.g.*, EX1011 (Yablonovitch Patent) at 2:16-19 (“The solar cell of the present invention shall be illustrated and described by a cell with p doped crystalline silicon and n-doped SIPOS. ***It is to be understood that the doping types may be interchanged.***”). In other words, it was well established that a solar cell could be formed either with an n-type substrate and a p-type emitter, or conversely with a p-type substrate and an n-type emitter.

239. That the dopant type of the substrate can be reversed is evident, for example, in the Neville textbook (EX1009), Figure VI.1, which depicts a variety of possible solar cell configurations including a back junction cell like Froitzheim, which has a substrate that is either “p or n” type and a backside emitter that is either “n or p” type. EX1009 at Fig. VI.1, 199-200; see also Paragraphs 102-103 above. The Spitzer patent also observed that for a back junction cell, the wafer (i.e., substrate) “may be formed of an n-type or p-type silicon.” EX1034 at 3:66-68. Froitzheim even alludes to this possibility of reversing the polarity of the substrate and emitter layer. EX1008, ¶7. Thus, alternatively, the Skilled Artisan would understand that Froitzheim could be reversed to have a p-type substrate and used with Kwark’s n-type SIPOS/polysilicon.

Neville, Fig. VI.1



240. Thus, the combination of Froitzheim and Kwark would simply have been the combination of prior art elements according to known methods to yield predictable results. Likewise, substituting Froitzheim’s in-substrate emitter with a

deposited SIPOS/polysilicon emitter and a chemox/interfacial oxide layer according to Kwark would be simple substitution of one known element for another to obtain predictable results. It would further constitute use of a known technique (depositing SIPOS/polysilicon emitters with a chemox or interfacial oxide layer) to improve similar devices (Froitzheim's back junction solar cell) in the same way. It would also constitute applying a known technique to a known device ready for improvement to yield predictable results.

D. Froitzheim and Kwark Disclose All Claim Limitation

1. Claim 1(a) – Preamble

241. The preamble to claim 1 recites: “*A method of fabricating a solar cell.*”

242. Froitzheim discloses methods of fabricating a solar cells. For example, Froitzheim discloses “[t]he method of manufacturing a solar cell according to [Froitzheim's] invention,” which includes the embodiments in Figures 1 and 3. EX1008, ¶¶38-50. Kwark also discloses steps that Kwark took to prepare the SIPOS/polysilicon emitter test structures for experimenting, which Kwark taught “translates into potential improvements of energy conversion efficiency for solar cells.” EX1006 at 742-43.

2. Claim 1(b) – Central Substrate

243. The first step of claim 1 recites: “*providing a wafer as a central substrate.*”

244. Both Froitzheim and Kwark satisfy this step. In Froitzheim's fabrication method, a silicon body is formed out of a wafer. EX1008, ¶38 ("A silicon body layer of n-type bulk doping, typically a wafer in <100> orientation that was sawed from a Cz grown and Phosphorous doped crystal, is provided."). Likewise, the first step of Yablonovitch's method starts by submerging silicon wafers in aqueous KOH. EX1009 at Table II, 1212. Kwark also disclosed starting with a wafer. EX1006 at 743 ("For both structures, devices were prepared with and without a chemically grown oxide (chemox) by dipping half of the wafer which underwent a full RCA clean in dilute HF.>").

245. The silicon wafers in Froitzheim and Kwark serve "*as a central substrate*" because the other layers of the solar cells are subsequently deposited or formed on the wafers. For example, EX1008 (Froitzheim), ¶41 ("a diffusion source layer... is applied, e.g. spun, only onto the back of the n- doped silicon wafer"); EX1006 (Kwark) at 743 (describing the formation of chemox and SIPOS/polysilicon emitters on the wafer).

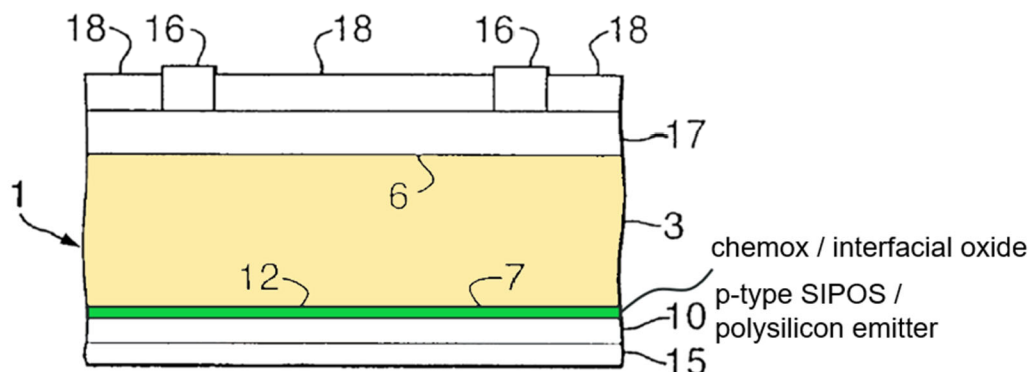
3. Claim 1(c) – Interface Passivation Layer

246. The next step of claim 1 is: "*depositing or growing at least one amorphous interface passivation layer over the substrate.*"

247. The combination of Froitzheim and Kwark, depicted below, has an SiO_x silicon oxide layer (green) that is an “*amorphous interface passivation layer*” formed on the substrate.

Combination of Kwark and Froitzheim

Fig. 1.



248. This step of the claim is found in Kwark, which discloses chemically growing an intentional “chemox” layer on a wafer “which underwent a full RCA clean.” EX1006 at 743. The RCA process grows a layer of silicon oxide on the surface of the silicon wafer. EX--- (Wolstenholme) at 225 (“For the first type (RCA treatment), the slice was given a dip in buffered HF followed by an RCA clean ... to produce a surface oxide layer of nominal thickness ~ 15Å.”)

249. Separately, Kwark also recognized that adding chemox resulted in a smaller improvement in the emitter saturation current J_{oe} for the test SIPOS emitters structures than adding the chemox did for the test polysilicon emitter structures. EX1006 at 743, Figs. 5-6. Based on this observation, Kwark postulated

that during subsequent annealing, a thin interfacial oxide layer forms between the SIPOS and the substrate, apart from any chemox layer that is intentionally formed:

That there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox would indicate that **the interface between SIPOS and monocrystalline silicon is similar in both cases. Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent with the observed similarities in J_{oe} . The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.** This would act as a more robust diffusion barrier and would limit the extent of outdiffusion of dopants from the SIPOS thus reducing bulk recombination in the monocrystalline emitter region. This is also consistent with the increased series resistance which would arise from a thicker interfacial layer. [EX1006 at 743.]

250. Either the chemox or the interfacial oxide can satisfy this element of the claim. Both the chemox and the interfacial oxide layer are comprised of silicon oxide SiO_2 . EX1006 at Fig. 3. Silicon oxide is understood to be amorphous, as I discussed for the Yablonovitch combination in Paragraph 135 above. *See, e.g.*, EX1021 (Matsumura) at abstract, 085212-1. Chemically grown oxide layer formed by RCA treatment is similarly amorphous. EX1017 (Wolstenholme) at 226 (“The interfacial oxide layer was seen as a thin bright band separating the silicon from the polysilicon. The band exhibited a random wormlike contrast in the lattice-

image micrographs, this being the characteristic behavior for an amorphous material.”).

251. Alternatively, Kwark also satisfies this step with the deposition of SIPOS emitter without a separate step of growing the chemox, as discussed in more detail with respect to Claim 3 below. Specifically, even without the separate step of growing the chemox, the oxygen in the deposited SIPOS film would segregate upon heating and react with the silicon wafer to form an interfacial oxide layer, which is an “amorphous interface passivating layer.” EX1006 at 743 (“the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintenance of this interfacial [oxide] layer”); EX1007 (Kwark II) at 1125 (“Such an oxide could form, for example during the anneal as oxygen segregates from the SIPOS.”).

252. Silicon oxide formed on silicon is also understood to be passivating, as I discussed for the Yablonovitch combination in Paragraph 134 above. *See, e.g.*, EX1018 (Quirk) at 227. The 074 Patent itself also lists silicon oxide as an example of a passivating interface layer. EX1001 at 5:56-61, 5:66-6:4.

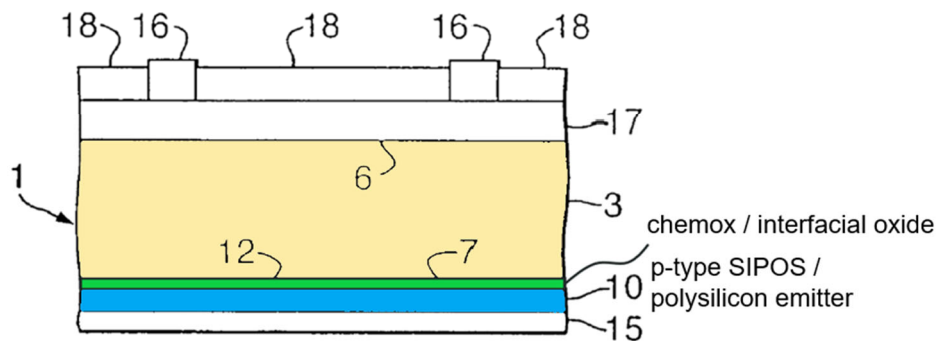
4. Claim 1(d) – Conductive and Passivating Layer

253. The next step of claim 1 is: “*depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant.*”

254. The combination of Froitzheim and Kwark, depicted below, has an p- or n-type SIPOS/polysilicon layer (blue) that is a “*conductive and passivating layer*” formed on the green chemox/interfacial oxide layer (*interface passivation layer*).

Combination of Kwark and Froitzheim

Fig. 1.



255. This step of the claim is found in Kwark. In particular, Kwark discloses depositing polysilicon over a chemox layer onto the substrate:

In order to establish unambiguous results for a relatively oxygen free film, POLY films doped insitu in an RF heated cold wall APCVD reactor using a hydrogen carrier were used in the next set of emitter contacts; these films did not etch in BHF. [EX1006 at 743]

As Kwark notes, the polysilicon film is “doped insitu,” meaning that either p- or n-type dopants were injected into the polysilicon while being formed on the test structures. EX1006 at 743. Kwark’s polysilicon film thus “*comprises a dopant*” per the claim.

256. In addition, Kwark discloses depositing a SIPOS emitter that is over the chemox or interfacial oxide, or forming the SIPOS emitter without an intentionally added chemox. EX1006 at 743. The SIPOS layer also meets this claim element. Kwark’s SIPOS emitters are also doped, likely with n-type dopants. *See* EX1006 at 742 (discussing “the addition of a dopant species” to SIPOS, “N-type SIPOS emitter contacts,” and “activat[ing] the dopant” in SIPOS via annealing). Kwark’s SIPOS film thus “*comprises a dopant*” per the claim.

257. The Skilled Artisan would have understood that doped SIPOS/polysilicon films are both conducting and passivating. For example, Kwark discloses that the SIPOS/polysilicon films are conducting. EX1006 at 742 (“The addition of a dopant species converts these films from semi-insulating to a form that can be made sufficiently conductive after annealing ...”). Kwark II discloses that “these films, pioneered at Sony, found initial application in their intrinsic form to the passivation of high voltage devices.” EX1007 at 1121. *See also*, EX1015 (Pan) at 589 (SIPOS “has been used in a variety of electronic devices ... as excellent surface passivation films in semiconductor devices”); EX1014 (Compagnini) at 885 (“[s]emi-insulating polycrystalline silicon (SIPOS) is widely used as a passivation layer.”); EX1020 (Lindholm) at 363 (“Highly conducting polysilicon contacts to crystalline silicon are widely used in bipolar integrated

circuits. Among other properties, these heterojunctions reduce recombination current by forming quasi-blocking contacts.”).

258. Finally, doped polysilicon and SIPOS like the emitters tested by Kwark are identified as examples of “*conductive and passivating*” materials. In particular, the 074 Patent specification identifies exemplary materials for fabricating an “electrically passivating and conductive film” of either p- or n-types. EX1001 at 5:49-55, 6:5-17. Some of the recited examples include “amorphous or polycrystalline silicon carbides,” “amorphous or **polycrystalline silicon**,” and “amorphous or poly-crystalline diamond-like-carbon.” EX1001 at 5:49-55, 6:5-15. The 074 Patent further notes that “[a]ny of the above listed examples may include oxygen,” which would apply to SIPOS. EX1001 at 5:54-55, 6:16-17. As Yablonovitch, Kwark, and others recognized, SIPOS is a combination of polycrystalline silicon and oxygen. *See, e.g.*, EX1005 (Yablonovitch) (“SIPOS (originally named semi-insulating polycrystalline silicon). In its annealed form it is a poorly understood mixture of microcrystalline silicon and silicon dioxide (SiO_x).”); EX1007 (Kwark II) at 1121 (SIPOS “has become the generic acronym for deposited silicon films doped with oxygen”); EX1035 (Matsushita) at abstract (“SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.”).

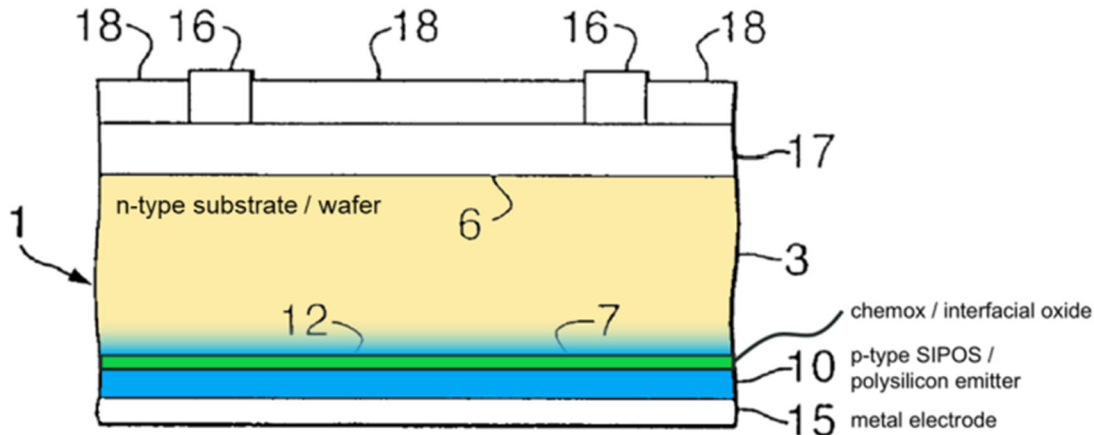
5. Claim 1(e) – Thermal Treatment

259. The next step of claim 1 is: “*providing thermal treatment at a temperature of about 500°C or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer.*”

260. In the combination of Froitzheim and Kwark, depicted below, the annealing step (*thermal treatment*) of Kwark crystallizes the blue SIPOS/polysilicon emitter (*conductive and passivating layer*) and facilitates diffusion of dopants through the green chemox/interfacial oxide layer (*interface passivation layer*).

Combination of Kwark and Froitzheim

Fig.1.



261. This step of the claim is found in Kwark. In particular, for both the polysilicon and the SIPOS emitters, Kwark discloses annealing (*thermal treatment*) the polysilicon/SIPOS test subjects at temperatures from 800-1000°C (*at a temperature of about 500°C or higher*). EX1006 at, e.g., Figs. 4-6 (graphing J_{oe} as a function of anneal temperatures), 743 (analyzing J_{oe} data for polysilicon emitters annealed above 900°C, and SIPOS emitters above 850°C).

262. Kwark's annealing step "*crystalliz[es], at least in part, the at least one conductive and passivating layer.*" For Kwark's polysilicon emitters, annealing at 800°C or above would crystallize the polysilicon. This is described, for example, in Quirk:

Annealing heats the implanted silicon substrate to repair crystalline damage and electrically activate dopants by moving the atoms into crystal lattice sites (see Figure

17.27 on page 500). **Crystal damage repair is done at about 500°C** and dopant activation occurs at about 950°C. [EX1018 at 499-501.]

See also EX1030-Streetman, 159-61 (explaining that annealing at temperatures up to 1000°C can be used to repair silicon lattice damage, i.e., to re-crystallize the silicon).

263. Likewise, Kwark's annealing step crystallizes the SIPOS emitters. SIPOS is amorphous when it is first deposited. E.g., EX1007 (Kwark II) at 1121 ("As-deposited, SIPOS is usually amorphous."); EX1013 (Fussel) at abstract ("As-deposited [SIPOS] layers are predominantly amorphous...."); EX1025 (Kwark III) ("SIPOS films prepared at 650°C are amorphous;"). Annealing the SIPOS at temperatures of 800-1000°C then causes the as-deposited SIPOS to crystallize into small grains of polycrystalline embedded in silicon oxide SiO₂. This is illustrated, for example, in FIG. 3 of Kwark, which shows that annealing results in "XTAL Si," i.e., "crystallization of the silicon crystallites." EX1006 (Kwark), Fig. 3.

Kwark II further explains the crystallization process for SIPOS film:

During annealing it has been found that the film morphology changes. Si precipitates into small grains of crystalline Si and the oxygen segregates as SiO₂ on the grain boundaries. [EX1007 at 1121.]

Kwark I, Fig. 3

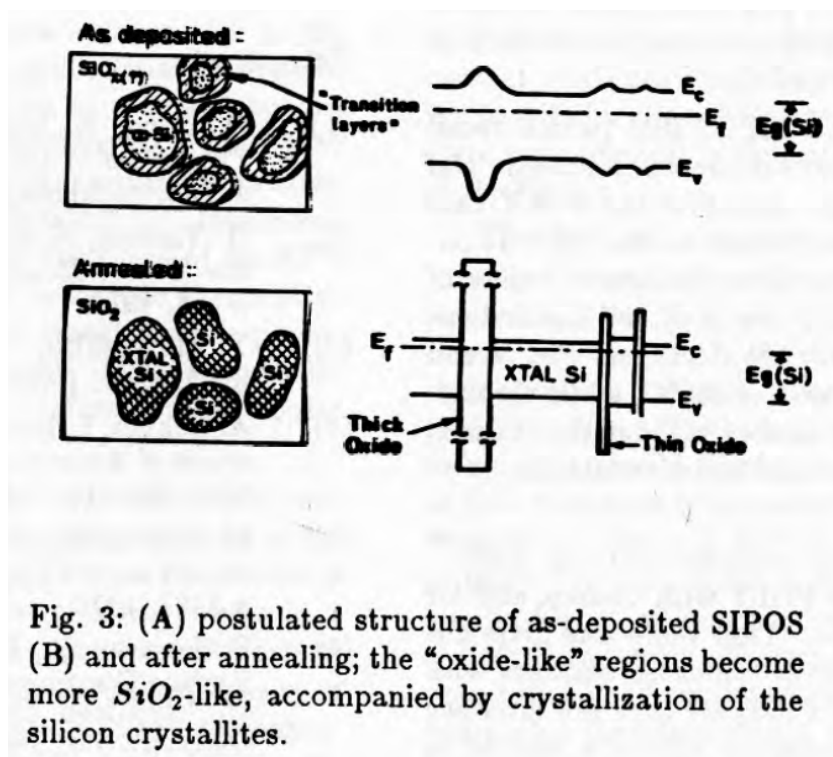


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

264. Kwark’s annealing process also “*facilitat[es] diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer.*” In particular, one of the polysilicon test structures Kwark analyzed with a chemox was “emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction.” EX1006 at 743. As Kwark explains, as the test polysilicon emitters were annealed at higher temperatures, “a component of J_{oe} due to outdiffusion from the heavily doped POLY which becomes increasingly significant for annealing temperatures above 900°C .” EX1006 at 743. An outdiffused emitter C was also prepared using SIPOS to form the emitter. EX1006 at Figs. 5-6 (depicting data for “Outdiffused Emitter

(C)” for SIPOS contacts). In the Kwark II paper published a few years later, Kwark provided additional clarity regarding the polysilicon/SIPOS outdiffused emitter C:

In addition, emitters of type C with no prediffusion were fabricated. These relied solely on outdiffusion from the *in-situ* doped SIPOS or poly-silicon to provide sufficient surface doping concentration. [EX1007 at 1123.]

“Outdiffusion” as used by Kwark here refers to the diffusion of the dopants from the polysilicon and SIPOS layers into the substrate. In fact, this was a common and known way to form emitters in the field. *See, e.g.*, EX1016 (Post) at 1718, Fig. 1. (“The second type of structure (Fig. 1(b)) is a polysilicon emitter in which the n⁺ dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitter/base junction.”). This outdiffusion increases with increasing annealing temperature. EX1006, 743.

265. In order for the dopants to diffuse from Kwark’s SIPOS/polysilicon emitters into the substrate to form the emitter/base (pn) junction, the dopants must pass through the chemox / interfacial oxide, because the chemox/interfacial oxide is between the emitter and the substrate. For example, Kwark noted: “That there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox would indicate that **the interface between SIPOS and monocrystalline silicon** is similar in both cases,” i.e., they both have an interfacial oxide layer. EX1006 at 743. This phenomenon of outdiffusion was also shown by

Fig. 1(b) of Post, which depicted the formation of a shallow n^+ diffusion region formed by outdiffusing dopants from the n^+ polysilicon emitter through an interfacial oxide region. EX1016 (Post) at 1718, Fig. 1.

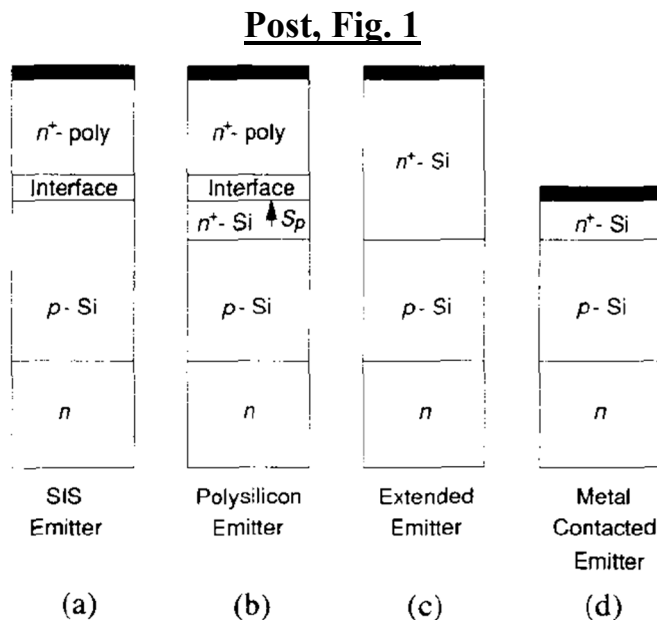


Fig. 1. Schematic diagrams of (a) an SIS emitter, (b) a polysilicon emitter, (c) an extended emitter, and (d) a metal contacted emitter.

266. Kwark's annealing step would also cause diffusion of boron through the interfacial oxide into the wafer when using a p-type SIPOS/polysilicon. See, e.g., EX1036 (Borden) at Fig. 4 (depicting the diffusion of boron dopants from p-type polysilicon through a tunnel oxide into an n-type substrate); EX1039 (Shimakura) §3.3, Fig. 8 ("Figure 8 shows the P-N junction depths formed in single crystalline Si by boron penetration through the SiO₂ films from doped polycrystalline Si. This figure shows that the diffusion of boron in SiO₂ films is strongly dependent on the drive-in ambients."). As I explained in paragraph 152,

boron has a greater diffusivity than phosphorus in SiO₂ films such that the Skilled Artisan would expect that boron would readily diffuse into the thin interfacial oxide layer of Kwark. *Id.* at Abstract (“It was found that the diffusion coefficient of boron in SiO₂ is about two orders of magnitude larger than that of phosphorus.”); EX1031 (Fair) at 712, Fig. 9 (diffusivity of boron greatly increases through SiO₂ for oxide thickness below 8 nanometers); EX1007 (Kwark II) at 1125 (“The similarity of results for the chemox poly-silicon contacts and SIPOS contacts suggests that these both obtain their improved performance through incorporating a thin, tunnelable interfacial oxide”).

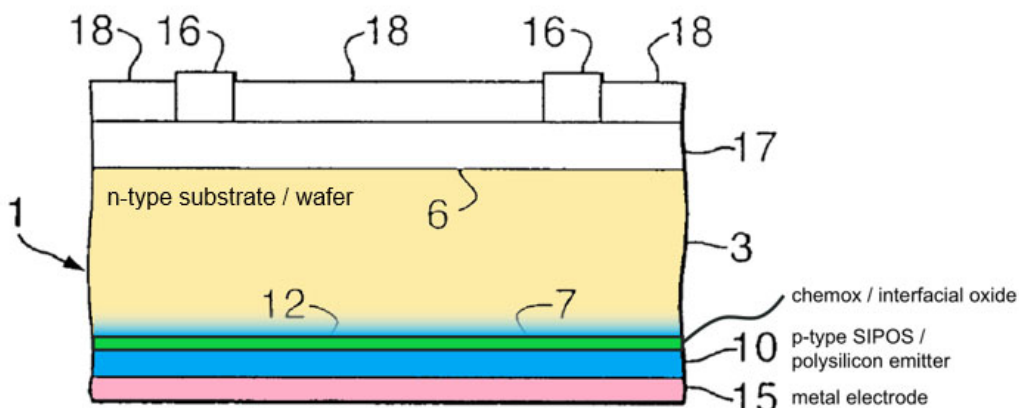
6. Claim 1(f) – Metallization

267. The next step of claim 1 is: “*providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

268. The combination of Froitzheim and Kwark, depicted below, has an electrode formed from metallization (pink) that “*directly contact[s] the at least one conductive and passivating layer,*” i.e., the blue SIPOS/polysilicon emitter layer.

Combination of Kwark and Froitzheim

Fig.1.



269. This step of the claim is found in Froitzheim, for the same reason as I discussed in paragraph 155. In particular, after Kwark’s step of annealing the SIPOS layer (which supplanted Froitzheim’s step of forming the in-substrate diffused emitter), Froitzheim discloses “*providing metallization as electrodes*” as shown in the “rear side contact 15” in Figure 1:

A rear side contact 15 is arranged in electrical connection with the p-doped layer 10. The rear side contact is shown covering a large part or substantially all of the rear side of the cell. [EX1008, ¶27.]

The Skilled Artisan would understand that the rear side contact is made of metal and acts as an electrode. Froitzheim explains that the front and rear side contacts function to “withdraw a photocurrent” or charge carriers, confirming their role as electrodes. EX1008, ¶¶2, 18, and 32. Further, in describing the rear contact of the

second embodiment in Figure 3 (in which the rear side contact 35 only covers the rear partially), Froitzheim states that “less material such as Ag [silver] or Al [aluminum] is required for the contacts,” which indicates that the full backside contact 15 is also made of either metal. *Id.*, ¶¶20, 33.

270. In general, a Skilled Artisan would know that electrodes could be made using aluminum, among other metals. Aluminum and silver, e.g., were both well known materials for making contacts, with tradeoffs for better efficiency (silver) versus lower costs (aluminum). *See, e.g.*, EX1032 (Cousins) at 5:52-55 (“The metal contact 110 may comprise silver... Other metals may also be used as a metal contact 110, such as aluminum, for example.”); EX1010 (Sasaki) at 3390, Fig. 2 (comparing solar cells with silver and aluminum contacts).

271. In addition, the electrode directly contacts the SIPOS or polysilicon emitter in the Froitzheim/Kwark combination (i.e., “*directly contact[ing] the at least one conductive and passivating layer*”). EX1008 (Froitzheim), ¶27 (“A rear side contact 15 is arranged **in electrical connection** with the p-doped layer 10.”).

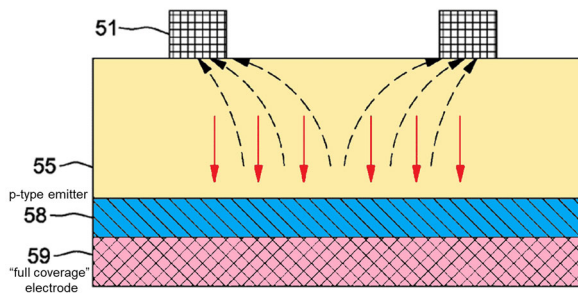
272. As discussed in paragraphs 264-266, the annealing step in Kwark also diffuses the dopant through the interfacial oxide layer and thus, also satisfies the limitation of: “*the dopant diffused through the at least one interface passivation layer.*” EX1006 (Kwark) at 743 (“emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction.... [O]utdiffusion from

the heavily doped POLY [] becomes increasingly significant for annealing temperatures above 900°C”).

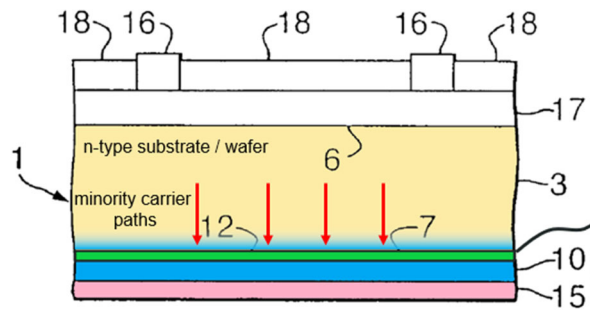
273. As discussed below, the Froitzheim/Kwark combination also satisfies the limitation: “*provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

274. **Combination Using Figure 1 of Froitzheim:** The combination of Kwark and Froitzheim Figure 1 meets the above “*shortened charge carrier flow paths*” limitation to the same extent that (and in the same manner as) the embodiment of Figure 5 of the 074 Patent satisfies this limitation, for the same reasons as I discussed above in my analysis of this claim element for the Yablonovitch and Froitzheim grounds in Paragraphs 160-164. Thus, to the extent Figure 5 (or Figure 3) of the 074 Patent satisfies this limitation of claim 1, the combination of Kwark and Figure 1 of Froitzheim would do so as well.

074 Patent, Figure 5



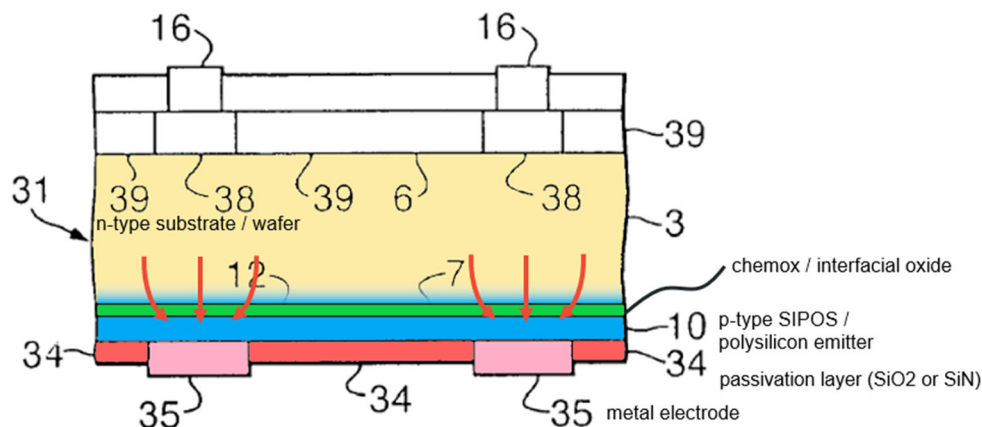
Kwark and Froitzheim, Fig. 1



275. **Combination Using Figure 3 of Froitzheim:** The combination of Kwark and Froitzheim Figure 3 meets the above “*shortened charge carrier flow paths*” limitation to the same extent that (and in the same manner as) the Patent Owner contends that Petitioner’s product satisfies this limitation in the district court complaint, for the same reasons as I discussed above in my analysis of this claim element for the Yablonovitch and Froitzheim grounds in Paragraphs 165-170. Thus, if Patent Owner’s allegations in the district court complaint (EX1024) at ¶¶79-81 are accepted, the combination of Kwark and Figure 3 of Froitzheim would meet the “*shortened charge carrier flow paths*” limitation as well, as shown by the red arrows in the figure below.

Combination of Kwark and Froitzheim Fig. 3¹⁷

Fig.3.



7. Claim 2 – Antireflective Layer

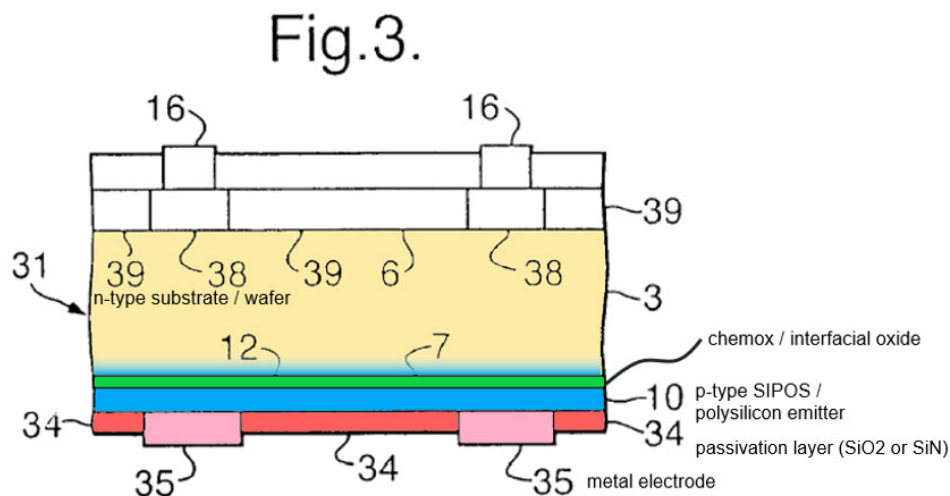
276. Claim 2 depends from claim 1 and adds the additional step: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

277. As I explained more fully in my analysis of the combination of Yablonovitch and Froitzheim in Paragraphs 172-**Error! Reference source not found.** above, in its district court complaint Patent Owner contends that a silicon nitride SiN_x layer through which the electrode makes contact with the substrate via

¹⁷ According to Patent Owner’s allegations in the district court complaint (EX1024) at ¶¶79-81.

holes meets the limitation in claim 2. According to Patent Owner's theory, the combination of Yablonovitch and Figure 3 of Froitzheim, depicted below, has a red passivation layer made of silicon nitride (SiN) or silicon oxide (SiO₂) that is an *"antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell."*

Combination of Kwark and Froitzheim Fig. 3¹⁸



278. This step of the claim is found in Froitzheim. Specifically, the red silicon nitride or silicon oxide passivation layer 34 is an *"antireflective layer"* as claimed for the same reasons as I discussed in my analysis of claim 2 for the Yablonovitch and Froitzheim grounds in Paragraphs 175-177 above.

¹⁸ According to Patent Owner's allegations in the district court complaint (EX1024) at ¶82.

8. Claim 3 – Separation

279. Claim 3 depends from claim 1 and adds the additional step: “*wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate and the providing thermal treatment of about 500° C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.*”

280. This step of the claim is found in Kwark. In particular, as discussed more fully in my analysis of claim elements 1(c) and 1(d) in Paragraphs 246-252 above, Kwark discloses depositing a SIPOS emitter (*conductive and passivating layer*), with or without an intentionally formed chemox layer. EX1006 at 743, Figs. 5-6.

281. Kwark’s annealing step separates the as-deposited SIPOS into an interfacial oxide and crystallized SIPOS, in accordance with claim 3. Kwark discloses that “the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintenance of this interfacial [oxide] layer,” which formation is “a result of the anneal process (Fig. 3).” EX1006 at 743. In Kwark II, Kwark further commented on this process for forming the interfacial oxide: “Such an oxide could form, for example, during the anneal **as oxygen**

segregates from the SIPOS.” EX1007 at 1125. In other words, the annealing step in Kwark at 800-1000°C causes an interfacial oxide to separate out from the as-deposited SIPOS layer to form such oxide layer at the interface with the silicon. The Skilled Artisan would be motivated to alternatively use this segregation method for the SIPOS to form the interfacial oxide layer to advantageously reduce series resistance by reducing the thickness of the oxide layer and to simplify the fabricating process by omitting an extra step. EX1006 at 743 (“This is also consistent with the increased series resistance which would arise from a thicker interfacial layer.”)

282. As Kwark explains, comparing the measured emitter saturation current J_{oe} for the SIPOS emitters with and without the intentional chemox layer, Kwark observed that “there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox [which] would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases.” EX1006 at 743. Kwark further explains that with the extra step of intentionally forming the chemox with the deposition of SIPOS film, the chemox adds additional thickness, but only slightly decreases the J_o compared to SIPOS film formed without the intentionally added chemox:

That there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases.

Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent with the observed similarities in J_{oe} . The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that **the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.** [EX1006 at 743.]

And although the J_o is slighter higher for SIPOS without the intentionally added chemox, this segregation method for the SIPOS/interfacial layer still performs substantially better than the conventional diffused emitter “Al contact” control. *Id.*, 745 (Figure 5).

283. In addition, SIPOS is a “*silicon-containing compound*”. SIPOS is a mixture of silicon and oxygen—or more precisely, grains of crystalline silicon embedded in silicon oxide SiO_2 . EX1006 (Kwark) at 742 (“Deliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties.”); EX1007 (Kwark II) (“SIPOS, for Semi-Insulating Polycrystalline Silicon, has become the generic acronym for deposited silicon films doped with oxygen.”).

284. Further, the SIPOS in Kwark is amorphous when it is first deposited. E.g., EX1007 (Kwark II) at 1121 (“As-deposited, SIPOS is usually amorphous.”);

EX1013 (Fussel) at abstract (“As-deposited [SIPOS] layers are predominantly amorphous....”); EX1025 (Kwark III) (“SIPOS films prepared at 650°C are amorphous;”). Kwark’s annealing step subsequently crystallizes the SIPOS emitters, i.e., causes the SIPOS to crystallize into small grains of polycrystalline embedded in silicon oxide SiO₂. This is illustrated, for example, in FIG. 3 of Kwark reproduced below, which shows that annealing results in “XTAL Si,” i.e., “crystallization of the silicon crystallites.” EX1006 (Kwark), Fig. 3. Kwark II further explains the crystallization process for SIPOS film:

During annealing it has been found that the film morphology changes. Si precipitates into small grains of crystalline Si and the oxygen segregates as SiO₂ on the grain boundaries. [EX1007 at 1121.]

Kwark, Fig. 3

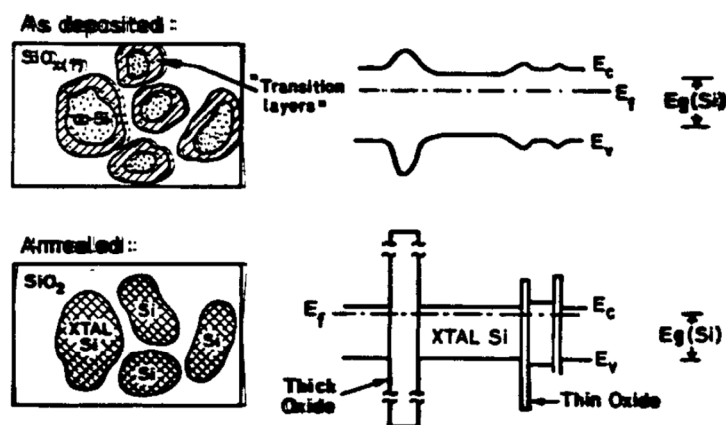


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO₂-like, accompanied by crystallization of the silicon crystallites.

285. In summary, Kwark's 800-1000°C annealing step (*thermal treatment of about 500° C. or higher*) causes amorphous as-deposited SIPOS (*amorphous silicon-containing compound*) to separate into an interfacial oxide (*interface passivation layer*) and crystallized SIPOS (*conductive and passivating layer*), and thus has all of the elements of the second part of claim 3.

9. Claim 4 – Perforation

286. Claim 4 depends on claim 1 and adds the additional step: “*wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.*”

287. This step of the claim is found in Kwark. As I discussed above in Paragraphs 259-266, Kwark discloses depositing SIPOS or polysilicon and thermally treating the SIPOS/polysilicon at temperatures between 800 and 1000°C. Kwark's annealing step results in the breakdown of the interfacial oxide and chemox layers, causing perforations to form.

288. In particular, Kwark measured the recombination current J_{oe} of the studied SIPOS/polysilicon emitter structures as a function of annealing temperature from 800-1000°C, with and without intentionally added chemox layers. EX1005, 743, Figs. 4-6. At Kwark's higher annealing temperatures, the oxide and chemox layer start to break up. This fact was explored in greater detail in Kwark II, in which Kwark concluded that for the SIPOS cells without a chemox layer “ J_{oe} again

increases with higher anneal temperatures,” and concluded that “the increase could be due to the break-up of an interfacial oxide,” which “form[s], for example, during the anneal as oxygen segregates from the SIPOS.” EX1007 (Kwark II) at 1124-25.

289. Likewise, for SIPOS emitters with the chemox layer added, Kwark’s data at higher anneal temperatures again “suggest[] the break-up of the interfacial oxide and an increase in surface doping concentration.” EX1007 (Kwark II) at 1125. However, for the SIPOS cells with a chemox layer, the constant J_{oe} between 850 and 900°C indicated that “the chemox is acting as a barrier to the out-diffusion of phosphorus, and thus prevents lifetime reduction in the surface region, or alternatively, **is more resistant to break-up during annealing than whatever oxide exists without the chemox.**” Kwark II at 1125 (emphases added). In other words, according to Kwark II’s findings, the chemox and interfacial oxide in Kwark act as barriers to the diffusion of dopants (e.g., phosphorus) into the substrate, but begin to break apart during higher annealing temperatures around 900-1000°C.

290. Kwark II’s observations are confirmed by others for polysilicon emitters. For example, Wosltenholme (EX1017) investigated “the electrical characteristics of polycrystalline silicon emitter bipolar transistors,” including devices “fabricated with and without a deliberately grown interfacial oxide layer.”

EX1017 at abstract. Wolstenholme's measurements revealed that the deliberately-grown interfacial oxide "breaks up when annealed at ~950°C and above," EX1017 at abstract. Like Kwark, Wolstenholme also observed that "electron microscopy also shows that a thin interfacial oxide layer is present even when not deliberately grown," and that "[t]his oxide breaks up when annealed at ~900°C and above." EX1017 at abstract. According to Wolstenholme, the breakup of the oxide layers resulted in "holes", i.e., perforations, opening in the oxide. E.g., EX1017 at 226 ("Some regions had increased in thickness to a maximum of 19 Å, some regions were thinner, and in some regions holes (B) were present in the layer"), 227 ("For the specimens given an RCA treatment, a 1000 °C preanneal and full processing (micrograph not included), the breakup of the interfacial oxide layer was more pronounced. Some regions had increased in thickness to a maximum of 22 Å, and more holes were present in the layer.").

291. The breakdown of the interfacial oxide results in greater dopant outdiffusion from the polysilicon/SIPOS emitter into the substrate. As Kwark explained, the interfacial oxide/chemox "act as a more robust diffusion barrier and would limit the extent of outdiffusion of dopants from the SIPOS thus reducing bulk recombination in the monocrystalline emitter region." EX1006 at 743. Thus, at higher anneal temperatures around 900-1000°C, as the interfacial oxide/chemox break down, greater concentrations of dopants are able to diffuse through the oxide

via the perforations. Because the effective area and dopant concentration of the dopant diffusion is greater, there is more recombination in the diffusion region, and J_{oe} increases. This is evidenced, for example, by Kwark's observation that "[a]t 1000°C, th[e] outdiffusion is severe enough to dominate the J_{oe} ," because at that temperature, there would be substantial breakdown of the interfacial oxide.

EX1006 at 743; see also EX1007 (Kwark II) at 1125 ("This suggests that either the chemox is acting as a barrier to the out-diffusion of phosphorus, and thus prevents lifetime reduction in the surface region, or alternatively, is more resistant to break-up during annealing than whatever oxide exists without the chemox.").

292. The Skilled Artisan would also have understood that the holes in the oxide as a result of high temperature breakdown also enable charge carriers to pass through the oxide in the form of current. In fact, Yablonovitch describes this phenomenon:

We believe the majority-carrier electrical contact is by individual microcrystalline grains which occasionally protrude into the oxide as shown in Fig. 3, i.e., electrical contact is via thin spots and pinholes in the SiO_2 .
[EX1005 at 1213.]

These contact spots "provide more than enough conductivity for majority-carrier electrons." EX1005 at 1213. Post likewise discloses that modeling the "discontinuous interfacial layer" shows that "the base current flows primarily

through those areas of the interface that are free from oxide,” i.e., regions with perforations. EX1016 at Abstract.

10. Claim 5 – Crystallization

293. Claim 5 depends from claim 1 and adds the additional step: “*wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.*”

294. This step of the claim is found in Kwark. As discussed more fully in my analysis of claim elements 1(c) and 1(d) in Paragraphs 246-252 above, Kwark discloses depositing a SIPOS/polysilicon emitter (*conductive and passivating layer*).

295. SIPOS and polysilicon are both “*silicon-containing compounds*”. SIPOS is a mixture of silicon and oxygen—or more precisely, grains of crystalline silicon embedded in silicon oxide SiO₂. EX1006 (Kwark) at 742 (“Deliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties.”); EX1007 (Kwark II) (“SIPOS, for Semi-Insulating Polycrystalline Silicon, has become the generic acronym for deposited silicon films doped with oxygen.”). Polysilicon *is* silicon; polysilicon is a shorthand for

polycrystalline silicon, which is silicon with a particular crystalline structure. *See, e.g.,* EX1019 (Luque) at 24 (“polysilicon (it is called polysilicon because it has many grains of crystalline Si, typically of about 1 mm)”).

296. Moreover, *as deposited*, both Kwark’s SIPOS and polysilicon emitters are amorphous, and become crystallized as a result of the annealing. *E.g.,* EX1007 (Kwark II) at 1121 (“As-deposited, SIPOS is usually amorphous.”); EX1013 (Fussel) at abstract (“As-deposited [SIPOS] layers are predominantly amorphous....”); EX1025 (Kwark III) (“SIPOS films prepared at 650°C are amorphous;”).

297. In fact, the point of annealing the SIPOS/polysilicon emitters at 800-1000°C is to crystallize the silicon. For example, Kwark discloses that the annealing step subsequently crystallizes the SIPOS emitters, i.e., causes the SIPOS to crystallize into small grains of polycrystalline embedded in silicon oxide SiO₂. This is illustrated, for example, in FIG. 3 of Kwark reproduced below, which shows that annealing results in “XTAL Si,” i.e., “crystallization of the silicon crystallites.” EX1006 (Kwark), Fig. 3. Kwark II further explains the crystallization process for SIPOS film:

During annealing it has been found that the film morphology changes. Si precipitates into small grains of crystalline Si and the oxygen segregates as SiO₂ on the grain boundaries. [EX1007 at 1121.]

Kwark, Fig. 3

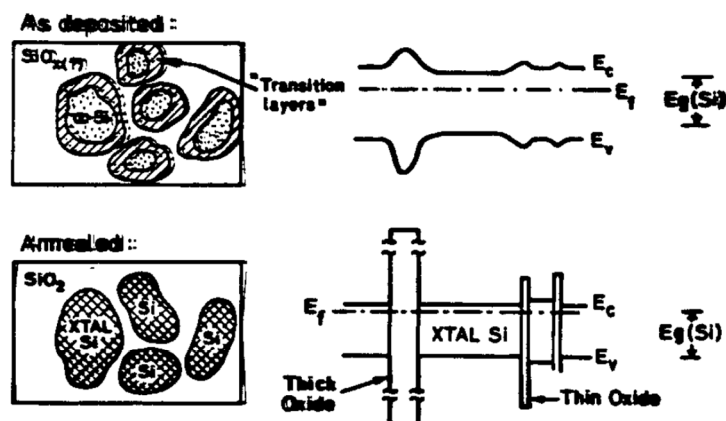


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Annealing is also a common technique used to crystallize amorphous silicon into polycrystalline silicon. EX1018 (Quirk) at 499-501 ("Annealing heats the implanted silicon substrate to repair crystalline damage and electrically activate dopants by moving the atoms into crystal lattice sites.... Crystal damage repair is done at about 500°C"); EX1026 (Streetman), 160-61 ("However, most of this damage can be removed in Si by heating the crystal after the implantation. This process is called *annealing*.").

298. Lastly, the annealing crystallizes the SIPOS and polysilicon emitters into a "*polycrystalline film*". Tautologically, the polysilicon emitter in Kwark is *polycrystalline* silicon once it is annealed. In addition, SIPOS once crystallized forms polycrystalline grains embedded in silicon oxide. As Kwark explained,

“[d]eliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS.” EX1006 at 742. Others in the art also characterized SIPOS as polycrystalline. *E.g.*, EX1035 (Matsushita) at abstract (“SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.”).

11. Claim 6 – Transmissivity

299. Claim 6 depends from claim 1 and adds the additional step: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and [b] increases the optical transmissivity.*”

300. Part [a] of claim 6 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer.*” I discussed how the combination of Froitzheim and Yablonovitch satisfies this limitation in Paragraphs 260-266 above.

301. As for part [b], in the combination of Froitzheim and Kwark, Kwark’s annealing step (*thermal treatment*) further “*increases the optical transmissivity*” of the SIPOS layer (*conductive and passivating layer*). In particular, Kwark disclosed

depositing the SIPOS layer and then annealing the SIPOS layer between 800-1000°C. EX1006 at Figs. 5-6. Kwark further explains that the SIPOS emitters described in Figs. 5 and 6 are “ $\gamma=0$ SIPOS” layers, which have “several atomic %[] amounts of oxygen. Kwark at 742-43.

302. SIPOS annealed at 800°-1000°C with several percent oxygen is more transmissive than SIPOS as-deposited. For example, Pan et al. investigated the “optical absorption characteristics of SIPOS.” EX1015 (“Pan”), §1. In the study Pan prepared “SIPOS films deposited at 650°C,” and observed that “[a]nnealing at different temperatures has modified the optical absorption of the films.” *Id.* §§2.1, 3. The relationship between annealing temperature and optical absorption for SIPOS films with 8% oxygen content is graphed in Figure 4 of Pan, reproduced with annotations below. *Id.* §3, Fig. 4. As shown, the optical absorption was greater for the as-deposited SIPOS films than for films annealed at 900°C.

Pan, Fig. 4

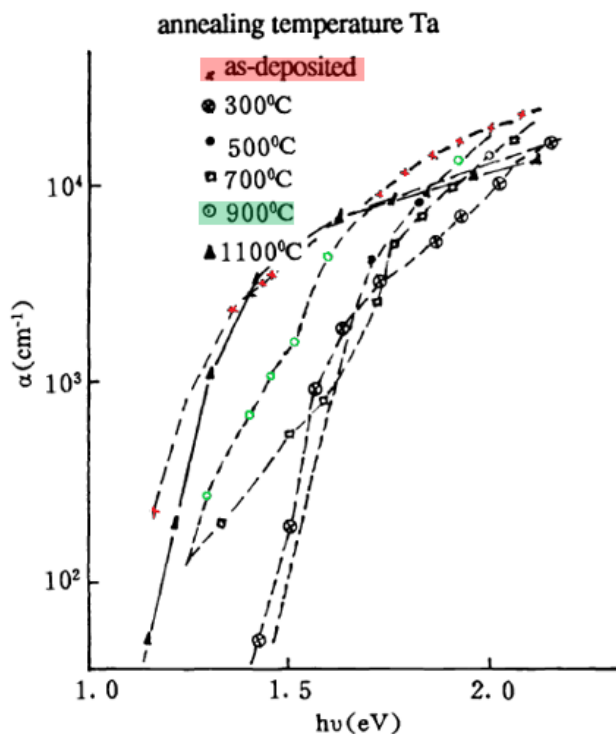


Fig. 4 Changes in optical absorption of SIPOS films (8 at.%) with annealing temperature T_a .

303. Optical absorption is the inverse of transmissivity. That is, the more light that is absorbed by a SIPOS layer, the less light that can be transmitted through the layer. Accordingly, Pan shows that SIPOS crystallized between 800-1000°C (for example, at 900°C) has greater optical transmissivity than amorphous SIPOS as-deposited. Similar results have been obtained by others. For example, Compagnini discloses that the optical transmission increases when SIPOS films were annealed, and the transmittance increases with increasing anneal temperature. EX1014 at 886 (Figure 1) and at 890 (Figure 8).

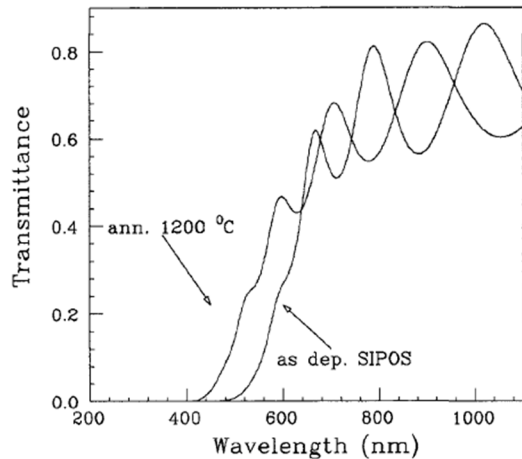


FIG. 1. Transmission curves in the fundamental absorption region for as-deposited and 1200 °C samples.

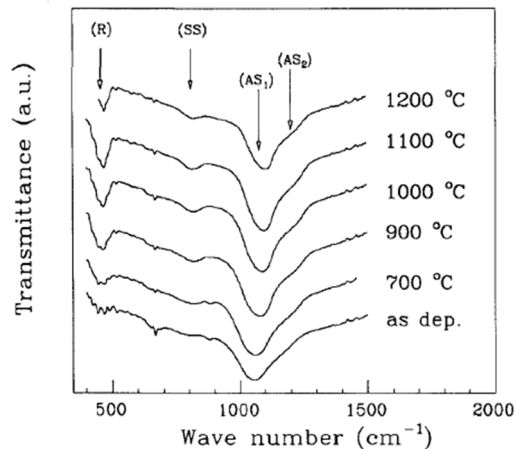


FIG. 8. Infrared absorption data in the region of the Si-O allowed vibrations.

And in general, crystallized silicon is more optically transmissive than amorphous, as-deposited silicon. For example, as reported by Janai et al., when silicon crystallizes as a result of annealing, “the absorption profile shifts back to higher energies and approaches that of single-crystal silicon.” EX1037, at 16, Fig. 1. In other words, the transmissivity of the polysilicon goes up across a broad spectrum of wavelengths.

304. The annealed SIPOS layer of Kwark, therefore, has greater optical transmissivity (and less absorption) than the as-deposited SIPOS layer, such that the thermal treatment annealing of Kwark increased the optical transmissivity.

12. Claim 7 – Dopant Activation

305. Claim 7 depends from claim 1 and adds the additional step: “*wherein* [a] *the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and* [b] *wherein the thermal treatment activates doping atoms in the compound.*”

306. Part [a] of claim 7 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound.*” I discussed how the combination of Froitzheim and Kwark satisfies this limitation in Paragraphs 260-266 above.

307. As for part [b], in the combination of Froitzheim and Kwark, Kwark’s annealing step (*thermal treatment*) further activates dopants in the SIPOS layer (“*activates doping atoms in the compound*”). In particular, Kwark disclosed that “the CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant.” EX1006 at 742.

308. The dopant activation process is further explained by Quirk, EX1018. As Quirk explains, “[d]opants are useful to form semiconductor silicon only if they are activated dopants, meaning they are part of the silicon lattice structure.” EX1018 at 480. Dopants become activated when thermal energy, for example, energy imparted as a result of annealing, moves a dopant into a regular crystal site. *Id.* (“Thermal energy moves dopants into the regular crystal sites, a process known as crystal activation.”). This dopant activation process works the same for both p-type and n-type dopants. *Id.* (“An activated dopant can act as a donor or acceptor of electrons and is an n-type or p-type dopant with respect to silicon.”). Thus, Kwark’s anneal step would also activate p-type dopants (boron) in p-type SIPOS in the same manner as the n-type dopant activation disclosed in Kwark.

13. Claim 8 – PN Junction

309. Claim 8 depends from claim 1 and adds the additional step: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.*”

310. Part [a] of claim 8 repeats a limitation that is in claim 5: “*the at least one conductive and passivating layer comprises an amorphous, silicon containing compound.*” I discussed how the combination of Froitzheim and Kwark satisfies this limitation in Paragraphs 260-266 above.

311. As for part [b], in the combination of Froitzheim and Kwark, Kwark’s annealing step (*thermal treatment*) results in the “*diffusion of dopant atoms into the substrate*”. In particular, Kwark disclosed that one of the tested SIPOS/polysilicon emitters was “emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction.” EX1006 at 743. An outdiffused SIPOS emitter was also studied. EX1006 at Figs. 5-6 (depicting data for “Outdiffused Emitter (C)” for SIPOS contacts). As I explained more fully above in Paragraph 264, outdiffusion from emitter C means that during the annealing dopants passed from the SIPOS/polysilicon emitter through the interfacial oxide / chemox layer to form a shallow diffusion region in the substrate.

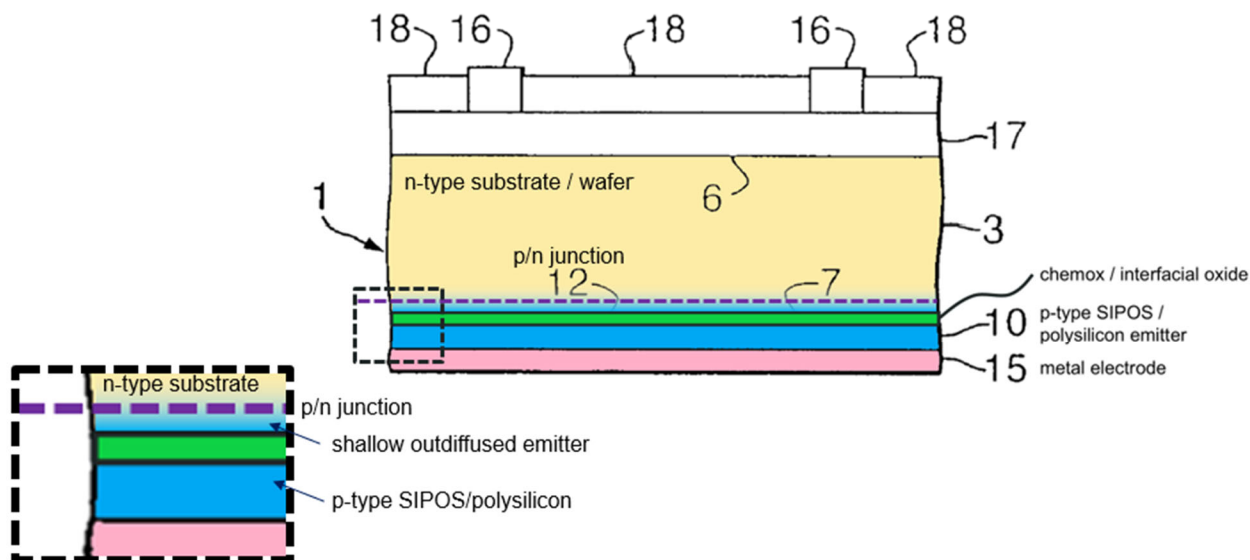
312. In the combination of Froitzheim and Kwark, depicted below, the diffusion of p-type dopants into the n-type substrate forms “a *p-n junction*”.

Froitzheim expressly discloses that the formation of a p-type diffused emitter on the back of an n-type substrate results in a pn junction. EX1008, ¶¶7, 25.

Replacing Froitzheim’s diffused in-substrate emitter with Kwark’s SIPOS or polysilicon emitter with interfacial oxide does not change that. Moreover, whether the combination of Froitzheim and Kwark is made using an n-type wafer and a p-type SIPOS/polysilicon emitter, or a p-type wafer and an n-type SIPOS/polysilicon emitter, either way the diffusion of the dopants from the emitter into the substrate results in a junction where p- and n-type dopant regions come together, thus forming a pn junction. EX1019 (Luque) at 83.

Combination of Kwark and Froitzheim

Fig.1.



X. CLAIMS 1-8 ARE UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, KWARK, AND NEVILLE

313. In my opinion, the combination of Froitzheim and Kwark in further view of Neville rendered obvious claims 1-8 of the 074 Patent.

314. I understand that Petitioner is asserting two distinct but similar grounds in the Petition, Ground III consisting of Froitzheim and Kwark and Ground IV consisting of Froitzheim, Kwark, and Neville. As I explained in Section IX above, the combination of Froitzheim and Kwark discloses each and every limitation of claims 1-8, and render these claims obvious.

315. Nevertheless, to the extent Patent Owner might argue that Kwark does not disclose a p-type SIPOS/polysilicon emitter, Neville makes clear that the

Skilled Artisan would understand that the dopant type of Froitzheim's n-type substrate, could be reversed. In particular, Figure VI.1 of Neville depicts a variety of possible solar cell configurations including a back junction cell like Froitzheim, which has a substrate that is either "p or n" type and a backside emitter that is either "n or p" type. EX1009 at Fig. VI.1, 199-200; see also Paragraphs 102-103 above.

316. Neville thus merely confirms that the Skilled Artisan would have no difficulty in combining Froitzheim and Kwark, for example, because the Skilled Artisan would understand that Froitzheim's substrate can be easily reversed from n-type to p-type and used with Kwark's n-type SIPOS or polysilicon emitter. See also, EX1034 (Spitzer) at 3:66-68 (for a back junction cell, the wafer (i.e., substrate) "may be formed of an n-type or p-type silicon."). The combination of Froitzheim, Kwark, and Neville, thus further renders obvious claims 1-8, for the same reasons as discussed above in Section VI.

XI. CLAIM 2 IS UNPATENTABLE AS OBVIOUS OVER FROITZHEIM, KWARK, AND SASAKI

317. In my opinion, the combination of Froitzheim, Kwark (and Neville), in further view of Sasaki (EX1010) further rendered obvious claim 2 of the 074 Patent.

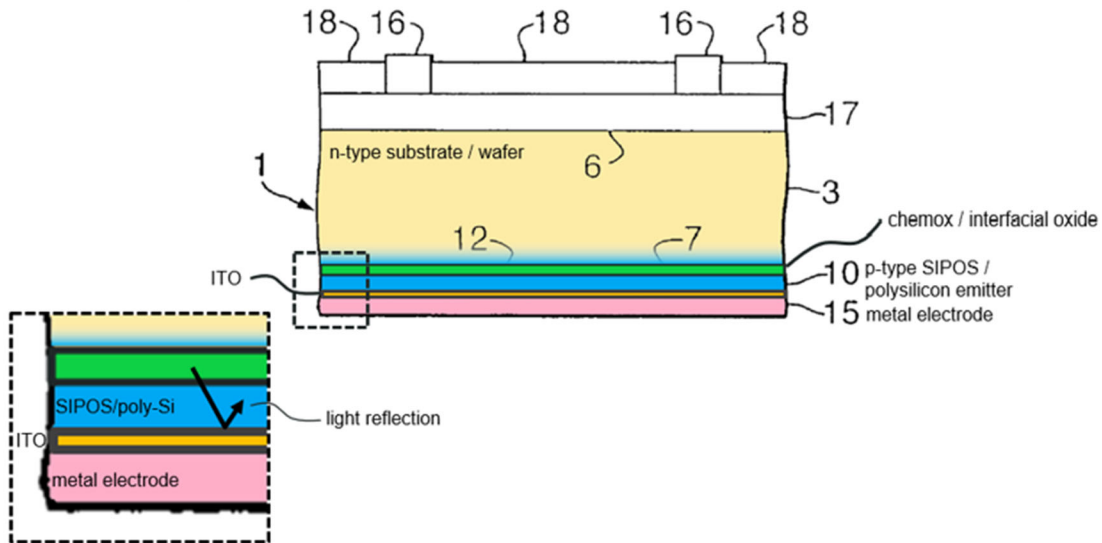
A. The Combination of Froitzheim, Kwark, and Sasaki

318. As discussed in more detail in the next section, Sasaki discloses inserting a transparent conductive indium tin oxide (ITO) film between an aluminum or silver contact and a silicon substrate in a solar cell. EX1010 at 3390.

319. In my opinion, it would have been obvious to a Skilled Artisan to further modify the combination of Froitzheim and Kwark by inserting the additional step of forming an ITO film as taught by Sasaki between the steps of forming the SIPOS emitter and forming the metal electrode, based on Sasaki's teachings that doing so would increase efficiency, as discussed more below. An exemplary device made using this combined method is illustrated in the figure below, in which Sasaki's ITO film (orange) is inserted between Kwark's SIPOS/polysilicon emitter (blue) and Froitzheim's rear electrode (pink).

Combination of Froitzheim, Yablonovitch, and Sasaki

Fig.1.



B. Sasaki Discloses the Method Step of Claim 2

320. Claim 2 depends from claim 1 and adds the additional step: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

321. Even if Patent Owner were to argue that the combination of Froitzheim and Kwark does not disclose the claim 2 step of depositing an antireflective layer or low reflective layer to form a good internal mirror, Sasaki also discloses this step for the same reasons as I discussed above in my analysis of this claim for the Yablonovitch, Froitzheim, and Sasaki ground in Paragraphs 209-213.

C. Motivation to Combine Froitzheim and Kwark with Sasaki's ITO Film

322. Sasaki, Froitzheim, and Kwark are analogous art because each is in the same field of endeavor—solar cell design. EX1008 (Froitzheim), Abstract, ¶¶1, 9; EX1006 (Kwark), 742. EX1010 (Sasaki) at abstract, 3389. Each is reasonably pertinent to the problems of efficiency and cost-effectiveness of solar cell designs. EX1008 (Froitzheim), Abstract, ¶¶1, 9; EX1006 (Kwark), 742; EX1010 (Sasaki) at abstract, 3389.

323. In my opinion, by April 2009, the Skilled Artisan would have been motivated to insert Sasaki's ITO film between the SIPOS/polysilicon emitter as taught by Kwark and the rear metal electrode as taught by Froitzheim, because Sasaki disclosed that the ITO film would improve the internal reflectivity of the back surface of the solar cell for both silver and aluminum electrodes, and thus the quality and efficiency of the solar cell compared to those that lacked the ITO film. In particular, Sasaki observed that by including an ITO film between the silicon substrate and a silver electrode, the internal reflectivity of the solar cell went up from 94.9% to 98.5%, and adding the ITO layer between the substrate and an aluminum contact increased internal reflectivity from 83.3% to 95.2%. EX1010 at 3390.

324. Increasing the internal reflectivity of the rear surface of the solar cell is important and advantageous because it increases the number of photons that are

converted into energy in the solar cell. Not every photon is absorbed and results in the generation of an electron/hole pair on the first pass through the solar cell. Once a photon passes completely through a solar cell, it is no longer available to form an electron/hole pair, and thus generate electrical current. However, by increasing the internal reflectivity at the back surface of a solar cell, some of photons of sunlight that enter the front of solar cell and pass unabsorbed through the substrate may get reflected at the back surface, rather than exiting the solar cell. Upon reflection, the photons then pass back through the solar cell, effectively doubling the probability that the photons will be absorbed. Internal reflectivity is therefore one way to increase a solar cell's efficiency in converting photons into electrical current.

325. Although Sasaki discloses the use of transparent and conductive oxide films in a thin-film solar cell, the Skilled Artisan would understand and be motivated to equally apply this to the Froitzheim/Kwark solar cell made from crystalline solar wafers. Even before 2008, these films were well known and have been used with heterojunction solar cells made from crystalline solar wafers, which have a very similar structure to the proposed combination. EX1019 (Luque) at 289 (Fig. 7.14) (“On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed” on top of the TCO layers; “Mass production of HIT cells started in 1997”).

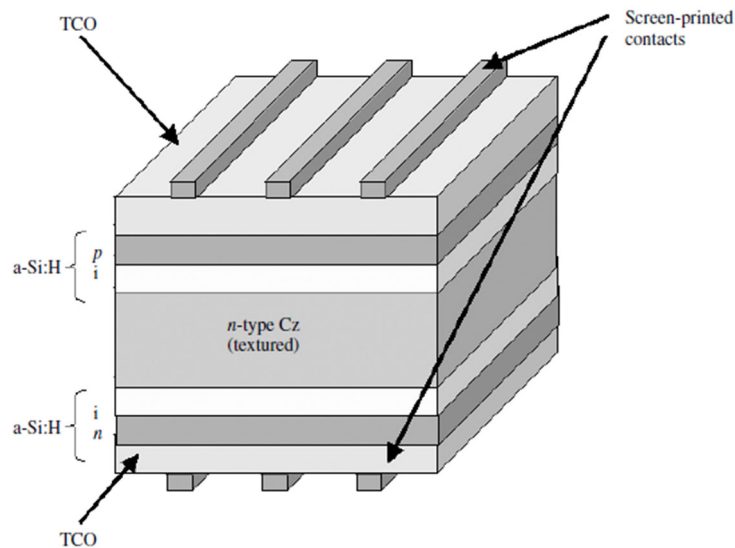


Figure 7.14 Structure of the HIT cell

D. Reasonable Expectation of Success

326. Inserting the ITO film of Sasaki between the SIPOS/polysilicon emitter layer and rear metal electrode in the combination of Kwark and Froitzheim, would have been well within the level of the Skilled Artisan by 2009. It would have been a simple addition of a known element for another to obtain predictable results.

327. Specifically, after completing Kwark's steps of depositing the SIPOS/polysilicon emitter and annealing the test structures, EX1006 at 743, the Skilled Artisan would perform the step of depositing the ITO layer as taught by Sasaki, EX1010 at 3390, before proceeding to Froitzheim's step of forming the rear metal contacts, EX1008, ¶¶48-49. The result would be a solar cell with increased internal reflectivity at the rear surface, as reported by Sasaki. EX1010 at 3390. Such a modification would further constitute use of a known technique

(depositing and ITO film) to improve similar devices (Froitzheim's back junction solar cell) in the same way. It would also constitute applying a known technique to a known device ready for improvement to yield predictable results.

328. Combining Froitzheim/Kwark with Sasaki as described here would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished with a reasonable expectation of success. Even before 2008, forming a TCO layer on top of deposited doped layers were well known and well within the skill of the Skilled Artisan. See EX1019 (Luque) at 289 (Fig. 7.14) ("On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed" on top of the TCO layers). The combinations would simply have been the combination of prior art elements according to known methods to yield predictable results, namely, the straightforward deposition of an indium tin oxide layer according to standard, well-known deposition techniques.

XII. OBJECTIVE FACTORS

329. I have not seen any evidence of commercial success attributable to the 074 Patent's claims. I understand that First Solar was not the original patent owner, but instead acquired the patent from the original owner, TetraSun, Inc. I also understand that Patent Owner does not practice the 074 Patent, according to a listing of marked patents available on Patent Owner's website. EX1033. Patent

Owner also does not assert it practices the 074 Patent in its district court complaint against Petitioner. EX1024. Moreover, I have been in working in the solar cell research for over 40 years. That Patent Owner is not practicing the 074 Patent is consistent with my understanding, based on my experience in this field and what I have read and reviewed over the years, because Patent Owner's commercial products are based on thin film cadmium telluride (CdTe) technology, rather than silicon wafer-based cells).

330. There is also no evidence of unexpected results for the claimed invention, or any long felt and unsolved need. In fact, Yablonovitch and Kwark both proposed forming an interfacial oxide between a SIPOS/polysilicon emitter layer, and using heat to drive dopants from the emitter through the oxide into the substrate, decades before the 074 Patent's effective filing date, and observed that doing so would be beneficial to the efficiency of solar cells. Accordingly, there is no unexpected result in replacing the backside diffused emitter in a back junction solar cell like Froitzheim with a polysilicon emitter having an interfacial oxide layer in between, as taught by Yablonovitch and Kwark. The Skilled Artisan would have expected to reap benefits from such modification such as higher solar cell efficiencies and lower recombination, as seen from the teachings of Yablonovitch and Kwark. EX1005 (Yablonovitch) at abstract ("We have found rather good performance in SIPOS-crystalline silicon-SIPOS double

heterostructure solar cells.... This suggests that crystalline silicon solar cells can be much more efficient than had been suspected.”); EX1006 (Kwark) at abstract (“an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role” in explaining the reduction in emitter saturation current in SIPOS emitters).

331. And including an oxide layer between the polysilicon layer and the substrate was well-known to confer expected benefits as well. For example, prior to the 074 Patent, Cousins (EX1032) did exactly that. In the embodiment Figure 1 of Cousins below, for example, a p-type polysilicon (blue) emitter is separated from an n-type substrate (yellow) by a tunnel oxide (green):

In the example of FIG. 1, the solar cell **100** includes a backside junction formed by a P-type doped polysilicon emitter **108** serving as a P-type diffusion region and an N-type silicon substrate **101** serving as an N-type diffusion region....

In one embodiment, the polysilicon emitter 108 is formed on a tunnel oxide layer 107. The polysilicon emitter 108 may be formed by forming a layer of polysilicon using Chemical Vapor Deposition (CVD), such as Low Pressure CVD (LPCVD) or Plasma Enhanced CVD (PECVD), and thermal anneal. The polysilicon emitter 108 may have a sheet resistance of 100 Ω /sq, and a thickness of 1000 to 2000 Angstroms. The tunnel oxide layer 107 may comprise silicon dioxide thermally grown to a thickness of about 10 to 50 Angstroms on the backside surface of the substrate 101. A metal contact 110 electrically connects to the polysilicon emitter 108 through contact holes 123 formed through a dielectric comprising a silicon dioxide layer 109. [EX1032, 2:28-31, 2:57-3:2.]

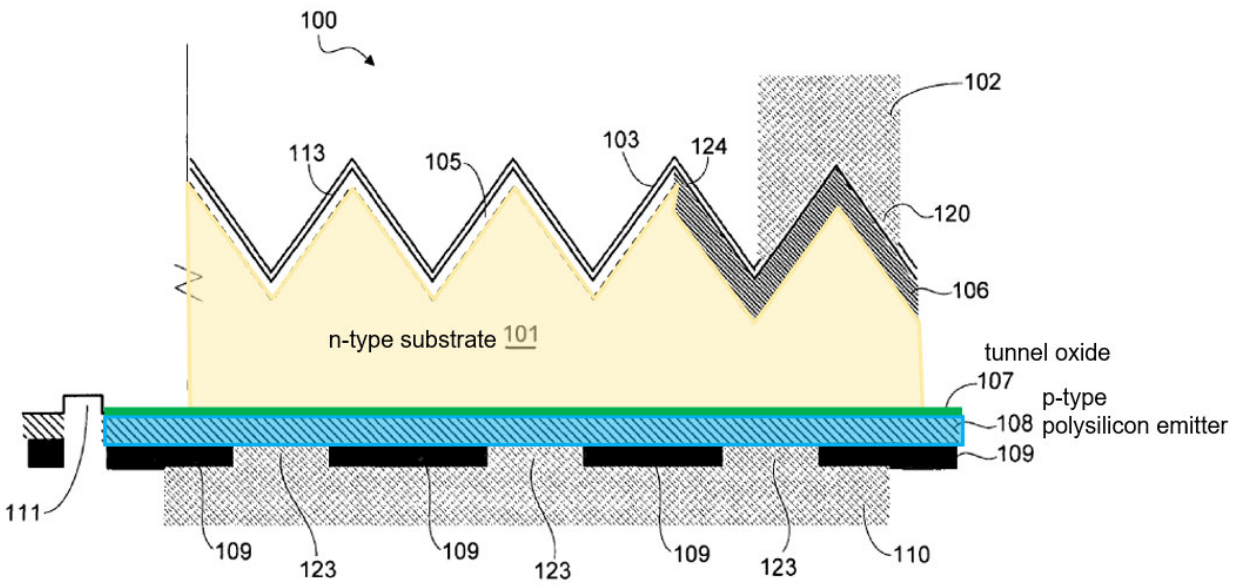


FIG. 1

Cousins also noted that, for power plants where power generation—not aesthetics—is the only concern for the design of a solar cell, front contact solar cells like the ones disclosed by Cousins are more efficient and inexpensive than prior solar cells:

While backside contact solar cells have an aesthetic advantage over front contact solar cells due to the absence of metal contacts on the front side, and are thus preferred for residential applications, aesthetics is not a major requirement for power plants and other applications where power generation is the main concern. **Disclosed herein are structures for a relatively efficient and cost-effective front contact solar cell and processes for manufacturing same.** [EX10032 at 1:32-42.]

332. The fact that Cousins made the combinations of Froitzheim and Yablonovitch or Kwark asserted here further suggests that the method of making

the combination itself does not confer unexpected results, but rather, reflects an application of known structures and methods of manufacture that were already understood to reap benefits.

PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,130,074

Attachment A
Materials Relied On

Exhibit #	Reference Name
1001	U.S. Patent No. 9,130,074
1002	File History of U.S. Patent No. 9,130,074
1005	E. Yablonovitch, et al., A 720 mV open circuit voltage SiO _x :c-Si:SiO _x double heterostructure solar cell, Appl. Phys. Lett. 47 (11) (Dec. 1, 1985) (“Yablonovitch”)
1006	Y.H. Kwark et al., “SIPOS Heterojunction contacts to silicon,” International Electron Devices Meeting (1984): 742-745 (“Kwark”)
1007	Y.H. Kwark, et al., N-Type SIPOS and Poly-Silicon Emitters, Solid-State Elecs. Vol. 30, No. 11, pp. 1121-1125 (1987)
1008	EP 1732142 A1 (“Froitzheim”)
1009	R. Neville, Solar Energy Conversion: The Solar Cell, 2nd Ed. (Elsevier 1995) (excerpted) (“Neville”)
1010	H. Sasaki, et al., Light Trapping for Thin-Film Silicon Solar Cells Fabricated on Insulator, Jpn. J. Appl. Phys., Vol. 33, pp. 3389-3392 (1994) (“Sasaki”)
1011	U.S. Patent No. 4,525,593 (“Yablonovitch Patent”)
1012	J.Y. Gan, et al, Polysilicon Emitters for Silicon Concentrator Solar Cells, Twenty First IEEE Photovoltaic Specialists Conference-1990, Vol. 1, pp. 245-250 (“Gan”)
1013	W. Fussel, et al., Structural, optical and electrical properties of SIPOS passivation layers, Microelectronic Engineering 22 (1993) 355-358 (“Fussel”)
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