

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CANADIAN SOLAR (USA) INC.,
Petitioner,

v.

FIRST SOLAR, INC.
Patent Owner.

Patent No. 9,130,074

Title: High-Efficiency Solar Cell Structures and Methods of Manufacture

Inter Partes Review No. IPR2025-01432

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,130,074**

CONTENTS

I.	INTRODUCTION	1
II.	IPR PROCEDURAL REQUIREMENTS	1
A.	CSUSA Can Contest The 074 Patent	1
B.	IPR Fee (37 C.F.R. §42.15(a))	1
C.	Mandatory Notices (37 CFR § 42.8(b))	2
III.	CHALLENGED CLAIMS AND GROUNDS	3
IV.	PERSON OF ORDINARY SKILL IN THE ART	3
V.	CONTESTED PATENT OVERVIEW	4
A.	Filing Date	4
B.	074 Patent Overview	4
C.	The 074 Patent’s Prosecution History	7
D.	The 074 Patent Claims	11
VI.	KNOWN TECHNOLOGIES NOT CONSIDERED BY EXAMINER	11
VII.	CLAIM CONSTRUCTION	14
VIII.	PRIOR ART DETAILED DESCRIPTION	14
A.	Yablonovitch (EX1005)	14
B.	Kwark (EX1006)	18
C.	Froitzheim (EX1008)	20
D.	Neville (EX1009)	21
IX.	GROUND I: CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE OVER FROITZHEIM AND YABLONOVITCH	22
A.	Motivation to Modify Froitzheim with Yablonovitch	24
B.	Reasonable Expectation of Success	27
C.	Froitzheim and Yablonovitch Disclosed All Claimed Steps	31

1. Claim 1	31
a) [1.a] Preamble.....	31
b) [1.b] Central Substrate.....	31
c) [1.c] Interface Passivation Layer.....	32
d) [1.d] Conductive and Passivating Layer	33
e) [1.e] Thermal Treatment.....	35
f) [1.f] Metallization.....	38
2. Claim 2 – Antireflective Layer	45
3. Claim 4 - Perforation.....	47
4. Claim 5 - Crystallization	48
5. Claim 6 – Transmissivity	49
6. Claim 7 – Dopant Activation	52
7. Claim 8 – PN Junction	52
 X. GROUND II: CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE OVER FROITZHEIM, NEVILLE, YABLONOVITCH.....	 54
 XI. GROUND III: CLAIMS 1-8 ARE UNPATENTABLE OVER FROITZHEIM AND KWARK.....	 55
A. Motivation to Modify Froitzheim with Kwark	56
B. Reasonable Expectation of Success	59
C. Froitzheim and Kwark Disclosed All Elements.....	62
1. Claim 1	62
a) [1.a] Preamble.....	62
b) [1.b] Central Substrate.....	62
c) [1.c] Interface Passivation Layer.....	63
d) [1.d] Conductive and Passivating Layer	64
e) [1.e] Thermal Treatment.....	65
f) [1.f] Metallization.....	67
2. Claim 2 – Antireflective Layer	69
3. Claim 3 – Separation.....	69

4. Claim 4 – Perforation	72
5. Claim 5 – Crystallization	74
6. Claim 6 – Transmissivity	75
7. Claim 7 – Dopant Activation	76
8. Claim 8 – PN Junction	76
XII. GROUND IV: CLAIMS 1-8 ARE UNPATENTABLE OVER FROITZHEIM, NEVILLE, AND KWARK.....	78
XIII. GROUNDS V AND VI: CLAIM 2 IS UNPATENTABLE IN FURTHER VIEW OF SASAKI	79
A. Sasaki Discloses the Step of Claim 2	80
B. Ground V: Froitzheim (with or without Neville), Yablonovitch, and Sasaki.....	81
C. Ground VI: Froitzheim (with or without Neville), Kwark, and Sasaki.....	82
D. Motivation to Combine	83
E. Reasonable Expectation of Success	85
XIV. OBJECTIVE FACTORS SUPPORT OBVIOUSNESS.....	86
 Attachment A. Proof of Service of the Petition	
 Attachment B. List of Evidence and Exhibits Relied Upon in Petition	
 Attachment C. Table of Claims and Elements	

I. INTRODUCTION

Canadian Solar (USA) Inc. (“CSUSA”) respectfully requests that claims 1-8 of U.S. Patent 9,130,074 (“074 Patent”) be cancelled as unpatentable. As demonstrated below, these claims are directed to well-known, obvious methods of making solar cells with a SIPOS/polysilicon emitter with an interfacial oxide layer, disclosed by others in publications more than one year before the effective filing date. None of the prior art references relied upon in this Petition were considered by the Examiner during prosecution, and they address the specific deficiencies that the Patent Owner (“PO”) argued was not in the prior art. PO does not practice the 074 Patent and the purported invention did not achieve unexpected results. Thus, the PTAB should institute this IPR and cancel claims 1-8 of the 074 Patent.

II. IPR PROCEDURAL REQUIREMENTS

A. CSUSA Can Contest The 074 Patent

CSUSA certifies it is not barred or estopped from requesting *inter partes* review (“IPR”) of the 074 Patent. Neither CSUSA, nor any party in privity with CSUSA, has filed a civil action challenging the 074 Patent’s validity nor filed any prior IPR against the 074 Patent. This IPR is filed within one year of the date of service of a complaint alleging infringement of the patent against CSUSA.

B. IPR Fee (37 C.F.R. §42.15(a))

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a) to Deposit Account No. 50-1597.

C. Mandatory Notices (37 CFR § 42.8(b))

Canadian Solar (USA) Inc., Canadian Solar Inc., CSI Solar Co. Ltd., Canadian Solar Manufacturing (Thailand) Co. Ltd., Canadian Solar International Limited, and Canadian Solar US Module Manufacturing Corporation are the real parties in interest. The 074 Patent is involved in the following legal proceedings:

- *First Solar, Inc. v. JinkoSolar Holding Co. Ltd.*, 1-25-cv-00223
(D. Del.)
- *Mundra Solar PV Limited v. First Solar, Inc.*, 1-25-cv-00462 (D. Del.)
- *First Solar, Inc. v. Canadian Solar Inc., et al.*, 1-25-cv-00582
(D. Del.)
- *JinkoSolar Co., Ltd. v. First Solar, Inc.*, IPR2025-01130 (P.T.A.B.)

Lead Counsel is Samuel N. Tiu (Reg. No. 47,997), stiu@sidley.com, 213-896-6095. Backup Counsel are Brooke S. Böll (Reg. No. 76,268), brooke.boll@sidley.com, 213-896-6633, Michael Roberts (Reg. No. 82,131), mlroberts@sidley.com, 214-981-3472.

Service on CSUSA may be made by email to counsel above and mail or hand delivery to: Sidley Austin LLP, 350 South Grand Avenue, Los Angeles, CA 90071. The fax number for lead and backup counsel is 213-896-6600.

Proof of service of this petition is provided in **Attachment A**.

III. CHALLENGED CLAIMS AND GROUNDS

Claims 1-8 of the 074 Patent are unpatentable as follows:

Ground	Claims	Basis	References
I	1-2, 4-8	§103	Froitzheim, Yablonovitch
II	1-2, 4-8	§103	Froitzheim, Yablonovitch, Neville
III	1-8	§103	Froitzheim, Kwark
IV	1-8	§103	Froitzheim, Kwark, Neville
V	2	§103	Froitzheim, Yablonovitch, Sasaki (with or without Neville)
VI	2	§103	Froitzheim, Kwark, Sasaki (with or without Neville)

Attachment B lists the evidence relied upon in this petition.

IV. PERSON OF ORDINARY SKILL IN THE ART

The person of ordinary skill in the art in the 074 Patent's field of solar cell design and fabrication in 2009 ("Skilled Artisan") would have been someone with an advanced degree involving the discipline of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field. Alternatively, that person would have had a bachelor's degree in electrical engineering, applied physics, or

materials science, and at least four years of experience designing, developing, or researching in the field. EX1003, ¶45.

V. CONTESTED PATENT OVERVIEW

A. Filing Date

The 074 Patent, filed as a PCT on April 21, 2010, claims priority to U.S. Provisional Application No. 61/171,194, filed April 21, 2009. All prior art relied upon in Grounds I-VI predate April 21, 2008.

B. 074 Patent Overview

The 074 Patent relates to solar cells and their manufacture. Figure 6 illustrates “a partial cross-sectional view of a solar cell 60 having an n-type front [topside], n- or p-type wafer [65] and a p-type back [bottom side].” EX1001, 5:14-15. When the cell utilizes an n-type wafer with a p-type back, the solar cell in Figure 6 is categorized as a “back junction solar cell” (*id.* at 5:35-37) and the “minority carriers are collected at the side opposed to the illumination” i.e., the backside. *Id.* at 4:32-33.

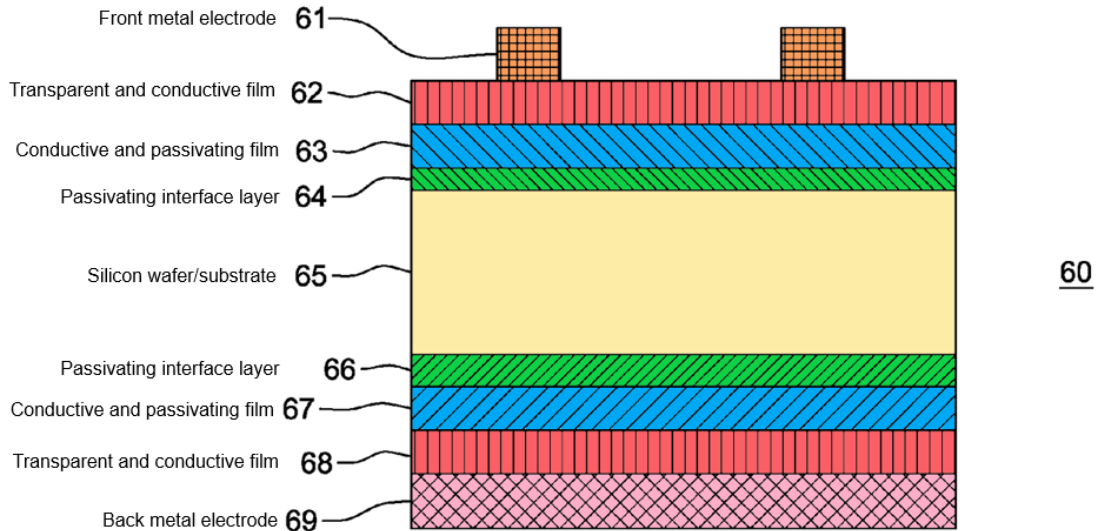


FIG. 6

On each side of the silicon wafer 65 is formed various layers of materials. First, immediately next to it is formed “electrically passivating interface layer[s]” 64 and 66, respectively. EX1001, 5:56-6:4.¹ For example, this layer can be formed of “*silicon oxide*, silicon nitride, intrinsic amorphous silicon, intrinsic polycrystalline silicon” *Id.* (emphasis added).

Next to the “passivating interface layer” 64 and 66 is formed a highly doped² “electrically passivating and conductive film” 63 and 67, respectively. EX1001,

¹ “Passivation” reduces recombination, which impacts solar cell efficiency.

EX1003, ¶75.

² “Doping” is the process of introducing impurities (“dopants”), typically boron or phosphorus, into silicon to alter the silicon’s conductive properties. EX1018, 34-

5:42-55, 6:5-15. According to the 074 Patent, among other materials, these layers can be formed of n-type and p-type “amorphous or *polycrystalline silicon*: phosphorus doped amorphous silicon” and “boron doped silicon,” respectively. *Id.* “Any of the above listed examples may include oxygen and hydrogen” *Id.* (emphasis added).

On top of the “passivating and conductive film[s]” 63 and 67 are formed “transparent and conductive film[s]” 62 and 68, respectively, made of, for example, transparent conductive oxides (“TCO”) like indium tin oxide or zinc oxide. EX1001, 5:32-41, 6:18-24.

And on the “transparent and conductive film[s]” 62 and 68 are formed the front metal electrode 61 and back metal electrode 68, respectively. EX1001 at 5:31, 6:25.

The specification explains that “[a] back junction cell with a full area back contact [e.g., as in Figure 6] has the advantage that the minority carriers do not have to flow laterally through the emitter to reach the contacts.” EX1001, 5:1-6. “This reduces the losses associated with the lateral transport of the minority carriers within the emitter,” unlike the front junction cell emitter 42 in FIG. 4. *Id.*

38. Silicon doped with boron is known as a “p-type” material, and silicon doped with phosphorous is known as an “n-type” material. *Id.*, 36.

at 5:4-11; 2:50-52. An emitter is generally known in the art as a doped region with dopants that have opposite polarity with the dopants in the substrate. EX1003, ¶70.

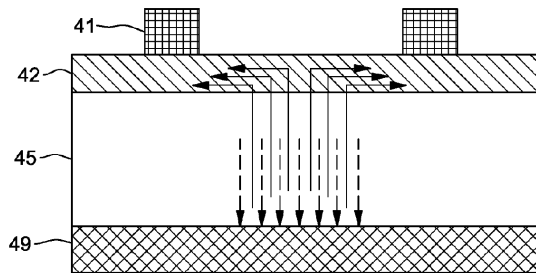


FIG. 4

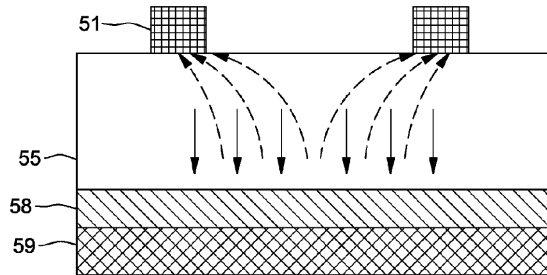


FIG. 5

FIG. 4 illustrates the minority and majority carrier flows for a front junction cell, where the minority carrier flow is represented by solid lines and the majority carrier flow is represented by dashed lines. *Id.* at 4:52-59. To reach the electrodes 41, the minority carriers generated from the wafer 45 must first flow vertically toward the emitter 42 and then laterally within the emitter 42. *Id.* In contrast, when the solar cell is a back junction cell like in FIG. 5 with full metal electrode coverage, “[t]he minority carriers (solid lines) can use the shortest geometrical path to reach the rear p-type emitter 58, and their transport within the emitter is vertical instead of mainly lateral.” *Id.* at 4:60-67. Reducing the lateral flow thus shortens the carrier flow path. *Id.*; EX1003, ¶¶54-55.

C. The 074 Patent’s Prosecution History

During prosecution, claim 1 initially recited:

A method of fabricating a solar cell, comprising:

providing a wafer as a central substrate;

depositing or growing at least one interface passivation layer over the substrate;

depositing at least one conductive layer over the passivation layer(s);

providing thermal treatment; and

providing metallization as electrodes.

EX1002, 125.

The Examiner initially rejected the claims as anticipated by WO2008/115814 (“Carlson”) and also by US6,821,875 (“Wenham”). *Id.*, 274. In response, the Applicant amended claim 1:

- First, the amended claim required the “conductive layer” to *also* have a “passivating” function, and to “comprise a dopant.”
- Second, the amended claim required the thermal treatment to be at 500°C or higher and to render two effects: “crystallizing, at least in part, the at least one conductive and passivating layer” and “facilitating diffusion of the dopant through the at least one interface passivation layer.”
- Third, the amended claim required the metallization as electrodes to be “over the at least one conductive and passivating layer”.

Id., 367.

With these modifications, the Applicant argued that the “at least one conductive and passivating layer comprising a dopant deposited on at least one interface passivating layer over a substrate” limitation is ‘itself believed to be

novel.” *Id.*, 371. The Applicant further argued that “[a] layer combining both conductive and passivating functions/features does not appear in the applied art” and this layer “provides both electrical conductivity to allow current flow as well as surface passivation to prevent carrier recombination.” *Id.*

As to the thermal treatment, the Applicant argued that this also “distinguish[es] amended claim 1 over the applied art.” *Id.*, 372. The thermal treatment, according to the Applicant, “preserves or improves the passivating qualities of the conductive and passivating layer through its crystallization ... and at the same time allows the dopant diffusion out of the conductive and passivating layer through the interface passivation layer(s).” *Id.*

Finally, regarding metallization, the Applicant argued that the claimed method allows the metal electrodes to be “provided over the conductive and passivating layer ... without the need for a protective dielectric layer, or the need to create openings or firing holes through multiple layers of the solar cell to permit contact between metal electrodes and semiconductor substrate.” *Id.*, 373. That is, the metal “can be deposited directly on the conductive and passivating layer(s)” or “additional conductive layers can optionally be placed over the conductive and passivating layer with metallization provided over the additional conductive layers.” *Id.*

After this response, the Examiner issued a Final Office Action rejecting the amended claims as obvious over Wenham in view of US2009/0235972 (“Fukushima”)³, and as further obvious over US6,210,991 (“Wenham II”) in view of Fukushima. *Id.*, 415, 417. In response, the Applicant further amended Claim 1. *Id.*, 466-67.

In the remarks accompanying the amendment, the Applicant continued to argue that Wenham “nowhere discloses providing a conductive and passivating layer comprising a dopant on an interface passivation layer.” *Id.*, 469. The Applicant further argued that Wenham and Wenham II “do not disclose providing thermal treatment to crystallize a conductive and passivating layer and facilitate diffusion of a dopant from a conductive and passivating layer throughout an interface passivation layer.” *Id.*, 470. In addition, the Applicant argued that its method of diffusing the dopant from the conductive and passivating layer through the interface passivating layer “enable[s] charge carrier flow paths through the conductive and passivating layer and the interface layer” resulting in the substrate and the electrodes “having direct electrical connectivity flow paths through the intervening layers of the solar cell via the diffused dopant.” *Id.*, 472. This allows for the “metallization as electrodes” to be formed after the thermal treatment,

³ The Fukushima publication was used as a translation for WO 2007/125903.

without the metal material needing “to penetrate through one or more other layers of the solar cell to make contact with the solar cell substrate.” *Id.*, 471.

Based on these comments, the Examiner accepted the Applicant’s arguments and initiated an interview to suggest certain amendments that “would bring the application into condition for allowance.” *Id.*, 483. In the Notice of Allowance, the Examiner made no mention of Wenham, Wenham II, or Fukushima, but instead discussed two additional references—a publication by Bau and US Patent No. 7,202,143 to Naseem. *Id.*, 485-86. The Examiner stated “there is no teaching or motivation to provide metallization as electrodes which directly contact the conductive and passivation layer, as that layer supports a layer which forms the absorbing portion of the solar cell.” *Id.*, 485.

D. The 074 Patent Claims

Attachment C includes a listing of claims 1-8.

VI. KNOWN TECHNOLOGIES NOT CONSIDERED BY EXAMINER

Contrary to the Applicant’s arguments during prosecution, a “conductive and passivating layer [e.g., a polycrystalline silicon layer] comprising a dopant deposited on at least one interface passivating layer [e.g., silicon oxide layer] over a substrate” was not novel.

The 074 Patent identifies doped polycrystalline silicon (with or without oxygen) as an exemplary material for the “[e]lectrically passivating and conductive

film,” EX1001, 5:42-55, 6:5-15, and silicon oxide as an exemplary material for the “[e]lectrically passivating interface layer.” *Id.* at 5:56-6:4. Long before 2009, those skilled in the art already recognized that polycrystalline silicon (also known as “polysilicon”) films, either mixed with small amounts of oxygen (known as “SIPOS”) or not, could reduce solar cell recombination by passivating the silicon substrate and thereby improve solar cell efficiency. EX1003, ¶¶79-84. An interfacial oxide layer was also known to further improve solar cell efficiency along with the polysilicon film. *Id.* An “interfacial oxide layer” refers to a thin layer of silicon oxide in between the substrate and the polysilicon layer. EX1003, ¶79.

Deposited polysilicon emitters with an interfacial oxide layer were first used to improve the performance of bipolar transistors in 1984. EX1003, ¶80 (citing EX1027, Ashburn). Then in 1985, Yablonovitch et al. showed that n- or p-type doped “SIPOS” films (i.e. polycrystalline silicon mixed with oxygen) together with the interfacial oxide layer reduces recombination (as measured by J_o) by one to two orders of magnitude compared to conventional dopant diffused layers. EX1003, 80 (citing EX1005 (Yablonovitch)). Yablonovitch states that its finding “suggests that crystalline solar cells can be much more efficient than had been suspected.” *Id.*, Abstract, *see also* EX1028, 597 (“There have been a considerable number of reports recently on improved bipolar transistor emitters made of polycrystalline

silicon or of SIPOS.... Such heterojunctions are valuable not only for emitter efficiency in bipolar transistors, **but also for solar cells**").

Subsequently in 1987, another publication modeled the projected efficiencies of what would be possible incorporating "SIPOS" emitters versus diffused emitters, and showed a more than one percent absolute increase in efficiency for the solar cell. EX1029, 2122; EX1003, ¶81.

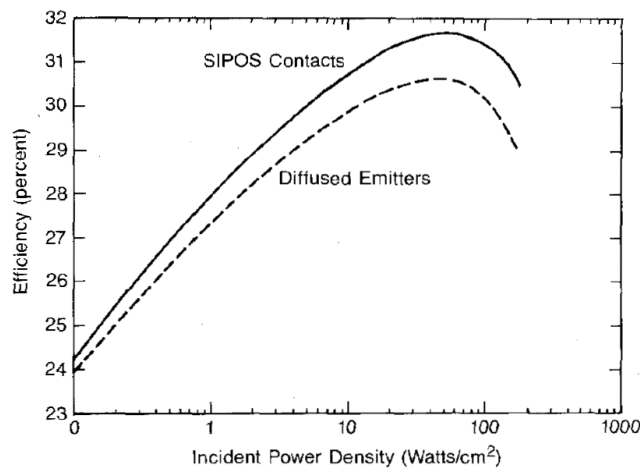


Fig. 9. A comparison of the projected efficiencies possible for a cell incorporating SIPOS emitters (solid curve), compared to projections for diffused emitters as used to date (dashed curve).

Around the same time, Kwarik extended the findings with SIPOS and an interfacial oxide layer to the use of relatively oxygen-free polysilicon with an interface oxide layer, recognizing that "incorporation of these films into the emitter structure ... translates into potential improvements of energy conversion efficiency for solar cells...." EX1006, 742.

By 2008, it was well recognized that "[g]reater improvements in open-circuit voltage and efficiency can be achieved from polysilicon contact solar cells in

devices with a deliberately grown interfacial oxide with thin polysilicon layer whatever the grain width and cell thickness.” EX1030 (Zouari), 322. By this time, others had published and filed patent applications describing front and back junction solar cells with the polysilicon emitter structure deposited on an interfacial oxide layer formed over the substrate. EX1003 ¶84 (citing EX1032, 2:28-31, 2:58-58, Fig. 1; EX1036, 1149).

VII. CLAIM CONSTRUCTION

Claim constructions are not necessary to resolve this Petition.

VIII. PRIOR ART DETAILED DESCRIPTION

A. Yablonovitch (EX1005)

Yablonovitch, et al, “A 720 mV open circuit voltage SiO_x :c-Si:SiO_x double heterostructure solar cell” (“Yablonovitch”) was published at least by 1988, and before April 2008. EX1005; EX1043, ¶¶43-58.⁴ Exhibit EX1005 is an authentic copy of Yablonovitch that was published before April 2008. *Id.* Yablonovitch is thus prior art under 35 U.S.C. §102(a) and (b)⁵.

⁴ The original specification of US7,851,336, filed March 13, 2008, discusses Yablonovitch, confirming its publication before April 2008. EX1022; EX1023 (excerpt of file history).

⁵ Citations to 35 U.S.C. §102 in this Petition refer to the pre-AIA statute.

In this paper, Yablonovitch reported that “crystalline silicon solar cells can be much more efficient than had been suspected” by using a SIPOS emitter layer on a crystalline silicon substrate. EX1005, Abstract. “SIPOS” stands for “semi-insulating polycrystalline silicon,” which is a “mixture of microcrystalline silicon and silicon dioxide (SiO_x).” EX1005, 1211. In particular, Yablonovitch suggested replacing existing homojunction-type solar cells, in which the emitter layer is formed by diffusing a portion of the solar cell’s substrate with the opposite dopant type, with heterojunctions, in which the emitter is made of SIPOS, which has a different bandgap. *E.g.*, EX1005, Abstract (“The processing of these solar cells gives insights into the truly outstanding performance of the $n^+ \text{SIPOS} : p\text{-Si}$ heterojunction”); *id.* at 1211 (“In this configuration a narrow band-gap active layer is sandwiched between two wide band-gap layers of opposite doping”); EX1003, ¶87.

In particular, Yablonovitch reported that “ n^+ -type SIPOS heterocontacts on $p\text{-Si}$ [p-type silicon substrate]” showed forward saturation current J_o “two orders of magnitude superior to a conventional homojunction,” and that p-type SIPOS on n-type substrates were also “superior to that of a homojunction.” EX1005, 1211. Yablonovitch also noted the “excellent surface passivation” of the SIPOS heterocontacts. EX1005, 1212.

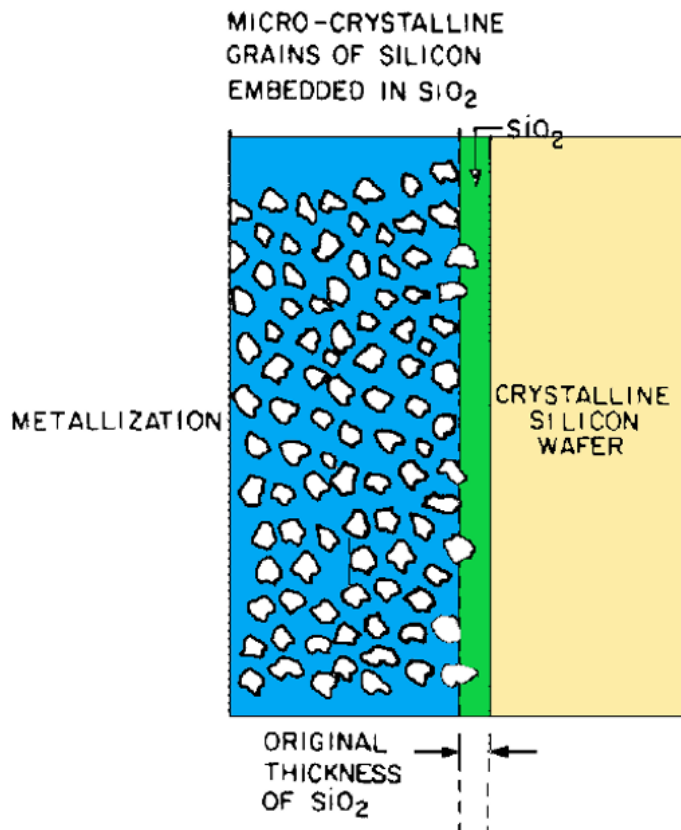
Yablonovitch summarized the process used to fabricate its SIPOS-based solar cells in Table II, reprinted below.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^\circ\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^\circ\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^\circ\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Prior to forming the SIPOS layers, Yablonovitch taught to thermally oxidize the silicon wafers with O_2 . EX1005, 1212, Table II (steps 5-6). Yablonovitch's oxidation step formed a thin layer of silicon oxide (SiO_2) on the surface of the wafer, shown in the excerpt of Yablonovitch Fig. 3 below. EX1005, Fig. 3⁶. Yablonovitch explained that the oxidation step was "[o]f critical importance in achieving th[e] performance level" Yablonovitch observed in the SIPOS solar cells, and "necessary toward achieving the most favorable figure of merit." EX1005, 1212.

⁶ Colorations in the figures are added by Petitioner unless otherwise noted.



Following the oxidation step, Yablonovitch deposited the SIPOS with a dopant. EX1005, 1213, Table II (step 7). The SIPOS mixture was then heated at 900°C, a step “necessary to precipitate microcrystalline silicon grains within the [SIPOS] material and to activate the phosphorus dopant.” EX1005, 1212, Table II (steps 8-9). Yablonovitch further noted that during the annealing step “phosphorus diffuses about 20-50Å into the silicon wafer.” *Id.*, 1212. As a result of heating, the micro-crystalline grains “protrude into the oxide as shown in Fig. 3,” such that “electrical contact [between the wafer and the SIPOS layer] is via thin spots and pinholes in the SiO₂.” *Id.*, 1213.

B. Kwark (EX1006)

Kwark et al., “SIPOS Heterojunction contacts to silicon,” International Electron Devices Meeting (1984): 742-745 (“Kwark”) was a paper presented in 1984 (EX1006, face) and published at least by 1985, and before April 2008. EX1043, ¶¶59-78. Kwark has also been known and cited by others in the field by at least 1997, including in a U.S. Patent that issued in 1997, further confirming its public dissemination before April 2009. EX1042, face. Exhibit 1006 is an authentic copy of Kwark that was published before April 2008. EX1043, ¶¶59-78. Thus, it is prior art under 35 U.S.C. §102(a) and (b).

Like Yablonovitch, Kwark taught the use of SIPOS and interfacial oxide layer for improving solar cells, but extended this to polysilicon (without oxygen) emitters. EX1006. As shown in Figure 4, Kwark likewise found that “intentionally grown chemical oxide [‘chemox’]” between polysilicon and the substrate “greatly decreases the J_{oe} ,” which “translates into potential improvements of energy conversion efficiency for solar cells.” EX1006, 742, 745; EX1003 ¶¶83, 93-95. Kwark noted a “large difference [i.e., decrease in performance] when the interfacial oxide is missing.” EX1006, 745, Fig. 4.

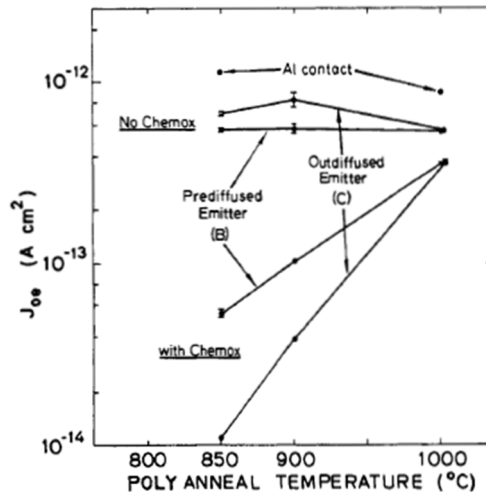


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

Moreover, in Fig. 4, “Al contact” refers to the “conventional aluminum contact” control with a diffused emitter that does not have either the polysilicon layer or SIPOS. EX1003, ¶¶93; EX1006, 743. As seen from the data, the recombination, as measured by J_{oe} , of the conventional diffused emitter is substantially higher than any of the experimental devices with polysilicon films with the chemox. *Id.*

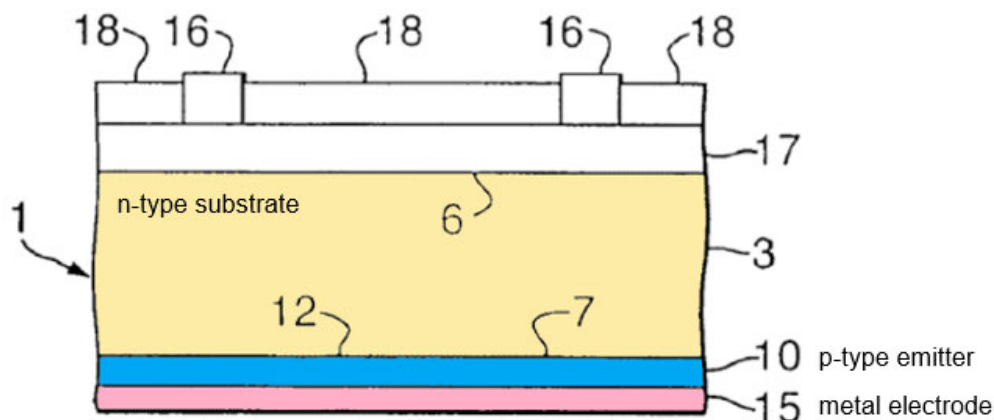
In 1987, the same authors published the same data in the *Solid State Electronics* and provided additional details of their testing. EX1007. This publication will be referred to as “Kwark II”. Kwark II is also prior art under 35 U.S.C. 102(b) having been published before April 2008. See EX1043, ¶¶79-98.

C. Froitzheim (EX1008)

EP1732142A1 (“Froitzheim”) was filed June 9, 2005 and published on December 13, 2006. EX1008, face. Froitzheim is thus prior art under 35 U.S.C. §102(a) and (b).

Froitzheim explained that in conventional solar cells, the emitter is placed at the front of the cell to form a PN junction with an oppositely doped substrate. EX1008, ¶2; EX1003, ¶99. However, Froitzheim proposed to instead place the emitter/PN junction at the rear side of the solar cell, and thus form a backside junction solar cell. EX1008, ¶8; EX1003, ¶99. Froitzheim’s Figure 1, shown below, is a solar cell 1 having an n-type body layer or substrate 3 with a front side 6 and a rear side 7. EX1008, ¶24.

Fig.1.



To fabricate this solar cell, Froitzheim starts with an n-type silicon substrate. EX1008, ¶39; EX1003, ¶99-100. The substrate’s rear surface is diffused with

boron, a p-type dopant. EX1008, ¶40. This diffused p-type doped layer 10 forms a backside junction or emitter with the oppositely doped n-type substrate. EX1003, ¶99. On the front side, phosphorus (an n-type dopant) is diffused onto the front surface of the substrate. EX1008, ¶¶43-44. Afterwards, passivation and anti-reflection coatings are applied “using known methods,” and front and rear metal contacts are applied. EX1008, ¶¶48-50, 60. Figure 1 of Froitzheim shows that the metal electrode 15 contacts the entire p-type emitter layer 10 at the backside of the substrate and provides full back coverage.

Froitzheim also discloses another embodiment in FIG. 3 where the metal electrode 35 is arranged in a “finger structure covering only part of the rear side” deposited by “screen-printing” and contacts the p-type emitter layer 10 at specific points through openings in a passivation layer 34. EX1008, ¶¶33, 48-50.

D. Neville (EX1009)

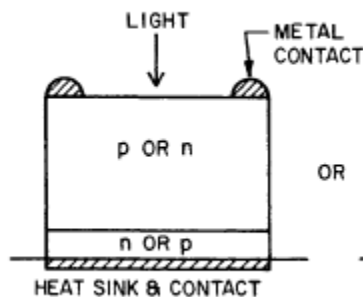
Although the specific embodiment illustrated in Froitzheim uses an n-type silicon substrate with a p-type emitter, it was well known to a Skilled Artisan that the dopant types for a back junction solar cell can also be reversed, i.e., a p-type silicon substrate used with an n-type emitter. EX1009, 200.

For example, the reverse dopant types were disclosed in a textbook authored by R. Neville, *Solar Energy Conversion, The Solar Cell*, Second Ed. (Elsevier

Science B.V.) (“Neville”), published no later than 1996. EX1009; EX1043, ¶¶99-122. Neville is therefore prior art under 35 U.S.C. §102(a) and (b).

In a chapter entitled “Solar Cell Configuration and Performance,” Neville depicted “three general configurations of solar cell-light interaction” in Fig. VI.1. EX1009, 199. One configuration depicts an “inverted configuration solar cell,” in which the emitter layer forms a PN junction on the backside of the cell. EX1009, 199, Fig. VI.1. As can be seen, the solar cell substrate is identified as either “p or n” type, while the emitter is labeled as “n or p” type, demonstrating that the Skilled Artisan understood that the polarity of the substrate and oppositely-doped emitter layer could be interchangeable.

Neville, Fig. VI.1 (Excerpt)



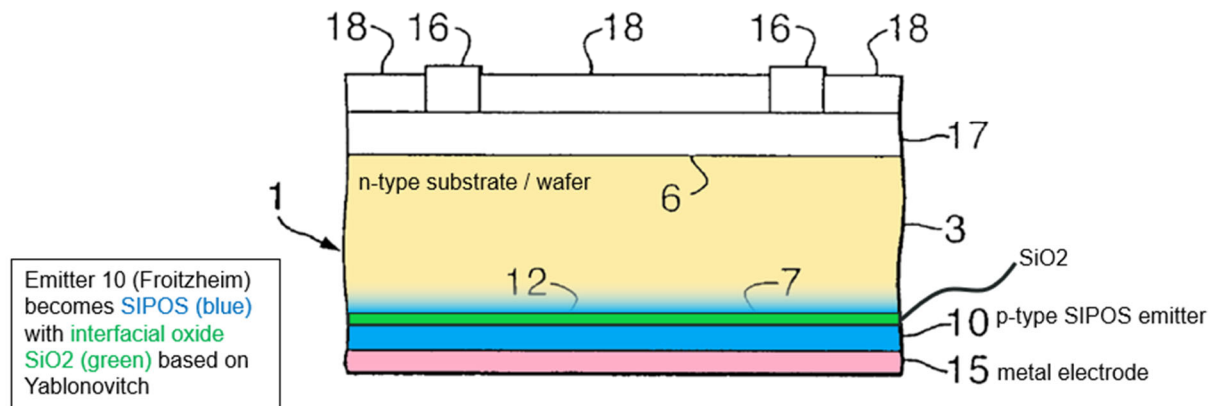
IX. GROUND I: CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE OVER FROITZHEIM AND YABLONOVITCH

To improve upon the back junction solar cell of Froitzheim, the Skilled Artisan would have replaced the *diffused* in-substrate emitter of Froitzheim with a deposited SIPOS emitter layer and an interfacial oxide layer, as taught by

Yablonovitch. The resulting modified solar cell is illustrated below using a modified Froitzheim Fig. 1 for illustration. EX1003, ¶108-110. The combination would be nothing more than replacing the backside diffusion step in Froitzheim with the steps of forming the oxide layer and SIPOS emitter in Yablonovitch on the backside of the Froitzheim's substrate before formation of Froitzheim's metal contacts. *Id.* This would form a backside junction SIPOS emitter with an interfacial oxide layer rather than a diffused in-substrate emitter layer. *Id.*

Combination of Yablonovitch and Froitzheim⁷

Fig. 1.



⁷ The “n-type” and “p-type” labels in the figure are merely illustrative. As discussed below, the dopant types of the substrate and emitter are interchangeable.

A. Motivation to Modify Froitzheim with Yablonovitch

Froitzheim and Yablonovitch are analogous art; they are both in the same field of solar cell design and fabrication. EX1003, ¶111; EX1008, Abstract, ¶¶1, 9; EX1005, Abstract, 1211-12. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1003, ¶111; EX1008, Abstract, ¶¶1, 9; EX1005, Abstract, 1211.

The Skilled Artisan would have been motivated to replace Froitzheim's diffused emitter with a deposited SIPOS emitter along with an oxide layer because Yablonovitch (and others) taught and suggested that this modification would improve the solar cell. EX1003, ¶112. Froitzheim's backside p-doped emitter is formed by diffusing boron (a p-type dopant) into an n-type substrate. EX1008, ¶¶24-26, 40-41. Because the p-type emitter 10 and n-type substrate are made of the same silicon material, they have the same bandgap and differ only in their polarity (i.e., dopant types). EX1003, ¶¶114-116. Froitzheim's emitter layer 10 thus forms what is known in the art as a "homojunction," in which two adjoining regions differ only in dopant type, but not in the bandgap of the material. *Id.*

Yablonovitch expressly taught the advantage of using SIPOS emitters over homojunctions such that the solar cells could be improved by replacing homojunctions with SIPOS emitters. Yablonovitch disclosed that it was known for SIPOS emitters to form "superior quality heterojunction[s]" having "greatly

enhanced current gains,” and Yablonovitch was interested in investigating SIPOS emitters in terms of “[a] more direct measure of heterojunction quality i[n] the forward saturation current J_o .”⁸ EX1005, 1211. Yablonovitch demonstrated that solar cells having SIPOS-emitters exhibited forward saturation currents J_o “superior to that of a homojunction” for both n⁺-type SIPOS contacts (on p-type silicon wafers) and p-type SIPOS contacts (on n-type silicon wafers). *Id.*

Yablonovitch discloses that its SIPOS-based cells also exhibited “excellent surface passivation.” EX1005, 1212. Yablonovitch credited the improved passivation to an oxidation step prior to SIPOS deposition that formed an SiO₂ oxide layer between the SIPOS emitter and the substrate: “Of critical importance in achieving this performance level is the oxidation step (6). In omitting that one step the ‘emitter Gummel number’ figure of merit degrades by almost an order of magnitude.” EX1005, 1212, Table II (step 6).

Based on these results, Yablonovitch concluded that “crystalline silicon solar cells can be much more efficient than had been suspected.” EX1005, Abstract, 1213 (“This design would rely on superior heterojunction emitters to

⁸ J_o or J_{oe} refers to saturation current density and is a measure of the electron/hole recombination in solar cells. EX1003, ¶¶87, 93.

improve the voltage and on light trapping to improve the current in a thin device.”).

A Skilled Artisan would thus have been motivated to modify a solar cell with a homojunction-based diffused emitter, like Froitzheim, by replacing the diffused emitter with a SIPOS-based emitter including an interfacial oxide layer, as taught by Yablonovitch, because Yablonovitch explicitly reported that such solar cells exhibit improved performance in terms of saturation current and passivation. Indeed, aside from Yablonovitch, other prior art references also suggested that SIPOS emitters could provide “more than one percent absolute increase in efficiency for the solar cell” compared to diffused emitters like Froitzheim. EX1029, 2122; EX1003 ¶81.

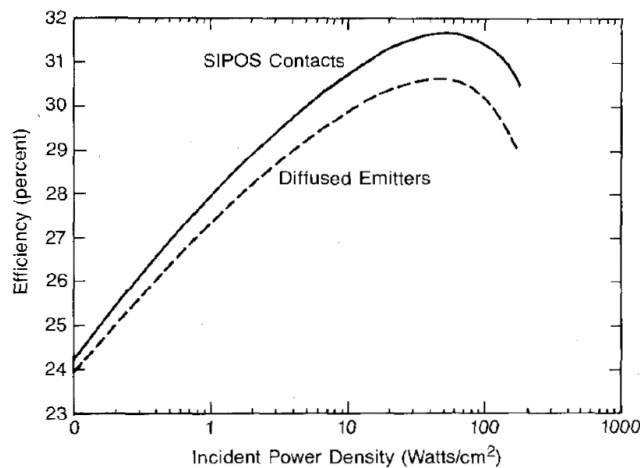


Fig. 9. A comparison of the projected efficiencies possible for a cell incorporating SIPOS emitters (solid curve), compared to projections for diffused emitters as used to date (dashed curve).

A Skilled Artisan would further have been motivated specifically to leave the emitter on the back side of the solar cell because Froitzheim disclosed that its

design “shows improved stability and good efficiency.” EX1008, ¶9. Indeed, a patent to Yablonovitch, U.S. 4,525,593, placed a SIPOS layer on the back of a solar cell. EX1011, Abstract (“At the rear of the cell is a high performance heterocontact made of SIPOS...”), 1:47-49. It was well known that back junction solar cells often led to higher solar cell efficiency than front junction cells. EX1003, ¶120. In the combination, Froitzheim’s modified emitter would continue to function as before, but with the expected additional improvement provided by the SIPOS emitter and interfacial oxide layer. EX1003, ¶119. And replacing the diffused emitter with the SIPOS emitter and interfacial oxide layer, as taught by Yablonovitch, merely substitutes one element for another already known in the field, yielding a predictable result. EX1003, ¶121. *See also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

B. Reasonable Expectation of Success

The Skilled Artisan would have considered the Froitzheim/Yablonovitch combination to be merely an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform (the emitter of Froitzheim continuing to act as an emitter, but modified to be of a SIPOS material with an interfacial oxide layer in between it and the substrate) and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). EX1003, ¶121-122.

Specifically, instead of introducing the boron dopant by diffusion at the substrate's rear side in Froitzheim, the Skilled Artisan would grow a thin SiO₂ oxide to form the interfacial layer followed by SIPOS deposition to form the p-type SIPOS layer on the oxide layer, at which point the wafer is heated and annealed as taught by Yablonovitch. EX1003, ¶122; EX1005, Table II (steps 6-11), 1212. The metallization could be performed as described by Froitzheim. EX1008, ¶¶27, 48-49. As Dr. Shea explained, it is well within the routine skill of the Skilled Artisan before 2009 to be able to optimize, process, and dope the front and backside of the solar cell differently, such as through masking and/or etching of one side or the other, which were known to the Skilled Artisan before 2009. EX1003, ¶122 (citing EX1032, EX1036, EX1044, and EX1045).

Combining Froitzheim/Yablonovitch as described here would have been well within the level of ordinary skill in the art. EX1003, ¶¶121-126. It would not have resulted in any unpredictable results and could have been accomplished with a reasonable expectation of success. *Id.* The combination would simply have been the execution of well-known prior art steps in solar cell fabrication to yield predictable results. *Id.* Likewise, substituting Froitzheim's in-substrate emitter with a SIPOS emitter and oxide layer on the substrate would be a simple substitution of one known element and corresponding fabrication steps for another to obtain predictable results. EX1003, ¶121-122. It would further constitute use of

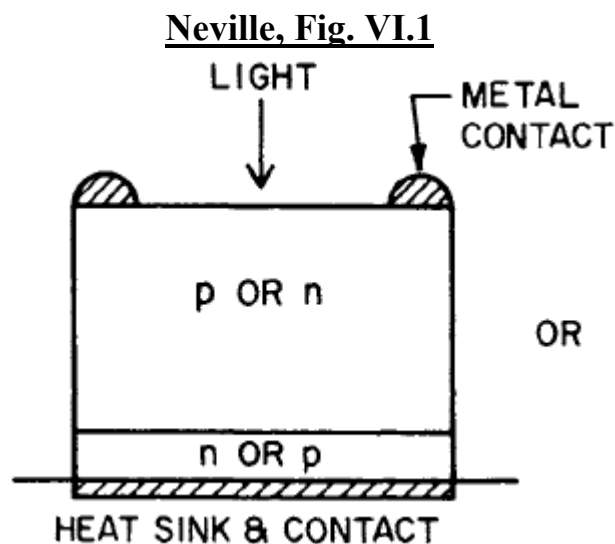
a known technique (depositing SIPOS emitters with an oxide layer) to improve similar devices (Froitzheim's solar cell) in the same way. *Id.* It is nothing more than applying a known technique to a known device ready for improvement to yield predictable results. *Id.*

Although Yablonovitch expressly discusses forming an n-type SIPOS on a p-type wafer, this would not prevent a Skilled Artisan from successfully combining the teachings of Yablonovitch and Froitzheim. EX1003, ¶¶123-125. Yablonovitch also noted that its p-type SIPOS was likewise “superior to that of a homojunction” diffused emitter. EX1005, 1211. In Yablonovitch's fabrication process, reversing the polarity of the SIPOS layer to be p-type would require no more than using a compound like diborane (B_2H_6) that would introduce a p-type dopant (B, boron), rather than phosphine (PH_3), which introduces an n-type dopant (P, phosphorus), during Yablonovitch's SIPOS deposition step. EX1005, Table II (step 7); EX1003, ¶123; EX1019, 528 (“As discussed in Section 12.2.6, a-Si can be doped n-type by mixing phosphine (PH_3) with the gas mixture or doped p-type by mixing diborane (B_2H_6)....”); EX1026, 450; EX1025, 198 (“The discovery that with suitable annealing treatments SIPOS films can be doped n- and p-type....”).

Moreover, it was well known in the art that the polarity (p-type versus n-type) of a back junction solar cell wafer and the emitter could be interchangeable. The interchangeability of the polarity of a solar cell was known and suggested for

years before the 074 Patent, as evidenced by Yablonovitch himself in Yablonovitch's patent. EX1011, 2:16-19 ("The solar cell of the present invention shall be illustrated and described by a cell with p doped crystalline silicon and n-doped SIPOS. *It is to be understood that the doping types may be interchanged.*").

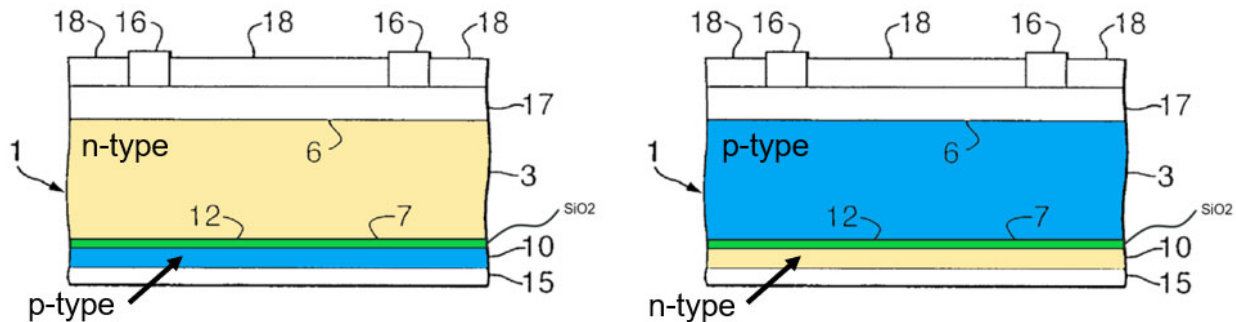
Froitzheim also disclosed that it was known in the art the polarity of the substrate and the emitter in solar cells could be reversed. EX1008, ¶7 ("Another alternative that has been considered is to reverse the doping of the base layer and the front side emitter layer...."). See also EX1009, 200, Fig. VI.1 (textbook chapter indicating that the substrate could be either n- or p-type, and that the rear emitter layer would then have the opposite polarity for back junction cells).



Thus, the polarity of Yablonovitch's SIPOS layer could be reversed (to be p-type) to conform with Froitzheim's n-type wafer in Fig. 1, or conversely, the

dopant type of Froitzheim's wafer could be reversed to be p-type to conform with Yablonovitch's n-type SIPOS.

Combinations of Yablonovitch and Froitzheim



C. Froitzheim and Yablonovitch Disclosed All Claimed Steps

1. Claim 1

a) [1.a] Preamble

Froitzheim and Yablonovitch both disclosed “*method[s] of fabricating a solar cell.*” *E.g.*, EX1005, Table II; EX1008, ¶¶38-51.

b) [1.b] Central Substrate

Claim 1 recites: “*providing a wafer as a central substrate.*” In Froitzheim, a “silicon body layer of n-type bulk doping, typically a wafer ... is provided.” EX1008, ¶39. Likewise, Yablonovitch starts with “silicon wafers,” which served as central substrates. EX1005, Table II. EX1003, ¶130.

Yablonovitch(EX1005), Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

c) [1.c] Interface Passivation Layer

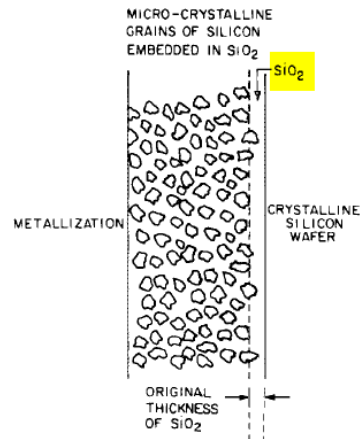
Claim 1 recites: “*depositing or growing at least one amorphous interface passivation layer over the substrate.*” Silicon oxide is an example of an interface passivation layer in the 074 Patent. *E.g.*, EX1001, 5:56-61, 5:66-6:4.

In the Froitzheim/Yablonovitch combination, a silicon oxide layer is formed on the substrate. Yablonovitch explicitly discloses an “oxidation step” that grows a layer of SiO_x (silicon oxide) over the silicon wafer. EX1005, 1212, Fig. 3, Table II. Silicon oxide formed by oxidizing a silicon substrate is generally amorphous. EX1021 (Tatsumura), 085212-1 (noting that the structure of SiO_2 thermally grown on crystalline silicon is amorphous); EX1003, ¶135. Yablonovitch teaches that this silicon oxide layer is “[o]f critical importance in achieving th[e] performance level” in reduced recombination (i.e., passivation) observed in Yablonovitch’s cells. EX1005, 1212.

Yablonovitch(EX1005), Table II and Fig. 3 (Excerpt)

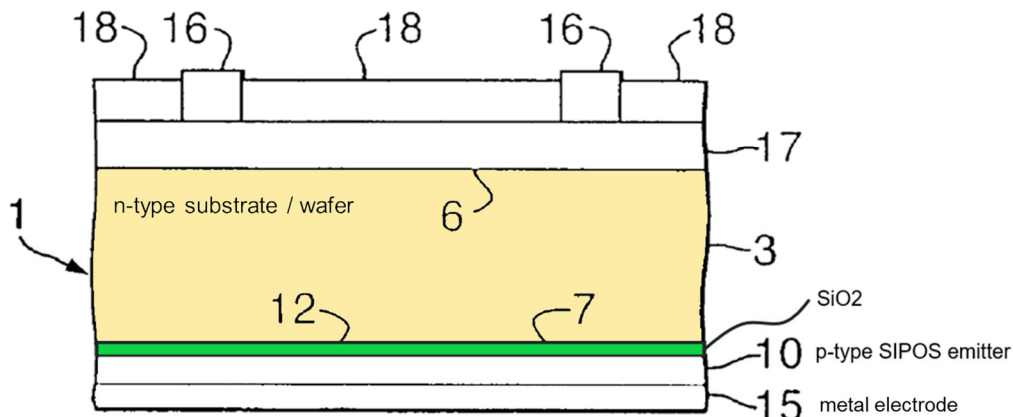
TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 $^{\circ}\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 $^{\circ}\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to 450 $^{\circ}\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.



Combination of Yablonovitch and Froitzheim

Fig.1.



d) [1.d] Conductive and Passivating Layer

Claim 1 recites: “*depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant.*” In the 074 Patent, a doped polysilicon layer is an example of the conductive and passivating layer (including polysilicon

with oxygen). EX1001, 5:49-55. In the art, “SIPOS films are chemically vapor-deposited polycrystalline-silicon doped with oxygen or nitrogen atoms.” EX1035, Abstract. Thus, the “*conductive and passivating layer*” of the 074 Patent can be a SIPOS layer.

In the Froitzheim/Yablonovitch combination, the backside diffused p-type emitter of Froitzheim is replaced with a doped SIPOS emitter, as taught by Yablonovitch. EX1003, ¶108-110. *See supra* §IX.A-B. Yablonovitch’s doped SIPOS emitter is both passivating and conductive. EX1005, 1211 (“The interface states between SIPOS and crystalline silicon (c-Si) seem to be passivated”), 1213 (“The individual contacts provide more than enough conductivity for majority-carrier electrons....”); *see also, e.g.*, EX1014, 885 (“(SIPOS) is widely used as a passivation layer....”); EX1022, 3:15-24 (discussing Yablonovitch and recognizing that SIPOS “may be doped to have high conductivity”); EX1003, ¶¶141-144.

In the combination, depositing the SIPOS layer follows the thermal oxidation step and replaces the boron diffusion step at the backside in Froitzheim. EX1003, ¶108-110, 139. Although Yablonovitch’s solar cell was illustrated with n+ SIPOS layers (comprising n-type dopant), Yablonovitch also disclosed p+ SIPOS layers (comprising p-type dopant) and taught that even p+ SIPOS layers were “superior to that of a homojunction.” EX1005, 1211.

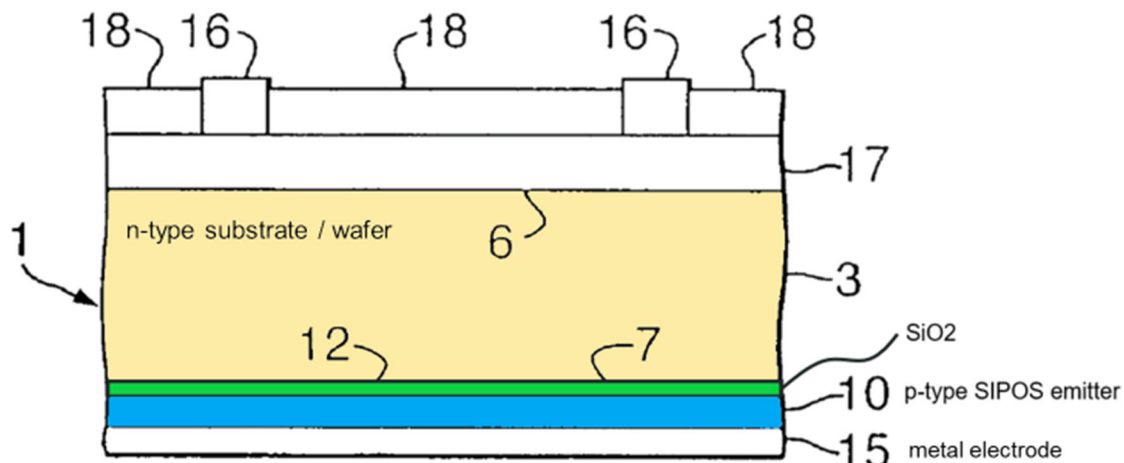
Yablonovitch, Table II

TABLE II. Processing sequence.

1. Thin silicon wafers to $50\text{ }\mu\text{m}$ in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to $650\text{ }^\circ\text{C}$ while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to $900\text{ }^\circ\text{C}$.
9. Anneal for 15 min.
10. Ramp furnace down to $450\text{ }^\circ\text{C}$.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Combination of Yablonovitch and Froitzheim

Fig. 1.



e) [1.e] Thermal Treatment

Claim 1 recites: “providing thermal treatment at a temperature of about $500\text{ }^\circ\text{C}$ or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from

the at least one conductive and passivating layer through the at least one interface passivation layer.”

The annealing step 9 in Table II of Yablonovitch is a thermal treatment at a temperature of 900°C and satisfies the claimed step. Yablonovitch explains that “[t]his step is necessary to precipitate microcrystalline silicon grains within the material” i.e., thus “crystallizing, at least in part,” the SIPOS layer. EX1005, 1212; EX1003, ¶¶148-150.

Yablonovitch, Table II

TABLE II. Processing sequence.

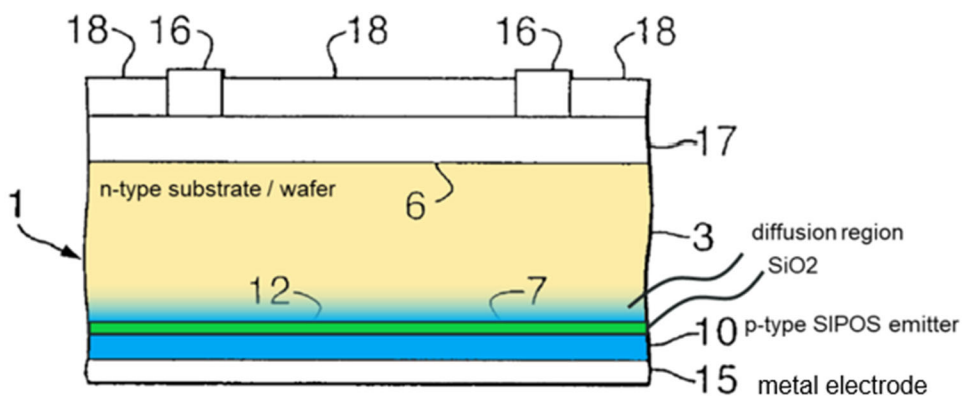
1. Thin silicon wafers to 50 μm in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N_2 .
5. Ramp up to 650 °C while maintaining N_2 purge.
6. Oxidize for 5 min with 100 ppm O_2 .
7. Deposit SIPOS from 1000 ppm SiH_4 , 50 ppm PH_3 , and 10 ppm O_2 .
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

Yablonovitch further explains that “during this step, the phosphorus [dopant] diffuses about 20-50 Å into the silicon wafer as measured by secondary ion mass spectrometry.” EX1005, 1212. Those skilled in the art would understand that this diffusion from the doped SIPOS layer into the substrate necessarily is through the silicon oxide layer because the oxide layer is in between SIPOS layer and substrate. EX1003, ¶151. *See also* EX1007 (Kwark II), 1123 (“emitters of type C

with no prediffusion were fabricated. These relied solely on outdiffusion from the in-situ doped SIPOS ... to provide sufficient surface doping concentration.”); EX1016 (Post), 1718 (“The second type of structure ... is a polysilicon emitter in which the n^+ dopant is diffused from the polysilicon into the underlying single-crystal silicon to form a very shallow emitter/base junction.”). Yablonovitch’s annealing step would also cause boron to diffuse into the wafer in the same manner. EX1003, ¶152; EX1036, Fig. 4 (depicting boron diffusion from polysilicon through oxide into substrate). Boron has greater diffusivity than phosphorus in silicon oxide and diffusivity also increases with thinner silicon oxide, as that used in Yablonovitch. EX1003, ¶152; EX1039, 994 §3.3, Fig. 8; EX1031, 172.

Combination of Yablonovitch and Froitzheim

Fig. 1.



f) [1.f] Metallization

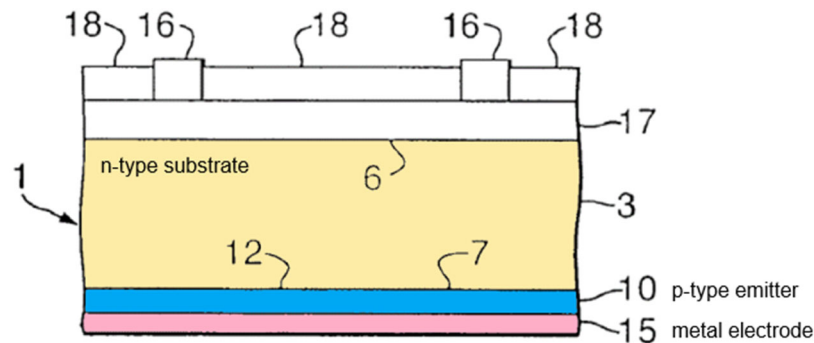
Claim 1 recites: “*providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

1. First Embodiment Combination

The Yablonovitch/Froitzheim combination satisfies the “*metallization*” limitation. Froitzheim discloses forming a “rearside contact [] arranged in electrical connection” with Froitzheim’s rear p-type emitter, which covers “substantially all” of the rear-side of the cell. EX1008, ¶27, Fig. 1. A Skilled Artisan would understand that Froitzheim’s metal contacts can be silver or aluminum. *Id.* ¶20; EX1003, ¶¶155-56.

Froitzheim, Fig. 1

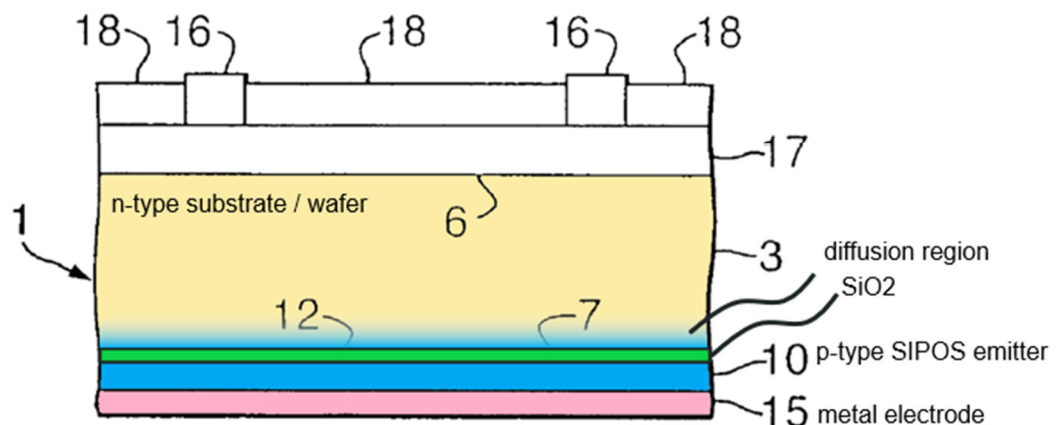
Fig. 1.



In Yablonoitch/Froitzheim combination, a metal electrode would likewise be provided covering the backside and directly contacting the SIPOS-emitter.

Combination of Yablonoitch and Froitzheim

Fig. 1.



Moreover, as discussed above, Yablonoitch discloses that the dopants in its SIPOS emitter diffuse through the interfacial oxide layer and into the substrate

upon heating. EX1005, 1212. Thus, the combination of Yablonovitch/Froitzheim would satisfy “*the dopant diffused through the at least one interface passivation layer.*”

Further, the combination of Yablonovitch/Froitzheim would also satisfy the “*shortened carrier flow paths*” limitation recited in the claim. EX1003, ¶¶160-164. According to the 074 Patent, for “[a] back junction cell with a full area back contact” like that in Fig. 5, “[t]he minority carriers (solid [red] lines) can use the shortest geometrical path to reach the rear p-type emitter 58” because “their transport within the emitter is vertical instead of mainly lateral.” EX1001, 4:60-5:11.

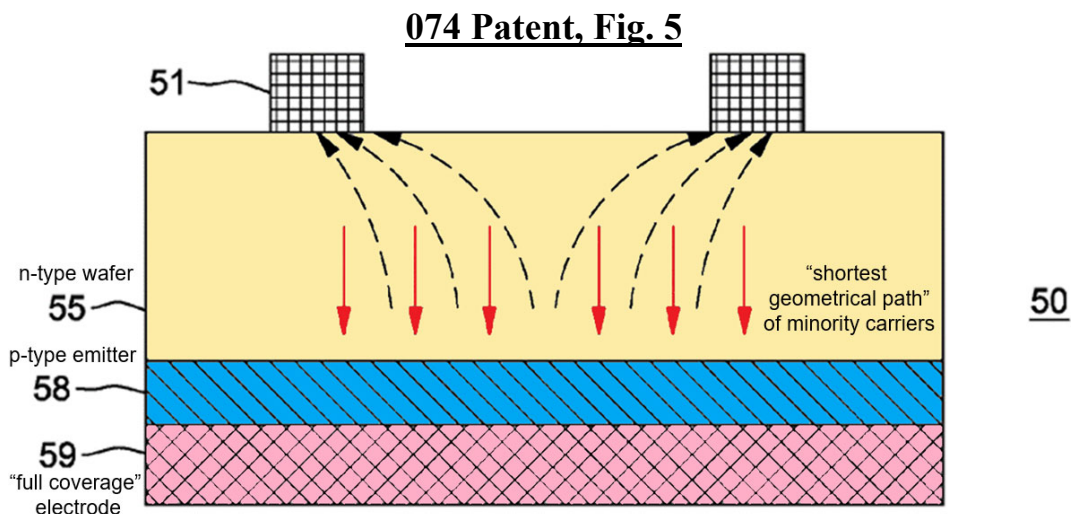


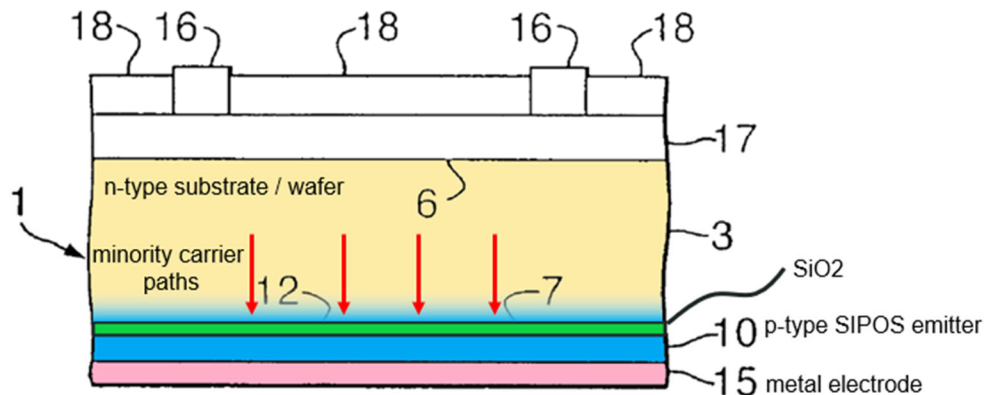
FIG. 5

In the proposed combination, an n-type wafer and a p-type SIPOS emitter form a backside p-n junction, and a rear-side electrode covers substantially all of

the back side of the cell, thus providing the shortest geometrical path for the minority carriers (shown in red below) in the same way as described in the solid line arrows of FIG. 5 of the 074 Patent. EX1003, ¶¶160-164.

First Combination of Yablonovitch and Froitzheim

Fig. 1.



2. Second Embodiment Combination

In its district court complaint, PO appears to take the position that localized metal contact that does not cover substantially all of the backside of Petitioner's accused solar cells nevertheless "provide metallization as electrodes" such that there are "shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer." EX1024 (Complaint), ¶¶79-81.

Under PO's allegation and infringement rationale in its complaint, Froitzheim and Yablonovitch also disclose the use of localized finger electrodes that would satisfy this claim limitation. Specifically, in Yablonovitch, the SIPOS

is “contacted with... a silver electrode,” denoted “Ag” in Figure 2 that does not cover the entire back surface. EX1005, 1212, Fig. 2.

Yablonovitch, Fig. 2

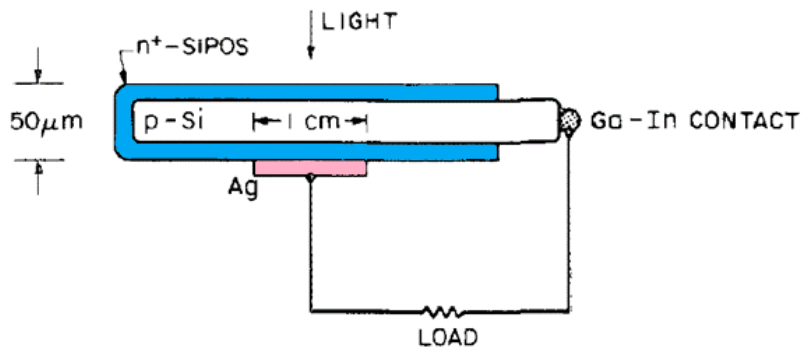


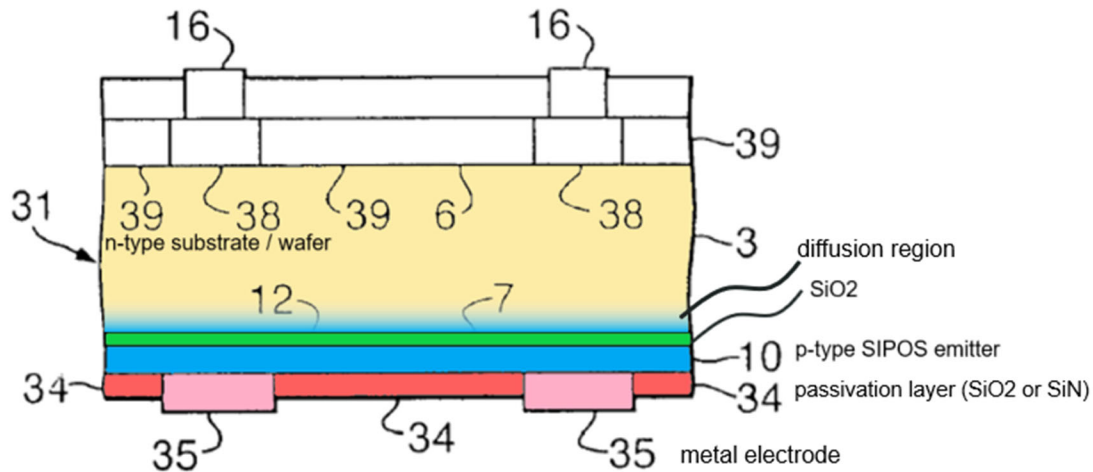
FIG. 2. Test configuration for the SIPOS : c-Si : SIPOS double heterostructure solar cells. In this design the fill factor was limited by the bulk resistance of the p-Si wafer itself.

Froitzheim also discloses another embodiment at Fig. 3 in which “the rear contacts 35 are arranged in a finger structure covering only part of the rear side.”⁹ EX1008, ¶33. Froitzheim teaches that the rear-side contacts can be formed by screen printing using a paste containing “silver particles.” EX1008, ¶¶48-49. Thus, under PO’s contention of infringement, Yablonovitch alone or in combination with Froitzheim FIG. 3 satisfies this limitation. EX1003, ¶¶165-170.

⁹ Froitzheim’s Figure 3 is otherwise the same as Figure 1 in relevant respects. EX1008, ¶¶33-34.

Second Combination of Yablonovitch and Froitzheim (Fig. 3)
According to Patent Owner's Allegations

Fig.3.



Specifically, PO's district court complaint explains that the "curved path between the electrodes and the substrate as represented by the dashed lines in Figure 5" of the 074 Patent represents "shortened" flow path. EX1024, ¶57.

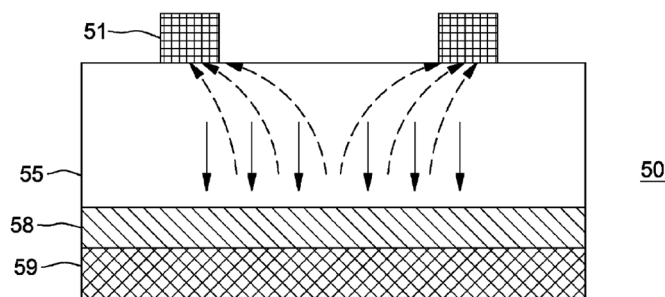


FIG. 5

And a shortening "similar in concept to that which is shown in Figure 5" occurs, according to PO, when "[t]he area where the dopant ... is incorporated into the interface passivation layer and ... the substrate makes the silicon in those areas more conductive and forms low resistance pathways through those layers along

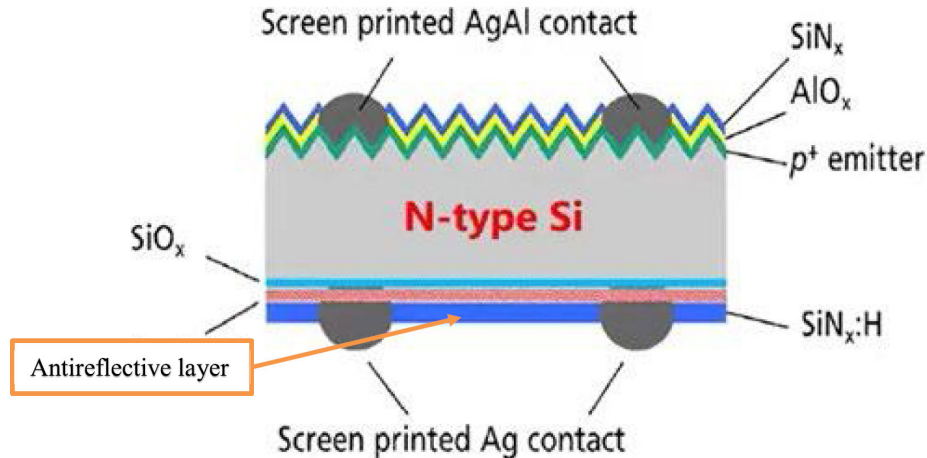
which electrons can more easily travel.” EX1024, ¶58. PO states that “the diffusion of dopant into these layers thus increases the conductivity of the solar cell near the back surface of the silicon substrate ... such that that its conductivity is more similar to the conductivity of the conductive and passivating layer.” *Id.* “As a result, [PO explains that] charges take a more direct route from the substrate toward the electrodes affixed to the back of the solar cell than they would otherwise without the diffusion of the dopant, similar in concept to that which is shown in Figure 5.” *Id.* PO further expands that the diffusion of the dopant through the interface passivation layer “result[s] in higher conductivity near the back surface of the substrate compared to an assembly that does not have dopant diffused through the interface passivation layer. This causes charge flow paths to curve toward the electrodes, shortening them as illustrated in concept in Figure 5 of the 074 Patent.” *Id.* ¶81. Thus, assuming PO’s contention is true, the combination of Yabonovitch with FIG. 3 of Froitzheim similarly satisfies this limitation of claim 1 because the dopant diffuses from the SIPOS into the substrate through the interfacial oxide layer, creating higher conductivity in the back surface of the substrate, thus resulting in this shortened, curve flow path similar to concept to what occurs in the front portion of FIG. 5 of the 074 Patent, based on PO’s explanation. EX1003, ¶¶165-170.

2. Claim 2 – Antireflective Layer

Claim 2 depends from claim 1 and recites: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

PO’s district court complaint points to a SiN_x (silicon nitride) layer with a silver electrode screen printed through it as the claimed “antireflective layer” in Petitioner’s accused device:

The manufacture of Canadian Solar’s TOPCon solar cells includes depositing at least one antireflective layer, a silicon nitride antireflective coating (the blue “ $\text{SiN}_x\text{:H}$ ” layer in the image below), on the back of the solar cell.... [EX1024, ¶82.]



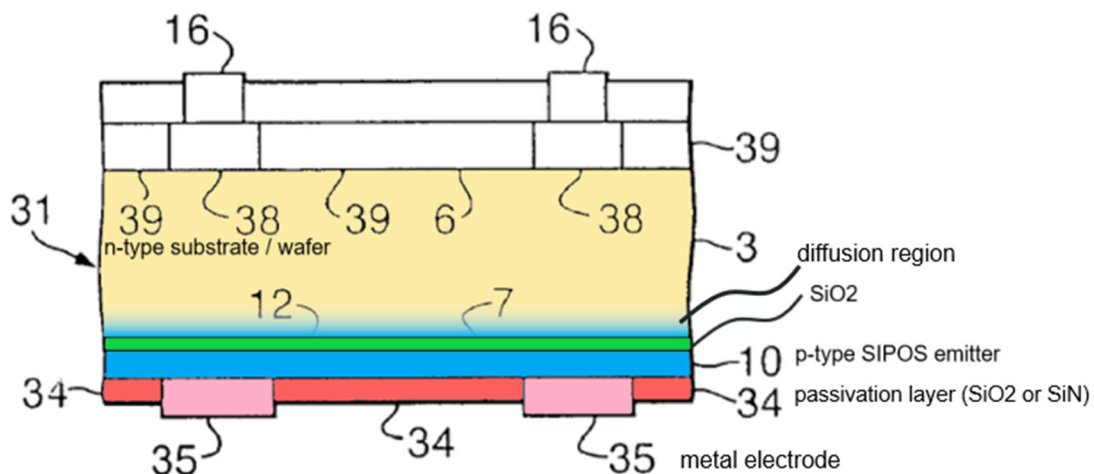
Based on PO’s contention, Froitzheim’s Fig. 3 combined with Yablonovitch would satisfy claim 2. EX1003, ¶¶172-177. Layer 34 in Froitzheim Fig. 3 is identified as a passivation layer “for which the same type of layers can be used as for the front side.” EX1008, ¶33. Froitzheim expressly discloses silicon nitride

(SiNx) as one possible material for this passivating layer 34. EX1008, ¶¶19, 30, 33. Silicon nitride is the same material layer in CSI's accused device that PO is accusing satisfies claim 2 in its complaint. EX1024, ¶82.

Froitzheim also expressly discloses that silicon dioxide (SiO₂) is one of the possible passivation materials on the front side, and thus it could also be used for layer 34 on the back side. EX1008, ¶¶19, 30, 33. The 074 Patent likewise lists silicon oxide as an one example of an antireflection film with a low refractive index. EX1001, 6:47-50.

Second Combination of Yablonovitch and Froitzheim (Fig. 3)
According to Patent Owner's Allegations

Fig.3.



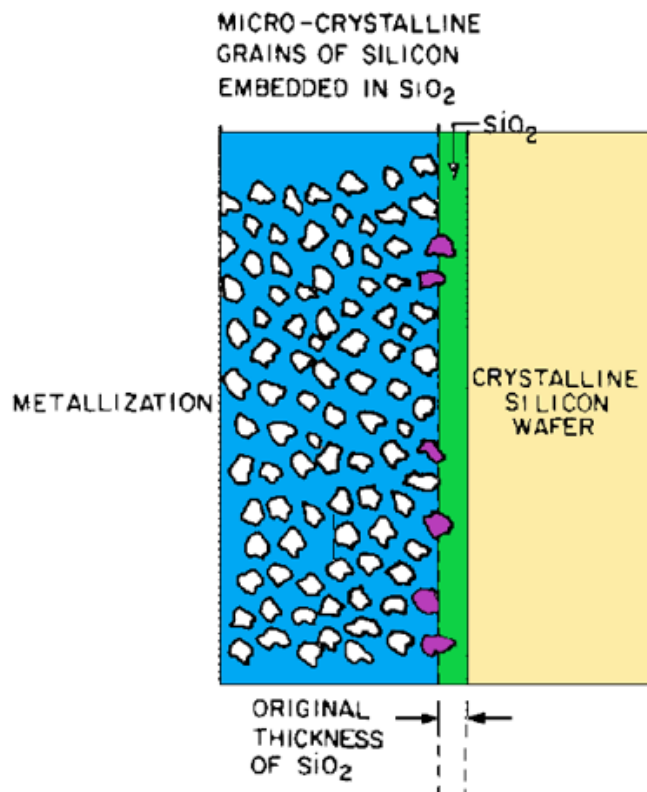
3. Claim 4 - Perforation

Claim 4 depends from claim 1 and recites: “*wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.*”

Yablonovitch discloses depositing and thermally treating a SIPOS layer by annealing it at 900°C for fifteen minutes. *See supra*, §IX.C.1.d (claim [1.d]).

Yablonovitch’s annealing step results in “a microcrystalline structure with a significant surface density of individual [silicon] grains protruding into the thin oxide layer,” as depicted in Fig. 3 below. EX1005, 1212-13, Fig. 3 (emphasis added).

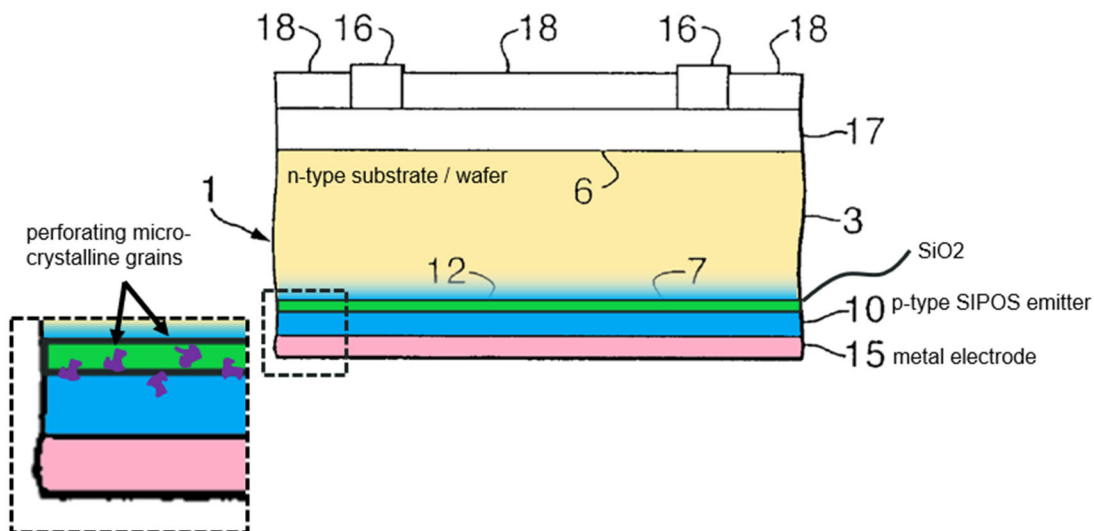
Yablonovitch, Fig. 3 (excerpt)



Moreover, Yablonoitch teaches that “electrical contact is via thin spots and pinholes in the SiO_2 ” created “by [the] individual microcrystalline grains which occasionally protrude into the oxide.” *Id.* That is, these holes or perforations in the SiO_2 layer allow for the adjacent SIPOS layer to make electrical contact with the substrate through the protruding microcrystalline grains. EX1003, ¶¶181-182. Thus, the proposed combination of Yablonoitch and Froitzheim discloses that thermal treatment results in perforation of the SiO_2 layer to enable carrier transport, as illustrated below.

Proposed Combination of Yablonoitch and Froitzheim

Fig.1.



4. Claim 5 - Crystallization

Claim 4 depends from claim 1 and recites: “*wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing*

compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.”

Yablonovitch’s SIPOS layer is amorphous initially, and crystallizes during subsequent thermal treatment (annealing). EX1003, ¶¶185-186. In particular, Yablonovitch discloses depositing “a disordered [i.e., amorphous] semiconductor heterojunction material, SIPOS (originally named semi-insulating polycrystalline silicon)” at 650°C. EX1005, 1211 (emphasis added), Table II (steps 5-7). SIPOS deposited at 650°C is amorphous. EX1025 (Kwark III), 200. The annealing step “precipitate[s] microcrystalline silicon grains within the material.” EX1005, 1211, 1213, Fig. 3 (describing the microcrystalline grains of silicon that form as a result of annealing). Thus, Yablonovitch’s annealing step crystallizes and causes microcrystalline grains of polycrystalline silicon to form as a SIPOS layer. EX1003, ¶¶185-186. *See also* EX1013, 355 (“The results shown in fig. 1 indicate a predominantly amorphous structure for the as-deposited [SIPOS] layers with a very low density of Si microcrystallites ... whereas the crystalline portion and the mean value of the crystallite increase with increasing annealing temperature.”).

5. Claim 6 – Transmissivity

Claim 6 depends from claim 1 and recites: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at*

least one conductive and passivating layer and [b] increases the optical transmissivity.” The combination of Yablonovitch and Froitzheim discloses part [a] of claim 6, *see supra* §IX.C.4 (claim 5).

Annealing Yablonovitch’s SIPOS layer to form microcrystalline silicon grains further increases optical transmissivity. Yablonovitch disclosed depositing the SIPOS layer at 650°C and then annealing the SIPOS layer at 900°C to form the crystalline grains. EX1005, Table II , 1212-13. The particular chemical mixture Yablonovitch uses to form the SIPOS layer results in “5% oxygen incorporation.” EX1005, 1213.

TABLE II. Processing sequence.

1. Thin silicon wafers to 50 μ m in aqueous KOH.
2. Getter in an oxidation furnace containing substantial chlorine.
3. Strip gettering oxide in HF acid.
4. Immediately load into cold APCVD furnace while purging with N ₂ .
5. Ramp up to 650 °C while maintaining N ₂ purge.
6. Oxidize for 5 min with 100 ppm O ₂ .
7. Deposit SIPOS from 1000 ppm SiH ₄ , 50 ppm PH ₃ , and 10 ppm O ₂ .
8. Ramp furnace to 900 °C.
9. Anneal for 15 min.
10. Ramp furnace down to 450 °C.
11. Anneal in forming gas for 2 h.
12. Pull wafers from cold furnace.

SIPOS annealed at 900°C with 5% oxygen is more transmissive than SIPOS as-deposited at 650°C. For example, Pan et al. investigated the “optical absorption characteristic of SIPOS.” EX1015 (“Pan”), 589 §1. In the study Pan prepared “SIPOS films deposited at 650°C,” and observed that “[a]nnealing at different temperatures has modified the optical absorption of the films.” *Id.*, 589-90 §§2.1,

3. The relationship between annealing temperature and optical absorption for SIPOS films with 8% oxygen content is graphed in Figure 4 of Pan, reproduced with annotations below. *Id.*, 590-91 §3, Fig. 4. As shown, the optical absorption was greater for the as-deposited SIPOS films than for films annealed at 900°C.

Pan, Fig. 4

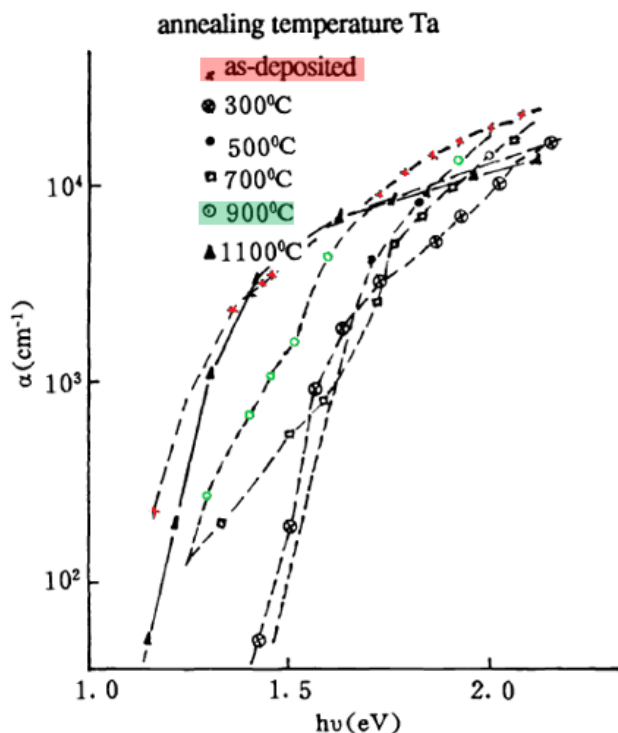


Fig. 4 Changes in optical absorption of SIPOS films (8 at.%) with annealing temperature T_a .

Optical absorption is the inverse of transmissivity—the more light that is absorbed by a SIPOS layer, the less light can be transmitted through the layer.

EX1003, ¶191. Optical transmission increases when SIPOS films are annealed, and it increases with increasing annealing temperature. *Id.* (citing EX1014). The

annealed SIPOS layer of Yablonovitch, therefore, has greater optical transmissivity than the as-deposited SIPOS layer.

6. Claim 7 – Dopant Activation

Claim 7 depends from claim 1 and recites: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein the thermal treatment activates doping atoms in the compound.*” The combination of Yablonovitch and Froitzheim discloses part [a] of claim 7, *see supra* §IX.C.4 (claim 5). As to part [b] of claim 7, Yablonovitch further taught that the annealing process “activate[s] the phosphorus dopant” in the SIPOS layer. EX1005, 1212. Annealing activates boron dopants in p-type SIPOS in the same way. EX1003, ¶196; EX1018, 479-480; EX1001, 16:16 (“Donors or acceptors get activated” during crystallization).

7. Claim 8 – PN Junction

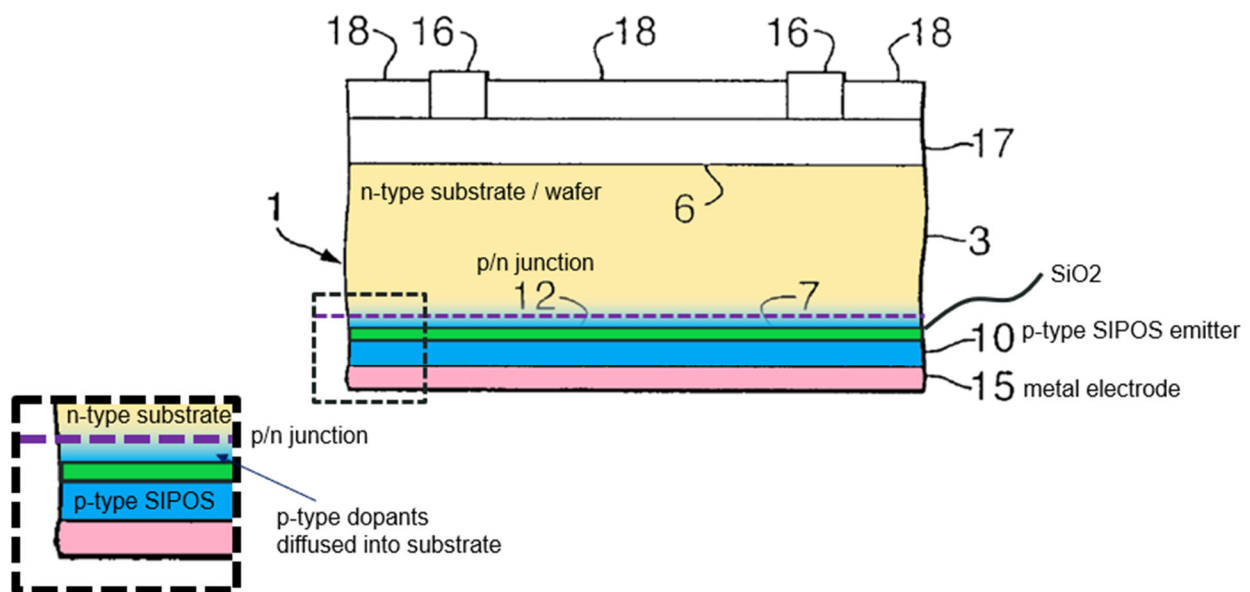
Claim 8 depends from claim 1 and recites: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.*” The combination of Yablonovitch and Froitzheim discloses part [a] of claim 8, *see supra* §IX.C.4 (claim 5).

As to part [b] of claim 8, Yablonovitch's annealing step diffuses n-type dopants (phosphorous) from the SIPOS layer through the SiO₂ layer "about 20-50 Å into the silicon wafer". EX1005, 1212. The same result would occur when diffusing p-type dopants (boron) during the annealing of a p-type SIPOS layer. EX1003, ¶¶152, 200; EX1039, 994 §3.3, Fig. 8; EX1036, Fig. 4; EX1031, 712 (Fig. 9).

Because the proposed combination of Yablonovitch and Froitzheim has an n-type substrate with a p-type SIPOS emitter layer (or vice versa), Yablonovitch's diffusion step results in the formation of a p-n junction. *See* EX1008, ¶¶25 ("At the rear side 7... a p/n-junction 12 with the body layer is formed."), 32, 68.

Proposed Combination of Yablonovitch and Froitzheim

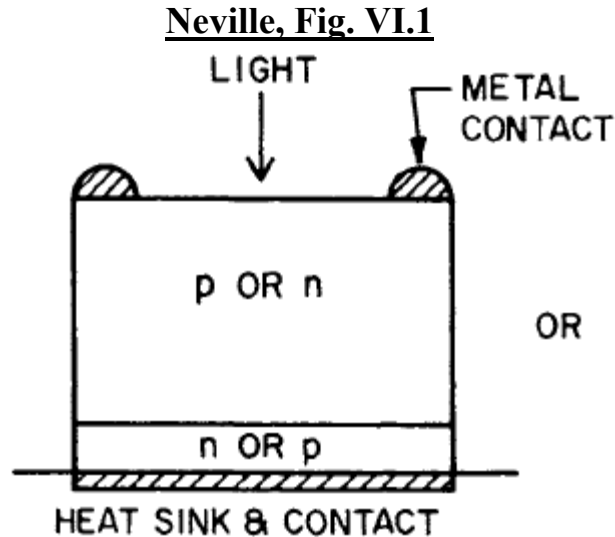
Fig.1.



X. GROUND II: CLAIMS 1, 2, AND 4-8 ARE UNPATENTABLE OVER FROITZHEIM, NEVILLE, YABLONOVITCH

As explained above in the Ground I combination of Froitzheim and Yablonovitch, the Skilled Artisan would understand that the polarity of the emitter layer and substrate in a back junction cell could be interchanged. *See* §IX.A-B. To the extent PO may argue that Yablonovitch teaches only use of n-type SIPOS layers, Claims 1-8 would still be obvious based on the combination of Froitzheim, Neville, and Yablonovitch.

Ground II is otherwise identical to Ground I, except that instead of using the n-type substrate in Froitzheim, the Skilled Artisan would replace it with a p-type substrate, as it is interchangeable as taught by Neville, Fig. VI.1. EX1003, ¶¶201-205; EX1009, 199, Fig. VI.1. *See ACCO Brands Corp. v. Fellowes, Inc.*, 813 F.3d 1361, 1367 (Fed. Cir. 2016) (when faced with only two known design permutations, it would be obvious for skilled artisan to make both); *Vanda Pharm. v. Teva Pharm. Inc.*, No. 2023-1247, 2023 WL 3335538, *5 (Fed. Cir. May 10, 2023) (same), *cert. denied*, 144 S. Ct. 1393 (2024).



This way, the Skilled Artisan can directly use the n-type SIPOS of Yablonovitch to replace the diffused in-substrate emitter in the back junction cell. EX1003, ¶¶124-126, 203. The Skilled Artisan would be motivated to make such a replacement because Yablonovitch expressly taught that the n-type SIPOS layer performs better than the p-type SIPOS layer, producing much lower J_0 . The use of a p-type substrate is well within the skill of the Skilled Artisan because p-type silicon substrates were widely used before 2008. EX1003, 203. Thus, the Skilled Artisan would reasonably expect success for such combination. EX1003, ¶¶124-126, 203-204.

XI. GROUND III: CLAIMS 1-8 ARE UNPATENTABLE OVER FROITZHEIM AND KWARK

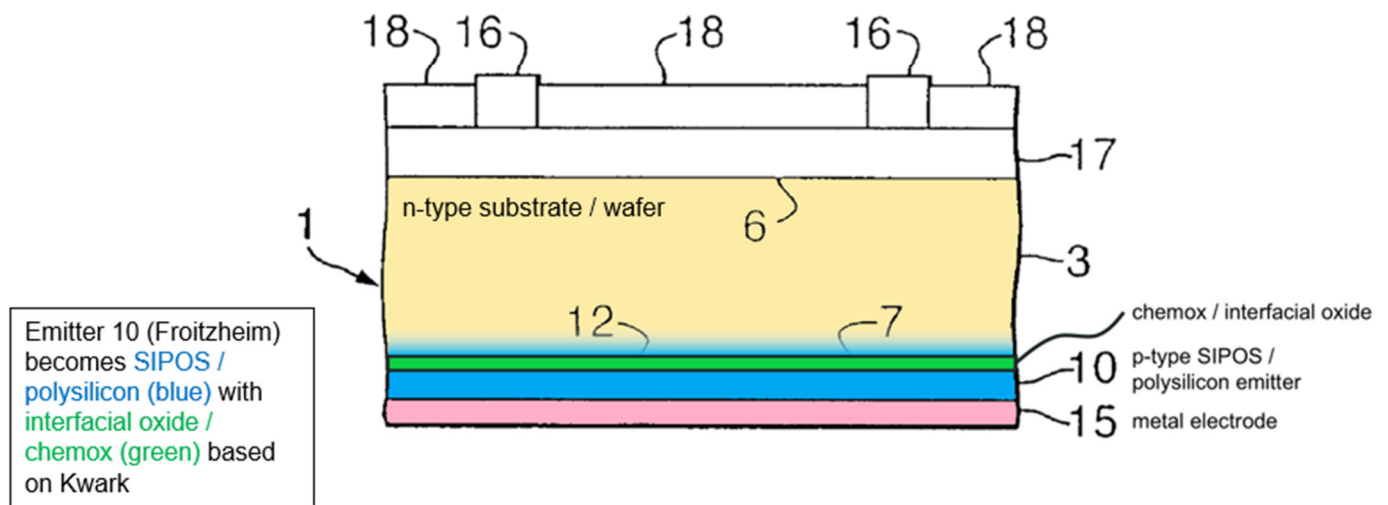
The combination Froitzheim and Kwark would have rendered Claims 1-8 obvious and unpatentable. The combination of Froitzheim and Kwark is similar to the Ground I, except that Kwark, instead of Yablonovitch, supplies the elements

for forming the SIPOS/polysilicon emitter and the oxide layer in between.

EX1003, ¶¶222-225.

Combination of Kwark and Froitzheim¹⁰

Fig.1.



A. Motivation to Modify Froitzheim with Kwark

Froitzheim and Kwark are analogous art because each is in the same field of endeavor—solar cell design. EX1003, ¶226. Kwark states that the incorporation of these films “translates into potential improvements of energy conversion efficiency

¹⁰ The “n-type” and “p-type” labels in the figure are merely illustrative. As discussed below, the dopant types of the substrate and emitter are interchangeable.

for solar cells.”¹¹ EX1006, 742. Thus, each reference is reasonably pertinent to the problems of solar cell efficiency. EX1003, ¶226; EX1008, Abstract, ¶¶1, 9; EX1006, 742.

The Skilled Artisan would have been motivated to modify Froitzheim’s emitter to be a polysilicon emitter with an oxide layer because Kwark taught and suggested that this modification would be an improvement transferable to solar cells. EX1003, ¶¶227-232. Kwark provided *J₀* data comparing polysilicon emitters with and without chemox, and against conventional diffused emitter (identified as “Al contact” below), and showed that SIPOS/polysilicon emitters result in much lower *J₀* than that of conventional diffused emitters (i.e., the “Al contact” control). EX1006, 745, Figs. 4-5.

¹¹ To the extent it is argued Kwark is directed to a bipolar transistor, a Skilled Artisan would still have looked to it when designing solar cells, as was commonly done in the art. EX1003, ¶¶227-228; EX1020, 363; EX1038, 497; EX1012, 245; EX1028, 597.

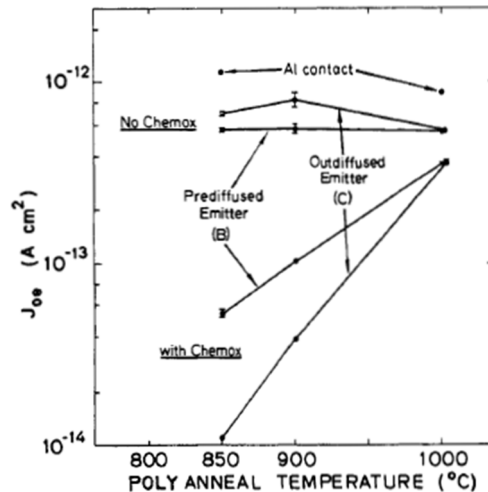


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

In replacing Froitzheim’s diffused emitter layer with a polysilicon layer, the Skilled Artisan would also have been motivated to form an oxide layer in between the polysilicon and substrate, as taught by Kwark, because of the beneficial effects of much lowered J_0 with the presence of the chemox.

Other references before 2008 similarly suggested replacing an in-substrate diffused emitter (like in Froitzheim) with a polysilicon emitter with interfacial oxide layer because of the benefits of a polysilicon emitter and interfacial oxide layer. EX1012, 245 (“cell performance can be improved if the diffused-emitter is replaced with the polysilicon emitter”); EX1003, ¶233. Although Kwark discloses an n-type polysilicon layer, the Skilled Artisan would have understood that a p-type SIPOS/polysilicon layer could also be used, as taught e.g., by Yablonovitch, Yablonovitch’s patent (discussed in Section IX.B above) and others. EX1003,

¶232; EX1012, 248 (Figures 4 and 5 showing low J_0 for both n-type and p-type polysilicon layers); EX1007, 1121 (“N-type and p-type conduction can be obtained at low oxygen concentrations by doping with phosphorus and boron.”).

Indeed, by February 2008, more than one year before the 074 Patent provisional application, Cousins filed a patent application¹² combining these teachings and disclosed a solar cell with “an N-type silicon substrate 101” and “a backside junction formed by a P-type doped polysilicon emitter 108,” formed directly on “a tunnel oxide layer 107.” EX1032, 2:28-31, 2:57-62. Cousins touted this solar cell configuration as “relatively efficient and cost-effective,” particularly for “power plants and other applications where power generation is the main concern.” *Id.*, 1:34-42. Cousins is thus additional evidence that the Skilled Artisan would have been motivated to combine Froitzheim and Kwark, and did in fact do so, to arrive at the proposed combination described above.

B. Reasonable Expectation of Success

The Skilled Artisan would have considered the Froitzheim/Kwark combination to be merely an arrangement of old method steps with each performing the same function it had been known to perform (the emitter of

¹² Cousins issued on July 17, 2012 from an application filed February 20, 2008 and is thus prior art under 35 U.S.C. §102(e). EX1032, face.

Froitzheim continuing to act as an emitter, but modified to be polysilicon with an interfacial oxide) and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). EX1003, ¶234-235.

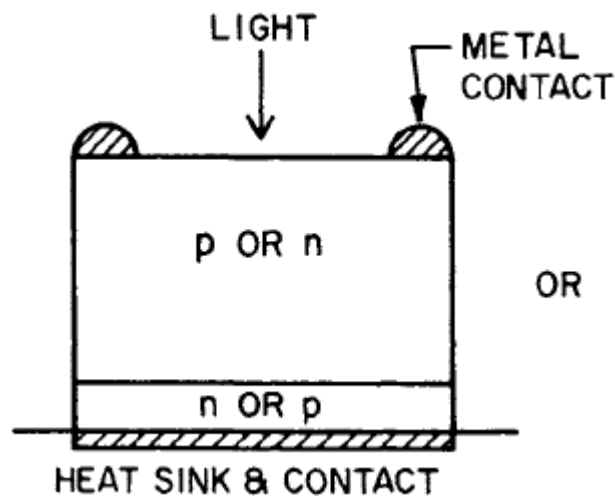
Specifically, instead of introducing the boron dopant by diffusion at the rear side of the substrate in Froitzheim, the Skilled Artisan would grow a chemox followed by polysilicon deposition to form a p-type polysilicon emitter layer on the oxide layer, at which point the wafer is annealed. EX1003, ¶235; EX1006, 742-43. The metallization as described by Froitzheim could then be used to form the metal electrodes. EX1008, ¶¶27, 48-49; EX1003, ¶233, 268-69.

Combining Froitzheim/Kwark as described here would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. EX1003, ¶¶235-240. The combination would simply have been the combination of prior art elements according to known methods to yield predictable results. *Id.* Likewise, substituting Froitzheim's in-substrate diffused emitter with a polysilicon emitter and oxide layer would be simple substitution of one known element for another to obtain predictable results. *Id.* It would further constitute use of a known technique (polysilicon emitters with an oxide layer) to improve similar devices (Froitzheim's solar cell) in the same way. *Id.* It would also constitute applying a known

technique to a known device ready for improvement to yield predictable results.

Id.

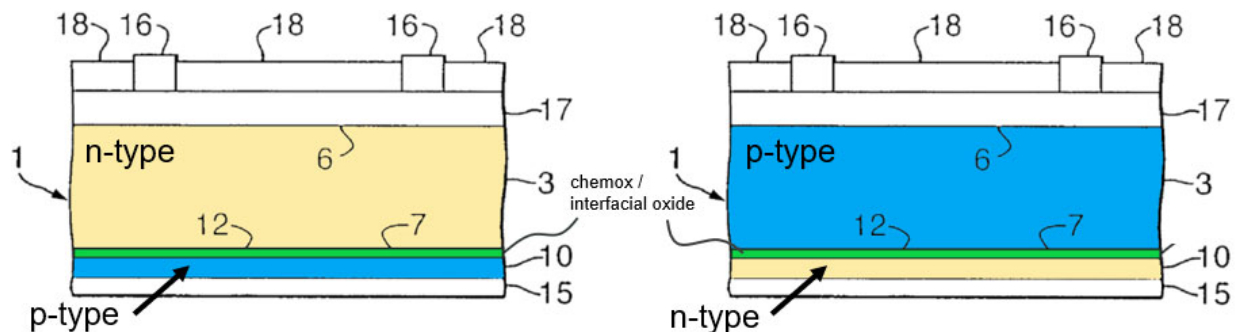
Although Kwark discusses the method steps for an n-type polysilicon on a p-type wafer, this would not prevent a Skilled Artisan from successfully combining the teachings of Kwark and Froitzheim. EX1003, ¶232-233. For one thing, Cousins obtained a patent (filed more than one year before the 074 Patent provisional application) to such a combination of an n-type wafer with a p-type polysilicon emitter. EX1032, 2:28-31, 2:58-58. And it was well known in the art that the polarity (p-type versus n-type) of a back junction solar cell wafer and emitter were interchangeable, as shown in the image below from Neville in 1995. EX1009, 200, Fig. VI.1.



Thus, the Skilled Artisan would understand that the polarity of Kwark's SIPOS/polysilicon layer could be reversed (to be p-type) to conform with Froitzheim's n-type wafer in Fig. 1, or vice versa. Reversing the polarity of the

polysilicon layer to be p-type would require no more than using a compound like diborane (B_2H_6) that would introduce a p-type dopant (boron), rather than phosphine (PH_3), during Kwark's polysilicon *in situ* deposition step. EX1003, ¶237; *see also* EX1019, 528; EX1026, 450.

Combinations of Kwark and Froitzheim



C. Froitzheim and Kwark Disclosed All Elements

1. Claim 1

a) [1.a] Preamble

Froitzheim discloses “a method of fabricating a solar cell.” *E.g.*, EX1008, ¶38, Fig. 1.

b) [1.b] Central Substrate

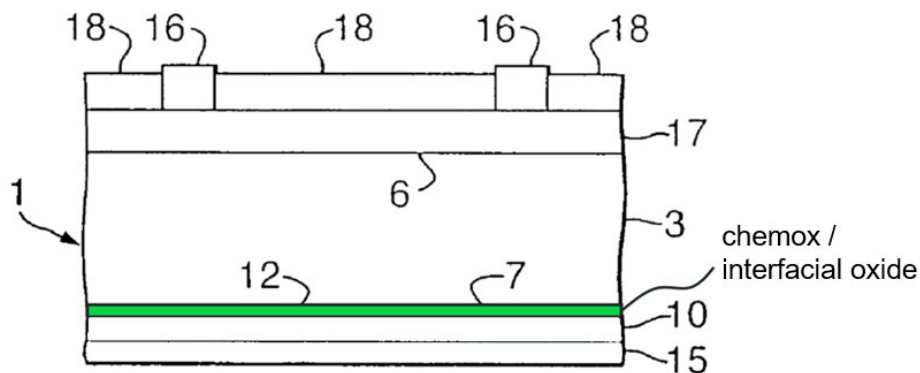
Both Froitzheim and Kwark disclose “providing a wafer as a central substrate.” In Froitzheim, a “silicon body layer of n-type bulk doping, typically a wafer ... is provided.” EX1008, ¶39. Likewise, Kwark's method starts with “wafer[s],” which served as central substrates. EX1006, 743; EX1003, ¶244-245.

c) [1.c] Interface Passivation Layer

Claim 1 next recites: “*depositing or growing at least one amorphous interface passivation layer over the substrate.*” Kwark discloses “chemically grow[ing]” a silicon oxide layer coined “chemox,” over the substrate via a RCA process. EX1006, 742-43. EX1003, ¶¶248-252. This chemox is grown before the deposition of the polysilicon emitter layer. *Id.* Such an oxide would be amorphous and passivating. EX1021, 085212-1; EX1003, ¶¶250-252.

Combination of Kwark and Froitzheim

Fig.1.



Kwark also satisfies this step with the deposition of SIPOS emitter without a separate step of growing the chemox, as discussed in more detail with respect to Claim 3 below.

d) [1.d] Conductive and Passivating Layer

Claim 1 recites: “*depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant.*”

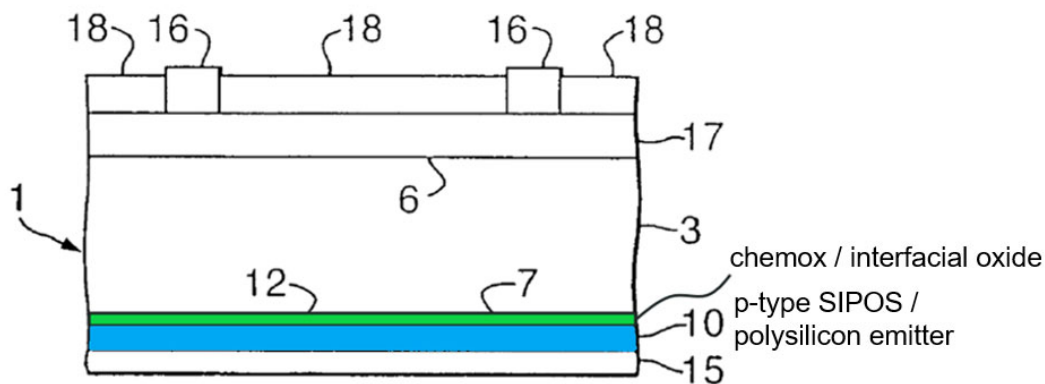
In the Froitzheim/Kwark combination, the backside diffused p-type emitter of Froitzheim is replaced with a polysilicon emitter deposited on the chemox, as taught by Kwark. EX1003, ¶¶223, 255-256. The polysilicon emitter in Kwark is also in-situ doped with a dopant. EX1003, ¶255; EX1006, 743. According to the 074 Patent, a doped polysilicon layer is an example of the conductive and passivating layer. EX1001, 5:49-55.

Thus, in the combination of Froitzheim and Kwark, forming the polysilicon layer with the chemox, as taught by Kwark, replaces the boron diffusion in Froitzheim. EX1006, 742-43; EX1003, ¶235. As discussed in §XI.B, the Skilled Artisan would be able to dope the polysilicon layer with p-type dopant to replace the p-type emitter of Froitzheim. EX1009, 200, Fig. VI.1; EX1032, 2:28-31, 2:58-58. It is well within the skill of the Skilled Artisan to process and dope the front and back side of the solar cell differently using well known techniques. EX1003, ¶235.

Kwark also satisfies this step with the deposition of doped SIPOS emitter without a separate step of growing the chemox, as discussed in more detail with respect to Claim 3 below.

Combination of Kwark and Froitzheim

Fig. 1.



e) [1.e] Thermal Treatment

Claim 1 recites: “*providing thermal treatment at a temperature of about 500°C or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer.*”

The post-deposition anneal temperatures in Kwark are all above 500°C. *See, e.g., EX1006, Figs. 4-6 (900-1000°C).* Kwark’s annealing/thermal treatment step also “*crystallizes, at least in part*” Kwark’s polysilicon emitters, as explained by in

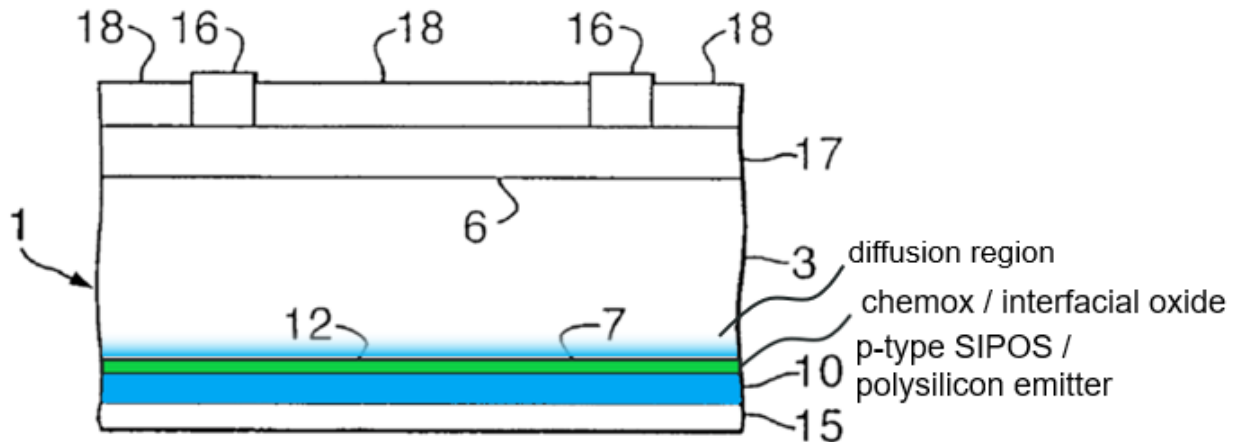
the legend of Kwark's Fig. 3: "after annealing, the 'oxide-like' regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites."

EX1006, Fig. 3; *see also* EX1007, 1121 ("[d]uring annealing it has been found that the [SIPOS] film morphology changes. Si precipitates into small grains of crystalline Si...."). Polysilicon films, like SIPOS films, are amorphous when deposited and crystallize upon heating at the temperature reported in Kwark. EX1018, 499-501; EX1026, 160-61; EX1003, ¶¶262-263.

Further, Kwark also discloses that the thermal treatment diffuses dopants from the in-situ doped SIPOS/polysilicon through the oxide layer and into the silicon wafer substrate. This is referred to in Kwark as the "outdiffused emitter (c)." EX1003, 264-265; EX1006, 743 ("emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction."); EX1007 (Kwark II), 1123 ("emitters of type c with no prediffusion were fabricated. These relied solely on outdiffusion from the in-situ doped SIPOS or poly-silicon to provide sufficient surface doping concentration"). This outdiffusion increases with increasing annealing temperature. EX1006, 743; EX1003, ¶264.

Combination of Froitzheim and Kwark

Fig. 1.



f) [1.f] Metallization

Claim 1 next recites: “*providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.*”

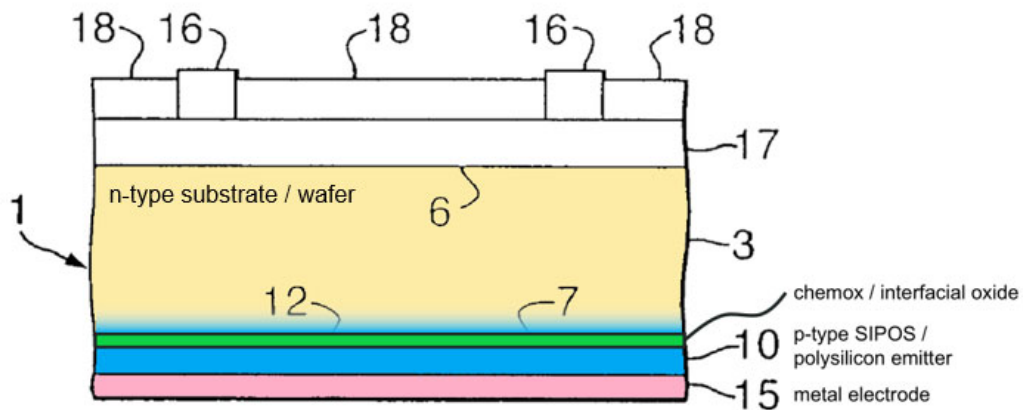
For the same reason discussed in §IX.C.1.f for the Froitzheim/Yablonoitch combination, the Froitzheim/Kwark combination satisfies this metallization step including the dopant diffusion and “shortened charge carrier flow paths” requirements, either using the combination of Froitzheim FIG. 1 with Kwark, or

Froitzheim FIG. 3 with Kwark (based on PO's contention in the district court).

EX1003, ¶¶268-275.

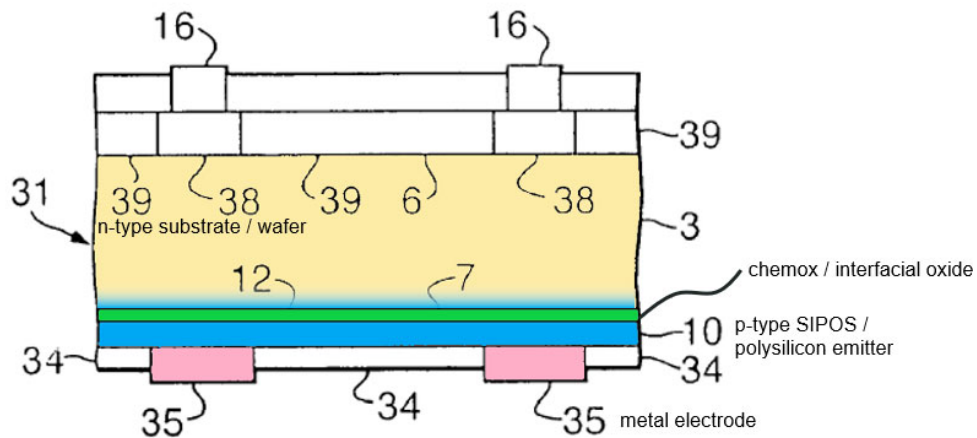
Combination of Kwark and Froitzheim

Fig.1.



Second Combination of Kwark and Froitzheim (Fig. 3)
According to Patent Owner's Allegations

Fig.3.

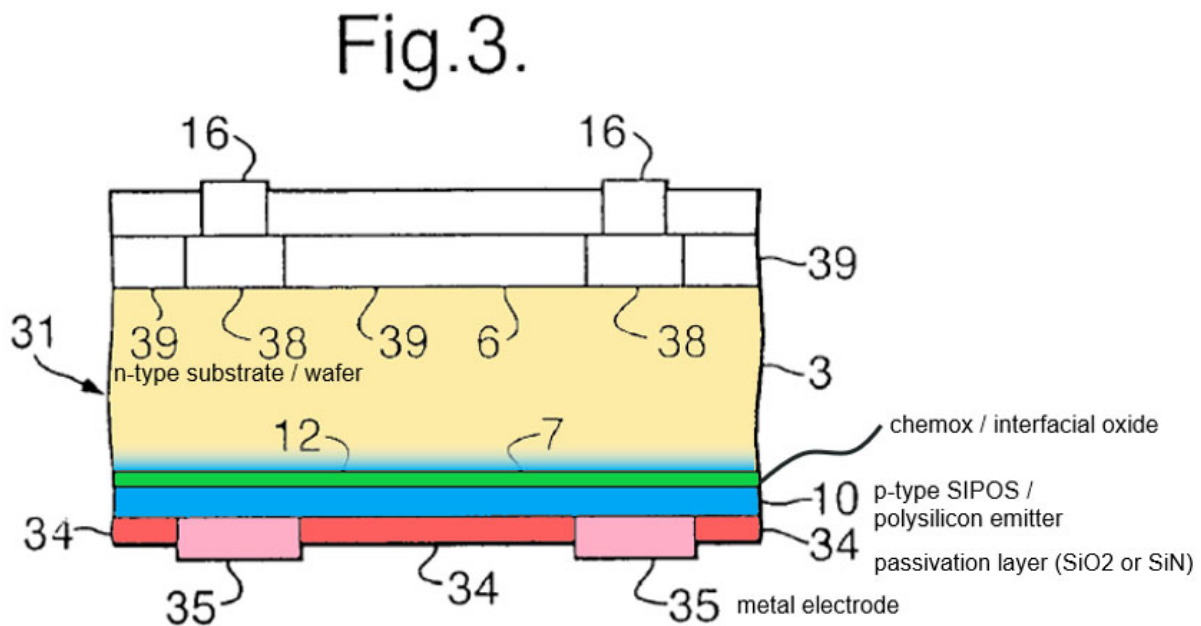


2. Claim 2 – Antireflective Layer

Claim 2 depends from claim 1 and recites: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*”

For the same reason discussed in §IX.C.2 for the Froitzheim/Yablonovitch combination, the Froitzheim/Kwark combination satisfies claim 2 using the combination of Froitzheim FIG. 3.

Second Combination of Kwark and Froitzheim (Fig. 3) According to Patent Owner’s Allegations



3. Claim 3 – Separation

Claim 3 depends from claim 1 and recites: “*wherein the depositing at least one interface passivation layer and the depositing at least one conductive and*

passivating layer comprises depositing an amorphous silicon-containing compound over the substrate and the providing thermal treatment of about 500° C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.”

The combination of Froitzheim and Kwark satisfies this step. EX1003, ¶¶280-285. In addition to polysilicon emitter, Kwark also discloses use and deposition of SIPOS emitters (without first forming a chemox layer), which are then heated/annealed above 500°C. SIPOS (which is polysilicon doped with oxygen) is a “*silicon-containing compound*” and is generally amorphous when deposited. EX1007, 1121; EX1003, ¶284.

Kwark further disclosed that the annealing process results in “the formation of an interfacial oxide” separate from the purposefully-deposited chemox layer. EX1006, 743 (“The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.”) (emphasis added); *see also* EX1007, 1121, 1125 (interfacial oxide “could form, for example, during the anneal, as oxygen segregates from the SIPOS”). In other words, the annealing step in Kwark results in the as-deposited SIPOS layer separating into a thin oxide layer (*at least one interface passivation layer*) and a layer of crystallized grains of

silicon (*at least one conductive and passivating layer*), as shown in Fig. 3 of Kwark below. EX1003, ¶¶281-282. Kwark recognized this separation as “the distinguishing feature of SIPOS.” EX1006, 743.

Kwark I, Fig. 3

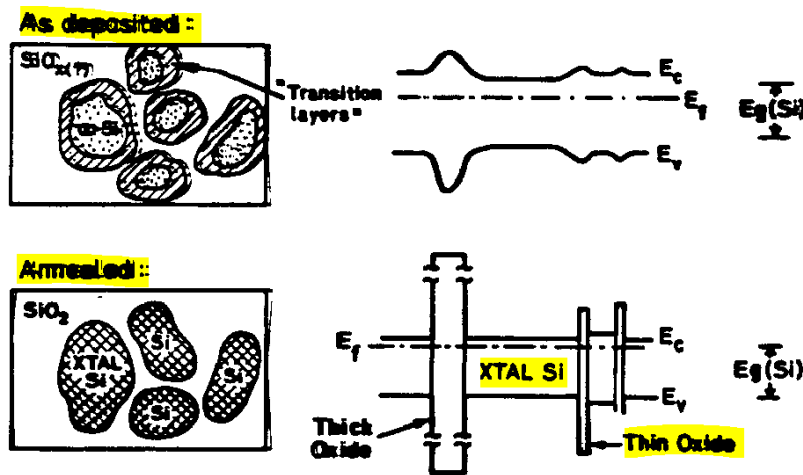


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the “oxide-like” regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Kwark’s Figures 5 and 6 further reported only a smaller decrease in J_o between SIPOS emitter deposited on a separately grown chemox and SIPOS emitter deposited without the additional chemox step. EX1006, 745; *see also, id.*, 743 (“Addition of the chemox to the SIPOS contact structure does not greatly affect the lowest values of J_{oe} attained.... The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step.”)

The Skilled Artisan would be motivated to alternatively use Kwark's segregation method for the SIPOS/interfacial layer to advantageously reduce series resistance by reducing the thickness of the interfacial oxide layer and to simplify the fabricating process. EX1003, ¶281; EX1006, 743 ("This is also consistent with the increased series resistance which would arise from a thicker interfacial layer.") And although the J_o is slighter higher, this segregation method for the SIPOS/interfacial layer still performs substantially better than the conventional diffused emitter "Al contact" control. *Id.*, 745 (Figure 5).

4. Claim 4 – Perforation

Claim 4 depends from claim 1 and recites: "*wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.*"

Kwark discloses depositing SIPOS/polysilicon and thermally treating it at temperatures between 900 and 1000°C. *See supra* §XI.C.1.d (claim [1.d]). At these annealing temperatures, Kwark's interfacial oxide and chemox layers would begin to form perforations. EX1003, ¶¶286-292. For example, Kwark II concluded that for SIPOS emitters without a chemox, an increase in J_o with higher temperatures "could be due to the break-up of the interfacial oxide" formed "during the anneal as oxygen segregates from the SIPOS." EX1007, 1125. For SIPOS emitters with the chemox layer added, Kwark's data that resistance

decreases at higher anneal temperatures again “suggest[] the break-up of the interfacial oxide.” EX1007, 1125.

However, for the SIPOS cells with a chemox layer, the constant J_{oe} between 850 and 900°C indicated that “the chemox is acting as a barrier to the out-diffusion of phosphorus, and thus prevents lifetime reduction in the surface region, or alternatively, is more resistant to break-up during annealing than whatever oxide exists without the chemox.” EX1007, 1125. In other words, according to Kwark’s findings, the chemox and interfacial oxide act as barriers to the diffusion of dopants (e.g., phosphorus) into the substrate at lower temperature, but begin to break apart during higher temperature annealing above 900°C. As Dr. Shea explains, the increase in J_{oe} is because the break-up of the interfacial oxide/chemox results in perforations that allow dopants to more easily diffuse into the oxide/chemox and the substrate. EX1003, ¶¶288-292; EX1017 (Wolstenholme), 226-27, Figs. 2-3 (describing the “holes” that begin to form in an interfacial oxide annealed at 950°C and “breakup of the interfacial oxide” at 1000°C). Charge carriers would be transported through these perforations in the oxide layer. EX1005, 1213 (“electrical contact is via thin spots and pinholes in the SiO₂”); EX1016 (“base current flows primarily through those areas of the interface that are free from oxide”); EX1003, ¶292.

5. Claim 5 – Crystallization

Claim 4 depends from claim 1 and recites: “*wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.*”

As Kwark explains, SIPOS is the result of introducing oxygen during the deposition of polysilicon. EX1006, 742. Kwark’s SIPOS layer is amorphous initially, and crystallizes during subsequent thermal treatment (annealing). EX1006, 742 (“[T]he CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant. A phase precipitation which results in a fine dispersion of silicon microcrystallites embedded in an oxygen rich matrix appears to be the result of such anneals (5)”); EX1007, 1121 (“As deposited, SIPOS is usually amorphous....”). The process of the SIPOS crystallization during annealing is depicted in Fig. 3 of Kwark I, reproduced below.

Kwark I, Fig. 3

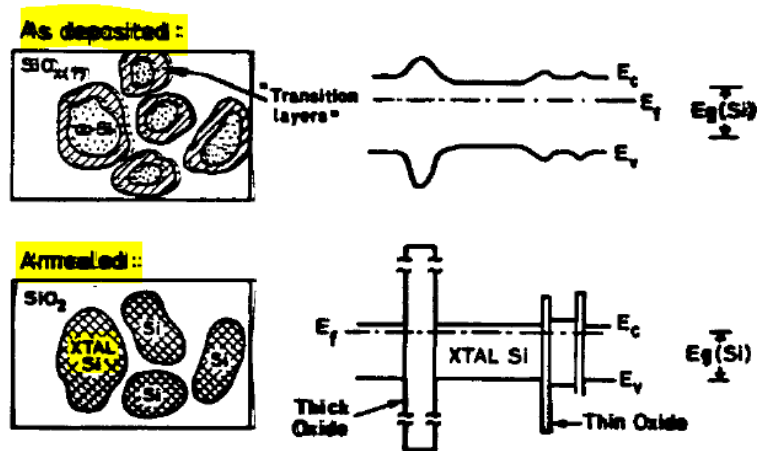


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2 -like, accompanied by crystallization of the silicon crystallites.

Likewise, Kwark discloses depositing polysilicon layers. *E.g.*, EX1006, 743. Polysilicon films, like the SIPOS films, are also amorphous when deposited and are crystallized upon heating to the high temperature disclosed in Kwark, which is above 500°C. EX1018, 499-501; EX1026, 160-61; EX1003, ¶¶296-297.

6. Claim 6 – Transmissivity

Claim 6 depends from claim 1 and recites: "*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer and [b] increases the optical*

transmissivity.” The combination of Kwark and Froitzheim discloses part [a] of claim 6, *see supra* §XI.C.5 (claim 5).

Annealing Kwark’s SIPOS layer to form microcrystalline silicon grains further increases optical transmissivity, for the same reasons discussed in §IX.C.5 above. EX1003, ¶¶300-304.

7. Claim 7 – Dopant Activation

Claim 7 depends from claim 1 and recites: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein the thermal treatment activates doping atoms in the compound.*” The combination of Kwark and Froitzheim discloses part [a] of claim 7, *see supra* §XI.C.5 (claim 5). As to part [b] of claim 7, Kwark further taught that the thermal treatment annealing process “activate[s]” the dopants in the SIPOS layer. EX1006, 742 (“[T]he CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant.”) (emphasis added). Although Kwark’s investigation studied n-type SIPOS, annealing would activate boron dopants in p-type SIPOS in the same way. EX1003, ¶308; EX1018, 480.

8. Claim 8 – PN Junction

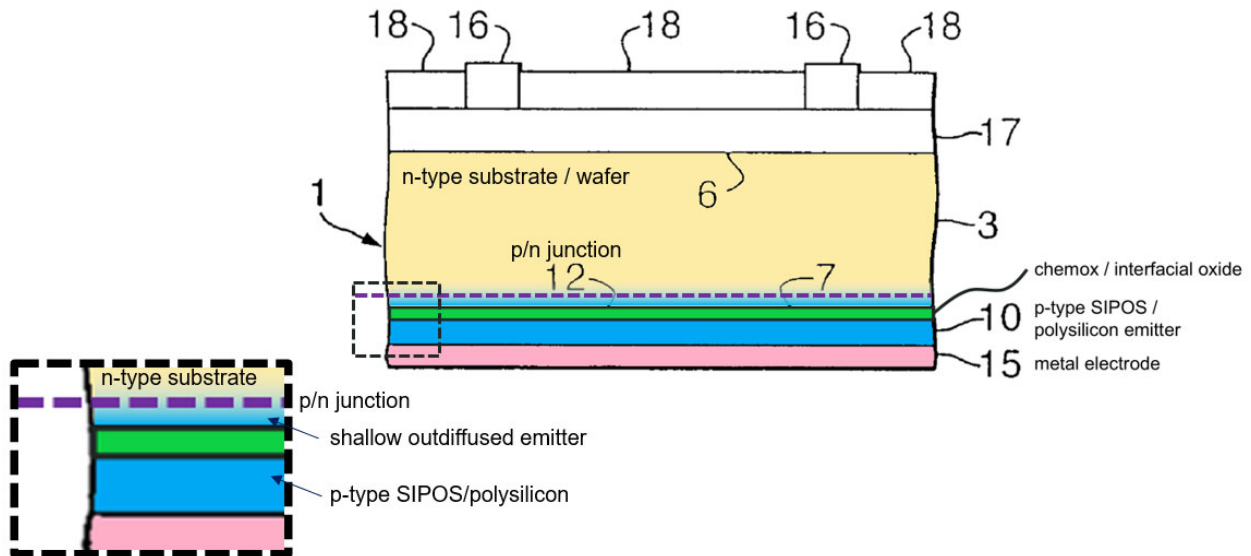
Claim 8 depends from claim 1 and recites: “*wherein [a] the at least one conductive and passivating layer comprises an amorphous, silicon containing*

compound, and [b] wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.” The combination of Kwark and Froitzheim discloses part [a] of claim 8, *see supra* §XI.C.5 (claim 5). As to part [b] of claim 8, Kwark’s annealing step diffuses n-type dopants from the SIPOS layer through the interfacial oxide layer into the substrate. EX1006, 743 (“emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction.”), Fig. 4. The same result would occur when diffusing p-type dopants (boron) during the formation of a p-type SIPOS layer. EX1003, ¶¶311-312; EX1036, Fig. 4; EX1039, §3.3, Fig. 8.

Because the proposed combination of Kwark and Froitzheim has an n-type substrate with a p-type SIPOS/polysilicon emitter layer (or vice versa), Kwark’s annealing step to activate boron (p-type) dopants in the SIPOS and diffuse boron into the n-type substrate would result in the formation of a p-n junction. *See* EX1008, ¶¶25 (“At the rear side 7, a p-doped layer 10 is arranged suitably such as discussed further below, and a p/n-junction 12 with the body layer is formed.”), 32, 68.

Proposed Combination of Kwark and Froitzheim

Fig. 1.

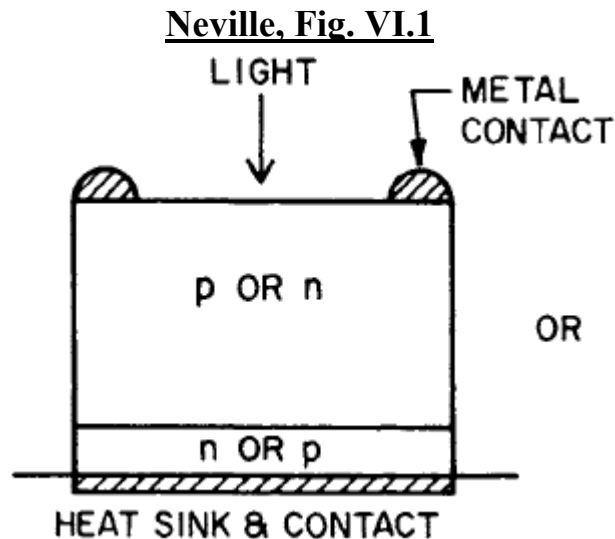


XII. GROUND IV: CLAIMS 1-8 ARE UNPATENTABLE OVER FROITZHEIM, NEVILLE, AND KWARK

As explained above in the Ground III combination of Froitzheim and Kwark, the Skilled Artisan would understand that the polarity of the emitter layer and substrate in a back junction cell could be interchanged. *See* §XI.A-B. To the extent PO may argue that Kwark teaches only use of n-type SIPOS layers, Claims 1-8 would still be obvious based on the combination of Froitzheim, Neville, and Kwark.

Ground IV is otherwise identical to Ground III, except that instead of using the n-type substrate in Froitzheim, the Skilled Artisan would use a p-type substrate because they are interchangeable as taught by Neville, Fig. VI.1. EX1003, ¶¶314-

316; EX1009, 199, Fig. VI.1. *See ACCO*, 813 F.3d at 1367 (obvious to try both possible options); *Vanda*, 2023 WL 3335538 at *5 (same).



This way, the Skilled Artisan can directly use the n-type SIPOS of Kwark to replace the diffused in-substrate emitter in the back junction cell. EX1003, 236-238. The use of a p-type substrate is well within the skill of the Skilled Artisan because p-type silicon substrates were widely used before 2008. EX1003, ¶315. Thus, the Skilled Artisan would reasonably expect success for such a combination. EX1003, 236-238.

XIII. GROUNDS V AND VI: CLAIM 2 IS UNPATENTABLE IN FURTHER VIEW OF SASAKI

H. Sasaki, et al., Light Trapping for Thin-Film Silicon Solar Cells Fabricated on Insulator, *Jpn. J. Appl. Phys.* Vol. 33 (1994) pp. 3389-3392 (“Sasaki”), is a paper published no later than 1997. EX1010, face; EX1043, ¶¶123-143. Exhibit

EX1010 is an authentic copy of Sasaki that was published before April 2008. *Id.*

Thus, it is prior art under 35 U.S.C. §102(a) and (b).

A. Sasaki Discloses the Step of Claim 2

Claim 2 depends from claim 1 and recites: “*further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.*” Figure 6 of the 074 Patent discloses a “transparent and conductive film” 68 can be transparent conductive oxides (“TCO”) formed on the backside that provides a “a low reflective layer for a good internal mirror on the back.” EX1001, 6:18-24, 15:31-34. This TCO can be indium tin oxide, aluminum-doped zinc oxide, and others. EX1001, 6:18-24.

Sasaki also discloses a TCO made of indium tin oxide that forms a good internal mirror on the back of a solar cell. As Sasaki explains, “cell structure can be used to achieve high light reflectivity using rear surface treatments such as a textured structure or deposition of highly reflective metals.” EX1010 at 3390. Sasaki thus proposed using a rear electrode of “silver (Ag) metal and a transparent conductive indium tin oxide (ITO) film inserted between the thin Si film and Ag layer.” EX1010 at 3390. As shown in Fig. 2 of Sasaki reproduced below, photons are internally reflected at the interface of the silicon and the ITO layer located on the rear side of the solar cell. EX1003, ¶211.

Sasaki, Fig. 2

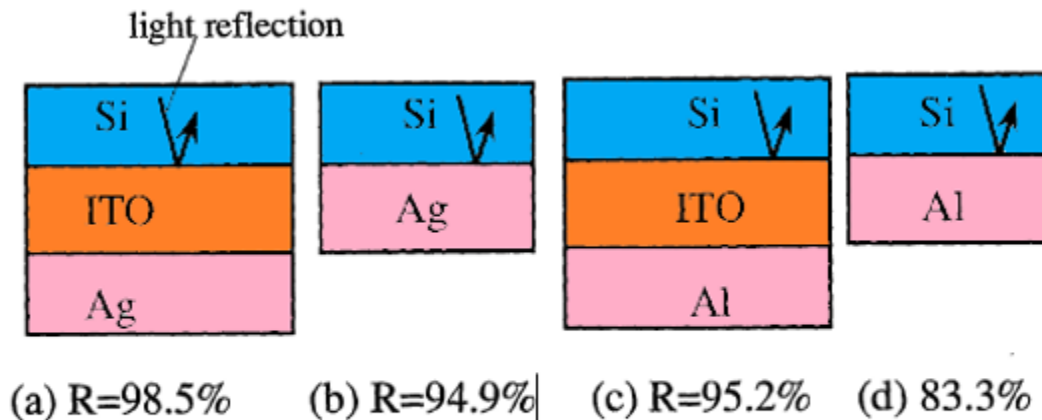


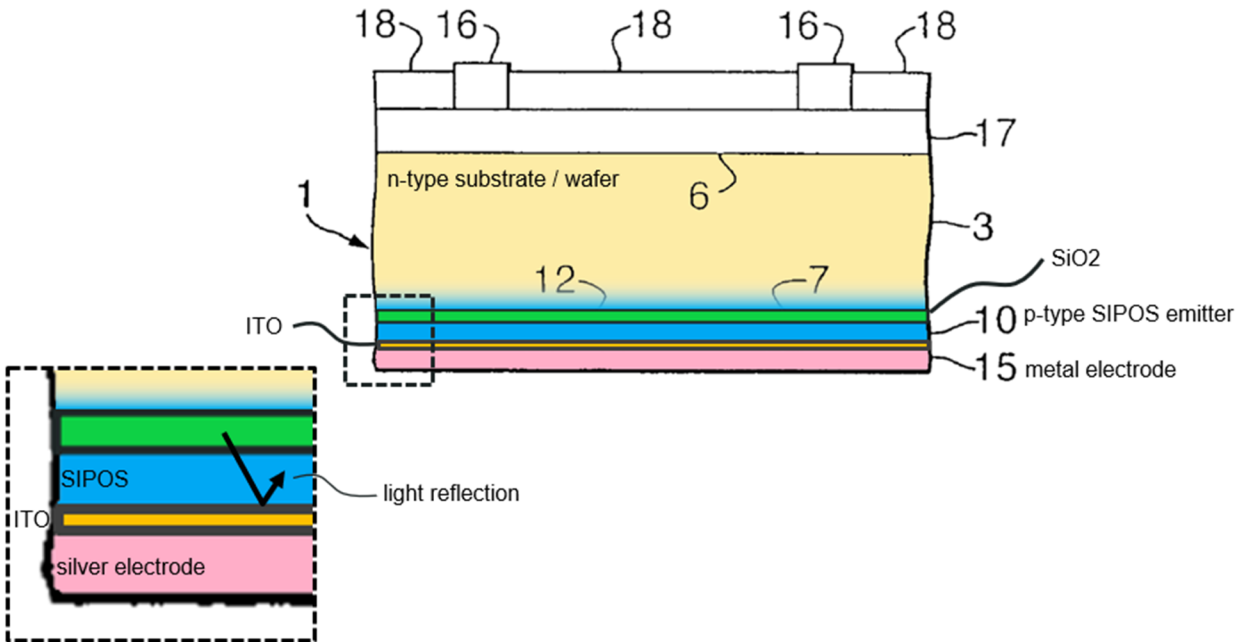
Fig. 2. Calculated reflectances for four different conditions of rear reflectors at opening.

B. Ground V: Froitzheim (with or without Neville), Yablonovitch, and Sasaki

As explained above, Froitzheim combined with Yablonovitch, with or without Neville, renders claim 2 obvious. Alternatively, the additional step in claim 2 is obvious based on Sasaki. In the proposed combination of Froitzheim (with or without Neville) and Yablonovitch, further with Sasaki, the ITO layer is further deposited on the SIPOS layer before forming the backside metal electrode to improve upon the solar cell by absorbing more photons. The resulting modified solar cell is illustrated below using a modified Froitzheim Fig. 1 for illustration. EX1003, ¶¶207-208. The combination would be nothing more than inserting Sasaki's step of depositing the ITO between Yablonovitch's step of forming and annealing of the SIPOS layer on the back of the substrate and Froitzheim's step for forming metal contacts. *Id.*

Proposed Combination of Froitzheim, Yablonovitch, and Sasaki

Fig.1.

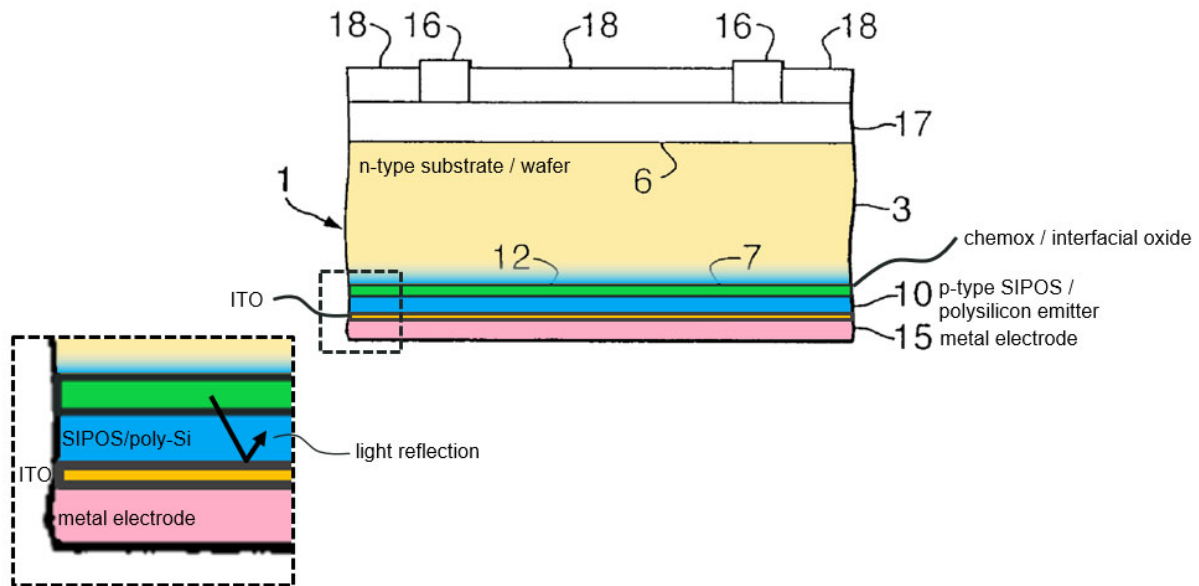


C. Ground VI: Froitzheim (with or without Neville), Kwark, and Sasaki

Likewise, to improve upon the solar cell combination of Froitzheim and Kwark, the Skilled Artisan would have inserted a TCO between the SIPOS/polysilicon emitter and electrode, such as the ITO layer taught by Sasaki. The resulting modified solar cell is illustrated below. EX1003, ¶¶318-319. The combination would be nothing more than inserting Sasaki's step of depositing the TCO between Kwark's step of depositing and annealing the SIPOS/polysilicon layer on the back of the substrate and Froitzheim's step for forming metal contacts. *Id.*

Proposed Combination of Froitzheim, Kwark, and Sasaki

Fig. 1.



D. Motivation to Combine

Sasaki, Froitzheim, Yablonovitch and Kwark are analogous art because each is in the same field of endeavor—solar cell design. EX1003, ¶¶214, 322; EX1008, Abstract, ¶¶1, 9; EX1005, Abstract, 1211-12; EX1010, Abstract, 3389; EX1006, 742. Each is reasonably pertinent to the problems of efficiency and cost-effectiveness of solar cell designs. EX1003, ¶¶214, 322; EX1008, Abstract, ¶¶1, 9; EX1005, Abstract, 1211; EX1010, Abstract, 3389; EX1006, 742.

The Skilled Artisan would have been motivated to further modify the combinations of Froitzheim/Yablonovitch and Froitzheim/Kwark (with or without Neville) to incorporate an ITO layer because Sasaki taught and suggested that this

modification would improve solar cell efficiency. EX1003, ¶¶215, 323. In particular, Sasaki taught that “insertion of the ITO film between Si and Ag [silver electrode] makes it possible to obtain a sufficiently high reflectance of $R=98.5\%$ ” from 94.9% using an Ag electrode alone, while for less-expensive aluminum electrodes “insertion of the ITO film can improve the reflectance from $R=83.3\%$ to $R=95.2\%$,” resulting in a solar cell with “high efficiency”. EX1010, 3390, 3392. Improving the reflectance increases the amount of photons being absorbed by the silicon substrate such that the more photons are converted into electricity by the solar cell. EX1003, ¶¶216, 324. Although Sasaki discloses the TCO use in a thin-film solar cell, the Skilled Artisan would understand and be motivated to equally apply this to the Froitzheim/Yablonovitch or Kwart solar cell made from crystalline solar wafers. EX1003, ¶¶217, 325. Even before 2008, TCO films were well known and had been used with heterojunction solar cells made from crystalline solar wafers, which have a very similar structure to the proposed combination. *Id.*; EX1019, Fig. 7.14, 289 (“On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed” on top of the TCO layers; “Mass production of HIT cells started in 1997”).

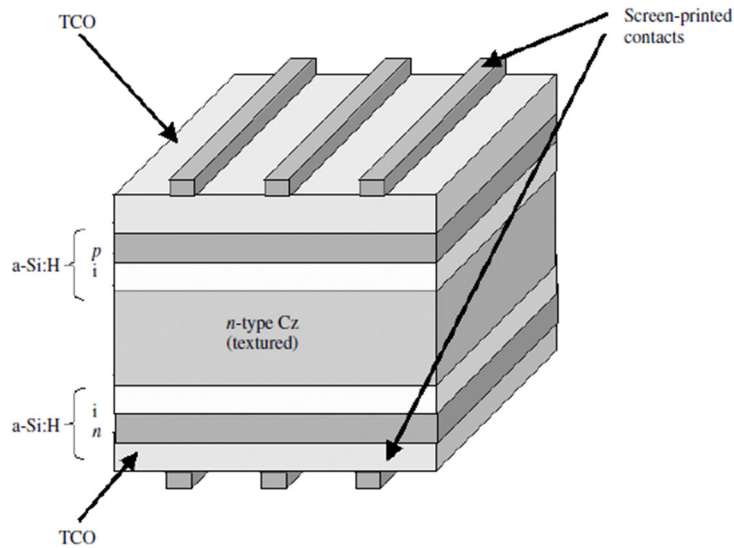


Figure 7.14 Structure of the HIT cell

E. Reasonable Expectation of Success

The Skilled Artisan would have considered the Sasaki combinations with Froitzheim/Yablonovitch and Froitzheim/Kwark (with or without Neville) to be merely an arrangement of old method steps with each performing the same function it had been known to perform (the combined solar cell discussed above, but modified to have an ITO) and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). EX1003, ¶¶218-220, 326-328.

Specifically, after annealing the SIPOS/polysilicon emitter as described by Yablonovitch or Kwark, but before forming a rear electrode, an ITO layer would be deposited on the SIPOS/polysilicon emitter as taught by Sasaki. EX1010, 3390. This ITO deposition step would then be followed by the metallization as described

by Froitzheim, to form a rear electrode made of silver and/or aluminum. EX1008, ¶¶27, 48-49.

Combining Froitzheim/Yablonovitch or Froitzheim/Kwark with Sasaki as described here would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. EX1003, ¶¶218-220, 326-328. Even before 2008, forming a TCO layer on top of deposited doped layers were well known and well within the skill of the Skilled Artisan. *See, e.g.*, EX1019, Fig. 7.14, 289 (“On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed” on top of the TCO layers). The combinations would simply have been the combination of prior art elements according to known methods to yield predictable results, namely, the straightforward deposition of an indium tin oxide layer according to standard, well-known deposition techniques. *Id.*

XIV. OBJECTIVE FACTORS SUPPORT OBVIOUSNESS

There is no commercial success attributable to the 074 Patent claims. EX1003, ¶329. Notably, PO acquired the 074 Patent from Tetrasun in 2013 prior to its issuance in 2015. PO then abandoned Tetrasun technology in 2016 and does

not practice the patent. *See, e.g.*, EX1033 (First Solar's current patent marking list). Thus, there is no commercial success attributable to the 074 Patent.

There is also no unexpected result in replacing the backside diffused emitter in a back junction solar cell like Froitzheim with a polysilicon emitter having an interfacial oxide layer in between, as taught by Yablonovitch and Kwark. EX1003, ¶¶330-332. The Skilled Artisan would have expected to reap benefits from such modification such as higher solar cell efficiencies and lower recombination, as seen from the teachings of Yablonovitch and Kwark. *Id.* And including an oxide layer between the polysilicon layer and the substrate was well-known to confer expected benefits as well. In fact, making such a modification to Froitzheim was simply following the conventional wisdom, which is evidenced by Cousins that in fact proposed that combination before the 074 Patent invention. *Id.*

Dated: August 22, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,314 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: August 22, 2025

Respectfully submitted,

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Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,130,074**

**Attachment A:
Proof of Service of the Petition**

CERTIFICATE OF SERVICE

I hereby certify that on this 22nd day of August 2025, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

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Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,130,074**

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074

Exhibit #	Reference Name
1001	U.S. Patent No. 9,130,074
1002	File History of U.S. Patent No. 9,130,074
1003	Declaration of Dr. Stephen Shea Regarding U.S. Patent No. 9,130,074
1004	Curriculum Vitae of Dr. Stephen Shea
1005	E. Yablonovitch, et al., A 720 mV open circuit voltage SiO _x :c-Si:SiO _x double heterostructure solar cell, Appl. Phys. Lett. 47 (11) (Dec. 1, 1985) (“Yablonovitch”)
1006	Y.H. Kwark et al., “SIPOS Heterojunction contacts to silicon,” International Electron Devices Meeting (1984): 742-745 (“Kwark”)
1007	Y.H. Kwark, et al., <i>N</i> -Type SIPOS and Poly-Silicon Emitters, Solid-State Elecs. Vol. 30, No. 11, pp. 1121-1125 (1987)
1008	EP 1732142 A1 (“Froitzheim”)
1009	R. Neville, Solar Energy Conversion: The Solar Cell, 2nd Ed. (Elsevier 1995) (excerpted) (“Neville”)
1010	H. Sasaki, et al., Light Trapping for Thin-Film Silicon Solar Cells Fabricated on Insulator, Jpn. J. Appl. Phys., Vol. 33, pp. 3389-3392 (1994) (“Sasaki”)
1011	U.S. Patent No. 4,525,593 (“Yablonovitch Patent”)
1012	J.Y. Gan, et al, Polysilicon Emitters for Silicon Concentrator Solar Cells, Twenty First IEEE Photovoltaic Specialists Conference-1990, Vol. 1, pp. 245-250 (“Gan”)
1013	W. Fussel, et al., Structural, optical and electrical properties of SIPOS passivation layers, Microelectronic Engineering 22 (1993) 355-358 (“Fussel”)
1014	G. Compagnini, Optical and structural properties of semi-insulating polycrystalline silicon thin films, J. Mater. Res., Vol. 10, No. 4 (Apr 1995) (“Compagnini”)

Exhibit #	Reference Name
1015	Y. Pan, et al., Study on the optical absorption of oxygen-doped polysilicon thin films, Optical Engineering 32(3), 589-592 (March 1993) (“Pan”)
1016	I. Post, et al., Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment, IEEE Transactions on Electron Devices, Vol. 39. No. 7 (July 1992) (“Post”)
1017	G.R. Wolstenholme, et al., An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations, J. Appl. Phys. 61 (1) (January 1987) (“Wolstenholme”)
1018	Michael Quirk and Julian Serda, Semiconductor Manufacturing Technology, Prentice-Hall, Inc. (2001) (“Quirk”)
1019	A. Luque, et al., Handbook of Photovoltaic Science and Engineering, John Wiley & Sons Ltd. (2003) (“Luque”)
1020	F. A. Lindholm, A. Neugroschel, M. Arienzo, and P. A. Iles. "Heavily Doped Polysilicon-Contact Solar Cells." IEEE Electron Device Letters, volume 6, number 7, July 1985, pages 363-365 (“Lindholm”)
1021	K. Tatsumura, et al., Residual order within thermally grown amorphous SiO ₂ on crystalline silicon, Phys. Rev. B 69, 085212 (2004) (“Tatsumura”)
1022	US Patent No. 7,851,336 (“Poplavskyy”)
1023	File History of US Patent No. 7,851,336 (excerpt)
1024	Complaint for Patent Infringement, <i>First Solar Inc. v. Canadian Solar Inc., et al.</i> , Case No. 1:25-cv-00582-JLH, Dkt. 1 (D. Del.)
1025	Y.H. Kwark., et al., Optical Absorption of Thin SIPOS Films, J. Electrochem. Soc., Solid-State Science and Technology, Vol. 129, No. 1, pp. 197-201 (1982) (“Kwark III”)

Exhibit #	Reference Name
1026	B. Streetman, et al., Solid State Electronic Devices, Sixth Ed., Prentice Hall (2006) (“Streetman”)
1027	P. Ashburn, et al., Comparison of Experimental and Theoretical Results on Polysilicon Emitter Bipolar Transistors, IEEE Transactions on Electron Devices, Vol. ED-31, No. 7 (July 1984) (“Ashburn”)
1028	E. Yablonovitch, et al., A Study of n ⁺ -SIPOS:p-Si Heterojunction Emitters, IEEE Electron Device Letters, Vol. EDL-6, No. 11 (Nov. 1985) (“Yablonovitch 1984”)
1029	R. Sinton, et al., Design Criteria for Si Point-Contact Concentrator Solar Cells, IEEE Transactions on Electron Devices, Vol. ED-34, No. 10 (Oct. 1987)
1030	A. Zuoari, et al., Simple analytical solution and efficiency improvement of polysilicon emitter solar cells, Solar Energy Materials & Solar Cells 92 (2008) 313–322 (“Zouari”)
1031	R. Fair, Physical Models of Boron Diffusion in Ultrathin Gate Oxides, J. Electrochem. Soc., Vol. 144, No. 2 (Feb. 1997) (“Fair”)
1032	U.S. Patent No. 8,222,516 (“Cousins”)
1033	First Solar’s Patent Marking Notification List (<i>available at</i> https://www.firstsolar.com/-/media/First-Solar/Documents/Patents/Patent-Marking-Notification.pdf as of August 14, 2025)
1034	U.S. Patent No. 4,667,060 (“Spitzer”)
1035	T. Matsushita, et al., Highly Reliable High-Voltage Transistors by Use of the SIPOS Process, IEEE Transactions on Electron Devices, Vol. ED-23, No. 8 (Aug. 1976) (“Matsushita”)
1036	P. Borden, et al., Polysilicon Tunnel Junctions as Alternates to Diffused Junctions, 23rd European Photovoltaic Solar Energy Conference, 1-5 September 2008 (“Borden”)

Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074

Exhibit #	Reference Name
1037	M. Janai, et al., Optical Properties and Structure of Amorphous Silicon Films Prepared by CVD, Solar Energy Materials 1 (1979), pp. 11-27 (“Janai”)
1038	S. Silvestre, Series Resistance in Double-Polysilicon-Contacted Silicon Solar Cells, 25th PVSC, 13-17 May 1996 (“Silvestre”)
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Petition for *Inter Partes* Review of U.S. Patent No. 9,130,074

**PETITION FOR INTER PARTES REVIEW
OF U.S. PATENT NO. 9,130,074**

**Attachment C:
Listing of the Claims of 9,130,074**

Claim Element	Claim Language
[1.a]	A method of fabricating a solar cell, comprising;
[1.b]	providing a wafer as a central substrate;
[1.c]	depositing or growing at least one amorphous interface passivation layer over the substrate;
[1.d]	depositing at least one conductive and passivating layer on the at least one interface passivation layer, the at least one conductive and passivating layer comprising a dopant;
[1.e]	providing thermal treatment at a temperature of about 500° C. or higher, the thermal treatment crystallizing, at least in part, the at least one conductive and passivating layer and facilitating diffusion of the dopant from the at least one conductive and passivating layer through the at least one interface passivation layer; and
[1.f]	providing metallization as electrodes which directly contact the at least one conductive and passivating layer following the thermal treatment thereof, wherein the dopant diffused through the at least one interface passivation layer provides shortened charge carrier flow paths between the substrate and the electrodes through the at least one conductive and passivating layer and the at least one interface passivation layer.
2	The method of claim 1, further comprising depositing at least one antireflective layer, and/or a low reflective index layer forming a good internal mirror on a back of the solar cell.

3	The method of claim 1, wherein the depositing at least one interface passivation layer and the depositing at least one conductive and passivating layer comprises depositing an amorphous silicon-containing compound over the substrate and the providing thermal treatment of about 500° C. or higher separates the amorphous silicon-containing compound into the at least one interface passivation layer and the at least one conductive and passivating layer.
4	The method of claim 1, wherein the thermal treatment results in perforation of the at least one interface passivation layer to allow carrier transport therethrough.
5	The method of claim 1, wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer into a polycrystalline film.
6	The method of claim 1, [a] wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and wherein the thermal treatment initiates crystallization of the at least one conductive and passivating layer [b] and increases the optical transmissivity.
7	The method of claim 1, [a] wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein the thermal treatment activates doping atoms in the compound.

8	The method of claim 1, [a] wherein the at least one conductive and passivating layer comprises an amorphous, silicon containing compound, and [b] wherein facilitating diffusion of the dopant further comprises facilitating diffusion of dopant atoms into the substrate to provide a high-low junction or a p-n junction.
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