Paper No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

Excelliance Mos Corporation,

Petitioner

v.

Force Mos Technology Co., Ltd.,

Patent Owner

Patent No. 7,629,634

Issue Date: December 8, 2009

Title: TRENCHED MOSFET WITH TRENCHED SOURCE CONTACT

Inter Partes Review No. IPR2025-01433

PETITION FOR *INTER PARTES* REVIEW

OF CLAIMS 1-9 OF U.S. PATENT NO. 7,629,634

UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *ET. SEQ.*

TABLE OF CONTENTS

I. INTRODUCTION 13

II. MANDATORY NOTICES PURSUANT TO 37 C.F.R. § 42.8(A)(1) 13

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1)) 13

B. Related Matters (37 C.F.R. § 42.8(b)(2)) 14

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)) 14

D. Service Information (37 C.F.R. § 42.8(b)(4)) 15

E. Payment of Fees (37 C.F.R. § 42.103) 15

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104 16

A. Grounds for Standing (§ 42.104(a)) 16

B. Identification of Challenge and Statement of Precise Relief Requested for Each of the Challenged Claims (§ 42.104(b)) 16

IV. INTRODUCTION TO '634 PATENT 17

A. The '634 Patent 17

B. The '634 Patent File History 19

V. OVERVIEW OF THE PRIOR ART 19

A. U.S. Patent Publication No. US 2006/0273384 A1 ("Hshieh") 20

B. U.S. Patent No. 6,984,864 B2 ("Uno") 21

VI. LEVEL OF ORDINARY SKILL IN THE ART 22

VII. CONSTRUCTION OF THE CLAIMS 23

A. Independent Claim 1: "the bottom base of said trenches in said base layer" 23

B. Independent Claim 1: "the sidewalls of said trenches in said base layer" 25

VIII. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS FOR UNPATENTABILITY 26

A. Ground 1: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Hshieh ('384) 26
1. Independent Claim 1 26
a. Limitation [1-preamble] 26
i. [1-preamble-1] 26
ii. [1-preamble-2] 27
b. Limitation [1a] 29
i. Limitation [1a-1] 29
1) [1a-1-1] 29
2) [1a-1-2] 31
3) [1a-1-3] 34
4) [1a-1-4] 36
ii. Limitation [1a-2] 38
1) [1a-2-1] 38
2) [1a-2-2] 40
3) [1a-2-3] 42
4) [1a-2-4] 44
c. Limitation [1b] 46
d. Limitation [1c] 48
e. Limitation [1d] 51
f. Limitation [1e] 55
g. Limitation [1f] 58
i. [1f-1] 58
ii. [1f-2] 62
iii. [1f-3] 66
2. Dependent Claim 2 67
a. Limitation [2a] 67
b. Limitation [2b] 69
c. Limitation [2c] 71
d. Limitation [2d] 73
3. Dependent Claim 3 78
a. Limitation [3a] 78
b. Limitation [3b] 80
4. Dependent Claim 4: 82
a. Limitation [4a] 82
b. Limitation [4b] 84
5. Dependent Claim 5 86
6. Dependent Claims 6 - 9 91

B. Ground 2: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Uno ('864) 93
1. Independent Claim 1 93
a. Limitation [1-preamble] 93
i. [1-preamble-1] 93
ii. [1-preamble-2] 94
b. Limitation [1a] 95
i. Limitation [1a-1] 95
1) [1a-1-1] 95
2) [1a-1-2] 96
3) [1a-1-3] 98
4) [1a-1-4] 99
ii. Limitation [1a-2] 101
1) [1a-2-1] 101
2) [1a-2-2] 102
3) [1a-2-3] 104
4) [1a-2-4] 105
c. Limitation [1b] 107
d. Limitation [1c] 108
e. Limitation [1d] 110
f. Limitation [1e] 112
g. Limitation [1f] 113
i. [1f-1] 113
ii. [1f-2] 115
iii. [1f-3] 117
2. Dependent Claim 2 118
a. Limitation [2a] 118
b. Limitation [2b] 120
c. Limitation [2c] 122
d. Limitation [2d] 123
3. Dependent Claim 3 125
a. Limitation [3a] 126
b. Limitation [3b] 127
4. Dependent Claim 4 128
a. Limitation [4a] 128
b. Limitation [4b] 129
5. Dependent Claim 5 131
6. Dependent Claims 6 - 9 132

C. Ground 3: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Hshieh ('384) and Uno ('864) (and *vice versa*) 132
1. Independent Claim 1 132
a. [Preamble] 133
b. Limitation [1a] 133
c. Limitation [1b] 133
d. Limitation [1c] 134
e. Limitation [1d] 134
f. Limitation [1e] 136
g. Limitation [1f] 136
2. Dependent Claims 2-9 136
3. Motivation to Combine 136

IX. CONCLUSION 137

TABLE OF AUTHORITIES

CASES

Atlas Powder Co. v. IRECO Inc., 190 F.3d 1342, 1347 (Fed. Cir. 1999) ---------125

Daiichi Sankyo Co. v. Apotex, Inc., 501 F.3d 1254, 1256 (Fed. Cir. 2007.) ------- 21

STATUTES

35 U.S.C. § 311---------- 15

35 U.S.C. § 312(a)(1)---------- 15

35 U.S.C. § 315---------- 15

35 U.S.C. § 325---------- 15

REGULATIONS

37 C.F.R. § 42.10(b) ----------14, 15

37 C.F.R. § 42.103 ---------- 14

37 C.F.R. § 42.104(a)---------- 15

37 C.F.R. § 42.15(a) ---------- 14

37 C.F.R. § 42.24----------140

37 C.F.R. § 42.8(a)(1) ---------- 12

37 C.F.R. § 42.8(b)---------- 12

37 C.F.R. § 42.8(b)(1) ---------- 12

37 C.F.R. § 42.8(b)(2) ---------- 13

37 C.F.R. § 42.8(b)(3) ---------- 13

37 C.F.R. § 42.8(b)(4) ---------- 14

EXHIBIT LIST

EXHIBIT	DESCRIPTION
1001	U.S. Patent No. 7,629,634 (the "'634 Patent" or "'634")
1002	File History of the '634 Patent
1003	Expert Declaration of Dr. Daniel Foty
1004	Expert Curriculum Vitae of Dr. Daniel Foty
1005	U.S. Patent Publication No. 2006/0273384 A1 ("Hshieh" or "'384")
1006	U.S. Patent No. 6,984,864 ("Uno" or "'864")
1007	B. Davari et al., *A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS*, International Electron Devices Meeting, 92-95 (1988)
1008	Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 191, 281, 385-387 (1990)
1009	S. Van Huylenbroeck et al., *A 0.25um SiGe BiCMOS Technology Including Integrated RF Passive Components Optimised for Low Power Applications*, European Solid State Device Research Conference (ESSDERC), 505-508 (2003)
1010	U.S. Patent No. 5,395,786
1011	H. Shichijo et al., *Trench Transistor DRAM Cell*, *IEEE Electron Device Letters*, vol. 7, 119-121 (1986)
1012	*Metal Insulator Semiconductor Field Effect Transistors (MISFETs)*, EEEGUIDE, https://www.eeeguide.com/metal-insulator-semiconductor-field-effect-transistors-misfets/ (last visited July 31, 2025)
1013	Adel S. Sedra and Kenneth C. Smith, *Microelectronics Circuits*, 237 (5th ed. 2004)
1014	U.S. Patent No. 4,980,747
1015	Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 1, 124, 187-

	191 (1986)
1016	Ashwin H. Shah et al., *A 4-Mbit DRAM with Trench-Transistor Cell*, IEEE Journal of Solid State Circuits vol. SC-21, 618-626 (1986)
1017	*Properties of SiO_2 and Si_3N_4 at 300K*, Comprehensive Reference on EESEMI Semiconductor Manufacturing, https://eesemi.com/sio2si3n4.htm (last visited July 31, 2025)
1018	A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 (1967)
1019	*Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG, E.D. Tex. (Marshall) 2022, ECF No. 416 (Trial Transcript Excerpt)
1020	Genshu Fuse et al., *Indirect Trench Sidewall Doping by Implantation of Reflected Ions*, Applied Physics Letters, vol. 54, 1534-1536 (1989)
1021	S. E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 379-382 (2003)
1022	Michael Quirk and Julian Serda, *Semiconductor Manufacturing Technology*, 475 (2001)
1023	A. Agrawal et al., *Self-Sealed Circular Channels for Micro-Fluidics, Sensors and Actuators (A: Physical)*, 80-87 (2006)
1024	D. Edelstein et al., *Full Copper Wiring in a Sub-0.25 um CMOS ULSI Technolog*y, IEDM Technical Digest, 773-776 (1997)
1025	S. Nizou et al., *Deep Trench Doping by Plasma Immersion Ion Implantation in Silicon*, Ion Implantation Technology: 16th International Conference on Ion Implantation Technology, 229-232 (2006)
1026	*Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG, E.D. Tex. (Marshall), 2022, ECF No. 132, 13-17

LISTING OF CLAIMS

U.S. Patent No. 7,629,634 (the "'634 Patent" or "'634")	
Claim Designation	**Claim Language**
[1-preamble]	"A trenched MOSFET with trenched source contact, comprising:"
[1-preamble-1]	"trenched MOSFET"
[1-preamble-2]	"trenched source contact"
Claim *[1a]*	"a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"
[1a-1]	"a semiconductor region having a drain region, a body region and a source region,"
[1a-1-1]	"a semiconductor region"
[1a-1-2]	"a drain region"
[1a-1-3]	"a body region"
[1a-1-4]	"a source region"
[1a-2]	"a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"
[1a-2-1]	"silicon substrate"
[1a-2-2]	"an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate"

[1a-2-3]	"a base layer corresponding to said body region disposed on the top of said epitaxial layer"
[1a-2-4]	"a source layer corresponding to said source region disposed on the top of said base layer"
[1b]	"a front metal layer formed on the upper surface of said semiconductor region;"
[1c]	"an interlayer oxide film formed between said source layer and said front metal layer,"
[1d]	"a bottom metal layer formed on the lower surface of said semiconductor region"
[1e]	"a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and"
[1f]	"a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer; wherein the bottom base of said trenches in said base layer are covered by the base contact layer."
[1f-1]	"a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer;"
[1f-2]	"the sidewalls of said trenches in said base layer are covered by the lateral contact layer"
[1f-3]	"the bottom base of said trenches in said base layer are covered by the base contact layer"
Claim 2	"The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type;

	and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."
[2a]	"the silicon substrate, the epitaxial layer, and the source layer are N-type"
[2b]	"the base layer and lateral contact layer are P-type"
[2c]	"each of the source contact trenches further has a P-type base contact layer at a bottom thereof"
[2d]	"the lateral contact layer has less doping concentration than the base contact layer at bottom."
Claim 3	"The trenched MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."
[3a]	"wherein further comprises a barrier metal layer and"
[3b]	"a plurality of contact metal plugs"
Claim 4	"The trenched MOSFET of claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."
[4a]	"the barrier metal layer is Ti/TiN"
[4b]	"the contact metal plug is Tungsten"
Claim 5	"The trenched MOSFET of claim 4, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."
Claim 6	"The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-

	type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."
[6a]	"wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof,"
[6b]	"and the lateral contact layer has less doping concentration than the base contact layer at bottom."
Claim 7	"The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."
Claim 8	"The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten."
Claim 9	"The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

I. INTRODUCTION

Petitioner, Excelliance Mos Corporation ("EMC" or "Petitioner"), respectfully requests institution of an *inter partes* review (IPR) and cancellation of Claims 1-9 ("the Challenged Claims") of U.S. Patent No. 7,629,634 (the "'634 Patent") (Ex. 1001.) The Challenged Claims generally relate to trenched MOSFET with trenched source contact. The claimed invention was well-known in the relevant art prior to the effective filing date of the '634 Patent.

II. MANDATORY NOTICES PURSUANT TO 37 C.F.R. § 42.8(a)(1)

Pursuant to 37 C.F.R. § 42.8(a)(1), the mandatory notices identified in 37 C.F.R. § 42.8(b) are provided below as part of this Petition.

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Excelliance Mos Corporation is the real party-in-interest for this Petition. No other persons or entities, other than the Petitioner, exercise control or could be said to have a direct interest in the outcome of this proceeding. Specifically, no other party has funded, directed, or influenced the preparation or filing of this petition, and no other party has the right to intervene, control, or participate in this proceeding.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

Petitioner identifies the following judicial and administrative proceedings involving the same patent or may otherwise impact, or be impacted by, the outcome of this proceeding:

1. *Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc*., No.: 2:22-cv-00460 (E.D. Tex.).
2. *Alpha and Omega Semiconductor Limited et al v. Force MOS Technology Co. Ltd.*, No.: 5:22-cv-05448 (N.D. Ca.).
3. *Inter partes* review filed by Inergy Technology, Inc., No.: IPR2024-00093 before the Patent Trial and Appeal Board.

Petitioner is not aware of any other pending judicial or administrative matter that would affect, or be affected by, a decision in this proceeding.

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3))

For purposes of this Petition, the following attorneys are lead and back-up counsel for Petitioner:

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BACK-UP COUNSEL
Sean K. Enos Registration No.: 69,468 *SCHMEISER OLSEN & WATTS LLP* 18 E. University Drive, Suite 101 Mesa, AZ 85201 Tel: 480-655-0073 Email: kenos@iplawusa.com

Pursuant to 37 C.F.R. § 42.10(b), Petitioner files herewith a Power of Attorney.

D. Service Information (37 C.F.R. § 42.8(b)(4))

For purpose of this Petition, Petitioner consents to electronic service by email at: jbruce@brucestone.us; kenos@iplawusa.com; and cshih@brucestone.us.

E. Payment of Fees (37 C.F.R. § 42.103)

Petitioner authorizes the United States Patent and Trademark Office (USPTO) to charge the fees set forth in 37 C.F.R. § 42.15(a) for this Petition, including any additional fees that might become due, to Deposit Account No. 601635 (Attorney Docket No. EMC-IPR-001). Petitioner certifies that this Petition complies with the fee requirements of 35 U.S.C. § 312(a)(1).

III. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104

A. Grounds for Standing (§ 42.104(a))

Petitioner certifies, pursuant to 37 C.F.R. § 42.104(a), that U.S. Patent No. 7,629,634 (the "'634 Patent") is available for inter partes review under 35 U.S.C. § 311. Petitioner further certifies that it is not barred or estopped under 35 U.S.C. § 315 or 35 U.S.C. § 325 from challenging the claims identified in this Petition on the grounds set forth herein.

B. Identification of Challenge and Statement of Precise Relief Requested for Each of the Challenged Claims (§ 42.104(b))

Pursuant to 37 C.F.R. § 42.104(b), Petitioner identifies the following grounds of unpatentability and requests cancellation of each challenged claim for the reasons below:

Ground	Challenged Claims	Statutory Basis	Prior Art Reference
1	Claims 1-9	§ 103(a)	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Hshieh ('384)
2	Claims 1-9	§ 103(a)	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Uno ('864)
3	Claims 1-9	§ 103(a)	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Hshieh ('384) in view of Uno ('864) (and *vice versa*)

Petitioner requests that the Board institute inter partes review and issue a final written decision finding each Challenged Claim unpatentable on the stated grounds.

IV. INTRODUCTION TO '634 PATENT

A. The '634 Patent

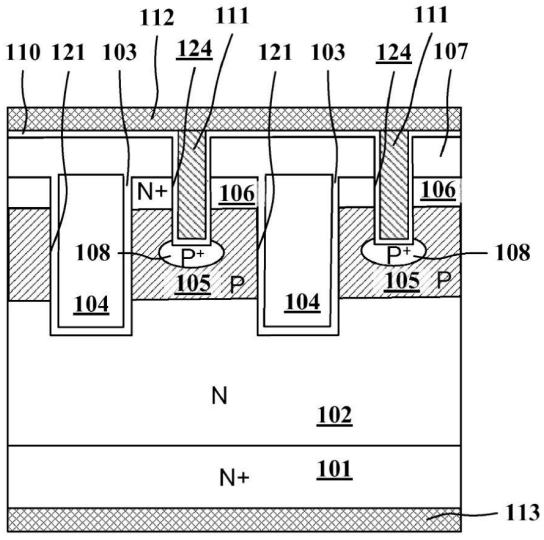
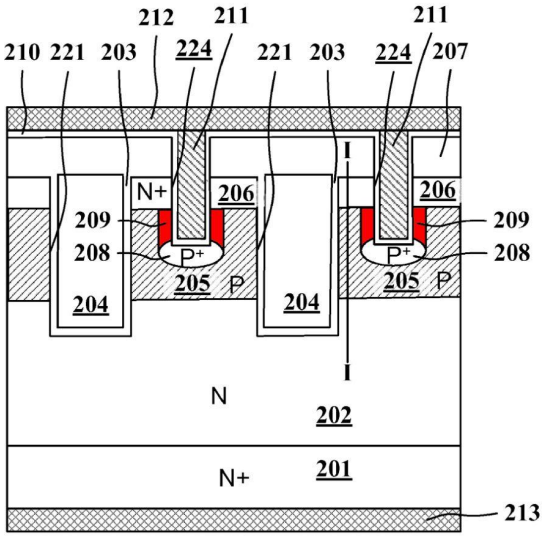
The '634 Patent is directed to trenched MOSFETs. (Ex. 1001, 1:48–50; Ex. 1003 ¶¶127–28.) It improves ohmic contact between the source and channel by reducing base resistance (Rp). Its stated sole allowable feature is the lateral contact layer along the trench sidewalls within the P-type base layer, used with the known prior art base contact layer at the trench bottom. (Ex. 1001, 1:66–2:10, 2:23–26; Ex. 1003 ¶¶131, 147.) The patent has one independent claim (1) and eight dependent claims (2–9) summarized as follows:

- Claim 1: MOSFET structure
- Claims 2 & 6: "lateral contact layer" relative doping concentration
- Claims 3 & 7: barrier metal layer & contact metal plugs
- Claims 4 & 8: tungsten plugs & Ti/TiN barrier metal layer
- Claims 5 & 9: trench shape (vertical or tapered)

The '634 Patent admits sharing the following elements taught by the prior art in FIG. 1: silicon substrate (101/201), drain region/epitaxial layer (102/202),

body region/base layer (105/205), source region/layer (106/206), interlayer oxide film (107/207), base contact layer (108/208), barrier metal layer (110/210), metal contact plugs (111/211), front metal layer (112/212), bottom metal layer (113/213), trenched gates (104/204), and source contact trenches (124/224). (Ex. 1001, 1:5–9, 1:18–41, FIG. 1; Ex. 1003 ¶¶122–23.)

The stated sole allowable structure – "lateral contact layer" (209) – of claim 1 is shown in red in FIG. 2G, illustrating the only difference from the admitted prior art. (Ex. 1001, 3:55–4:6, FIG. 2G; Ex. 1003 ¶122.)

Ex. 1001 ('634 Hsieh)	Ex. 1001 ('634 Hsieh)
	
Fig. 1 (PRIOR ART)	*Fig. 2G (Annotated)*

Dependent Claims 2 & 6 narrow Claim 1 by requiring the "lateral contact layer" (209) have a doping concentration between that of the base contact layer (108/208) and the base layer (105/205). The '634 Patent states this layer ensures

good ohmic contact between the source contact and body region, underscoring its functional importance in the claimed MOSFET:

> "Compared with the conventional trenched MOSFET, the present invention provides good ohmic contact to sidewall [sic] of the source contact…" (Ex. 1001, 2:23–25.)

B. The '634 Patent File History

The '634 Patent was allowed based on the examiner's interpretation of a distinction over Kobayashi—that the lateral contact layer covers the entire sidewall of the source contact trench in the base layer. (Ex. 1002, p. 55.)

V. OVERVIEW OF THE PRIOR ART

Prior art discloses vertical trench MOSFETs with doped source contact trenches where doping extends along the entire trench sidewalls and bottom within the base layer to improve ohmic contact. The '634 Patent calls these doped sidewalls the "lateral contact layer," but the feature was inherently present in the prior art—same location, same function, even if unnamed. Hshieh and Uno both teach doped trench sidewalls within the base layer, teaching Claim 1's structure and, by trench geometry and disclosed fabrication methods, necessarily meeting Claim 2's relative doping limitation.

A. U.S. Patent Publication No. US 2006/0273384 A1 ("Hshieh")

Hshieh, published December 7, 2006, discloses a trench MOSFET nearly identical to that of the '634 Patent. The alleged point of novelty—the "lateral contact layer"—is met by Hshieh's source contact trenches (244) entirely surrounded by a P^+ region (128/228) along trench sidewalls and bottom within the base layer (125/225), providing enhanced ohmic contact to the source plug. This"lateral contact layer" is annotated in medium blue in FIGs. 9G, 9J, and 9G' and supported by Hshieh's fabrication steps.

Ex. 1005 ('384 Hshieh)

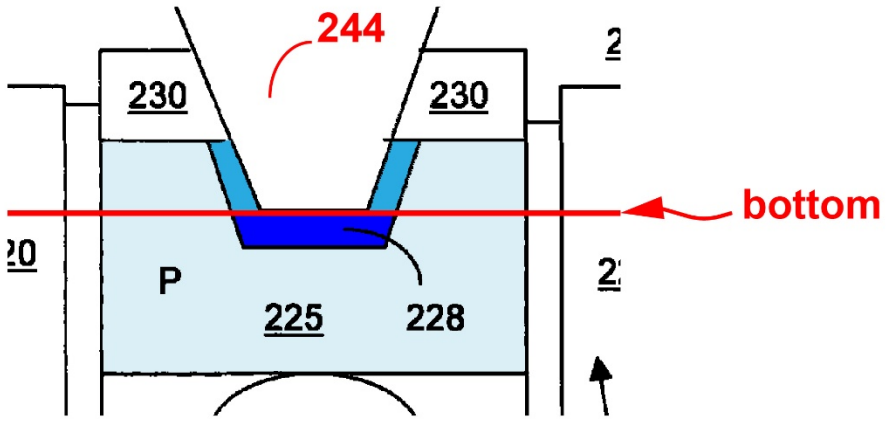


Fig. 9G (Annotated partial enlarged view)

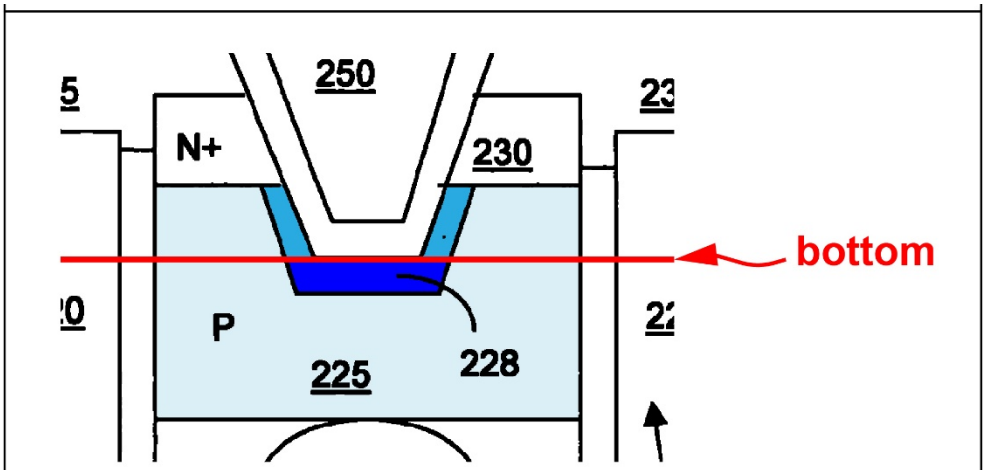


Fig. 9J (Annotated partial enlarged view)

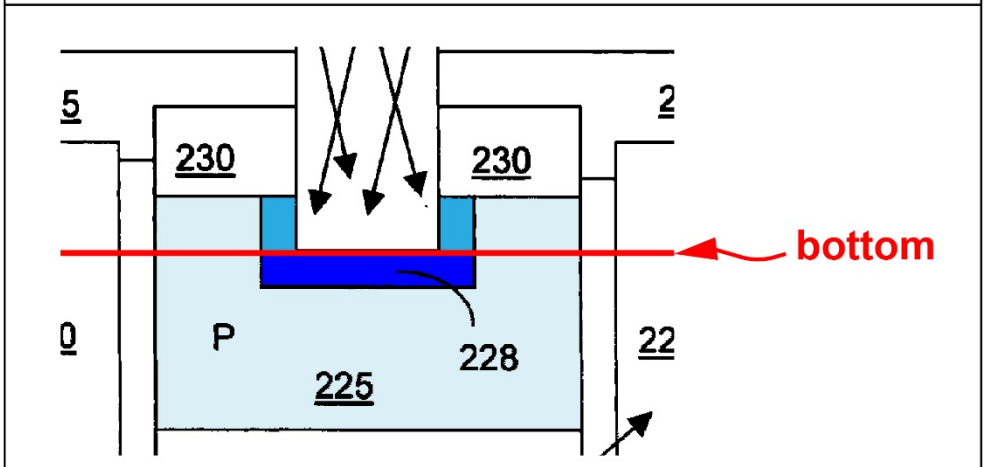


Fig. 9G' (Annotated partial enlarged view)

B. U.S. Patent No. 6,984,864 B2 ("Uno")

Uno, issued January 10, 2006, discloses a trench MISFET nearly identical to that of the '634 Patent. The alleged point of novelty—the "lateral contact layer"—is met by Uno's source contact trenches (21s) fully surrounded by a P^+ region (23) along trench sidewalls and bottom within the body layer (15), providing enhanced ohmic contact between source and base.

Ex. 1006 ('864 Uno)

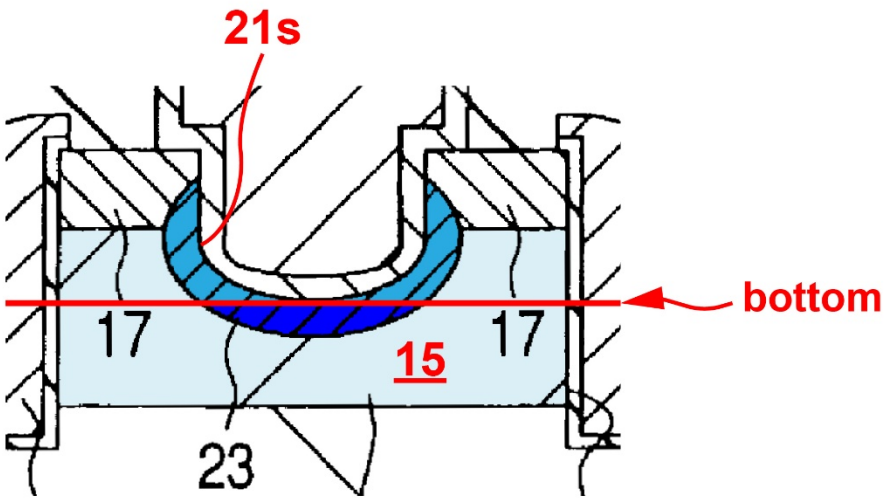


Fig. 38 (Annotated partial enlarged view)

Alone, together, or with POSITA knowledge, these prior art references disclose all claim limitations. The admitted prior art further supports a POSITA's motivation to combine. These references render all claims of the '634 Patent unpatentable under 35 U.S.C.§103.

VI. LEVEL OF ORDINARY SKILL IN THE ART

At the time of the '634 Patent, a POSITA would have had at least a B.S. in electrical engineering or a related field and 2–3 years' MOSFET design or work experience. (Ex. 1003 ¶31.) The Federal Circuit recognizes this as a flexible inquiry, with education offsetting practical experience and vice versa. *See Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007.)

VII. CONSTRUCTION OF THE CLAIMS

A. Independent Claim 1: "the bottom base of said trenches in said base layer"

Based on the specification and file history of the '634 Patent, this claim term should be construed as:

> **"the bottom base of said trenches in said base layer, defined as the region of the base layer located at and below a horizontal plane intersecting the lowest point of said trenches"**

The '634 Patent describes the prior art as a MOSFET wherein "the P+-type region is located **only at source contact trench bottom**." (Ex. 1001, 1:33-35 (*emphasis added*), 2:3-8, FIG. 1 (Admitted Prior Art).) In distinguishing itself from the prior art, the '634 Patent specification describes a MOSFET with a distinct base contact layer and lateral contact layer. "The P+-type base contact layer (208) and the P*-type lateral contact layer (209) are formed **at the bottom** and **sidewall** of the source contact trenches (224), **respectively**." (Ex. 1001, 5:9-12 (*emphasis added*).)

Notably, the '634 Patent explicitly describes the formation process of the base contact layer as "to form a P+-type base contact layer (208) **under the bottom** of the source contact trench (224)" (Ex. 1001, 3:50-55 (*emphasis added*).)

Accordingly, given the description of the base contact layer (108/208) being formed at or beneath the bottom of the source contact trench (124/224), and

considering the patent's explicit contrast with prior art having a P+-type region located only at the bottom, the bottom of the source contact trench (124/224) must necessarily be defined by the boundary separating the trench sidewalls from the trench bottom.

FIG. 2G of the '634 Patent has been annotated in accordance with the patent's teachings. It clearly illustrates the boundary position defining the bottom of the source contact trench (124/224) and the trench sidewall within the base layer (105/205), which together delineate the region the patent owner identifies as the lateral contact layer (209).

Ex. 1001 ('634 Hsieh)

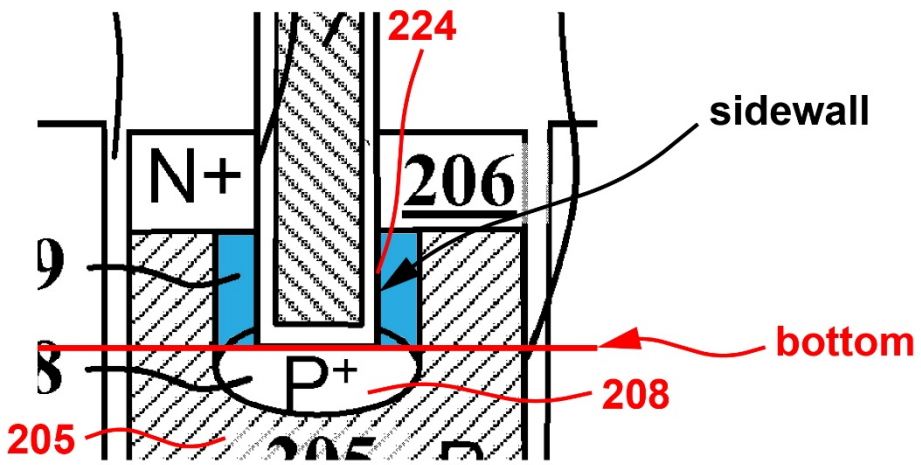


Fig. 2G (Annotated partial enlarged view)

B. Independent Claim 1: "the sidewalls of said trenches in said base layer"

Based on the specification and file history of the '634 Patent, this claim term should be construed as:

> **"the sidewalls of said trenches in said base layer, defined as the portion of said trenches within said base layer above a horizontal plane intersecting the lowest point of said trenches"**

The '634 Patent, Claim 1, explicitly recites that "the sidewalls of said trenches in said base layer are covered by the lateral contact layer." (Ex. 1001, claim 1.) The specification further confirms: "Each of the source contact trenches has a lateral contact layer at a sidewall thereof." (*Id*. at 1:66–67.)

The patent differentiates the claimed invention from the prior art by emphasizing improved ohmic contact along the trench sidewalls:

> "Compared with the conventional trenched MOSFET, the present invention provides good ohmic contact to sidewall [sic] of the source contact…" (*Id*. at 2:23–25.)

By contrast, the prior art is described as lacking such contact due to inadequate doping:

> "The sidewall of source contact trench has no ohmic contact (due to low doping concentration of P base) with the contact metal plug…" (*Id*. at 1:36–37.)

The '634 Patent asserts a distinction between the lateral contact layer (209) and the base contact layer (108/208). It states:

> "The P^+-type base contact layer (108/208) and the P*-type lateral contact layer (209) are formed at the bottom and sidewall of the source contact trenches (224), respectively." (Ex. 1001, 5:9–12).

Additionally, the specification confirms that the base contact layer is "**under the bottom** of the source contact trench (224)." (*Id*. at 3:50–55) (emphasis added).

Because the patent specifies that the base contact layer is positioned at or beneath the trench bottom, it follows that the sidewalls—and thus the lateral contact layer—must be located above the trench bottom, within the base layer (105/205).

VIII. CLAIM-BY-CLAIM EXPLANATION OF GROUNDS FOR UNPATENTABILITY

A. Ground 1: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Hshieh ('384)

1. Independent Claim 1

a. Limitation [1-preamble]

i. [1-preamble-1]

Hshieh discloses a "trenched MOSFET," explicitly describing "[a] trenched metal oxide semiconductor field effect transistor (MOSFET)." (Ex. 1005, Abstract, ¶¶14, 26; Ex. 1003, ¶¶176-77, 179, 181.) This direct disclosure in a preferred embodiment teaches *[1-preamble-1]*. (Ex. 1003, ¶¶181,189.)

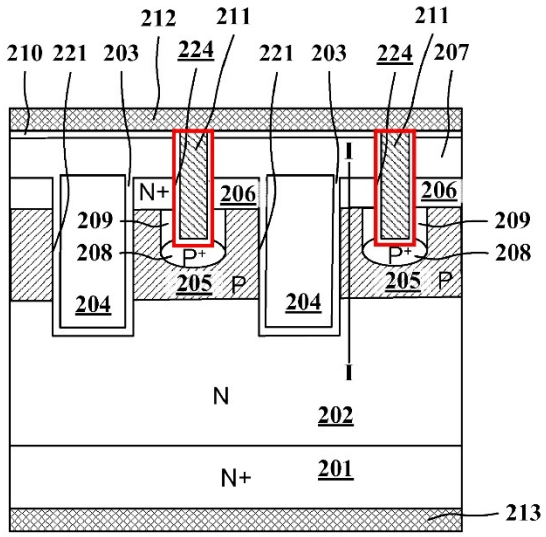
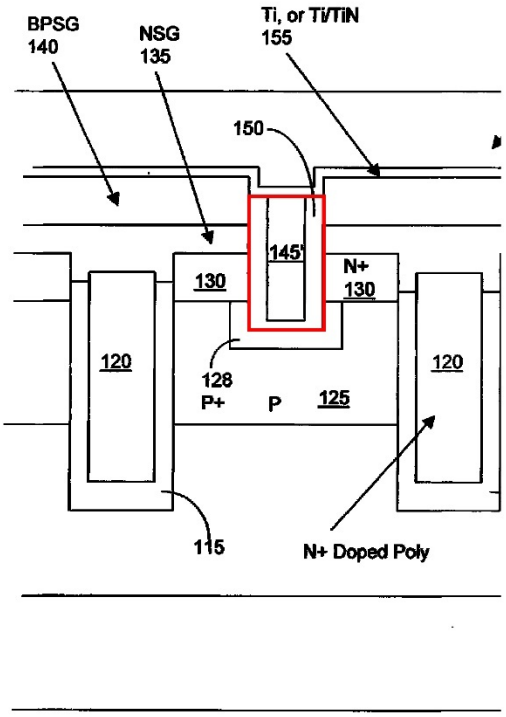
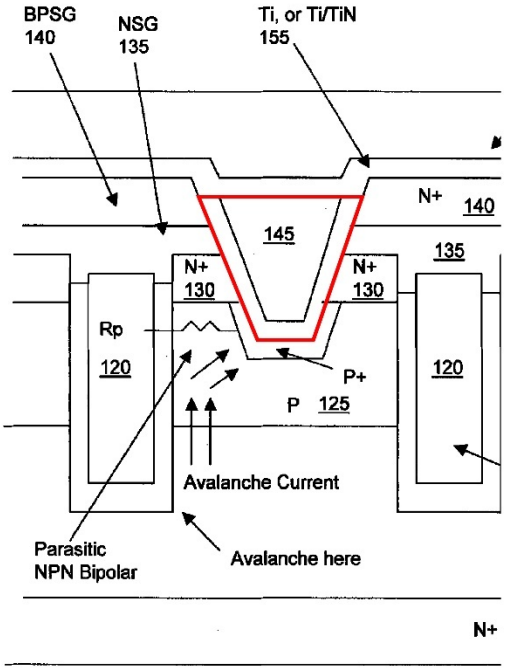
ii. [1-preamble-2]

Hshieh expressly teaches a trenched source contact. (*Id*. ¶¶176, 178-80, 182-89.) Hshieh's Abstract states that the "MOSFET cell further includes a source-body contact trench opened with sidewalls substantially extend vertically relative to a top surface into the source and body regions and filled with contact metal plug." (Ex. 1005, Abstract; Ex. 1003, ¶¶178, 183.) Hshieh also teaches that "a plurality of trenched source contact" are provided "[f]or the purpose of improving the source contact to the source regions 130." (Ex. 1005, ¶27.) The annotated Hshieh figures below illustrate this teaching (Ex. 1003, ¶¶184-89):

<*This space intentionally left blank.*>

[1-preamble-2]

trenched source contact

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

b. Limitation [1a]

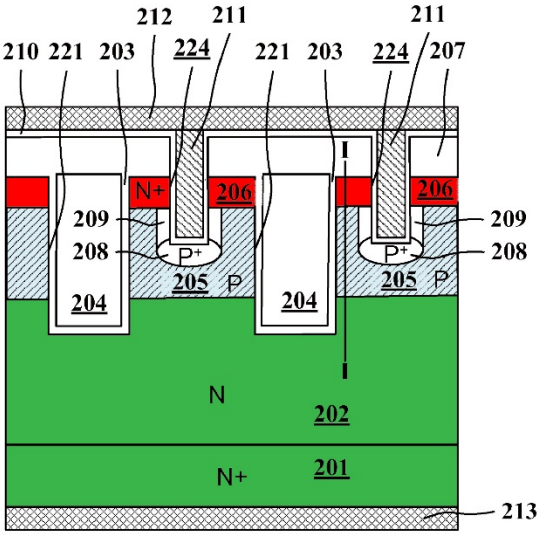
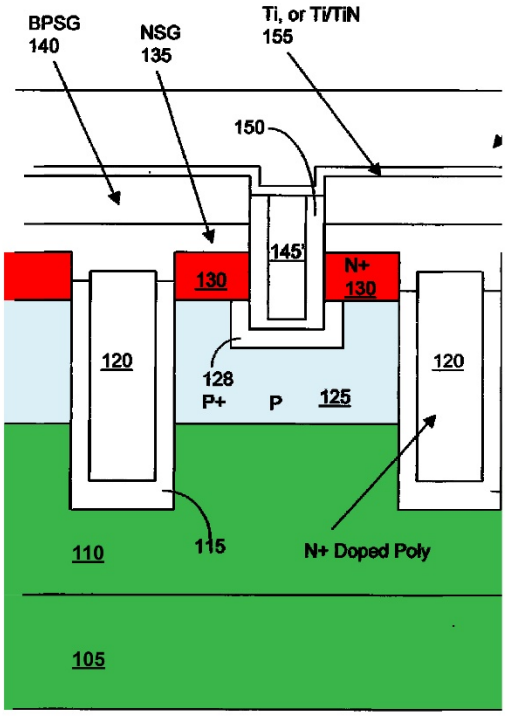
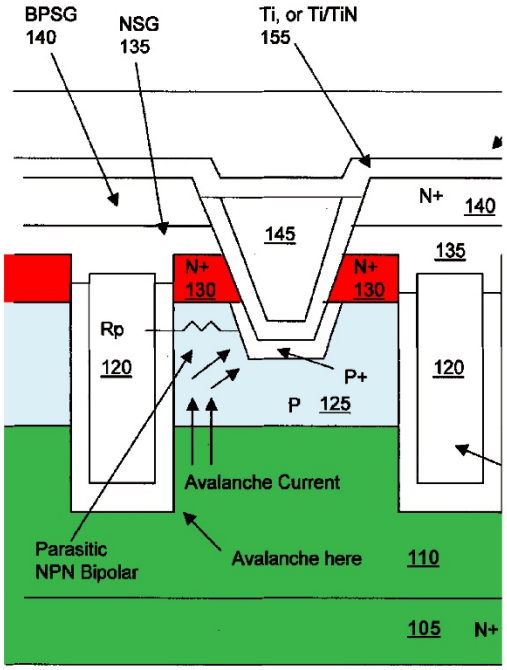
This limitation is addressed in parts.

i. Limitation [1a-1]

1) [1a-1-1]

Hshieh's MOSFET device 100 includes a semiconductor region formed by the N+ substrate 105, N-type epitaxial layer 110, P-body region 125, and source region 130. (Ex. 1005, FIG. 3.) In the annotated figures below, the drain region is shaded green, the body light blue, and the source red. Hshieh describes a semiconductor region comprising a drain, body, and source region, consistent with the '634 Patent's layered structure (101/201, 102/202, 105/205, 106/206). It discloses "an N+ substrate 105 formed with an N epitaxial layer 110," identifying both the substrate and overlying epitaxial layer. (*Id*. ¶26; Figs. 3–8, elements 105, 110; Ex. 1003, ¶194.) Hshieh also describes "an N+ source 130 with a P-body 125 and the N-epitaxial layer 110," identifying the source, body, and drain regions in vertical sequence. (Ex. 1005, ¶¶28–30; Figs. 3–8, elements 110, 125, 130; Ex. 1003, ¶195.) These disclosures confirm that Hshieh teaches *[1a-1-1]*: "semiconductor region." (Ex. 1003, ¶¶193–96.)

[1a-1-1]
semiconductor region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

2) [1a-1-2]

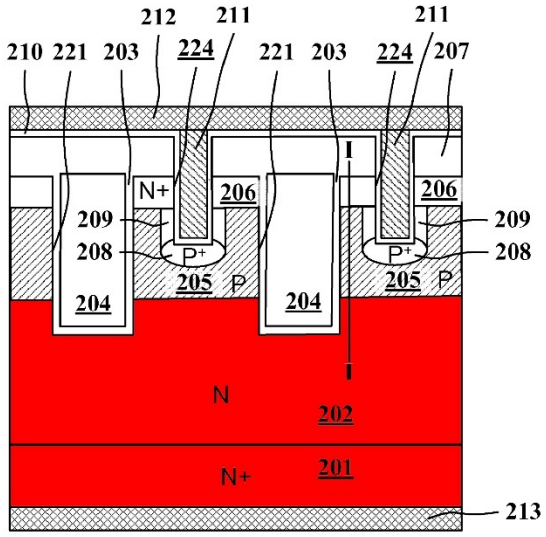
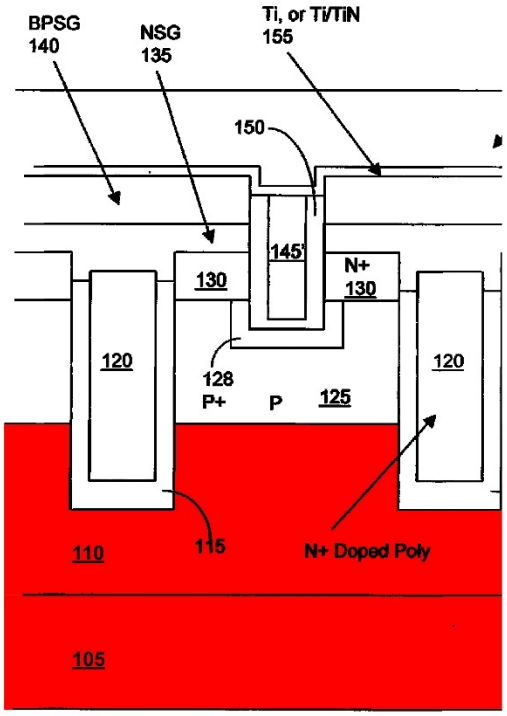
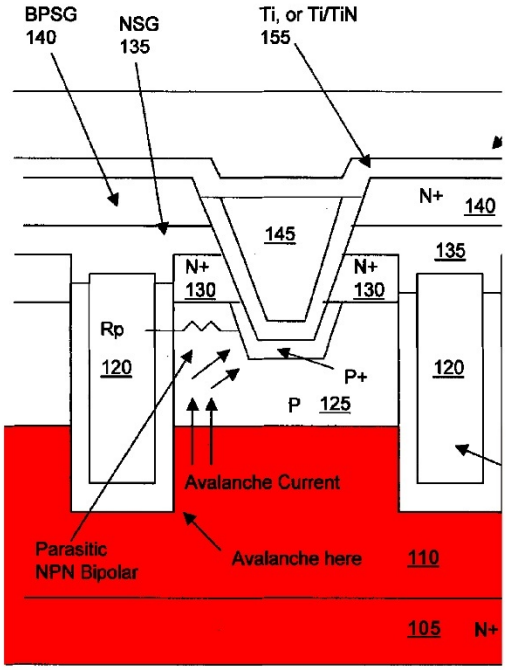
Hshieh discloses a drain region. The ’634 Patent describes the epitaxial layer (102/202) as comprising the drain region, but Claim 1 is ambiguous as to whether the silicon substrate is also included or if the drain is limited to the epitaxial layer. (Ex. 1001, claim 1; Ex. 1003, ¶197.) The cause of this ambiguity is that Claim 1 recites “semiconductor region” having three distinct regions “a drain region, a body region and a source region.” Those regions are then followed by the term "comprising” which introduces an open-ended list of components. Under well-established claim construction principles, each element following the colon must fall within one of the three enumerated regions—i.e., the drain, body, or source regions. However, the claim identifies only the epitaxial layer as “corresponding to said drain region.” No such correspondence is ascribed to the silicon substrate. As written, the claim omits any indication that the substrate belongs to any of the three required subregions. This omission is not corrected elsewhere in the claim.

Regardless, Hshieh discloses both an epitaxial layer and a silicon substrate—whether considered together or separately—thereby teaching a drain region and rendering any semantic ambiguity concerning scope of the drain region moot. (Ex. 1003, ¶197.) Hshieh recites “a drain region disposed on a bottom surface of a substrate” that “extends all the way to the bottom surface of [the] substrate,” indicating a vertical drain structure. (Ex. 1005, claims 1 & 20; ¶¶13, 36; Ex. 1003,

¶198.) It describes "an N epitaxial layer 110" formed on an N^+ substrate 105, together forming the vertical drain path. (Ex. 1005, ¶¶26, 28–30; Figs. 3–8; Ex. 1003, ¶199.) In an alternative embodiment, Hshieh discloses "an epitaxial layer 210" serving the same role. (Ex. 1005 ¶34; Figs. 9A–9G'; Ex. 1003, ¶200.) Both embodiments show an epitaxial layer on an N^+ substrate, consistent with the '634 Patent's vertical drain configuration. (Ex. 1003, ¶200.) Thus, Hshieh teaches an epitaxial layer and substrate forming a continuous vertical conduction path from source to drain, aligning with the plain meaning of "drain region" and disclosing *[1a-1-2]*. (*Id*. ¶¶197-201.)

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[1a-1-2]
drain region

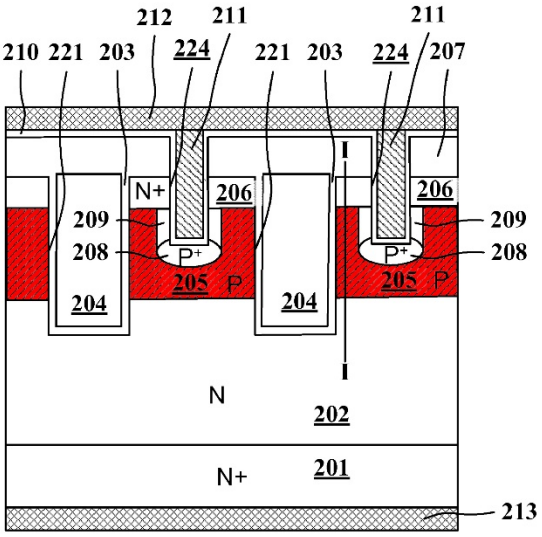
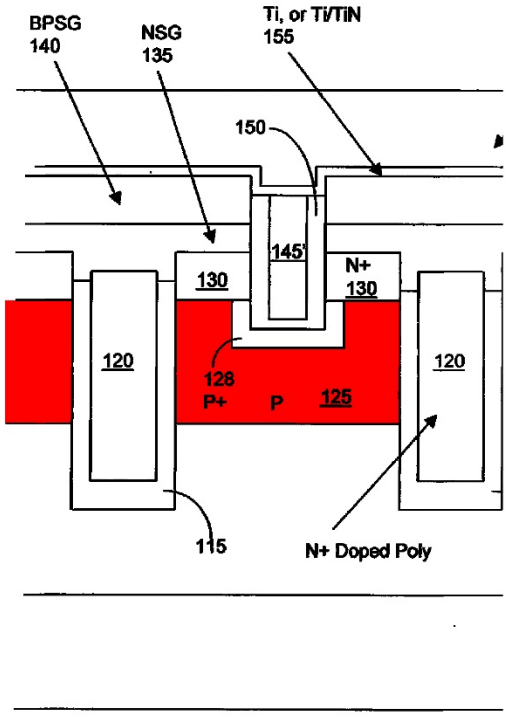
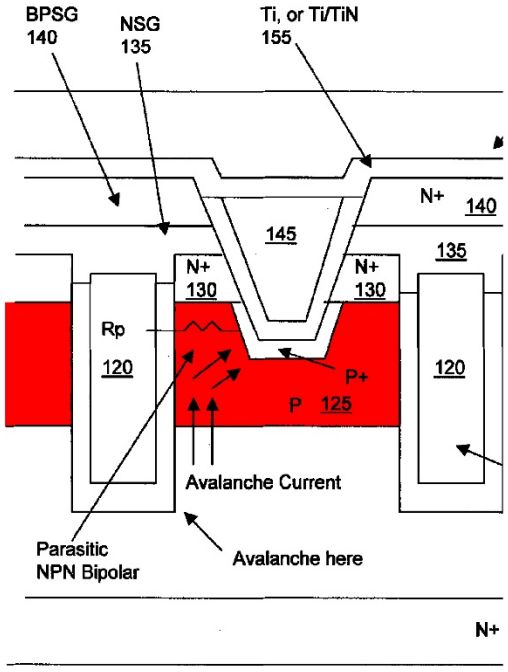
Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

3) [1a-1-3]

Hshieh discloses a base layer corresponding to the claimed body region, consistent with elements 105/205 of the ’634 Patent. (Ex. 1003, ¶202.) It refers to “a body region above a drain region,” indicating its structural placement. (Ex. 1005, ¶¶13–14; FIG. 1, element 25; FIGs. 3–8, element 125; FIGs. 9C–J & G’, element 225; Ex. 1003, ¶203.) The specification identifies “a body region 125” in relation to other device regions. (Ex. 1005, ¶¶26, 27–33; FIGs. 3–8.) In an alternative embodiment, “the body region 225” is similarly identified. (Ex. 1005, ¶¶34–35; FIGs. 9C–J & G’; Ex. 1003, ¶204.) The claim language likewise supports its presence and role. (Ex. 1005, claims 1, 2, 6, 16, 20, 21, 25.) These disclosures confirm that Hshieh describes a P-type body region consistent with the base layer recited in the ’634 Patent, thereby disclosing *[1a-1-3]*. (Ex. 1003, ¶¶202–05.)

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[1a-1-3]
body region

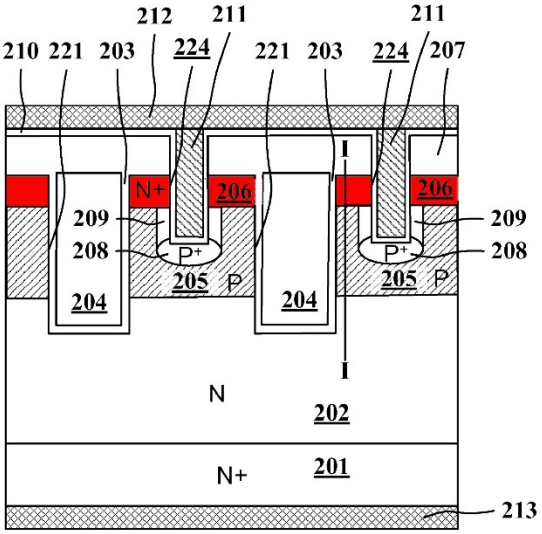
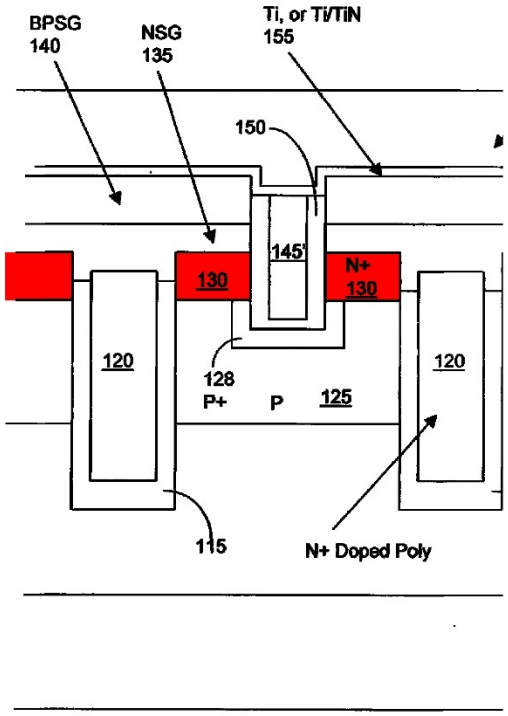
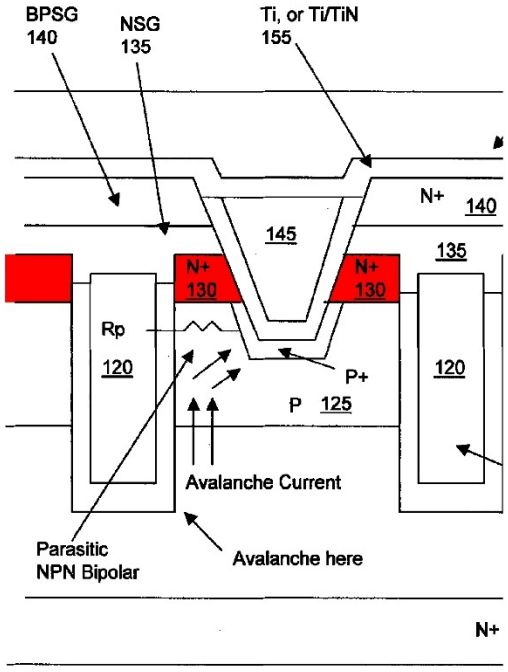
Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

4) [1a-1-4]

Hshieh provides a source region, consistent with element '634-106/206 of the '634 Patent. (Ex. 1003, ¶206.) Hshieh identifies "source region 30" as part of the device structure. (Ex. 1005, ¶¶6–7, 13–14; FIG. 1.) In later embodiments, Hshieh discloses "source regions 130" and "source regions 230," each positioned above the body region and functioning as conduction paths, consistent with the source region in the '634 Patent. (Ex. 1005, ¶¶26, 28–30, 34; FIGs. 3–8, 9D–J & G'; Ex. 1003, ¶207.) Accordingly, Hshieh discloses a source layer corresponding to the '634 Patent's source region and teaching *[1a-1-4]*. (Ex. 1003, ¶¶206-09.)

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[1a-1-4]
source region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

ii. Limitation [1a-2]

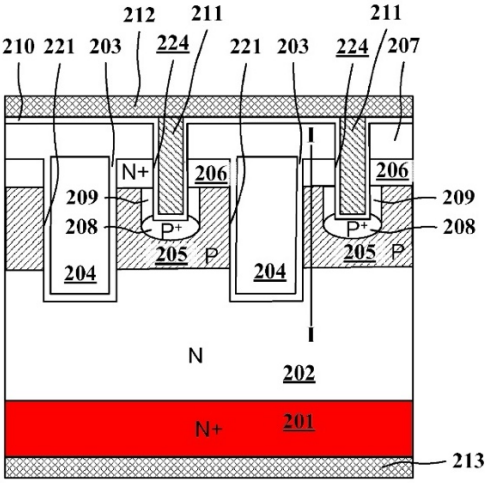
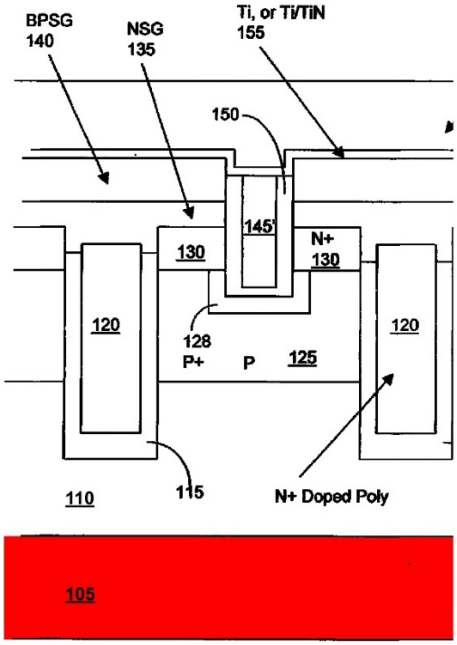
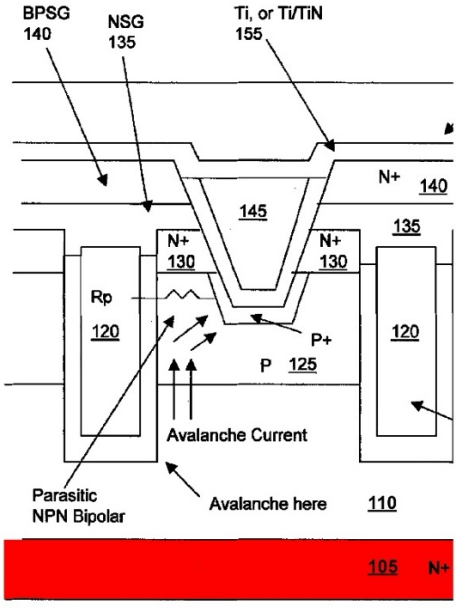
1) [1a-2-1]

Hshieh discloses a semiconductor substrate corresponding to element 101/201 of the '634 Patent. (Ex. 1003, ¶213) Hshieh states that "device 100 is supported on a N^+ substrate 105," identifying the device's foundational substrate. (Ex. 1005, ¶26; FIGs. 3–8.) In another embodiment, "substrate 205" serves the same function. *(* Ex. 1005, ¶34; FIGs. 9A–J & G'; claims 1, 5, 11–14, 20, 24, 27–30; Ex. 1003, ¶213.)

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[1a-2-1]

silicon substrate

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

Although Hshieh does not state substrates 105 and 205 are silicon, a POSITA would understand them as silicon. (Ex. 1003, ¶214.) Such trench MOSFETs were conventionally built on silicon wafers, and absent contrary indication, "semiconductor substrate" means silicon. (*Id*. ¶¶214-15.) Hshieh's N^+-doped substrate with an epitaxially grown N-type layer—typical of silicon-based trench MOSFETs—and its figures showing textbook silicon MOSFET architecture reinforce this. *(Id*. ¶216.)

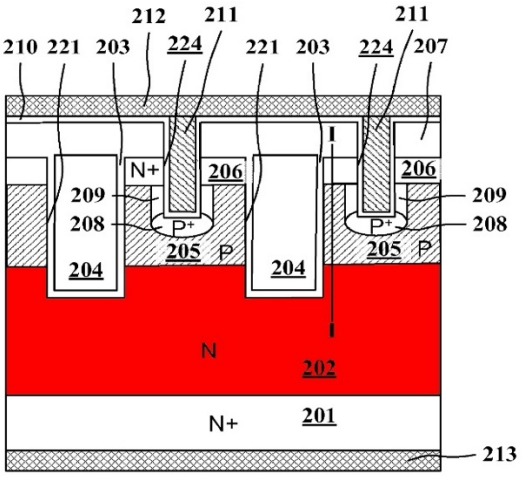
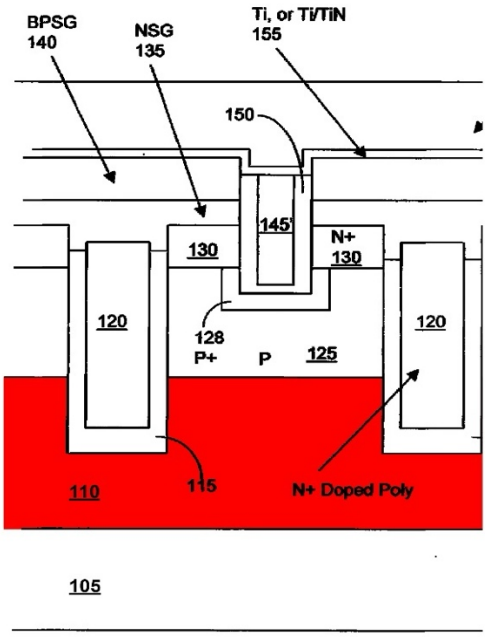
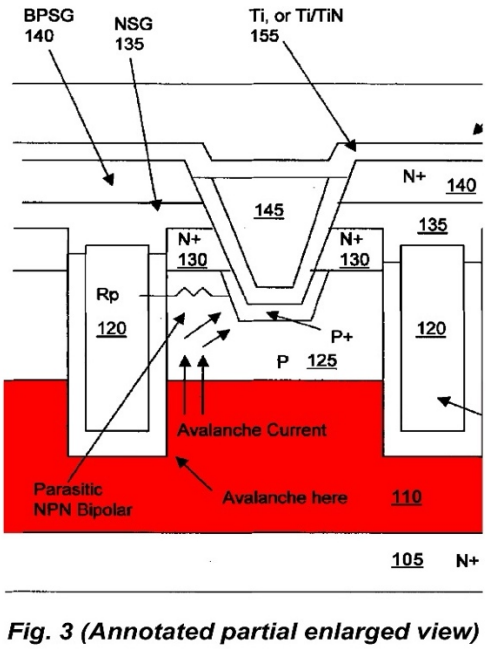
Accordingly, Hshieh discloses a silicon substrate, and teaches limitation *[1a-2-1]*. (*Id*. ¶¶213–17.)

2) [1a-2-2]

Hshieh discloses an epitaxial layer corresponding to the drain region, consistent with element 102/202 of the '634 Patent. (Ex. 1003, ¶218.) Hshieh first identifies "an epitaxial layer 20" as part of the semiconductor structure. (Ex. 1005, ¶6; FIG. 1.) In a preferred embodiment, Hshieh describes "an N+ substrate 105 formed with an N epitaxial layer 110," where the epitaxial layer lies directly above the substrate and forms the lower portion of the semiconductor region. (*Id*. ¶¶26, 28–31; FIGs. 3–8; Ex. 1003, ¶219.) In an alternative embodiment, "an epitaxial layer 210" is similarly disclosed as supported on substrate 205. (Ex. 1005, ¶34; FIGs. 9A–J & G'.) These disclosures confirm that Hshieh provides an epitaxial

layer positioned above the substrate and forming part of the drain region. (Ex. 1003, ¶¶218-21.)

[1a-2-2]
epitaxial layer

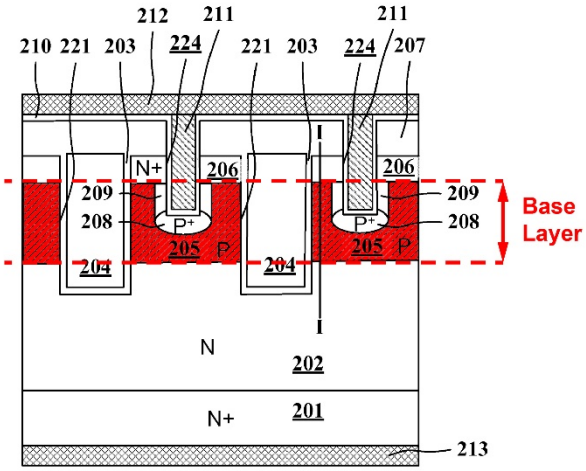
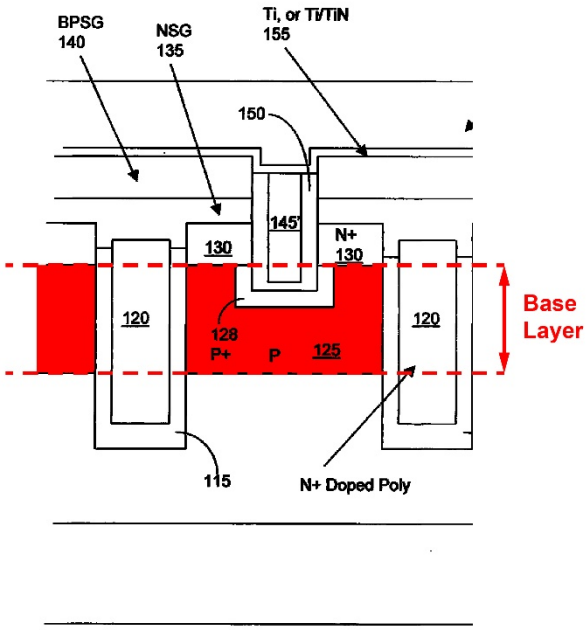
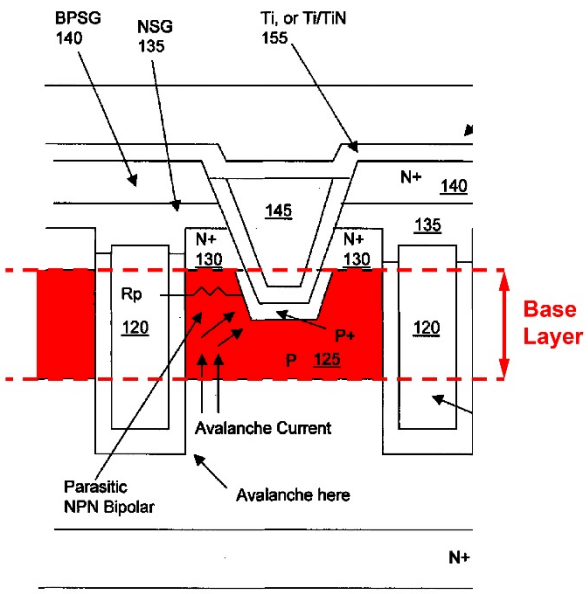
Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

3) [1a-2-3]

Hshieh discloses a body region corresponding to the base layer, consistent with element 105/205 of the ’634 Patent. (Ex. 1003, ¶¶222-24.) It describes in multiple embodiments a P-type body region (25/125/225) located between the epitaxial layer (10/110/210) and source region (30/130/230). (Ex. 1005, ¶¶26–31, 34; FIGs. 3–8, 9C–J & G’; Ex. 1003, ¶¶224–26.) These disclosures confirm that Hshieh provides a P-type base layer functioning as the body region. (Ex. 1003, ¶¶222–27.)

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[1a-2-3]
base layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

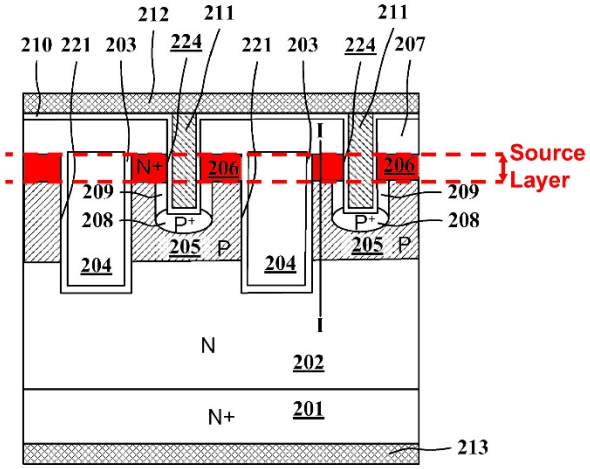
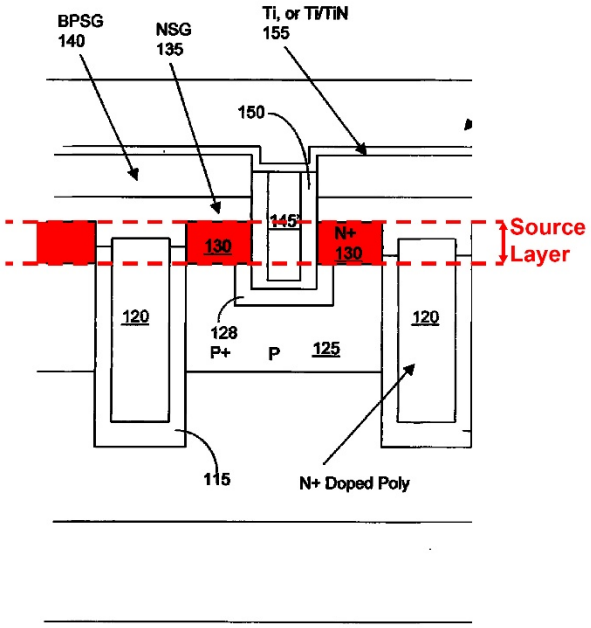
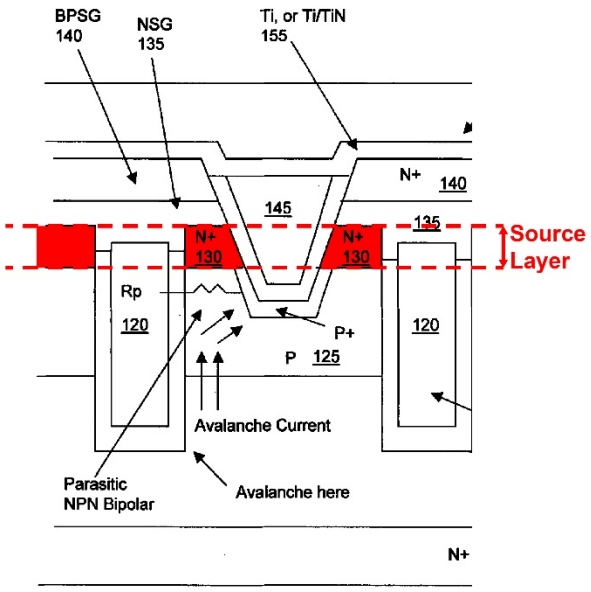
4) [1a-2-4]

Hshieh discloses a source region corresponding to the source layer, consistent with element 106/206 of the ’634 Patent. (Ex. 1003, ¶228.) Hshieh discloses a “body region 25” below a “source region 30,” placing the source above the P-type body layer as required. (Ex. 1005, ¶¶6, 13–14; FIG. 1.) This is consistent in other embodiments, where Hshieh describes “the P-body regions 125 encompass[ing] a source region 130 doped with…,” indicating a highly doped N-type source consistent with the ’634 Patent’s source layer. (*Id*. ¶¶26, 27–28, 34; FIGs. 3–8, 9D–J & G’(element 230); Ex. 1003 ¶¶229–31.)

A POSITA would recognize that Hshieh discloses a source layer (30/130/230) from its structure and doping. (Ex. 1003 ¶¶230-33.) Thus, Hshieh teaches a source layer above the base layer, consistent in placement and doping with the ’634 Patent. (*Id*. ¶¶228–33.)

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[1a-2-4]
source layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

c. Limitation [1b]

Hshieh discloses a front-side metallization structure corresponding to the "front metal layer" (elements 112/212) of the '634 Patent. (Ex. 1003, ¶235.) Specifically, Hshieh identifies element 60/160 as a "top contact layer." (Ex. 1005, ¶¶6, 27; FIGs. 1, 3-8.) This layer is "formed on the upper surface of said semiconductor region," clearly located on the front side of the device, as required by the '634 Patent. (Ex. 1001, claim 1; Ex. 1003, ¶236.) In the annotated figures below, this entire region is marked in red and identified as the front metal layer ('634-112/212), consistent with the scope of Claim 1. (Ex. 1003, ¶236.)

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[1b]

front metal layer

Ex. 1001 ('634 Hsieh)

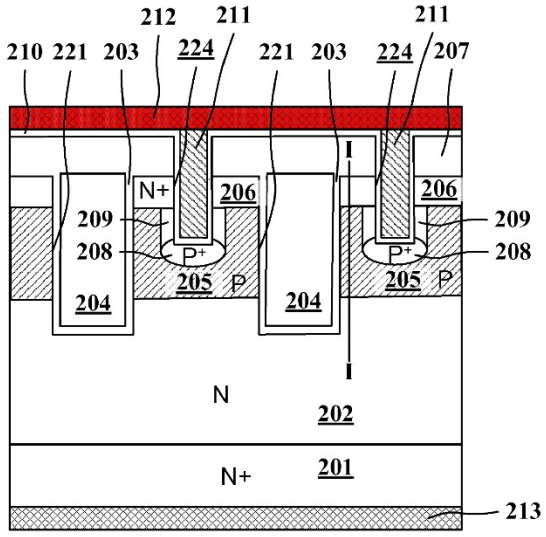


Fig. 2G (Annotated)

Ex. 1005 ('384 Hshieh)

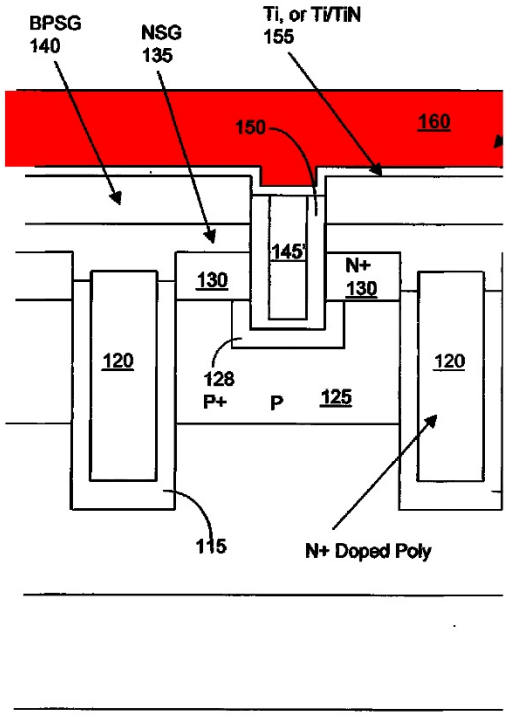


Fig. 4 (Annotated partial enlarged view)

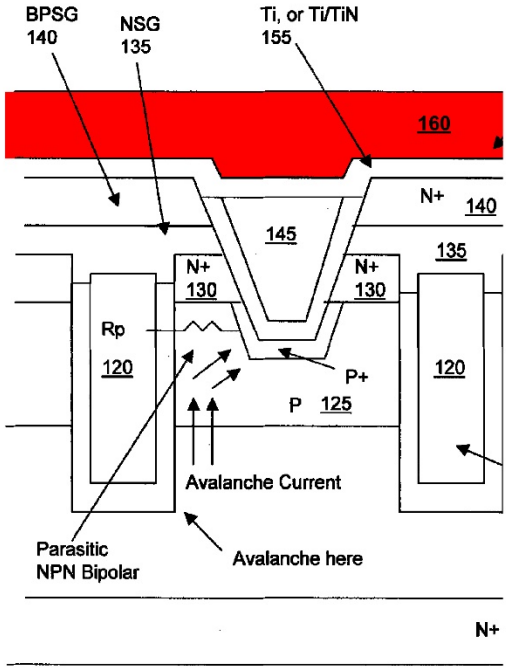


Fig. 3 (Annotated partial enlarged view)

Hshieh further describes the composition of this top contact layer as including aluminum, aluminum-copper, AlCuSi, Ni/Ag, Al/NiAu, AlCu/NiAu, or AlCuSi/NiAu—all standard interconnect materials by 2008. (Ex. 1005, ¶27; Ex. 1003, ¶237.) These same metals are also identified in the '634 Patent for the front metal layer. The '634 Patent states: "The front metal layer (212) is preferably as thick as possible in order to reduce the resistance component of AlSi or AlSiCu." (Ex. 1001, 4:31–33.)

This overlap confirms that the materials disclosed by Hshieh for its top contact layer are consistent with those contemplated for the front metal layer in the '634 Patent. (Ex. 1003, ¶¶237-38.) Hshieh's structure performs the same function and occupies the same position as the claimed front metal layer. Accordingly, Hshieh discloses *[1b]*. (*Id*. ¶¶235-39.)

d. Limitation [1c]

Hshieh discloses an interlayer oxide film corresponding to element 107/207 of the '634 Patent, which recites an insulating oxide layer between the source region and the front metal layer. (*Id*. ¶241.) Hshieh teaches functionally and structurally equivalent dielectric oxide films in multiple embodiments. (*Id*.) For example, it describes contact trenches formed "through the NSG and BPSG protective layers 135 and 140," confirming the presence of insulating layers above the active regions. (Ex. 1005, ¶27; FIGs. 3–8; Ex. 1003, ¶241.) An alternative

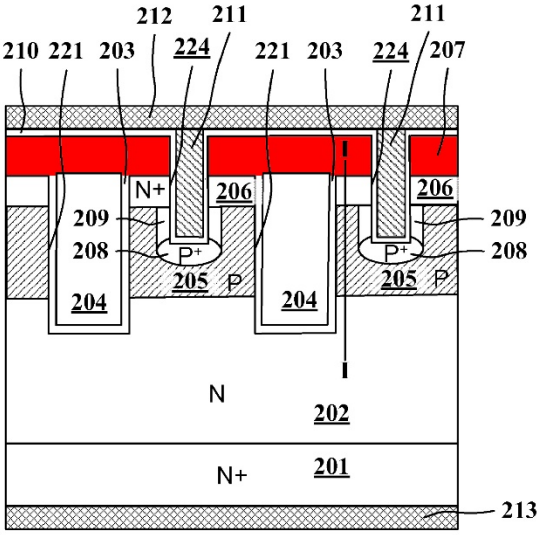
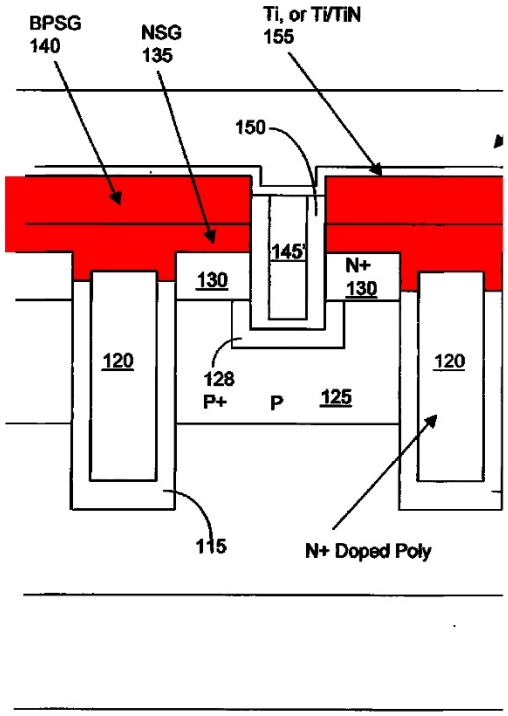
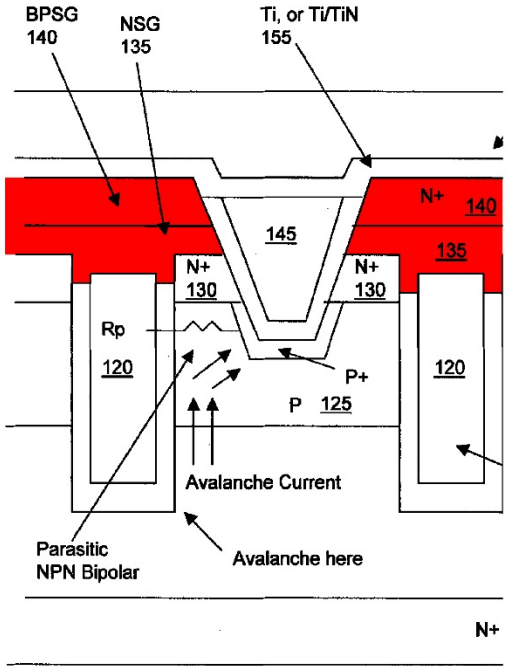
embodiment discloses a "non-doped oxide (NSG) layer 235 and a BPSG layer 240" deposited on the top surface. (Ex. 1005, ¶34; FIGs. 9E–9G'.)

Although Hshieh does not define the acronyms, FIG. 3 labels these layers as "NSG" and "BPSG." As well established in the art, NSG refers to non-doped silicate glass and BPSG to borophosphosilicate glass—both widely used oxide-based insulating materials composed primarily of silicon dioxide (SiO_2). (Ex. 1015, pp. 187–91.) These materials are standard interlayer dielectrics used for electrical isolation in semiconductor devices. (Ex. 1017, p. 1, ¶1.)

A POSITA would have readily recognized these as conventional insulating oxides and understood that Hshieh teaches oxide films positioned between the source region and the front metal layer. (Ex. 1003, ¶242.) The use of one or more such oxides would represent a routine design choice yielding the same functional result as the interlayer oxide film of the '634 Patent. (*Id*. ¶243) Moreover, the admitted prior art in FIG. 1 of the '634 Patent confirms that a POSITA would have been motivated to implement such a structure. (*Id*. ¶243) Accordingly, Hshieh discloses *[1c]*. (*Id*. ¶¶241–43.)

[1c]

interlayer oxide film

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

e. Limitation [1d]

A bottom metal layer formed on the lower surface of the semiconductor region is rendered obvious by Hshieh. (*Id*. ¶244.) Hshieh discloses a drain region disposed on the bottom surface of a substrate. (Ex. 1005, Abstract; ¶¶13–14; claim 1.) The N^+ substrate 105, identified as the drain, is explicitly described as enhancing performance by reducing drain-to-source and spreading resistance. (*Id.* ¶¶31–32.; Ex. 1003, ¶¶245-46.) A POSITA would have understood that forming a low-resistance ohmic contact to the N^+ substrate is necessary, and that the most straightforward and widely accepted method—long established in MOSFET fabrication—is to apply a metal layer to the backside of the substrate. (*Id*. ¶¶247-55.) This backside contact technique has been standard practice since at least the 1960s. (Ex. 1018, p. 330, Fig. 11.8.)

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Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 Fig. 11.8 (1967)

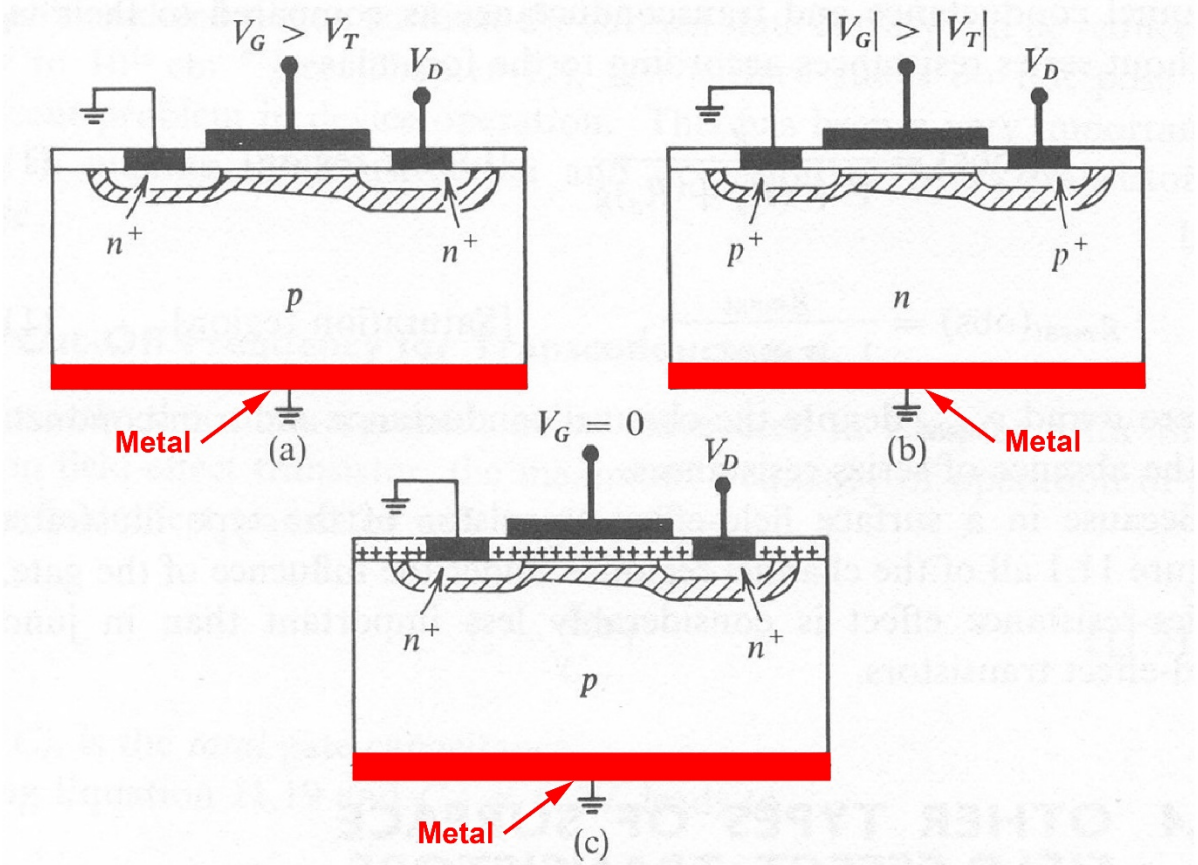


Fig. 11.8 Surface field-effect transistors with field-induced channels.
(a) Normally "off" *n*-channel device.
(b) Normally "off" *p*-channel device.
(c) Normally "on" *n*-channel device.

Fig. 11.8 (Annotated)

While Hshieh does not explicitly illustrate a bottom contact, its absence would not deter a POSITA, who would recognize it as a necessary and obvious implementation detail given the goal of minimizing series resistance in the source-body-drain path. (Ex. 1003, ¶250.) This understanding is reinforced by Hshieh's

emphasis on reducing drain to source resistance (RDS) and the absence of space or trenching support for a top-side drain contact. (*Id*. ¶¶250-263.)

Ex. 1005 ('384 Hshieh)

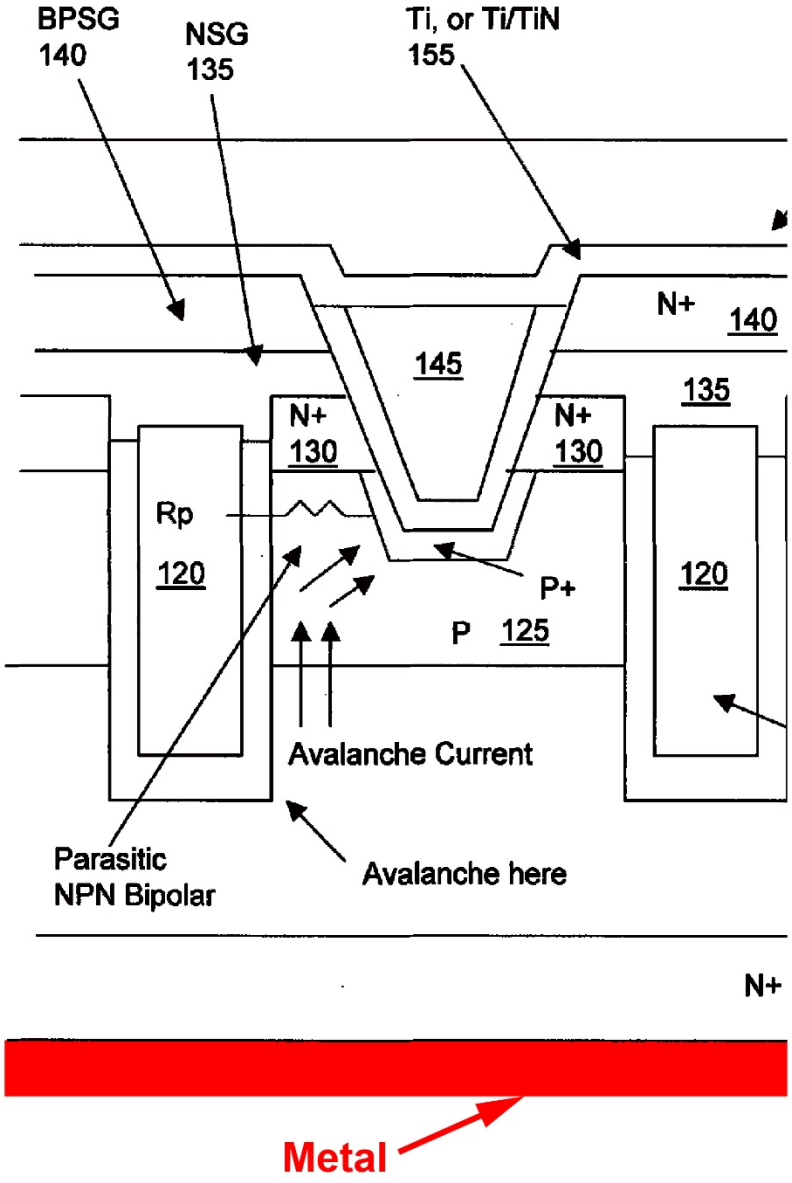


Fig. 3 (Annotated partial enlarged view)

Moreover, the ’634 Patent itself acknowledges the bottom metal layer as conventional. FIG. 1 (Admitted Prior Art) shows a bottom metal layer (element 11) on the lower surface of the substrate. (Ex. 1001, 1:18–41; FIG. 1.) This confirms that such a structure was known and expected in trenched-gate MOSFETs. (Ex. 1003, ¶254.)

Ex. 1001 ('634 Hsieh)

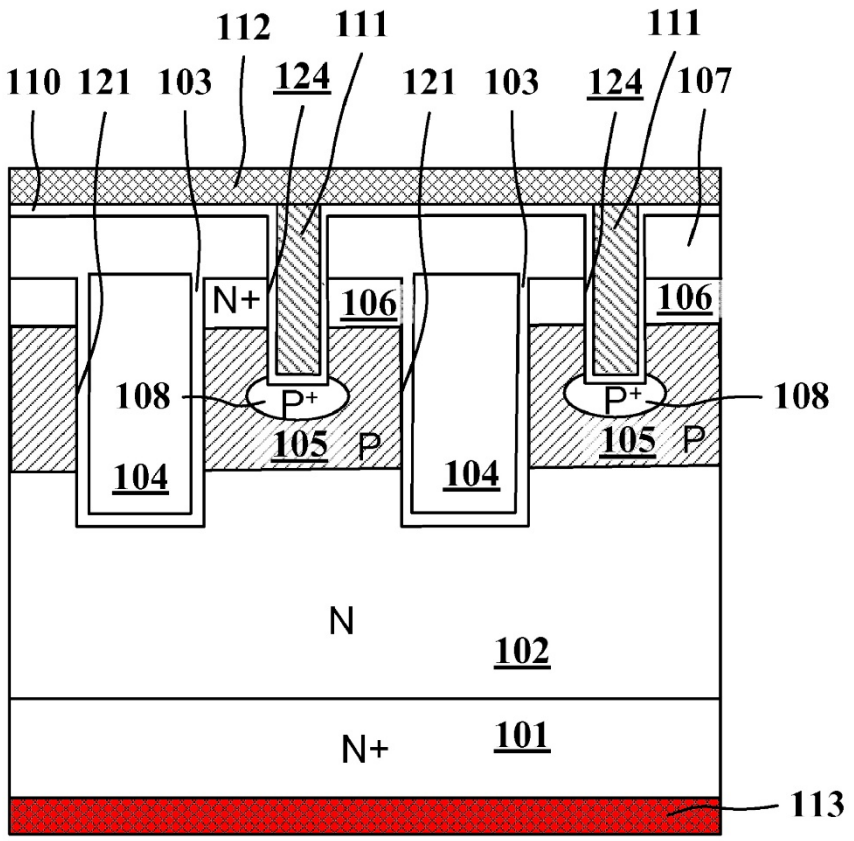


Fig. 1 (PRIOR ART) (Annotated)

Implementing a back-side contact in Hshieh’s structure would have required no inventive skill. (*Id.* ¶¶250-55.) In contrast, adding a top-side drain contact

would introduce complexity, such as deep trenching through multiple layers to reach the N^+ substrate, risking wafer integrity and violating Hshieh's design goal of minimizing resistance. (*Id.* ¶¶256-62.) Hshieh contains no suggestion of such a complex alternative, and a POSITA would favor the simpler, well-established backside metal contact. (*Id.* ¶¶259-63.)

Accordingly, Hshieh, in combination with the knowledge of a POSITA and admitted prior art, renders *[1d]* obvious by disclosing a bottom metal layer formed on the lower surface of the semiconductor region, as recited in the '634 Patent. (*Id*. ¶¶244-64.)

f. Limitation [1e]

Based on the plain and ordinary meaning, element *[1e]* describes the structural arrangement in which a plurality of trenched gates are positioned on top of the source layer and extend downward through the base layer to a portion of the epitaxial layer, with the trenched gates covered by the interlayer oxide film. In the Patent Owner's litigation captioned *Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.), the district court adopted this same interpretation, explaining that "[t]he specification teaches that **the form of the trench gates** in the final device extends from the top of the source layer and through the base layer, which is what the claim language requires." (Ex. 2026, p. 15) (*emphasis added*). The Court further explained that the trench gates were

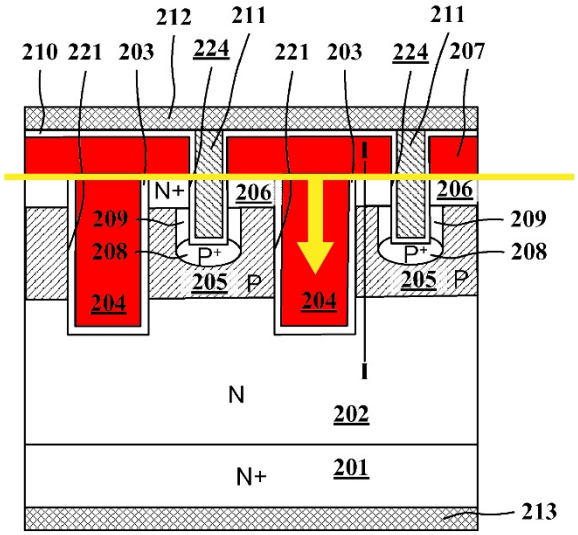
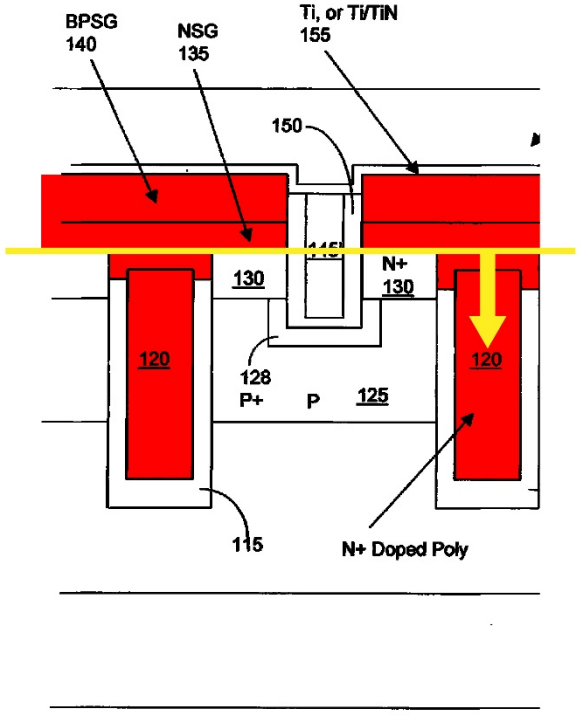
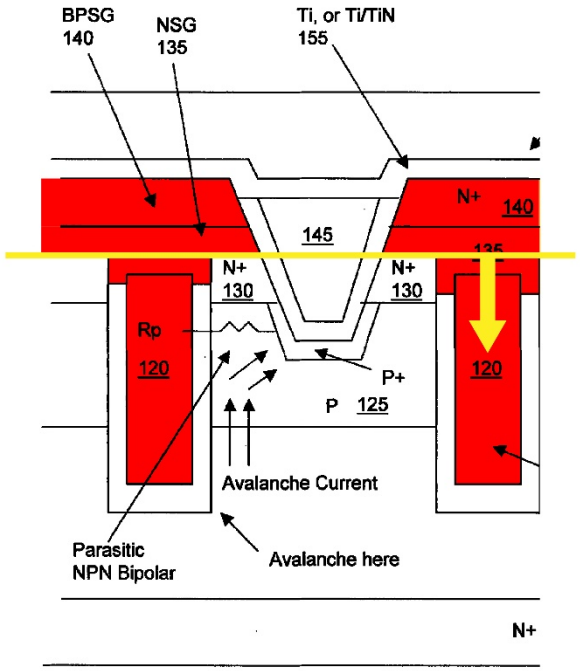
"formed" by etching trenches into the same silicon material that later became the source layer. (*Id*. at 14.) Critically, the Court declined to read into the claim any requirement regarding the height of the gates themselves relative to the top of the source layer, agreeing with Patent Owner's position that the gates need not "extend from above" the source layer. (*Id*.)

Hshieh therefore teaches this claim element. In FIGs. 3–8, the trenched gate structures extend downwardly from above the source region (130/230), through the P-type body region (125/225), and into the N-type epitaxial layer (110/210). (Ex. 1005, ¶¶26, 28, 31; Figs. 3–8, 9C–9J; claim 1; Ex. 1003, ¶268.) Hshieh expressly describes "a trench gate 120 disposed in" the semiconductor body, identifying a vertically extended gate structure integrated within the device. The interlayer oxide film resides above the source layer and covers the trenched gates. This structural relationship matches the plain and ordinary meaning of the claim and is consistent with both Hshieh and the '634 Patent. (Ex. 1003, ¶¶268.)

<*This space intentionally left blank.*>

[1e]

a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

Viewed through the lens of a POSITA's knowledge, it would have been obvious that a MOSFET would include trench gates formed downward through the silicon material—extending through what would become the source and base layers in the final device—and covered by an interlayer oxide film, reaching to a portion of the epitaxial layer so as to provide the function required in a MOSFET. (*Id*. ¶268.) The admitted prior art in FIG. 1 of the '634 Patent confirms that trench gates of this configuration were known and accepted in the art, and would have provided a POSITA with clear motivation to employ the same configuration as taught in Hshieh. (*Id*. ¶269.) Accordingly, Hshieh teaches element *[1e]*. (*Id*. ¶¶267–70.)

g. Limitation [1f]

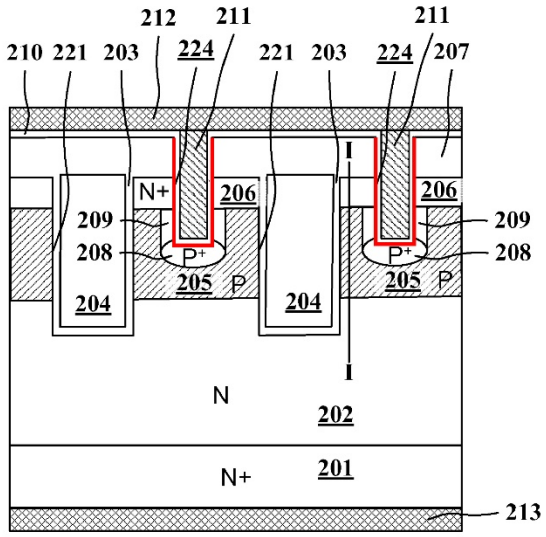
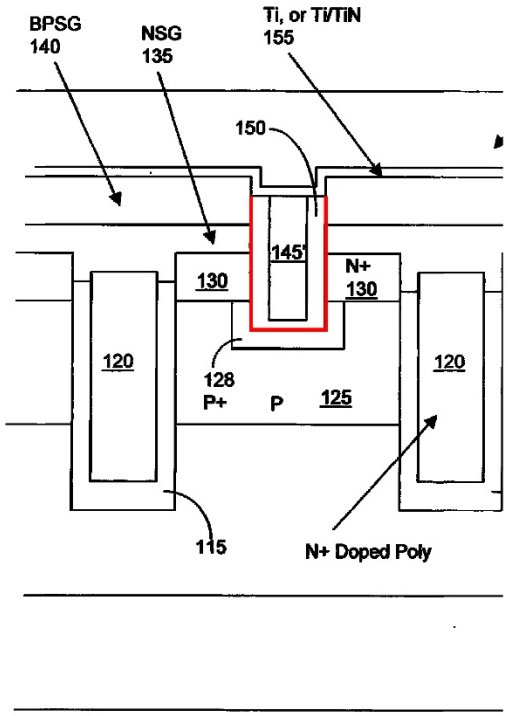
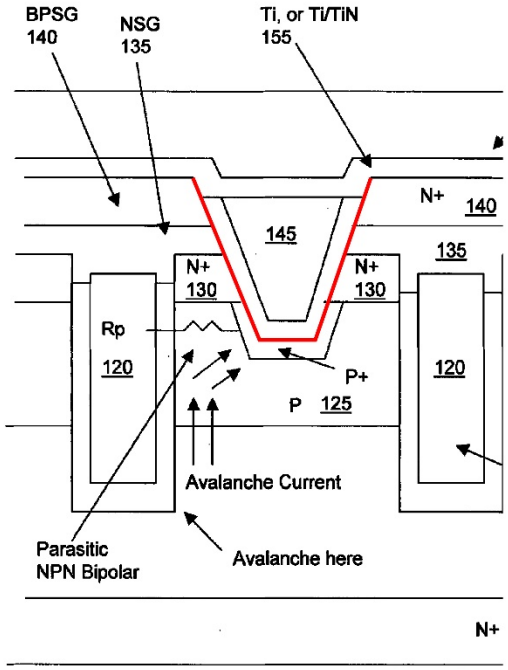
i. [1f-1]

This claim sub-element is taught by Hshieh.

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[1f-1]

a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

Hshieh discloses source contact trenches corresponding to element 124/224 of the '634 Patent. Specifically, Hshieh identifies "contact trenches 244," also referred to as "source-body contact trench 244" in FIG. 9F. (Ex. 1005, ¶¶34-35.) As shown, trench 244 extends downward through the source layer 230 and into a portion of the base layer 225. (Ex. 1003, ¶274.)

Ex. 1005 ('384 Hshieh)

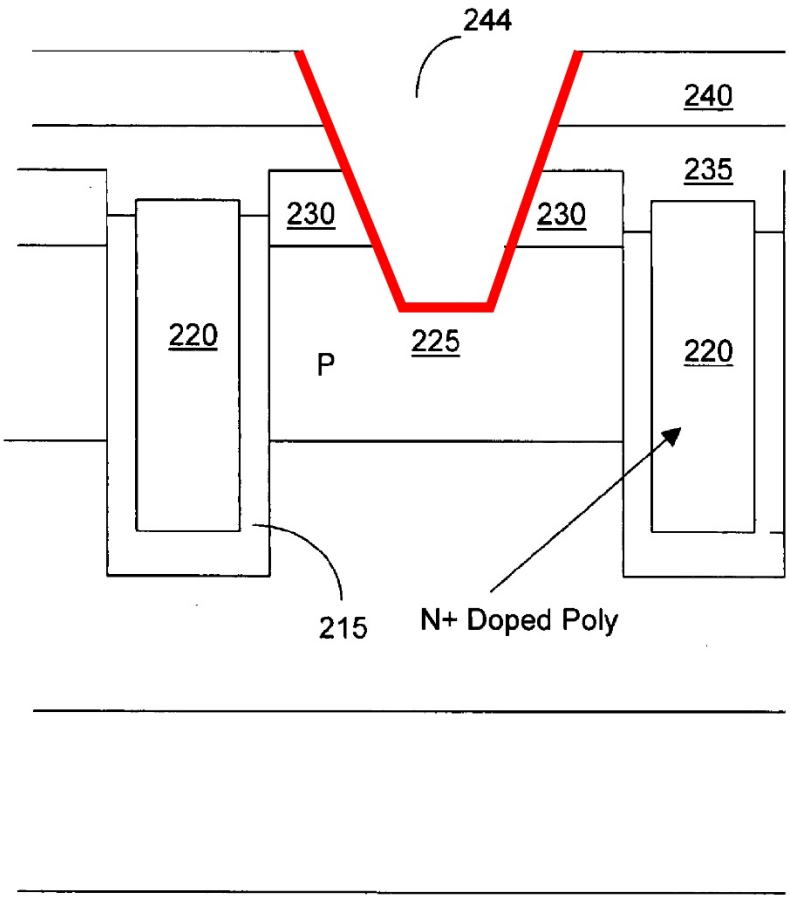


Fig. 9F (Annotated partial enlarged view)

Annotated FIG. 3 further illustrates the relevant layers: elements 135 and 140 are interlayer oxide films, 130 denotes the source regions (within the source layer), and 125 identifies the body regions (within the base layer). (*Id*. ¶275.) These designations are consistent with the structural configuration recited in this limitation.

[1f-1]

a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer

Ex. 1005 ('384 Hshieh)

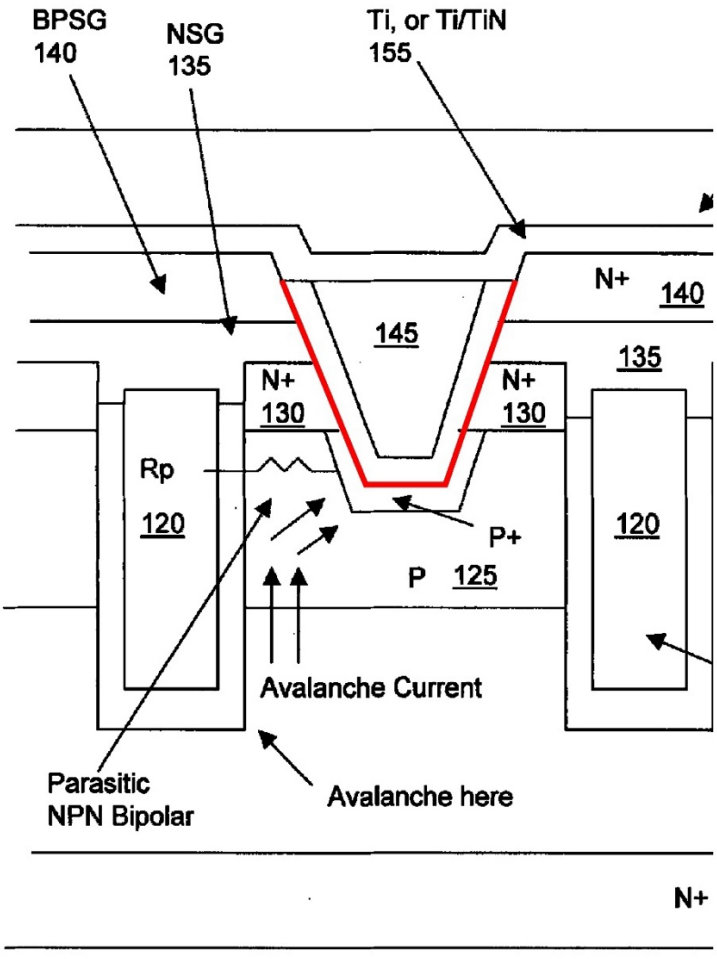


Fig. 3 (Annotated partial enlarged view)

Although the trenches are unnumbered in FIG. 3, they are explicitly referenced in the text and annotated in the reproduced figure. Their numbering absence appears to result from tungsten plug 145 occupying the trench. (*Id*. ¶276.) Nevertheless, Hshieh states that "a plurality of trenched source contact[s] filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is provided to improve contact to the source regions. (Ex. 1005, ¶27.) These repeated structures confirm the presence of multiple source contact trenches. (Ex. 1003, ¶276.)

As shown in FIG. 9F above, these trenches (element 244) are formed through etching directly into the silicon, confirming that they are both "formed on top of the interlayer oxide film" and "extend downwardly through the source layer to a portion of the base layer," as required. (*Id.* ¶277.)

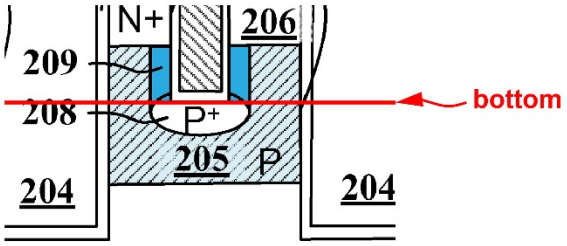
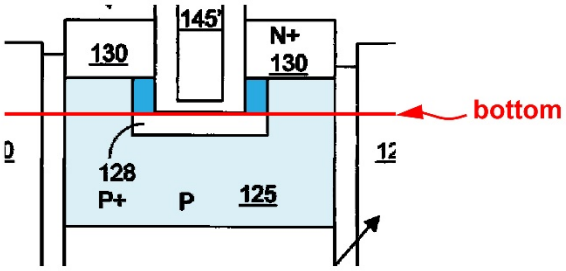
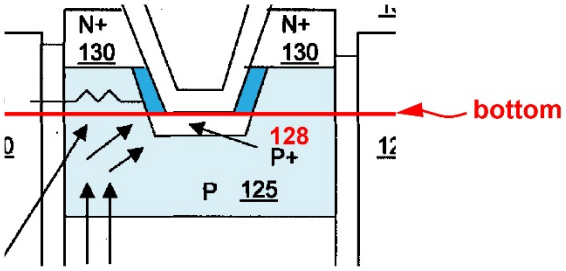
Accordingly, Hshieh teaches the structural features recited in limitation *[1f-1]*. (*Id.* ¶¶273-77.)

ii. [1f-2]

This sub-element is obvious from Hshieh, which identifies P^+-doped regions (128/228) extending along sidewalls and bottoms of source-body contact trenches in the body region (125/225), "surrounding the trenched source-body contact 145." (Ex. 1005, ¶¶28-30, 32-33; Ex.1003, ¶287.) These P^+ regions constitute the "lateral contact layer" as described in the '634 Patent. (Ex. 1005, ¶¶28–30; FIGs. 3–4.)

[1f-2]

wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*  *Fig. 3 (Annotated partial enlarged view)*

Although Hshieh does not subdivide the P^+ region into lateral and bottom components, a POSITA would understand the P^+ region along the trench sidewalls to meet the structural requirements of the claimed "lateral contact layer." (Ex. 1003, ¶279.) The '634 Patent defines this layer as extending from the trench bottom upward along the trench walls within the base layer—precisely as shown and described in Hshieh. (*Id.* ¶280.)

Ex. 1005 ('384 Hshieh)

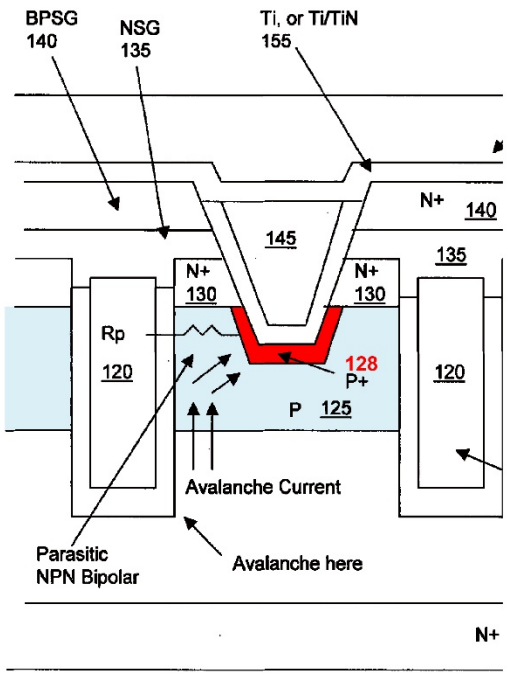


Fig. 3 (Annotated partial enlarged view)

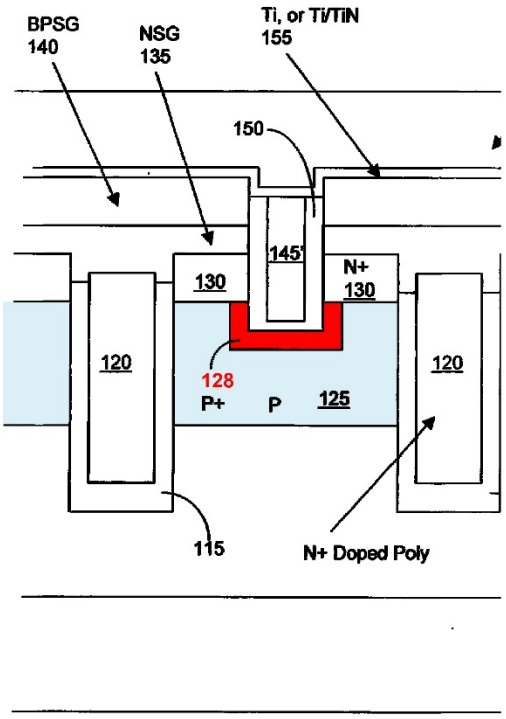


Fig. 4 (Annotated partial enlarged view)

Importantly, the claim imposes no specific dopant concentration, and both "P^+" and "P*" doped layers serve the same purpose—ensuring a low-resistance ohmic contact between the body region and the metal plug. (Ex. 1005, ¶30, Ex. 1003, ¶281.) This practice was well established in the art, as lightly doped regions produce higher contact resistance or undesirable Schottky behavior, which impedes current flow like a diode rather than allowing an ohmic connection. (Ex. 1003, ¶¶282-84.)

Hshieh expressly explains that these heavily doped P^+ regions reduce body resistance (Rp), prevent parasitic bipolar activation, and enable effective avalanche current management. (Ex. 1005, ¶¶18–23, 28–30.) The fabrication steps confirm

this structure: "[T]he sloped trenches allow the formation of heavily doped P^+ regions 128 along both the trench sidewalls and the bottom through zero-degree ion implantation of boron or BF_2." (Ex. 1005, ¶28; Ex. 1003, ¶¶285-86.) In FIG. 4 above, Hshieh describes "the high doped region 128 surrounding the trenched source-body contact 145'," reinforcing the interpretation that the P^+ layer fully covers the trench interface. (Ex. 1005, ¶29; Ex. 1003, ¶289.) As shown in annotated FIG. 9G below, the portion of doped region 128/228 adjacent to the trench sidewall corresponds to the claimed "lateral contact layer," depicted in blue.

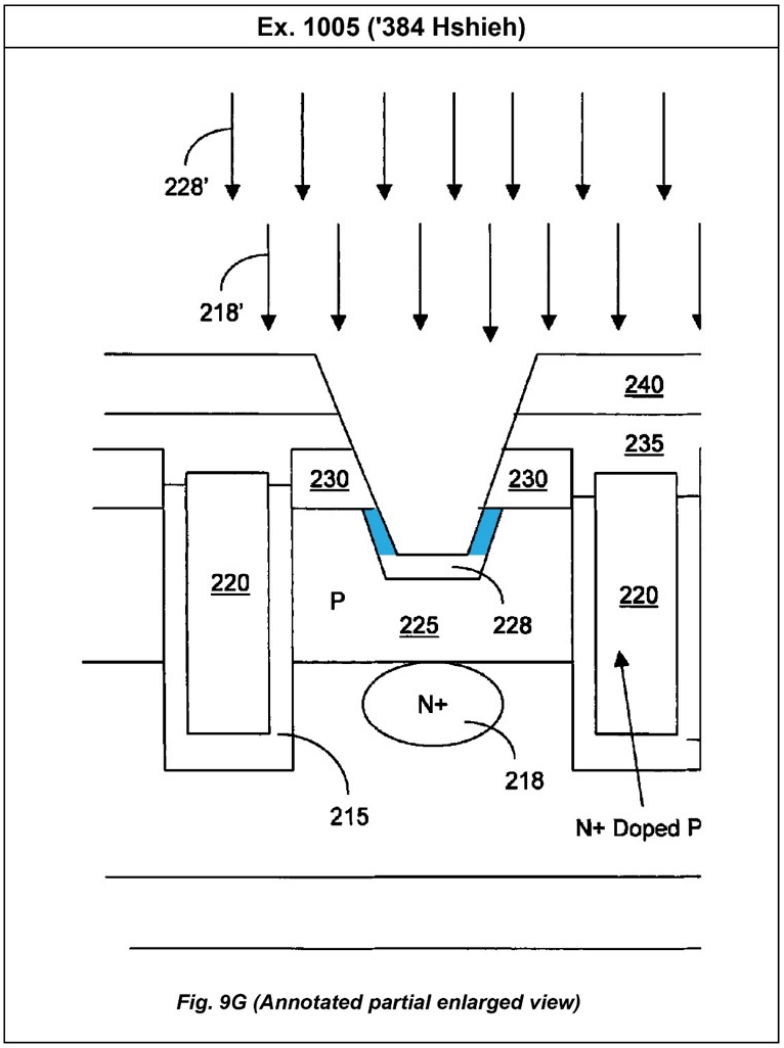
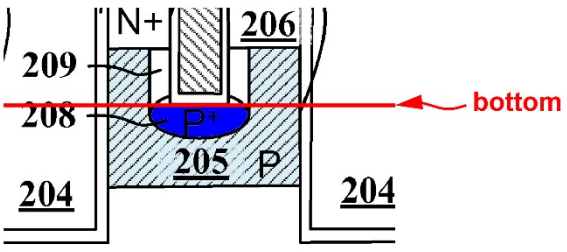
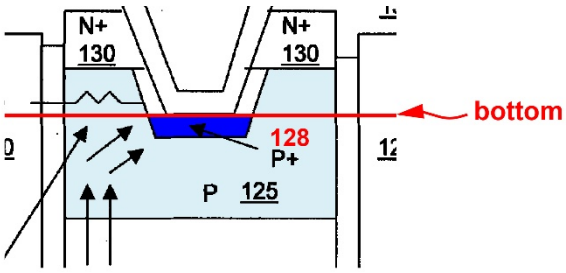


Fig. 9G (Annotated partial enlarged view)

Accordingly, a POSITA would recognize the P^+ region 128/228 as a conventional contact layer, surrounding the contact plug and extending along the trench sidewalls in the body region to form a lateral contact layer—precisely as required by *[1f-2]*. (Ex. 1003, ¶¶279-91.)

iii. [1f-3]

This claim sub-element is taught by, or at least rendered obvious over, Hshieh. Hshieh discloses a P^+-doped region (element 128/228) that extends from the bottom surface of the source-body contact trench, thereby satisfying the structural requirement of a "base contact layer" as defined in the '634 Patent. (Ex. 1005, ¶28; Figs. 3–4; Ex. 1003, ¶293.) Although Hshieh does not label this region as having distinct sub-parts, the portion of the P^+ region annotated in dark blue corresponds to the base contact layer located at the trench bottom. (Ex. 1005, FIG. 3; Ex. 1003, ¶293-94.)

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated partially enlarged view)	*Fig. 3 (Annotated partial enlarged view)*

As explained in the claim construction above, the ’634 Patent defines the base contact layer as the doped silicon at the bottom of the source contact trench, within the body region. Hshieh describes this P^+ region as “surrounding” the source-body contact, which necessarily includes the trench bottom where the contact interfaces with the silicon. (Ex. 1005, FIG. 3*;* Ex. 1003, ¶¶295-96.)

To the extent further explanation is needed, a POSITA would recognize that forming a heavily doped region at the trench bottom—just as at the sidewalls—ensures low-resistance ohmic contact with the body region. (Ex. 1003, ¶284-86, 290.)

Accordingly, Hshieh teaches, or at minimum renders obvious, the structure required by *[1f-3]*. (*Id.* ¶¶392-96.)

2. Dependent Claim 2

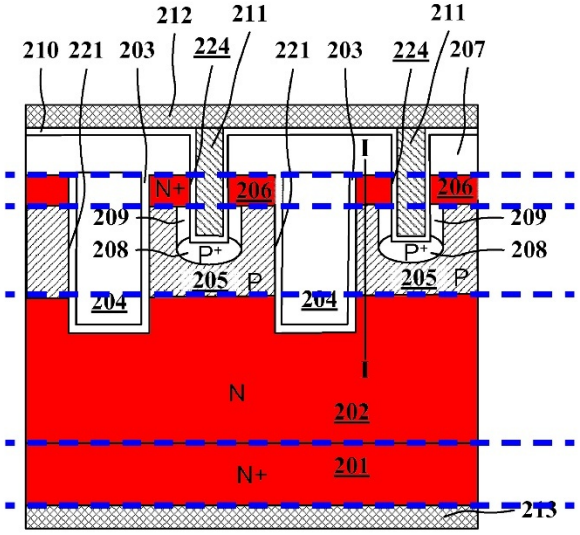
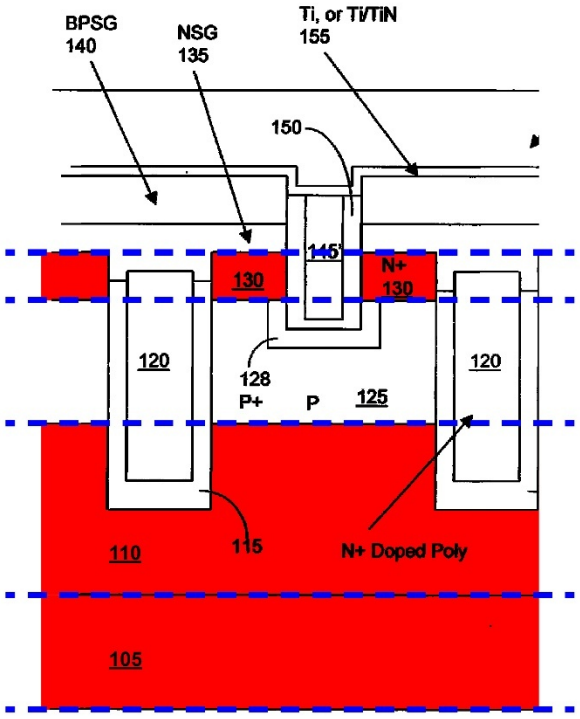
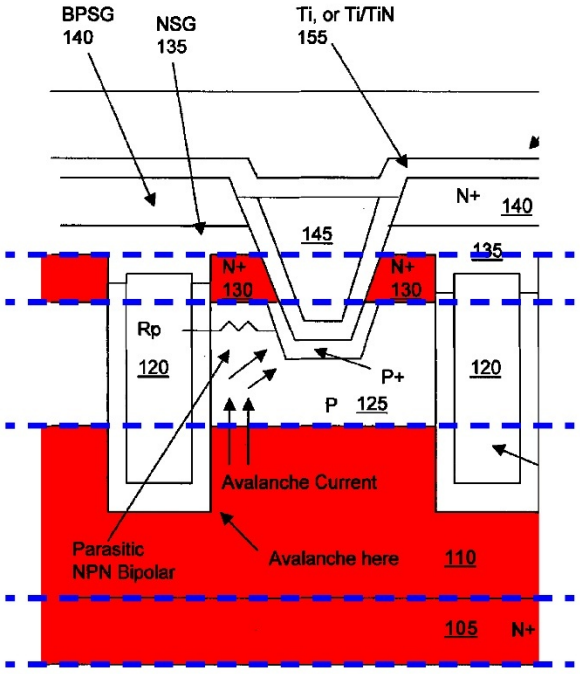
Claim 2 depends on Claims 1 and is taught by Hshieh alone or with POSITA knowledge. (*See* Section VIII.A.1.; Ex. 1003, ¶¶298-351.)

a. Limitation [2a]

Hshieh discloses a device structure comprising an N-type silicon substrate (105), an N-type epitaxial layer (110), and a heavily doped N-type source region (130), corresponding to elements 101/201, 102/202, and 106/206 of the ’634 Patent. (*Id.* ¶¶301-04.)

[2a]

N-type silicon substrate, epitaxial layer, & source layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

In the primary embodiment, Hshieh states that "a N+ substrate 105 [is] formed with an N epitaxial layer 110," identifying both the substrate and overlying epitaxial layer. (Ex. 1005, ¶26; Figs. 3–8, elements 105 and 110; Ex. 1003, ¶315.) The same vertical arrangement appears in an alternative embodiment using substrate 205 and epitaxial layer 210. (Ex. 1005, ¶34; Figs. 9A–G'.)

Above the N-type epitaxial layer and P-body, Hshieh discloses a heavily doped N^+-type source region. (Ex. 1003, ¶305.) This region appears as "source region 30" in the introductory embodiment (Ex. 1005, ¶6; FIG. 1, element 30), and as elements 130 and 230 in subsequent embodiments. (*Id.* ¶¶26, 28–30, 34; Figs. 3–8, element 130, 9D–J, 9G', element 230; Ex. 1003, ¶305-06.) These source regions are formed above the P-body and are consistent with standard N^+-type source structures described in the '634 Patent. (Ex. 1003, ¶306.)

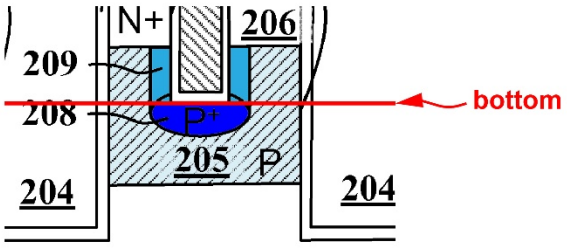
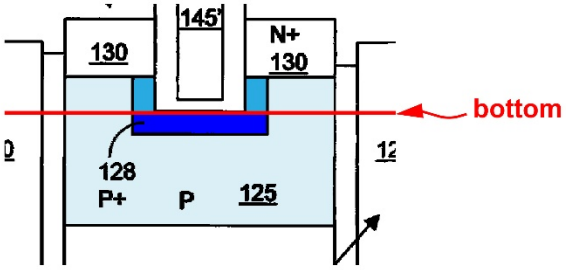
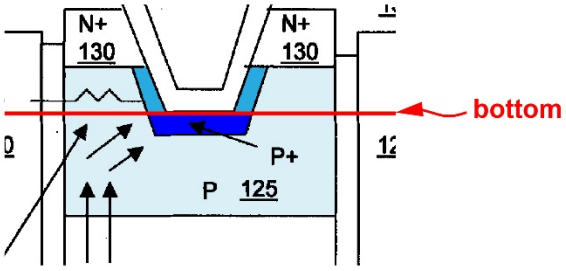
Accordingly, Hshieh teaches the full N-type semiconductor structure required by *[2a]*. (*Id*. ¶¶301-07.)

b. Limitation [2b]

Hshieh teaches both a P-type base layer and a P-type lateral contact layer, corresponding to elements 105/205 and 209 of the '634 Patent.

[2b]

P-type base layer & lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*  *Fig. 3 (Annotated partial enlarged view)*

The ’634 Patent identifies the P-type base layer as the structural source of the MOSFET’s body regions. (Ex. 1001, 5:1–2.) Hshieh discloses this base layer as the precursor to the P-body regions formed during trench etching. (Ex. 1003, ¶308.) In the first embodiment, this is referred to as “a P-body region 25.” (Ex. 1005, ¶6; FIG. 1, element 25.) In the alternative embodiments, Hshieh describes “P-body 125” and “P-body 225” formed by boron implantation into the upper portion of the epitaxial layer. (*Id.* ¶¶26-34; Figs. 9C–G’, element 125/225.)

Hshieh also discloses a P^+-type doped region along the sidewalls of the source contact trench. (Ex. 1003, ¶309.) It states that “the P^+ doped region 228 [is]

to surround the trenches 224," forming a low-resistance ohmic contact with the base. (Ex. 1005, ¶¶35-36; Figs. 9G–G'.) This corresponds to the "lateral contact layer" ('634-209) of the '634 Patent, which is defined as extending along the trench sidewalls, distinct from the base contact layer at or beneath the trench bottom. (Ex. 1001, 3:50–55; 5:9–12; Ex. 1003, ¶¶309-10.)

Accordingly, Hshieh discloses both a P-type base layer and a lateral contact layer and teaches *[2b]*. (Ex. 1003, ¶¶308-11.)

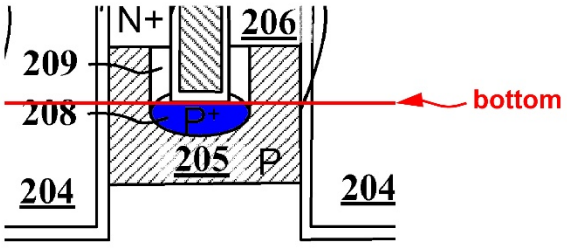
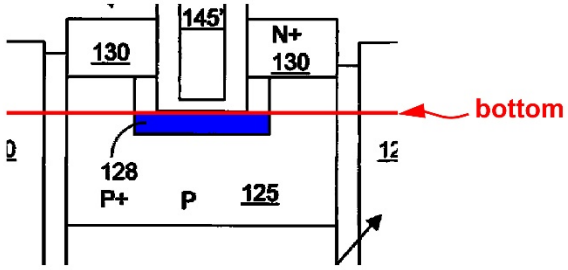
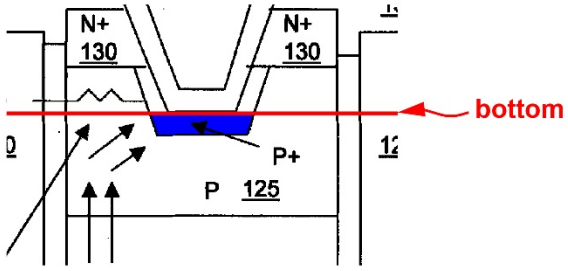
c. Limitation [2c]

Hshieh discloses a P-type base contact layer corresponding to element 108/208 of the '634 Patent, formed at the bottom of the source contact trenches (124/224). (*Id*. ¶312.) The '634 Patent describes this layer as being located at or beneath the trench bottom to enable low-resistance ohmic contact to the deeper P-type base. (Ex. 1001, 3:50–55; 5:9–12.)

<*This space intentionally left blank.*>

[2c]

P-type base contact layer at bottom of source contact trenches

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

Hshieh teaches a functionally equivalent structure. (Ex. 1003, ¶312-14.) It states that "the P^+ doped region 228 [is] to surround the trenches 224," confirming that region 228, and its alternative embodiment region 128, extends along both the trench sidewalls and the trench bottom. (Ex. 1005, ¶¶28-30, 32-33, 35–36; Figs. 3-4, 6-7, element 128, Figs. 9G–G' element 228.) Although Hshieh does not explicitly subdivide region 128/228, the use of "surround" and the trench-bottom depiction in the figures make clear that this region provides ohmic contact at the trench floor. (Ex. 1003, ¶315.)

This aligns with the structural distinction in the ’634 Patent between the lateral contact layer (on trench sidewalls) and the base contact layer (at the trench bottom). Region 128/228, in contact with the underlying P-body 125/225, satisfies both the location and function of the claimed base contact layer. (*Id*.)

Accordingly, Hshieh teaches a P-type base contact layer formed at the trench bottom, disclosing *[2c]*. (*Id*. ¶¶312-16.)

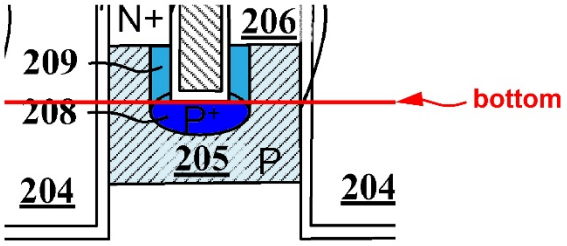
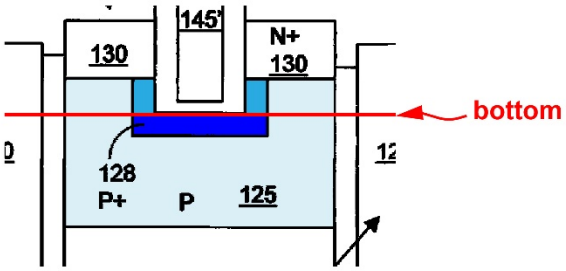
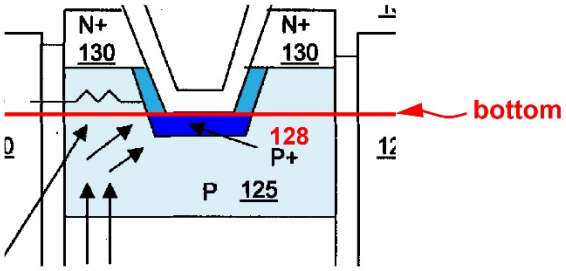
d. Limitation [2d]

This claim sub-element is rendered obvious by Hshieh. As discussed in *[1f-2]* and *[1f-3]*, Hshieh discloses a P^+-doped region (element 128/228) that surrounds the source-body contact trench (element 244/244’/224), extending along both the sidewalls and the trench bottom. (Ex. 1005, ¶¶35–36; FIGs. 9G–G’.) This region corresponds to the lateral contact layer (sidewalls) and base contact layer (trench bottom) of the ’634 Patent. (Ex. 1001, 3:50–55, 5:9–12; Ex. 1003, ¶318)

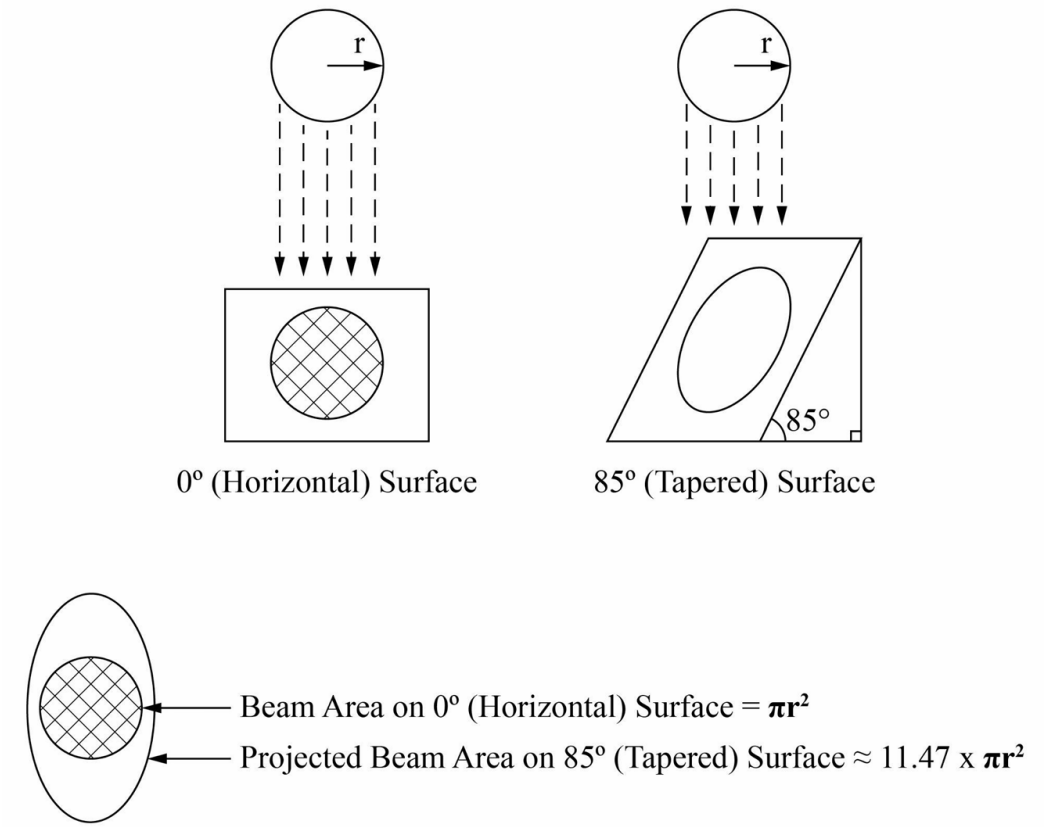
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[2d]

lateral contact layer has less doping concentration than the base contact layer at bottom

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated partially enlarged view)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

While Hshieh does not quantify doping levels separately, it describes a perpendicular ("zero-degree") ion implantation of boron or BF_2 into a trench with sloped sidewalls. (Ex. 1005, ¶35; Ex. 1003, ¶¶320-22.) A POSITA would recognize that the angle of incidence on sloped trench walls causes the ion flux to spread over a larger area, reducing dopant concentration per unit surface area compared to the trench bottom, where ions strike perpendicularly. (Ex. 1003, ¶¶323-51.) This fundamental geometric principle, as explained by Dr. Foty, is illustrated in the diagram below:

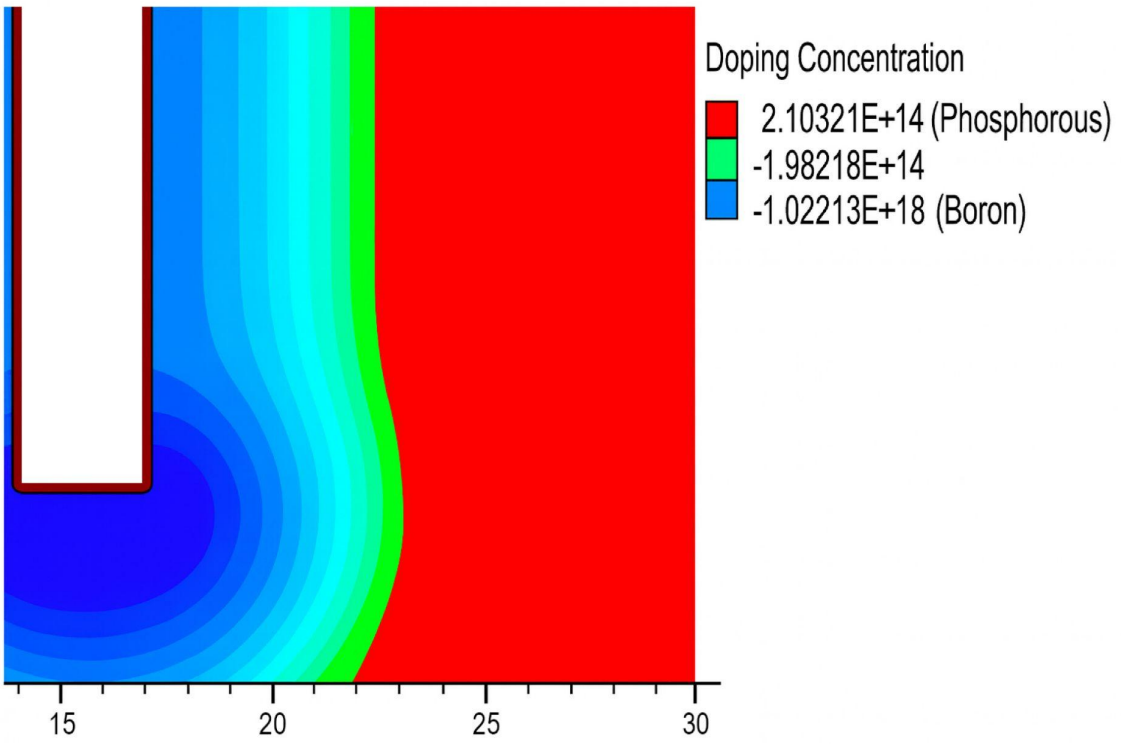


This principle is well established in semiconductor fabrication. Like sunlight striking Earth more intensely at the equator than at higher latitudes, ion implantation produces a higher dopant dose at flat surfaces (trench bottom) than angled ones (sidewalls). (Ex. 1003, ¶¶327-37.)

This phenomenon is confirmed by multiple sources pre-dating the ’634 Patent, including:

• Berberich et al. (2003) – proposing optimized sidewall doping profiles with lower concentrations than trench bottoms (Ex. 1021, p. 3, Fig. 2 & accompanying text; Ex. 1003, ¶344, 346.);

Ex. 1021, S.E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 5 Fig. 8 (2003)



• Fuse et al. (1989) – describing ion reflection and non-uniform trench doping (Ex. 1020, pp. 2–3, Figs. 2–4 & accompanying text; Ex. 1003, ¶¶341, 345.);

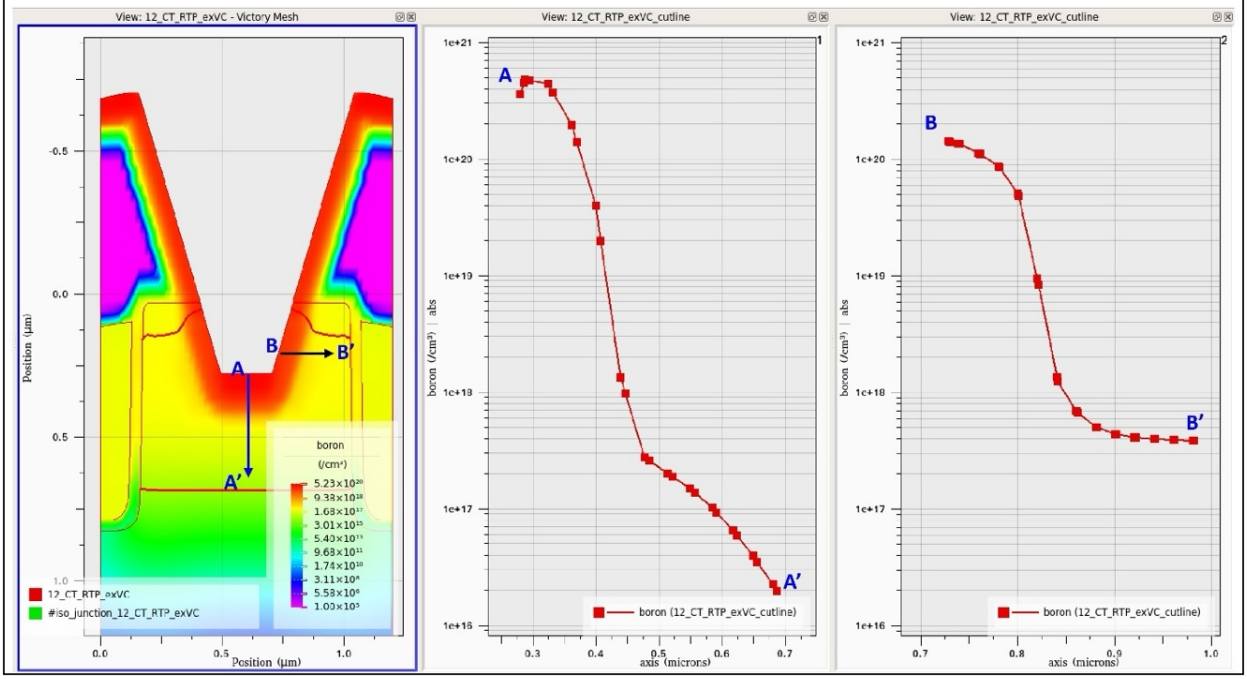
• Davari et al. (1988) and Nizou et al. (2006) – describing various sidewall doping control techniques (Ex. 1022, pp. 475–477, Table 17.2 & accompanying text; Ex. 1003, ¶347).

Trial testimony in *Force Mos Tech. v. AsusTek* further supports this conclusion, with the patentee's expert analogizing ion doping to rainfall: the

horizontal trench bottom receives a higher "dose" than the angled sidewalls. (Ex. 1019, pp. 143, 146–47.)

Further, a Monte Carlo method simulation—using parameters that are typical for forming shallow, heavily doped (i.e., P^+ or N^+) regions within the source contact trench, and specifically relied on in the fabrication processes disclosed in both Hshieh ('384) and the '634 Patent—conclusively demonstrates that the trench sidewalls inherently receive a lower dopant concentration than the trench bottom, confirming that this physical principle is not only inherent but also fundamentally part of the teachings of both Hshieh ('384) and the '634 Patent. (Ex. 1003, ¶¶339-40.)

Monte Carlo Simulation: Ion Implantation (IMP) followed by Rapid Thermal Annealing (RTA) on MOSFET with 109°-tapered trench — Implant Species: BF2; Dose: 5 × 10^{15} cm^{-2}; Energy: 20 keV; Implant Angle: 90° (relative to epitaxial layer); 1,000°C for 15 seconds



The ’634 Patent requires only that the lateral contact layer have a lower doping concentration than the base contact layer—not that it falls below a threshold. A POSITA would understand that both regions may still be “P^+,” with the trench bottom receiving a higher concentration due to direct implantation and sidewalls a lesser concentration due to angular incidence. (*Id*. ¶340.) This inherent physical result, dictated by well-known ion implantation geometry, would have been obvious to a POSITA applying standard design practices to Hshieh’s structure. (*Id*.)

Accordingly, even though Hshieh does not expressly quantify the dopant gradient, its structure, combined with POSITA knowledge, renders *[2d]* obvious. (*Id*. ¶¶317-51).

3. Dependent Claim 3

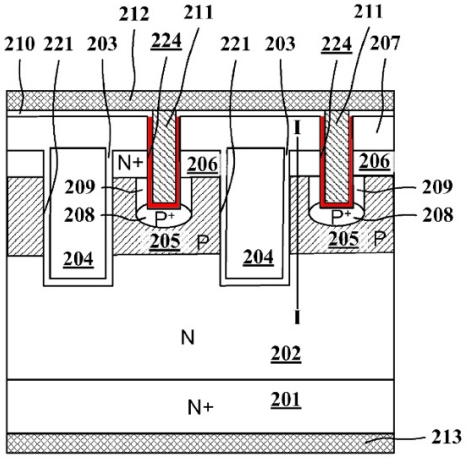
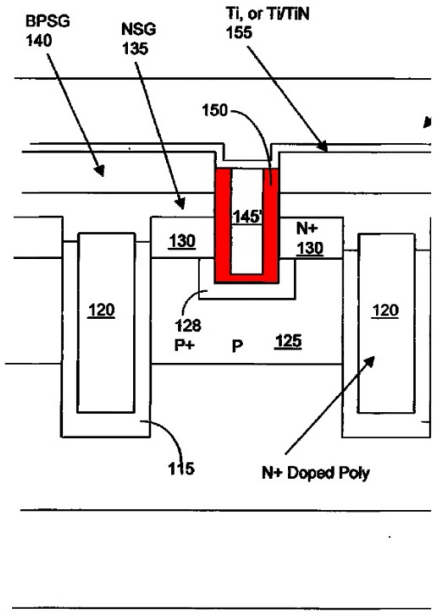
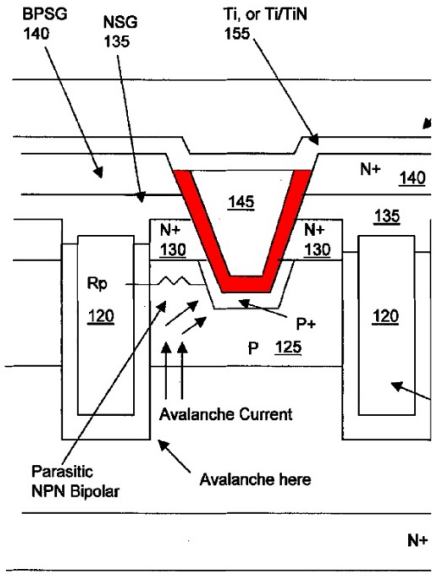
Claim 3 depends on Claims 1–2 and is taught by Hshieh. (*See* Section VIII.A.1–2.; *Id*. ¶¶352-73.)

a. Limitation [3a]

Hshieh teaches a barrier metal layer corresponding to element 110/210 of the ’634 Patent. The ’634 Patent describes this layer as an intermediate conductive film that lines the contact opening, surrounds the tungsten plug, and functions to prevent diffusion and maintain contact integrity (e.g., adhesion). (Ex. 1001, 4:9–23; FIGs. 2F–2G; Ex. 1003, ¶354.)

[3a]

barrier metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

Hshieh discloses the same structural and functional element. (Ex. 1003, ¶355.) It identifies a barrier layer 150 (or 245 in an alternative embodiment) surrounding a tungsten plug (element 145/250) within the trenched source contact.

(Ex. 1005, ¶27, 35; FIGs. 3–8, elements 145 and 150, 9H–9J, element 245/250.) Hshieh states that "a plurality of trenched source contact filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is formed. (*Id*.)

To the extent the barrier metal layer is understood to extend over the interlayer oxide film (element 107/207), as shown in FIG. 2G of the '634 Patent, Hshieh discloses a corresponding structure. It states: "A low resistance metal layer 255 is deposited over the top surface… composed of Ti or Ti/TiN to assure good electric contact is established." (Ex. 1005, ¶27, 35; FIGs. 3–8, 9J, elements 155 and 255; Ex. 1003, ¶356)

Hshieh's Ti/TiN barrier layers serve the same function: isolating the plug, preventing diffusion, and promoting adhesion—without impairing electrical performance. (Ex. 1003, ¶357.) The structure and purpose match those of the '634 Patent's barrier metal layer.

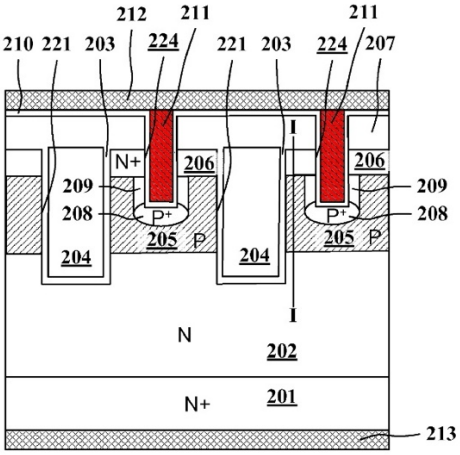
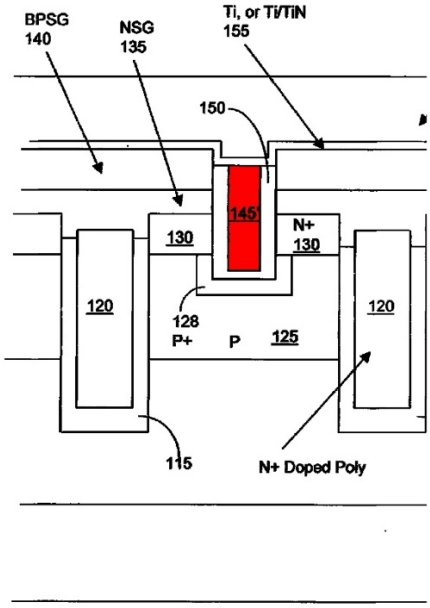
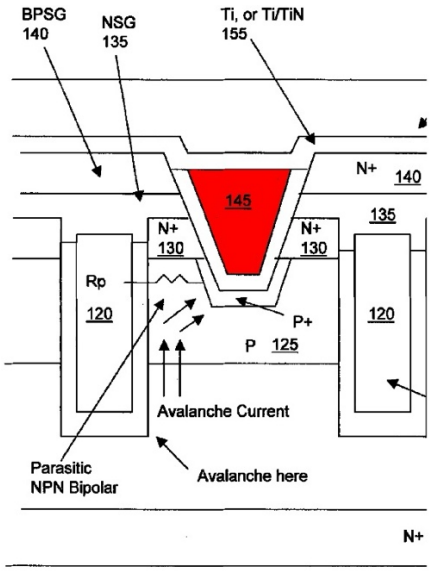
Accordingly, Hshieh discloses a barrier metal layer surrounding the tungsten plug and formed between it and surrounding materials, thereby teaching *[3a]*. (*Id*. ¶¶354-58.)

b. Limitation [3b]

Limitation *[3b]* is disclosed in Hshieh, which provides contact metal plugs corresponding to element 111/211 of the '634 Patent. The '634 Patent describes these plugs as conductive fill structures—typically tungsten—deposited within the

source contact trench to electrically connect the underlying diffusion regions to the front metal layer. (Ex. 1001, 4:13–27; FIGs. 2F–2G, elements 111/211; Ex. 1003, ¶359.)

[3b]
contact metal plugs

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*  *Fig. 3 (Annotated partial enlarged view)*

Hshieh discloses the same feature. It describes "a plurality of trenched source contact[s] filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150." (Ex. 1005, ¶27; FIGs. 3–8, elements 145 and 150.) In an alternative embodiment, the tungsten plug is labeled as element 250, surrounded by barrier layer 245. (*Id.* ¶35; FIGs. 9H–9J, elements 245 and 250.)

These tungsten plugs fill the source contact trenches and provide vertical conduction between the P^+-doped body region and the top-side source electrode. (Ex. 1003, ¶361.) As in the '634 Patent, the metal plugs in Hshieh are electrically and structurally integrated into the vertical current path and are isolated from surrounding dielectric layers by a barrier metal film. (*Id.*)

Accordingly, Hshieh teaches contact metal plugs consistent with those recited in the '634 Patent, thereby teaching*[3b]*. (*Id.* ¶¶359-62.)

4. Dependent Claim 4:

Claim 4 depends on Claims 1–3 and is taught by Hshieh. (*See* VIII.A.1–3; *Id*. ¶¶363–69.)

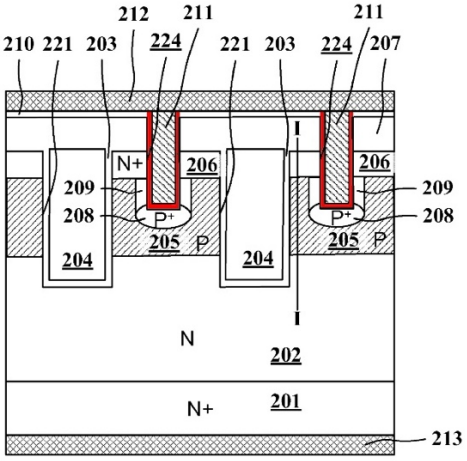
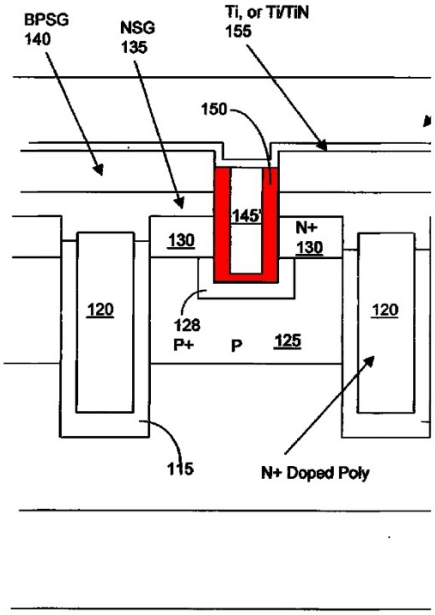
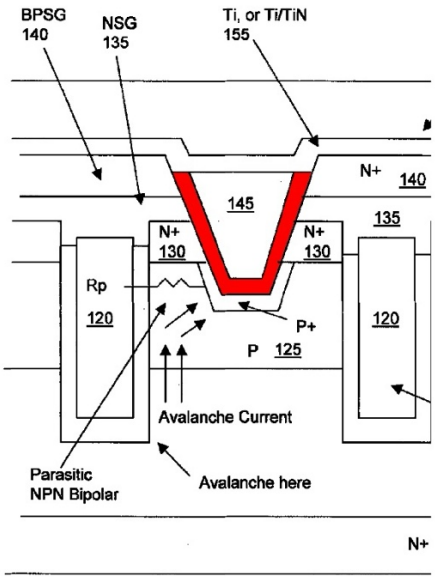
a. Limitation [4a]

Limitation *[4a]* is disclosed in Hshieh, which provides a barrier metal layer composed of Ti/TiN, corresponding to element 110/210 of the '634 Patent. (Ex. 1003, ¶365.) The '634 Patent describes the barrier metal layer as a conductive film

that prevents diffusion and maintains structural integrity at the interface between the tungsten plug and surrounding dielectric. (Ex. 1001, 4:9–23; Figs. 2F–2G.)

[4a]

barrier metal layer is Ti/TiN

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

Hshieh expressly discloses this composition. It states that the source contact trench is "filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150." (Ex. 1005, ¶27; FIGs. 3–8, elements 145 and 150.) In an alternative embodiment, Ti/TiN barrier layer 245 surrounds tungsten plug 250. (*Id*. ¶35; FIGs. 9H–9J.) Accordingly, Hshieh discloses a barrier metal layer of Ti/TiN, satisfying [4a]. (Ex. 1003, ¶¶365-66.)

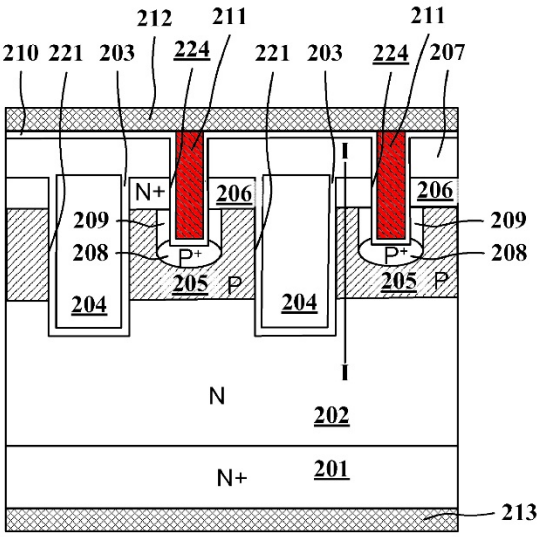
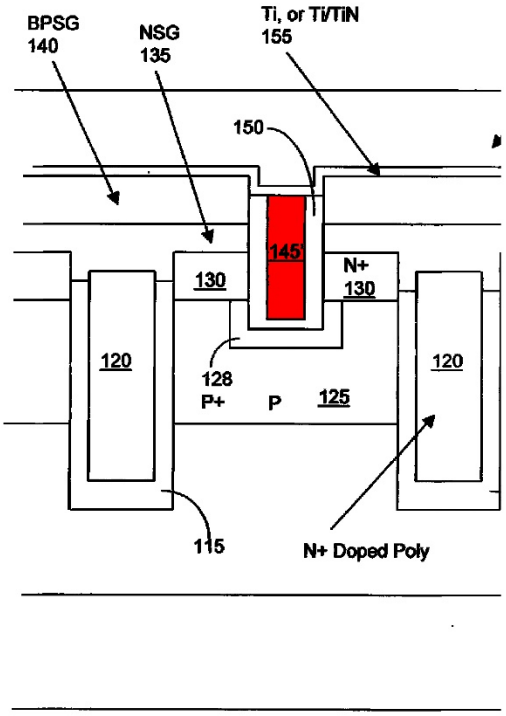
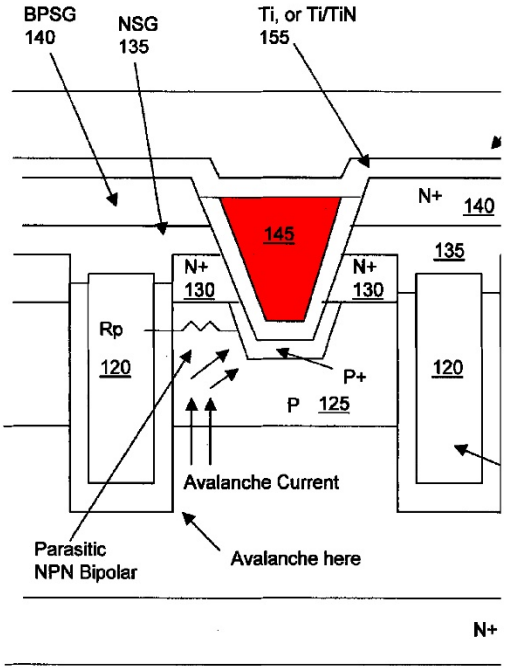
b. Limitation [4b]

Limitation [4b] is disclosed in Hshieh, which teaches a tungsten contact metal plug corresponding to element 111/211 of the '634 Patent.

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[4b]

contact metal plug is Tungsten

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

Hshieh states that "a plurality of trenched source contact[s] filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is formed. (Ex. 1005, ¶27; FIGs. 3–8, elements 145 and 150.) In an alternative embodiment, the plug is identified as tungsten plug 250, surrounded by barrier layer 245. (*Id.* ¶35; FIGs. 9H–9J.)

These plugs are explicitly identified as tungsten, consistent with the structure described in the '634 Patent. (Ex. 1003, ¶¶368-69.) Accordingly, Hshieh discloses a contact metal plug made of tungsten, teaching *[4b].* (*Id*. ¶¶367-69.)

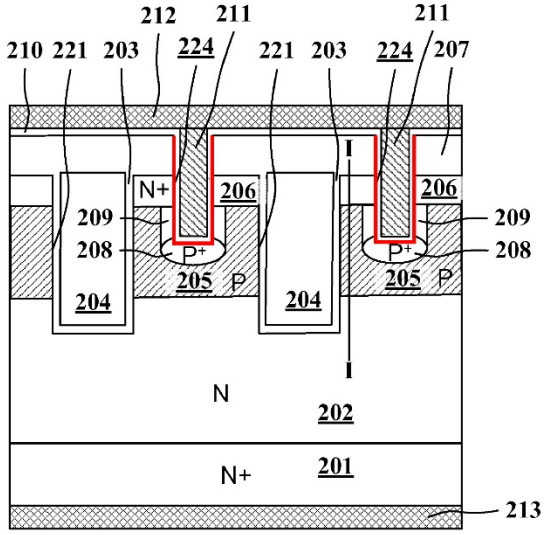
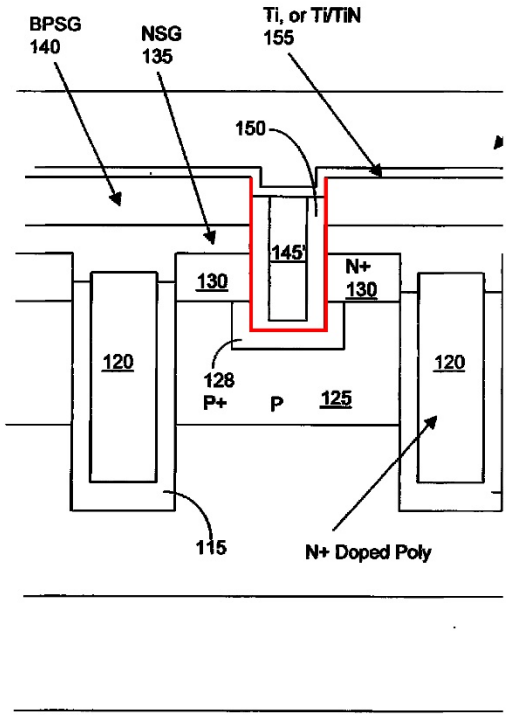
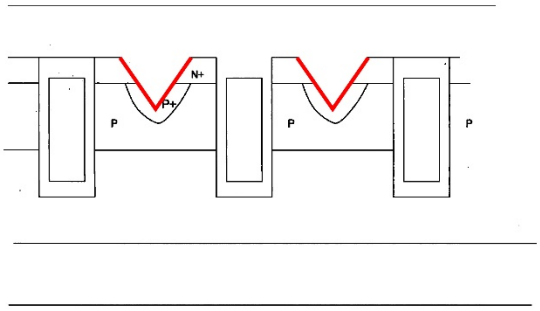
5. Dependent Claim 5

Claim 5 depends on Claims 1–4 (*See* VIII.A.1–4) and is taught by Hshieh. (Ex. 1003, ¶¶370-73.)

Hshieh expressly teaches source contact trenches with either vertical or tapered profiles, consistent with element 124/224 of the '634 Patent. (Ex. 1001, 4:50–52; Ex. 1005, ¶34) It discloses "trenched source contacts" (element 145) formed by etching into the semiconductor body and filling with conductive material. FIGs. 4, 5, 7, 8, and 9G' illustrate vertical trenches, while FIGs. 2, 6, 9G–9J show tapered trenches that narrow from top to bottom. (Ex. 1005, ¶34, FIGs. 2, 4-8, G', 9G–9J.) These tapered profiles are routinely produced by standard etch processes and fall squarely within the claimed scope. (Ex. 1003, ¶¶372-73.)

[5]

source contact trench vertical or tapered shape

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 2 (Annotated)

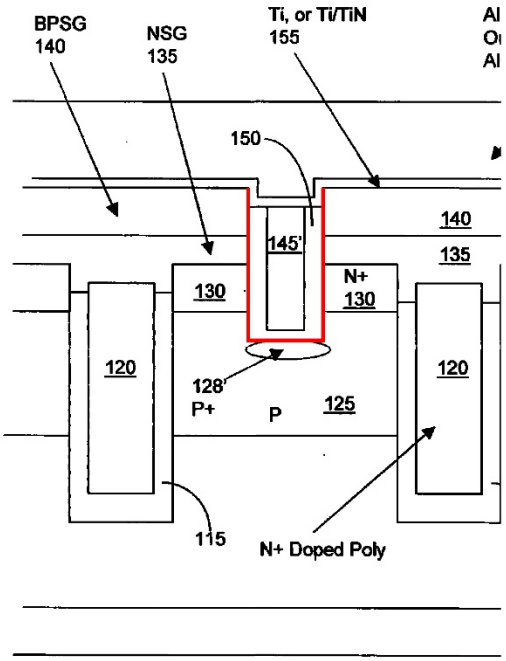


Fig. 5 (Annotated partial enlarged view)

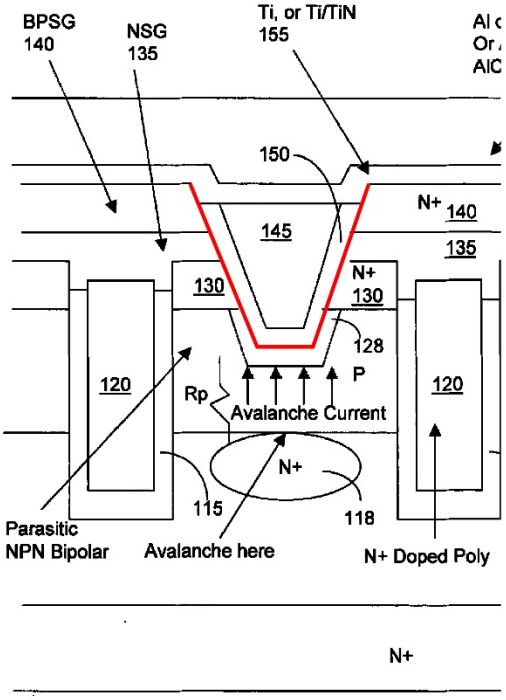


Fig. 6 (Annotated partial enlarged view)

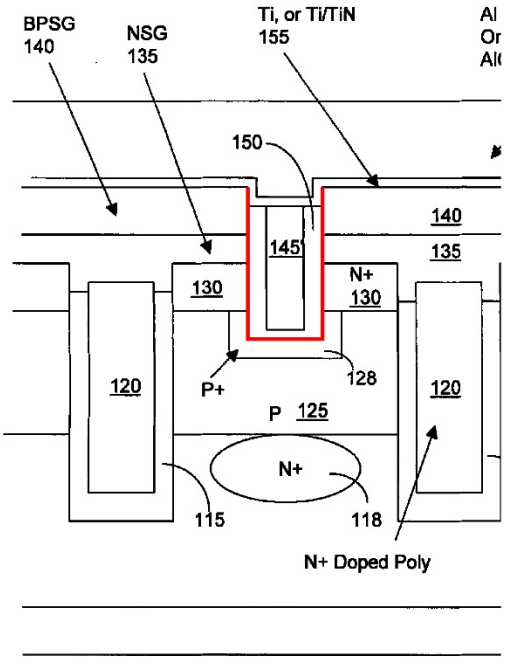


Fig. 7 (Annotated partial enlarged view)

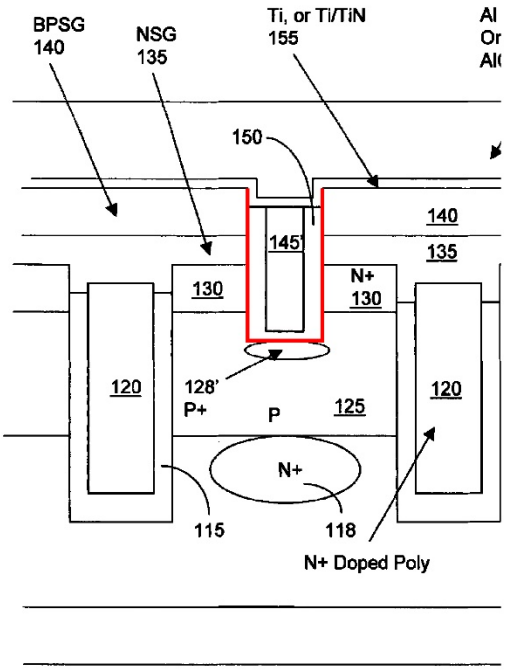


Fig. 8 (Annotated partial enlarged view)

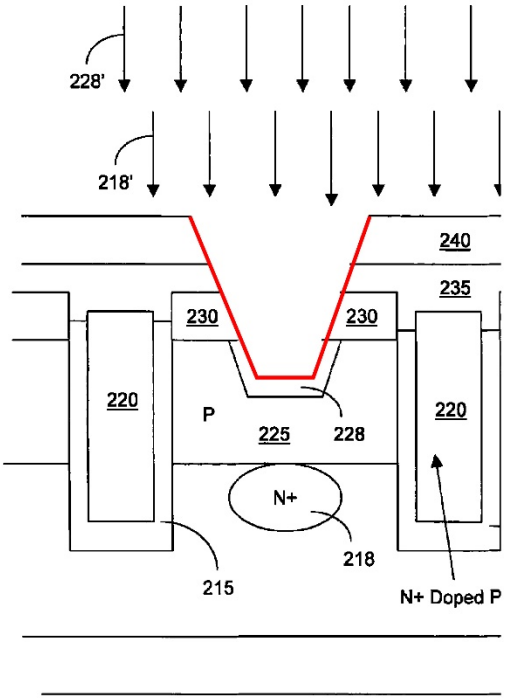


Fig. 9G (Annotated partial enlarged view)

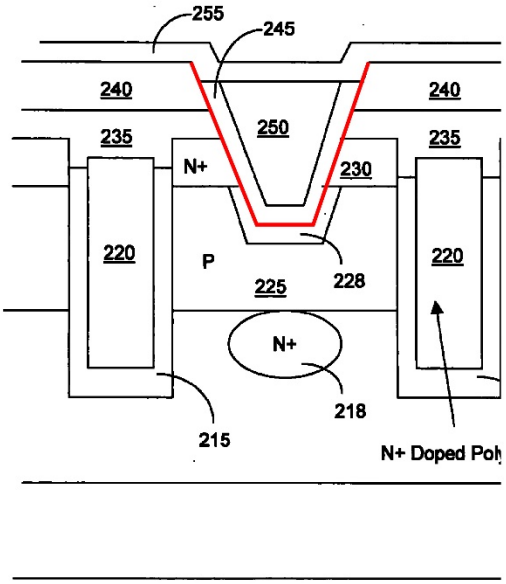


Fig. 9J (Annotated partial enlarged view)

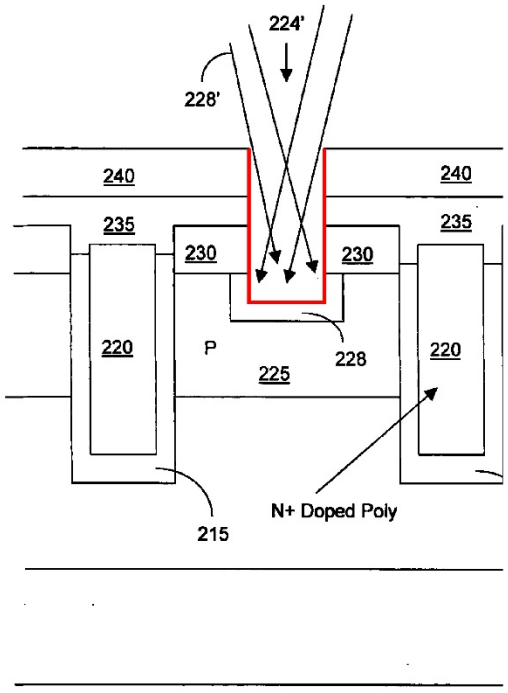


Fig. 9G' (Annotated partial enlarged view)

Accordingly, Hshieh discloses both vertical and tapered source contact trenches, teaching the remainder of Claim 5. (*Id.* ¶¶370-73.)

6. Dependent Claims 6 - 9

Claims 6-9 are rendered obvious in view of the analyses of Claims 1 and 2-5, along with the additional discussion below. (*Id.* ¶¶374-86.)

Each of Claims 6–9 corresponds directly to Claims 2–5, respectively: 6 = 2, 7 = 3, 8 = 4, and 9 = 5. (*Id.* ¶¶374-75, 381-82, 383-84, 385-86.) Accordingly, the analysis applicable to each corresponding limitation applies equally here. The sole distinction is that Claim 6 reverses all dopant polarities, converting the n-channel MOSFET of Claim 2 into its electrical mirror image—a p-channel (pMOS)

MOSFET. (*Id*. ¶377.) Specifically, the silicon substrate, epitaxial layer, and source layer become P-type, while the base layer, lateral contact layer, and base contact layer become N-type. (*Id*. ¶¶377-80.) Since Claims 7–9 depend from Claim 6, their structures also reflect this reversed doping, but the corresponding claim analyses remain unchanged. (*Id*. ¶¶381-86.)

The ability to fabricate either nMOS or pMOS transistors by simply reversing dopant polarities has long been a foundational concept in semiconductor design. This is well illustrated in Grove (1967) depicting an nMOS in Fig. 11.8(a) and a pMOS in Fig. 11.8(b), which shows structurally identical MOSFETs whose electrical behavior depends solely on dopant type. (Ex. 1018, Fig. 11.8; Ex. 1003, ¶378.)

Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 Fig. 11.8 (1967)

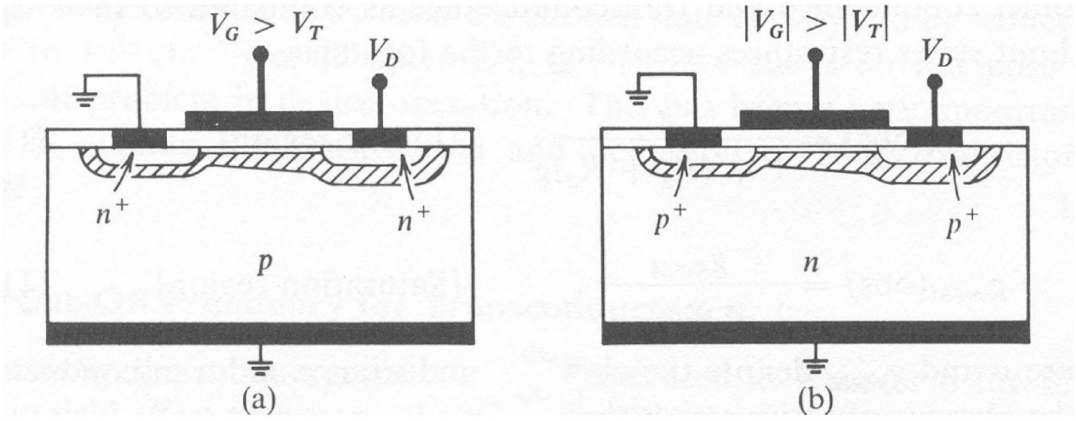


Fig. 11.8 (Annotated partial enlarged view)

A POSITA would readily recognize that the structural configurations disclosed in both the ’634 Patent and Hshieh remain unchanged when transitioning from nMOS to pMOS. The substitution of N-type and P-type dopants is a routine design choice that does not affect geometry, layout, or fabrication steps. (Ex. *1003,* ¶¶378-79.)

Accordingly, Claim 6-9 is rendered obvious over Hshieh in view of a POSITA’s knowledge and is taught by the same analysis as Claim 2-5. (*Id*. ¶¶374-86.)

B. Ground 2: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Uno (’864)

1. Independent Claim 1

a. Limitation [1-preamble]

i. [1-preamble-1]

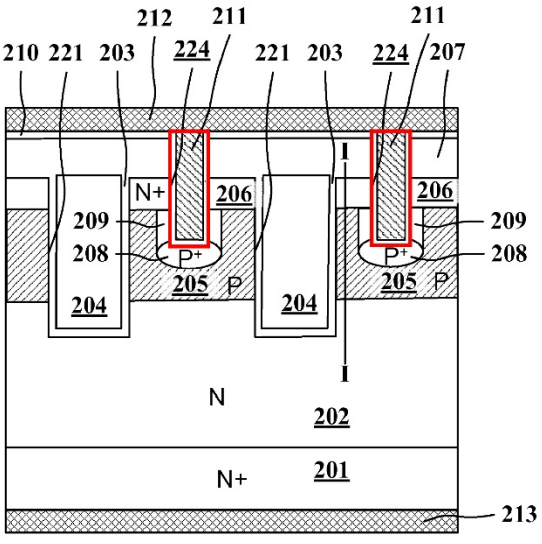
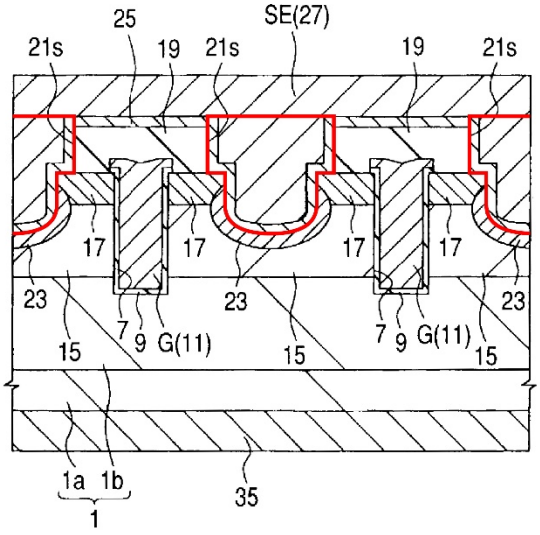
Uno (’864) discloses a “trenched MOSFET.” (Ex. 1003, ¶397.) It describes metal-insulator-semiconductor field-effect transistors (MISFETs), and a POSITA would recognize MOSFETs as a common subclass of MISFETs, with the “O” (oxide) in MOSFET replaced by “I” for the more generic term “insulator.” (*Id*. ¶162.) Accordingly, a POSITA would understand Uno’s disclosure as necessarily encompassing a MOSFET. (*Id*. ¶411.) Importantly, Uno discloses all structural

features of a MOSFET as claimed, rendering any difference purely semantic. (*Id.* ¶¶397–400.) Thus, Uno teaches *[1-preamble-1]*.

ii. [1-preamble-2]

Uno discloses a trenched source contact consistent with element 124/224 of the '634 Patent. It describes forming a "contact trench (source-contact) 21s" by etching through the silicon oxide film 19 and underlying substrate 1. (Ex. 1006, 15:31–35; Ex. 1003, ¶401-02.) Multiple figures—FIGs. 9, 12, 15, 16, 18, 20, 24, and 36–38—and their descriptions collectively show the structure and fabrication of the trenched source contact. (*Id.* ¶403.)

[1-preamble-2]
trenched source contact

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

A POSITA would understand that Uno teaches a trenched source contact consistent with *[1-preamble-2]*, both structurally and functionally. (*Id*.)

To the extent the preamble is limiting, Uno teaches the "trenched MOSFET" and "trenched source contact" required by Claim 1's preamble. (*Id*. ¶¶401–04.)

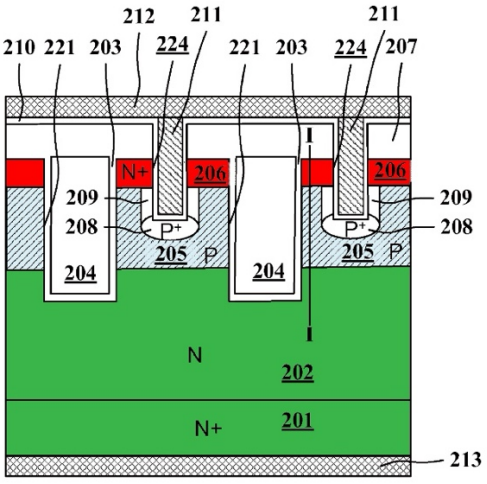
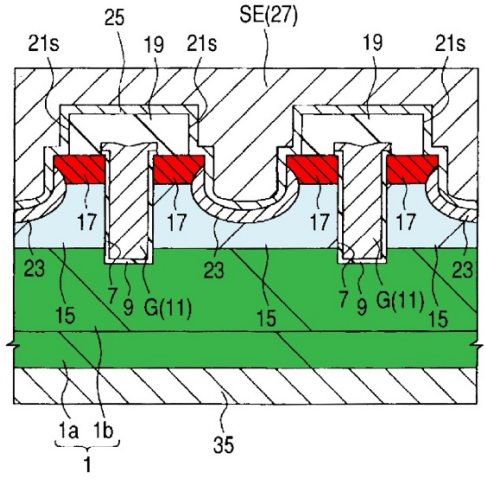
b. Limitation [1a]

i. Limitation [1a-1]

1) [1a-1-1]

Uno ('864) discloses a semiconductor region comprising a drain region (1a & 1b), body region (15), and source region (17)—consistent with the layered structure recited in the '634 Patent (elements 101/201, 102/202, 105/205, and 106/206). (*Id.* ¶409.)

[1a-1-1]
semiconductor region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Specifically, Uno states:

> "In an n-channel type power MISFET… an npn-type parasitic bipolar transistor PB constituted with an n-semiconductor region (source region) 17, a p-semiconductor region (channel region) 15, and a drain (1a, 1b) is present inside…" (Ex. 1006, FIG. 20; 8:24–28.)

Uno explains that "a single crystal silicon layer 1b doped with an n-impurity (e.g., phosphorus) is epitaxially grown on an n-single crystal silicon substrate 1a," corresponding to the substrate and epitaxial layer. (Ex. 1006, 4:55–58.) The P-type region 15 and N^+-type region 17 correspond to the body and source regions. (*Id*. 5:35–36.) These regions appear in FIGs. 8–9, 11–16, 18, 20, and 36–38 (elements 1a, 1b, 15, 17). (Ex. 1003, ¶409-10.)

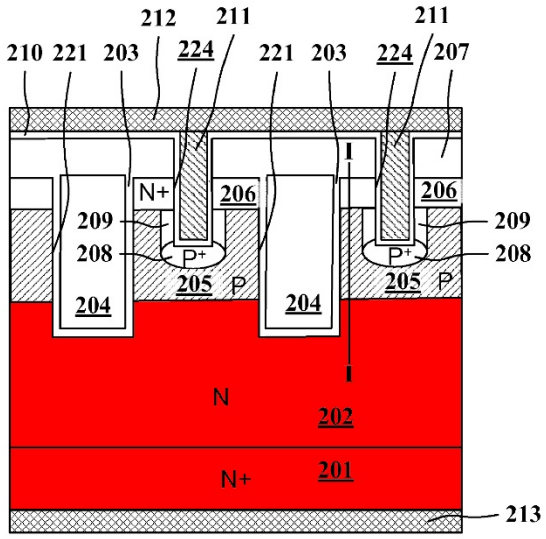
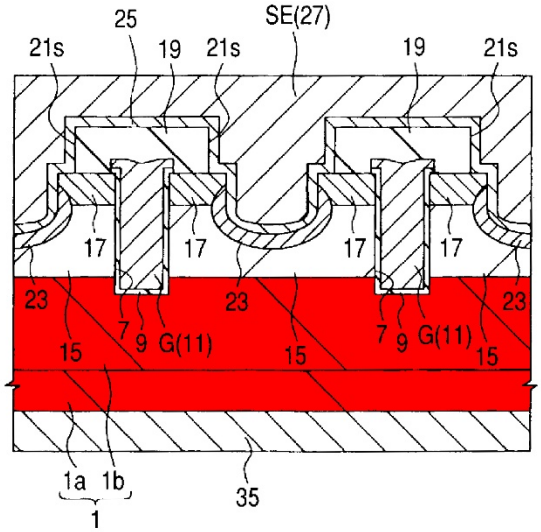
From bottom to top, the structure comprises: (1) N^+ silicon substrate (1a), (2) N-type epitaxial layer (1b), (3) P-type body region (15), and (4) N^+ source region (17). This vertical stack matches the multi-layered structure recited in *[1a-1-1]*. Accordingly, Uno discloses a semiconductor region comprising a drain, body, and source, and therefore teaches *[1a-1-1]* of the '634 Patent. (*Id*. ¶¶408–11.)

2) [1a-1-2]

Uno ('864) teaches a drain region (1a & 1b) consistent with element 101/201 & 102/202 of the '634 Patent. (Ex. 1003, ¶412.) The '634 Patent identifies the epitaxial layer (102/202) as comprising the drain region, but as discussed in

Ground 1 *[1a-1-2]*, Claim 1 is ambiguous as to whether it includes only the epitaxial layer (102/202) or also the substrate (101/201). (Ex. 1001, claim 1.)

[1a-1-2]
drain region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno discloses both: a single crystal silicon epitaxial layer 1b—doped with an N-type impurity such as phosphorus—grown on an N-type silicon substrate 1a. (Ex. 1006, 4:55–58.) These correspond to elements 102/202 and 101/201 of the '634 Patent. (Ex. 1003, ¶413.) Together, layers 1a and 1b form a continuous vertical conduction path, and Uno semantically refers to this structure as "drain (1a, 1b)." (Ex. 1006, 7:27, 8:27, 10:10.) This configuration appears in FIGs. 1, 3, 5, 6, 8, 9, 11–18, 20, and 38. A POSITA would view this arrangement—whether considering the epitaxial layer and silicon substrate together or individually—as

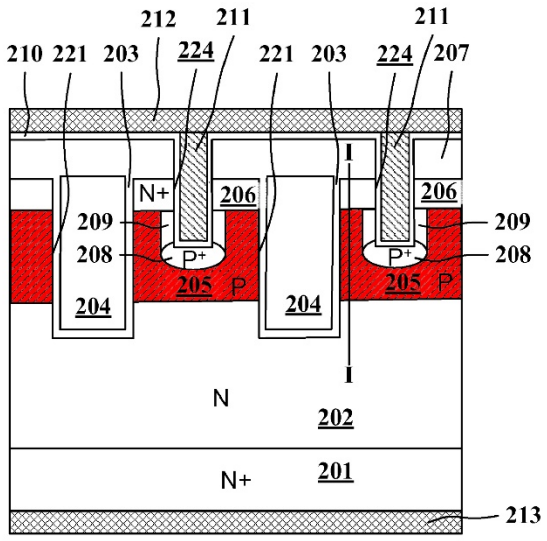
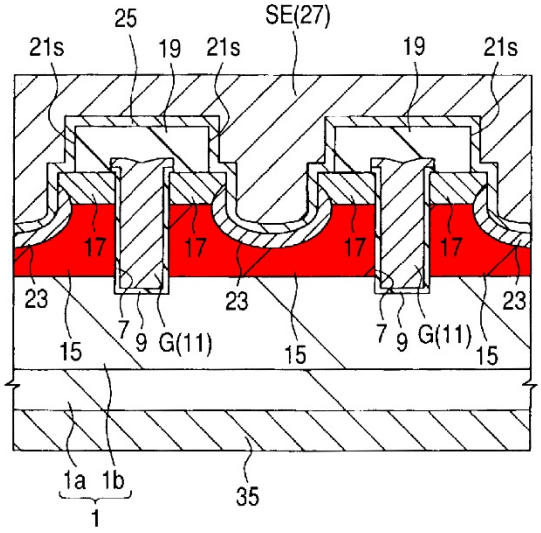
satisfying the plain and ordinary meaning of "drain region" in the '634 Patent. (Ex. 1003, ¶414.)

Accordingly, Uno discloses a drain region comprising both an epitaxial layer and a substrate, teaching *[1a-1-2]*. (*Id*. ¶¶412–14)

3) [1a-1-3]

Uno discloses a "base layer" corresponding to a "body region" 15 consistent with element 105/205 of the '634 Patent.

[1a-1-3]
body region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno describes a "p-semiconductor region (channel region) 15" between the source and drain, serving as the gate-controlled conduction path. (Ex. 1006, 5:67;

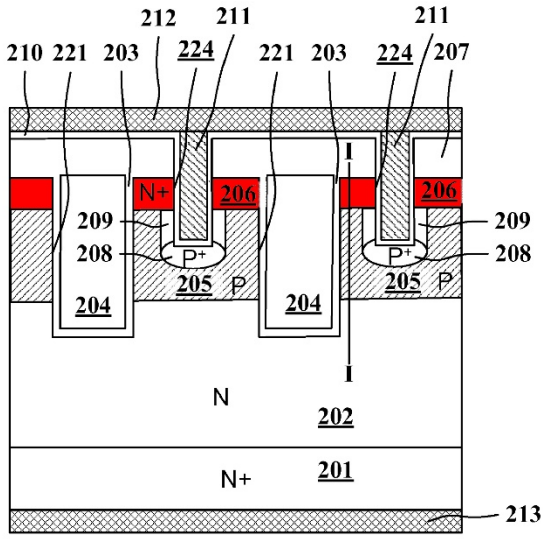
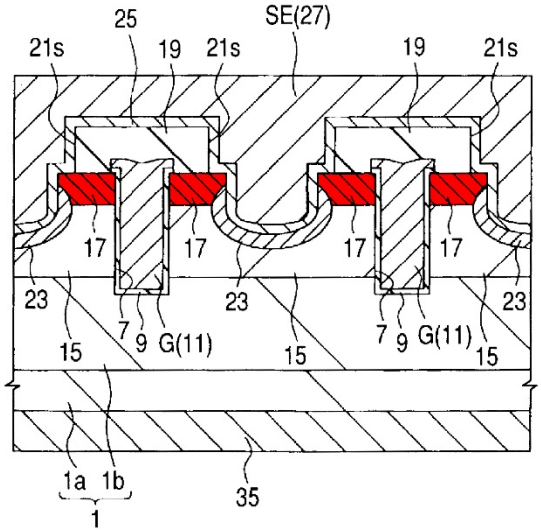
FIGs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38.) This is structurally and functionally equivalent to the P-type body region 105/205 in the ’634 Patent. (Ex. 1003, ¶416.) Uno further states that “a channel portion [is] arranged between the source portion and the drain portion,” consistent with conventional body region placement in trench-type or planar MOSFETs. (Ex. 1006, 2:28–30.) An alternative embodiment features an “n-semiconductor region (channel region, well) 215,” indicating the channel/body region may be P-type or N-type depending on device polarity. (Ex. 1006, 9:30–32; FIG. 24, element 215; claim 1; Ex. 1003, ¶417.)

In both embodiments, the channel region serves the same role as the body region recited in the ’634 Patent. (Ex. 1003, ¶417.) Thus, Uno teaches a body region consistent with *[1a-1-3]*. (*Id*. ¶¶415–18.)

4) [1a-1-4]

Uno teaches a source region 17 consistent with element 106/206 of the ’634 Patent. The ’634 Patent describes a heavily doped N^+ source region above the P-type body region, forming part of the vertical conduction path. (Ex. 1001, 3:33-40; Ex. 1003, ¶419.)

[1a-1-4]
source region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

Uno discloses that "an n-impurity (e.g., As) is implanted into the substrate 1 between trenches 7 to form an n-semiconductor region (source region) 17," characterized as an "n^+-semiconductor region," consistent with high doping typical of trench-type MOSFETs. (Ex. 1006, 5:26–29, 5:47, 6:10–11, 6:26, 8:26, 8:60.) Source region 17 is above the P-type region 15, matching the source-to-body configuration of the '634 Patent. (*Id.* 5:26–32.) This arrangement appears in FIGs. 5, 6, 8–9, 11–18, 20–22, 24–25, and 36–38, where element 17 is consistently labeled as the source region. (*Id.* 5:29–30, 5:57, 8:26, 15:64.)

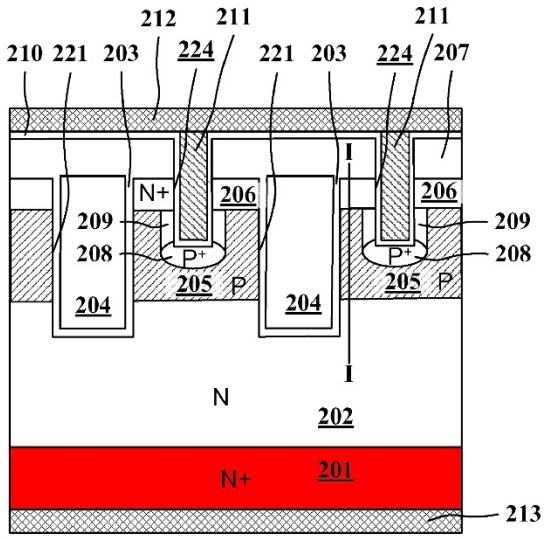
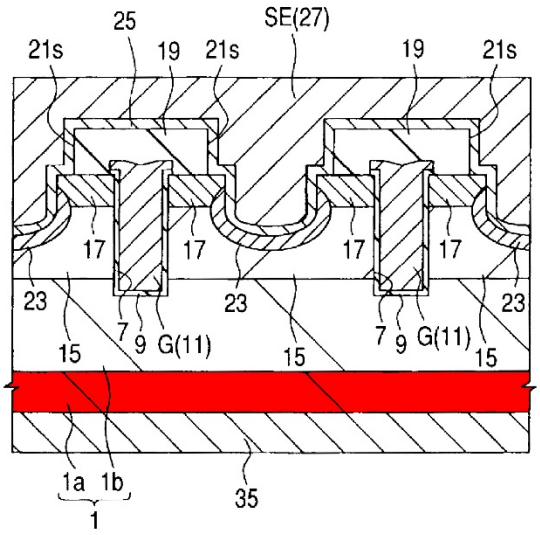
Thus, Uno discloses a source region performing the same structural and functional role as in the ’634 Patent, teaching *[1a-1-4]*. (Ex. 1003, ¶¶419–22.)

ii. Limitation [1a-2]

1) [1a-2-1]

Uno teaches a silicon substrate 1a corresponding to element 101/201 of the ’634 Patent.

[1a-2-1]
silicon substrate

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

Uno describes “an n-single crystal silicon substrate 1a” as the device’s foundational layer. (Ex. 1006, 4:58; FIGs. 1, 3, 5, 6, 8, 9, 11–18, 20, 36–38, element 1a.) The specification adds that “a single crystal silicon layer 1b doped

with an n-impurity… is epitaxially grown on the surface of an n-single crystal silicon substrate 1a," mirroring the '634 Patent's substrate and epitaxial layer configuration. (Ex. 1003, ¶429-30.)

Substrate 1a serves as the structural and electrical base, consistent with the silicon substrate's role in the '634 Patent. An N^+-type substrate with an N-type epitaxial layer is standard in MOS transistor manufacturing. (Ex. 1015, p. 124; Ex. 1008, pp. 385–87.) This is understood in the art as Wolf (1986) notes, "Either n-epi on n+ substrates or p-epi on p+ substrates can be used." (Ex. 1015, p. 386; Ex. 1003, ¶431.)

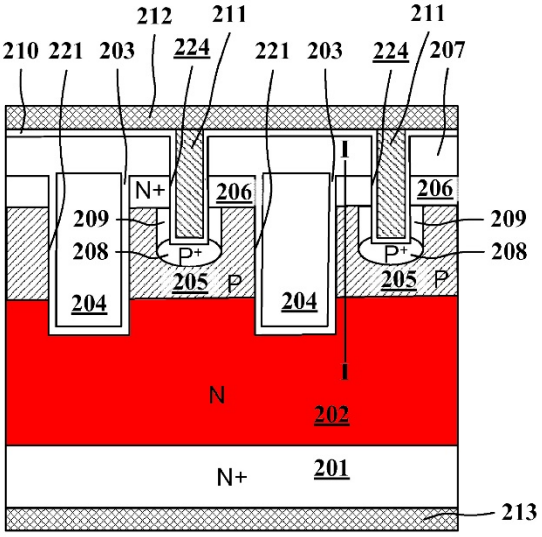
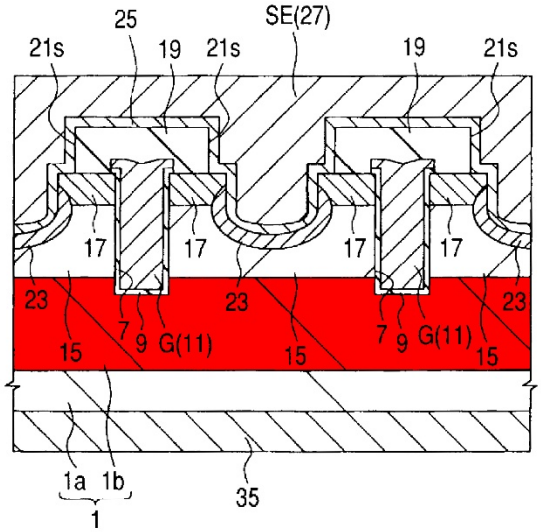
This configuration, with reversed doping, was used in the Texas Instruments 4Mb DRAM and aligns with the '634 Patent. Uno also contemplates polarity reversal to fabricate pMOS instead of nMOS devices. (Ex. 1006, 9:20–29.) Accordingly, Uno discloses a silicon substrate as the foundational device layer, satisfying *[1a-2-1]*. (Ex. 1003, ¶¶428–34.)

2) [1a-2-2]

Uno discloses an epitaxial layer corresponding to the drain region, consistent with element 102/202 of the '634 Patent. It states that "a single crystal silicon layer 1b doped with an n-impurity (e.g., phosphorus or arsenic) is epitaxially grown on the surface of an n-type single crystal silicon substrate 1a." (Ex. 1006, 4:55–59.)

Layer 1b lies directly above substrate 1a and forms part of the drain region. (Ex. 1003, ¶436.)

[1a-2-2]
epitaxial layer

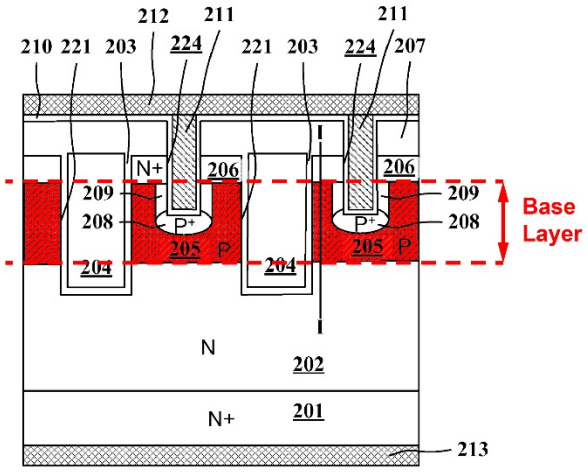
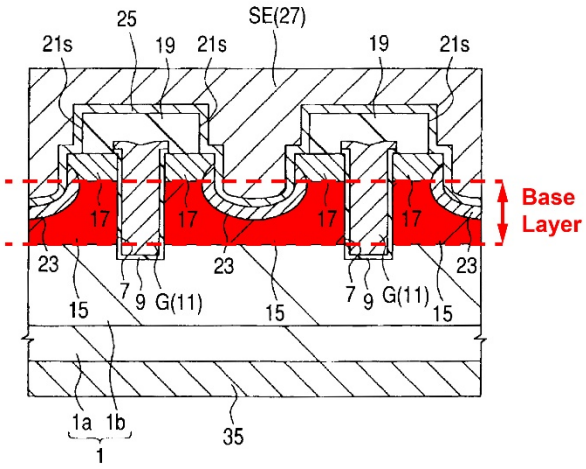
Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

This mirrors the ’634 Patent, where the epitaxial layer provides a vertical conduction path between the body region and the substrate. Uno depicts this across FIGs. 1, 3, 5, 6, 8, 9, 11–18, 20, and 36–38, with element 1b labeled as the epitaxial layer. (Ex. 1006, claim 1.) Accordingly, Uno discloses an epitaxial layer above a silicon substrate forming part of the drain region, teaching *[1a-2-2]*. (Ex. 1003, ¶¶435–37.)

3) [1a-2-3]

Uno teaches a base layer consistent with element 105/205 of the ’634 Patent.

[1a-2-3]
base layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno describes a “p-semiconductor region (channel region) 15” between the source and drain, functioning as the gate-controlled conduction path. (Ex. 1006, 5:67–6:3; FIGs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38, element 15.) This P-type region is structurally and functionally equivalent to the ’634 Patent’s body region and is formed within the base layer. (Ex. 1003, ¶439.)

In an alternative embodiment, Uno discloses an “n-semiconductor region (channel region, well) 215,” showing it may be P-type or N-type depending on polarity. (Ex. 1006 9:32; FIG. 24, element 215; claim 1.) In both embodiments, the

channel region lies between the source and drain as part of the base layer. (Ex. 1003, ¶440.)

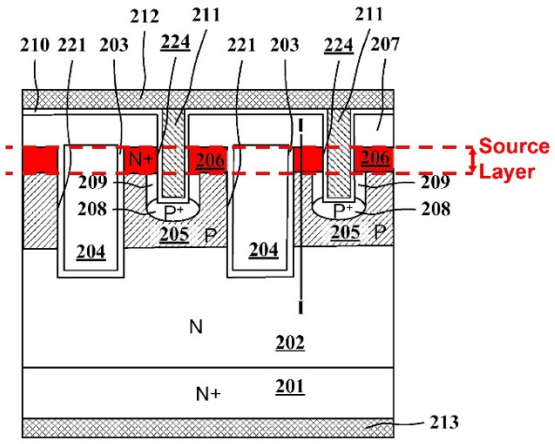
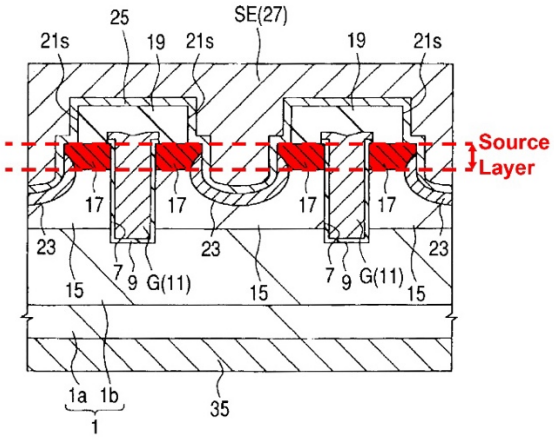
The Patent Owner's admitted prior art supports this interpretation. FIG. 1 of the '634 Patent shows the body region within the base layer, and the specification states that "the P-type base layer (205) [corresponds] to the body region of the trenched MOSFET." (Ex. 1001, 5:1–2.)

Thus, Uno discloses a body region above the epitaxial layer and below the source region—within a base layer—teaching *[1a-2-3]*. (Ex. 1003, ¶¶438–42.)

4) [1a-2-4]

Uno teaches a source region consistent with the source layer in element 106/206 of the '634 Patent.

[1a-2-4]
source layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

It discloses "an n^+-semiconductor region (source region) 17," above the P-type body region, functioning as a highly doped source. (Ex. 1006, 5:26–29, 5:43–45, 8:26, 15:64.) This region is identified in FIGs. 5, 6, 8–9, 11–18, 20–22, 24–25, and 36–38 (element 17). (Ex. 1006, 5:55–58; Ex. 1003, ¶444.)

In an alternative embodiment, Uno shows a "p^+-semiconductor region (source region) 217," indicating the source may be N-type or P-type depending on polarity. (Ex. 1006, 9:33; FIG. 24, element 217; claim 1.) In both, the source is highly doped, above the body, and configured to interface with the contact structure—aligning with the source layer and its sub-regions in the '634 Patent. (Ex. 1003, ¶¶445.)

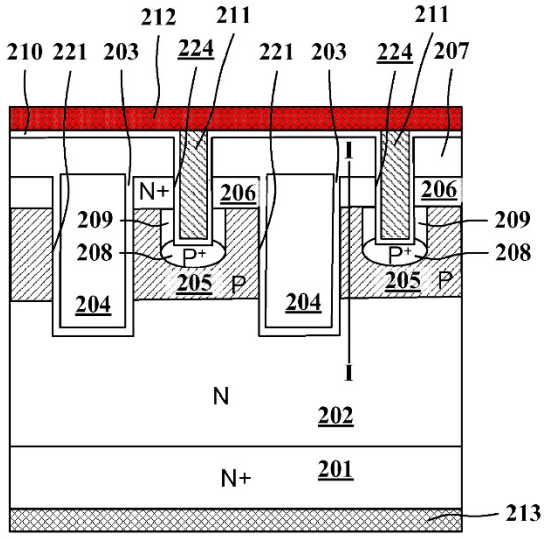
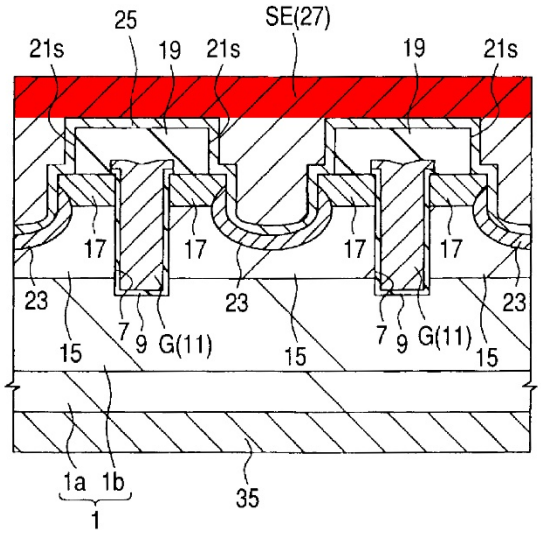
Although Uno does not use "source layer," a POSITA would recognize these consistently located regions above the base and epitaxial layers as the '634 Patent's source layer. (*Id.*) The Patent Owner's admitted prior art supports this: FIG. 1 shows the source regions within the source layer and states that "the N^+-type source layer (206) [is] corresponding to the source region of the trenched MOSFET." (Ex. 1001, 4:66–5:1.) The vertically stacked arrangement—substrate, epitaxial layer, base layer, and source layer—is likewise reflected in Uno. (*Id*. 1:29–32.)

Thus, Uno discloses a source region consistent with both the "source region" and "source layer" of the '634 Patent, teaching *[1a-2-4]*. (Ex. 1003, ¶¶443–47.)

c. Limitation [1b]

Uno teaches a front-side metal contact consistent with the "front metal layer" recited in element 112/212 of the '634 Patent. Claim 1 requires "a front metal layer formed on the upper surface of said semiconductor region." (Ex. 1001, claim 1.)

[1b]
front metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno discloses an analogous structure: "a source electrode SE comprising an aluminum film 27" formed on the front surface of the device. (Ex. 1006, 6:19–20; 7:1; FIGs. 9, 11, 12, 15, 16, 18, 20, 24, 36–38, element 27.) This aluminum layer is formed in a single step and functions as both the contact plug and the front metal

layer. (Ex. 1003, ¶449-50.) Although Uno does not use the term "front metal layer," a POSITA would understand that, despite being deposited together, the contact plug and the overlying conductive layer serve distinct purposes—consistent with known fabrication techniques such as dual-damascene copper metallization. (Ex. 1024, pp. 773–76; Ex. 1003, ¶451.)

Furthermore, the aluminum composition in Uno aligns with the '634 Patent, which identifies AlSi and AlSiCu as preferred front metal layer materials. (Ex. 1001, 4:28-29; Ex. 1003, ¶451.) The top-side, current-carrying role of Uno's aluminum film is confirmed by multiple claims in the reference, including claims 3, 5, 7, 9, 11, 14, 20, 27, and 31–34. (Ex. 1003, ¶451.)

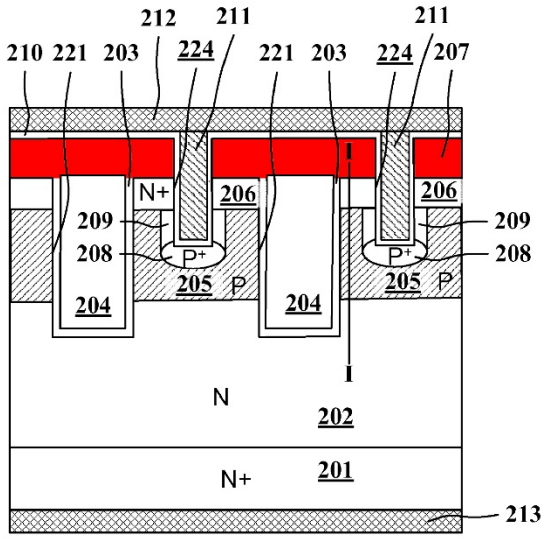
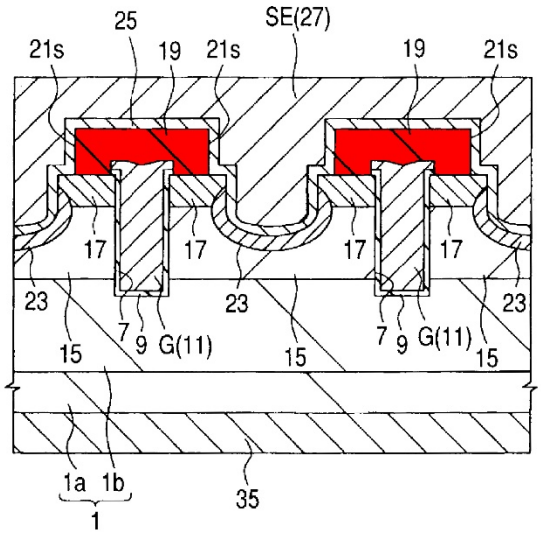
Accordingly, Uno discloses a front-side metal layer formed on the upper surface of the device, functionally and structurally equivalent to the front metal layer recited in the '634 Patent. These disclosures teach limitation *[1b]*. (*Id.* ¶¶448-53.)

d. Limitation [1c]

Uno teaches an interlayer oxide film corresponding to element 107/207 of the '634 Patent. (*Id.* ¶463.)

[1c]

interlayer oxide film

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

Uno identifies "silicon oxide film 19" as being formed over the semiconductor surface and functioning as a dielectric layer between the source region and the front metal contact. (Ex. 1006, 5:34–35, 5:49–50, 6:7–8, 6:65–66, 15:7, 15:10, 15:24–25, 15:31; FIGs. 6, 8, 9, 11, 12, 14–16, 18, 20, 24, 36–38, element 19; Ex. 1003, ¶455.) The oxide layer's placement between the source region and the top metal layer is repeatedly illustrated and described throughout Uno, and its function is consistent with long-standing practices in semiconductor design.

In semiconductor engineering, "silicon oxide" and "silicon dioxide" are used interchangeably, both referring to a standard interlayer dielectric material. As summarized in industry literature:

> "Two dielectric workhorses in device fabrication are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4)… the former is extensively used in electrical isolation." (Ex. 1017)

A POSITA would have recognized that silicon oxide film 19 functions as an interlayer oxide film—even if not expressly labeled as such—and that its use as a dielectric layer between the source region and front-side metal was conventional. (Ex. 1003, ¶456.) The admitted prior art of FIG. 1 in the '634 Patent further confirms that this configuration was well known and would have provided a POSITA motivation to use the express teachings of Uno. (*Id.*)

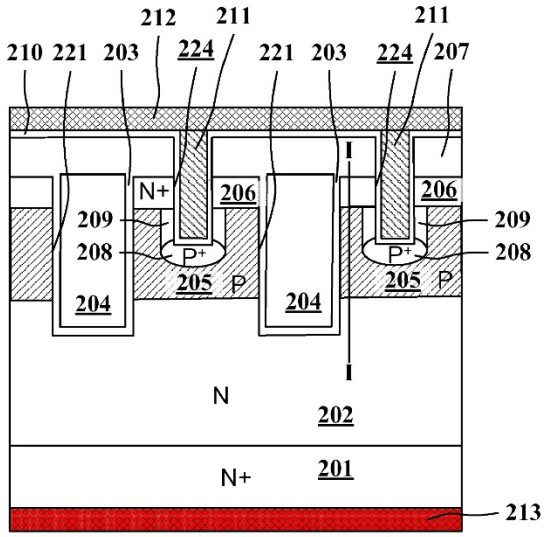
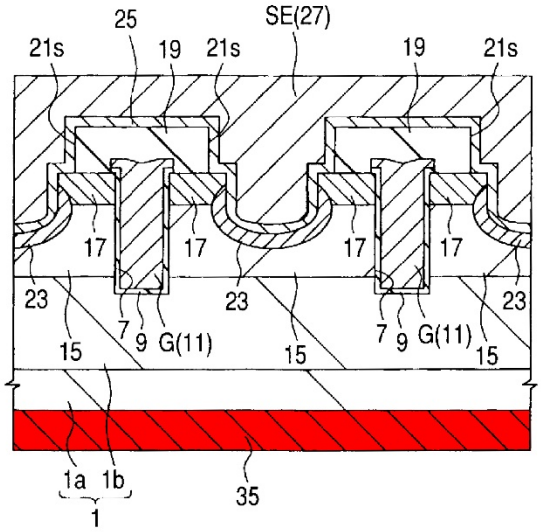
Accordingly, Uno discloses an interlayer oxide film, both in composition and in placement between the source layer and the front metal layer, thereby teaching limitation *[1c]*. (*Id.* ¶¶455-57.)

e. Limitation [1d]

This claim element is taught by Uno.

[1d]

bottom metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

Uno identifies element 35 as "a conductive film 35 forming a drain electrode," and shows it formed on the lower surface of the semiconductor region. (Ex. 1006, 6:20–21.) Uno further specifies that this conductive film is formed by sputtering a stack of metal layers—such as Ni (nickel), Ti (titanium), and Au (gold)—on the rear surface of the substrate (element 1a), resulting in a stacked metal film 35. Ex. 1006, 7:19–27; Ex. 1003, ¶459.)

Uno explains that this stacked film functions as a "lead electrode (drain electrode DE) for the drain (1a, 1b)," which clearly identifies this metal structure as the back-side electrical contact for the device. (Ex. 1003, ¶460.) In this context,

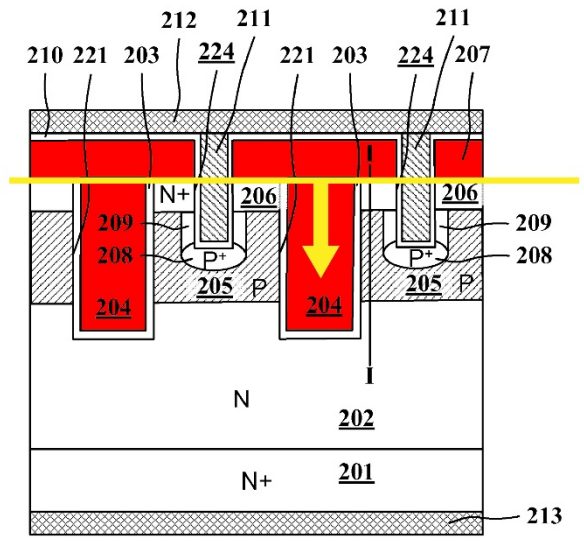
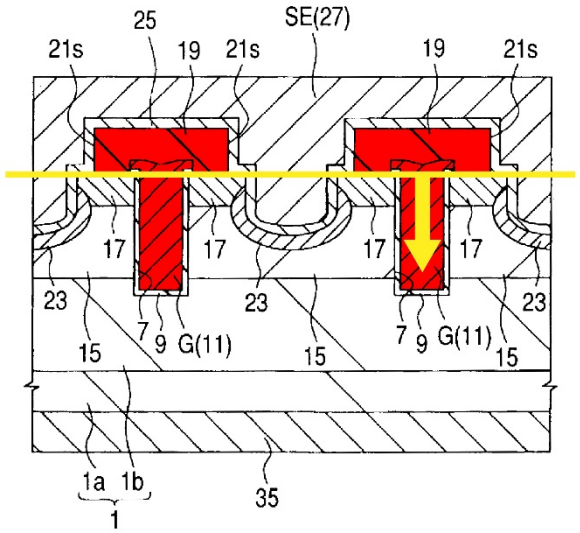
the term "lead electrode" refers to an electrical terminal—here, specifically the drain electrode—rather than to the metal element lead (Pb). (*Id.)*

Thus, Uno teaches limitation [1d] and discloses a metal contact formed on the bottom surface of the semiconductor region that functions as the drain electrode. This structure matches the "bottom metal layer" recited in the '634 Patent. (*Id*. ¶¶458-62.)

f. Limitation [1e]

[1e]

a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno likewise teaches the *[1e]* claim element when construed according to the plain and ordinary meaning of the claim language as explained by the district

court in *Force Mos v. ASUSTeK*, Uno identifies element 11 (G(11)) as the trenched gates, 19 as the interlayer oxide film, 17 as the source region formed within the broader source layer, 15 as the body region formed within the base layer, and 1b as the epitaxial layer. (Ex. 1006, FIG. 38; Ex. 1003, ¶464; Ex. 2026, p. 14-15.) These layers are arranged in the vertical order as required by the '634 Patent. (Ex. 1003, ¶466.) Additionally, the gate trenches are formed downward through the source and base layers into a portion of the epitaxial layer. Finally, the trenched gates are covered by the interlayer oxide film–Uno element 19. (*See Id*. 6:26–27, 6:59–60, 15:8, 15:18–19, 15:61–65; claims 1, 12, 16–18, 25, 30–34, 37.)

Accordingly, Uno discloses trenched gates and teaches limitation *[1e]*. (*Id.* ¶¶463-67.)

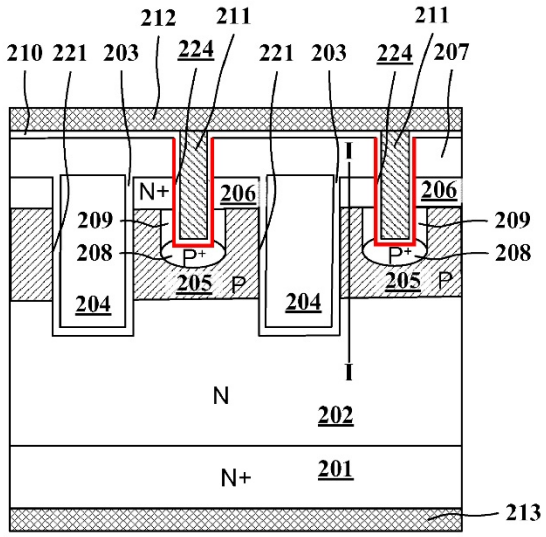
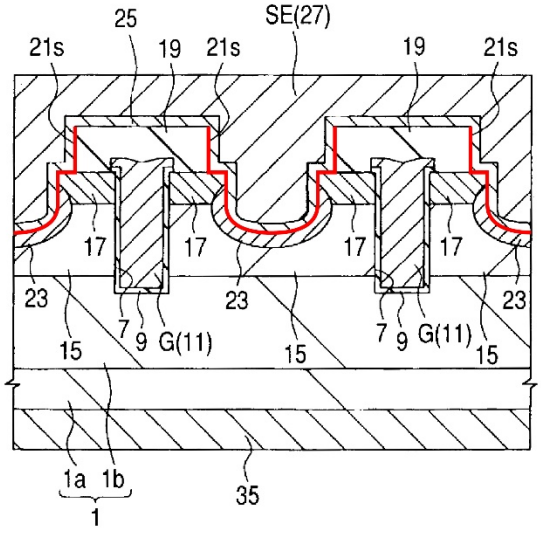
g. Limitation [1f]

i. [1f-1]

This claim sub-element is taught by Uno, which discloses source contact trenches corresponding to elements 124/224 of the '634 Patent.

[1f-1]

a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno identifies layer 19 as the interlayer oxide film, layer 17 as the source region (within the broader source layer), and layer 15 as the body region (within the base layer). (Ex. 1006, FIG. 38.) These layers are vertically arranged in the same order and functional relationship as required by the claim. (Ex. 1003, ¶471.)

Uno further explains that, after forming silicon oxide film 19, the film and underlying substrate are etched to form "contact trenches (source contact) 21s." (Ex. 1006, 5:35–38; 5:45–48, 5:55–60, 6:22–27, 6:35–36, 15:10–15, 15:29–30, 15:35–36; FIGs. 9, 12, 15, 16, 18, 20, 24, 36–38.) These trenches are explicitly shown as formed on top of oxide layer 19, extending downward through the source region 17 and into a portion of the P-type base region 15. (Ex. 1003, ¶472.)

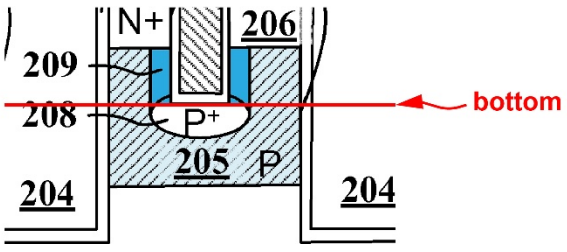
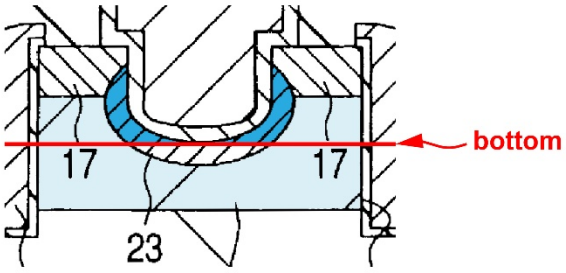
This structure satisfies the requirement that the trenches be "formed on the top of said interlayer oxide film" and "extend downwardly through said source layer to a portion of said base layer." (*Id*. ¶473.)

Accordingly, Uno teaches limitation *[1f-1]*. (*Id*.¶¶470-73.)

ii. [1f-2]

This claim sub-element is taught by Uno or, at minimum, rendered obvious in view of Uno combined with the knowledge of a POSITA. (*Id*. ¶474.)

[1f-2]
lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

Uno identifies region 23 as a "p^+-semiconductor region (back gate contact region)." (Ex. 1006, 5:54–55.) In MOSFET terminology, "back gate contact" is synonymous with "body contact."(Ex. 1003, ¶475.) The annotated portions of region 23 align with the "lateral contact layer" recited in this limitation, as they are positioned along the sidewalls of the source contact trenches. (*Id*.) While Uno does

not explicitly subdivide region 23 into lateral and bottom sub-regions, the darker blue annotated portion corresponds to the lateral contact layer as described in the ’634 Patent. (*Id.*)

The rationale for this contact structure would have been well-known to a POSITA. (*Id*. ¶¶476-79.) It is standard practice in transistor fabrication to form body contacts using heavily doped silicon (e.g., P^+ or N^+), ensuring a low-resistance ohmic interface with the metal contact. (*Id*. ¶477.) Contacting lightly doped silicon would risk high resistance or a non-ohmic Schottky junction—both undesirable. (*Id*.)

Uno explicitly acknowledges the need for low contact resistance between metal and semiconductor, stating that the source contact interfaces with the body region through a heavily doped (P^+) surface layer. (Ex. 1006, 9:17–19.) If both P^+ and P* layers are sufficiently doped to qualify chemically as P^+, they provide the necessary low-resistance ohmic behavior for the source-body contact interface. (Ex. 1003, ¶478.)

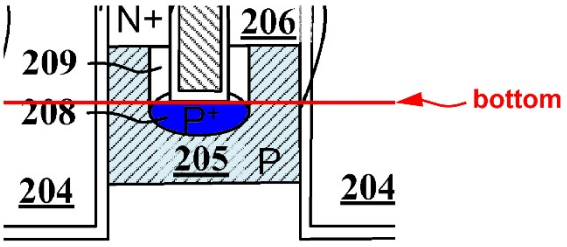
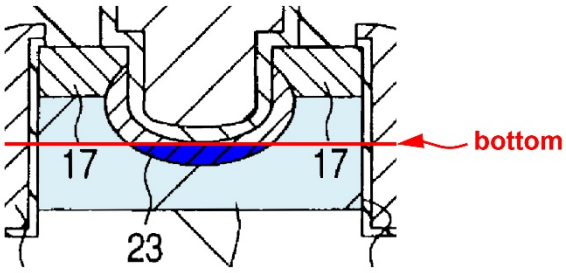
To “surround” the source-body contact, the heavily doped P^+ region must extend along the trench sidewalls within the body region. This is exactly what is depicted in Uno, where region 23 extends along the sidewalls—constituting the lateral contact layer. (*Id*. ¶480.)

Accordingly, Uno teaches or renders obvious the structure of limitation *[1f-2]*. (*Id*. ¶¶475-80.)

iii. [1f-3]

Uno discloses that trench 21s extends into a portion of the base layer, and that the P^+ region 23 covers the bottom and sidewalls of the trench within the base layer, forming an ohmic contact to the base region. (Ex. 1006, 15:10–13, 15:31–36; FIG. 6.) The annotated portion of region 23 shown in darker blue in FIG. 38 below corresponds to the "base contact layer" as defined in the '634 Patent. Although Uno does not explicitly separate the P^+ region into sub-regions, its structure and placement satisfy this limitation. (Ex. 1003, ¶482.)

[1f-3]
P-type base layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

As established in the claim construction, the ’634 Patent defines the base contact layer as a heavily doped region at or below the trench bottom within the base layer. That is precisely what is shown in Uno. (*Id*. ¶483.)

Further, a POSITA would be aware that it has long been standard practice to form the metal-base contact at a heavily doped trench bottom to ensure low-resistance ohmic behavior. (*Id*. ¶¶484, 282-84, 290.)

Accordingly, Uno discloses that the bottom base of the trench is covered by a base contact layer, thereby teaching limitation *[1f-3]*. (*Id*. ¶¶481-84.)

2. Dependent Claim 2

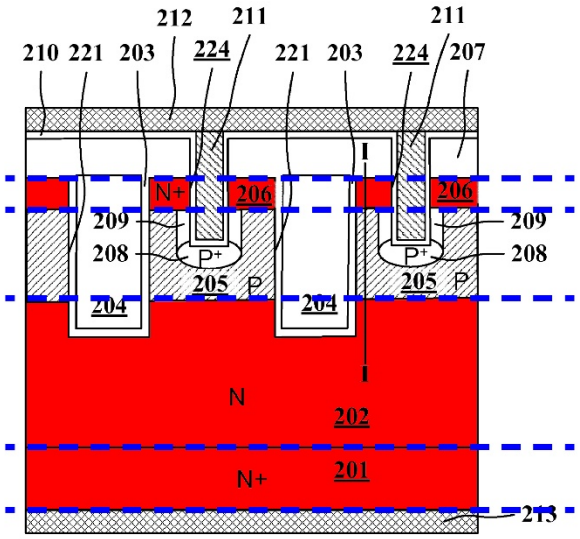
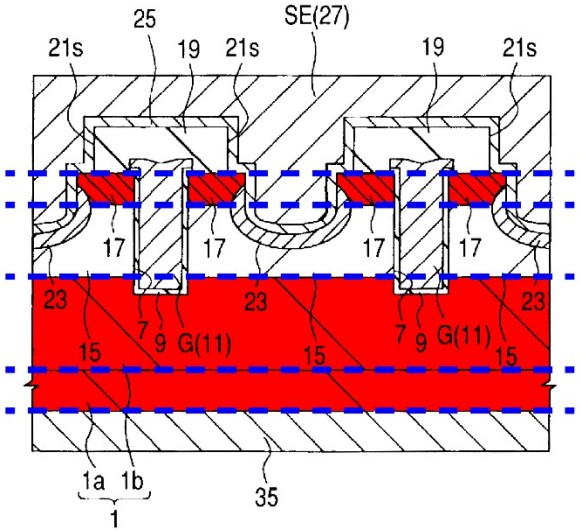
Claim 2 is rendered obvious based on the analysis of Claim 1 and the additional discussion below. (*Id.* ¶¶486-517.)

a. Limitation [2a]

Limitation *[2a]*: Uno provides an N-type silicon substrate (1a), an N-type epitaxial layer (1b), and an N-type source layer (17), corresponding to elements 101/201, 102/202, and 106/206 of the ’634 Patent. (Ex. 1006, FIGs. 36-38; Ex. 1003, ¶¶490, 493.)

[2a]

N-type silicon substrate, epitaxial layer, & source layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno discloses "an n-single crystal silicon substrate 1a" and a "single crystal silicon layer 1b" epitaxially grown on top. (Ex. 1006, 4:55–59; FIGs. 1, 3, 5, 6, 8–9, 11–18, 20, 36–38, elements 1a, 1b.) Epitaxial layer 1b serves as the drain-side region of the vertical device structure, consistent with the '634 Patent. (Ex. 1003, ¶494.)

Above this structure, Uno describes "an n^+-semiconductor region 17" functioning as the source layer. This heavily doped region lies above the P-type channel region 15 and is used for forming the source contact. (Ex. 1006, at 5:29–31, 5:35–36, 5:43–44, 6:10–11, 6:26–27, 8:25–29, 8:44, 8:60–61; FIGs. 5, 6, 8–9, 11–18, 20–22, 24–25, 36–38; Ex. 1003, ¶495.)

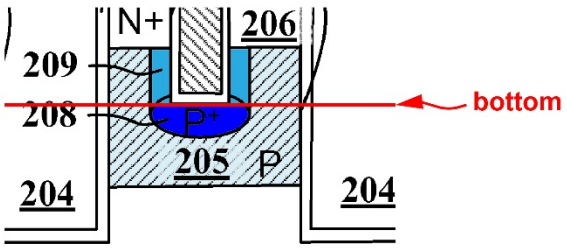
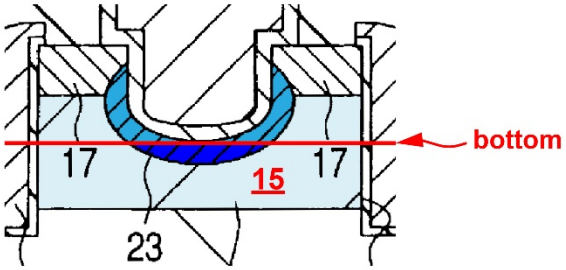
Accordingly, Uno discloses a vertically layered semiconductor structure with an N-type substrate, an N-type epitaxial layer, and an N^+-type source layer, teaching limitation *[2a]*. (Ex. 1003, ¶¶489-96.)

b. Limitation [2b]

Uno provides a P-type base layer and a lateral contact layer corresponding to elements 105/205 and 209 of the ’634 Patent. (Ex. 1003, ¶497.) The ’634 Patent identifies the body regions as subsets of the larger base layer. Uno discloses a “p– semiconductor region (channel region) 15,” which functions as the P-type base/body layer in the vertical MOSFET structure. (Ex. 1006, 5:65; FIGs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38; claims 1, 12, 16, 18, 25, 29, 31, 33–36.) Uno also teaches a “p^+-semiconductor region (back gate contact region) 23,” formed within the P-type base layer. (*Id*. at 5:54–65, 6:11–13, 8:40–43, 8:52; FIGs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38.) A portion of region 23 lies along the sidewalls of the source contact trench and corresponds to the “lateral contact layer” described in the ’634 Patent, providing an ohmic path between the base and the source contact. (Ex. 1003, ¶¶497-98.)

[2b]

P-type base layer & lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

The ’634 Patent draws a distinction between the lateral contact layer—depicted in medium blue in annotated FIG. 2G above—as being formed along the trench sidewalls above the trench bottom, and the base contact layer—shown in dark blue—which is formed at or below the trench floor. (Ex. 1001, 5:9–12; 3:50–55.) This distinction is consistent with Uno’s disclosure, in which a portion of region 23 lies above the trench bottom within the P-type base layer and therefore constitutes the P-type lateral contact layer. (Ex. 1006, 5:59–61; Ex. 1003, ¶¶499-500.)

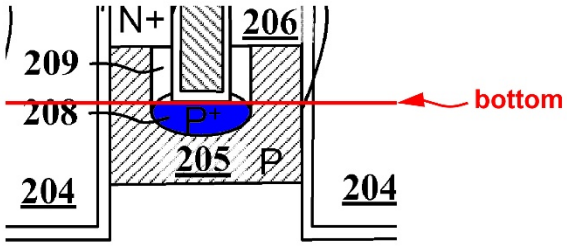
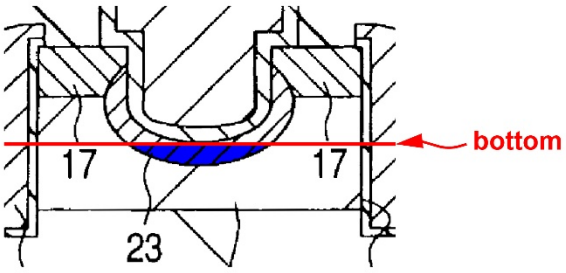
Accordingly, Uno discloses both a P-type base layer (15) and a P^+-type lateral contact layer (23). These disclosures teach limitation *[2b]*. (1003, ¶¶497-501.)

c. Limitation [2c]

Uno provides a P-type base contact layer corresponding to element 108/208 of the ’634 Patent. The ’634 Patent defines this layer as a P^+ diffusion region formed at or beneath the bottom of the source contact trench, providing ohmic contact to the deeper portion of the P-type base. (Ex. 1001, 3:50–55; 5:9–12.)

[2c]

P-type base contact layer at bottom of source contact trenches

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

Uno discloses a corresponding structure: a “p^+-semiconductor region (back gate contact region) 23,” formed within the P-type base region. (Ex. 1006, 5:54–64, 6:13, 8:40–42, 8:51–52; FIGs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38; Ex. 1003, ¶503.) A portion of region 23 lies at or beneath the bottom of the source contact trench (element 21s), and in direct contact with the underlying P-type channel region (element 15). Its vertical placement and function—providing ohmic contact to the body—mirror the base contact layer described in the ’634 Patent. (Ex. 1003, ¶503.)

While Uno refers to region 23 as a "back gate contact region," its structure and function are consistent with a base contact layer. It is distinct from the lateral contact layer, which the '634 Patent describes as being formed along the trench sidewalls above the trench bottom. (*Id*. ¶504.)

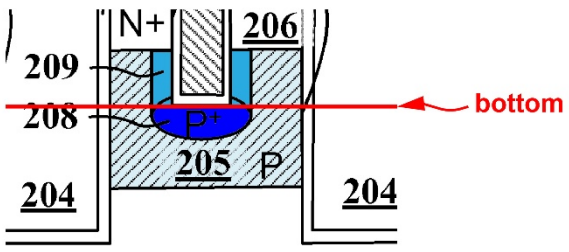
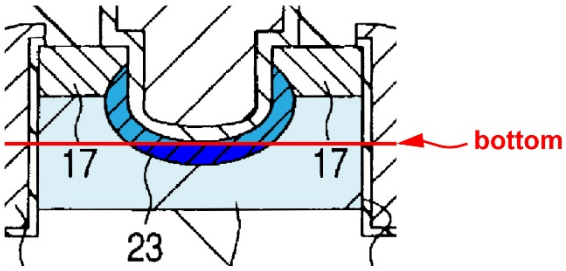
Accordingly, Uno discloses a P-type base contact layer at the bottom of the source contact trenches. This teaches limitation *[2c]*. (*Id*. ¶¶502-05.)

d. Limitation [2d]

This limitation is rendered obvious by Uno as understood by a POSITA. (*Id*. ¶506.) As expressly stated in the '634 Patent, the lateral contact layer is formed along the sidewalls of the source contact trench above the trench bottom, while the base contact layer is formed at or beneath the trench bottom. (Ex. 1001, 5:9–12; 3:50–55.)

[2d]

lateral contact layer has less doping concentration than the base contact layer at bottom

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

Uno discloses a P^+-type region 23 ("back gate contact region") formed within the P-type base region 15 and adjacent to the source contact trench 21s. (Ex. 1006, 5:54–55, 5:58–64; FIGs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38.) As annotated in FIG. 38, the portion of region 23 located above the trench floor corresponds to the lateral contact layer, while the portion at or below the trench bottom corresponds to the base contact layer. (Ex. 1003, ¶508.)

Uno's teaches various trench geometries including tapered and vertical. (*Id*. 508-511.) During ion implantation, any angled geometry causes the sidewalls to receive a lower dopant dose than the trench bottom due to increased projected surface area. (*Id*.) The trench bottom, being flat and perpendicular to the ion beam, receives a higher dopant concentration. Thus, even though Uno describes region 23 as a single P^+ region, the doping concentration inherently varies—being higher at the trench bottom than along the sidewalls. (*Id*. ¶¶509-10.)

This behavior follows from the physics of ion implantation and is confirmed by Uno's disclosure that boron fluoride (BF_2) is implanted and then diffused to form region 23. (Ex. 1006, 5:52–55; 6:11–13; Ex. 1003, ¶511-12.) Implantation followed by thermal diffusion is a well-established doping technique. (Ex. 1022, p. 475.)

Under principles of inherency, structures or properties that necessarily result from a disclosed process are considered disclosed—even if not expressly

appreciated by the prior art. (*Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999), holding "[T]he discovery of a previously unappreciated property of a prior art composition, or of a scientific explanation for the prior art's functioning, does not render the old composition patentably new to the discoverer.") Here, Uno's trench geometry and implantation method necessarily produce a lateral contact layer with lower doping concentration than the base contact layer. This outcome is supported by long-standing technical literature, including Berberich *et al.,* which confirms that trench sidewall doping is inherently lower than trench-bottom doping due to implantation angle and ion reflection. (Ex. 1021, pp. 379–82.)

Further, as discussed in relation to Hshieh ('384) in Ground 1, Monte Carlo method simulations conclusively demonstrate that tapered source contact trench sidewalls inherently receive a lower dopant concentration than the trench bottom. (Ex. 1003, ¶¶339-40.)

Accordingly, Uno discloses a lateral contact layer with lower doping concentration than the base contact layer, teaching limitation *[2d]*. (Ex. 1003, ¶¶506-17.)

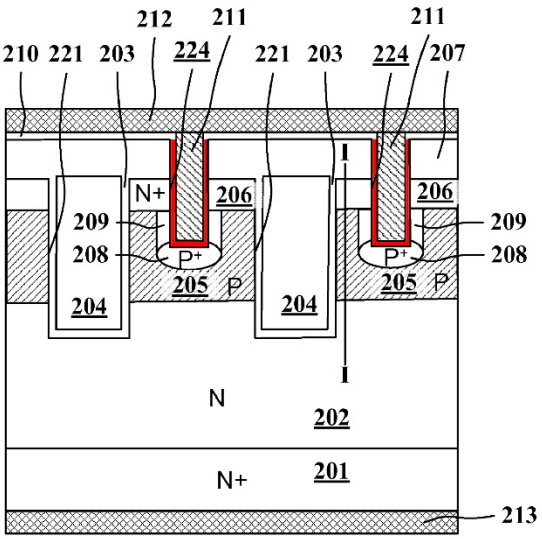
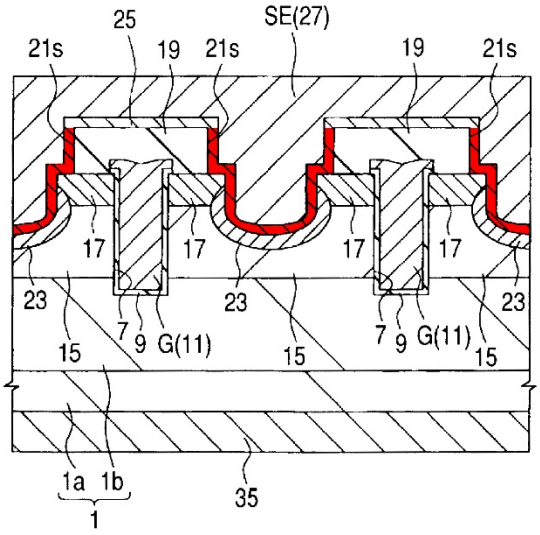
3. Dependent Claim 3

Claim 3 is rendered obvious based on the analysis of Claim 2 and the additional discussion below. (Ex. 1003, ¶¶518-30.)

a. Limitation [3a]

Uno teaches a barrier metal layer corresponding to element 110/210 of the ’634 Patent. The ’634 Patent describes this layer as a Ti/TiN or equivalent film positioned between the tungsten plug and the underlying oxide or silicon, preventing metal diffusion and improving contact integrity by serving as an adhesion layer. (Ex. 1001, 5:15–20; 6:18–20; FIGs. 2F–2G, 15.)

[3a]
barrier metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

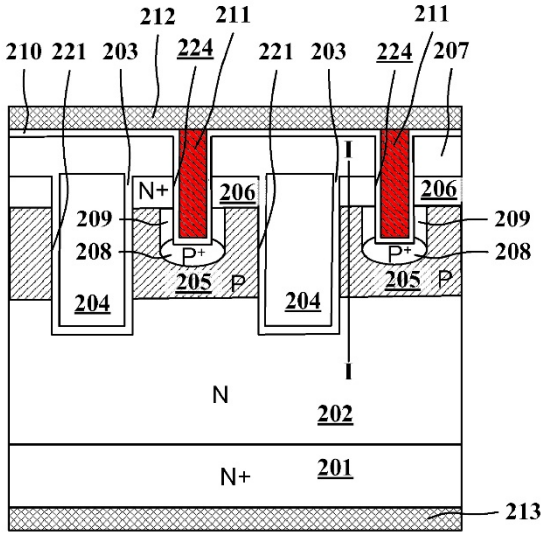
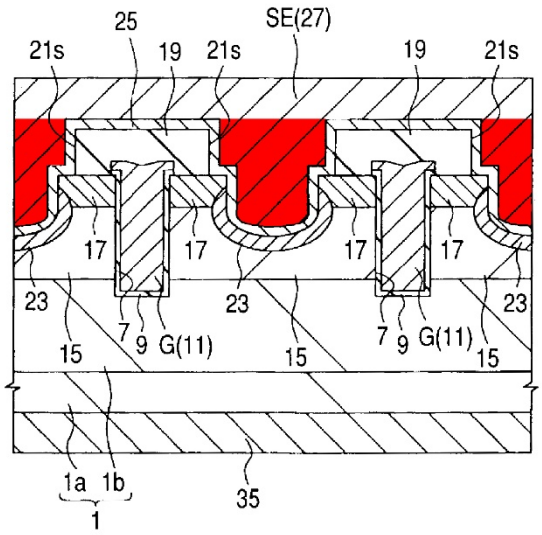
Uno discloses a structurally and functionally equivalent barrier layer. (Ex. 1003, ¶524.) It identifies element 25 as a “barrier film (barrier metal film)” made of TiN formed at contact locations to prevent undesired reaction layers or underlayer diffusion. (Ex. 1006, 1:23–25, 14:61–67, 15:18–20, 15:30–37.)

Accordingly, Uno discloses a barrier metal layer that is structurally and functionally consistent with the barrier metal layer described in the ’634 Patent, teaching limitation *[3a]*. (Ex. 1003, ¶¶523-26.)

b. Limitation [3b]

Uno provides contact metal plugs corresponding to element 111/211 of the ’634 Patent. The ’634 Patent defines these plugs as conductive materials—such as tungsten—deposited into the source contact trench to establish electrical connection between the buried contact regions and the upper metal interconnect. (Ex. 1001, 5:13–20, 5:44–46; FIGs. 2F–2G.)

[3b]
contact metal plugs

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Uno discloses a structurally and functionally equivalent feature. It states:

> "The embodiment described above may also be applied to a conductive portion connected electrically with the source or drain and well (for example, plugs or wiring portions)." (Ex. 1006, 16:12–15.)

A POSITA would recognize that such conductive structures—extending from the body region to the top metal layer—were conventional and consistent with standard industry practices at the time. Uno's disclosure aligns with this understanding and reflects the common use of metal plugs within source contact trenches. (Ex. 1003, ¶528-29.)

Accordingly, Uno teaches contact metal plugs consistent with the structure and function of the '634 Patent, teaching limitation *[3b]*. (*Id*. ¶¶527-30.)

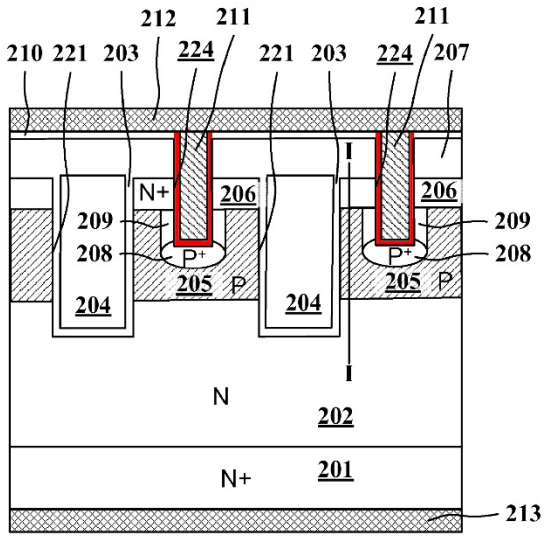
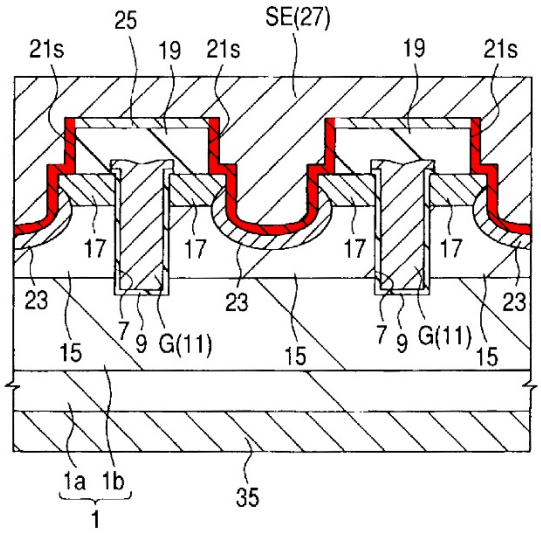
4. Dependent Claim 4

a. Limitation [4a]

Uno teaches *[4a]* by disclosing a barrier metal layer composed of Ti/TiN, corresponding to element '634-110/210 of the '634 Patent. Uno explicitly states that "[i]n addition to Ti, TiN (titanium nitride) may also be used" as a barrier metal material. (Ex. 1006, 13:9–10; Ex. 1003, ¶¶534-35.) Further, a POSITA would have recognized that a Ti/TiN barrier layer was a conventional combination, selected for its known reliability and compatibility with standard semiconductor fabrication processes. (Ex. 1003, ¶¶536-45.)

[4a]

barrier metal layer is Ti/TiN

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

This disclosure confirms that Uno identifies Ti and TiN—either individually or in combination—as suitable barrier metal materials, consistent with the '634 Patent's designation of Ti/TiN as the preferred composition for the barrier metal layer. (*Id*. ¶¶534-35.)

Accordingly, Uno discloses a Ti/TiN barrier metal layer and teaches limitation *[4a]*. (*Id*. ¶¶534-46.)

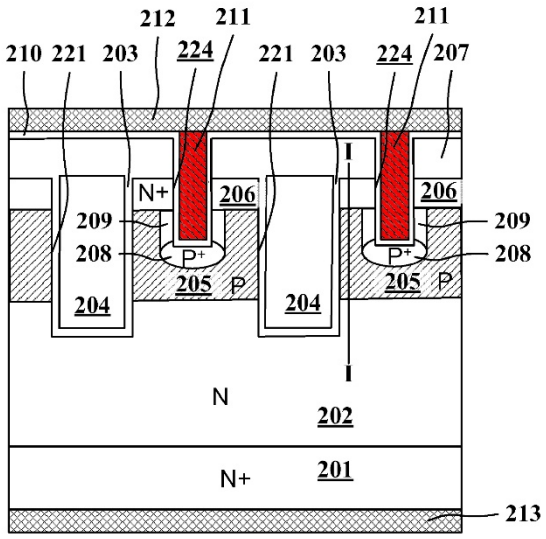
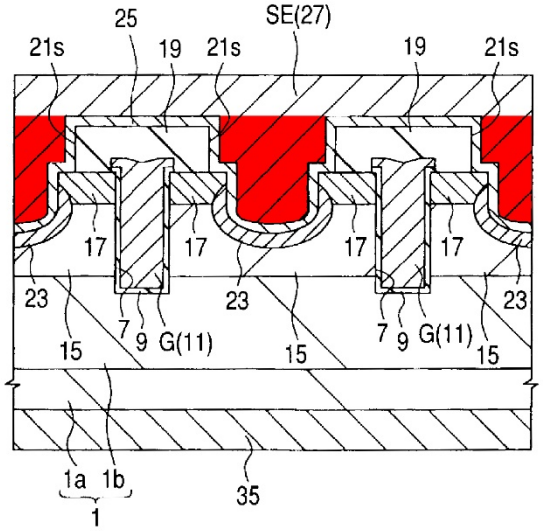
b. Limitation [4b]

Limitation *[4b]* is rendered obvious by Uno. While Uno describes an aluminum plug structure (element 27), a POSITA would have recognized that tungsten was the industry-standard contact plug material at the time of the '634

Patent. By the 1990s, tungsten had largely replaced aluminum in contact plug applications due to its superior resistance to spiking, better compatibility with scaled geometries, and more reliable ohmic contact formation—particularly when used in conjunction with barrier layers such as Ti or Ti/TiN. (Ex. 1008, p. 281; Ex. 1003, ¶¶537-45.)

[4b]

contact metal plug is Tungsten

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

Given Uno's disclosure of a plug structure and the widespread adoption of tungsten plugs in conventional semiconductor processes, a POSITA would have been motivated to substitute tungsten for aluminum and would have had a reasonable expectation of success in doing so. (Ex. 1003, ¶545.)

Accordingly, the use of tungsten for the contact metal plug is rendered obvious over Uno, teaching limitation *[4b]*. (*Id*. ¶537-45, 547.)

5. Dependent Claim 5

Claim 5 is rendered obvious based on the analysis of Claim 4 and the additional discussion below. (Ex. 1003, ¶¶548-50.)

Uno discloses that, following the formation of a silicon oxide film, element 19 is etched in a patterned manner to form various shapes of "contact trenches (source contact) 21s." Uno explicitly considers the shape of the contact trench to improve coverage. As shown in FIGs. 36–38 of Uno, the contact trench may have either a vertical profile or a tapered profile. (Ex. 1006, 15:2–5, 15:18–20, 15:29–30, 15:35–36; FIGs. 9, 11, 12, 15, 16, 18, 20, 24, 36–38.)

Ex. 1006 ('864 Uno)

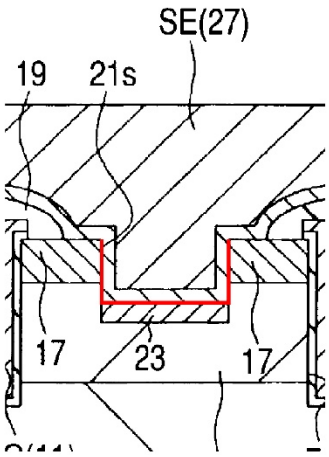


Fig. 36 (Annotated partial enlarged view)

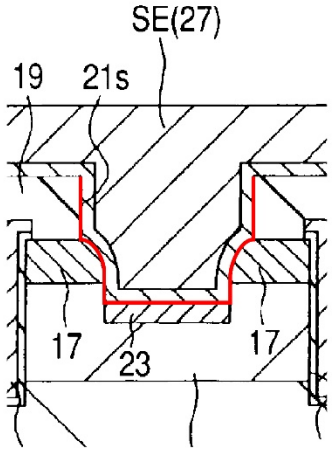


Fig. 37 (Annotated partial enlarged view)

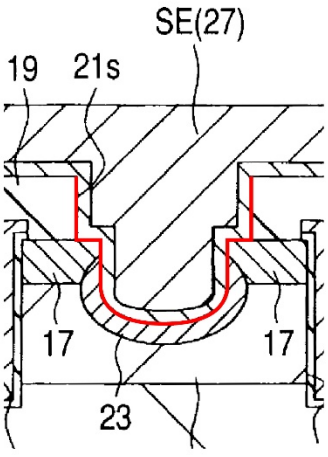


Fig. 38 (Annotated partial enlarged view)

Additionally, a POSITA would have recognized that, by 2008, it was well known in the art that source contact trenches could have vertical or tapered profiles. (Ex. 1003, ¶550.)

Accordingly, Uno alone and in view of the knowledge of a POSITA, teaches the subject matter of Claim 5. (*Id*. ¶¶548-50.)

6. Dependent Claims 6 - 9

Claims 6-9 are rendered obvious in view of the analyses of Claims 1 and 2-5, along with the additional discussion below. (*See* VIII.B.2–5; Ex. 1003, ¶¶551-64.)

Claims 6–9 mirror the limitations of Claims 2–5 with reversed dopant polarity. As such, the analysis set forth in Grounds 2 for Claims 2–5 applies equally to Claims 6–9, with no substantive deviation. (*See* VIII.B.1–5.)

C. Ground 3: Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as Obvious Over Hshieh ('384) and Uno ('864) (and *vice versa*)

1. Independent Claim 1

Petitioner respectfully contends that claim 1 is unpatentable over both Hshieh and Uno as discussed in Grounds 1 and 2 above.

To the extent the Patent Owner argues that Hshieh fails to teach one or more limitations, it would have been obvious to a POSITA to modify Hshieh with Uno.

Likewise, to the extent the Patent Owner argues that Uno fails to teach one or more limitations, it would have been obvious to a POSITA to modify Uno with Hshieh.

Combination of Hshieh and Uno (or Uno and Hshieh) is discussed in more detail below with respect to pertinent claim limitations.

a. [Preamble]

The *[Preamble]* is disclosed by both Hshieh and Uno, as explained in Grounds 1 (Sections VIII.A.1.a; Ex. 1003, ¶¶175-89) and 2 (Section VIII.B.1.a; Ex. 1003, ¶¶392-404.)

b. Limitation [1a]

Limitation *[1a]* is disclosed by both Hshieh and Uno as explained in Grounds 1 (Sections VIII.A.1.b; Ex. 1003, ¶¶190-233) and 2 (VIII.B.1.b; Ex. 1003, ¶¶405-47.)

c. Limitation [1b]

Limitation *[1b]* is disclosed by both Hshieh and Uno as explained in Grounds 1 (Sections VIII.A.1.c; Ex. 1003, ¶¶234-39) and 2 (Sections VIII.B.1.c; Ex. 1003, ¶¶448-53.)

d. Limitation [1c]

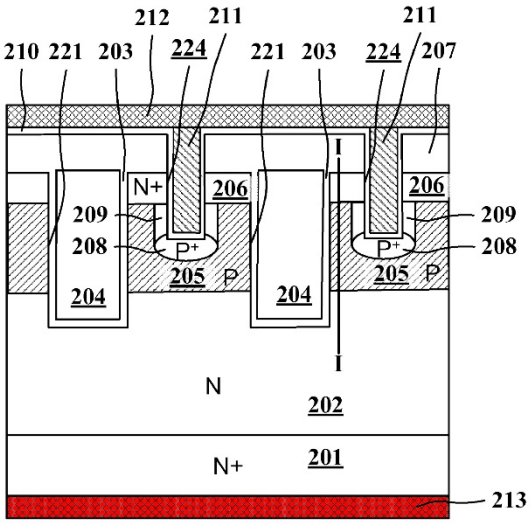
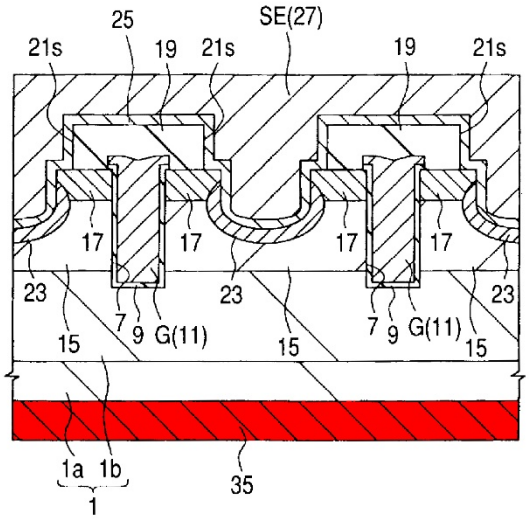
Limitation *[1c]* is disclosed by both Hshieh and Uno, as explained in Grounds 1 (Sections VIII.A.1.d; Ex. 1003, ¶¶240-43) and 2 (VIII.B.1.d.) (Ex. 1003, ¶¶454-57.)

e. Limitation [1d]

As explained in Ground 1, Hshieh discloses limitation *[1d]*. (Section VIII.A.1.e; Ex. 1003, ¶¶244-64.) Hshieh's structure inherently includes a bottom metal layer, which is not explicitly shown in the figures but is nonetheless fully supported by the disclosure of Hshieh ('384). (*Id.,* ¶567.) As explained in Ground 2, Uno also discloses limitation *[1d]*. (Section VIII.B.1.e; Ex. 1006, 7:25; Ex. 1003, ¶¶458-62.) Uno states that "the stacked film 35 forms a lead electrode (drain electrode DE) for the drain (1a, 1b)," describing a conductive layer applied to the bottom of the device for electrical contact with the drain. (FIGs. 11–12, 15, 16, 18, 20, 24, 36–38.) This drain electrode is positioned beneath the epitaxial and substrate layers and performs the same function and structural role as the bottom metal layer recited in the '634 Patent.

[1d]

bottom metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

Accordingly, to the extent the Patent Owner argues that Hshieh fails to teach or suggest a bottom metal layer, it would have been obvious to a POSITA to implement a bottom metal layer on Hshieh's device, as taught by Uno. (Ex. 1003, ¶575.) This modification would represent a standard approach to forming a drain contact in trench MOSFET devices and would have been both routine and expected in the field. (*Id.*)

Accordingly, limitation *[1d]* would have been apparent to a POSITA in view of the combined teachings of Hshieh and Uno. (*Id.* ¶¶572-75.)

f. Limitation [1e]

Limitation *[1e]* is disclosed by both Hshieh and Uno, as explained in Grounds 1 (Section VIII.A.1.f; Ex. 1003, ¶¶244-70) and 2 (Section VIII.B.1.f.; Ex. 1003, ¶¶463-67.)

g. Limitation [1f]

Limitation *[1f]* is disclosed by both Hshieh and Uno, as explained in Grounds 1 (Section VIII.A.1.g; Ex. 1003, ¶¶271-306) and 2 (Section VIII.B.1.g; Ex. 1003, ¶¶468-84.)

2. Dependent Claims 2-9

The limitations of claims 2-9 are disclosed by both Hshieh and Uno, as explained in Grounds 1 and 2. (Section VIII.A.2 – Section VIII.A.6; Ex. 1003, ¶¶298-386); Section VIII.B.2 – Section VIII.B.6; Ex. 1003, ¶¶486-564.)

3. Motivation to Combine

A POSITA would have been motivated to combine Hshieh and Uno with a reasonable expectation of success. (Ex. 1003, ¶¶569-72.) The proposed combination involves the predictable application of known elements to achieve well-understood functions in trench-gated, vertical-conduction-path MOSFETs. (*Id.* ¶570) Moreover, the features disclosed by Hshieh and Uno could be readily implemented into one another's architectures without undue experimentation or inventive effort. (*Id.* ¶571.) Both references rely on conventional and well-

established silicon fabrication techniques, further supporting a POSITA's reasonable expectation of success. (*Id.*)

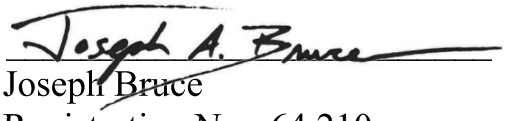
A POSITA would thus be motivated to modify Hshieh's MOSFET to incorporate Uno's bottom metal layer. Conversely, a POSITA would also be motivated to implement features from Hshieh—such as its source contact structure, barrier metal made of TiN, and plugs made of Tungsten—into Uno's architecture. Patent Owner's admitted prior art, as illustrated in FIG. 1 (Admitted Prior Art) of the '634 Patent, reflects the state of the art at the time and supports a POSITA's background knowledge, further reinforcing the motivation to combine these references. (*Id.* ¶572.)

IX. CONCLUSION

For the foregoing reasons, Petitioner respectfully asks that inter partes review of the '634 Patent be instituted and Claims 1-9 of the '634 Patent be found unpatentable and canceled.

Respectfully submitted,

Dated: August 15, 2025

By: 

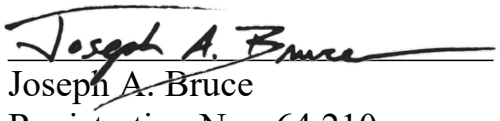
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CERTIFICATE OF COMPLIANCE

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,885 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: August 15, 2025 By: 

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CERTIFICATE OF SERVICE

I hereby certify that on August 15, 2025, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,629,634 under 35 U.S.C. § 311-319 and 37 C.F.R. § 42.100 Et Seq.
- Exhibits 1001 – 1026
- Power of Attorney

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