IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EXCELLIANCE MOS CORPORATION,

Petitioner

v.

FORCE MOS TECHNOLOGY CO., LTD.,

Patent Owner

Case No.: IPR2025-01433

U.S. Patent No. 7,629,634

DECLARATION OF DR. DANIEL FOTY IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,629,634

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I. INTRODUCTION

1. I have been retained by counsel for Excelliance Mos Corporation ("Excelliance" or "Petitioner") in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of Claims 1-9 (the "Challenged Claims") of U.S. Patent No. 7,629,634 (the "'634 Patent" or the "Challenged Patent").

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration–supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly-introduced items.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the "Board")) the technology disclosed in the Challenged Patent–including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein; this may include (among other things) background information on MOS transistor technology, silicon trench technology, integrated circuit process development, and integrated circuit manufacturing.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in electronics technology are set forth in my curriculum vitae–Ex. 1004–which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in semiconductor process development and manufacturing, in RF technology for wireless communications, in technology development, and in technical and business development.

5. My curriculum vitae contains further details regarding my experience, education, and other qualifications which allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

6. I am being compensated for my work in this matter at an hourly rate of $600 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this investigation.

IV. MATERIALS CONSIDERED

7. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

EXHIBIT	DESCRIPTION
1001	U.S. Patent No. 7,629,634 (the "'634 Patent")
1002	File History of the '634 Patent
1003	Expert Declaration of Dr. Daniel Foty
1004	Expert Curriculum Vitae of Dr. Daniel Foty
1005	U.S. Patent Publication No. 2006/0273384 A1 ("Hshieh ('384)")
1006	U.S. Patent No. 6,984,864 ("Uno ('864)")
1007	B. Davari et al., *A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS*, International Electron Devices Meeting, 92-95 (1988)
1008	Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 191, 281, 385-387 (1990)
1009	S. Van Huylenbroeck et al., *A 0.25um SiGe BiCMOS Technology Including Integrated RF Passive Components Optimised for Low Power Applications*, European Solid State Device Research Conference (ESSDERC), 505-508 (2003)
1010	U.S. Patent No. 5,395,786.
1011	H. Shichijo et al., *Trench Transistor DRAM Cell*, *IEEE Electron Device Letters*, Vol. 7, 119-121 (1986)
1012	*Metal Insulator Semiconductor Field Effect Transistors (MISFETs)*, EEEGUIDE, https://www.eeeguide.com/metal-insulator-semiconductor-field-effect-transistors-misfets/ (last visited July 31, 2025)
1013	Adel S. Sedra and Kenneth C. Smith, *Microelectronics Circuits*, 237 (5th ed. 2004)
1014	U.S. Patent No. 4,980,747
1015	Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 1, 124, 187-

	191 (1986)
1016	Ashwin H. Shah et al., *A 4-Mbit DRAM with Trench-Transistor Cell*, IEEE Journal of Solid State Circuits, Vol. SC-21, 618-626 (1986)
1017	*Properties of SiO_2 and Si_3N_4 at 300K*, Comprehensive Reference on EESEMI Semiconductor Manufacturing, https://eesemi.com/sio2si3n4.htm (last visited July 31, 2025)
1018	A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 (1967)
1019	*Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG, E.D. Tex. (Marshall) 2022, ECF No. 416, 143, 146~147 (Trial Transcript Excerpt)
1020	Genshu Fuse et al., *Indirect Trench Sidewall Doping by Implantation of Reflected Ions*, Applied Physics Letters, Vol. 54, 1534-1536 (1989)
1021	S. E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 379-382 (2003)
1022	Michael Quirk and Julian Serda, *Semiconductor Manufacturing Technology*, 475 (2001)
1023	A. Agrawal et al., *Self-Sealed Circular Channels for Micro-Fluidics, Sensors and Actuators (A: Physical)*, 80-87 (2006)
1024	D. Edelstein et al., *Full Copper Wiring in a Sub-0.25 um CMOS ULSI Technolog*y, IEDM Technical Digest, 773-776 (1997)
1025	S. Nizou et al., *Deep Trench Doping by Plasma Immersion Ion Implantation in Silicon*, Ion Implantation Technology: 16th International Conference on Ion Implantation Technology, 229-232 (2006)
1026	*Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG, E.D. Tex. (Marshall), 2022, ECF No. 132, 13-17.

8. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, demonstratives, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony. I note here that citations in this declaration are to the "endorsed" page numbers placed by counsel in the lower right corner of each exhibit.

9. My conclusions and opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and silicon technology principles in reaching my conclusions and forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

10. I am not an attorney, but I have been informed of several legal principles–which I have employed in reaching my conclusions and in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

1. Claim Construction

11. I have been informed that the claims of the Challenged Patent in this proceeding are to be construed using the same claim construction standard applied in district court. I have been informed that claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called "intrinsic evidence." I have been further informed that the meaning of a claim term may also be guided by "extrinsic evidence," such as contemporaneous dictionaries and treatises, as well as the testimony of technically-skilled witnesses such as myself.

2. Burden of Proof

12. I have been informed that the petitioner in an inter partes review bears the burden of establishing unpatentability by "a preponderance of the evidence." I have been further informed and understand that, to prove an assertion by "a preponderance of the evidence," the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Obviousness

13. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the claimed invention. I have been further informed that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and "secondary considerations" or objective indicia of non-obviousness.

14. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

15. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a

patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

16. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

17. I have also been informed that an obviousness analysis can involve identification of one-or-more physical principles upon which the teachings of the challenges rely and that were well known in the art–but which are not discussed (either explicitly or implicitly) in the Challenged Patent or in specific prior-art references. Further, I have been informed—and understand—that recognition of the underlying physical principles in the POSITA at the time of the invention is not required, so long as those principles were inherently present in the prior art. Inherency does not require that a POSITA recognize the principle or result at the

time; it is sufficient that the claimed feature or outcome necessarily flows from the prior art disclosure.

18. I have been informed that various "secondary considerations" (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

19. Copying: evidence that others, including the accused infringer, copied the patented invention.

20. Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.

21. Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

22. Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.

23. Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

24. Praise: evidence of praise directed to an invention by others in the field.

25. Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

26. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a "nexus" between the claimed invention and the evidence proffered on secondary considerations (e.g., proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Filing Date

27. I have been informed that the '634 Patent does not claim priority to an earlier filed application. I have been instructed by counsel for Petitioner to use February 23, 2008 (the "Filing Date") as the Filing Date for all claims of the '634 Patent.

C. Level of Skill in the Art

28. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

29. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

30. The ’634 Patent generally pertains to the field of silicon process technology and silicon manufacturing technology–and more particularly to the development, manufacturing, and operation of trench-based silicon MOSFETs and the operational behavior of such devices.

31. Thus, a person of ordinary skill in the art (“POSITA”) in the technology field of the ’634 Patent at the Filing Date would have had at least a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience with the development and manufacture of integrated circuits containing trench structures–such as trench-based silicon

MOSFETs. This background would include a working knowledge of semiconductor fabrication processes and integrated circuit manufacturing, including the principles ion implantation. A Master's or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.

32. I was at the time of the alleged invention at least a POSITA in the art relevant to the Challenged Patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2008–and I am familiar with how a POSITA would have understood and used the terminology found in the '634 Patent when filed, and with the state of the art at that time.

VI. SUMMARY OF OPINIONS

33. I have been asked to evaluate the patentability of the claims of the '634 Patent in view of the prior art references listed above in Section IV. Based on my evaluation and analysis, it is my conclusion and opinion that, as of the '634 Patent's Filing Date, the Challenged Claims are unpatentable as being rendered obvious by a particular reference Hshieh ('384) when combined with the knowledge of a POSITA (Ground 1); unpatentable as being rendered obvious by a particular reference Uno ('864) when combined with the knowledge of a POSITA (Ground 2); and are also unpatentable as being rendered obvious by that same reference when combined with other references and vice versa (Ground 3). The

table below summarizes the prior art references that, in my opinion, render the Challenged Claims unpatentable as obvious under pre-AIA 35 U.S.C. § 103(a):

Ground	Prior Art References
1	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Hshieh (’384)
2	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Uno (’864)
3	Unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Hshieh (’384) in view of Uno (’864) (and *vice versa*)

34. My substantive analysis in Section XI will explain in detail why I have concluded that the three Grounds listed above render the Challenged Claims unpatentable.

35. Further, I reserve the right to cite and rely on additional portions of the cited prior art in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

36. Before considering the ’634 Patent in detail, some background on the technology of the ’634 Patent should be considered. This involves some basic concepts of silicon integrated circuit development, manufacturing, and functionality.

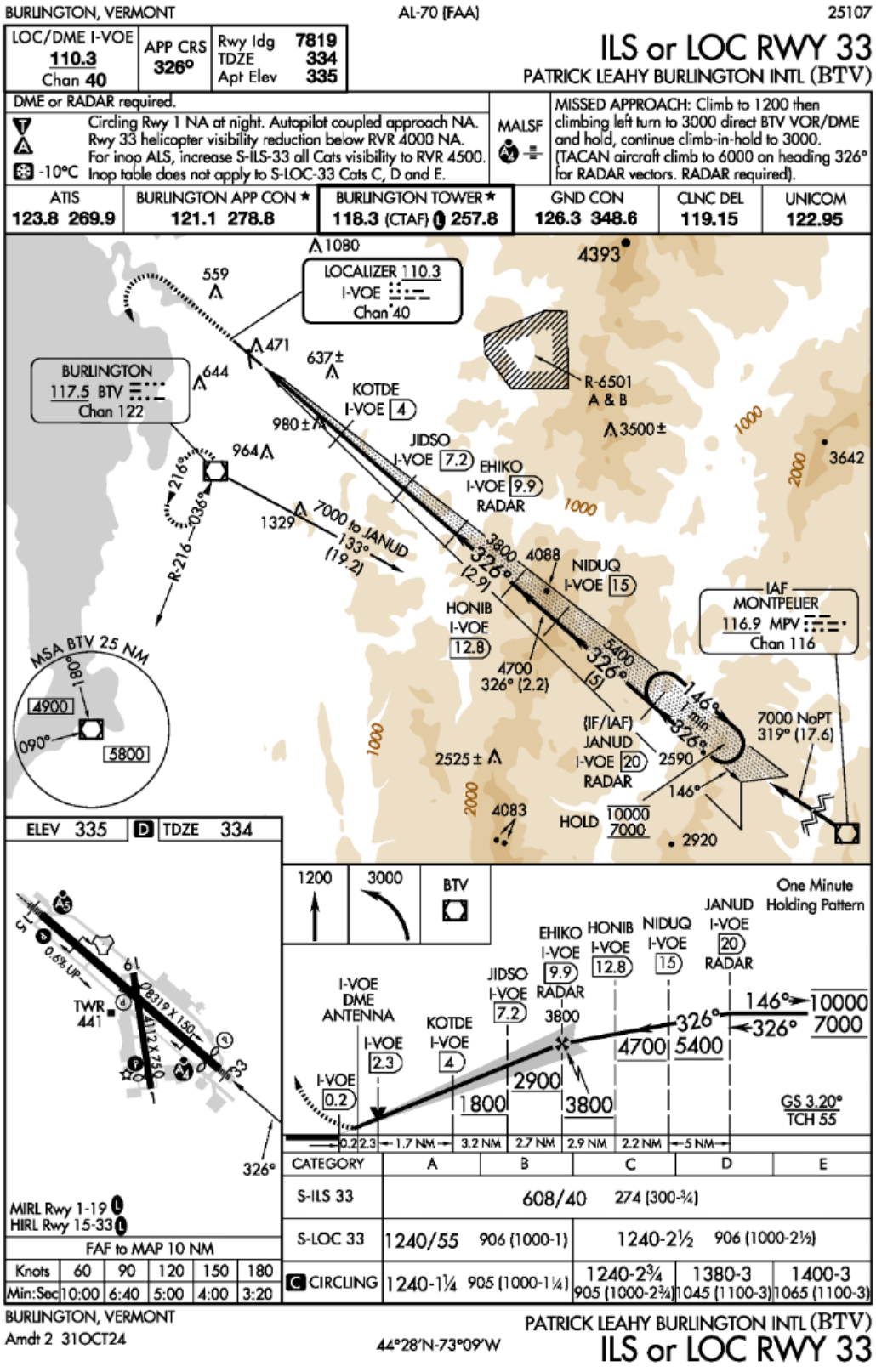
A. Integrated Circuits

37. While the now-ubiquitous silicon-based integrated circuit (i.e., the so-called "silicon chip") has a long and interesting history, it can be noted that the unique properties of silicon allowed for the development of the metal-oxide-semiconductor (MOS) transistor, and for its use in a circuit technology known as CMOS (complementary MOS) technology. It was CMOS technology that proved to be a natural for predictable and successive rounds of size reductions–eventually allowing thousands, millions, and eventually billions of transistors to be placed on the same relatively-small-sized pieces of silicon. This has led to silicon slivers that feature the integration of large numbers of transistors and circuits–products which are thus commonly-known nowadays as integrated circuits (ICs).

38. For purposes of this Declaration, it is worth noting that an interesting and important aspect of integrated circuit fabrication and design is that each task is approached from a fundamentally different perspective. Fabrication is typically considered from a cross-sectional point of view, focusing on the vertical layering and material interactions throughout the depth of the semiconductor wafer. In contrast, design is approached from a plan-view (top-down) perspective, emphasizing the lateral layout and connectivity of devices across the wafer surface. The following image—which is the FAA "approach plate" describing the instrument approach procedure to be used when flying the "ILS-33" approach into

Burlington, Vermont–conceptually illustrates both the cross-sectional and plan-view perspectives, thereby highlighting the distinction between how fabrication and design are visualized in integrated circuit technology. (*See* illustrative image below.)

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BURLINGTON, VERMONT
AL-70 (FAA)
25107
ILS or LOC RWY 33
PATRICK LEAHY BURLINGTON INTL (BTV)
LOC/DME I-VOE 110.3 Chan 40
APP CRS 326°
Rwy Idg 7819
TDZE 334
Apt Elev 335
DME or RADAR required.
Circling Rwy 1 NA at night. Autopilot coupled approach NA. Rwy 33 helicopter visibility reduction below RVR 4000 NA. For inop ALS, increase S-ILS-33 all Cats visibility to RVR 4500. Inop table does not apply to S-LOC-33 Cats C, D and E.
-10°C
MALSF
MISSED APPROACH: Climb to 1200 then climbing left turn to 3000 direct BTV VOR/DME and hold, continue climb-in-hold to 3000. (TACAN aircraft climb to 6000 on heading 326° for RADAR vectors. RADAR required).
ATIS 123.8 269.9
BURLINGTON APP CON ★ 121.1 278.8
BURLINGTON TOWER ★ 118.3 (CTAF) 257.8
GND CON 126.3 348.6
CLNC DEL 119.15
UNICOM 122.95
LOCALIZER 110.3 I-VOE Chan 40
BURLINGTON 117.5 BTV Chan 122
KOTDE I-VOE 4
JIDSO I-VOE 7.2
EHIKO I-VOE 9.9 RADAR
NIDUQ I-VOE 15
HONIB I-VOE 12.8
IAF MONTPELIER 116.9 MPV Chan 116
(IF/IAF) JANUD I-VOE 20 RADAR
7000 to JANUD 133° (19.2)
7000 NoPT 319° (17.6)
R-6501 A & B
MSA BTV 25 NM
4900
5800
ELEV 335
D TDZE 334
TWR 441
MIRL Rwy 1-19
HIRL Rwy 15-33
FAF to MAP 10 NM
Knots 60 90 120 150 180
Min:Sec 10:00 6:40 5:00 4:00 3:20
1200
3000
BTV
One Minute Holding Pattern
I-VOE DME ANTENNA
I-VOE 2.3
I-VOE 0.2
KOTDE I-VOE 4
JIDSO I-VOE 7.2
EHIKO I-VOE 9.9 RADAR
HONIB I-VOE 12.8
NIDUQ I-VOE 15
JANUD I-VOE 20 RADAR
1800
2900
3800
4700
5400
146° 10000 7000
326° 326°
GS 3.20° TCH 55
0.2 2.3 1.7 NM 3.2 NM 2.7 NM 2.9 NM 2.2 NM 5 NM
CATEGORY A B C D E
S-ILS 33 608/40 274 (300-¾)
S-LOC 33 1240/55 906 (1000-1) 1240-2½ 906 (1000-2½)
C CIRCLING 1240-1¼ 905 (1000-1¼) 1240-2¾ 905 (1000-2¾) 1380-3 1045 (1100-3) 1400-3 1065 (1100-3)
BURLINGTON, VERMONT
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44°28'N-73°09'W
PATRICK LEAHY BURLINGTON INTL (BTV)
ILS or LOC RWY 33
NE-1, 10 JUL 2025 to 07 AUG 2025
NE-1, 10 JUL 2025 to 07 AUG 2025

The plan view description of the approach appears in the upper (map-like) part of the plate, while the cross-sectional description of the approach appears in the lower-right part of the plate.

B. Silicon Integrated Circuit Fabrication Technology

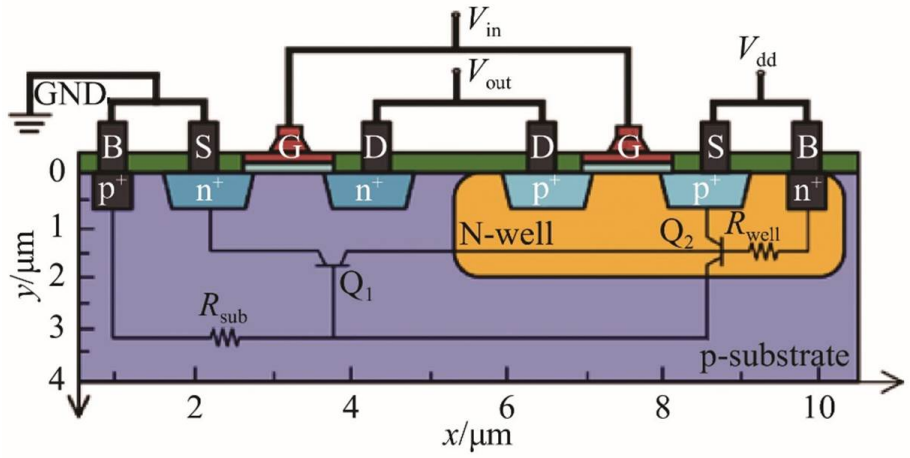
39. Silicon integrated circuit technology is a rather complicated topic–and not only are the fabrication details of that technology rather complicated, but they are actually a moving target as the fabrication technology evolved over time to meet a wide variety of challenges (as transistors became smaller, and integrated circuits came to contain larger and larger numbers of transistors).

40. However, the basic, fundamental processes themselves were already well established during the 1950s and 1960s–and while particular modifications have been introduced, the basic underlying methods that are used have remained roughly the same.

41. Thus, this background section will not attempt to walk through a detailed "typical" CMOS process flow–since, as just explained, such a "typical" process flow simply does not exist (for anything other than a brief period of time). Rather, the methods and goals will be addressed–particularly as the general methodologies can be used for a wide variety of structures, such as the trenched-gated transistors that are at the center of this matter.

1. Primary Goal

42. The primary goal of CMOS integrated circuit fabrication is to produce structures of this sort (*See* illustrative image below):



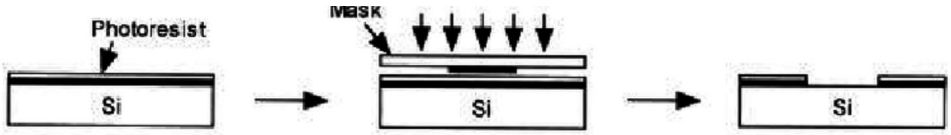
This is a simple two-transistor structure–which shows that the silicon is not addressed with physical intrusions, but rather with *chemical* intrusions that cause the electrical properties of the various colored layers to be altered by design. Further, the intermediate layer (above the silicon) shows that contacts are made to the terminals of these transistors, and (higher up) wiring is provided to electrically-connect the transistors together in particular ways (again, by design).

43. This is essentially the nature of silicon integrated circuit technology–and as the figure above and the discussion in the prior paragraph should make clear, the fabrication of a silicon integrated circuit involves the sequential execution of a set of steps in a fabrication sequence–from the silicon, upward to the contacts and wiring lines.

44. There are basically five categories of process methods that are germane to that fabrication sequence.

2. Lithography

45. Lithography is essentially a photographic method of defining structures in-and-on the silicon during the sequential steps that are used as the integrated circuit is built up (*See* illustrative image below).



46. Lithography defines those structures and the spatial separations between them. Further, lithography serves to allow some places to be exposed to particularly processing activities, while other places are shielded from that activity.

47. The limiting factor in reducing the size of features (in and on the silicon) is the lithography–where the limits are the smallest feature size that the lithography can produce, and the smallest distance between two features that the lithography can produce; generally, these two items (minimum size and minimum separation) are the same value. This minimum value defines a particular silicon integrated circuit manufacturing process–e.g., when reference is made to a "10nm process," that means that the lithographic process used is able to successfully-and-reliably produce features of that size and feature-separation of that distance.

3. Diffusion

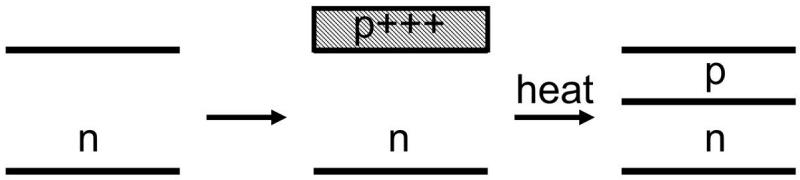
48. Diffusion is a process that is (and has long-been) well-known in nature–and which is readily described by what is known as "Fick's Law." Without going into that level of details, diffusion is simply a process that occurs when there is any sort of non-uniformity in the concentration (at particular points in space) of either matter or energy; constituents of that matter or energy will attempt to move around until they have rendered that once-non-uniform distribution uniform–or at least diffuse "against the concentration gradient."

49. Semiconductor processing has (from its origins) exploited this simple property of atoms moving against a concentration gradient to alter the electrical properties of silicon. This has mostly involved the use of a very-concentrated source of atoms as a diffusion source, and then (as per what Fick's Law indicates) using high temperatures to cause diffusion to occur in a timely manner.

50. Semiconductor materials are able to carry current as either negative charge or as positive charge–depending on the type of atoms that are added to that silicon. Some types of atoms cause the silicon to carry current as negative charge (making that material "n-type"), while other atoms cause the silicon to carry current as positive charge (making that material "p-type").

51. These impurity atoms (added to silicon) are known as "dopant atoms," and the process of introducing them into silicon is known as "doping." Atoms such as phosphorus and arsenic will dope silicon to be n-type, while atoms such as boron will dope silicon to be p-type.

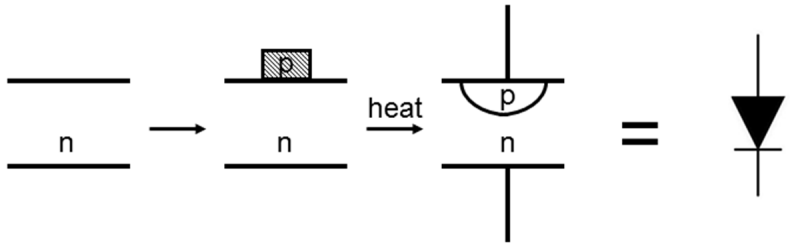
52. The doping-by-diffusion methodology is rather simple (*See* illustrative image below):



A high-concentration doping source is placed on the silicon, a heat cycle is carried out to diffuse (i.e., drive) the dopant atoms into the silicon, and then the doping source is removed–leaving behind a doped layer in the silicon.

53. One useful aspect of this type of process is that silicon, by doping, can be converted from one type to another–that is, p-type silicon can be doped more-heavily with n-type atoms and become n-type; the p-type atoms are still there, but they are greatly outnumbered by the invading n-type atoms and become irrelevant; generally, an invading doping concentration that is at least ten times that of the incumbent-atom concentration is sufficient for the doping type of the silicon to be regarded as "changed to the opposite."

54. By creating a single horizontal layer, or by introducing dopants only in a pocket, a simple electronic device can be created (*See* illustrative image below):

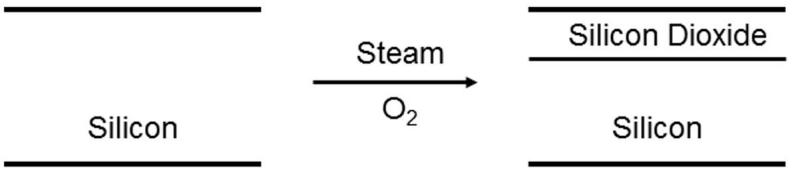


This figure shows a typical process for creating a simple p-n junction diode– a very basic silicon-based electronic device. What is particularly notable about this structure is that *the underlying silicon lattice remains unaffected*; the electrical properties have been created solely by chemical methods and the introduction of a chemical difference (over location) within the silicon.

55. One final aspect of diffusion is that it is a very good process for use in manufacturing such electronic devices in large numbers–as the process is very easy to tightly control (in suitable furnace equipment), and thus is very robust, reliable, and repeatable; this allows large numbers of electronic devices (such as the aforementioned diode) to be produced that are essentially identical to each other–a delightful rarity in any manufacturing environment.

4. Oxidation

56. Another aspect of silicon is that it is a material that is easy to oxidize– that is, by exposing a silicon surface to oxygen (and perhaps steam) in a furnace of the type mentioned above, an "oxide" (i.e., a layer of silicon dioxide (SiO_2)) will natively grown on the silicon; while this process is akin to the rusting of iron (which is the production of iron oxide on iron by exposure to air and moisture), the silicon dioxide that is produced by the oxidation of silicon leads to the growth of what "silicon dioxide" actually is–a type of glass. (*See* illustrative image below.)



57. Interestingly, the dominance of silicon as the material of choice for semiconductor devices is due primarily to its unique ability to form a high-quality native oxide—silicon dioxide (SiO_2)—through direct thermal oxidation. While germanium was historically used in early semiconductor devices and offers inherently higher carrier mobility (and thus faster operation) than silicon, it lacks the ability to form a stable, insulating oxide layer comparable to SiO_2. As a result, germanium has been largely relegated to niche or special-case applications,

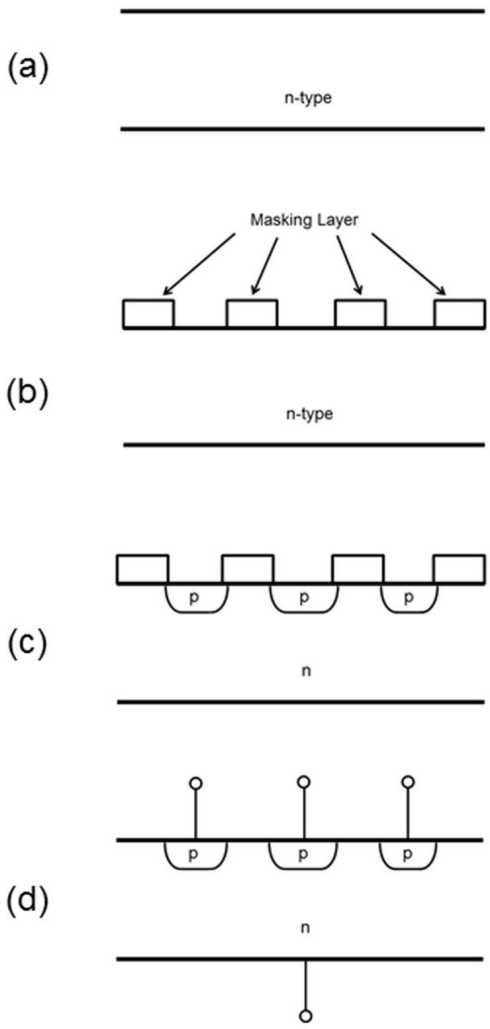
whereas silicon has become the foundational material for mainstream integrated circuit technology

58. Further, as silicon dioxide growth on silicon (as mentioned above) uses the same furnace equipment as was used for diffusion, the processes for doing this were also robust, reliable, and repeatable–so that high-quality silicon dioxide layers of identical thickness could be grown both across a single wafer and across multiple wafers. This accidental property of silicon that was simply supplied by nature is one of the most profound occurrences in history.

59. Grown silicon dioxide has been used for many purposes–with that usage expanding over time as engineering abilities with silicon dioxide became better with experience.

60. At first, silicon dioxide provided a masking layer for activities such as the aforementioned diffusion-based creation of p-n diodes. (*See* illustrative image below.)

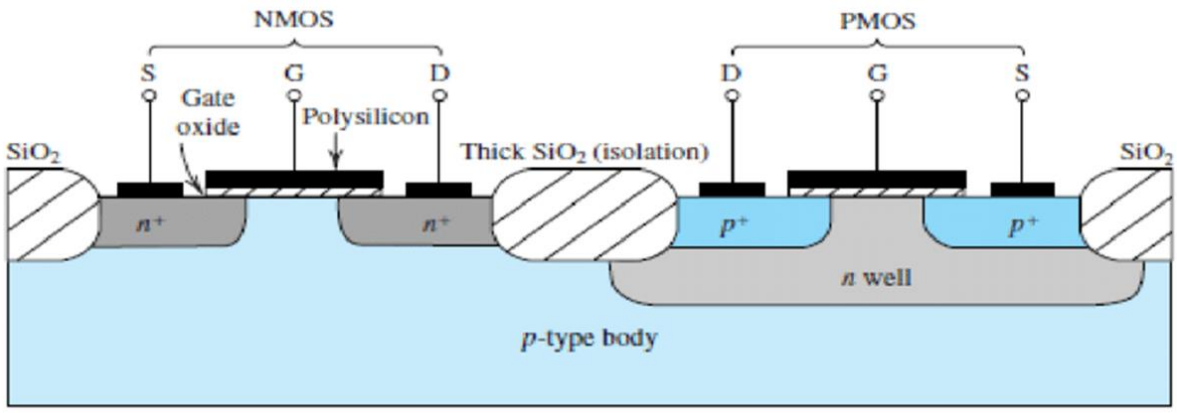
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As the sequence in this figure shows, first silicon dioxide is grown, and then photolithographic processes are used to create "windows" through the silicon dioxide. Then, the aforementioned diffusion process is used to restrict the diffusion to the "window" locations–which results in the formation of multiple p-n diodes in the same piece of silicon. After this is done, the silicon dioxide is removed from the surface–leaving behind the individual p-n diodes.

61. Eventually, grown silicon dioxide turned out to be so robust and so repeatable in formation that it came to be used for the gate dielectric in the MOSFET structure. It was this breakthrough that allowed what we now call "Moore's Law" to happen–and for the simple structures of the 1950s to evolve into the billion-plus transistor ICs of today.

62. Thicker grown silicon dioxide layers also came to be used for lateral isolation between adjacent MOSFETs–since as dimensions decreased, adjacent transistors began to operationally-interfere with each other. (*See* illustrative image below.)



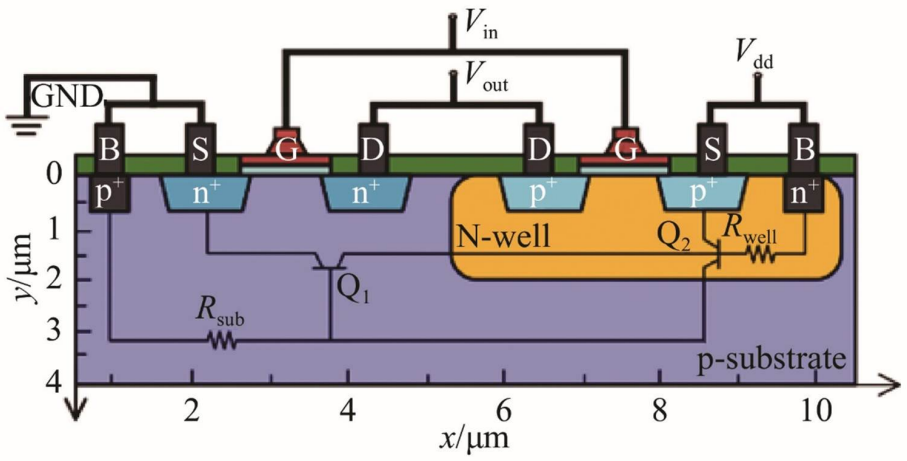
Note that the figure above depicts both the very thin gate dielectric "gate oxide" inside the transistor structure, *and* the thick "isolation oxide" that is used to electrically-separate adjacent transistors.

5. Deposition

63. Deposition is another technique used in silicon processing–which basically means what it says; a material is deposited onto a target surface by one method or another.

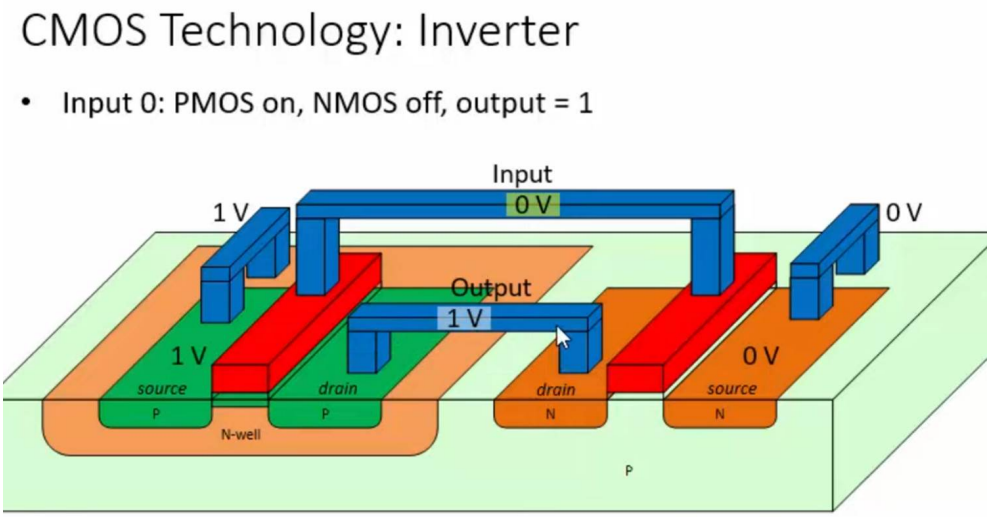
64. Initially, deposition was not used to a great extent in semiconductor fabrication–and was chiefly used in the deposition of the metal layers that were used to provide contacts to transistor terminals as well as on-chip wiring between-and-among various components.

65. This was depicted in the upper parts of a figure that was presented earlier. (*See* illustrative image below.)



As explained earlier, metal contacts are made to the device terminals in the silicon (at the n+ and p+ pockets), and wiring connects these terminals together in various ways that are used to implement circuit functionality.

66. The contacts and wiring can more-readily be seen in a more-detailed three-dimensional depiction. (*See* illustrative image below.)



As can be seen, the contacts are topped with metal studs that rise up above the contacts–for the purpose of connecting with the wiring lines that are shown (and which are organized, as mentioned above, to implement circuit functionality).

67. In the early days of silicon integrated circuits, contacts, plugs (if used), and wiring lines were all made using aluminum–as aluminum has good electrical conductivity, is easy to work with, and is ubiquitous. Aluminum was deposited using a simple technique–such as vacuum evaporation or sputtering.

6. Evolution

68. As mentioned earlier, these five techniques formed the set of methods that were used in silicon processing–and are still the basis of silicon processing today. However, shrinking device dimensions has forced amendments to silicon

processing–largely because smaller spaces and topographic challenges have, over time, made those basic techniques more and more problematic.

69. One major problem is that these early techniques were isotropic in nature–that is, they acted in all directions (such as both vertically and laterally) at the same rate. This did not matter when structures (and the distances between them) were rather large; however, when these dimensions became smaller, the lateral extent of isotropic methods was no longer tolerable; anisotropic methods had to be found and introduced.

7. Lithography

70. As described earlier, lithography is the base process for the ability to create separate structures in a silicon integrated circuit. Lithography is actually not an isotropic process, but essentially a photographic process. While lithography has changed drastically from its early days–largely by the use of light sources with smaller and smaller wavelengths–the basic notions of lithography have remained the same as structural dimensions have continually decreased.

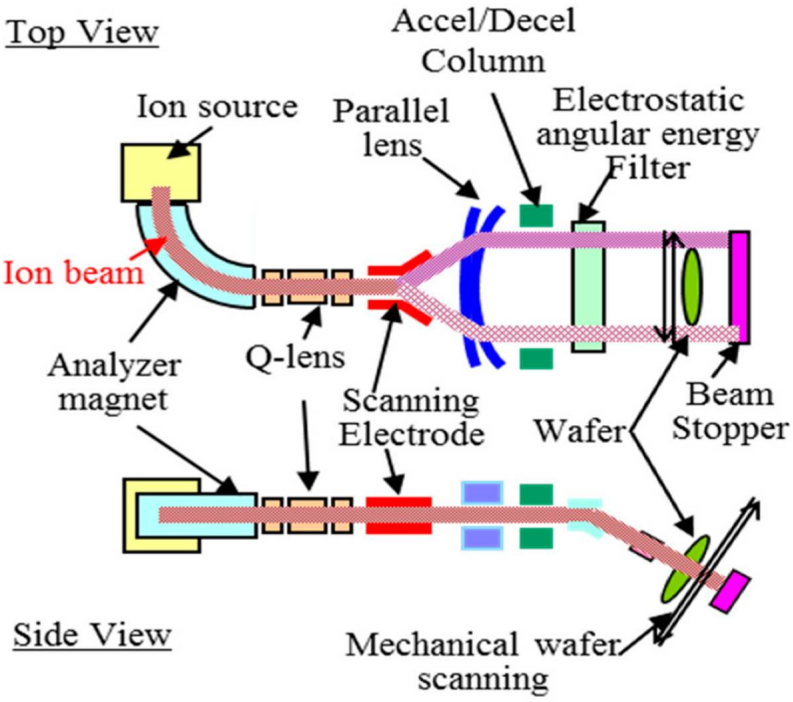
8. Doping

71. As noted earlier, simple diffusion was long used in silicon processing to introduce layers and pockets of dopant atoms, for the purpose of chemically-altering the electrical properties of the host silicon. However, as also noted earlier,

diffusion is an isotropic process–with diffusion pushing dopants uniformly in all directions.

72. As dimensions decreased and features became smaller and more-closely packed together, this isotropic behavior became problematic–and a directional method (i.e., an isotropic method) was increasingly required.

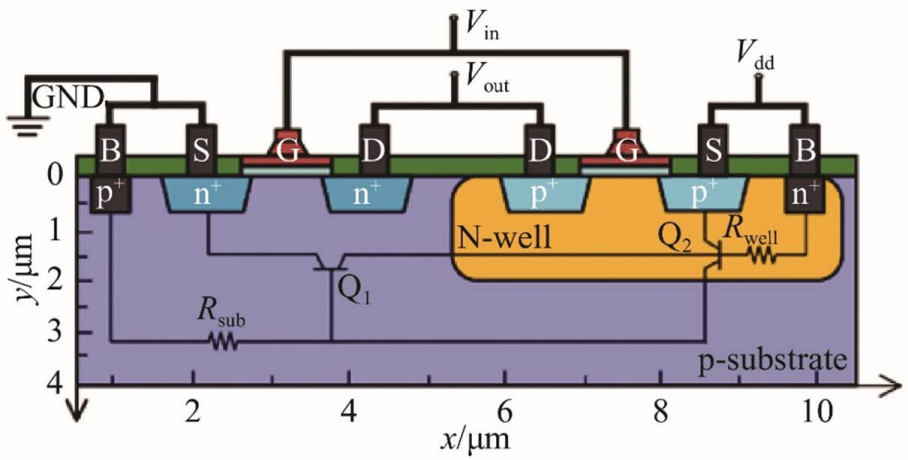
73. Ion implantation had long been proposed for anisotropic doping–and it did gradually supplant simple diffusion. Ion implantation is carried out basically as the name suggests; using electric and magnetic fields (in a manner that is similar to that used in particle accelerators), atoms are ionized and then accelerated to high speeds and "fired" into silicon. (*See* illustrative image below.)



This method provides two improvements over simple diffusion.

74. First, as per the discussion above, the use of a beam allows the doping layer or pocket produced to be formed using a method that is directional (i.e., anisotropic)–that is, dopant atoms can be driven deep into the silicon, but they do not spread out laterally to a great degree. Second, simple diffusion from a high-concentration dopant source that is placed on the surface will always result in a doping concentration that is highest at the surface (with the concentration decreasing the further one moves below the surface)–while ion implantation allows the highest doping concentration to be placed below (often well-below) the surface; this provides design flexibility during process development–as it allows for the creation of a specially designed "doping profile" with depth in the silicon.

75. On that count, reconsider the early-shown depiction of a simple silicon CMOS structure with two transistors (one nMOS and one pMOS). (*See* illustrative image below.)



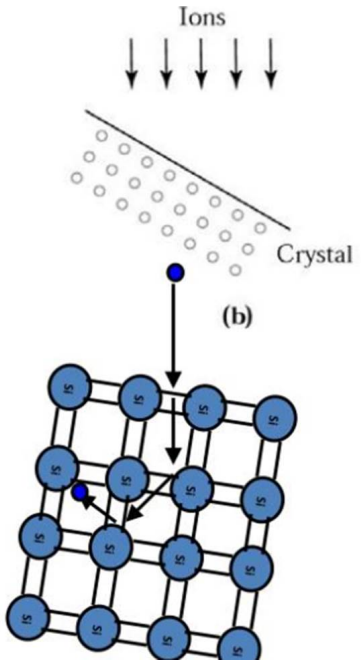
Consider the pMOS transistor on the right-hand side, and how the doping layers there can be created using ion implantation. Beginning with the p-substrate, the n-well is created using a deep implantation of n-type dopant atoms, in (as described earlier) a sufficient quantity to turn the p-type silicon into n-type silicon (by providing an n-dopant concentration that is ten-times-or-more greater than the background p-type doping concentration of the substrate). Then, the n+ and p+ pockets are created by shallow implantations of very high concentrations of dopant atoms as appropriate. Thus, solely by introducing dopant into different locations in the silicon, the electrical properties of those regions can be tailored chemically to the desired form.

76. A further aspect of ion implantation is that it need not be done "straight on"–that is, the implantation does not have to be done perpendicular to the wafer surface; rather, the wafer can be tilted in the implantation machine–so that the dopant beam impinges upon the wafer at an angle.

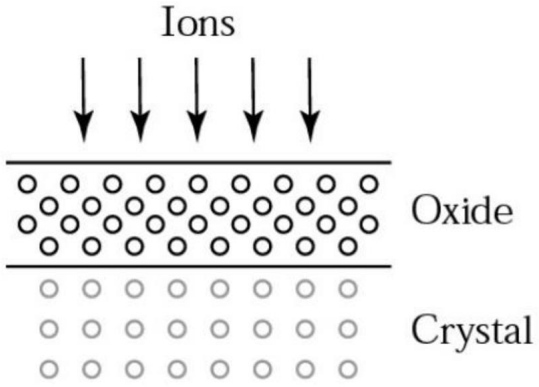
77. There are two common reasons for using an angled ion implantation.

78. The first is a simple one; when a perpendicular ion beam is impinged upon a silicon substrate, it lines up directly with open "lanes" in the silicon crystal lattice structure–which provides a pathway for some of the atoms to travel into these lanes and penetrate very deeply into the silicon, which harms the overall doping profile of the doping layer produced. The simple solution was to tilt the

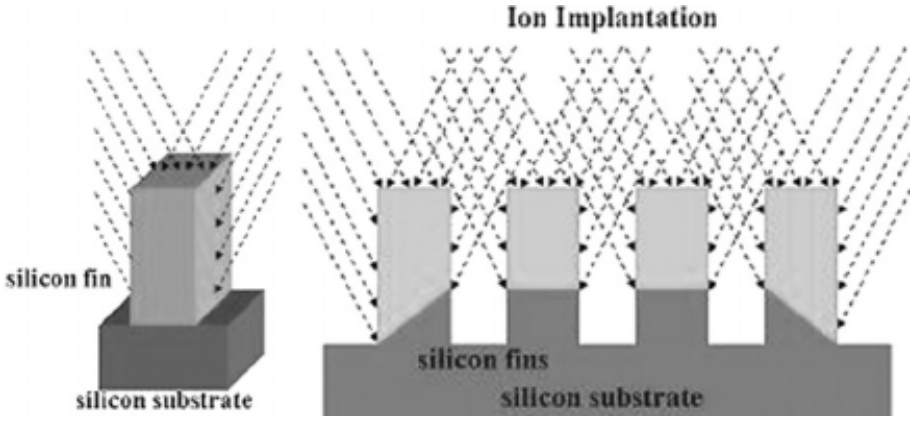
wafer at an angle of 7° for the purpose of preventing ion impingement into those lanes. (*See* illustrative image below.)



This has been a commonly-used method–although the same outcome can be achieved by creating a sacrificial silicon dioxide layer on the surface and using perpendicular implantation. (*See* illustrative image below.)

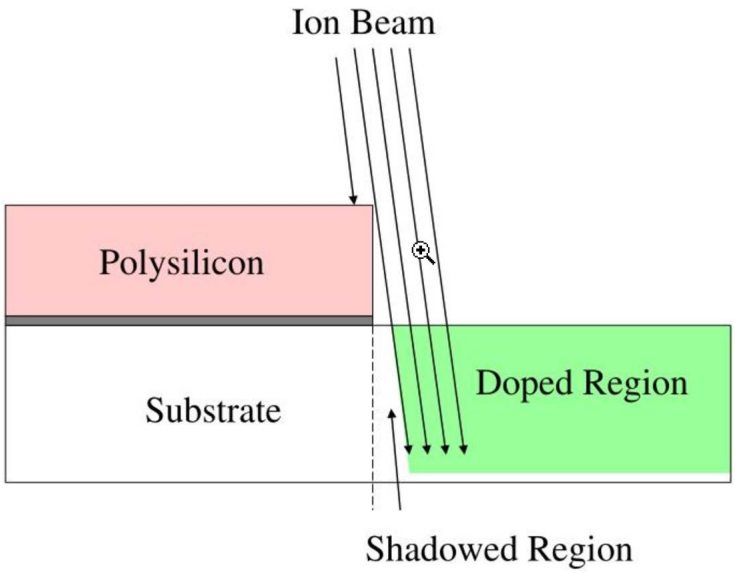


79. Angled implantation also came to be used at much larger angles–for the express purpose of implanting dopant atoms into non-planar structures of various sorts. (*See* illustrative image below.)



As will be described below (in Section VII. C), angled implantation became particularly useful when trenches were introduced into silicon fabrication technology–while also presenting some unique challenges, such as the "shadowing" that occurs when angled ion implantation is used with such topographical features. (*See* illustrative image below.)

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Shadowing can be a bug–or a feature.

80. As noted earlier, simple diffusion–carried out using specialized furnaces–is a doping process that is robust, reliable, and repeatable; among other things, this allowed for large numbers of diffused layers/pockets to be created across many wafers that were essentially identical–so that statistical variable could be ignored and the different instances treated as identical. In contrast, ion implantation has significant run-to-run statistical variability–to the degree that this variability must be taken into consideration with regard to the electrical behavior of the transistors thusly produced. The need for an anisotropic doping method eventually came to outweigh this statistical-variability shortcoming of ion implantation.

9. Oxidation

81. As also noted earlier, oxidation of silicon to produce silicon dioxide was a marvelous physical coincidence that was put to good use for a variety of uses and structures in silicon integrated circuits. In particular, grown silicon dioxide layers could be made that were very thin–while still being robust, reliable, and repeatable; this allowed very thin grown silicon dioxide to be used for the gate dielectric layer of the MOS transistor–which is an inherent feature of silicon that allowed the MOS transistor to become the most-constructed object in human history.

82. However, the reduction of dimensions and the introduction of more complex topographies led to a number of additions and changes to the widespread use of grown silicon dioxide–largely via the introduction of deposited dielectric materials (both simple oxides and more complex dielectrics).

10. Deposition

83. As described earlier, deposition originally was used basically-exclusively for the deposition of the aluminum metal layers that provided contacts and wiring for MOS transistors. However, as just noted above, deposition over time expanded into a variety of uses in silicon integrated circuit fabrication.

84. One use, mentioned above, was the introduction of topographic features into silicon processing–such as trenches (to be discussed in more detail below, in Section VII.C):

Ex. 1007, B. Davari et al., *A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS*, International Electron Devices Meeting, 93 Fig. 1 (1988)

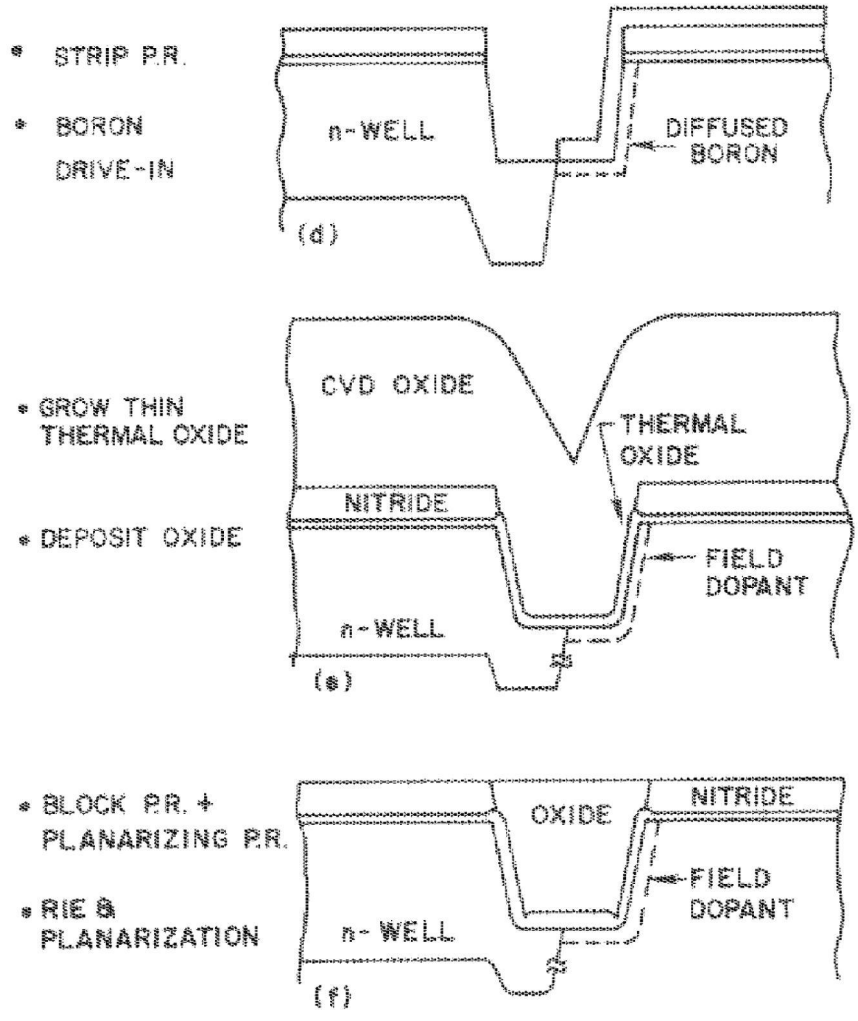


FIG.1 Shallow Trench Isolation process flow

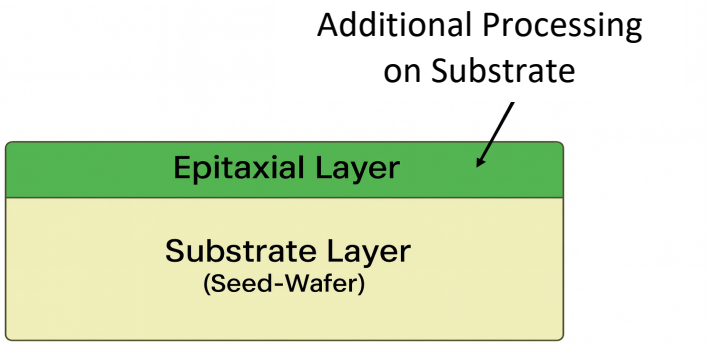
As can be seen, while a silicon dioxide layer can be grown uniformly on the surface of the trench (i.e., the bottom and sidewalls of the trench), the trench can only be filled via the use of a deposited oxide. Note further that the source of this figure is the original paper on the use of shallow-trench isolation for inter-transistor isolation–as a replacement for the thick grown oxide layer that had previously been used for that purpose.

85. Deposited oxides also came to be used for other purposes–such as to provide isolation between metal layers-and-lines (as will be discussed below). In more recent years, deposited oxides have even come to be required for the MOS transistor gate dielectric–as feature-size-reduction has led to gate oxide thinness requirements that are too thin for the grown silicon dioxide layer to meet. As a result, in contemporary MOS transistors, the gate dielectric is no longer even a silicon dioxide layer–but rather that layer is generally provided by a deposited layer of hafnium oxide (i.e., Hf2O5).

86. Deposition came to further be very widely used in silicon fabrication of integrated circuits–due to smaller feature sizes, more transistors per IC, and more complexity–in order to cope with the layered nature of integrated circuits. One prominent example was the replacement (during the 1980s) of the aluminum metal gate electrode of the MOS transistor with a polysilicon gate electrode (which will be discussed in more detail below)–as like aluminum, polysilicon must be

deposited onto the silicon structures during fabrication. In addition (as will also be explained further below), the stacking-up of metal wiring layers also required extensive use of deposition–for both the conducting metal materials and for the dielectric insulating layers that were placed between them.

87. An extension of deposition that was also introduced into silicon processing was carried out on the basic starting wafer before any MOS-transistor-related structures (either chemical or physical) were created. This is the growth of an epitaxial layer of silicon on top of the starting silicon substrate wafer. (*See* illustrative image below.)



An epitaxial layer is a layer of crystalline silicon that has a lower defect concentration than does the substrate wafer–and, when an epitaxial layer is included onto the starting wafer, all of the MOS transistor structures of the planar MOSFET devices depicted above (again, both physical and chemical) are formed in this epitaxial layer.

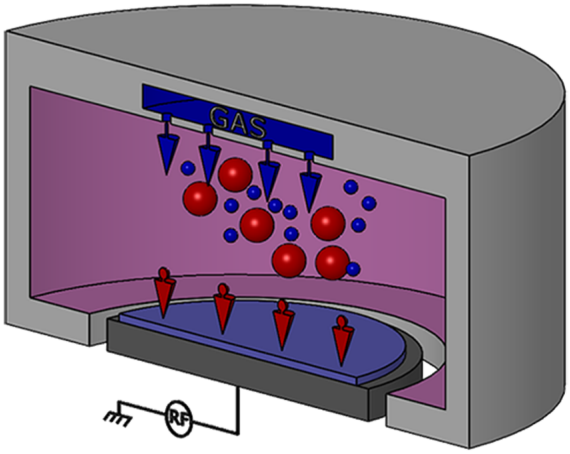
88. In addition to being more-orderly, the epitaxial layer also (due to that better order and fewer defects) has a lower resistivity than does the substrate-wafer silicon; this is actually the main reason that epitaxial layers were introduced, as this lower resistivity helps to suppress a destructive failure mechanism known as "latch-up." (*See* Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 385-387 (1990).)

11. Etching

89. As also described earlier, in the early days of silicon processing, "etching" referred to the use of liquid chemical mixtures for "wet etching" of silicon, silicon dioxide, and other materials. However, like diffusion-based doping, wet etching is an isotropic process–and as was also the case with doping, smaller feature sizes led to a need for anisotropic etching methods.

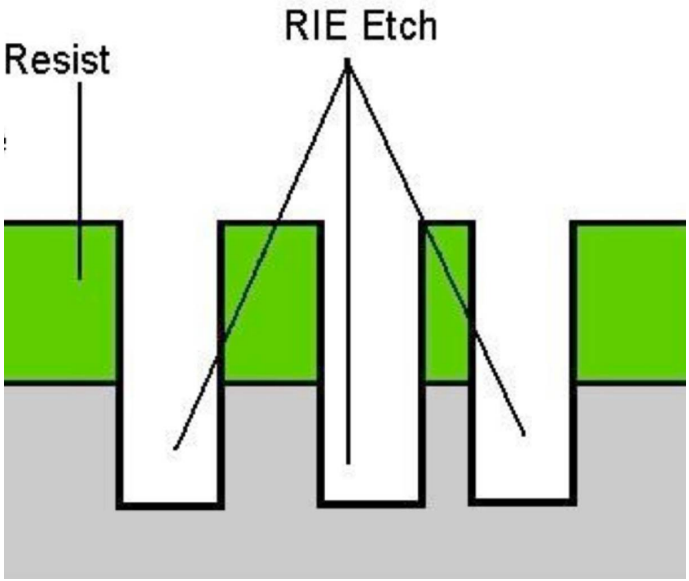
90. A good example of these needs can be seen via examination of the introduction of polysilicon to replace aluminum as the gate electrode material in MOS transistors. Polysilicon can be deposited and etched–but this etching must be directional so as to leave behind well-defined polysilicon lines that provide the transistor gate electrodes.

91. To carry out this type etching, a directional method known as "reactive ion etching" was developed. (*See* illustrative image below.)

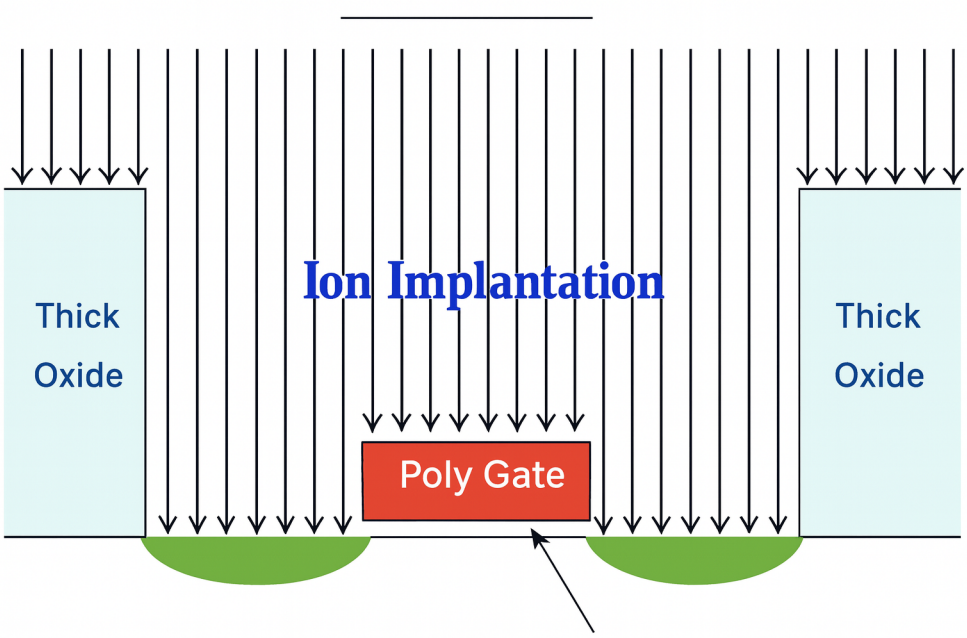


Ionized atoms (i.e., a plasma) are accelerated (by an electric field) toward the silicon–where they interact with the surface (but not any sidewall) to gassify the target layer (such as polysilicon), with the product gas then pulled out of the chamber.

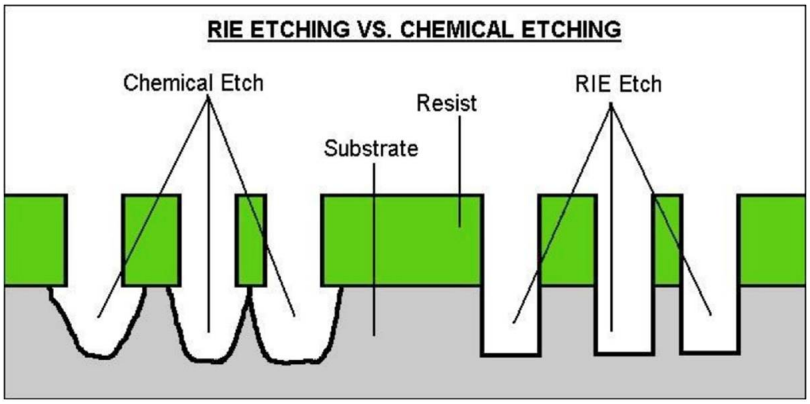
92. In this way, a layer (such as the aforementioned polysilicon layer) can be etched so as to have quite-vertical sidewalls along the mask-protected part of the polysilicon. (*See* illustrative image below.)



The ability to etch the polysilicon shape into this form allowed for the use of that polysilicon as an in-situ mask for the implantation of the source and drain regions of a MOS transistor–allowing the source and drain to be "self-aligned" in the resulting MOS transistor structure. (*See* illustrative image below.)



93. Reactive-ion etching quickly became the mainstay etching method of silicon processing–due to its anisotropic (i.e., directional) capabilities, and the growing need for anisotropic etching as silicon structures became more complex (along with the ability to make such more-complex silicon structures due to the availability of this now-ubiquitous anisotropic etching method). Why this happened can be seen in the following comparison. (*See* illustrative image below.)



Anisotropic reactive-ion etching allows for the creation of structures that simply cannot be made using wet etching–particularly at smaller and smaller dimensions.

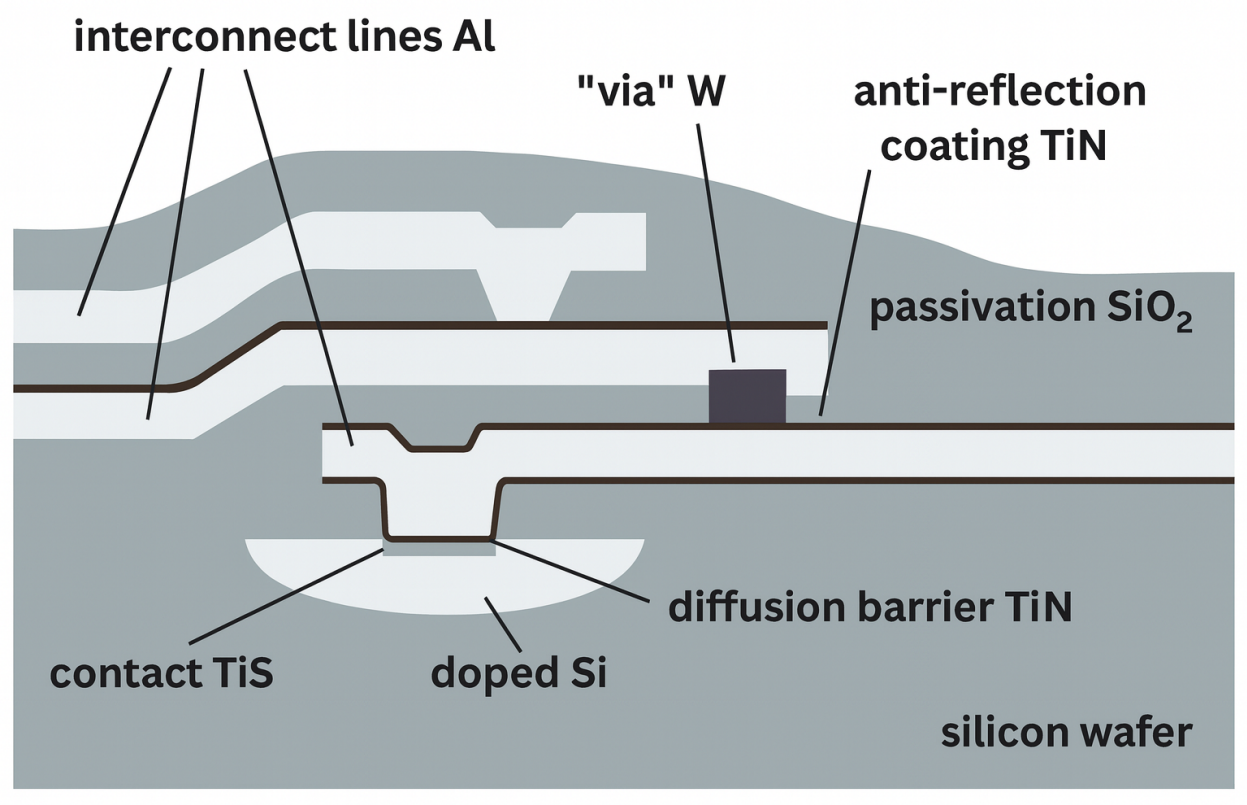
94. However, as was the case with ion implantation, reactive ion etching is more variable in practice than is wet etching–but once again in a similar way, the need for directional etching greatly outweighed the excellent repeatability of wet etching.

12. Metallization

95. As already described, silicon integrated circuits required metal layers to serve as wires–in order to connect the transistor terminals among numerous transistors (and other components) for the purpose of providing desired circuit functionalities; as also described earlier, this was originally done by depositing aluminum using a simple technique–such as vacuum evaporation or sputtering.

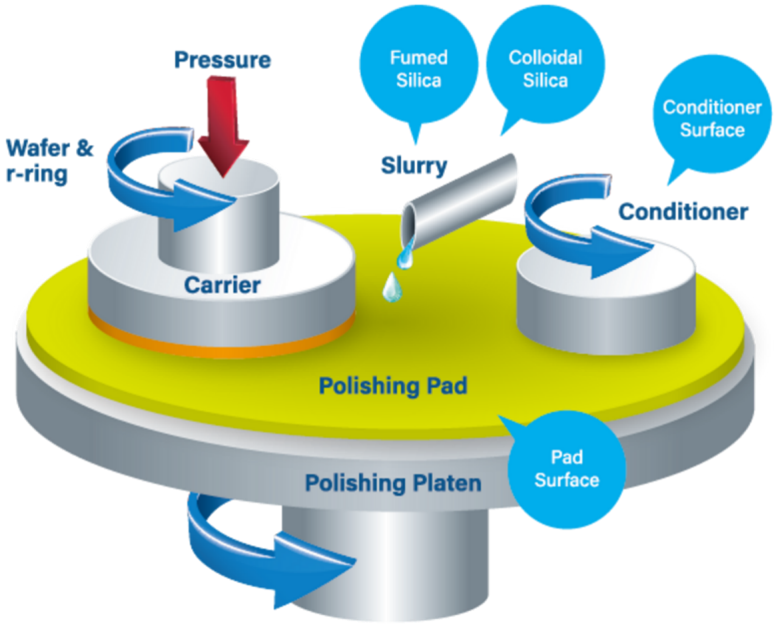
96. However, decreasing feature sizes, decreasing inter-feature space distance, more-complex integrated circuits, and more (vertically-stacked) metal layers required that this simple aluminum metallurgy be replaced with more-complicated (but more functional) approaches.

97. The first generational change came with the introduction of tungsten "via plugs" and aluminum wiring layers–where the aluminum wiring provided the aforementioned transistor interconnections (for circuit functionality), while the tungsten plugs provide the vertical connections between-and-among the various stacked aluminum wiring layers. (*See* illustrative image below.)



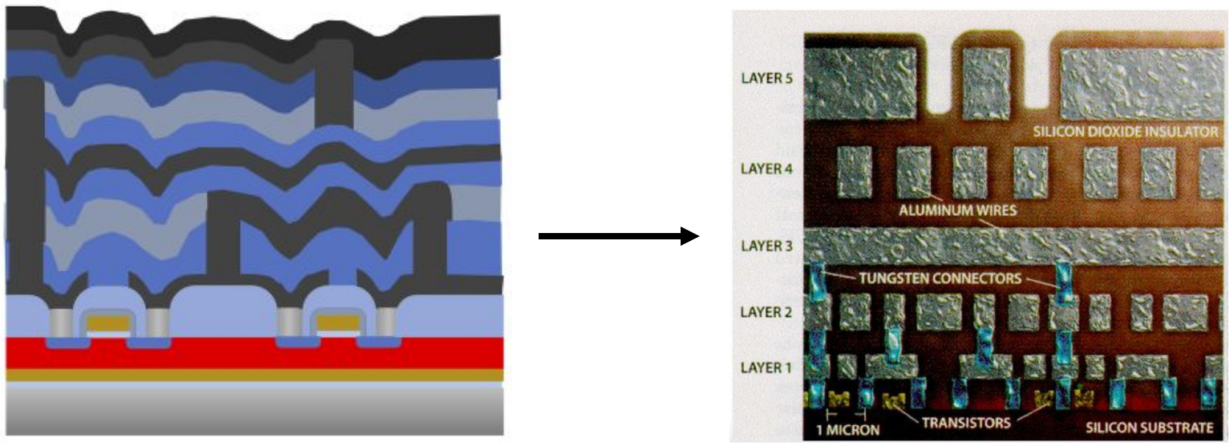
What was described above can be seen here–aluminum is used for the wiring layers, and tungsten plugs provide the vertical "via" interconnections between-and-among those aluminum wiring layers.

98. As can also be seen in this figure, this relatively-simple structure has three metal layers–with a non-flat overall topography. Eventually, the need for more metal layers made non-flat topography untenable–and chemical-mechanical polishing (CMP) was introduced to provide flat topography in the interconnect layers. (*See* illustrative image below.)

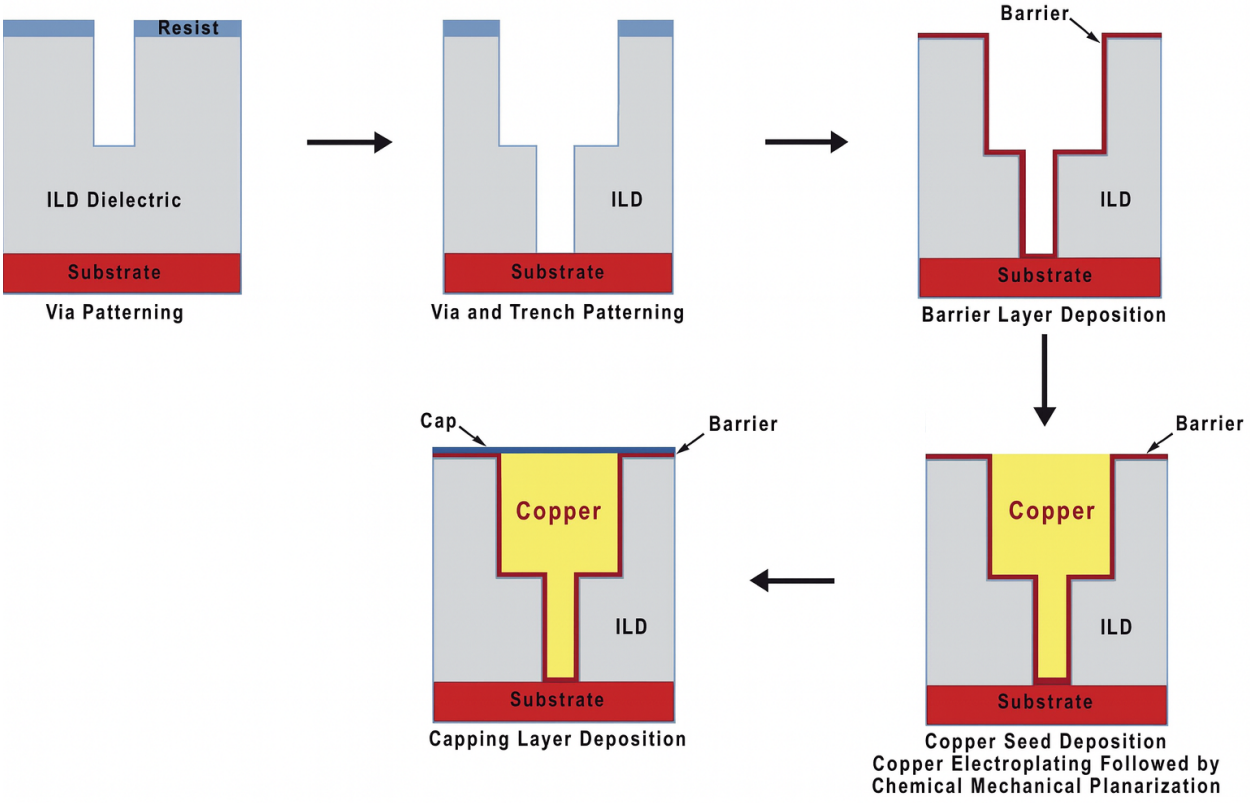


99. CMP allowed for a vast expansion in the number of metal layers that could be included in a silicon integrated circuit–since the flat topography eliminated the problem of non-flat topography making it too difficult to build up

such a sequence of layers. This allowed for a dramatic transformation in the topography of interconnect layers–even though in both cases, tungsten plugs and aluminum wiring lines were used. (*See* illustrative image below.)

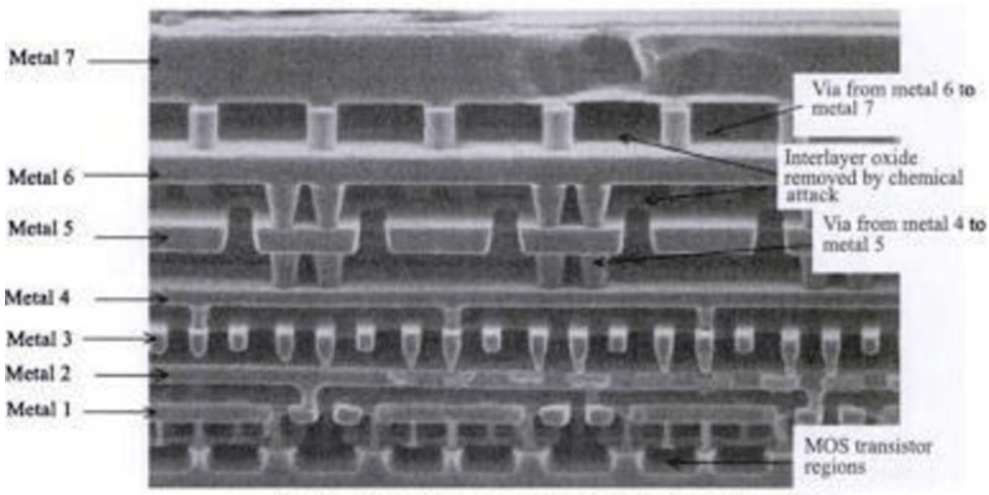


100. In more recent years, this tungsten-plug/aluminum-wire approach has been replaced with the use of an all-copper metallurgy–as the resistance of (narrower and narrower over time) aluminum lines was becoming problematic, and copper has a lower electrical resistivity. In contrast to the separate use of tungsten plugs for filling vias and aluminum for the wiring, copper is used for both of these functions–with copper being grown by a seeding process that allows the via and the overhead metal line to both be produced in the same processing step. (*See* illustrative image below.)



101. The use of a barrier layer to completely enclose the copper metallurgy is extremely important in this system–since unlike aluminum (which is self-passivating), copper is liable to outdiffuse copper atoms that can wander to unwanted to unwanted places in the integrated circuit, or to grow dendrites that can grow through adjacent isolating dielectric layers and produce unwanted electrical shorting to other copper lines.

102. The introduction of this "dual-damascene" copper metallization process has allowed for the deployment of a stupefying number of metal layers in contemporary integrated circuits. (*See* illustrative image below.)



Cross-section of a 0.12 µm technology (*Courtesy:* Fujitsu)

This 0.12 µm (i.e., 120 nm) manufacturing process has seven metal layers–with the structure being orderly and with extremely smooth topography from layer to layer. Because of this orderly topography, it became typical for each new process generation to introduce an additional metal layer–with contemporary processes now containing 15-or-more such stacked metal layers.

103. This basic semiconductor fabrication technology can, of course, be applied to structures other than the basic "surface channel" MOS transistor.

13. Units and the Presentation of Units

104. In this Declaration, there is considerable discussion of both doping concentrations in silicon and the use of ion implantation to introduce dopant atoms into silicon for the purpose of doping. While these concepts are understandable from a qualitative point of view, the detailed aspects of their usage in the art – as

reflected in both the prior art references to be cited in this Declaration, and in the '634 patent itself – require that a quantitative point of view also be considered.

105. As discussed above, ion implantation involves the creation of a "beam" of ions – wherein those ions are accelerated (by an electric field) and then directed to impinge upon a silicon surface (or surfaces). To a reasonable approximation, this ion beam can be considered to be uniform across its cross-section – so that the total number of ions in the beam can be specified as the areal density of those ions in the beam (known as the "dose" applied during ion implantation); the actual quantity of this dose is chosen based on the degree of doping that is intended to be produced in the silicon – with a higher dose being chosen for a higher doping concentration (and, conversely, a lower dose being chosen for a lower doping concentration).

106. This "dose," based on the aforementioned areal density of the ion beam, is specified as the number of ions per unit area in the beam – with the units being the number of ions in the beam per square centimeter across the cross-sectional area of the beam. This is typically specified numerically in forms such as "$5.0\times10^{15}/cm^2$" or "$5.0\times10^{15}\ cm^{-2}$" – which are two different ways of specifying a dose (5.0×10^{15} ions) per square centimeter in the cross-section of the ion beam (and which will be directed to impinge upon a target).

107. In a similar fashion, dopant concentrations in silicon are described in a volumetric fashion – that is, in terms of dopant atoms per unit volume of silicon. This is done in terms of the number of dopant atoms per cubic centimeter in the silicon – in forms such as "$2.0\times10^{17}/cm^3$" or "$2.0\times10^{17}\ cm^{-3}$" – which are two different ways of specifying that the dopant concentration in the silicon is 2.0×10^{17} dopant atoms per cubic centimeter in the silicon.

108. However, as some of the references cited in this declaration indicate, the doping of semiconductor materials (such as silicon) predates the availability of word-processing software that allows for clean subscripts and superscripts to be created (as was done above). Thus, it became common to specify implantation doses and doping concentrations in a manner that did not use subscripts or superscripts – or mathematical symbols (such as the "×" used above). Rather, a dose would be specified in a form such as "5E15 cm-2" (rather than the "$5.0\times10^{15}\ cm^{-2}$" used above), while a doping concentration would be specified in a form such as "2E17 cm-3" (rather than the "$2.0\times10^{17}/cm^3$" used above).

109. It is thus typical for this latter form of presentation to be found in the patent art – and the '634 patent is a good example of this usage (*see, e.g.,* the '634 patent at 3:52 and 3:58). However, for clarity, it should be noted that these two different formats are conveying the same actual information.

110. In this Declaration, both formats are used – as the "newer" method of presentation (which uses superscripts) provides more clarity and is what is typically used in the technical literature, while the "simpler" method is used in the '634 patent. As just noted, both methods of presentation are conveying the same information – and it is that information that is material to both this Declaration and to the various references (including the '634 patent) which are cited.

C. Silicon Trench Technology

111. While MOS technology is inherently a "planar" (i.e., operating at the silicon surface) technology, it wasn't long after its introduction before the use of the third dimension began to creep into this technology. For example, "local oxidation of silicon" (LOCOS) was introduced–in order to provide thick oxide bumps for inter-transistor isolation; as a further example, as the growing number of transistors in a single integrated circuit required more wiring, metal wiring (i.e., interconnect) layers were stacked on top of each other in regions above the silicon surface.

112. Trenches began to appear in MOS technology during the 1980s–for two notable purposes.

113. One was the use of "shallow" trenches (where "shallow" implies that the depth of a trench is similar-to or less-than the width of the trench) to replace LOCOS and provide inter-transistor isolation.

Ex. 1007, B. Davari et al., *A Variable-Size Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS*, International Electron Devices Meeting, 93 Fig. 1 (1988)

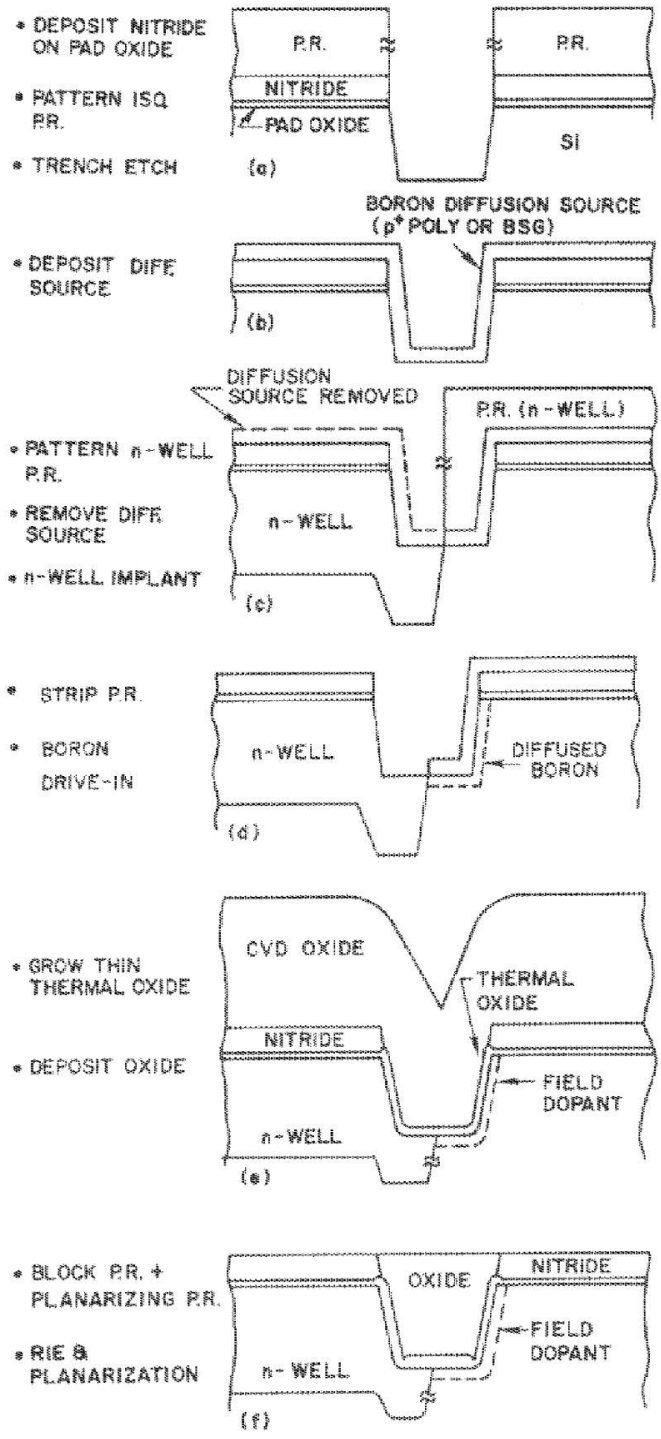


FIG.1 Shallow Trench Isolation process flow

114. The other use of trenches was the (more-spectacular) introduction of "deep" trenches (where "deep" implies that the trench is deeper than it is wide)– mainly for the storage capacitor node in DRAM cells, but also for a variety of other purposes:

Ex. 1009, S. Van Huylenbroeck et al., *A 0.25um SiGe BiCMOS Technology Including Integrated RF Passive Components Optimised for Low Power Applications*, European Solid State Device Research Conference (ESSDERC), 505 Fig. 1 (2003)

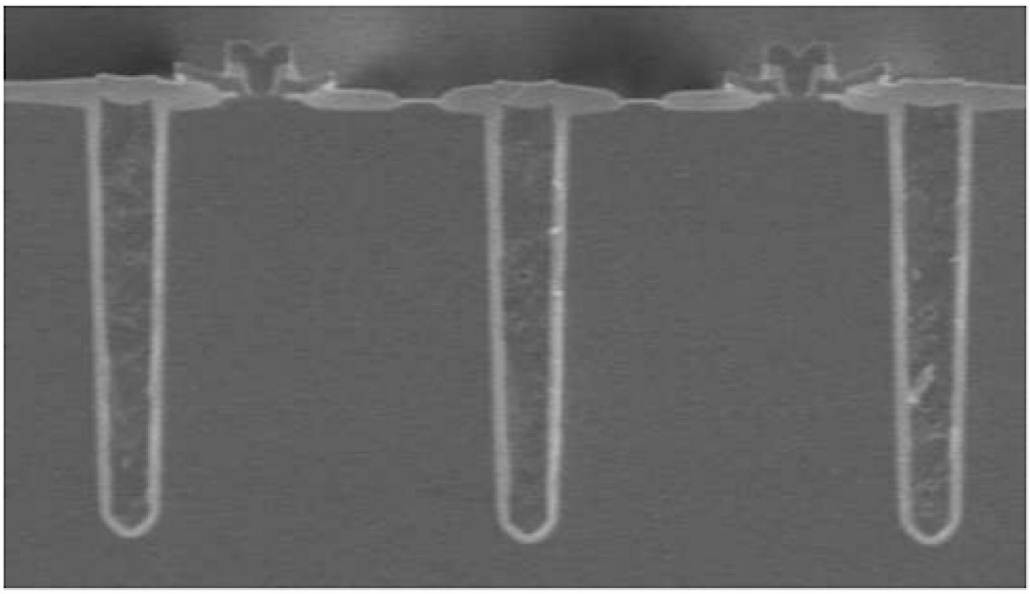


Figure 1. SEM cross section of the deep trench after complete BiCMOS processing.

115. When used in DRAMs, the use of a deep trench allowed for an increase in the amount of charge stored in a DRAM cell in the same amount of surface-silicon area–or some similar form of an improved overall combination of charge and areal density.

116. For the most part, deep trench DRAM cells used the trench as the storage capacitor node–while the access transistor was still a planar transistor up on the silicon surface.

Ex. 1010, U.S. Patent No. 5,395,786, Fig. 13

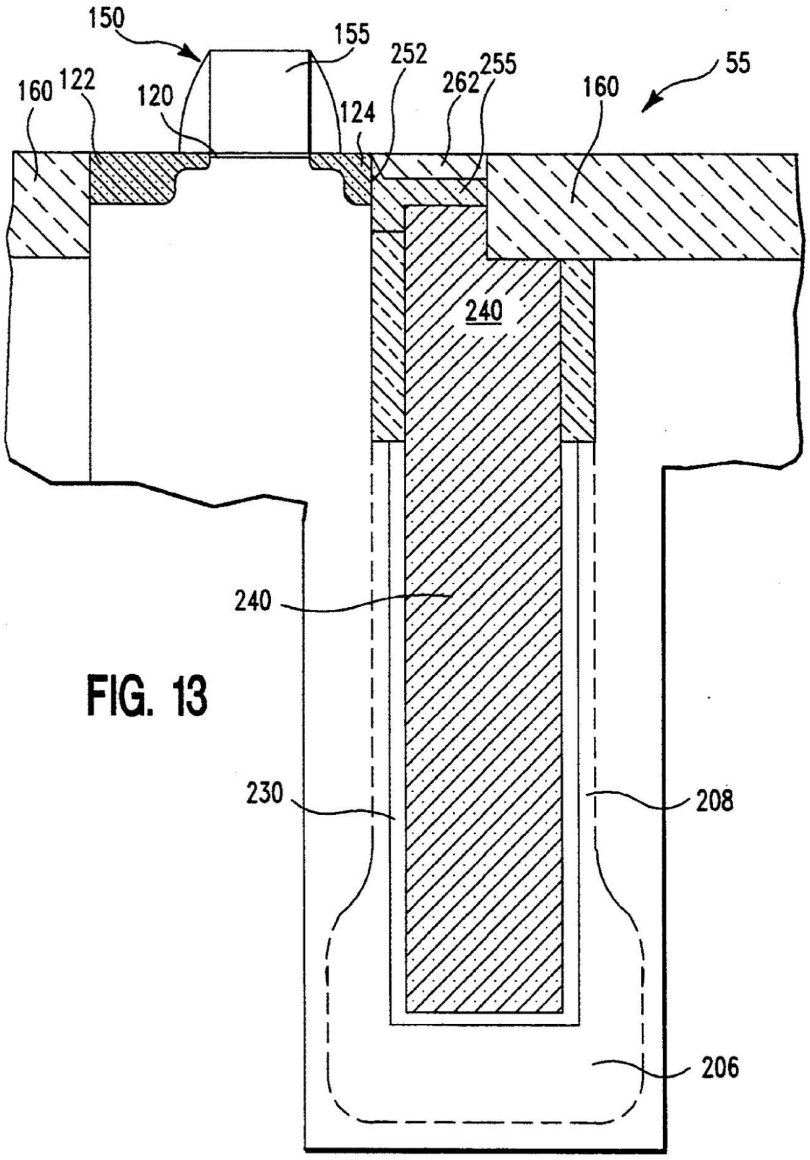


FIG. 13

117. However, in 1986, Texas Instruments introduced a trench DRAM cell in which the access transistor was not on the surface (as above)–but rather was also created in the trench, by putting that transistor in a vertical configuration on the sidewall of the storage node trench.

Ex. 1011, H. Shichijo et al., *Trench Transistor DRAM Cell, IEEE Electron Device Letters*, vol. 7, 119 Fig. 1 (1986).

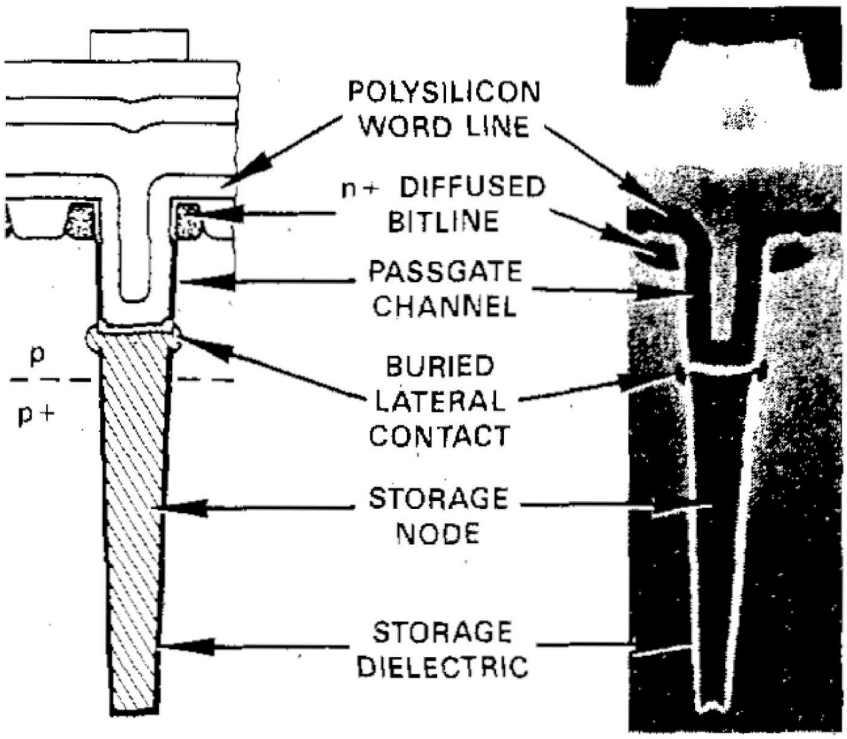


Fig. 1. TTC schematic diagram and SEM cross section.

118. As can be seen, the lower part of the trench serves as one plate of the storage node capacitor–while a vertical MOS transistor (which, as mentioned above, provides the access transistor) is placed on the sidewall of the upper part of the trench. This, of course, reduces the amount of silicon surface area needed for

the DRAM cell–since both the storage capacitor *and* the access transistor are contained in the deep trench.

D. Modern Trench MOSFET Technology

119. The many positive characteristics of the silicon MOS transistor allow that type of transistor to be used in a wide variety of applications–such as in power electronics for both switching and amplification. Among the various MOSFET known MOSFET structures, trench-gate MOSFETs are widely employed in applications which require high efficiency, low on-resistance (RDS(on)), and fast switching speeds.

120. Unlike conventional planar MOSFETs, which have a lateral current path across the surface of the silicon, trench MOSFETs (as briefly described above) utilize a vertical (rather than horizontal) channel structure. In a typical trench MOSFET, current flows vertically–from the source at the top of the device, through the channel region, and through the "drain region" (aka "drift region") to the drain terminal at the bottom. This structure allows for more-efficient use of silicon surface area while still providing a high current density.

121. The defining feature of a trench MOSFET is the trench gate—a gate electrode formed by etching deep trenches into the silicon surface and then lining them with a gate dielectric layer. The gate trenches extend downward to below the

bottom of the P-body region in order to provide proper electrical coupling between the gate and both the source and drain of the transistor.

122. The trench MOSFET structure allows for tighter cell spacing and greater channel density (i.e., the same amount of current flow occurs from a smaller amount of silicon surface area). Further, this configuration significantly reduces the on-resistance as compared to what is the case with planar devices.

123. Key elements of a trench MOSFET typically comprise:

- A heavily doped N^+ substrate (for the drain contact);
- An N-type epitaxial drift layer for voltage blocking;
- A P-type body region in which the conducting channel appears when the device is turned on;
- An N^+-type source region for low-resistance current entry;
- Gate trenches filled with polysilicon (or a similar material) and insulated by a gate dielectric;
- Body contact or source contact trenches to ensure a proper direct body-source contact while suppressing the activation of a parasitic bipolar transistor that is inherent in the trench MOSFET structure;
- A front metal layer formed on the upper surface, providing electrical contact to source regions and (with some exceptions)

gate regions, and also to provide connectivity between, e.g., device terminals;

- A bottom metal layer formed on the lower surface, providing electrical contact to the drain region;
- An interlayer oxide film to electrically isolate and protect the semiconductor regions from the front metal layer and gate structures.

124. To optimize performance, various structural enhancements are used, including:

- Shielded gates or split gate designs to reduce gate-drain capacitance (Cgd);
- P^+ body contact regions to suppress parasitic bipolar transistor turn on, and to provide a low-resistance ohmic contact to the silicon of the body region;
- Superjunction structures to increase the breakdown voltage without sacrificing RDS(on).

125. Fabrication typically involves well-known silicon processing techniques–such as deep trench etching, ion implantation, epitaxial growth, and multiple diffusion steps; all of these impact device characteristics such as threshold voltage, breakdown voltage, and switching behavior.

126. In sum, trench MOSFETs offer a superior trade-off between breakdown voltage and conduction losses, making them the preferred architecture for modern power devices in computing, automotive, and industrial electronics.

VIII. THE ’634 PATENT

A. Overview

127. U.S. Patent No. 7,629,634 (“the ’634 Patent”) is entitled “Trenched MOSFET with Trenched Source Contact.” The sole inventor is Fu-Yuan Hsieh, and the listed assignee is Force MOS Technology Co., Ltd. The application which led to the issuance of the ’634 Patent was filed on February 23, 2008, and the Patent issued on December 8, 2009; no earlier prior dates are claimed by the ’634 Patent–and I have been instructed by Counsel to use February 23, 2008 as the Filing Date for the ’634 Patent. It is my understanding that these dates show that the ’634 Patent was prosecuted and issued under “pre-AIA” United States patent law.

128. All of the claims of the ’634 Patent are apparatus claims; that apparatus is a trenched-gated MOSFET with a vertical current-flow path along a trench sidewall, and a “trenched source contact” that reaches downward through the structure to provide electrical contact with the body of the MOSFET.

Ex. 1001 ('634 Hsieh)

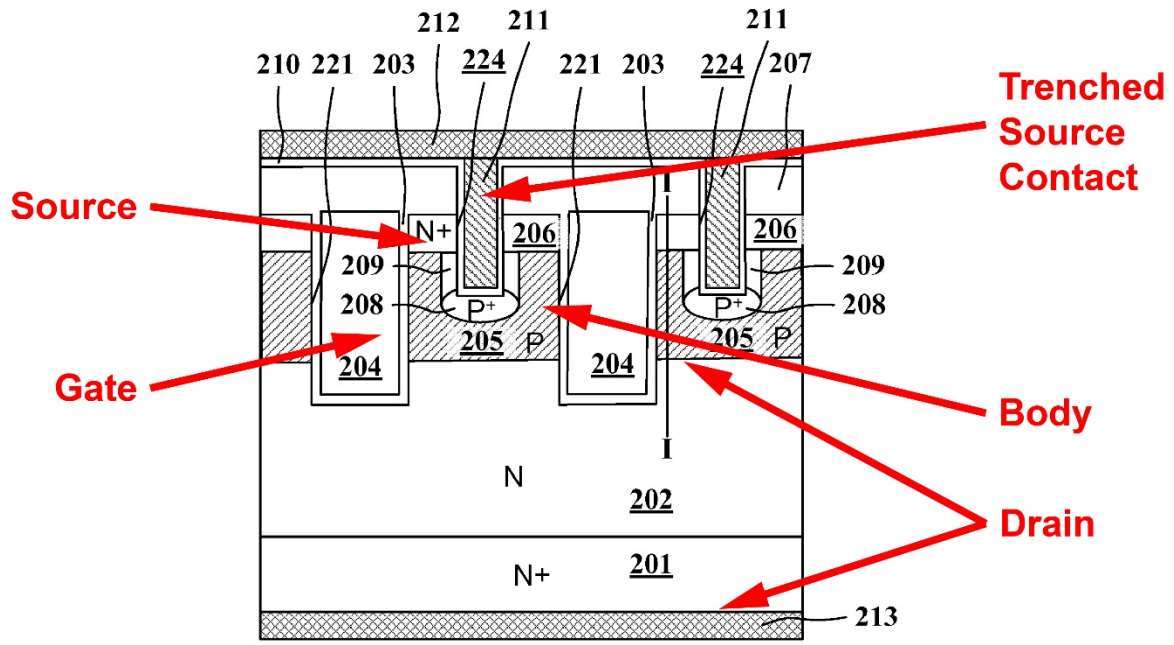


Fig. 2G (Annotated)

The drain of the transistor is an extended structure, reaching from the bottom edge of the body region all the way down to the bottom of the substrate–where the drain contact (213) is provided.

129. Note also that while the ’634 Patent refers to a “trenched source contact” (211), this structure in fact provides the required (for a MOS transistor) body contact–while also making direct electrical contact with the source (and thus directly-connects together the body and the source of the transistor); this is a common practice in the MOS transistor art.

130. In addition, it should be noted that this source (i.e., combined source-body) contact needs to be placed on the top side of the depicted structure–since the bottom surface of the substrate is already taken up by the drain contact.

131. A notable aspect of the ’634 Patent can be ascertained via examination of the admitted prior art that the includes as Fig. 1:

Ex. 1001 ('634 Hsieh)

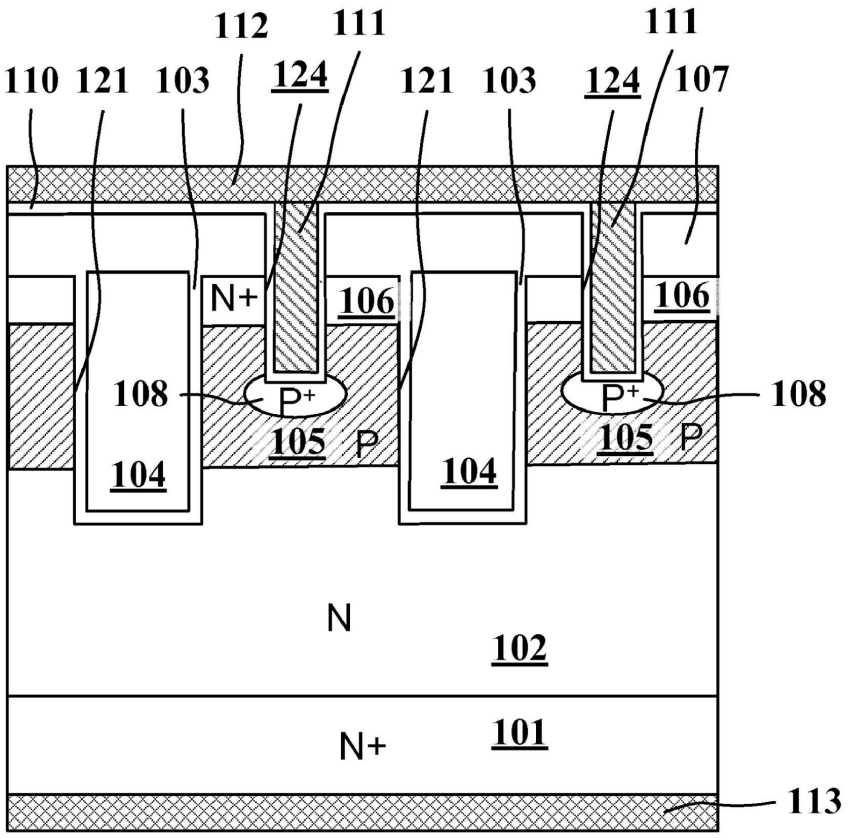


Fig. 1 (PRIOR ART)

When comparing this depiction with the stated sole allowable structure—specifically as illustrated in Fig. 2G of the ’634 Patent—there is only one material

difference between the two. In Fig. 2G, the "lateral contact layers" (element 209) are added to the structure shown in Fig. 1. This addition represents the only allegedly novel and inventive subject matter actually claimed by the '634 Patent.

132. As described above, all of the claims of the '634 Patent are directed to an apparatus, and each incorporates the introduction of the "lateral contact layer" (element 209) into the prior art structure. However, the claims do not recite any specific method for forming these lateral contact layers. While the specification discusses the use of ion implantation—a well-known technique in the art—for this purpose, it should be noted that other methods for forming such doped regions were also well known in the art at the time of the '634 Patent.

133. It should also be noted that the '634 Patent–as is also the case with the Hshieh ('384) reference and the Uno ('864) reference (and as is also typical for discussions of semiconductor processing engineering)–views things from the perspective of a "cross-sectional" viewpoint; that is, the device structures are evaluated along the plane of a vertical cut-through of the structure(s). This is due to the processing methods of integrated circuit engineering, which largely operate in a top-down fashion–and (outside of doping) the use of those processing steps (to build up a full IC structure) in sequence so that "layers" rise (in location) vertically as the IC structure is built up during the sequential steps of the manufacturing flow.

134. In the ’634 Patent, this manifests itself as some challenging terminology–which appears (at least as far as the material considered here is concerned) only in the ’634 Patent. The ’634 Patent refers to “regions” of the trenched-gate MOSFET device as actual defined-and-operational parts of that device–such as the “source region(s)” to refer to the source(s) of the MOSFET, and the “body region(s)” to refer to the body(s) of the MOSFET.

135. However, the ’634 Patent provides some confusion by also referring (both in the claims and in the specification) to what it calls “layers”–such as the “source layer” and the “base layer.” In the ’634 Patent, these two layers–from the cross-sectional viewpoint–are treated as being simple horizontal layers that extend laterally across the entire structure. This seems like a strange thing to do–and while the ’634 Patent provides no explanation for this situation, it is fairly easy to intuit what is going on.

136. The process sequence described in the ’634 Patent begins by growing an epitaxial layer on the silicon–and then forming and filling the trenches that provide the (trenched) locations for the gate dielectric and the gate electrode. After this is done, ion implantation is used to provide doping into the silicon of the MOSFET-to-be structure–with a p-type layer created below the surface (to provide the body of the transistor) and an n+-type layer created at the surface (to provide the source of the transistor); this is depicted in Fig. 2C of the ’634 Patent:

Ex. 1001 ('634 Hsieh)

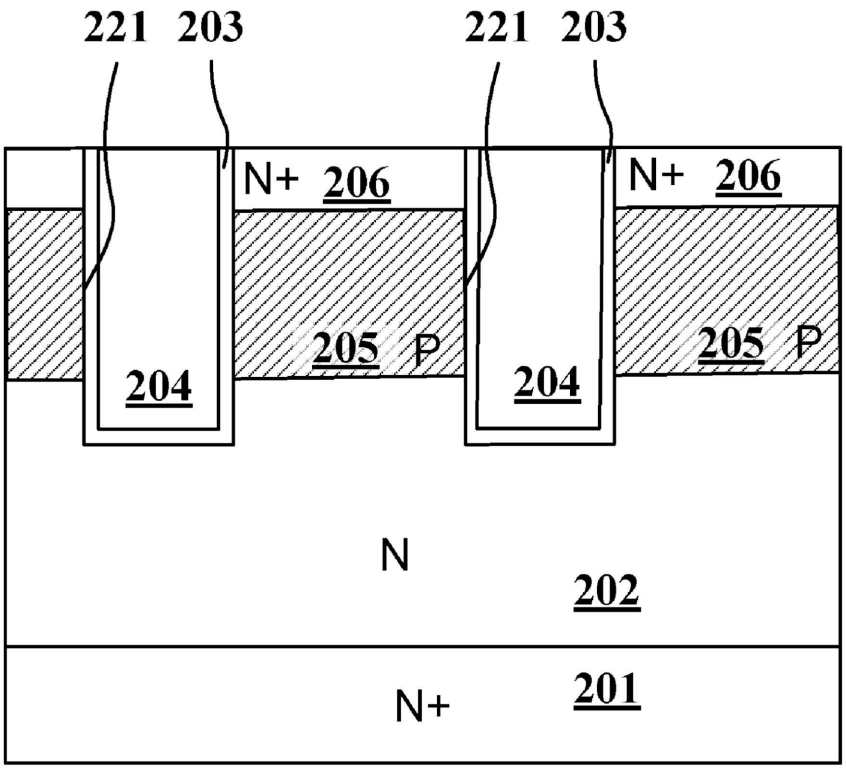


Fig. 2C

The specification of the ’634 Patent identifies 203 as being the gate dielectric 204 as being the gate electrode, the p-type layer 205 as the “base layer,” and the n+-type layer (206) as the “source layer.” (’634 Patent at 3:26-40.)

137. Once these doped layers are formed, an interlayer dielectric film is deposited, and the source contact trenches are etched; these trenches are etched vertically (as usual), and extend downward–completely through the source layer, and partially into the base layer; this is depicted in Fig. 2D of the ’634 Patent:

Ex. 1001 ('634 Hsieh)

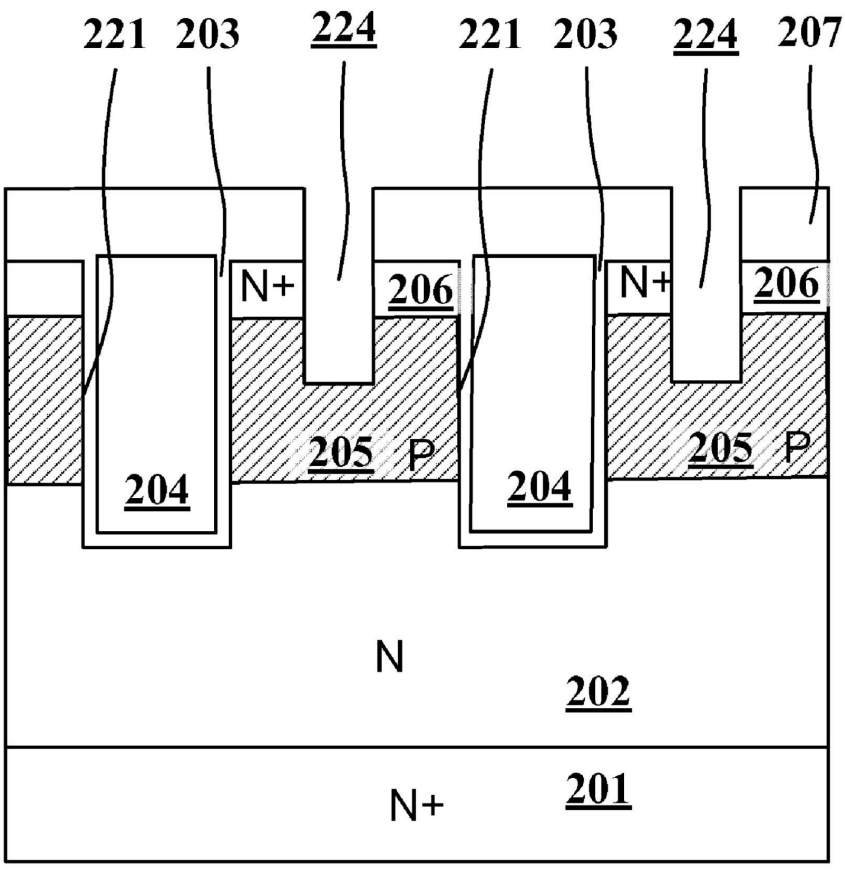


Fig. 2D

The specification of the ’634 Patent identifies 207 as being the interlayer oxide film and 224 as being the (as yet unfilled) source contact trench.

138. In the ’634 Patent, the regions 205 and 206 are, respectively, the “base layer” and the “source layer” that are described in the ’634 Patent. The patent further describes the base layer as corresponding to the body region of the trenched MOSFET, and the source layer as corresponding to the source region of the

trenched MOSFET (’634 Patent at Abstract, 1:52-55, and 4:66-5:2–as well as in Claim 1).

139. Unlike the “base layer” (which is specifically identified in the figures as 205) and the “source layer” (which is specifically identified in the figures as 206), the ’634 Patent identifies the “body region” and the “source region” only through this language–and provides no further details about what is meant by these two terms. However, for purposes here, the “body regions” can be regarded as transistor-specific subsets of the larger (in extent) “base layer,” while the “source regions” can be regarded as subsets of the larger (in extent) “source layer.”

140. The interplay between “layers” and “regions” will become clearer during the claim-by-claim analysis of Section XI.

B. Prosecution History

141. The application which led to the issuance of the ’634 Patent was filed on February 23, 2008–and claims no earlier priority date. As this date is before the codification into federal patent law of the “American Invents Act” of 2012, it is my understanding that the ’634 Patent must be evaluated on a “pre-AIA” basis.

142. On July 28, 2009, the applicant received a notice of allowance–and after publication of the application on August 27, 2009, U.S. Patent No. 7,629,634 issued on December 8, 2009.

143. Notably, in the “Reasons for Allowance,” the Examiner stated that:

Claims 1-9 are allowed.

144. The following is an examiner's statement of reasons for allowance:

> *Claim 1 limits the trenched MOSFET to having a trench in which the base and entire sidewall are covered with the lateral trench contact layer. Kobayashi (US 6,888,196) covers the base and only a portion of the trench sidewall with the lateral contact layer.*
>
> Claims 2-9 are allowed as being properly dependent upon allowed claim 1.

145. This comports with what was said above regarding the one allowable aspect claimed by the '634 Patent.

IX. CLAIM TERMS AND CLAIM CONSTRUCTION

146. With certain exceptions (to be detailed below), I have given the terms in the Challenged Claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '634 Patent. I have applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

147. However, after reviewing the '634 Patent, it is my conclusion and opinion that certain terms in the claims of the '634 Patent require construction.

A. Independent Claim 1: "the bottom base of said trenches in said base layer"

148. Based on the specification and file history of the '634 Patent, this claim term should be construed as:

> **"the bottom base of said trenches in said base layer, defined as the region of the base layer located below a horizontal plane intersecting the lowest point of said trenches"**

This proposed construction is based on an analysis of the intrinsic evidence– that is, the specification of the '634 Patent.

149. The '634 Patent describes a prior art trench-gated MOSFET in which "the P+-type region is located **only at [*the*] source contact trench bottom**." (*See* Ex. 1001, '634 Patent, 1:33-35 (*emphasis added*), Fig. 1 (which is labeled as "Prior Art"); *see also* 2:3-8.) In order to distinguish itself from this admitted prior art, the '634 Patent specification describes a MOSFET with a distinct base contact layer and a lateral contact layer. "The P+-type base contact layer (208) and the P*-type lateral contact layer (209) are formed **at the bottom** and **sidewall** of the source contact trenches (224), **respectively**." (*See* Ex. 1001, '634 Patent, 5:9-12 (*emphasis added*).)

150. Notably, the '634 Patent explicitly describes the formation process of the base contact layer as "to form a P+-type base contact layer (208) **under the**

bottom of the source contact trench (224)" (*See* Ex. 1001, '634 Patent, 3:50-55 (*emphasis added*).)

151. Accordingly, given the description of the base contact layer ('634-108/208) being formed at or beneath the bottom of the source contact trench ('634-124/224), and considering the patent's explicit contrast with prior art having a P+-type region located only at the bottom, the bottom of the source contact trench ('634-124/224) must necessarily be defined by the boundary separating the trench sidewalls from the trench bottom.

152. Below, Fig. 2G of the '634 Patent has been annotated in accordance with the patent's teachings; it clearly illustrates the boundary location which defines the bottom of the source contact trench ('634-124/224) *and* the trench sidewall within the base layer ('634-105/205)–which together delineate the region which the patent identifies as the lateral contact layer ('634-209).

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Ex. 1001 ('634 Hsieh)

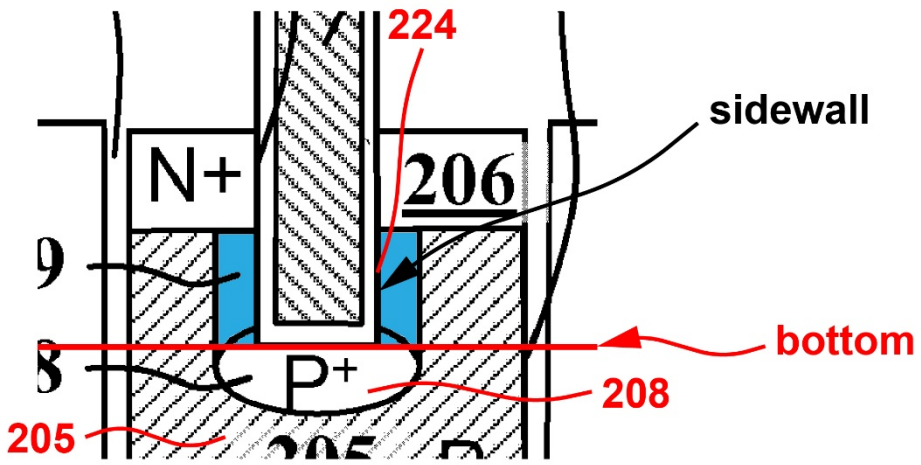


Fig. 2G (Annotated partial enlarged view)

B. Independent Claim 1: "the sidewalls of said trenches in said base layer"

153. Based on the specification and file history of the '634 Patent, this claim term should be construed as:

> **"the sidewalls of said trenches in said base layer, defined as the portion of said trenches within said base layer above a horizontal plane intersecting the lowest point of said trenches"**

154. Reviewing the intrinsic evidence, the '634 Patent claim 1 explicitly states that "**the sidewalls** of said trenches in said base layer **are covered by the lateral contact layer**" (*See* Ex. 1001, '634 Patent, claim 1.) The patent further specifies: "[E]ach of the source contact trenches has **a lateral contact layer at a sidewall** thereof." (*See* Ex. 1001, '634 Patent, 1:66-67.) This clearly differentiates the invention from prior art by emphasizing the sidewall ohmic contact:

"Compared with the conventional trenched MOSFET, the present invention provides good ohmic contact **to sidewall** [*sic*] of the source contact…" -whereas the prior art that is explicitly referenced in the '634 Patent is described not having an ohmic contact in this region, due to low doping concentration of the unaltered body region: "The sidewall of [the]source contact trench has no ohmic contact (due to low doping concentration of P base) with the contact metal plug…" (*See* Ex. 1001, '634 Patent, 1:36-37.)

155. Further reinforcing this definition, the '634 Patent explicitly describes the formation of the lateral contact layer at the sidewalls via the use of angled ion implantation:

> "…another implantation procedure of BF2 with angle ranging from 45 to 80 degree respective to the surface of the epitaxial layer (202) and dose ranging from 1E14 to 4E14 cm-2, and another activation by heat treatment are carried out to form a P*-type lateral contact layer (209) **at the sidewall of the source contact trench** (224)..." (*See* Ex. 1001, '634 Patent, 3:56-61.)

156. Further, the '634 Patent explicitly differentiates the lateral contact layer ('634-209) from the base contact layer ('634-108/208). (*See* Ex. 1001, '634 Patent, 5:9-12.) "The P+-type base contact layer (208) and the P*-type lateral contact layer (209) are formed **at the bottom** and **sidewall** of the source contact trenches (224), **respectively**." (*emphasis added*). Since the '634 Patent specifies the base contact layer ('634-108/208) as positioned at or beneath the bottom of the

trench (’634-124/224), it logically follows that the sidewalls—and thus the lateral contact layer (’634-209)—must be located above the bottom of the source contact trench (’634-124/224) within the body region (’634-105/205). (*See* Ex. 1001, ’634 Patent, 3:50-55.) (“to form a P+-type base contact layer (208) **under the bottom** of the source contact trench (224)”) (*emphasis added*).

X. OVERVIEW OF THE PRIOR ART REFERENCES

157. This section provides brief overviews of the main prior art references that I used in my analysis (which will be detailed in Section XI).

A. The Hshieh (’384) Reference

158. The Hshieh (’384) reference is U.S. Patent Publication 2006/0273384, entitled “Structure for Avalanche Improvement of Ultra High Density Trench MOSFET.” The sole listed inventor is Fwu-Iuan Hshieh, and the listed assignee is M-MOS San. Bhd. The application was filed on September 26, 2005, and claims a priority date of June 6, 2005 based on an earlier application; the publication date is December 7, 2006. These dates indicate that Hshieh (’384) is prior art to the ’634 Patent; however, it is my understanding that this patent application falls under the “pre-AIA” legal standards. Also, this application was never pursued to the issuance of a patent–and is marked as “abandoned” on the USPTO website.

159. Hshieh (’384) also discloses trench-gated MOSFET structures, such as the one depicted in Fig. 3:

Ex. 1005 ('384 Hshieh)

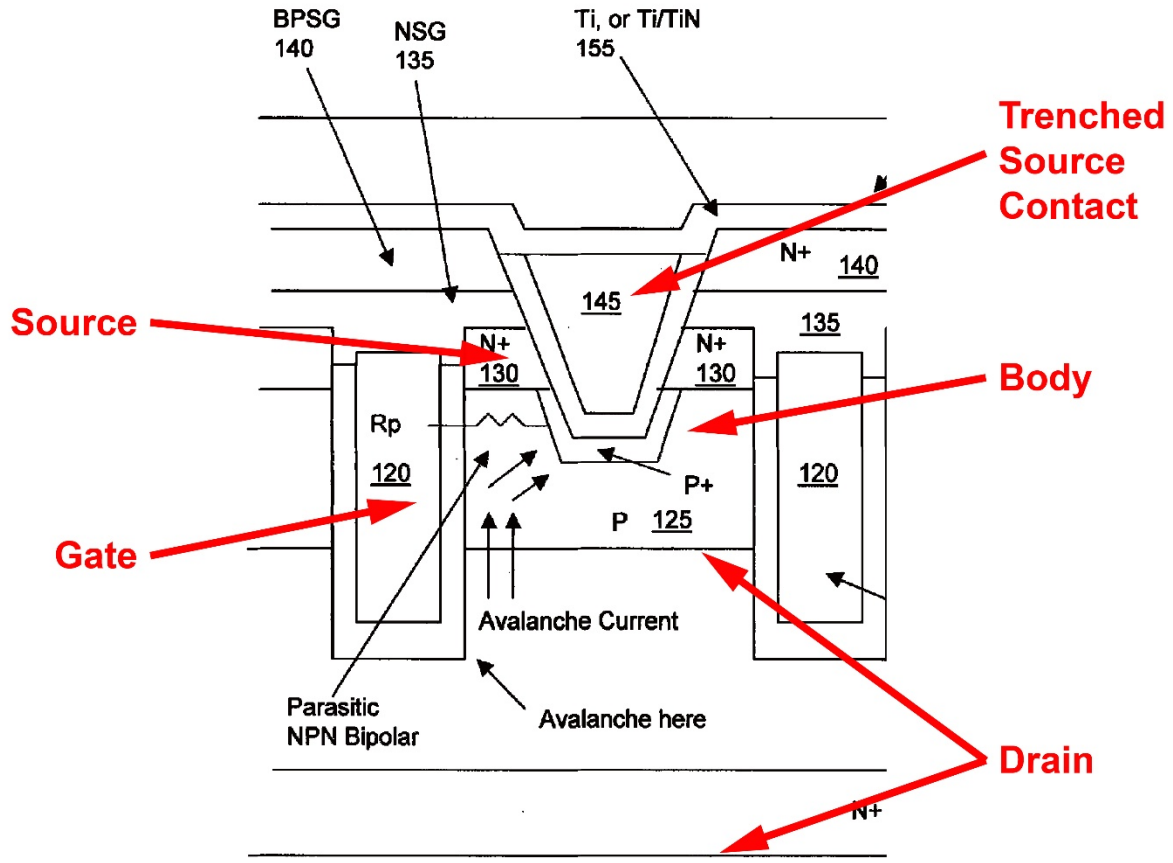


Fig. 3 (Annotated partial enlarged view)

Hshieh ('384) contains multiple embodiments, such as the embodiment of Fig. 4 (which depicts source-contact trenches that are vertical rather than sloped) that is also a trench-gated MOSFET structure:

Ex. 1005 ('384 Hshieh)

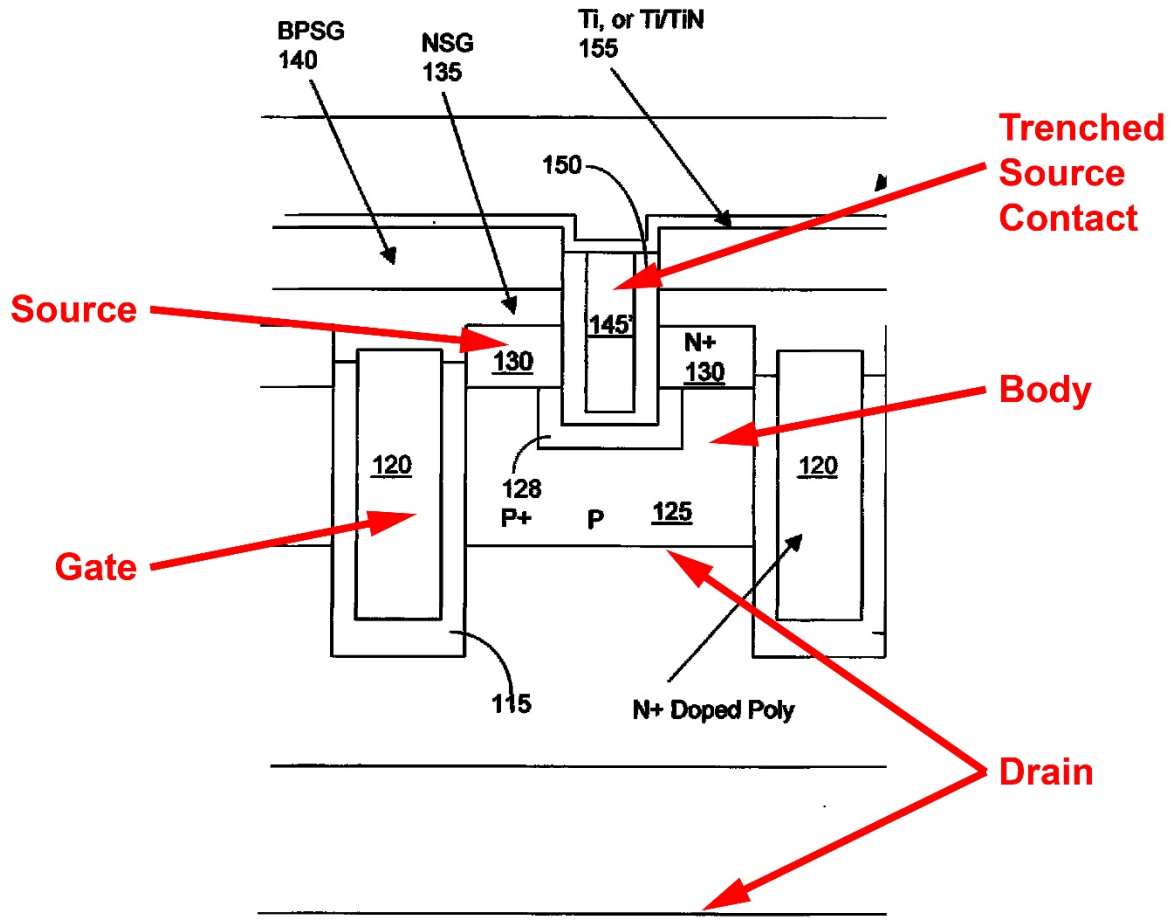


Fig. 4 (Annotated partial enlarged view)

160. Unlike the ’634 Patent, Hshieh (’384) includes method claims that describe method of fabricating the structures described in the claims and specification; however, like the ’634 Patent, ion implantation is the only method of doping the silicon that is discussed (here, both in the claims and in the specification).

161. It is my understanding that inventor “Fwu-Iuan Hshieh” of Hshieh (’384) and inventor “Fu-Yuan Hsieh” of the ’634 Patent are the same individual.

B. The Uno ('864) Reference

162. The Uno ('864) reference is U.S. Patent No. 6,984,864, entitled "Semiconductor Device with MISFET Having Low Leakage Current." "MISFET" is an acronym that is identical to the acronym MOSFET, except that the "O" ("oxide") in MOSFET is not used and the more-general "I" ("insulator") is used. This more-general "insulator" allows the term "MISFET" to cover a wider range of devices–with "MOSFET" being a subset of "MISFET." As an online reference explains,

> The Metal Insulator Semiconductor Field Effect Transistors (MISFETs) is [*sic*] one of the most widely used electronic devices, particularly in digital circuits, because of relatively small size-thousands of devices can be fabricated in a single integrated circuit (IC). Since it is constructed with the gate terminal insulated from the channel, it may be referred to generally as an insulated-gate field-effect transistor (IGFET).
>
> However, since most of such devices are made using silicon for the semiconductor, SiO2 for the insulator, and metal or heavily doped polysilicon for the gate electrode, the term metal-oxide-semiconductor field-effect transistor (MOSFET) or simply MOS is commonly used. MISFET is the more general term, where the insulator is not necessarily silicon dioxide (SiO2) and the semiconductor is not necessarily silicon (Si). Here discussion will be about MOSFETs although the same physics applies to the Metal Insulator Semiconductor Field Effect Transistors.
>
> (*See* Ex. 1012, *Metal Insulator Semiconductor Field Effect Transistors (MISFETs)*, EEEGUIDE, https://www.eeeguide.com/metal-insulator-semiconductor-field-effect-transistors-misfets/ (last visited July 31, 2025).)

163. The listed inventors of Uno ('864) are Tomoaki Uno and Yoshito Nakazawa, and the listed assignee is Renesas Technology Corp. The application that eventually led to the issuance of Uno ('864) was filed on June 18, 2003, and claims a priority date of July 19, 2002 based on an earlier Japanese patent application; the publication date (as US 2004/0012050) is January 22, 2004, and the patent was issued on January 10, 2006. These dates indicate that Uno ('864) is prior art to the '634 Patent; however, it is my understanding that this patent falls under the "pre-AIA" legal standards.

164. Uno ('864) also discloses trench-gated MOSFET structures, such as the one depicted in Fig. 38:

Ex. 1006 ('864 Uno)

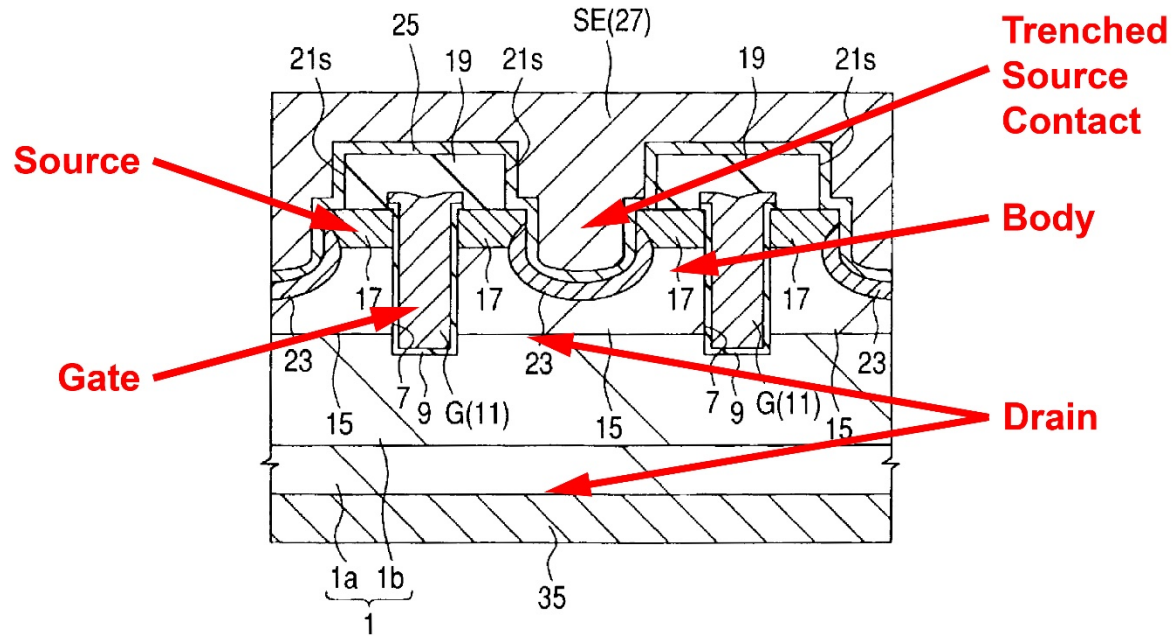


Fig. 38 (Annotated)

Uno (’864) provides multiple embodiments, all of which are similar to the structure depicted in Fig. 38.

165. Like the ’634 Patent, all of the claims of Uno (’864) are apparatus claims; however, also like the ’634 Patent, the specification of Uno (’864) discusses methods of fabricating the disclosed structures–including the use of ion implantation for doping of silicon.

C. Other References

166. In my analysis of the ’634 Patent and the available prior art literature, I was able to identify a large number of prior art references which demonstrate the state of knowledge of a POSITA in 2008 regarding various techniques that were already in widespread use at the time for the fabrication of silicon integrated circuit structures of various sorts (including, in particular, those used in silicon processing that involved trenches). These references (which are exemplary among a vast sea of such references) demonstrate that such techniques were well-known in the art by 2008–and would have been well-known to a POSITA at that time; thus, these references demonstrate the level of knowledge of a POSITA in 2008. As will be discussed with respect to Grounds discussed herein, the combination of this demonstrated knowledge of a POSITA with Hshieh (’384), Uno (’864), or combination thereof renders Claims 1-9 of the ’634 Patent obvious.

167. Because these references are being used for the purpose just described, detailed overviews of them will not be provided here; rather, their details will be cited as necessary there for that analysis that will be provided.

XI. UNPATENTABILITY ANALYSIS

168. As will be explained in detail below, it is my conclusion and opinion that all the claims of the ’634 Patent are unpatentable–as they are either taught the time of the filing of the ’634 Patent application by Hshieh (’384) or are obvious by Hshieh (’384) in view of the knowledge of a POSITA, are taught by Uno (’864) or are obvious by Uno (’864) in view of the knowledge of a POSITA, or are rendered obvious by Hshieh (’384) in combination with Uno (’864) or vice versa in view of the knowledge of a POSITA.

169. With regard to the obviousness analysis presented below, it should be noted that while specific prior art references are cited in portions of this analysis, the relevant technical content is not exclusive to those references. Other prior art sources also demonstrate that the teachings relied upon were well known in the art at the time of the ’634 Patent’s filing. The references selected for this analysis are exemplary, and numerous additional references could be cited to establish the same points and support the same conclusions.

A. Ground 1–Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being Obvious Over Hshieh ('384)

170. It is my conclusion and opinion that Claims 1-9 of the '634 Patent are either taught by Hshieh ('384), or are rendered obvious by Hshieh ('384) in combination with the knowledge of a POSITA.

171. As briefly noted earlier (in Section X.C), the knowledge of a POSITA at the time of the filing of the '634 Patent (2008) can readily be ascertained by examination of some of the relevant technical literature (books, papers, patents, etc.) It was also noted there that this literature is vast and deep–and that a few references can be chosen from this vast sea to demonstrate the knowledge of a POSITA at the relevant time; this will be done as necessary below, in the claim-by-claim analysis.

1. A POSITA Would Have Had a Motivation and a Reasonable Expectation of Success

172. It is my conclusion and opinion that, based on my education, training, and experience, a person of ordinary skill in the art ("POSITA") would have been motivated, as of the Filing Date of the Challenged Patent, to implement the teachings of Hshieh (U.S. Patent Application Publication No. US 2006/0273384) in view of his/her existing knowledge and known-and-routine engineering practices. A POSITA would have recognized that Hshieh ('384) addresses specific design objectives—such as managing trench-gated vertical conduction paths in

MOSFET devices—using methods that align with contemporary device performance and manufacturability requirements. Thus, a POSITA would have had a clear reason to apply Hshieh ('384) in the claimed context–not merely because it existed in the art, but because it offered a solution to a recognized problem in the field; this is consistent with what I understand is the "flexible motivation analysis" endorsed by the Supreme Court in *KSR International Co*., and in the Federal Circuit under the "obvious-to-try" rationale.

173. Furthermore, it is my conclusion that a POSITA would have had a reasonable expectation of success in applying Hshieh ('384)'s teachings without undue experimentation. At the relevant time, the structures and the fabrication techniques disclosed in Hshieh ('384) were well-understood *and* predictably-operable within standard silicon processing flows. The predictable nature of the trench-MOSFET architectural choices in Hshieh ('384), and their compatibility with known fabrication protocols, provides a solid basis for concluding that success would be expected—not merely hoped for—even if specific sub-elements were unstated or unlabeled in the reference.

174. My analysis explicitly avoids impermissible hindsight in two respects. First, it relies solely on the state of the art as of the Filing Date—namely Hshieh ('384) itself and general contemporaneous engineering knowledge, and not on the teachings of the Challenged Patent. Second, the motivation and expectation of

success are based on reasoned explanations grounded in the field's known problems, design incentives, and standard practices—not on hindsight reconstructions after knowing the patent outcome.

2. Independent Claim 1

175. Claim 1 is an independent claim–and is the only independent claim of the '634 Patent; it is also an apparatus claim.

a. [1-preamble]: "A trenched MOSFET with trenched source contact, comprising:"

176. To the extent that a preamble is limiting, Hshieh ('384) teaches the preamble of Claim 1–as can easily be seen via simple examination of Hshieh ('384).

177. Hshieh ('384) discloses a "trenched MOSFET," as can be seen via the Abstract of Hshieh ('384) :

> A trenched metal oxide semiconductor field effect transistor (MOSFET) cell that includes a trenched gate surrounded by a source region encompassed in a body region above a drain region disposed on a bottom surface of a substrate. (Ex. 1005, Hshieh ('384), Abstract.)

178. Further, Hshieh ('384) also discloses a "trenched source contact":

> The MOSFET cell further includes a source-body contact trench opened with sidewalls substantially extend vertically relative to a top surface into the source and body regions and filled with contact metal plug. (Ex. 1005, Hshieh ('384), Abstract.)

179. Both the "trenched MOSFET" and the "trenched source contact" of Hshieh ('384) are also evident in this annotated excerpt from Fig. 3 of Hshieh ('384):

Ex. 1005 ('384 Hshieh)

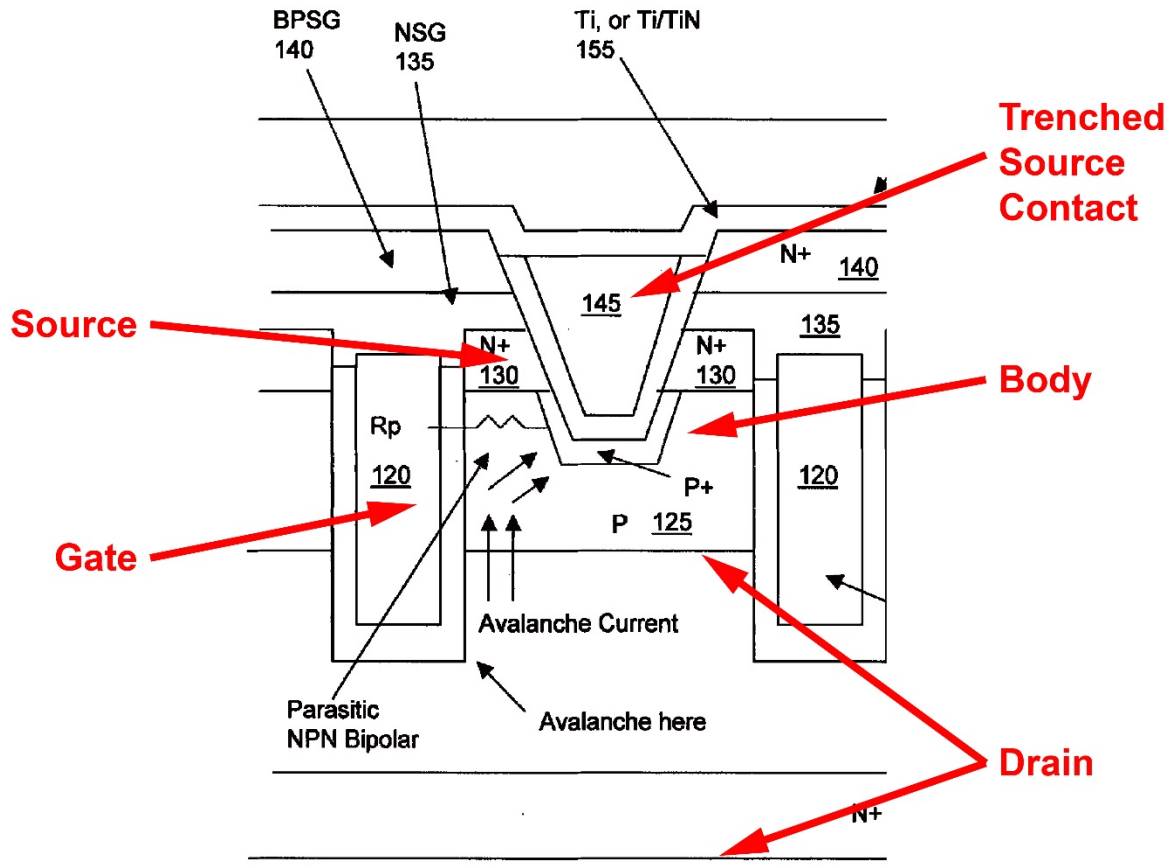


Fig. 3 (Annotated partial enlarged view)

180. It should be noted that what the '634 Patent calls a "source contact" and what Hshieh ('384) calls a "source-body contact" are the same thing–as in both instances, the source of the MOS transistor and the body of the MOS transistor are connected together by that contact; the connecting-together of the source and the

body of a MOS transistor is a common and well-known practice in the art. (*See* Ex. 1013, Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits,* 236-237 (5th ed. 2004).) Further, in some prior art references (*see* Ex. 1014, U.S. Patent No. 4,980,747), this same sort of contact is called simply a "substrate contact". Accordingly, in this Declaration, the terms "source contact", "source-body contact", and "substrate contact" are intended—unless otherwise noted—to refer to the same structure. Any variation in terminology reflects the usage in the respective reference from which the term is drawn.

i. [1-preamble-1]: "trenched MOSFET."

181. ***[1-preamble-1]*: "trenched MOSFET."** Hshieh ('384) discloses a "trenched MOSFET", which I will refer to as *[1-preamble-1]*, for the reasons set forth above and as further elaborated as follows. Hshieh ('384) expressly states that "[a] first preferred embodiment of this invention [is] where a metal oxide semiconductor field effect transistor (MOSFET) device 100" is provided. (Ex. 1005, Hshieh ('384), ¶[0026].) Further, Hshieh ('384) discloses that "[t]his invention further discloses a method for manufacturing a trenched metal oxide semiconductor field effect transistor (MOSFET) cell comprising a step of forming said MOSFET cell with a trenched gate surrounded by a source region encompassed in a body region above a drain region disposed on a bottom surface of a substrate." (*Id.* ¶[0014].) This language confirms that the disclosed structure is

a trenched MOSFET device–which features a source/body/drain region configuration and a trench gate; consistent with the type of device claimed in the ’634 Patent. Based on the above, it is my conclusion and opinion that Hshieh (’384) expressly discloses a trenched MOSFET structure, and thus teaches limitation *[1-preamble-1]*–“trenched MOSFET”.

ii. [1-preamble-2]: “trenched source contact.”

182. ***[1-preamble-2]*: “trenched source contact.”** Hshieh (’384) also teaches a “trenched source contact,” which I will refer to as *[1-preamble-2]*. Before beginning the analysis of this limitation, it should once again (see above) be noted that what the ’634 Patent calls a “source contact” (’634-124/224) and what Hshieh (’384) calls a “source-body contact” are the same thing–as in both instances, the source of the MOS transistor and the body of the MOS transistor are connected together by that contact.

183. Returning to the analysis, Hshieh (’384) teaches this claim limitation *[1-preamble-2]* in the Abstract–differing (as explained above) only by calling this a “source-body contact”:

> The MOSFET cell further includes a source-body contact trench opened with sidewalls substantially extend[ing] vertically relative to a top surface into the source and body regions and filled with contact metal plug. (Ex. 1005, Hshieh (’384), Abstract.)

184. In addition, Hshieh ('384) states that "[f]or the purpose of improving the source contact to the source regions 130, a plurality of trenched source contact [sic] [is] provided." (Ex. 1005, Hshieh ('384), ¶[0027].) This disclosure makes clear that Hshieh ('384) teaches the use of trenched contacts that are specifically designed and included for the purpose of providing an electrical connection to the source regions (and also the body regions) of the MOSFET device.

185. The specification further details the construction of these trenched source contacts, starting with an etched trench opening (element 244/244'), then filled with a tungsten plug (element 145/145') and further surrounded by a barrier layer of Ti/TiN (element 150/150'/245)–both of which are implemented within the trench structure. (*Id.* ¶¶[0034-0035], Fig. 9F, element 244, claims 1, 3, 4, 5, 11-15, 19- 20, 23-24, 26, 31; ¶[0036], element 244'; ¶¶[0027], [0031], Figs. 3, 6, claims 1, 7-9, 16, 26, element 145; ¶¶[0029]-[0030], [0032], Figs. 4-5, 7-8, element 145'; ¶¶[0027]-[0028], [0031], Figs. 3-8, claim 7, element 150; ¶¶[0029]-[0030], element 150'; ¶[0035], Figs. 9I-9J, element 245.)

186. Notably, Hshieh ('384) explains: "Referring to FIG. 3 again, the source-body trenched contact 145 surrounded by the barrier layer 150 as shown are opened with a slope relative to the regular perpendicular direction for contacting a P+ doped region 128 surrounding the source-body trenched contact." (*Id.* ¶¶[0028]; *see also* [0032]-[0033], element 128'.)

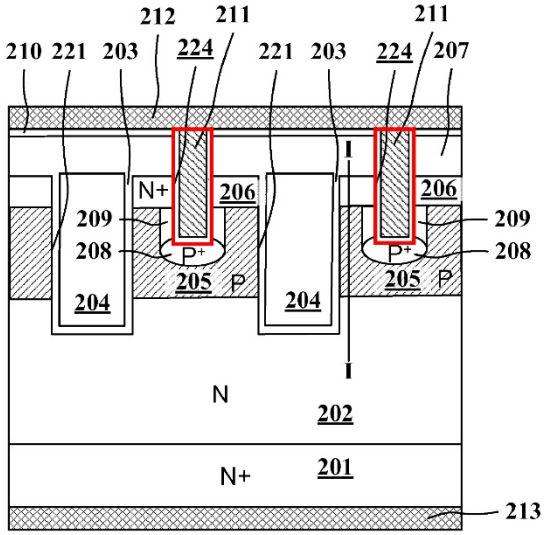
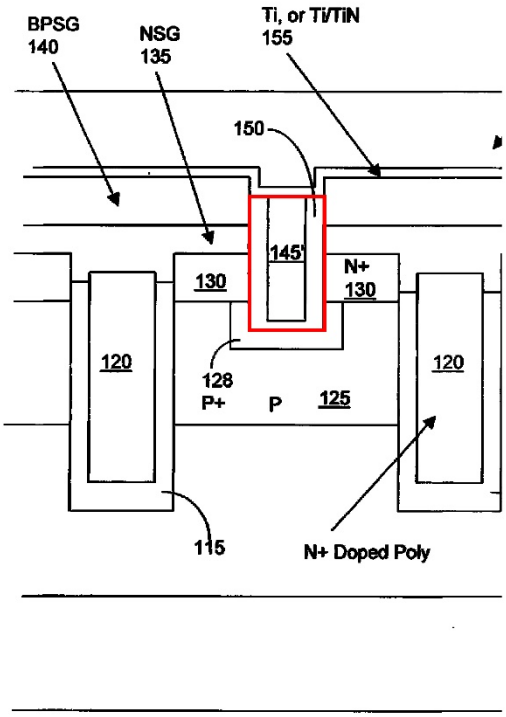
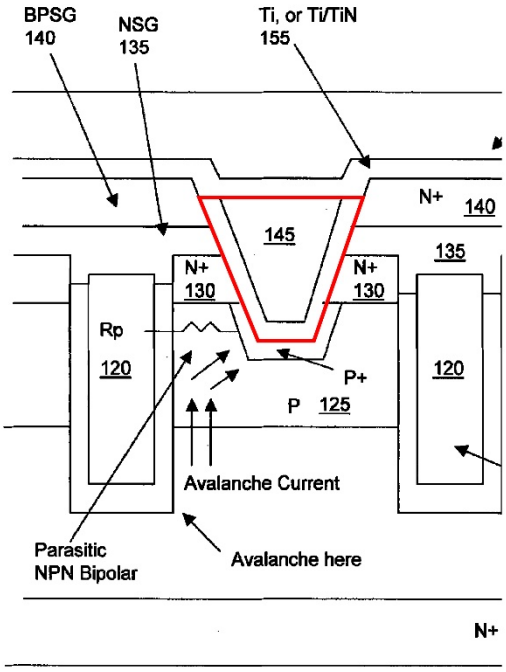
187. This statement illustrates the structural and electrical function of the contact—namely, to provide a conductive path that (electrically) ties together the source and body regions; this is done by forming a trench that is in contact with both the source region(s) and the body region(s), and using a metal contact plug embedded in a barrier layer to provide the aforementioned electrical connection.

188. Taken together, these disclosures confirm that Hshieh (’384) teaches the formation and function of trenched source contact structures, consistent with those recited in the ’634 Patent. Accordingly, it is my conclusion and opinion that Hshieh (’384) teaches limitation *[1-preamble-2]*–“trenched source contact”.

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[1-preamble-2]

trenched source contact

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

189. For the reasons stated above and to the extent the preamble is limiting, Hshieh ('384) teaches both the "trenched MOSFET" and the "trenched source contact" of the '634 Patent–and thus teaches the preamble of Claim 1.

b. [1a]: "a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"

190. This claim element of Claim 1 of the '634 Patent is taught by Hshieh ('384).

191. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [1a-1]: "a semiconductor region having a drain region, a body region and a source region, comprising,"

192. This claim sub-element is taught by Hshieh ('384). All of these "regions" are present in Hshieh ('384), as evidenced by this excerpt from the Abstract of Hshieh ('384):

> A trenched ***metal oxide semiconductor field effect transistor (MOSFET)*** cell that includes a trenched gate surrounded by a ***source region*** encompassed in a ***body region*** above a ***drain region*** disposed on a bottom surface of a ***substrate***. (Ex. 1005, Hshieh ('384), Abstract; *emphases added*.)

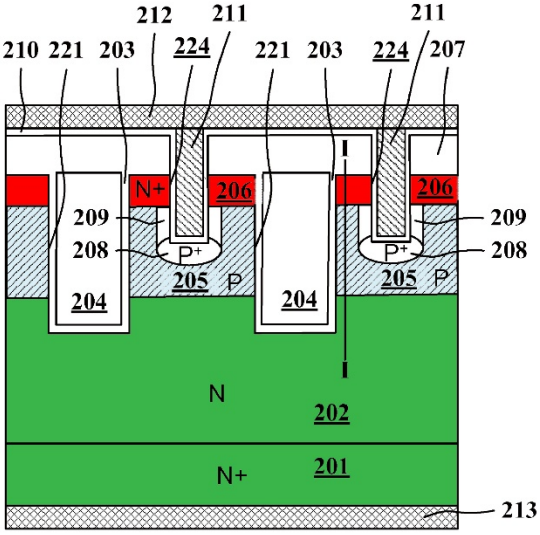
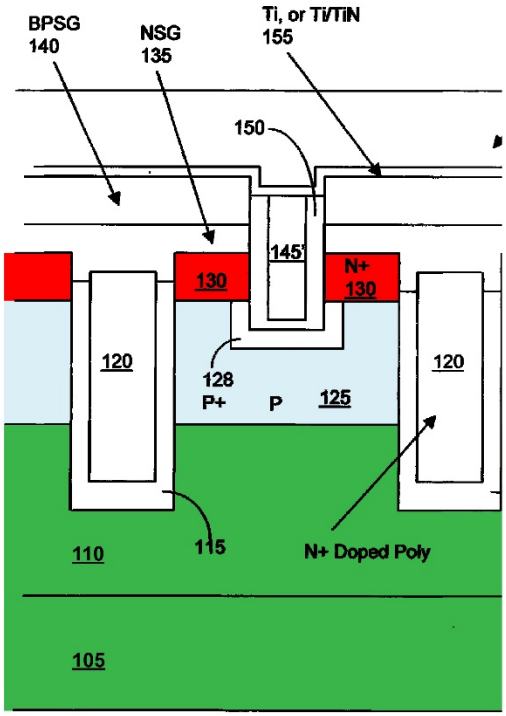
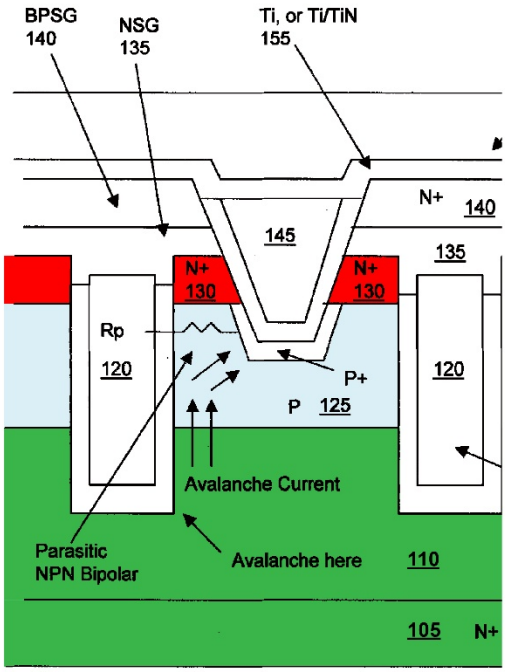
By definition, a MOSFET includes a source region, a body region, and a drain region that are all formed together in a unitary sample of a semiconductor material (i.e., a semiconductor region).

1) [1a-1-1]: "semiconductor region."

193. The limitation *[1a-1-1]*–"semiconductor region"–of the '634 Patent is expressly disclosed by Hshieh ('384). Hshieh ('384) describes a semiconductor region comprising a drain region, a body region, and a source region–arranged in a vertical stack, consistent with the layered structure recited in the '634 Patent (e.g., elements 101/201, 102/202, 105/205, and 106/206 of the '634 Patent). (In the annotated figures below, the drain region has been shaded green, the body region has been shaded light blue, and the source region has been shaded red.)

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[1a-1-1]
semiconductor region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

194. Specifically, Hshieh ('384) discloses "a N+ substrate 105 formed with an N epitaxial layer 110", thereby identifying a heavily doped N+ substrate and an overlying N-type epitaxial layer. (Ex. 1005, Hshieh ('384), ¶[0026]; Figs. 3–8, elements 105 and 110.) The N+ substrate (element 15/105/205) corresponds to the drain region of the claimed structure, while the N-type epitaxial layer (element 20/110/210) corresponds to what is commonly referred to in the art as a "drain extension" or "drift region"—both well-established terms in the field of vertical power MOSFET design. (*Id.* ¶[0006], Fig. 1, element 15; ¶[0026], Figs. 3-8, element 105; ¶[0034], Figs. 9A-9G', claims 1, 5, 11-14, 20, 24, 27-30, element 205; ¶[0006], Fig. 1, element 20; ¶¶[0026], [0028]-[0031], Figs. 3-8, element 110; ¶[0034], Figs. 9A-9G', element 210.)

195. Hshieh ('384) further discloses "an N+ source 130 with a P-body 125 and the N-epitaxial layer 110"–thereby explicitly identifying the source region (element 30/130/230), body region (element 25/125/225), and the underlying drain region (element 20/110/210) in their proper vertical sequence. (*Id*. ¶¶[0028]–[0030]; Figs. 3–8, elements 110, 125, 130; ¶[0006], Fig. 1, element 30, claims 1, 16, 20; ¶¶[0026]-[0030], Figs. 3-8, element 130; ¶[0034], Figs. 9D-9G', element 230; ¶[0006], Fig. 1, element 25; ¶¶[0026]-[0033], Figs. 3-8, claims 1, 2, 6, 16, 20-21, 25, element 125; ¶¶[0034]-[0035], Figs. 9C-J and 9G', element 225; ¶[0006],

Fig. 1, element 20; ¶¶[0026], [0028]-[0031], Figs. 3-8, element 110; ¶[0034], Figs. 9A-9G', element 210.)

196. These disclosures, taken together, establish that Hshieh ('384) teaches a semiconductor device structure comprising, in order from bottom to top: (1) an substrate (15/105/205), (2) a drain region (epitaxial layer 20/110/210), (3) a body region (25/125/225), and (4) a source region (30/130/230). This configuration corresponds directly to the multi-layered semiconductor region recited in the '634 Patent. Therefore, it is my conclusion and opinion that Hshieh ('384) discloses limitation *[1a-1-1]*–"semiconductor region"–of the '634 Patent.

2) [1a-1-2]: "drain region."

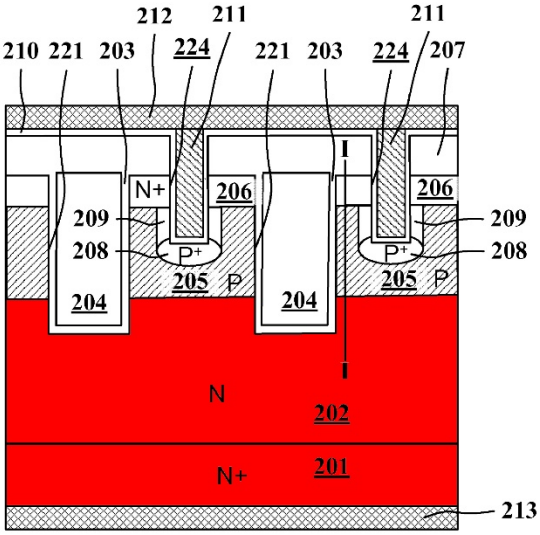
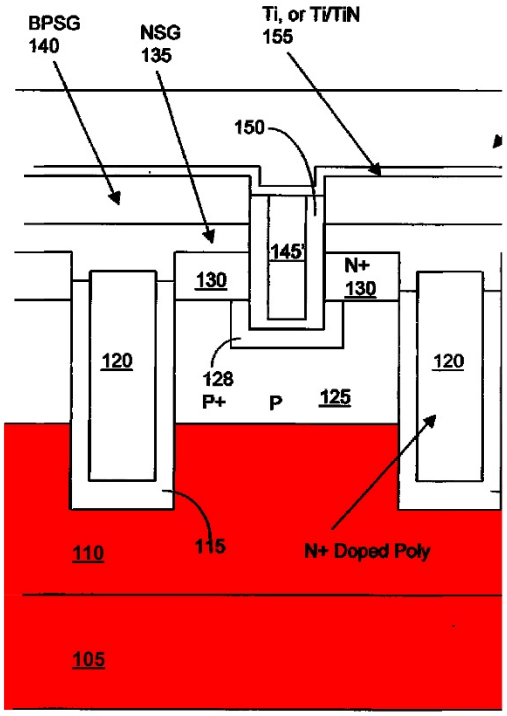
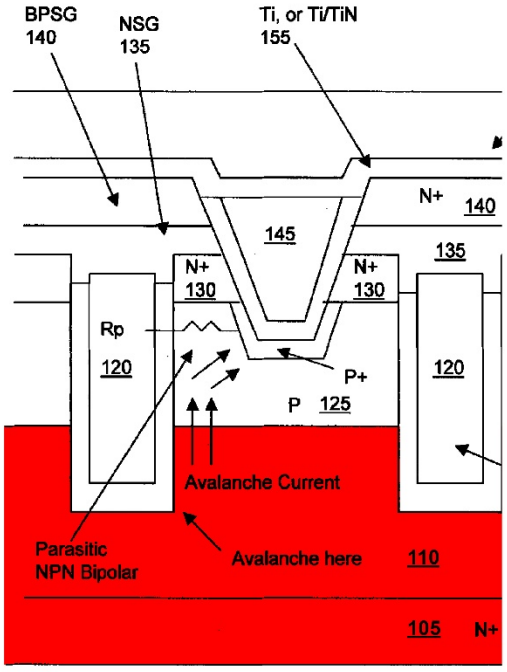
197. To begin, it must first be noted that the '634 Patent identifies the limitation *[1a-1-2]*–"drain region"–as being formed in the epitaxial layer (elements '634-102/202). However, Claim 1 of the '634 Patent introduces ambiguity—based on the grammatical structure of the sentence—as to whether the drain region is limited solely to the epitaxial layer or also includes the underlying silicon substrate. (*See* Ex. 1001, '634 Patent, claim 1.) Although this ambiguity introduces some interpretive uncertainty regarding the precise scope of the claimed drain region, Hshieh ('384) discloses both structures—namely, the epitaxial layer (element 20/110/210) and the substrate (elements 15/105/205)—regardless of whether they are construed collectively or separately as part of the drain region.

(Ex. 1005, Hshieh ('384), ¶[0006], Fig. 1, element 15; ¶[0026], Figs. 3-8, element 105; ¶[0034], Figs. 9A-9G', claims 1, 5, 11-14, 20, 24, element 205; ¶[0006], Fig. 1, element 20; ¶¶[0026], [0028]-[0031], Figs. 3-8, element 110; ¶[0034], Figs. 9A-9G', element 210.)

198. Turning now to Hshieh ('384), Hshieh ('384) expressly recites "a drain region disposed on a bottom surface of a substrate"–which clearly indicates that the device includes a vertically-oriented drain structure. (Ex. 1005, Hshieh ('384), claim 1; claim 20; ¶[0013].) Further, the figures in Hshieh ('384)–such as the annotated figures below–make it clear what Hshieh ('384) means here; the drain region is the lower part of the structure, and extends all the way to the "bottom surface of [the] substrate." (*Id*. claim 1.)

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[1a-1-2]
drain region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

199. The specification of Hshieh ('384) further identifies "an N epitaxial layer 110" as part of the drain region. (*Id.* ¶¶[0026], [0028]–[0031]; Figs. 3–8, element 110.) This epitaxial layer (element 20/110/210) is formed on a heavily doped N^+ substrate (element 15/105/205), and together these layers define a vertical conduction path for the drain current. (*Id.* ¶[0006], Fig. 1, element 15; ¶[0026], Figs. 3-8, element 105; ¶[0034], Figs. 9A-9G', claims 1, 5, 11-14, 20, 24, element 205; ¶[0006], Fig. 1, element 20; ¶¶[0026], [0028]-[0031], Figs. 3-8, element 110; ¶[0034], Figs. 9A-9G', element 210.) Moreover, Hshieh ('384) explicitly states: "this invention where a metal oxide semiconductor field effect transistor (MOSFET) device 100 is supported on a N+ substrate 105 formed with an N epitaxial layer 110." (*Id.* ¶[0026].)

200. In an alternative embodiment, Hshieh ('384) discloses an "epitaxial layer 210," which serves the same structural and functional role in the drain region. (*Id.* ¶[0034]; Figs. 9A–9G', element 210.) In both embodiments, Hshieh ('384) teaches a drain-forming epitaxial layer (element 20/110/210) disposed on an N^+ substrate (element 15/105/205), consistent with the vertically oriented drain structure of the '634 Patent.

201. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a drain region comprising both an epitaxial layer (element 20/110/210) and a substrate (element 15/105/205) that together provide a continuous vertical

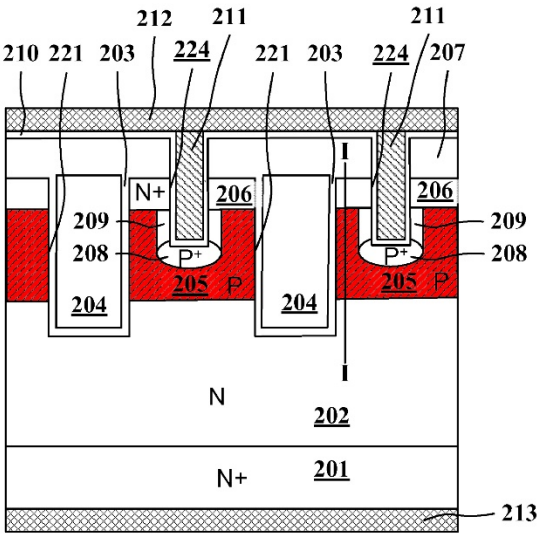
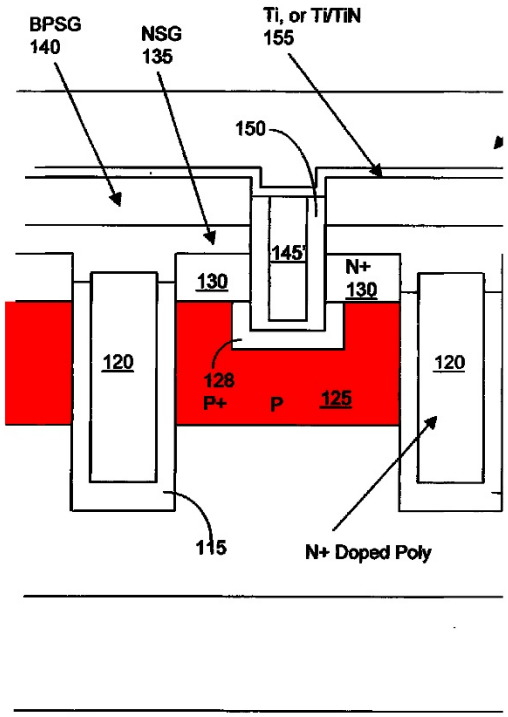
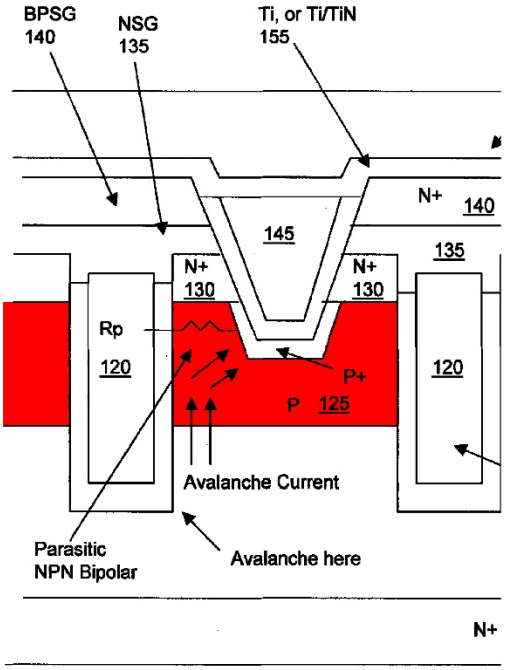
path for current conduction. This structure corresponds to the plain and ordinary meaning of "drain region" as that term would be understood by a person of ordinary skill in the art at the time of the invention. Therefore, limitation *[1a-1-2]*–"drain region"–is taught in Hshieh ('384).

3) [1a-1-3]: "body region."

202. Hshieh ('384) discloses a "body region," which I will refer to as limitation *[1a-1-3]*–"body region." Hshieh ('384) describes a base layer corresponding to the claimed body region, consistent with elements 105/205 of the '634 Patent. The '634 Patent describes a P-type body region disposed above the drain region, forming part of the vertical semiconductor structure–and Hshieh ('384) provides an analogous structure.

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[1a-1-3]
body region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

203. Specifically, Hshieh ('384) refers to "a body region above a drain region," clearly identifying the vertical placement of the body region (element 25/125/225) within the device architecture. (Ex. 1005, Hshieh ('384), ¶¶[0013]–[0014]; Fig. 1; ¶[0006], Fig. 1, element 25; *see also* ¶¶[0026]-[0031], [0033], Figs. 3–8, element 125; ¶¶[0034]-[0035], Figs. 9C–J and 9G', element 225.) The specification further identifies and repeatedly references a "body region 125," which is explicitly described in relation to the surrounding regions such as the source and drain. (*Id.* ¶[0026]; *see also* ¶¶[0027]–[0033]; Figs. 3–8.)

204. In an alternative embodiment, Hshieh ('384) describes a "body region 225," which appears in substantially the same vertical and functional position relative to the source and drain as body region 125 in the first embodiment. (*Id.* ¶¶[0034]–[0035]; Figs. 9C–J and 9G', element 225.) These disclosures are further supported by the claim language of Hshieh ('384), which recites a body region in claims 1, 2, 6, 16, 20, 21, and 25; this indicates the central structural and functional role of the body region within the device.

205. Accordingly, it is my conclusion and opinion that Hshieh ('384) teaches a P-type body region (element 25/125/225) that corresponds to the body region (element 25/125/225) recited in the '634 Patent; the vertical arrangement and role of this body region are consistent with the base layer described in the '634

Patent claims. Therefore, limitation *[1a-1-3]*–"body region"–is taught by Hshieh ('384).

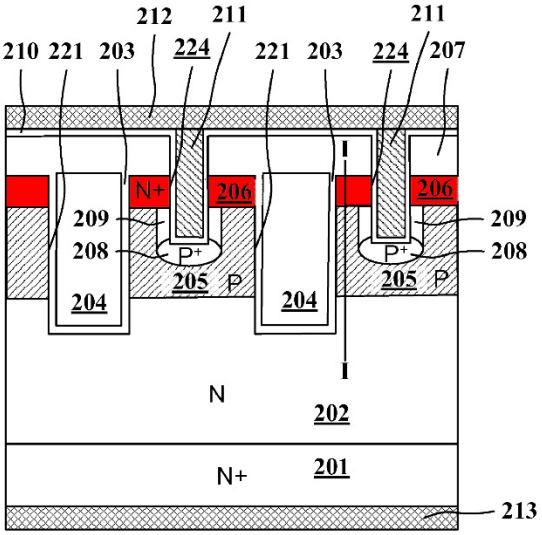
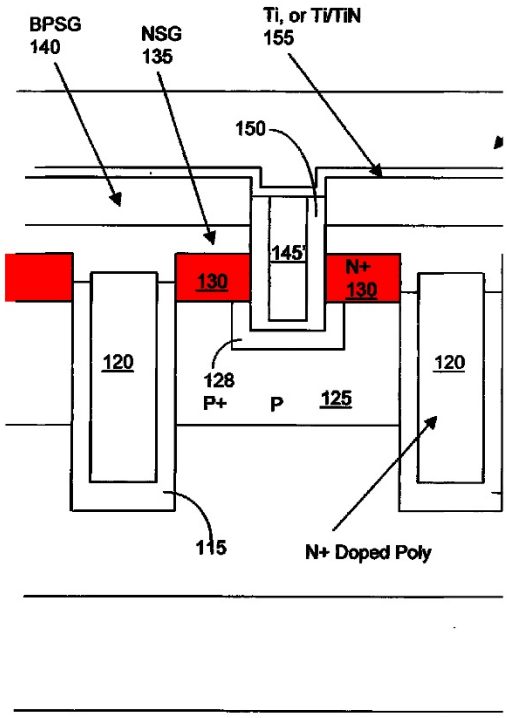
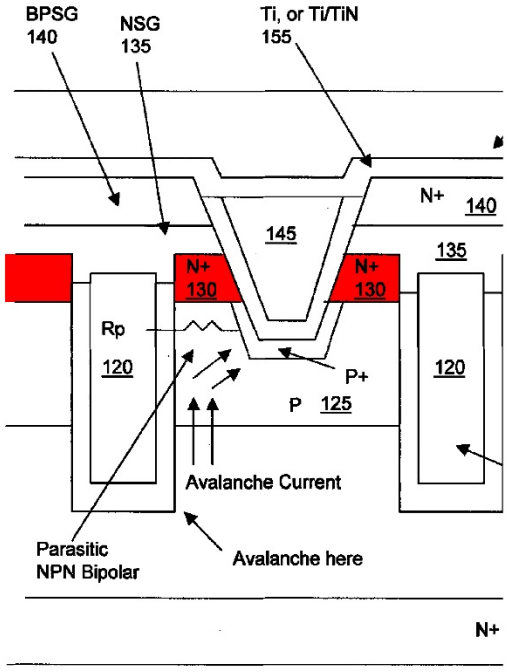
4) [1a-1-4]: "source region."

206. Hshieh ('384) teaches a source region, which I will refer to as *[1a-1-4]*–"source region," consistent with the structure and function of element 106/206 of the '634 Patent. The '634 Patent describes a heavily doped N^+ source region positioned above the P-type body region and forming part of the vertical conduction path of the MOSFET device; Hshieh ('384) provides an analogous source structure.

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[1a-1-4]

source region

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

207. In particular, Hshieh ('384) identifies "source region 30," specifically described as an N^+ source region, in connection with the vertical device architecture. (Ex. 1005, Hshieh ('384), ¶¶[0006]–[0007], [0013]–[0014]; Fig. 1, element 30.) In subsequent embodiments, Hshieh ('384) discloses "source regions 130" and "source regions 230," which are located above the respective body regions, and which function as the source terminals of the device. (*Id.* ¶¶[0026]-[0027]; *see also* ¶¶[0028]–[0030]; Figs. 3–8, element 130; ¶[0034]; Figs. 9D–J and 9G', element 230.) These source regions (element 30/130/230) are consistently positioned above the P-type body (element 25/125/225), and operate in the same manner as the source region(s) 106/206 described in the '634 Patent–which is to serve as the origin of conduction electrons during forward operation of the MOSFET.

208. Moreover, the presence of these source regions (element 30/130/230) is further confirmed by the claim language of Hshieh ('384), which recites the "source region" in at least claims 1, 16, and 20.

209. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a source region (element 30/130/230) corresponding to the source layer (element 30/130/230) recited in the '634 Patent. Therefore, Hshieh ('384) teaches limitation *[1a-1-4]*–"source region".

ii. [1a-2]: "a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"

210. This claim sub-element is taught by Hshieh ('384).

211. This is readily seen via an annotated excerpt from Fig. 3 of Hshieh ('384):

Ex. 1005 ('384 Hshieh)

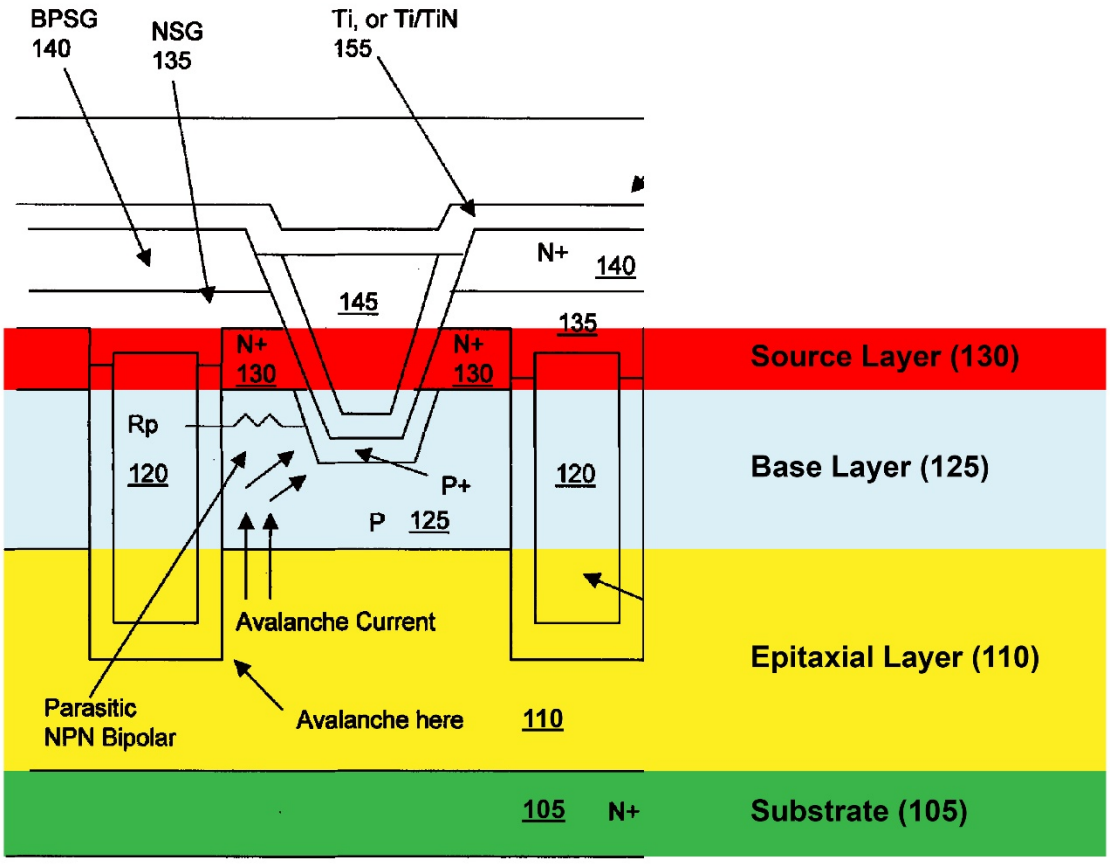


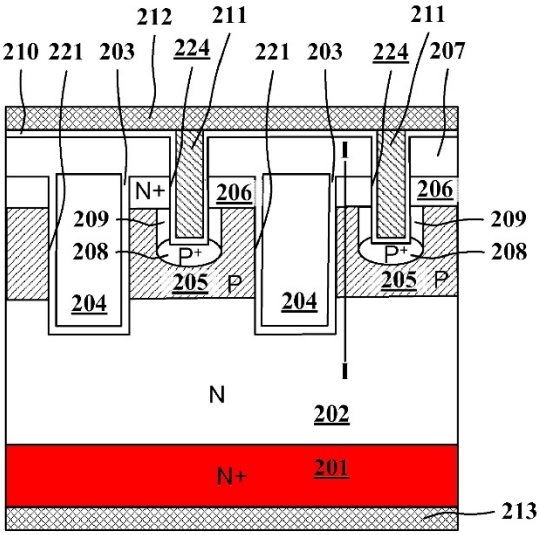
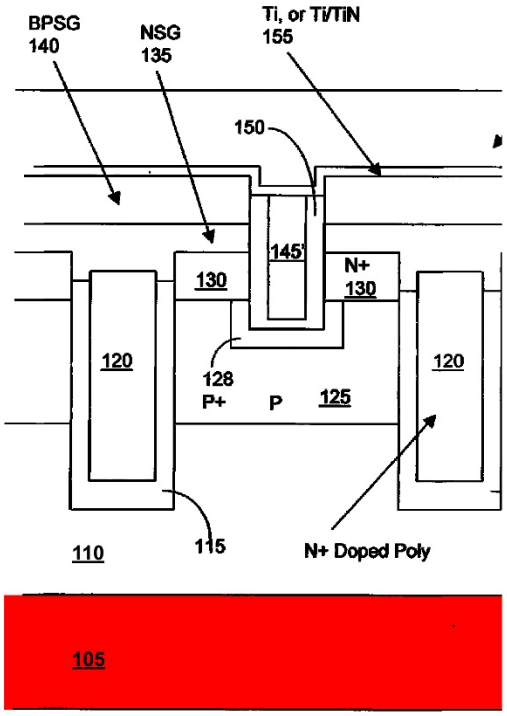
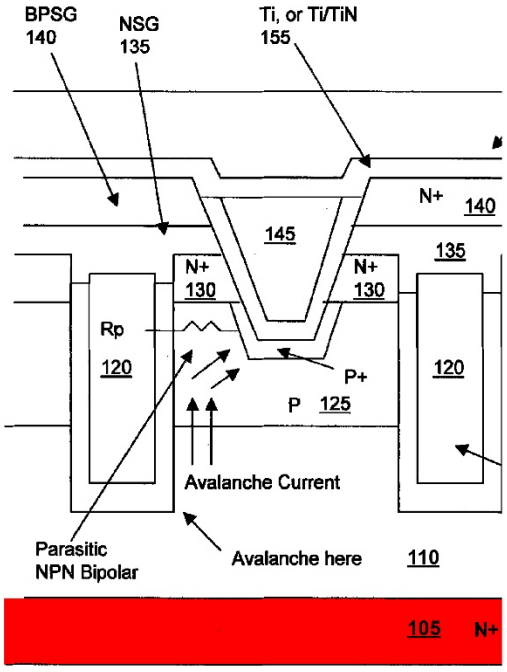
Fig. 3 (Annotated partial enlarged view)

212. Hshieh ('384) identifies 105 as being a "substrate," 110 as being an "epitaxial layer," 125 as being a "body region," and 130 as being a "source region" (Ex. 1005, Hshieh ('384), ¶[0026]); further, these layers are disposed in the layering-order specified in the claim sub-element. The body region 125 refers to the body region of individual MOSFET structures, whereas the broader and collective "base layer" recited in the claim sub-element includes the body regions that are discrete segments of the overall base layer. Similarly, the source region 130 denotes the source regions of specific MOSFET structures, while the broader and collective "source layer" recited in the claim sub-element includes source regions that are discrete segments of the overall source layer.

1) [1a-2-1]: "silicon substrate."

213. Hshieh ('384) teaches a semiconductor substrate corresponding to element 101/201 of the '634 Patent. Specifically, Hshieh ('384) states that "device 100 is supported on a N^+ substrate 105," thereby clearly identifying the foundational semiconductor substrate upon which the epitaxial layer is grown and upon which the device is constructed. (Ex. 1005, Hshieh ('384), ¶[0026]; Figs. 3–8, element 105.) In an alternative embodiment, the substrate is similarly described as "substrate 205," which likewise supports the semiconductor structure that will eventually be constructed above it. (*Id.* ¶[0034]; Figs. 9A–J and 9G', element 205; *see also* claims 1, 5, 11–14, 20, 24, and 27–30.)

[1a-2-1]
silicon substrate

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

214. As an initial matter, while Hshieh ('384) does not expressly identify the material composition of substrates 105 and 205 or explicitly restrict the material composition of that substrate to a single material, a person of ordinary skill in the art (POSITA) would have understood that, in practice, these substrates are composed of silicon. At the time of the invention, trench MOSFET devices of the type described in Hshieh ('384) were conventionally fabricated on silicon wafers. In the absence of any indication to the contrary, a person of ordinary skill in the art (POSITA) would have understood the term "semiconductor substrate"—particularly one described as N^+-doped, overlaid with an epitaxially grown N-type layer, and incorporating a MOSFET structure with a gate oxide surrounding the gate electrode—as referring, in practice, to a silicon substrate.

215. Hshieh ('384) specifically discusses the use of a "silicon etch" in the manufacture of the disclosed device. In the context of semiconductor fabrication, a silicon etch refers to a process that selectively removes silicon or silicon-based materials from a wafer surface in accordance with a patterned masking layer. This etching step is a fundamental and widely used manufacturing process that is employed to define critical device features such as transistor gates and trenches. The reference to a silicon etch confirms that the underlying semiconductor material being processed is, in fact, silicon—further supporting that Hshieh ('384) discloses a silicon-based MOSFET structure. In practice, a person of ordinary skill in the art

would have readily understood that the use of a "silicon etch" necessarily implies a silicon wafer.

216. This conclusion is further supported by the structural context of the disclosure. A doped N^+ substrate with an N-type epitaxial layer grown on top, as shown in Hshieh ('384) (*See* e.g. Ex. 1005, Hshieh ('384), Figs. 3–8; Figs. 9A–J and 9G'), has long been known as a commonly-used approach in MOS transistor manufacturing. (*See* Ex. 1015, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 1, 124 (1986); Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era* Vol. 2, 385-387 (1990); *in particular*, *Id.* at 386 "Either n-epi on n+ substrates or p-epi on p+ substrates can be used.") This includes its use in trenched-gate MOS transistors–as evidenced by its use in the Texas Instruments 4Mb DRAM that was discussed in Section VII.C (using a doped P+ substrate and a P-type epitaxial layer grown on top–which is what is described in both Hshieh ('384) and the '634 Patent, but with the doping polarities reversed).

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Ex. 1016, Ashwin H. Shah et al., *A 4-Mbit DRAM with Trench-Transistor Cell*, IEEE Journal of Solid-State Circuits, vol. 21, 619 Fig. 1 (1986)

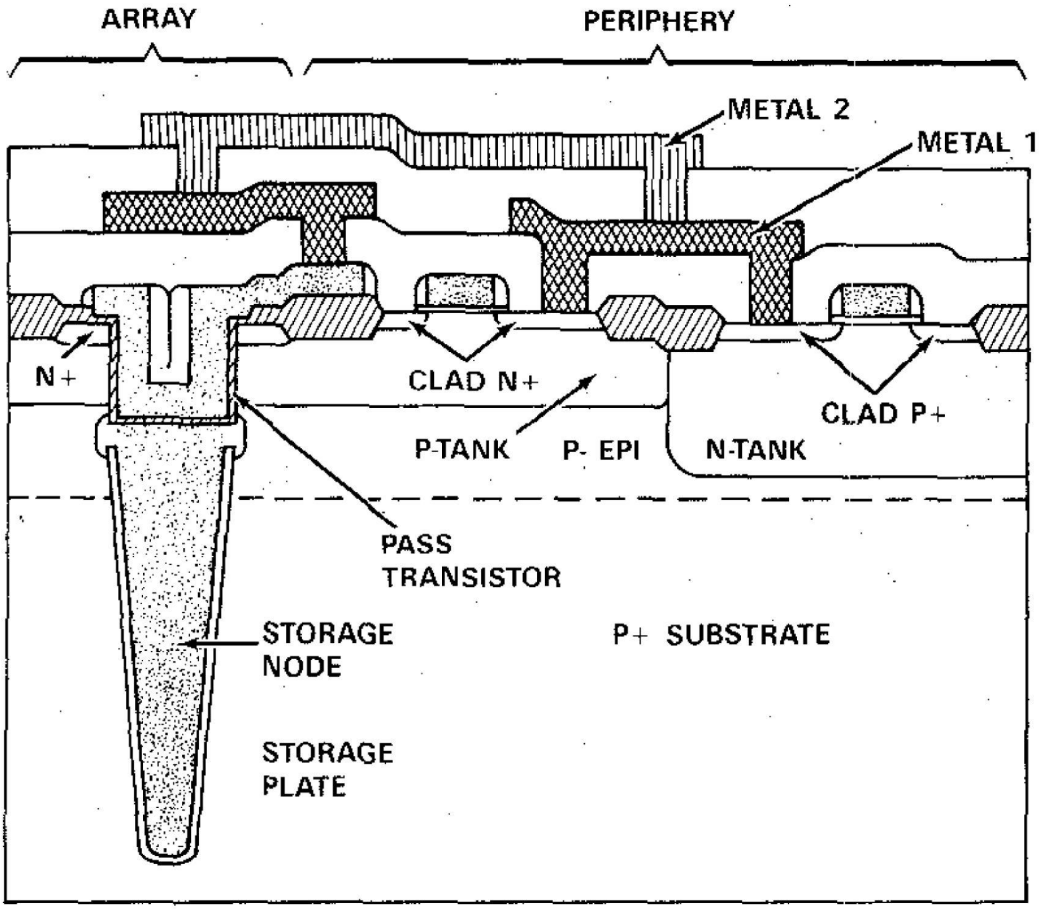


Fig. 1. Typical cross section of process topography.

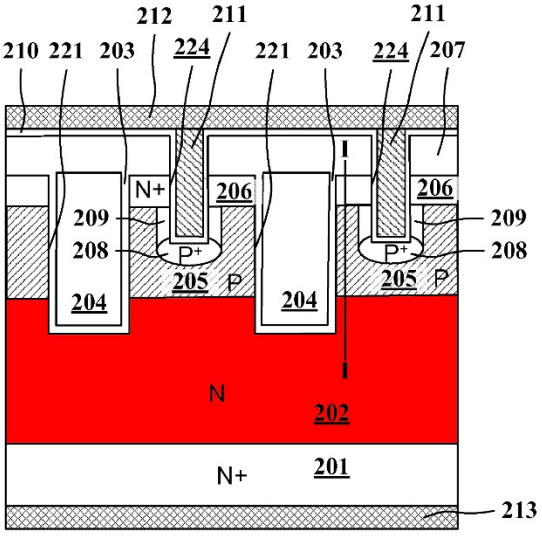
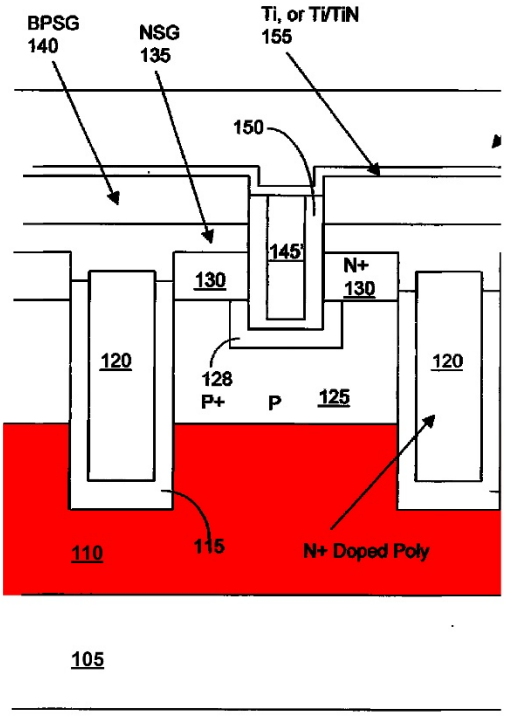
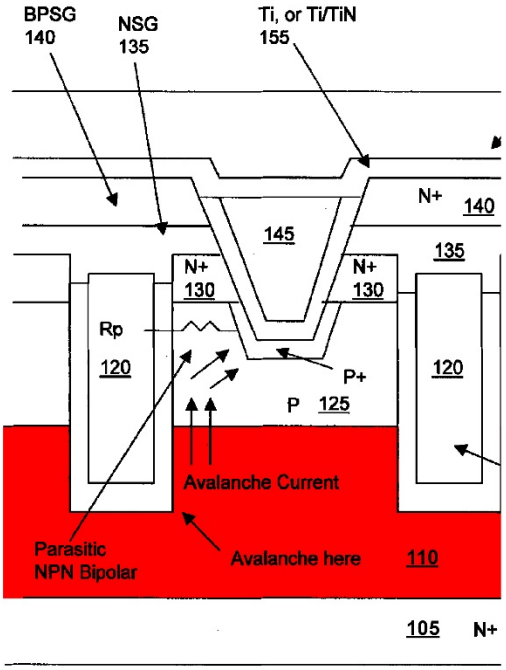
217. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a silicon substrate (element 15/105/205) that serves as the foundation for the semiconductor device–which is consistent with the "silicon substrate" recited in the '634 Patent. Therefore, Hshieh ('384) teaches limitation *[1a-2-1]*–"silicon substrate".

2) [1a-2-2]: "epitaxial layer."

218. Hshieh ('384) describes an epitaxial layer, which I will refer to as limitation *[1a-2-2]*–"epitaxial layer", consistent with element 102/202 of the '634 Patent. The '634 Patent recites an epitaxial layer formed on a semiconductor substrate and functioning as part of the drain region; Hshieh ('384) provides a materially-identical structure.

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[1a-2-2]
epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

219. Specifically, Hshieh (’384) initially identifies “an epitaxial layer 20” as part of the semiconductor structure in its background discussion. (Ex. 1005, Hshieh (’384), ¶[0006]; Fig. 1, element 20.) In a preferred embodiment, Hshieh (’384) discloses “an N^+ substrate 105 formed with an N epitaxial layer 110,” where the epitaxial layer 110 is disposed directly above the substrate and serves as the lower portion of the vertically-layered semiconductor region. (*Id.* ¶[0026]; *see also* ¶¶[0028]–[0031]; Figs. 3–8, element 110.)

220. In an alternative embodiment, Hshieh (’384) discloses “an epitaxial layer 210 supported on a substrate 205,” preserving the same relative arrangement and functional role between the epitaxial layer and the underlying substrate. (*Id.* ¶[0034]; Figs. 9A–J and 9G’, element 210.) In both embodiments, the epitaxial layer functions as part of the vertical drain-region current path–just as in the ’634 Patent.

221. Accordingly, it is my conclusion and opinion that Hshieh (’384) discloses an epitaxial layer (element 20/110/210) positioned above the semiconductor substrate (element 15/105/205) and forming part of the drain region, consistent with the structure recited in the ’634 Patent. These disclosures teach limitation *[1a-2-2]*–“epitaxial layer”.

3) [1a-2-3]: "base layer"

222. Hshieh ('384) teaches a "base layer" that will eventually be segmented into body regions (when the trenches are etched into the silicon)– consistent with element 105/205 of the '634 Patent. Therefore a POSITA would recognize that the layers correspond to the final regions as annotated in the figure below.

Ex. 1005 ('384 Hshieh)

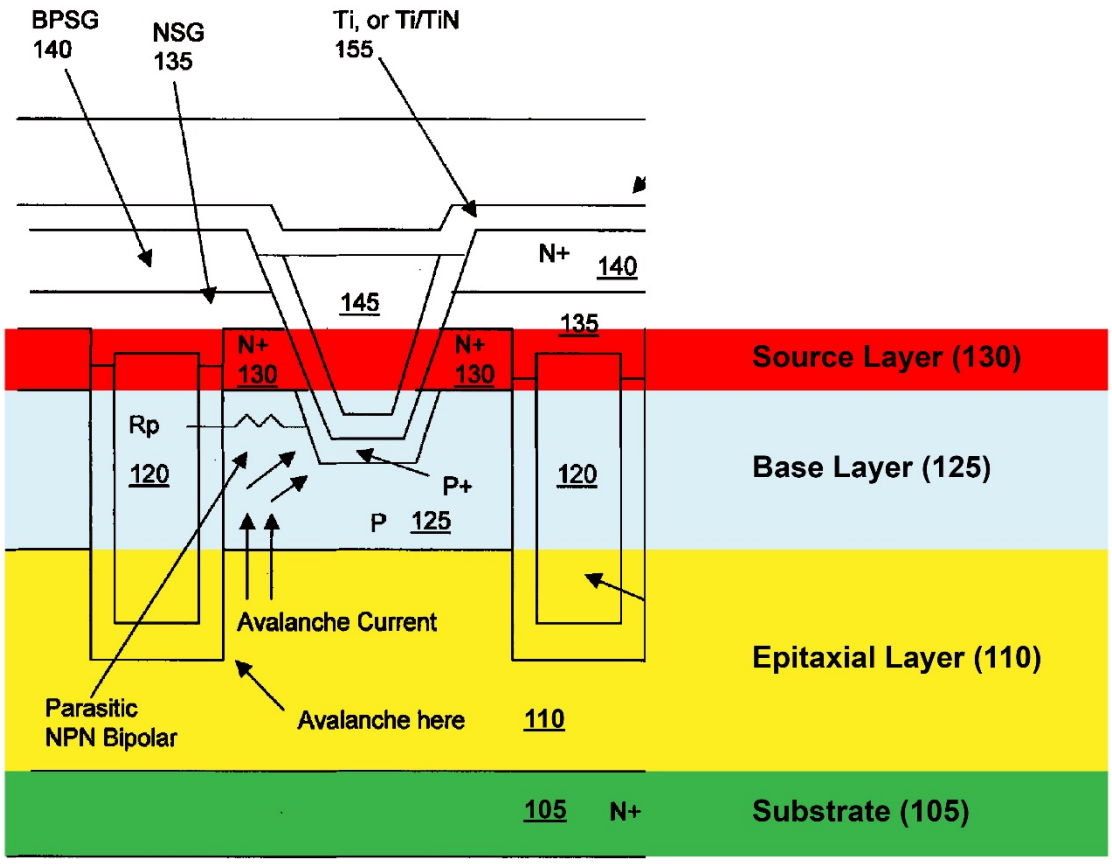
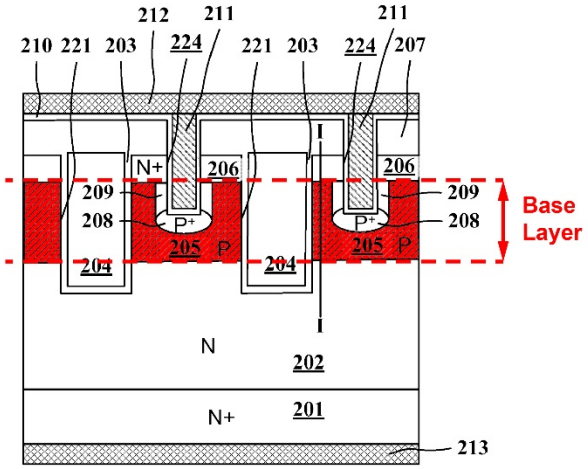
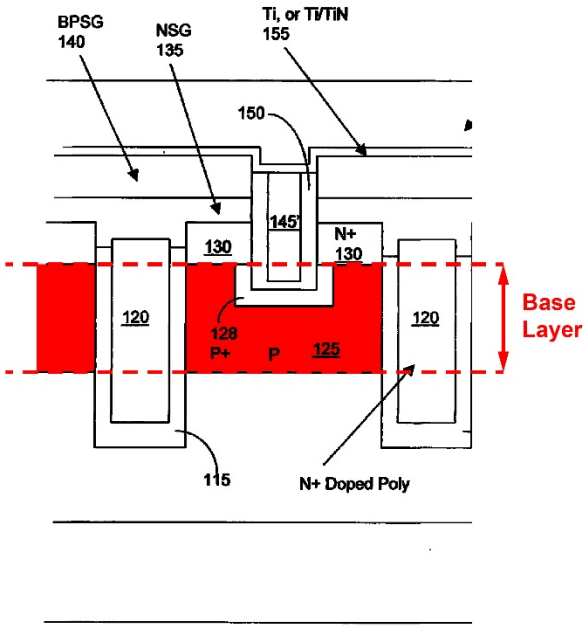
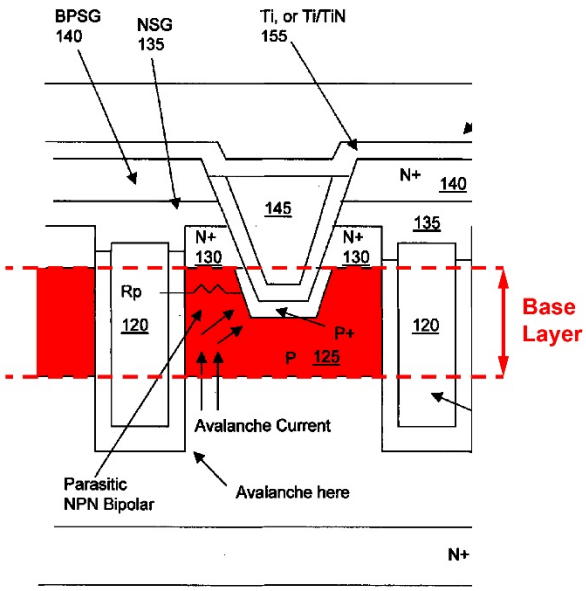


Fig. 3 (Annotated partial enlarged view)

223. For the purposes of discussing the base layer, the body regions depicted in the figures of both Hshieh (’384) and the ’634 Patent delineate the boundaries of the base layer as it exists after processing. The ’634 Patent describes a 105/205 P-type body region disposed above the 102/202 epitaxial layer and beneath the 106/206 source region, serving as a key element of the transistor’s vertical structure. Hshieh (’384) discloses an identical structural configuration, with a body region (element 25/125/225) positioned in the same vertical sequence and performing the same function within the MOSFET architecture.

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[1a-2-3]
base layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

224. As previously mentioned, the post-processing regions define the boundaries of what the ’634 Patent defines as “layers”; these “layers” never physical exist in the structures described in the ’634 Patent–but rather define a larger-scale horizontal region (as shown above) in which the identified “regions” reside (e.g., the “body regions” reside in the larger-scale “base layer”). Accordingly, analysis of the regions depicted in both Hshieh (’384) and the ’634 Patent helps to inform our understanding of how the ’634 Patent defines and characterizes its claimed layers. Specifically, Hshieh (’384) discloses “A body region 125 that is doped with a dopant of second conductivity type, e.g., P-type dopant, extends between the trenched gates 120.” (Ex. 1005, Hshieh (’384), ¶¶[0026]; *see also* [0027]–[0031]; Figs. 3–8, element 125.) As illustrated in Figures 1, 3–8, 9C-J and 9G’ of Hshieh (’384), the body region 25 and its alternative embodiments 125 or 225 is disposed beneath the source region 30/130/230 and above the N-type epitaxial layer 20/110/210, consistent with the vertical layer arrangement recited in the ’634 Patent.

225. Further, in an alternative embodiment, Hshieh (’384) discloses “a P-body region 225” disposed over epitaxial layer 210, which likewise reflects the same relative positioning and function. (*Id.* ¶[0034]; Figs. 9C–J and 9G’, elements 210 and 225.) In both cases, note that the body regions (element 25/125/225) are subdivisions of the overall “base layer.”

226. My conclusion is further supported by the Patent Owner's admitted prior art, as illustrated in Fig. 1 (Prior Art) of the '634 Patent, which shows that the base regions are formed within the base layer. Specifically, the '634 Patent states that "the P-type base layer (205) are [sic] corresponding to the body region of the trenched MOSFET." (Ex. 1001, '634 Patent, 5:1–2.) Moreover, the relative position of the body region (element 25/125/225) in Hshieh ('384)—located beneath the source layer (element 30/130/230) and above the epitaxial layer (element 20/110/210) and silicon substrate (element 15/105/205)—is consistent with the '634 Patent's structural disclosure that "[t]he N^+-type silicon substrate (101), the N-type epitaxial layer (102), the P-type base layer (105), and the N^+-type source layer (106) are stacked in sequence." (Ex. 1001, '634 Patent, 1:29–32.)

227. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a P-type body region (element 25/125/225) disposed above the epitaxial layer (element 20/110/210) and beneath the source region (element 30/130/230), thereby corresponding to the base layer as recited in the '634 Patent–and that this would be obvious to a POSITA examining Hshieh ('384). These disclosures therefore teach *[1a-2]*.

4) [1a-2-4]: "source layer"

228. Hshieh ('384) teaches a source layer consistent with element 106/206 of the '634 Patent. The '634 Patent recites "a source layer corresponding to said

source region disposed on the top of said base layer," and while Hshieh ('384) does not explicitly label a layer as the "source layer," it nevertheless provides a structure functionally and spatially consistent with that requirement.

229. As with the "base layer" discussed above, the "source layer" in Hshieh ('384) will ultimately be segmented into discrete source regions as the trenches are etched into the silicon. Therefore, for the purposes of discussing the source layer, the source regions depicted in the figures of both Hshieh ('384) and the '634 Patent delineate the boundaries of the source layer as it exists after processing. Specifically, Hshieh ('384) discloses "a source region 30" situated above a portion of the body region (element 25/125/225), consistent with the structure described in the '634 Patent. (Ex. 1005, Hshieh ('384), ¶[0006]; *see also* ¶¶[0013]–[0014]; Fig. 1, element 30.) Therefore, a person of ordinary skill in the art (POSITA) examining the figures of Hshieh ('384)—for example, Figures 3 or 4—would recognize the region annotated in the following figure as corresponding to the "source layer," since it encompasses, as a subset, the source regions (element 30/130/230) that serve as the origin of conduction for individual trenched MOSFET transistors.

Ex. 1005 ('384 Hshieh)

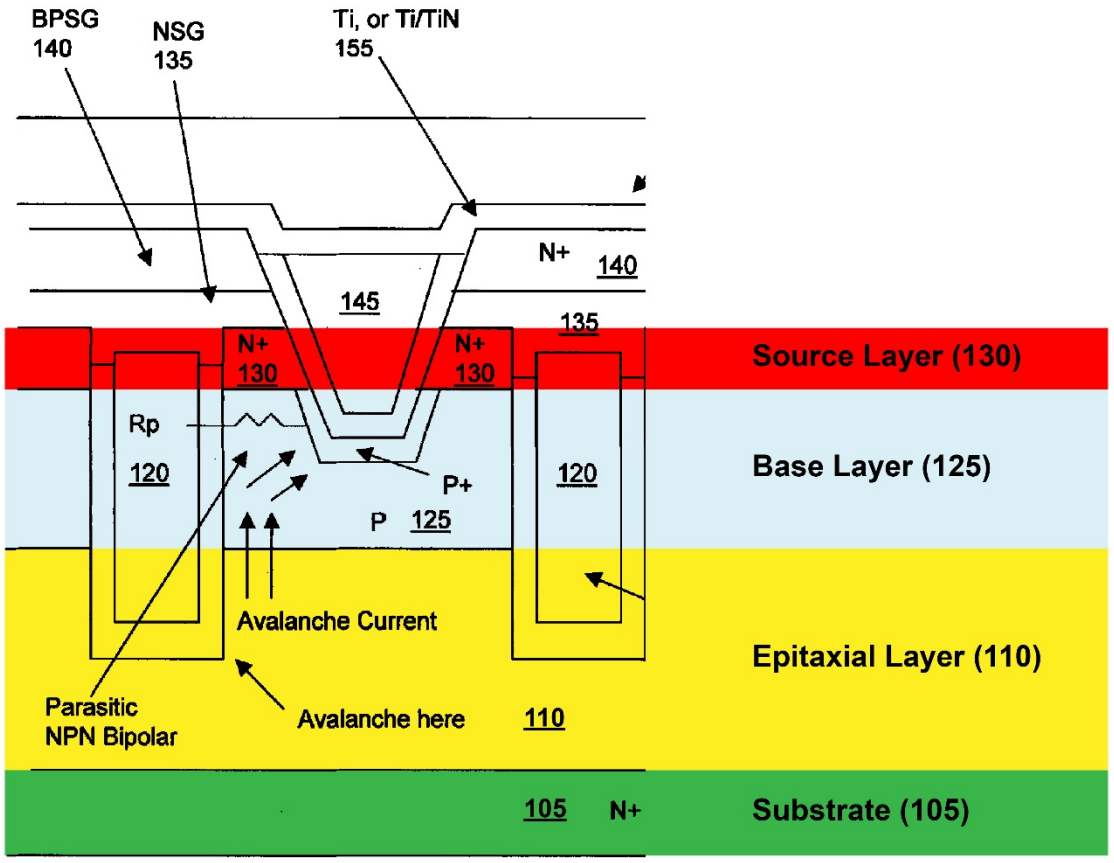


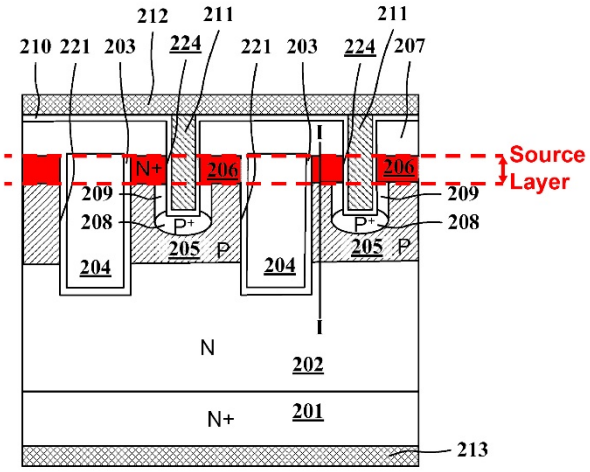
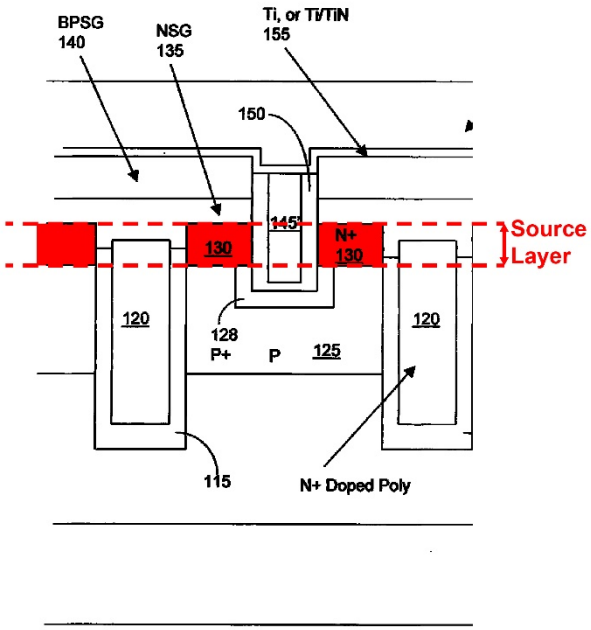
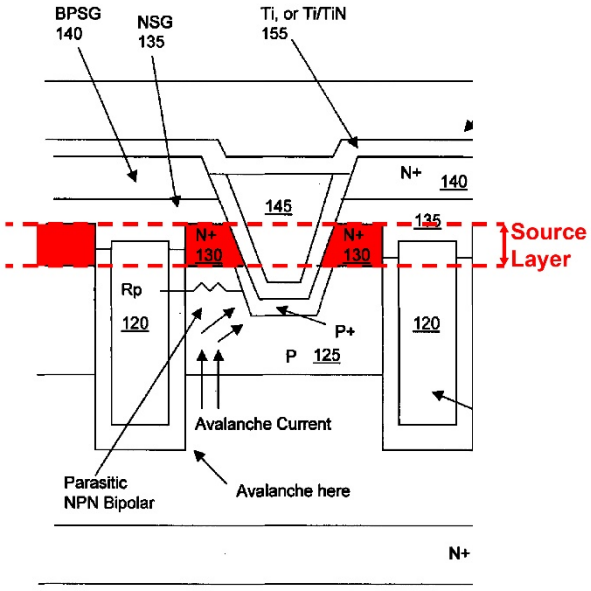
Fig. 3 (Annotated partial enlarged view)

230. In a preferred embodiment, Hshieh ('384) further states that "a source region 130 doped with…"—referring to a heavily doped N-type region that serves as the source. (*Id.* ¶[0026]; *see also* ¶¶[0027]–[0030]; Figs. 3–8, element 130.) This source region (element 30/130/230) is located in the upper portion of the vertical structure–positioned above the epitaxial layer (element 20/110/210) and base layer (element 25/125/225), and adjacent to the trench gates–in a manner consistent with the claimed source layer.

231. Additional embodiments disclose a similar configuration in which element 230 serves as the source region located above a portion of the body region 225 and above epitaxial layer 210. (*Id.* ¶[0034]; Figs. 9D–J and 9G', element 230.)

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[1a-2-4]
source layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

232. My conclusion is further supported by the Patent Owner's admitted prior art, as illustrated in Fig. 1 (Prior Art) of the '634 Patent, which shows that the source regions are formed within the source layer. Specifically, the '634 Patent states that "the N^+-type source layer (206) [is] corresponding to the source region of the trenched MOSFET." (Ex. 1001, '634 Patent, 4:66–5:1.) Moreover, the relative position of the source region (element 30/130/230) in Hshieh ('384)—situated above the base layer (element 25/125/225), epitaxial layer (element 20/110/210), and silicon substrate (element 15/105/205)—is consistent with the '634 Patent's structural disclosure that "[t]he N^+-type silicon substrate (101), the N-type epitaxial layer (102), the P-type base layer (105), and the N^+-type source layer (106) are stacked in sequence." (*Id.* at 1:29–32.)

233. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a source layer (element 30/130/230) in a manner consistent with the "source layer" recited in the '634 Patent–and that this would be obvious to a POSITA examining Hshieh ('384). Thus, these disclosures in Hshieh ('384) teach limitation *[1a-2]*.

c. [1b]: "a front metal layer formed on the upper surface of said semiconductor region;"

234. This claim element is taught by Hshieh ('384).

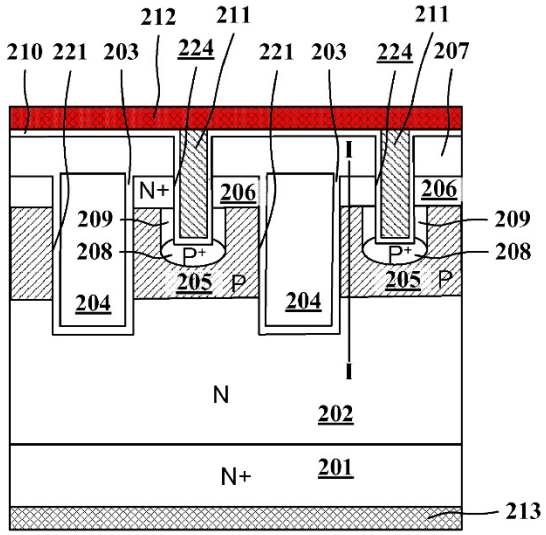
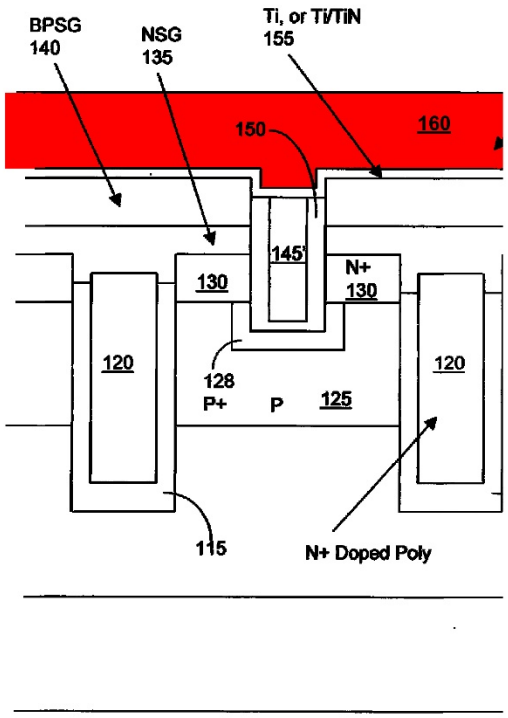
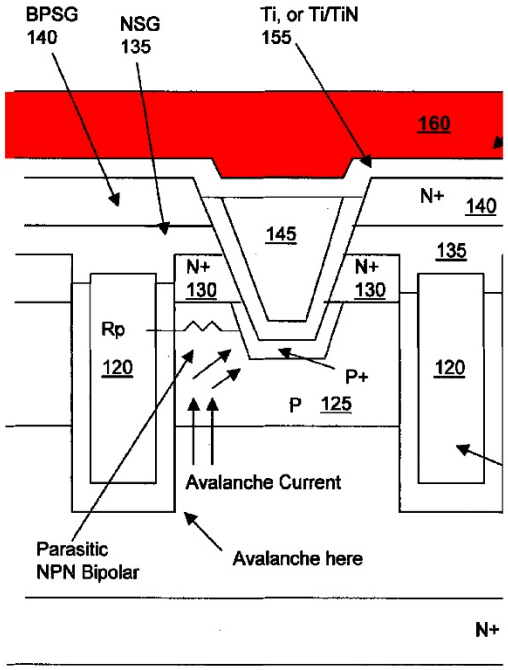
235. Hshieh (’384) teaches a front-side metallization structure corresponding to the “front metal layer” 112/212 recited in the ’634 Patent, which I will identify as *[1b]*–“front metal layer”. Specifically, Hshieh (’384) identifies element 160 as a “top contact layer.” (Ex. 1005, Hshieh (’384), ¶[0027], Figs. 3-8, element 160.)

236. The top contact layer in Hshieh (’384) is “formed on the upper surface of said semiconductor region” as required by the ’634 Patent and is clearly located on the front side of the device structure, corresponding to the “front metal layer” recited in the ’634 Patent claim element. (Ex. 1001, ’634 Patent, claim 1.)

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[1b]

front metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

237. Hshieh ('384) further describes the properties and composition of this top contact layer as follows:

> The top contact layer 160 is formed with aluminum, aluminum-cooper *[sic]*, AlCuSi, or Ni/Ag, Al/NiAu, AlCu/NiAu or AlCuSi/NiAu as a wire-bonding layer. (Ex. 1005, Hshieh ('384), ¶[0027].)

238. The metals and metal alloys described in the excerpt above were, by the time of the '634 Patent (i.e. 2008), well known in the art as interconnect materials—commonly used to provide electrical connections between transistors and other components in integrated circuits. In fact, these are some of the same metals identified in the '634 Patent for use in the front metal layer. The '634 Patent expressly states: "The front metal layer (212) is preferably as thick as possible in order to reduce the resistance component of AlSi or AlSiCu." (Ex. 1001, '634 Patent, 4:31-33.) This further confirms that the materials disclosed by Hshieh ('384) for its top contact layer (element 60/160) are consistent with those contemplated in the '634 Patent for the claimed front metal layer; in fact, these are some of the same metallic materials (here, metallic alloys) that are identified in the '634 Patent as being suitable for use as the front metal layer. (Ex. 1005, ¶[0006], Fig. 1, element 60; ¶[0027], Figs. 3-8, element 160.) (Note that AlSi and AlSiCu are alloys of aluminum that are commonly-used in metal interconnect layers–with small concentrations of silicon or silicon-and-copper added to the aluminum; this alloying technique has long been used in silicon process

engineering–in order to make the aluminum lines more resistant to electromigration, and to mitigate some topographic problems. (*See* Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 191 (1990).)

239. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a front-side metal structure that performs the same function and occupies the same position as the front metal layer recited in the '634 Patent. These disclosures teach limitation *[1b]*–"front metal layer".

d. [1c]: "an interlayer oxide film formed between said source layer and said front metal layer,"

240. This claim element is taught by Hshieh ('384).

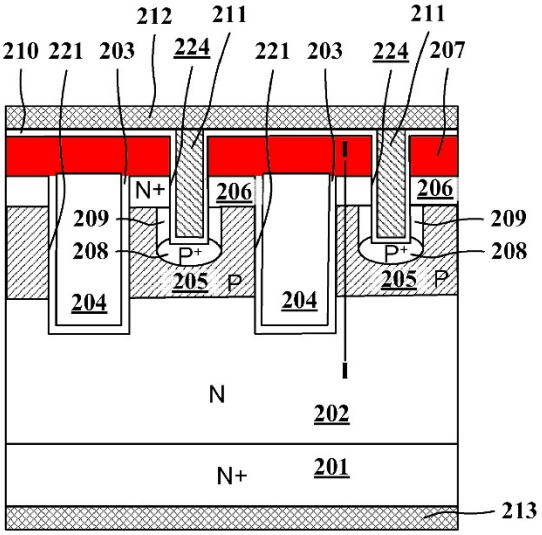
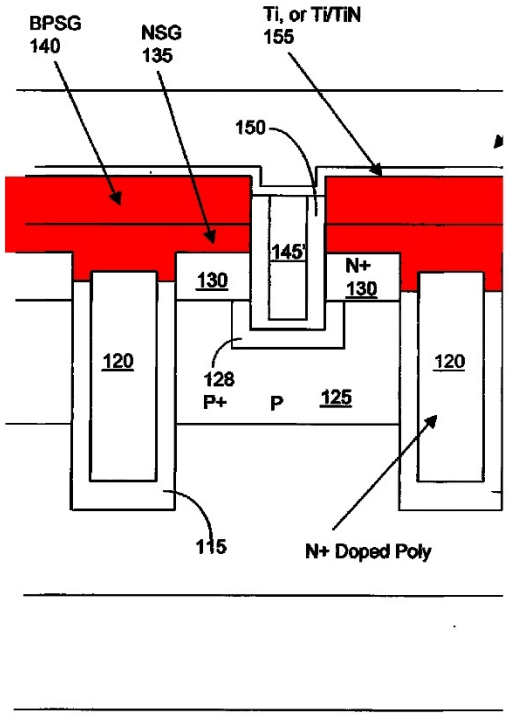
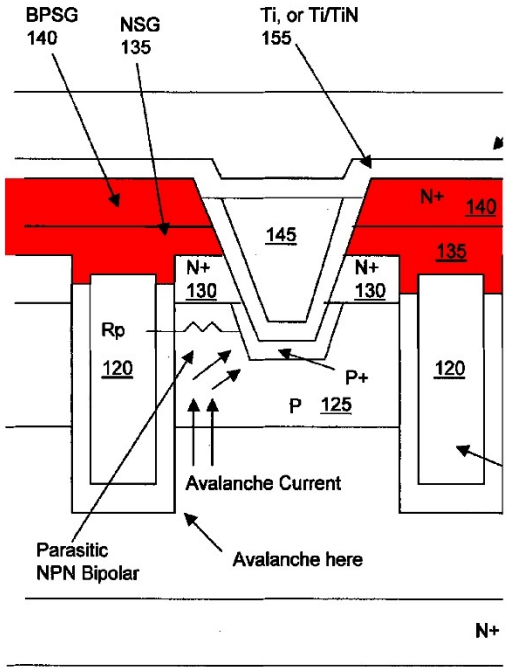
241. Hshieh ('384) teaches an interlayer oxide film corresponding to element 107/207 of the '634 Patent. The '634 Patent recites an insulating oxide layer positioned between the source region and the front metal layer. Hshieh ('384) likewise teaches functionally and structurally equivalent oxide-based dielectric films in multiple embodiments. For example, Hshieh ('384) describes that contact trenches are formed "through the NSG and BPSG protective layers 135 and 140 to contact…" underlying device structures, confirming the presence of insulating layers situated above the active semiconductor regions. (Ex. 1005, Hshieh ('384), ¶[0027]; Figs. 3–8, elements 135 and 140.) In an alternative embodiment, the patent discloses that "a non-doped oxide (NSG) layer 235 and a BPSG layer 240

are deposited on the top surface," again confirming the deposition of insulating oxide films above the semiconductor body and source regions. (*Id.* ¶[0034]; Figs. 9E–9G', elements 235 and 240.) For completeness, "BPSG" is a well-known acronym for "borophosphosilicate glass"–a well-known doped insulating material that is deposited for use as an insulating dielectric material. (*See* Ex. 1015, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 1, 187-191 (1986).)

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[1c]

interlayer oxide film

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

242. Although Hshieh ('384) does not explicitly define the acronyms in the specification, Fig. 3 labels layer 135 as "NSG" and layer 140 as "BPSG"; as explained earlier, these terms have long been known in the semiconductor fabrication art: "NSG" stands for non-doped silicate glass, and "BPSG" stands for borophosphosilicate glass (as just noted above); both are widely used oxide-based insulating dielectric materials. As the term "glass" suggests, they are composed of silicon dioxide (SiO_2) and can serve as (and are therefore used as) interlayer dielectrics. It has long been common practice in the art to use such materials to electrically isolate conductive regions in integrated circuit structures. "Two dielectric workhorses in device fabrication are the silicon dioxide (SiO2) and the silicon nitride (Si3N4). Aside from being used for masking purposes, the former is extensively used in electrical isolation." (*See* Ex. 1017, *Properties of SiO_2 and Si_3N_4 at 300K*, Comprehensive Reference on EESEMI Semiconductor Manufacturing, https://eesemi.com/sio2si3n4.htm (last visited July 31, 2025)). A POSITA would have readily recognized these materials as standard insulating oxides at the time of filing of the '634 Patent, and would have understood that Hshieh ('384) teaches interlayer dielectric films (element 45-1/135/235 and 45-2/140/240) positioned between the source region (element 30/130/230) and the front metal layer (element 60/160).

243. Further, the use of one or more oxide films would represent a routine design choice for a person of ordinary skill in the art (POSITA) when implementing an interlayer oxide film. Regardless of the specific oxide materials selected, such a choice would yield the same functional result as the interlayer oxide film disclosed in the ’634 Patent. The admitted prior art depicted in Fig. 1 (Prior Art) of the ’634 Patent further confirms that a POSITA would have been motivated to implement the same. Accordingly, these disclosures teach limitation *[1c]–interlayer oxide film*–of the ’634 Patent.

e. [1d]: “a bottom metal layer formed on the lower surface of said semiconductor region;”

244. This claim element is rendered obvious by Hshieh (’384) and the knowledge of a POSITA.

245. Hshieh (’384) identifies the drain region as being below the body region, with the drain region extending to the bottom surface of the substrate; e.g.,

> [A] body region above a drain region disposed on a bottom surface of a substrate. (Ex. 1005, Hshieh (’384), Abstract; ¶¶[0013]-[0014]; Claim 1.)

This readily allows for the identification of the drain portion of Hshieh (’384)’s trench-gate MOSFET structure–such as in Fig. 3:

Ex. 1005 ('384 Hshieh)

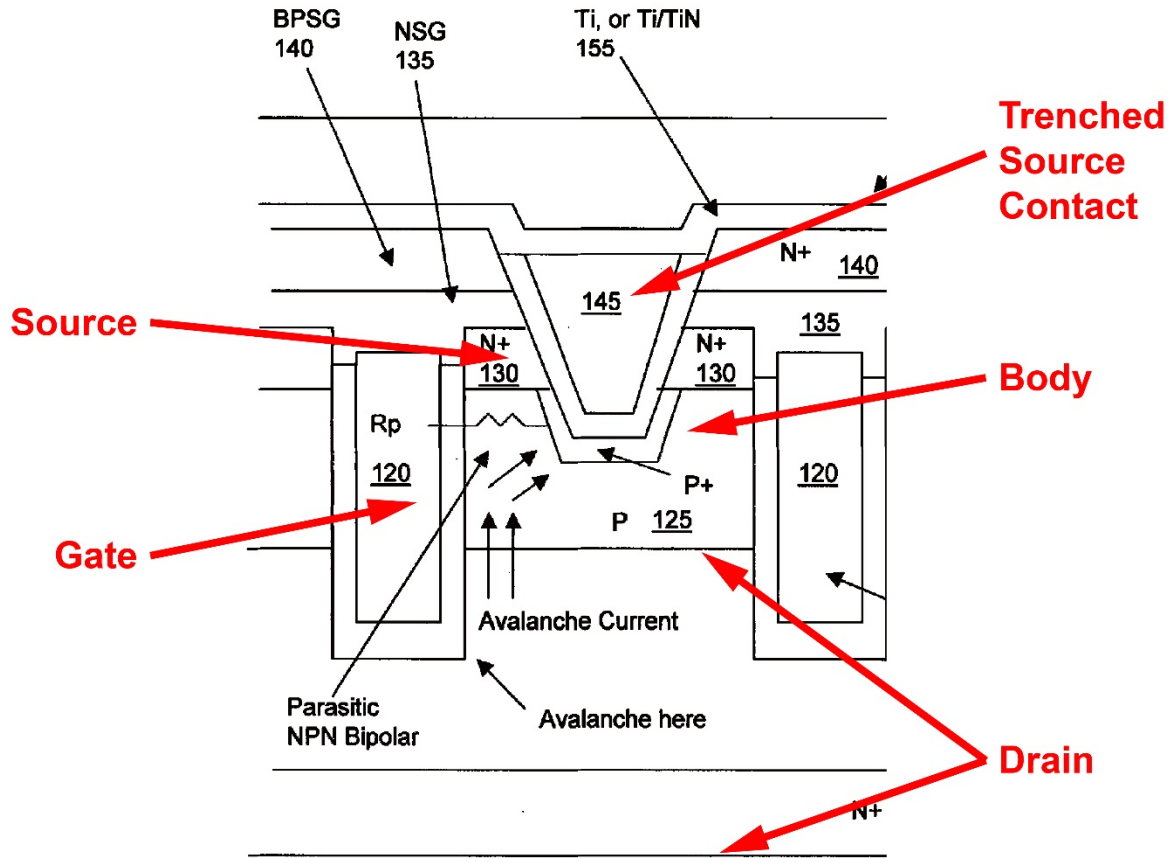


Fig. 3 (Annotated partial enlarged view)

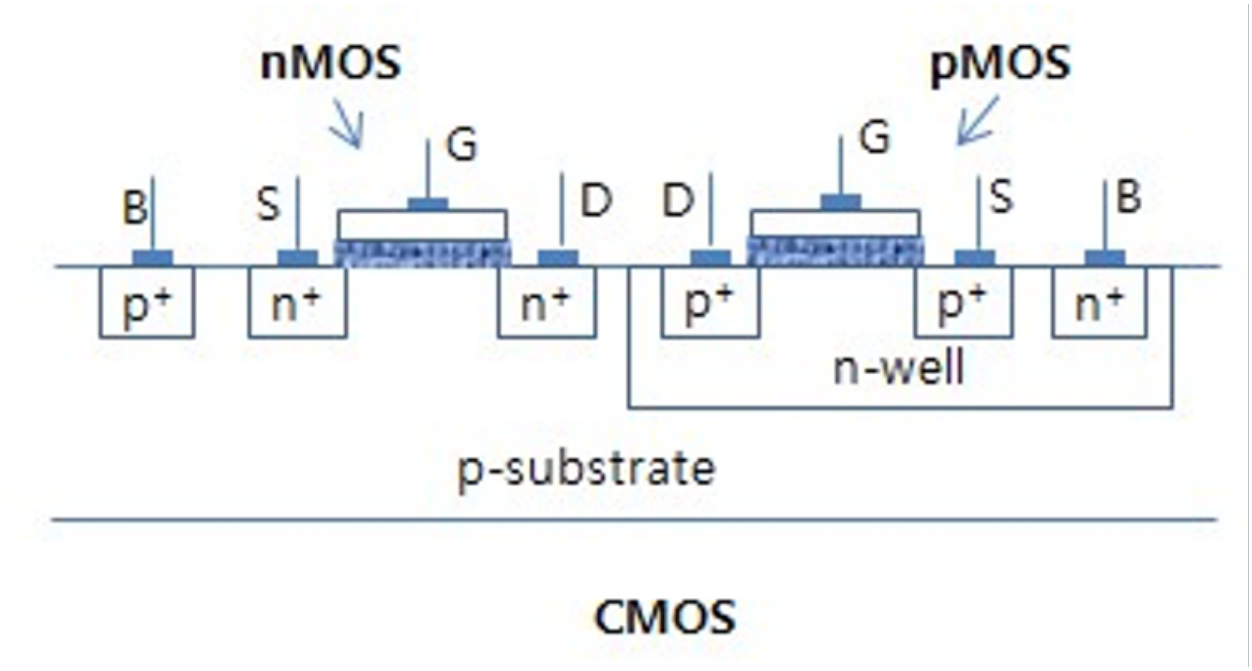
246. Further, Hshieh ('384) associates the drain of his MOSFET device structure with the N+ layer (element 15/105/205)–and also provides an explanation of how this N+ layer improves the performance of that MOSFET device:

> Furthermore, the drain to source resistance is reduced because the buried N+ region 118. The reduced Rds further reduces the spreading resistance between the drain and the channel region. (Ex. 1005, Hshieh ('384), ¶[0031].)

> The drain to source resistance and the spreading resistance between the drain and the channel regions are also reduced. (Ex. 1005, Hshieh ('384), ¶[0032].)

247. All of this is straightforward, and has long been a key part of MOS transistor fabrication and operation–the heavily-doped N+ layer (element 15/105/205) has higher electrical conductivity than does the lower-doped N-epi region (element 20/110/210), and this higher electrical conductivity serves to reduce the resistance along the MOSFET current-conduction-pathway (along the line of source-body-drain); if the resistance along this line is lower, then a larger current will flow for the same applied (drain-to-source) voltage–which increases the performance (i.e., drain output current) of that MOS transistor.

248. In addition, it has also long been common practice to provide a heavily-doped region (either N+ or P+, as appropriate) in the silicon to which the contact metallization is applied (i.e., the source, drain, and body contacts, which serve to connect the transistor with the rest of the circuitry). (*See* illustrative image below.)



249. This is done to provide a low-resistance ohmic contact to a MOSFET's body region–as otherwise (such as when a metallic contact is formed in contact with a more-lightly-doped region of silicon) the contact will be ohmic but with a resistance level that is electrically-significant (i.e., too high), or (much worse) the contact that is created is non-ohmic (e.g., a Schottky diode contact is produced).

250. Thus, it is apparent—and would have been readily understood by a person of ordinary skill in the art (POSITA)—that a drain contact is required in Hshieh ('384)'s structure to enable connection to the drain electrode. Given the architecture disclosed, this contact must be formed by establishing a metallic connection to Hshieh's N^+ substrate layer (element 15/105/205). While Hshieh ('384) does not explicitly depict a drain electrode contact in the figures, a POSITA,

applying their existing knowledge, would have readily understood how to implement this necessary (though unspecified) contact. This conclusion is reinforced by Hshieh ('384)'s own discussion of the importance of minimizing series resistance in the conduction path of the MOSFET device, which inherently requires a low-resistance drain contact.

251. A POSITA would be well-aware that the simplest approach would be to form the metal contact electrode on the bottom of Hshieh ('384)'s structure:

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Ex. 1005 ('384 Hshieh)

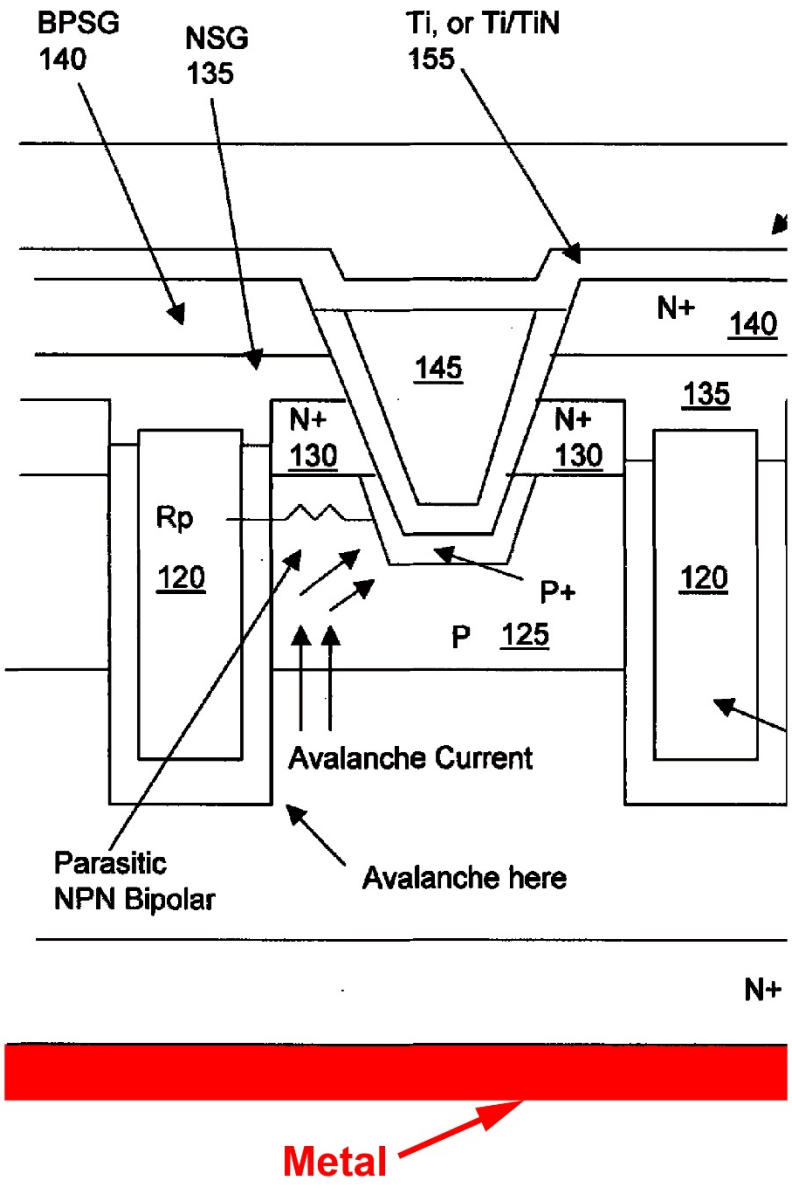


Fig. 3 (Annotated partial enlarged view)

This would be the most-obvious solution–as it would provide the required low-resistance ohmic contact to the N+ layer (element 15/105/205), and would do so in line with everything else that Hshieh (’384) is teaching (as described above).

252. Further, the use of a back-side metallic contact in this way has long been well-known in the semiconductor device art. For example, *see* Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 Fig. 11.8 (1967), depicts MOS transistors with a metal contact on the back side of the substrate:

Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 Fig. 11.8 (1967)

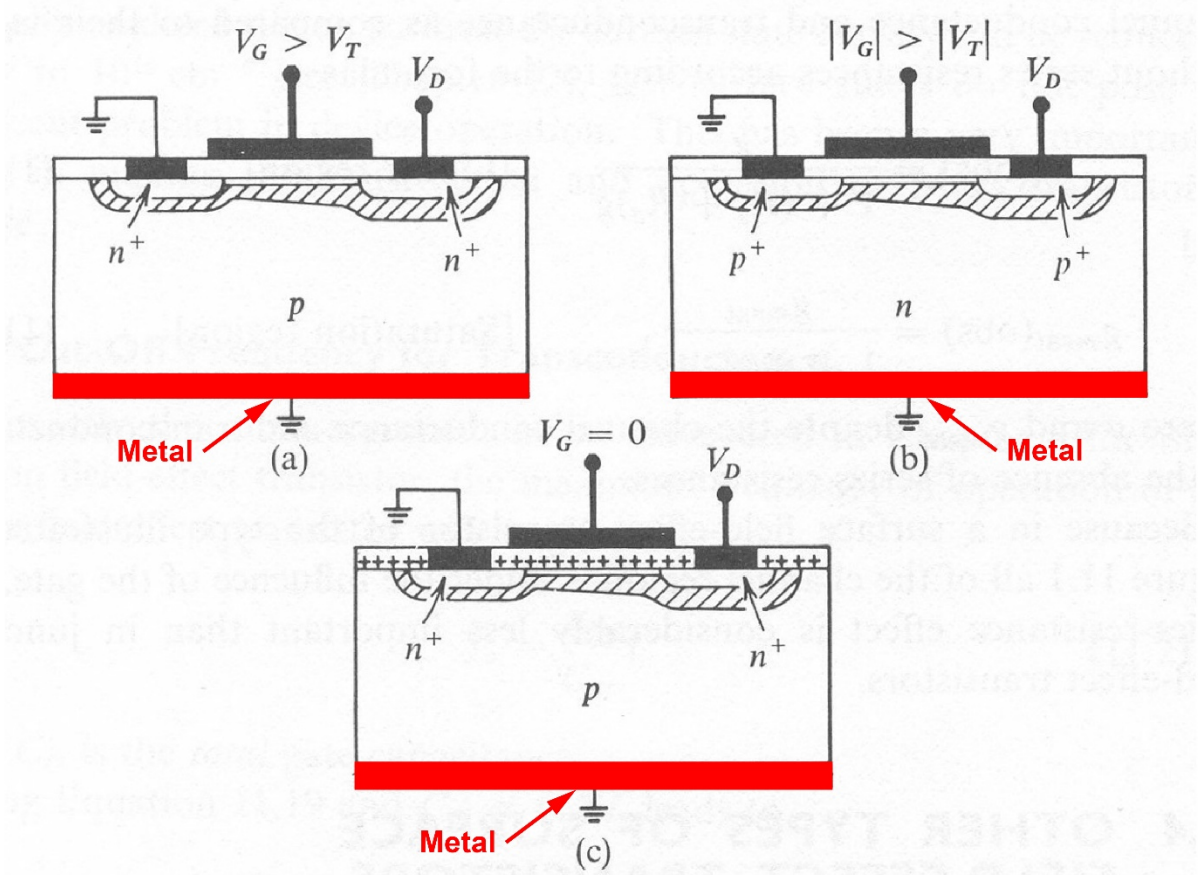


Fig. 11.8 Surface field-effect transistors with field-induced channels.
(a) Normally "off" *n*-channel device.
(b) Normally "off" *p*-channel device.
(c) Normally "on" *n*-channel device.

Fig. 11.8 (Annotated)

Note that all of the jet-black shapes in the figure above also represent metal–as the source contact, the drain contact, and the (at the time) gate electrode (which, being composed of metal itself, does not require a specific metal contact of its own–and, of course, this metal gate electrode does not contact silicon but rather contacts the insulating material of the gate dielectric).

253. Thus, a POSITA would have been aware of this type of contact–and further, given that this was well-known in the art by at least as early as 1967, a POSITA would have had a reasonable expectation of success in deploying such a well-known technology into Hshieh ('384)'s structure.

254. Notably, the '634 Patent itself acknowledges that a bottom metal layer, limitation *[1d]*, was already present in the prior art. It identifies element 113 in FIG. 1 as a bottom metal layer formed on the lower surface of the semiconductor region–and expressly includes it among the conventional structural elements shared between the prior art and the claimed invention. (*See* Ex. 1001, '634 Patent, 1:18–41, Fig. 1.) The '634 Patent admitted prior art thus confirms a motivation to incorporate the known a backside metal drain contact feature in MOS transistor technology–as well as an expected feature in trenched-gate MOSFETs at the time of Filing Date of the '634 Patent.

Ex. 1001 ('634 Hsieh)

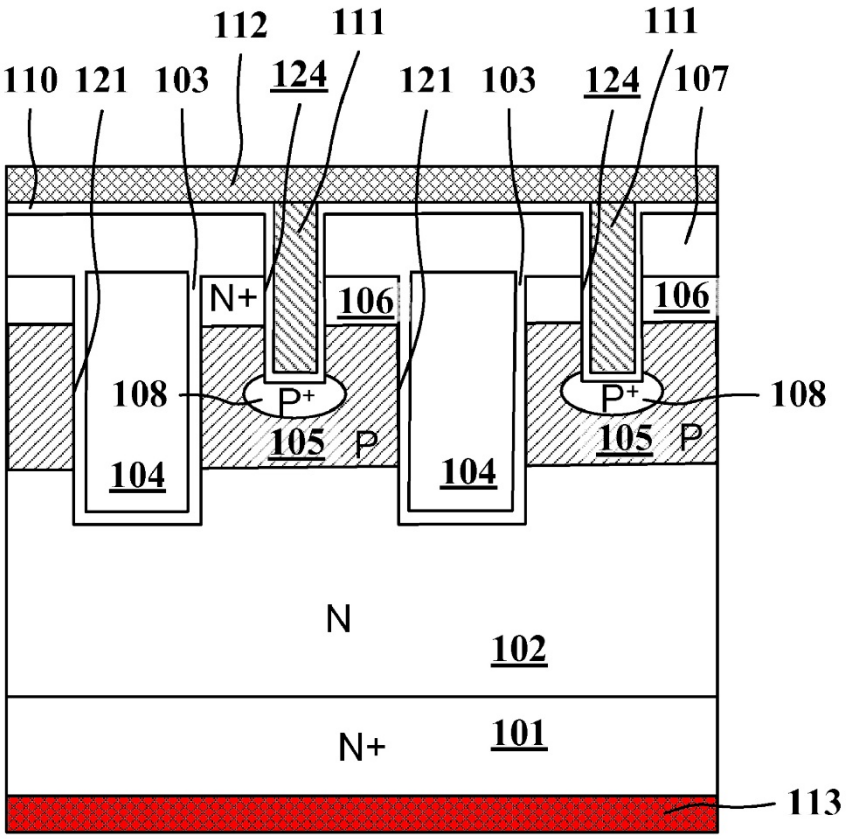
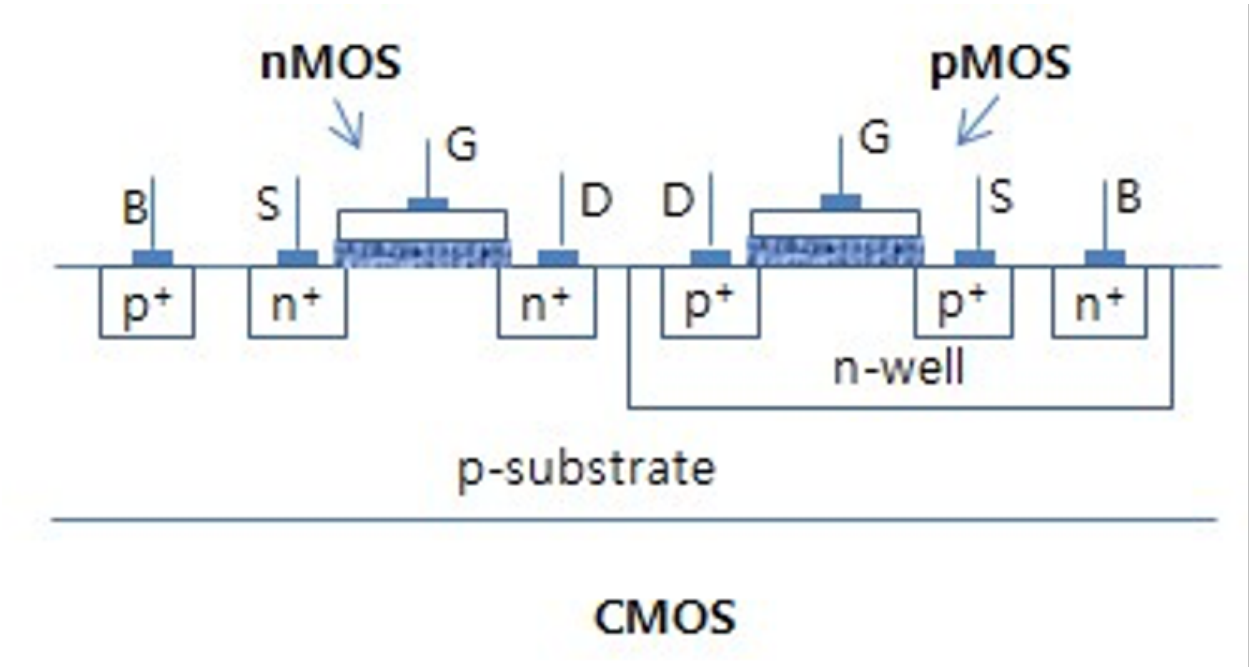


Fig. 1 (PRIOR ART) (Annotated)

255. Thus, a POSITA would have been aware of this type of metallic contact–and further, given that this was well-known in the art by at least as early as the Filing Date of the ’634 Patent–and is also of the same type of contact known to have been successfully used at least as far back as 1967–a POSITA would have had a reasonable expectation of success in deploying such a well-known technology into Hshieh (’384)’s structure.

256. For completeness, it should be noted that—given the structure disclosed in Hshieh ('384)—the only other approach to providing a drain contact electrode would be to place the drain contact on the top side of the structure, rather than on the back side. While such a configuration could conceivably be considered for various reasons (as discussed momentarily it would have been neither the ideal choice nor the most logical choice from the perspective of a POSITA when implementing a MOSFET based on the teachings of Hshieh ('384).

257. The main reason for the introduction and use of only top side electrodes was due to the planar structure of CMOS circuitry itself–as was explained in Section VII.C. As CMOS involves placing (at the minimum) an nMOS transistor and a pMOS transistor in the same silicon substrate, each device had to be placed in a "well" of the appropriate type (i.e., p-type for nMOS transistors and n-type for pMOS transistors). This could involve an "n-well" for the pMOS transistors (with the nMOS transistors formed in a p-type substrate), or a "twin-well" process in which there is an appropriate "well" for each polarity of MOS transistor (and in which case the well of the same polarity as the substrate (such as a p-well in a p-substrate) provides an inherent electrical connection between that well and the substrate (*See* illustrative image below)):



(Note that each instance of the "B" contact lead refers to a "body contact"–with one to the p-substrate for the nMOS transistor and one to the n-well for the pMOS transistor.)

258. As can readily be understood via these depictions, at least one (if not both) of the body contacts (for either the nMOS transistor or the pMOS transistor) must be on the top of the structure–as at least one of the wells does not reach the bottom of the substrate (where a backside contact would typically be placed–if used).

259. However, in Hshieh's ('384) trenched-gate MOSFET structure, a POSITA would reject this approach in favor of the simpler backside contact approach–for at least three reasons.

260. First, as can be seen by examination of Hshieh's ('384) structure (e.g., in Fig. 3 of Hshieh ('384), as depicted above), there is little space available at the top of the structure to add another type of contact.

261. Second, trench contact structures are already in place for the MOSFET gate electrode and for the MOSFET source/body contact:

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Ex. 1005 ('384 Hshieh)

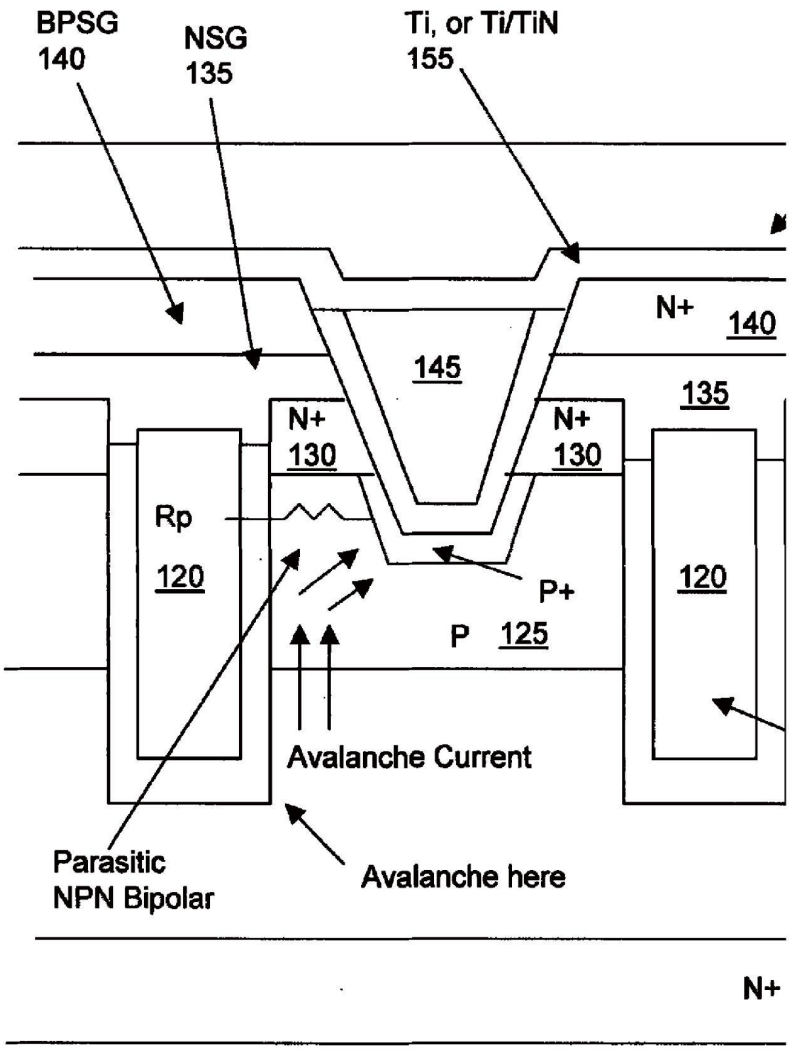


Fig. 3 (Annotated partial enlarged view)

A top-side drain contact would require the inclusion of a third family of trenches–to provide an electrical connection *all the way down to the N+ substrate layer* (element 15/105/205) at the bottom of the structure–something that would also require the formation of a trench all the way down to the N+ substrate layer

(element 15/105/205) (which, among other things, could compromise the physical integrity of the silicon wafer), followed by the filling of that deep trench (i.e., much deeper than those deployed for the gate electrode and the source/body contact) with a barrier layer metal (element 150/150'/245) and a metal contact plug; this makes the process for fabricating Hshieh's ('384) MOSFET structure even more complicated–whereas, in sharp contrast, the introduction of a simple metal backside contact is very straightforward and non-complex. Further, the addition of a top-side trenched drain contact would require expanding the size of the structure to accommodate it - while the use of a simple back side metal drain contact does not cause this detrimental problem to happen.

262. And third, as Hshieh ('384) teaches that his structure is specifically designed to keep the series resistance of the current path (i.e., the current path source-body-drain) low, the use of a simple backside metal contact will provide a low-resistance pathway in the simplest manner possible.

263. Had Hshieh ('384) contemplated a more-complex front-side drain contact structure—despite the practical disadvantages associated with such an approach—one would expect the disclosure to include additional discussion or to offer a more elaborate design accommodating that configuration. However, no such discussion or structural accommodation appears in the Hshieh ('384)

disclosure, further confirming that Hshieh envisioned a conventional back-side drain contact through the N^+ substrate (element 15/105/205).

264. Therefore, Hshieh ('384), when considered in combination with the knowledge of a POSITA and the admitted prior art, discloses "a bottom metal layer formed on the lower surface of said semiconductor region," consistent with the structure recited in the '634 Patent.

f. [1e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer, and"

265. This claim element is taught by Hshieh ('384), or by Hshieh ('384) and the knowledge of a POSITA.

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Ex. 1005 ('384 Hshieh)

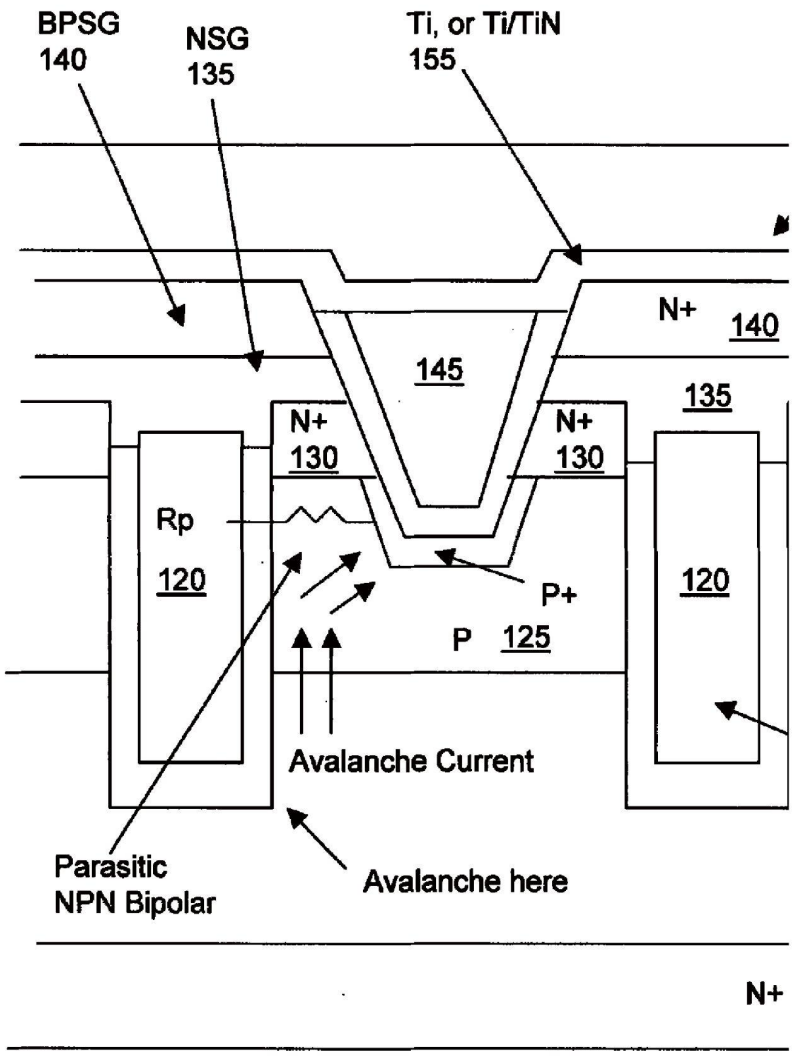


Fig. 3 (Annotated partial enlarged view)

266. ***[1e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer, and."***

267. Through the attorneys for the petitioner, I was provided a copy of the portion of the Claim Construction Order in the Patent Owner's litigation captioned *Force Mos Technology Co., Ltd. v. ASUSTeK Computer, Inc.*, No. 2:22-cv-00460 (E.D. Tex.) concerning limitation *[1e]*. The district court adopted a plain and ordinary meaning for the claim elements. Specifically, the court explained that "[t]he specification teaches that **the form of the trench gates** in the final device extends from the top of the source layer and through the base layer, which is what the claim language requires." (Ex. 2026, *Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc*., 2:22-cv-00460-JRG, E.D. Tex. (Marshall), 2022, ECF No. 132, p. 15) (*emphasis added*). The Court further explained that the trench gates were "formed" by etching trenches into the same silicon material that later became the source layer. (*Id*. at 14.) Critically, the Court declined to read into the claim any requirement regarding the height of the gates themselves relative to the top of the source layer, agreeing with Patent Owner's position that the gates need not "extend from above" the source layer. (*Id*.)

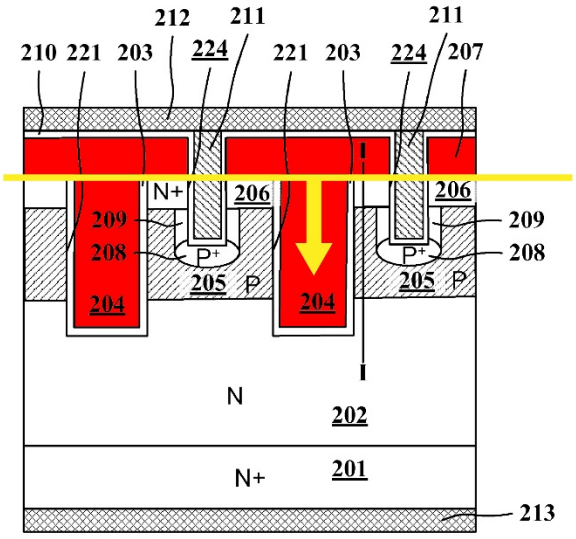
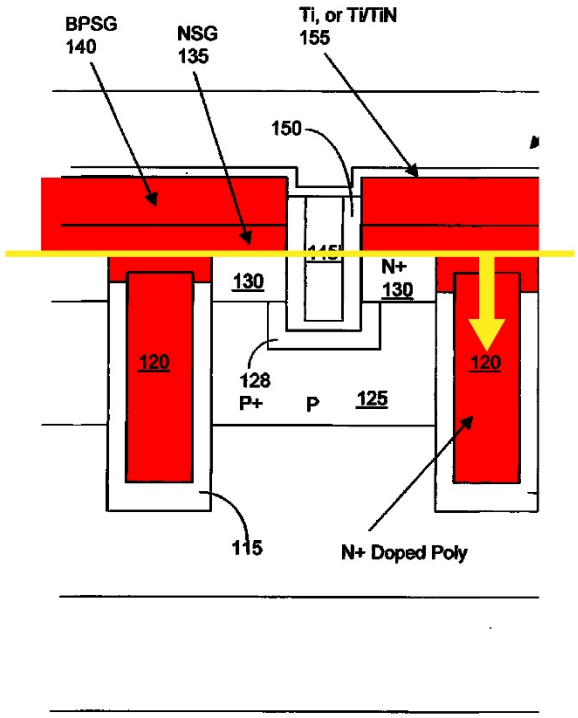
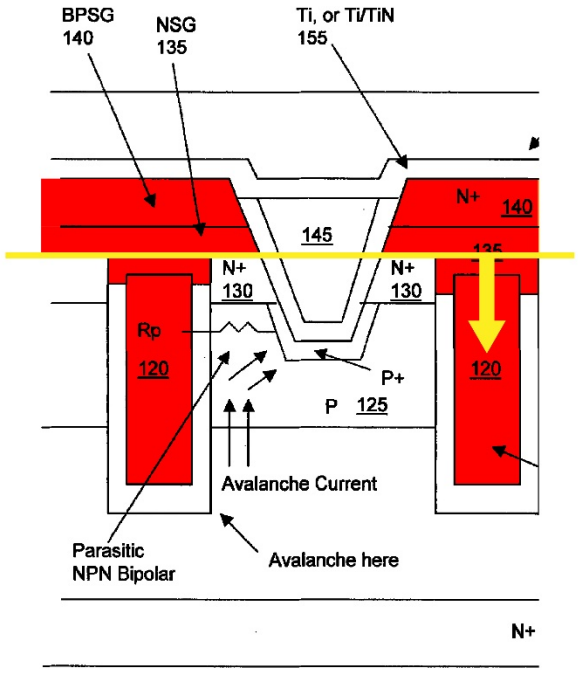
268. Hshieh ('384) clearly teaches this claim element, as shown in the annotated figures from both the '634 Patent and Hshieh ('384) below—consistent with the district court's explanation of the plain and ordinary meaning that the

trenched gates are formed downwardly through the source and base layers into a portion of the epitaxial layer and are covered by an interlayer oxide film.

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[1e]

a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

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As can be readily seen in the annotated figures from Hshieh ('384)–which depict two different embodiments–the claim element *[1e]* is clearly disclosed. Specifically, the trenched gates required by this element of the '634 Patent are unambiguously present in Hshieh ('384). The trenched gates (element 120), which are covered by the interlayer oxide film (element 135/140), extend from the top of the source layer (element 130) and through the base layer (element 125) into a portion of the epitaxial layer (element 110), which is what the claim language requires. (Ex. 1005, Hshieh ('384), ¶[0026], Figs. 3-8, element 120; ¶[0006], Fig. 1, elements 45-1, 45-2; ¶[0027], Figs. 3-8, elements 135, 140; ¶[0034], Figs. 9E-J and 9G', elements 235, 240; ¶[0006], Fig.1, element 30; ¶¶[0026]-[0030], Figs. 3-8, element 130; ¶[0034], Figs. 9D-J and 9G', element 230.)

269. Further, given the admitted prior art shown in Fig. 1 (PRIOR ART) of the '634 Patent, the concept of a trenched gate—covered by an interlayer oxide film extending downward from the top of the source layer, through the base layer, and into a portion of the epitaxial layer—was already well-known in the art.

270. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses limitation *[1e]*.

g. [1f]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein the sidewalls of said trenches in said base layer are covered by the lateral

contact layer; wherein the bottom base of said trenches in said base layer are [sic] covered by the base contact layer."

271. This claim element is taught by Hshieh ('384), or is rendered obvious by Hshieh ('384) in combination with the knowledge of a POSITA.

272. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [1f-1]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer;"

273. This claim sub-element is taught by Hshieh ('384).

274. ***[1f-1]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer".*** This claim element is disclosed in Hshieh, which teaches source contact trenches that correspond to element '634-124/224 of the '634 Patent. Specifically, Hshieh discloses "contact trenches 244." (*See* Ex. 1005, ¶34-35.) These are further identified as "source-body contact trench 244," as shown in FIG. 9F (reproduced below). As depicted, trench 244 extends downwardly through the source layer 230 and into a portion of the base layer 225.

Ex. 1005 ('384 Hshieh)

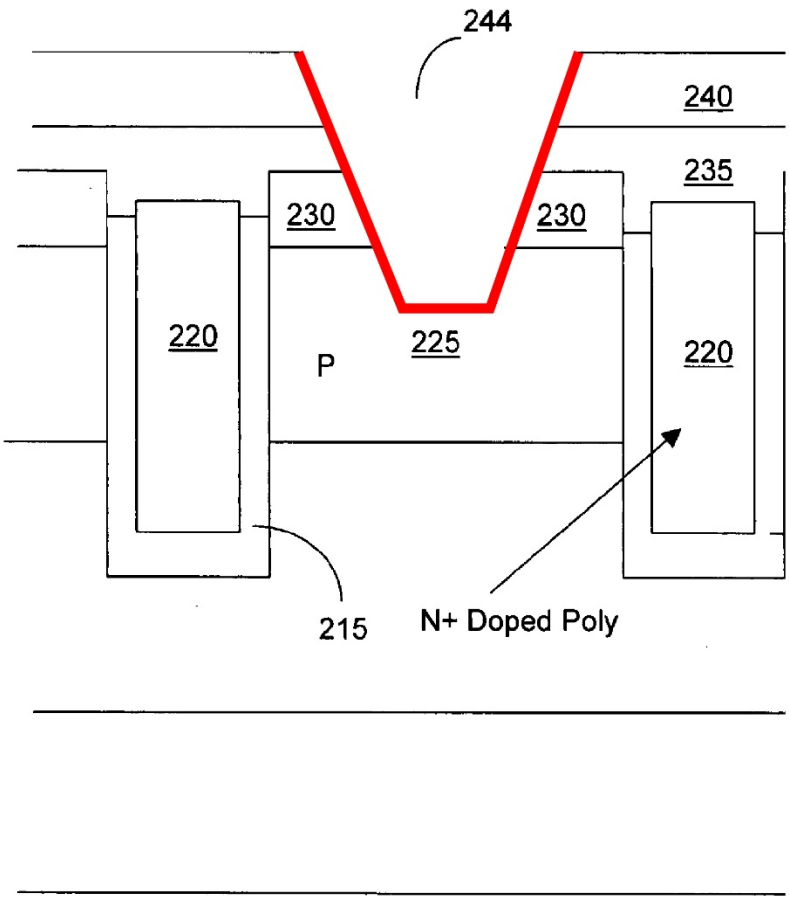


Fig. 9F (Annotated partial enlarged view)

275. Additionally, in annotated FIG. 3 of Hshieh (’384), elements 135 and 140 are identified as interlayer oxide films, element 130 as the source regions (formed within the source layer), and element 125 as the body regions (formed within the base layer). These designations are consistent with the prior discussion above. (*See* Section XI A.2.b.) The spatial arrangement of these layers in Hshieh is

consistent with the structural configuration recited in the challenged claim sub-element.

[1f-1]

a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer

Ex. 1005 ('384 Hshieh)

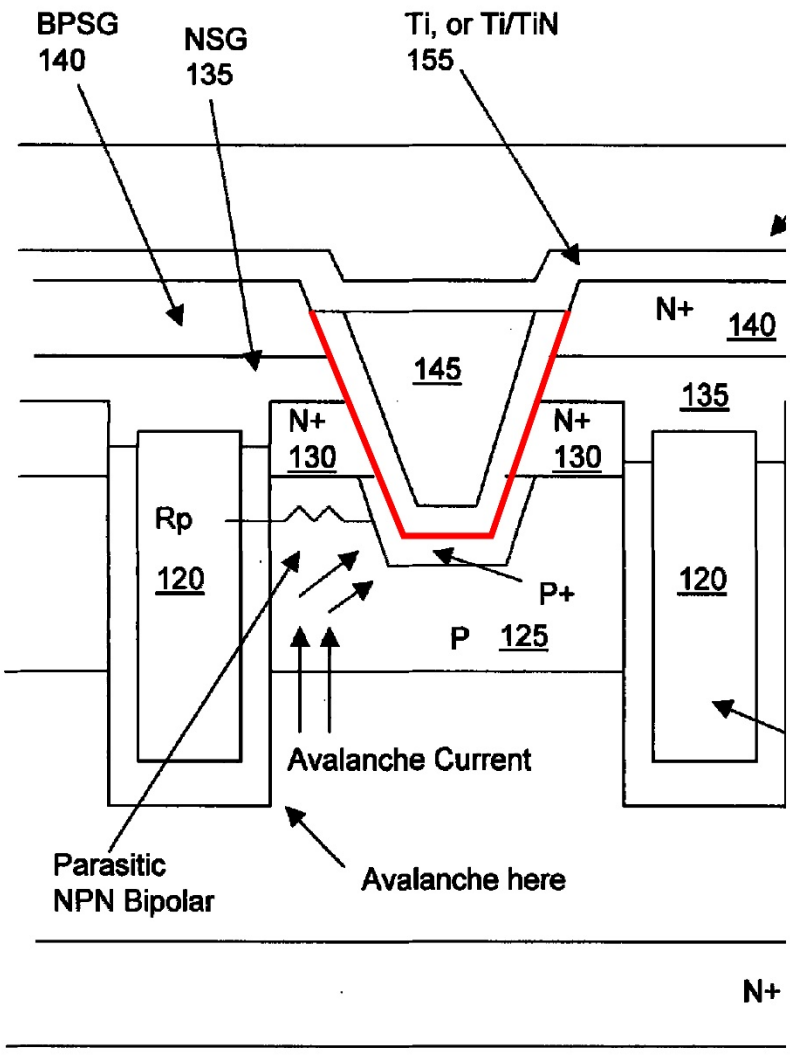
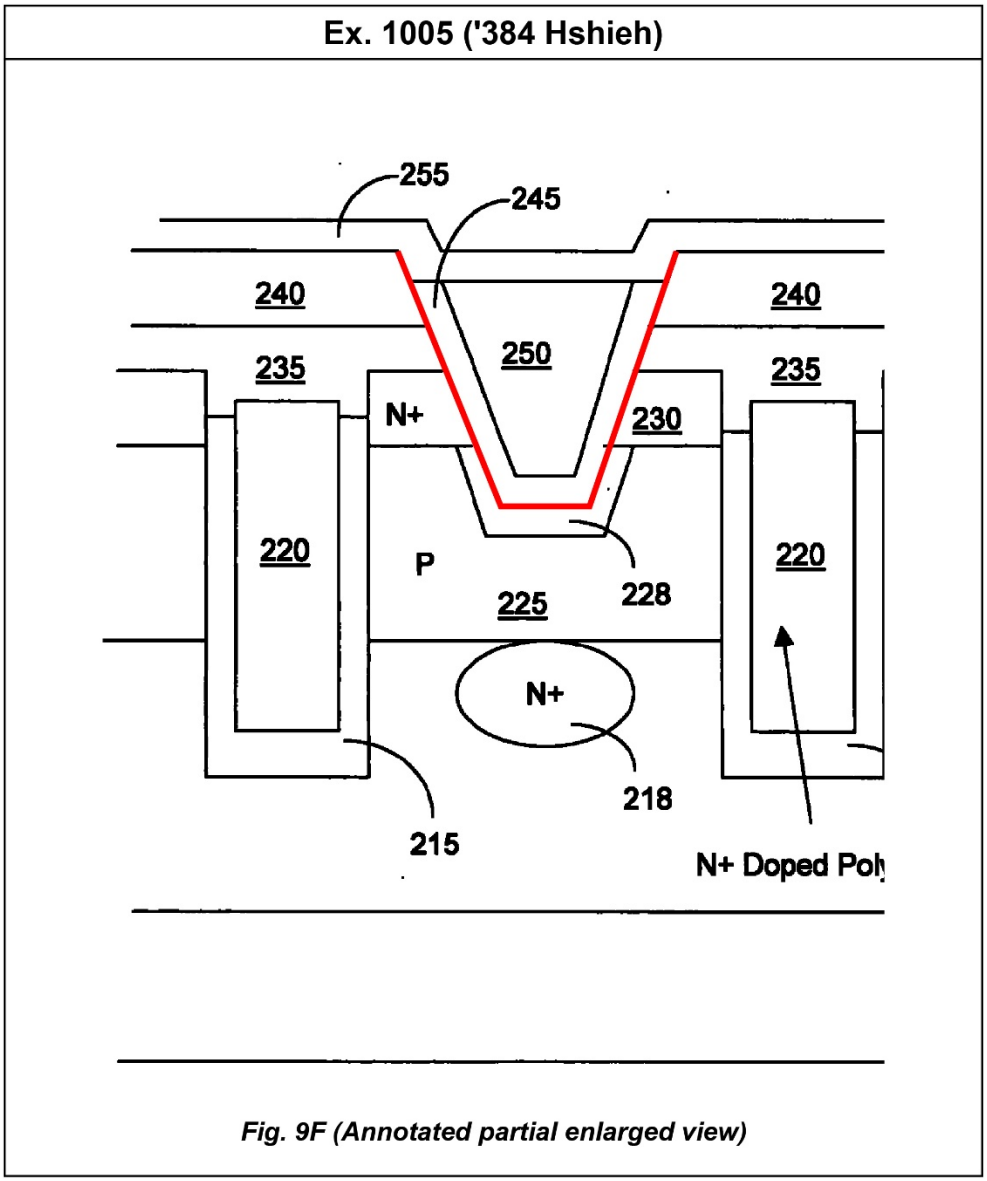


Fig. 3 (Annotated partial enlarged view)

276. For completeness, although the source contact trenches are unnumbered in FIG. 3, they are explicitly referenced in the text and visually annotated in the reproduced figure. Their lack of numbering appears to be due to the presence of the tungsten plug 145 occupying the contact trench 244. Nonetheless, Hshieh clearly discloses a plurality of source contact trenches. As stated in ¶27, "[f]or the purpose of improving the source contact to the source regions 130, a plurality of trenched source contact filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is provided. (*Id.* at ¶27.) Element 145 is thus used to refer to the trenched source contacts. (*Id.* at ¶28-29; Fig. 3-4.)The multiple instances of these structures in FIG. 3 confirm that Hshieh teaches a plurality of source contact trenches.

277. As further detailed in Section XI A.2.b., the structure and placement of these trenches are established during the etching process, which forms them directly in the silicon. The location and extent of the trench structures are defined when these trenches are etched and thus formed in the silicon, which shows that the source contact trenches are both "formed on the top of the interlayer oxide film and extend downwardly through the source layer to a portion of the base layer. (*Id.* Fig. 9F.) This teaches the limitations of the claim sub-element requiring the source contact trenches to be "formed on the top of said interlayer oxide film" and to

"[extend] downwardly through said source layer to a portion of said base layer." (*Id.* Fig. 9F.)



ii. [1f-2]: "wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;"

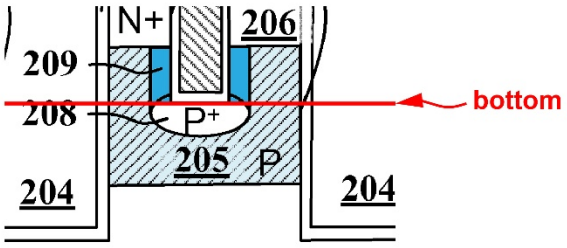
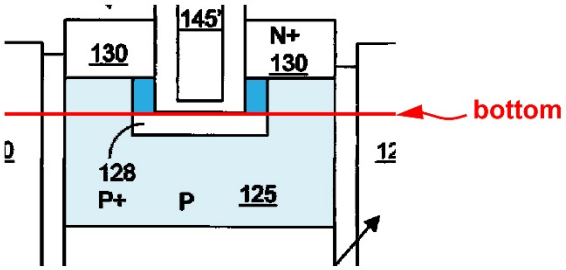
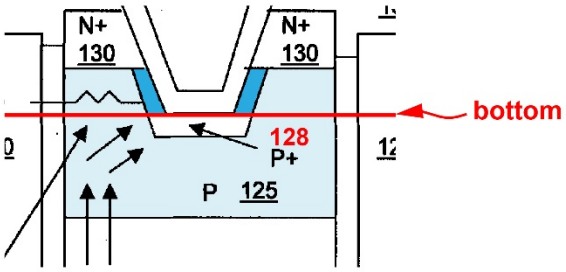
278. This claim sub-element is rendered obvious by Hshieh ('384) in combination with the knowledge of a POSITA.

279. ***[1f-2]:*** **"wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer."** The annotated "P^+" layer(s) (128) of Hshieh ('384) satisfy the claim sub-element requirement of providing a "lateral contact layer," as these layers extend along the sidewalls of the trenches within the body regions of the base layer. (*See* Ex. 1005, ¶29; FIG. 4, element 128 labeled as 228 in FIGs. 9A to 9J.) Although Hshieh ('384) does not explicitly identify its P^+ regions as comprising two separately distinguishable subregions, the portion annotated below in medium blue corresponds to the "lateral contact layer" described in the '634 Patent.

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[1f-2]

wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

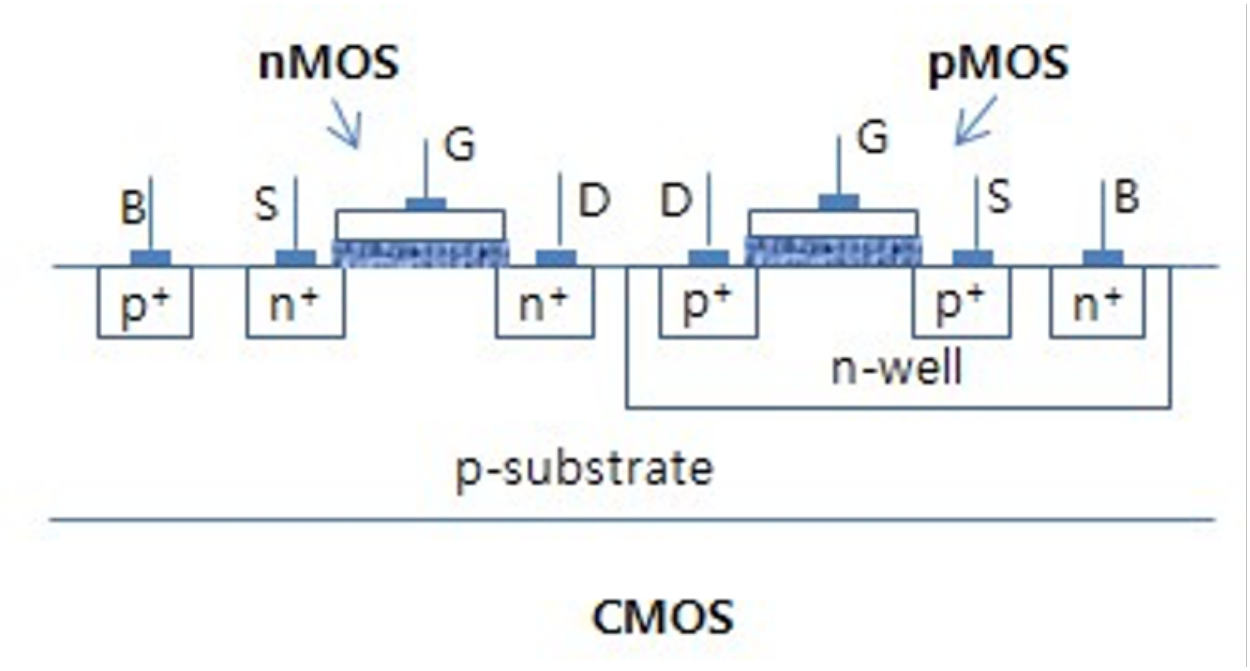
280. As discussed in the claim construction analysis above, the ’634 Patent explicitly defines the “lateral contact layer” as extending from the bottom of the source contact trench along the sidewalls of the trench within the base layer.

281. It is important to note that, although Hshieh (’384) labels the “lateral contact layer” (128/228) as “P^+,” the relative doping concentration (e.g., P, P*, or P^+) is irrelevant to the analysis of claim 1, as the claim is directed solely to the structural configuration of the MOSFET and does not impose any specific limitations on relative doping levels. As explained in more details below in Section

XI.A.3 (where Claim 2 is considered), as long as both the labeled "P+" layer and the labeled "P*" layer have sufficient dopant concentrations to make both of them chemically "P+" material, they will provide the required low-resistance ohmic contact necessary for the trenched source contact to function properly when it comes in contact with the silicon of the body region.

282. To the extent it is necessary to explain why the "lateral contact layer" is annotated as such in the Hshieh ('384) figure, the rationale for providing this form of body contact layer surrounding the entirety of the source contact trench within the base layer—as a whole—was well known in the art, and therefore would have been readily understood by a person of ordinary skill in the art (POSITA) at the time of the '634 Patent.

283. As described above in the discussion associated with claim element *[1d]* (in Section XI.A.2.e), it has long been common practice in transistor fabrication to place the body contact electrode on a pocket of heavily-doped silicon (doped either N+ or P+, as the situation requires); reprising the example provided the previous section: (*See* illustrative image below.)



284. As explained earlier, the metal electrode forming the body contact makes physical contact only with the silicon within the heavily doped region (whether P^+ or N^+), as depicted above. This configuration is intentional and well understood in the art, as it ensures that the resulting body contact is a low-resistance ohmic contact. In contrast, if the metal were to contact a relatively lightly doped P-type substrate or N-well, the result would be either an ohmic contact with unacceptably high resistance or, worse, a non-ohmic contact—such as a Schottky barrier. Any contact that fails to establish a low-resistance ohmic connection would degrade the electrical behavior and performance of the transistor, making such configurations undesirable in practical semiconductor design.

285. In fact, Hshieh ('384) explicitly recognizes this design requirement and clearly states that the source contact should interface with the body region only through a heavily doped surface layer (i.e., P^+), for the reasons discussed in the preceding paragraph. For example, Hshieh ('384) repeatedly emphasizes the use of "doped regions surrounding the trenched source-body contact to reduce the ohmic resistance Rp of the body region." (Ex. 1005, Hshieh ('384), ¶¶[0018]–[0023]; *see also* ¶¶[0028]-[0029].) Hshieh ('384) further explains that maintaining this low contact resistance is critical to preventing the activation—what Hshieh refers to as "the triggering"—of a parasitic N^+/P/N bipolar transistor inherent in this type of trench MOSFET structure. (*Id.* ¶¶[0028]–[0030].)

286. Hshieh ('384) further provides a detailed explanation of the process steps for forming the MOSFET structure shown in Fig. 3, stating: "The sloped trenches allow the formation of heavily doped P^+ regions 128 along both the trench sidewalls and the bottom through zero-degree ion implantation of boron or BF_2." (*Id.* ¶[0028]) This statement demonstrates that Hshieh ('384) explicitly distinguishes between the **trench sidewalls** and the **trench bottom**.

287. Furthermore, with specific reference to Fig. 3, Hshieh ('384) describes "a P^+ doped region 128 surrounding the source-body trenched contact." (Ex. 1005, Hshieh ('384), ¶[0028].) To fully surround the source-body trenched contact, the P^+ doped region must necessarily extend along both the **trench**

sidewalls and the **trench bottom**—encompassing the entire contact area as shown in the Fig. 3 below:

Ex. 1005 ('384 Hshieh)

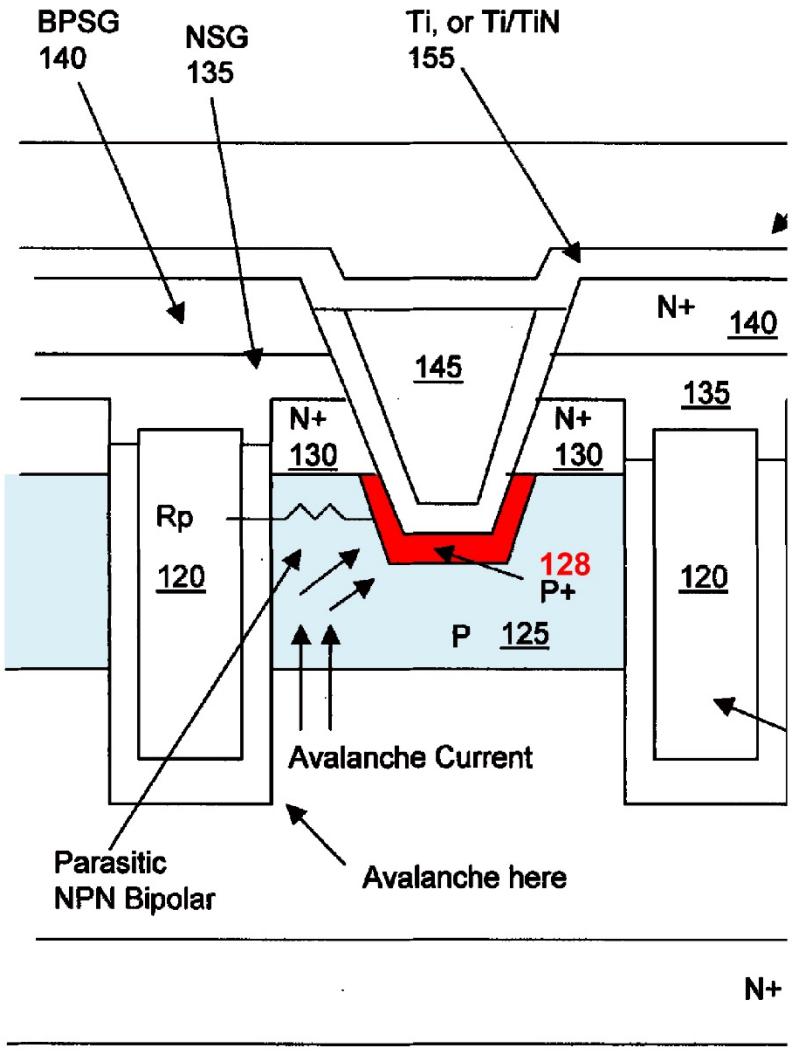


Fig. 3 (Annotated partial enlarged view)

288. Consistent with what was described above, Hshieh ('384) again states that one purpose of the creation of a p+ layer that "surrounds" the source-body

trench contact is that "[t]he P+ doped region 128 is formed to enhance avalanche current before triggering parasitic N+PN bipolar, i.e., the N+ source 130 with a P-body 125 and the N-epitaxial layer 110." (Ex. 1005, Hshieh ('384), ¶[0028].)

289. Finally, with respect to Fig. 4 of Hshieh ('384)—and specifically the P^+-doped layer located entirely at the surface of the silicon within the body region, where it interfaces with the metal of the source contact plug—Hshieh ('384) describes "the high doped region 128 surrounding the trenched source-body contact 145'." (Ex. 1005, Hshieh ('384), ¶[0029].)

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Ex. 1005 ('384 Hshieh)

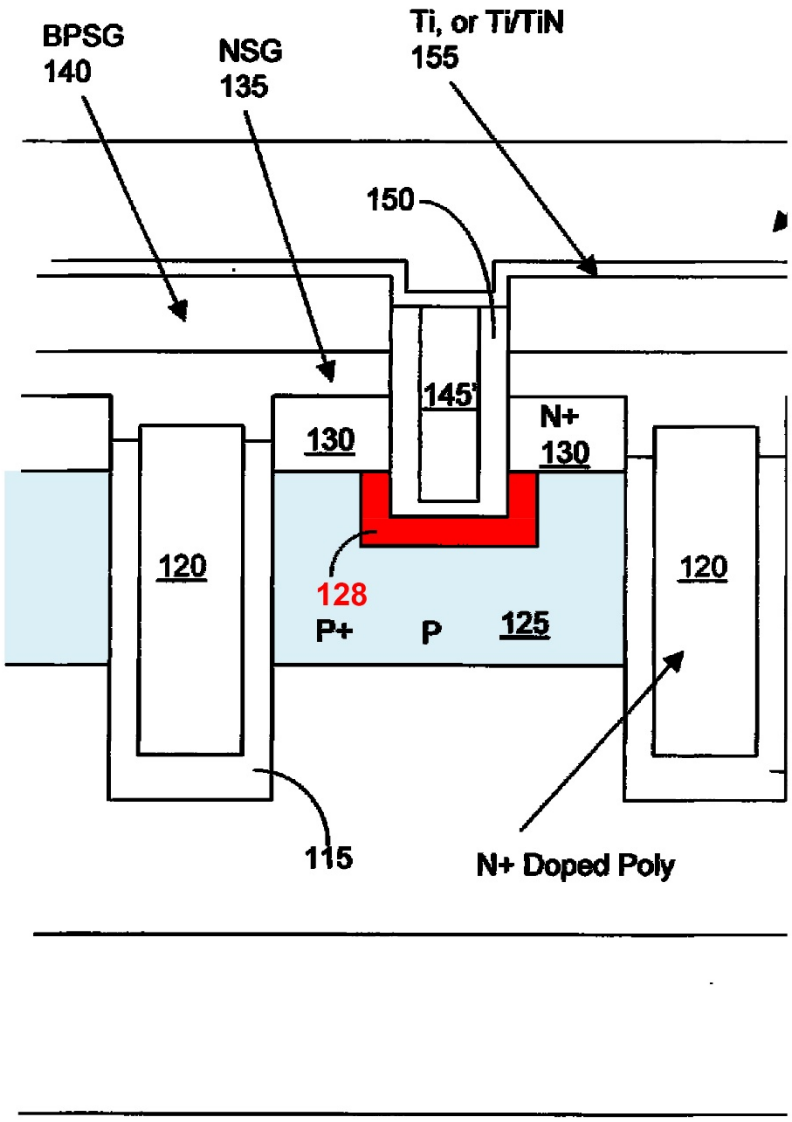


Fig. 4 (Annotated partial enlarged view)

Hshieh (’384) describes the function of this p+ layer (128) that “surrounds” the source-body contact (and completely covers the interface between the source-body contact metal and the silicon of the body region) as “[t]he highly P+ doped regions 128 serves the same function as described for FIG. 3.” (Ex. 1005, Hshieh

('384), ¶[0029].) Hshieh ('384) also treats other embodiments consistently, specifically identifying "P^+ doped regions 228 surrounding the source-body trenched contact." (Ex. 1005, Hshieh ('384), ¶¶[0035]-[0036].)

290. Thus, a POSITA would understand a structure in which the metal contact plug makes contact with the body region only through a layer of heavily doped silicon—consistent with the commonly used and well-known practice described above, for the reasons previously discussed, and as explicitly stated by Hshieh ('384).

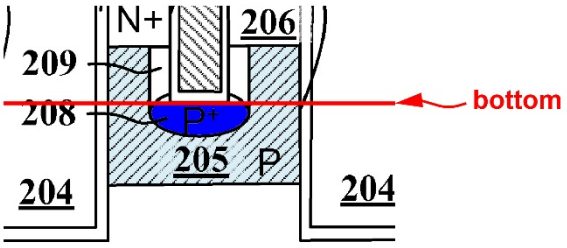
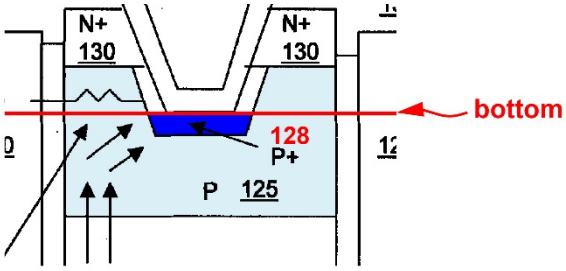
291. In order for this p+-doped layer to "surround" the source-body contact, this doped layer must extend upward so that it is present in the sidewalls of the trench that are part of the body region; this is the "lateral contact layer" of this claim sub-element.

iii. [1f-3]: "wherein the bottom base of said trenches in said base layer are [sic] covered by the base contact layer."

292. This claim sub-element is taught by Hshieh ('384), or is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

293. The annotated "P^+" layer teaches the claim sub-element requirement of providing a "base contact layer," as this layer covers the bottom of the trenches. Although Hshieh ('384) does not label or describe the identified P^+ region as consisting of two separately identifiable sub-regions, the portion of the P^+ region

annotated in the figures above in dark blue corresponds to the base contact layer as described in the ’634 Patent.

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated partially enlarged view)	*Fig. 3 (Annotated partial enlarged view)*

294. As discussed in the claim construction analysis above, the ’634 Patent explicitly defines the “base contact layer” as existing at the bottom of the source contact trench within the base layer.

295. To the extent it is necessary to explain why the contact layer in Hshieh (’384) is shaped as depicted—and why it is formed in that particular configuration—this issue has already been addressed above in the discussion of claim sub-element *[1f-2]*, in Section XI.A.2.g.ii.

296. Finally, as noted above with respect to claim sub-element *[1f-2]*, Hshieh (’384) describes the identified P^+-doped layer as “surrounding” the source-body contact, and depicts this “surrounding” to include the presence of the P^+-doped layer at the silicon surface at the bottom of the trench—where the source-body contact interfaces with the silicon body region. (Ex. 1005, Hshieh (’384),

¶[0028].)This region corresponds to the "base contact layer" recited in this claim sub-element.

h. Claim 1 Summary

297. For all of the reasons described above, Claim 1 of the '634 Patent is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

3. Claim 2: "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

298. Claim 2 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2) that Claim 1 of the '634 Patent is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

299. The remainder of Claim 2 is also rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

300. To simplify the analysis, this claim will be split into claim elements.

a. [2a]: "wherein the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof,"

301. This claim element is taught by Hshieh ('384).

Ex. 1005 ('384 Hshieh)

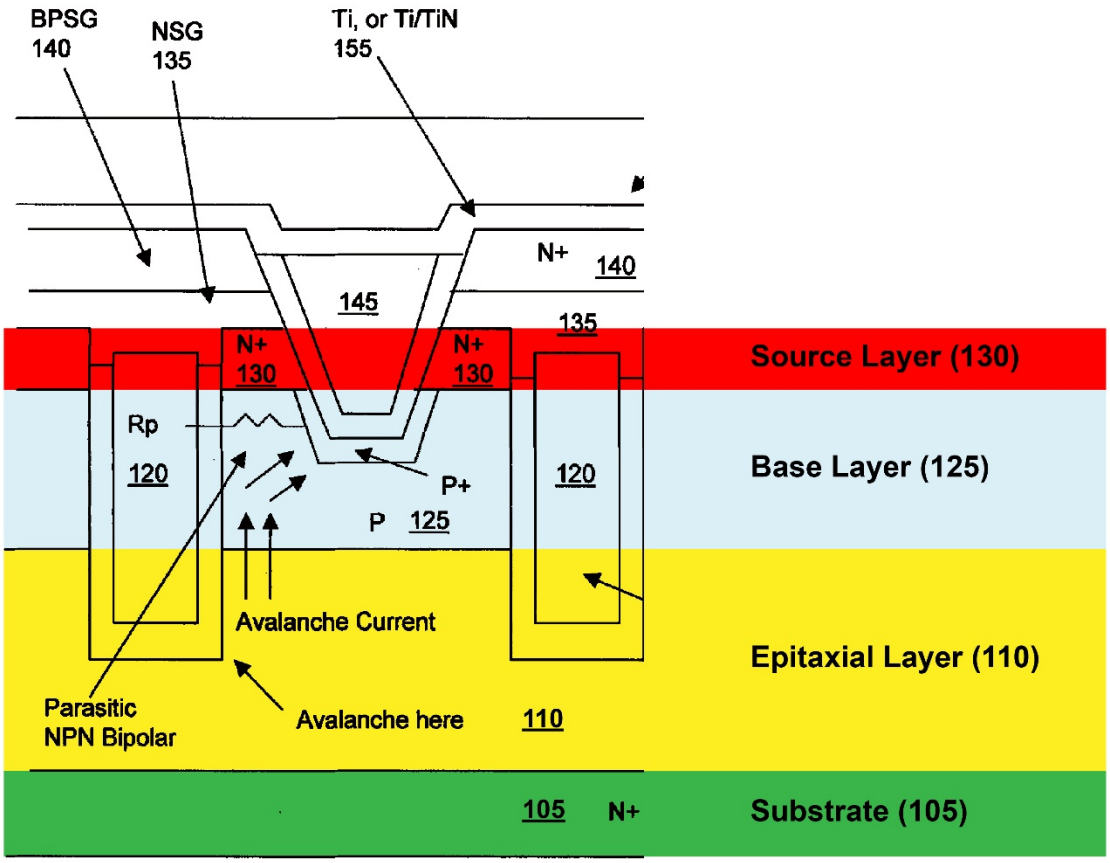
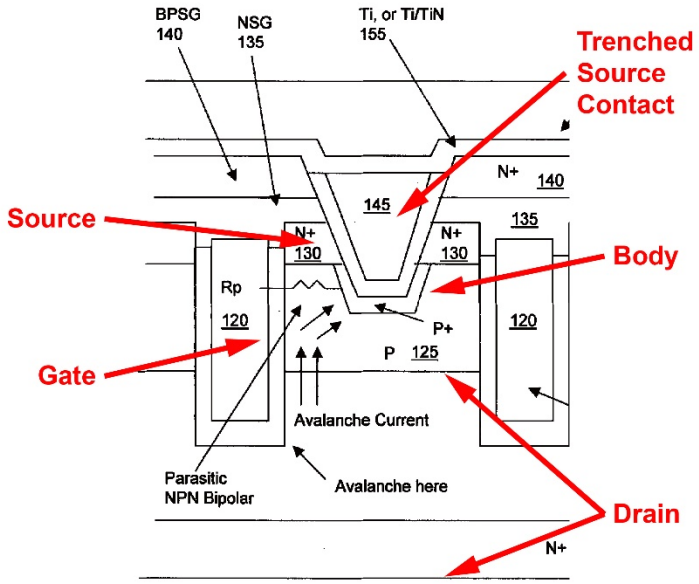
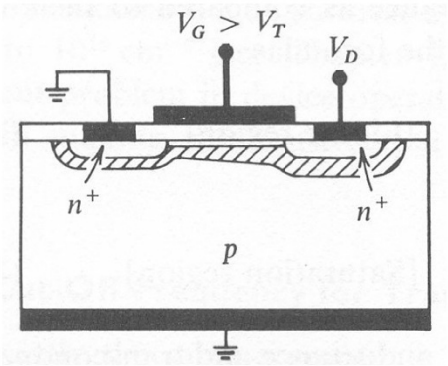


Fig. 3 (Annotated partial enlarged view)

In Fig. 3, Hshieh ('384) identifies the substrate 105, the epitaxial layer 110, and the source layer (which here has been divided up into the source regions 130) as being "N-type," the base layer (which here has been divided up into the body regions 125) and the lateral contact layer (as described in the discussion of claim sub-element *[1f-2]* (in Section XI.A.2.g.ii)) as being "P-type," and the source contact trenches have a P-type base contact layer (as described in the discussion of claim sub-element *[1f-2]* (in Section XI.A.2.g.ii)) at the bottom of those trenches.

302. It should also be noted that the transistor depicted in Hshieh ('384) Fig. 3 is readily-identified as being an nMOS type of transistor.

Ex. 1005 ('384 Hshieh)	Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 (1967)
 ***Fig. 3 (Annotated partial enlarged view)***	 ***Fig. 11.8 (Annotated partial enlarged view)***

303. The claim element above is, among other things, a verbose way of stating that the transistor structure described therein is an nMOS transistor.

304. Hshieh ('384) clearly teaches a device structure comprising an N-type silicon substrate, an N-type epitaxial layer, and an N-type source region, corresponding to elements 101/201, 102/202, and 106/206 of the '634 Patent.

305. Hshieh ('384) discloses a layered semiconductor structure that begins with a heavily doped N^+-type silicon substrate; specifically, the patent states that "a

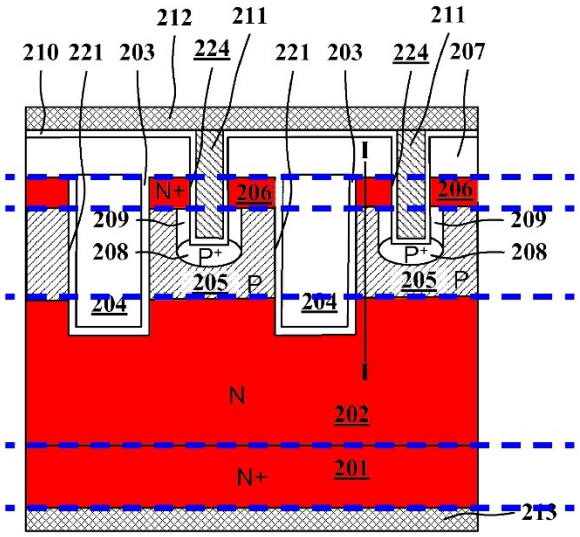
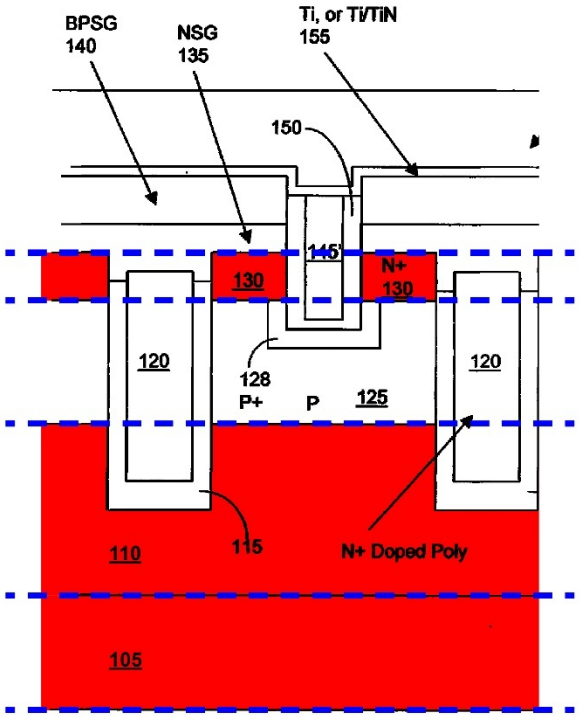
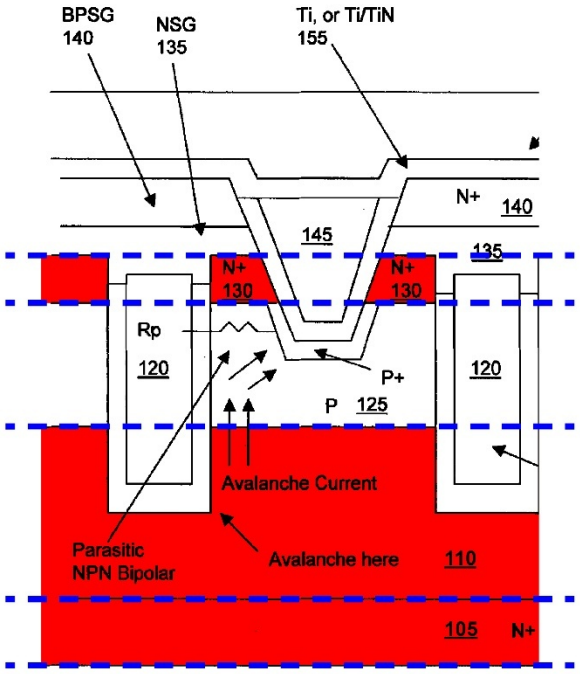
N+ substrate 105 [is] formed with an N epitaxial layer 110," thereby describing the substrate and overlying epitaxial layer. (Ex. 1005, Hshieh ('384), ¶[0026]; Figs. 3–8, elements 105 and 110.) This same vertical structure is preserved in an alternative embodiment–where the corresponding elements are labeled as substrate 205 and epitaxial layer 210. (*Id.* ¶[0034]; Figs. 9A–G'.)

306. Positioned above the N-type epitaxial layer and P-body is a highly doped N^+-type source region. In the introductory embodiment, Hshieh ('384) refers to this region as "source region 30." (*Id.* ¶[0006]; Fig. 1, element 30.), while in the main and alternative embodiments, the source regions are labeled as elements 130 and 230, respectively. (*Id.* ¶¶[0026], [0028]–[0030], [0034]; Figs. 3–8, element 130; Figs. 9D–J and 9G', element 230.) These source regions are formed above the P-type body and above the N-type epitaxial region, and are described as being heavily doped–which is consistent with standard N^+-type source fabrication and with the structure recited in the '634 Patent.

307. Accordingly, it is my conclusion and opinion that Hshieh ('384) discloses a device comprising an N-type silicon substrate, an N-type epitaxial layer, and an N-type source region–as required by limitation *[2a]* of the '634 Patent.

[2a]

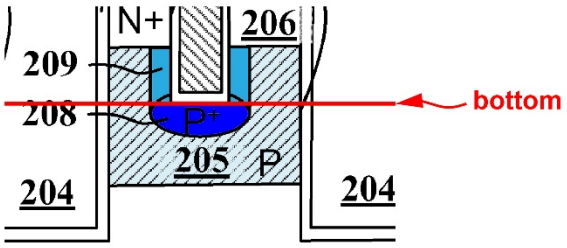
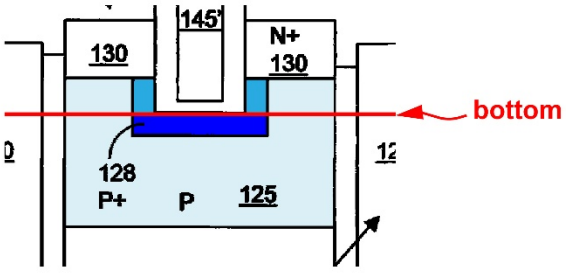
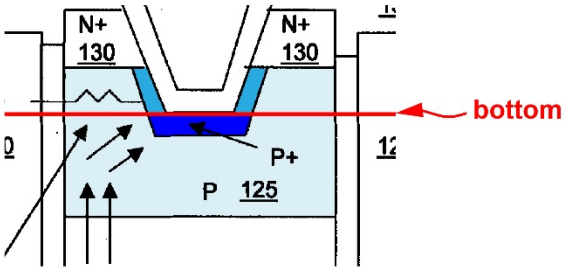
N-type silicon substrate, epitaxial layer, & source layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

b. [2b]: P-type base layer & P-type "lateral contact layer."

308. Hshieh ('384) teaches a P-type base layer and a lateral contact layer corresponding to elements 105/205 and 209 of the '634 Patent. The '634 Patent identifies the P-type base layer as providing the body regions of the MOSFET structure. (*See* Ex. 1001, '634 Patent, 5:1–2.) Hshieh ('384) discloses a P-type base layer–as this base layer is necessary for the eventual formation of the separate body regions (which are defined when the trenches are etched) that Hshieh ('384) refers to as "a P-body region 25," forming part of the vertical structure. (*See* Ex. 1005, Hshieh ('384), ¶[0006]; Fig. 1, element 25.) In alternative embodiments, the base layer is again the precursor to the eventual body regions–which are there referred to as "P-body 125" and "P-body 225," formed by implantation or boron into the upper portion of the epitaxial layer of the device. (*Id.* ¶¶[0026]-[0034]; Figs. 9C–G', element 225.)

[2b]
P-type base layer & lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

309. The ’384 patent also discloses a P+-type doped region formed along the sidewalls of the source contact trench. Specifically, it states that “the P+ doped region 228 [is] to surround the trenches 224,” forming a low-resistance ohmic contact to the base region along the trench perimeter. (*Id.* ¶¶[0035]–[0036]; Figs. 9G–G’, element 228.) This region corresponds to the “lateral contact layer” (’634-209) of the ’634 Patent.

310. As explicitly stated in the ’634 Patent, the “lateral contact layer” (’634-209) is formed along the trench sidewalls, while the base contact layer (’634-

108/208) is formed at or beneath the trench bottom. (*See* Ex. 1001, '634 Patent, 5:9–12; 3:50–55.) This structural distinction confirms that the "lateral contact layer" in Hshieh ('384)—formed along the trench sidewalls—must reside above the trench bottom, within the P-type base layer ('634-105/205), while any "base contact layer" would reside at or beneath the floor of the trench and in contact with deeper portions of the base.

311. Thus, it is my conclusion and opinion that Hshieh ('384) discloses limitation *[2b]* of the '634 Patent where both the base layer and lateral contact layer are p-type.

c. [2c]: P-type base contact layer at bottom of source contact trenches.

312. Hshieh ('384) provides a P-type base contact layer (i.e. '634-108/208) at the bottom of source contact trenches (i.e. '634-124/224). The '384 patent publication provides "... to form the P+ doped region 228 to surround the trenches 224" (Ex. 1005, Hshieh ('384), ¶[0035]-[0036]; Figs. 9G-G' element 228.)

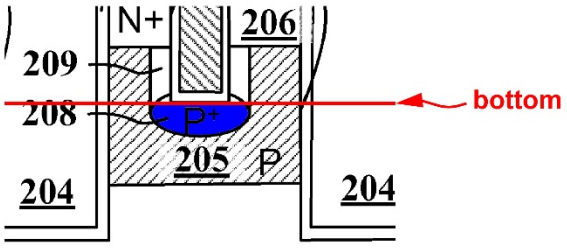
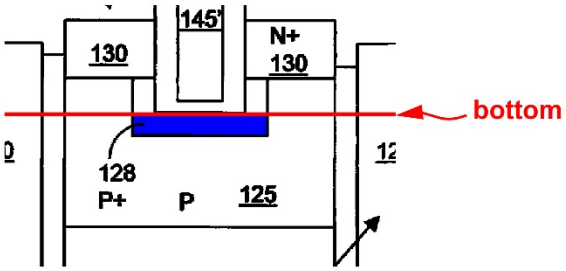
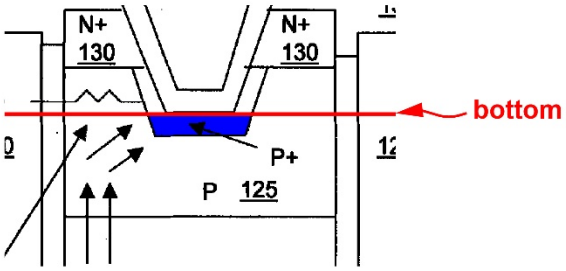
313. Limitation *[2c]* is disclosed in Hshieh ('384), which provides a P-type base contact layer corresponding to element 108/208 of the '634 Patent. The '634 Patent describes this base contact layer as being formed at or beneath the bottom of the source contact trench, to establish a direct low-resistance ohmic contact to the deeper region of the P-type base. (*See* Ex. 1001, '634 Patent, 3:50–55; 5:9–12.).

314. Hshieh (’384) discloses a similar structure. Specifically, the patent states that “the P+ doped region 228 [is] to surround the trenches 224,” indicating that this region encompasses both the sidewalls and bottom of the trench. (*See* Ex. 1005, Hshieh (’384), ¶[0035]; *see also* ¶[0036]; Figs. 9G–G’, element 228.) Although not explicitly segmented into sidewall and bottom regions, the use of the word “surround” and the description of region 228 at the base of the trench in the figures make clear that this region also functions as a base contact layer, positioned at the trench floor bottom to provide low-resistance electrical contact to the underlying P-type base region (element 225).

<This space intentionally left blank.>

[2c]

P-type base contact layer at bottom of source contact trenches

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
	
Fig. 2G (Annotated partially enlarged view)	*Fig. 4 (Annotated partial enlarged view)*
	
	Fig. 3 (Annotated partial enlarged view)

315. This structure is consistent with the distinction made in the ’634 Patent between the lateral contact layer (formed on the trench sidewalls) and the base contact layer (formed at or beneath the trench bottom). While Hshieh (’384) does not explicitly label the bottom region as a base contact layer (128/228), its functional placement at the trench bottom and its contact with the underlying body layer (P-body 25/125/225) satisfy both the position and purpose of element ’634-108/208.

316. Accordingly, Hshieh ('384) discloses a P-type base contact layer formed at the bottom of the source contact trench, providing ohmic contact to the P-type base, and thereby teaches limitation *[2c]*.

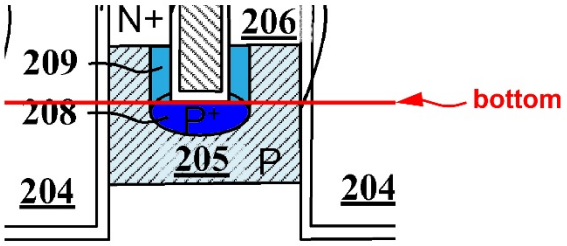
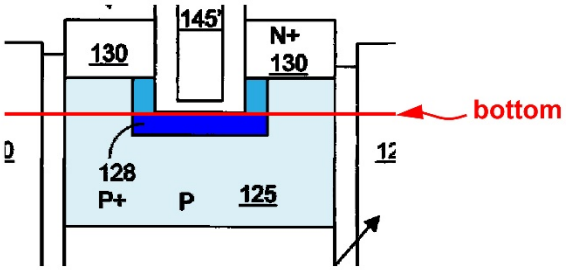
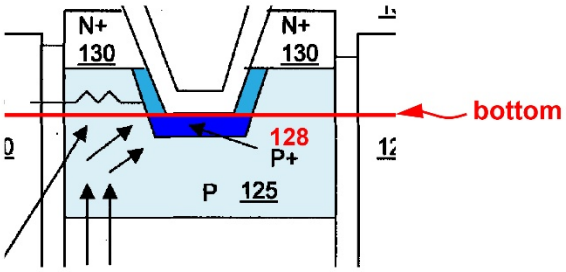
d. [2d]: "and the lateral contact layer has less doping concentration than the base contact layer at bottom."

317. This claim sub-element, which I refer to as limitation *[2d]*, is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

318. As discussed in *[1f-2] and [1f-3]*, Hshieh ('384) teaches that the source contact trenches (element 244/244'/224) are surrounded by a P^+-type doped region (element 128/228), which corresponds to both the "lateral contact layer" and the "base contact layer" of the '634 Patent (elements 209 and 108/208 respectively). (*See* Ex. 1005, Hshieh ('384), ¶¶[0035]–[0036]; Figs. 9G–G'.) Hshieh describes this P^+ doped region as being formed to "surround" the trench—meaning, as shown in the figures, that the doped region is present along both the trench sidewalls and the trench bottom. Hshieh ('384) explicitly teaches this P^+-doped layer "surround" the source-body contact within the body region and extend upward from the trench bottom to form the "lateral contact layer" as claimed in the '634 Patent. (*See* discussion of limitation *[1f-2]* above.)

[2d]

lateral contact layer has less doping concentration than the base contact layer at bottom

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated partially enlarged view)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

319. It should be noted that both the claims of the ’634 Patent and those of Hshieh (’384) are directed to apparatus, not method, claims. While Hshieh (’384) does not explicitly disclose this particular claim element, the specification describes fabrication methods from which it readily follows that at least one of those methods would result in a structure that inherently satisfies this claim element.

320. In Fig. 9G, Hshieh (’384) discloses a proposed method of creating the doped layer that provides a heavily-doped region in the body regions of the

transistor–for the purpose of providing complete coverage of the surface where the metal plug of the source contact makes physical contact with the body region (as explained in the discussion of claim sub-element *[1f-2]* in Section XI.A.2.g.ii):

Ex. 1005 ('384 Hshieh)

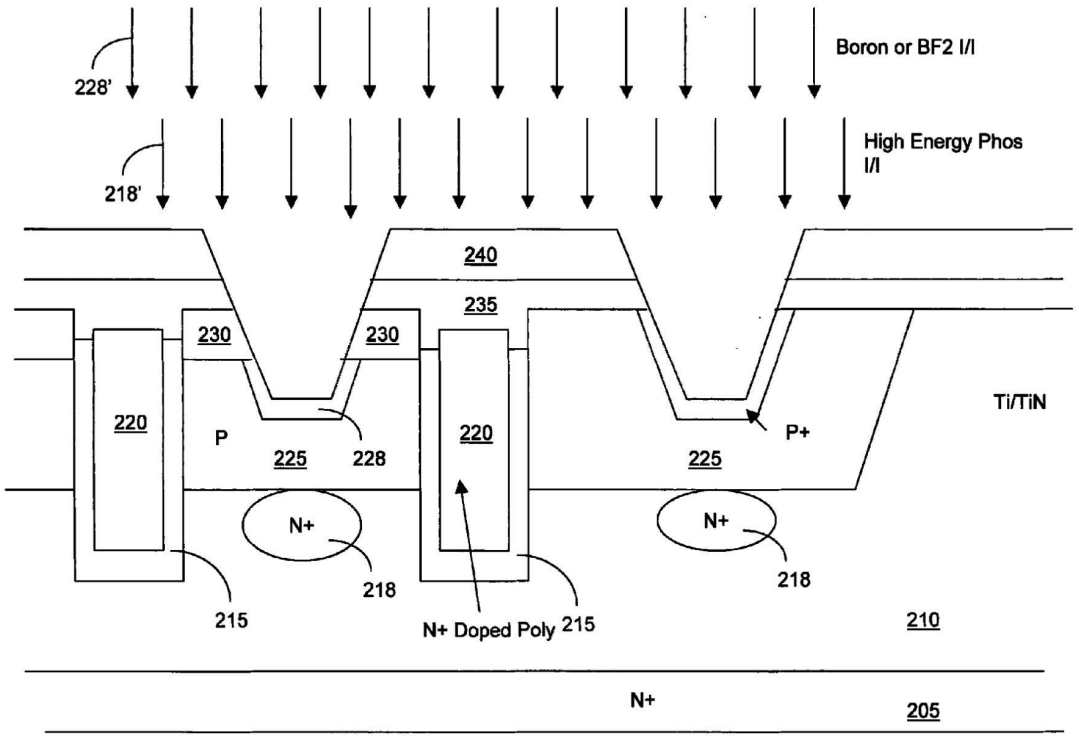


Fig. 9G

321. Hshieh ('384) explains that the doping contact layer—labeled as element 128/228 in the figures—is created by a "Boron or BF_2" implant (element 228'). Hshieh ('384) also explains why the implant is done straight-on to the structure (rather than at an angle), and what results:

> In FIG. 9G, a boron or BF2 implant with P+ ions 228 is first performed to form the P+ doped region 228 to surround the trenches 224. The implantation is carried out along a direction of zero degree relative to a

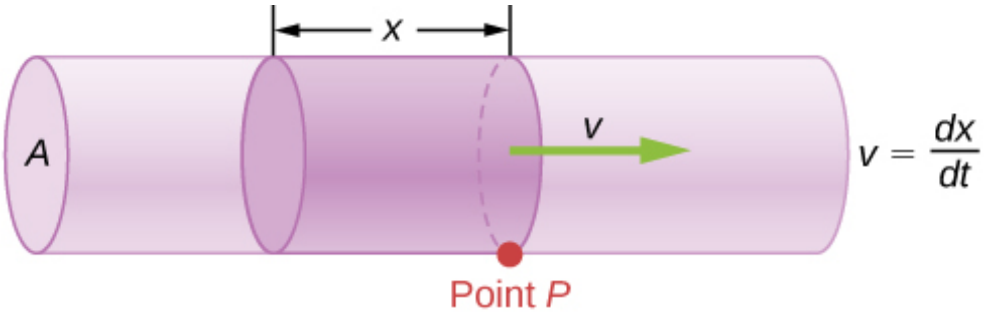
> perpendicular direction relative to the substrate top surface because the sloped sidewalls of the contact trenches 244. (Ex. 1005, Hshieh ('384), ¶[0035].)

322. The second (and final) sentence of this paragraph makes clear what is going on–that because the sidewalls of the trench are sloped, the straight-on (i.e., "zero degree relative") implantation direction will cause both the bottom of the trench and the sidewalls of the trench to receive the implanted dopants–and to a degree sufficient to make those regions be sufficiently doped to provide the desired complete heavily-doped-p-type coverage for the surface where the source contact will meet the body region.

323. However, it would be obvious to a POSITA that the concentration of dopants in this configuration would be less on the sidewalls of the trench than on the bottom of the trench–because of some very simple aspects of basic geometry.

324. I will first explain this physical phenomenon using terms and concepts familiar to a POSITA, and then simplify the concept by presenting two analogies that may be more accessible to a lay audience. Finally, process simulations will be presented to confirm what happens in the silicon during processing.

325. Consider a flow of matter or energy that is areally-uniform–that is, the same amount of matter or energy is flowing per-unit-area through a cross-section that is perpendicular to the one-dimensional flow of that matter or energy. (*See* illustrative image below.)



$$v = \frac{dx}{dt}$$

$$Q = \frac{dv}{dt} = \frac{d}{dt}(Ax) = A\frac{dx}{dt} = Av$$

326. Note that atoms flowing out of an ion-implantation apparatus are (to a good approximation at least) behaving in this way–as is reflected in the use of a quantified "dose" of such atoms per unit area (e.g., being implanted with a dose of 1.5×10^{14} ions/cm²). (*See* illustrative image below.)

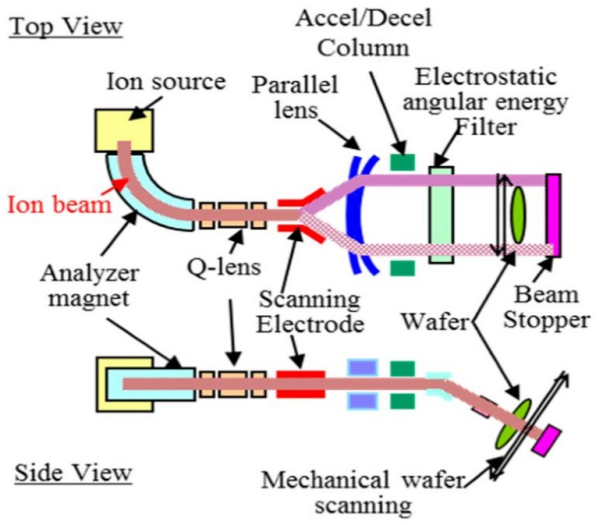


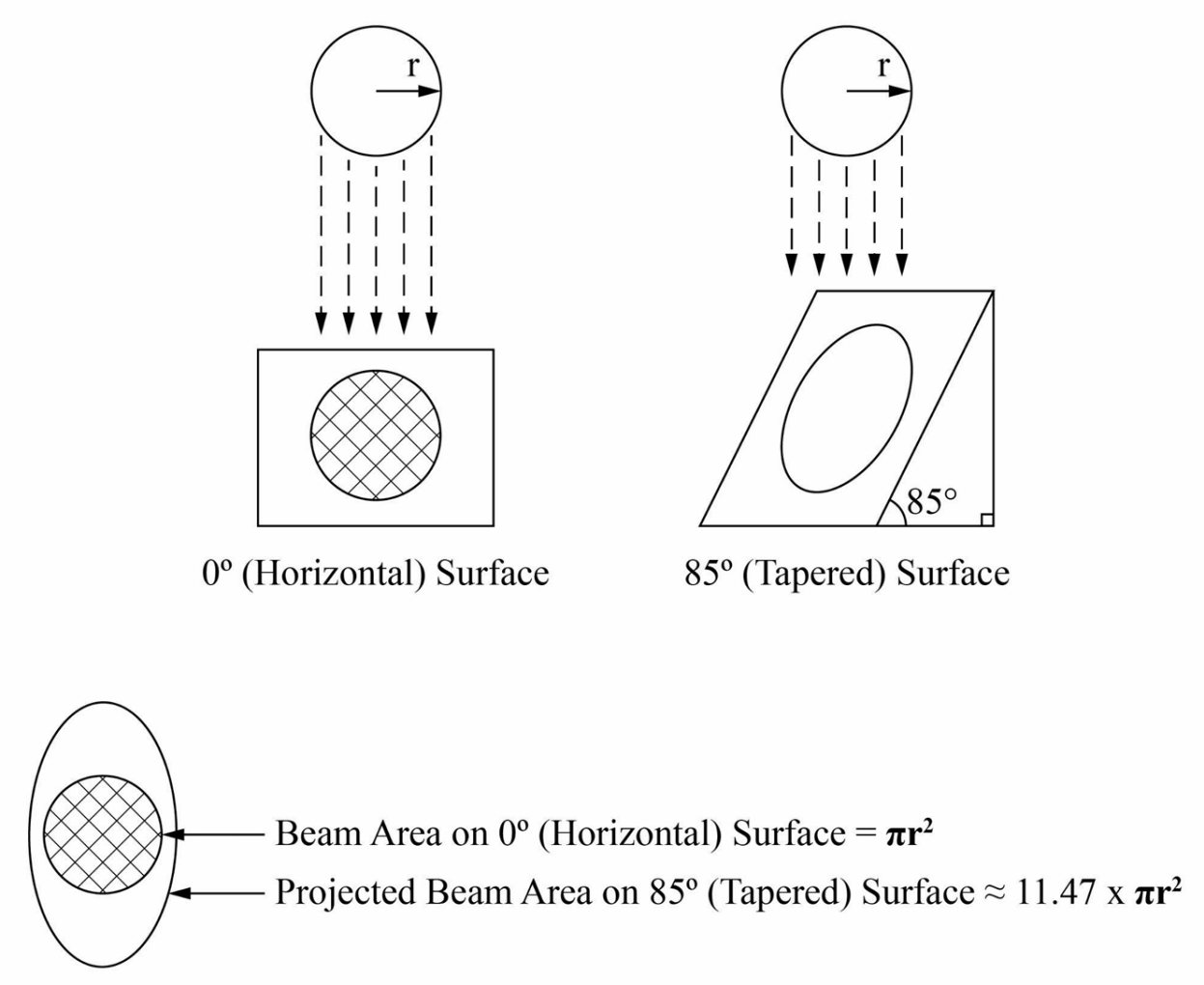
Figure 2. The top view and side view block diagrams of a medium current ion implanter, NV-MC3-II, of SMIT [14].

327. When the implantation ion stream strikes a flat surface perpendicular to that stream, that stream will impact the surface with an areal density equal to the

flux density of the stream. However, when that stream strikes a surface that is not perpendicular to that stream, then the areal density of that stream on the surface will be less than in the perpendicular case–since that flux density will strike a larger area on that surface.

328. This can readily be observed in the depiction below, and it follows that the steeper the angle of incidence, the more spread out the stream becomes at the surface—resulting in a lower density of particles or energy striking the surface per unit area.

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Just as the sun's rays feel more intense when directly overhead but spread out and weaken when striking at a shallow angle—as during sunrise or sunset—the same principle applies here.

329. I have been provided with the trial transcript in the case *Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG. (*See* Ex. 1019, *Force Mos Technology, Co. Ltd. v. AsusTek Computer, Inc.*, 2:22-cv-00460-JRG, E.D. Tex. (Marshall) 2022, ECF No. 416, 143, 146-147 (Ex. 1019, Trial

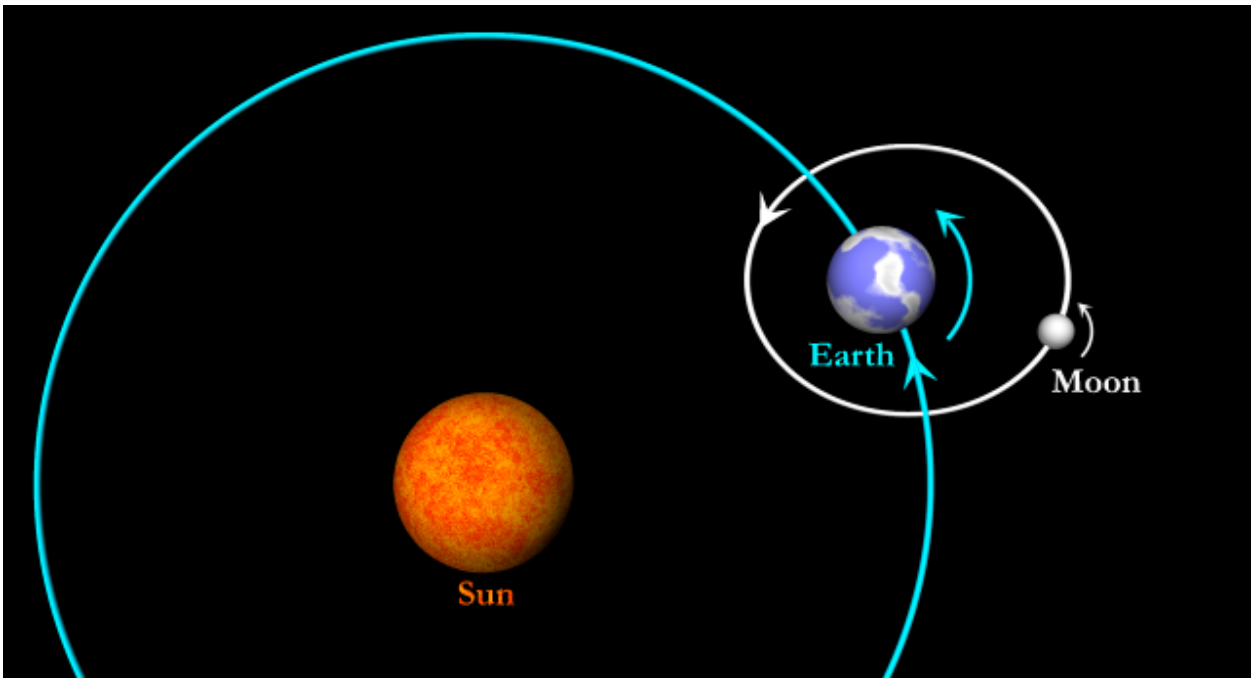
Transcript Excerpt). On pages 143 and 146-147 of the transcript, the patent owner's expert used the analogy of the ion implantation process being similar to rain falling on the bottom and sidewalls of the source contact trench, thereby naturally resulting in lesser doping concentration along the sidewalls and more at the trenched bottom. Patent Owner's expert, Dr. Neikirk, explained:

> "[a]nd just like when it's raining, if you stand up, your sides, your sidewalls, they'll get wet, but they won't get soaked; whereas, if you lay down, when you're horizontal, you'll get soaked. So you end up with many more dopants here than you do here." (*Id.* at p. 143).

> "Again, this is fine along with the ion implantation explanation. Again, the sidewalls receive dopants, but fewer than the bottom. The base region, the body region, establishes the reference for P. So the sidewalls are implanted and their doping concentration is greater than P. But, again, the bottom receives a great deal more doping. That would establish a reference for P+. The requirement for a lateral contact layer is that it be doped between P and P+, otherwise called by the patent P*. And the characteristics of the implant process in this geometry will produce such a lateral contact layer." (*Id.* at p. 146-147 (*referring to a tapered source contact trench geometry*)).

This analogy is consistent with the geometric explanation provided above, and supports the inference discussed therein—that a lower doping concentration would be expected along the sidewalls of a tapered trench.

330. Another (and perhaps clearer) analogy would be the flux density of radiation from the Sun (i.e., sunlight) striking the Earth: (*See* illustrative image below.)

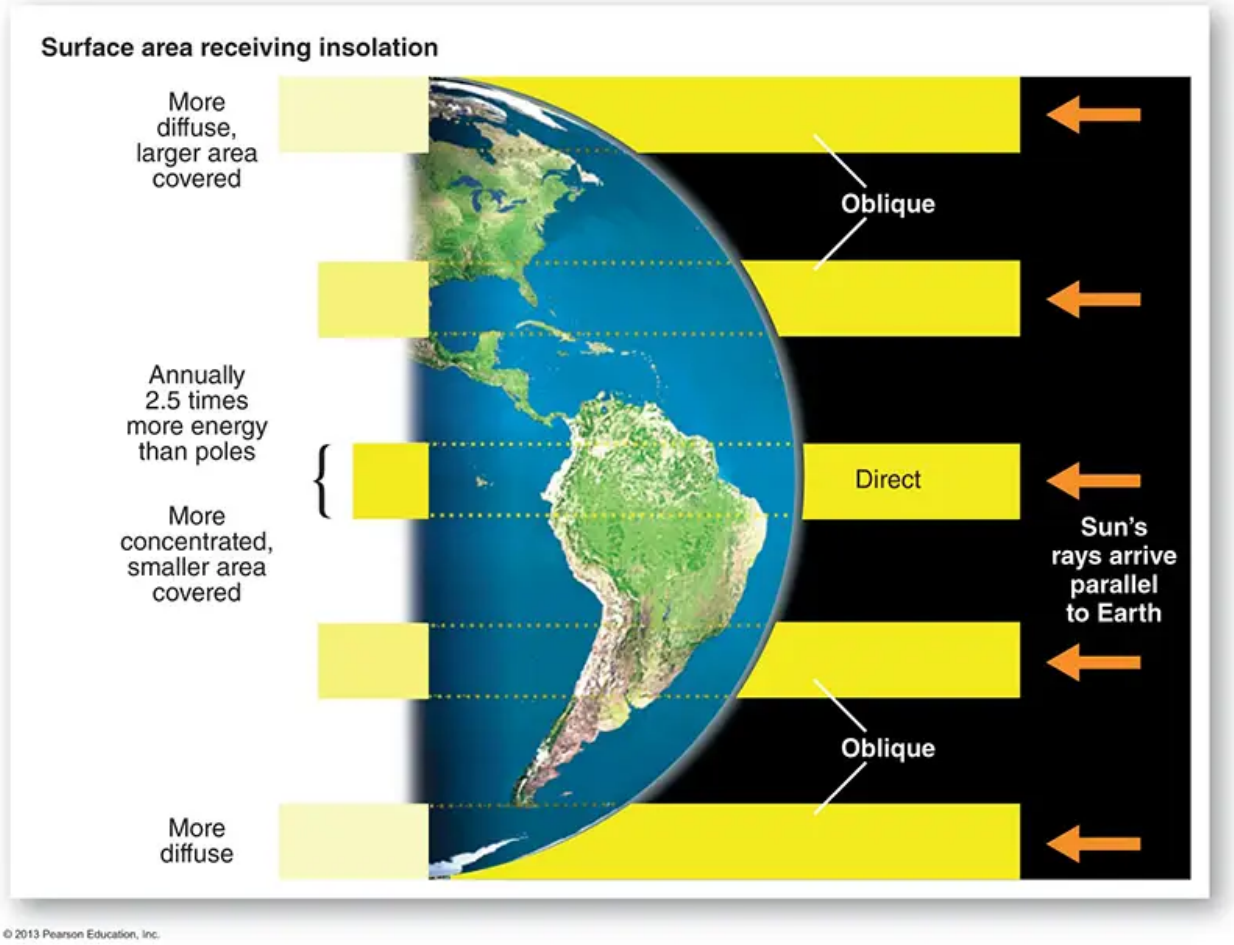


Because the Earth is, to a reasonable approximation, a sphere, it presents what appears to be a flat circular cross-section when viewed from the Sun. An observer viewing from that perspective might incorrectly conclude that the density of the incoming solar radiation—specifically, its flux density—is distributed uniformly across the entire sunlit surface of the Earth.

331. However, because the Earth is a sphere, the flux density at its surface is not uniform. This variation arises from the fact that solar radiation strike different points on the Earth's surface at different angles of incidence, depending on geographic location. At locations where the solar radiation strikes the surface perpendicularly (i.e., at normal incidence), the flux density at the surface is equal to the flux density of the incoming solar radiation. At all other locations, where the

sunlight arrives at an angle, the same amount of solar energy is spread over a larger surface area, resulting in a reduced flux density.

332. It is well understood that as one moves north or south from the equator, solar radiation strikes the Earth's surface at increasingly oblique angles—that is, the angle of incidence becomes steeper the farther one moves from the equator toward higher latitudes. (*See* illustrative image below.)



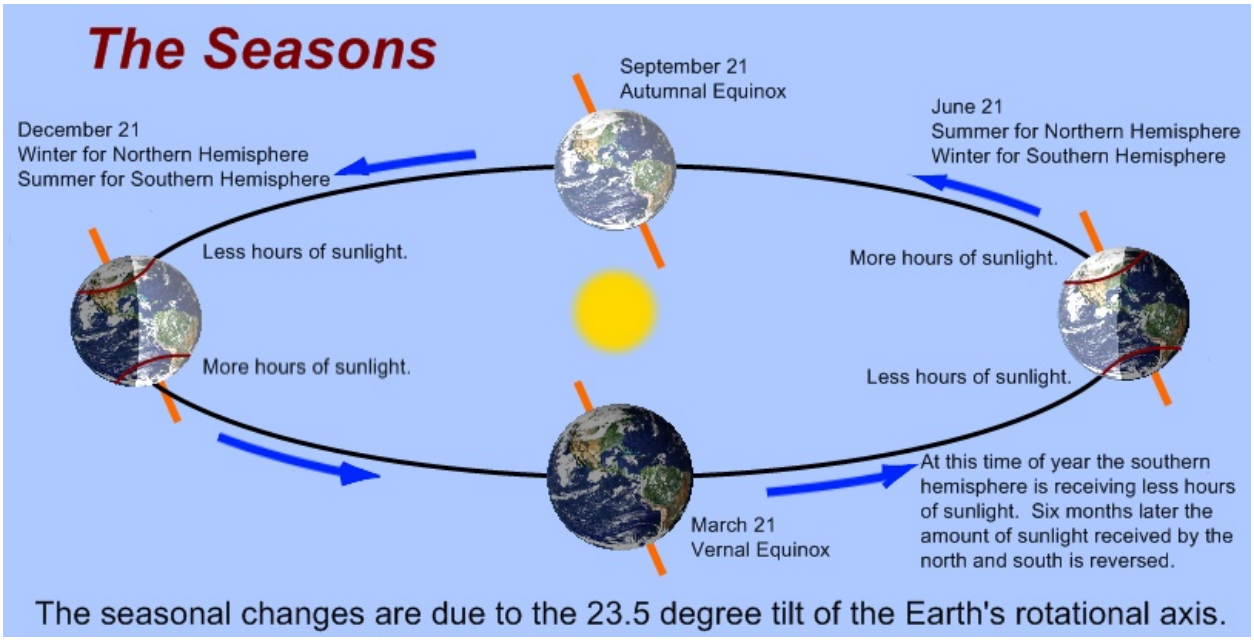
Therefore, the solar radiation striking the Earth per unit area at such points will be less than at the point where the solar radiation strikes the Earth at a

perpendicular angle–as per the explanation above regarding the basic geometry behavior when an areally-uniform flux of particles or energy strikes a surface at a non-perpendicular angle.

333. When it comes to the Earth, this configuration has two dramatic consequences.

334. First, because sunlight is more concentrated (i.e., more direct) when it strikes the surface at or near a perpendicular angle, regions closer to the equator receive more intense solar radiation and are therefore warmer—these are the tropical regions. In contrast, regions farther from the equator receive sunlight at steeper angles, causing the same energy to be spread over a larger area, resulting in lower flux density and colder climates—these are the polar regions.

335. Second, the Earth's axial tilt, combined with the geometric behavior described above, causes the location of the "perpendicular point" (where the sun's rays strike the Earth most directly) to shift over the course of the year. As the Earth orbits the Sun, this point migrates between approximately 23.5° north latitude at the June solstice and 23.5° south latitude at the December solstice, producing the seasonal variation in solar exposure. (*See* illustrative image below.)



336. When sunlight strikes the Earth more directly, it results in summer; when it strikes at a more oblique angle, it results in winter. This difference in solar angle also explains why summer and winter occur at opposite times of the year in the northern and southern hemispheres.

337. In the same way, as discussed above, the concentration of dopant atoms at a surface will be lower when implantation occurs at a steeper angle. Accordingly, it is inherent in the teachings of Hshieh ('384) that the sidewalls of the trench—i.e., within the lateral contact layer—will receive a lower concentration of dopants compared to the base contact layer, where implantation occurs at or near normal incidence. Because this outcome follows directly from geometric principles governing ion implantation, it would have been obvious to a POSITA that the "lateral contact layer" would exhibit a lower dopant concentration

than the "base contact layer." Thus, this claim element is rendered obvious by the inherent structure disclosed in Hshieh ('384), in view of basic and well-known implantation behavior.

338. As discussed above, Hshieh ('384) teaches a nominal (i.e. perpendicular) ion implantation dose on the entire bottom and tapered sidewalls of the source contact trench within the base layer, to achieve a known result of providing a low-resistance ohmic contact between the metallic source contact plug and the body region. (*See* Ex. 1005, Hshieh ('384), ¶[0035].) While Hshieh ('384) labels this region as "P+", for the reasons discussed above, it would be obvious to a POSITA that the tapered sidewalls (i.e. "lateral contact layer") have a lesser doping concentration than does the trench bottom (i.e. "base contact layer"), due to the angle of incidence of the implant. Accordingly, Hshieh ('384) teaches the '634 Patent's requirement that the "lateral contact layer" has a lower doping concentration than the "base contact layer."

339. To further confirm this inherent result—when a straight-on ion implantation, is performed into a tapered trench structure using typical ion implantation parameters that are employed when forming shallow heavily-doped regions in silicon—I provided parameters to Petitioner, through their attorneys, for use in a commercial process simulation program, Victory Process (version 8.42.5.R) by Silvaco Inc. This "computer experiment" modeled ion implantation

into a tapered trench structure and enabled precise identification and quantification of the resulting doping concentration at any point in the structure, with particular focus on the lateral contact layers and the bottom contact layer. The simulation employed a "Monte Carlo" method, in which ions are simulated individually, with each trajectory determined by the statistical and probabilistic interactions that occur when an incoming ion strikes the silicon structure. By repeating this single-particle simulation many times, the statistical behavior of the entire implantation is determined and, when combined with the overall implant dose, used to calculate the doping concentration at any location within the silicon. Monte Carlo methods are commonly used for process simulation - such as for modeling the doping profiles and doping concentrations produced by ion implantation.

340. This simulation was conducted using ion implantation parameters that are typically used for creating shallow heavily-doped (i.e., p+ or n+) regions in silicon, and were applied to the tapered-trench structure of Hshieh ('384) as depicted in Fig. 9G:

Ex. 1005 ('384 Hshieh)

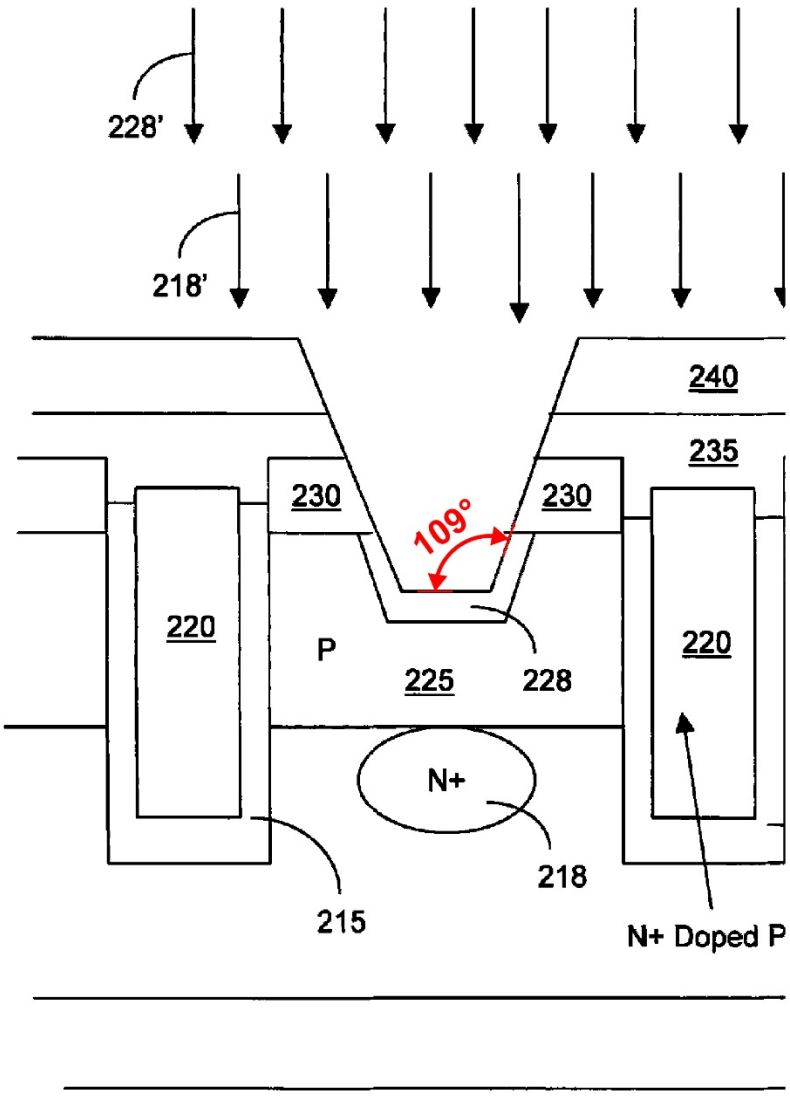


Fig. 9G (Annotated partial enlarged view)

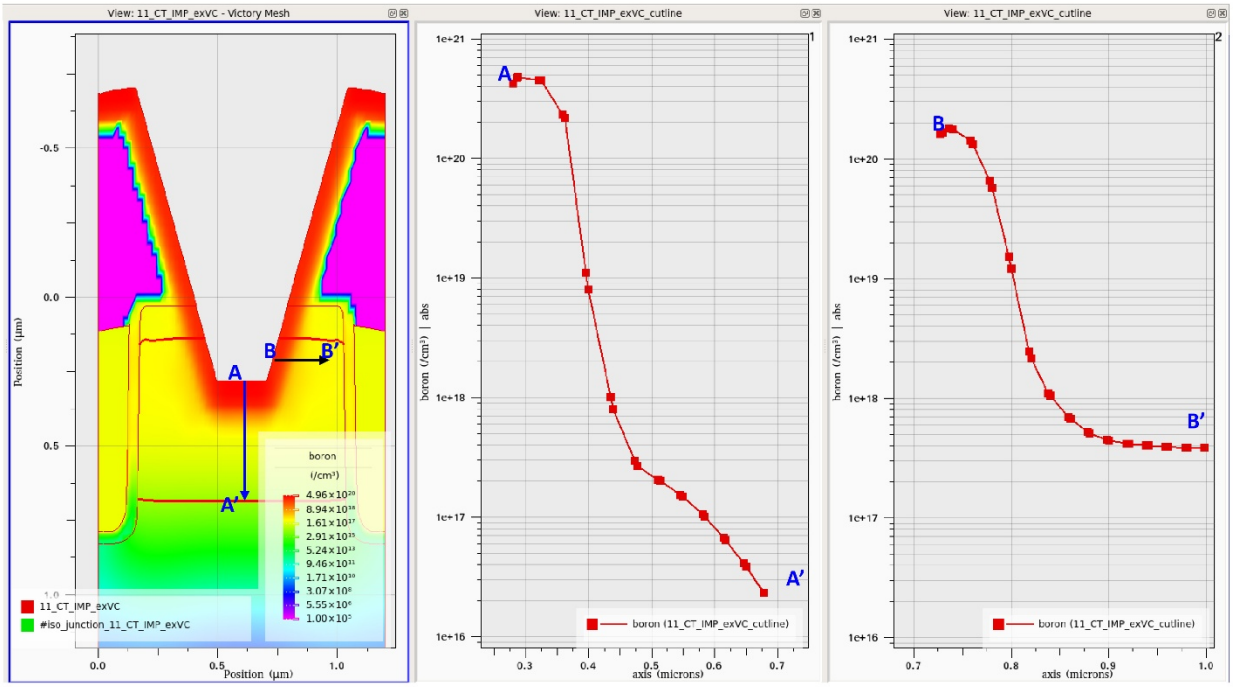
- A tapered contact trench angle of 109 degrees, as measured from Fig. 9G of Hshieh (’384) (and as shown in the annotated figure above);
- The implant species used was BF2 (Ex. 1001 3:50-54) - an implant species commonly-used to implant boron atoms into silicon.

- The implant dose was 5.0×10^{15} cm^{-2}; this dose was selected because it is in the typical range that is used for forming P^+ layers in silicon.
- The implant energy was 20 keV - which is a typical energy used for implants that are to be concentrated near the targeted surface (rather than having the doping peak below the targeted surface);
- The implant angle was 90 degrees to the surface defined by the bottom of the trench and the surfaces of the other layers (such as the surface of the epitaxial layer);
- As mentioned above, the simulation method chosen was one using a Monte Carlo method.

The simulation results produced are summarized in this set of figures:

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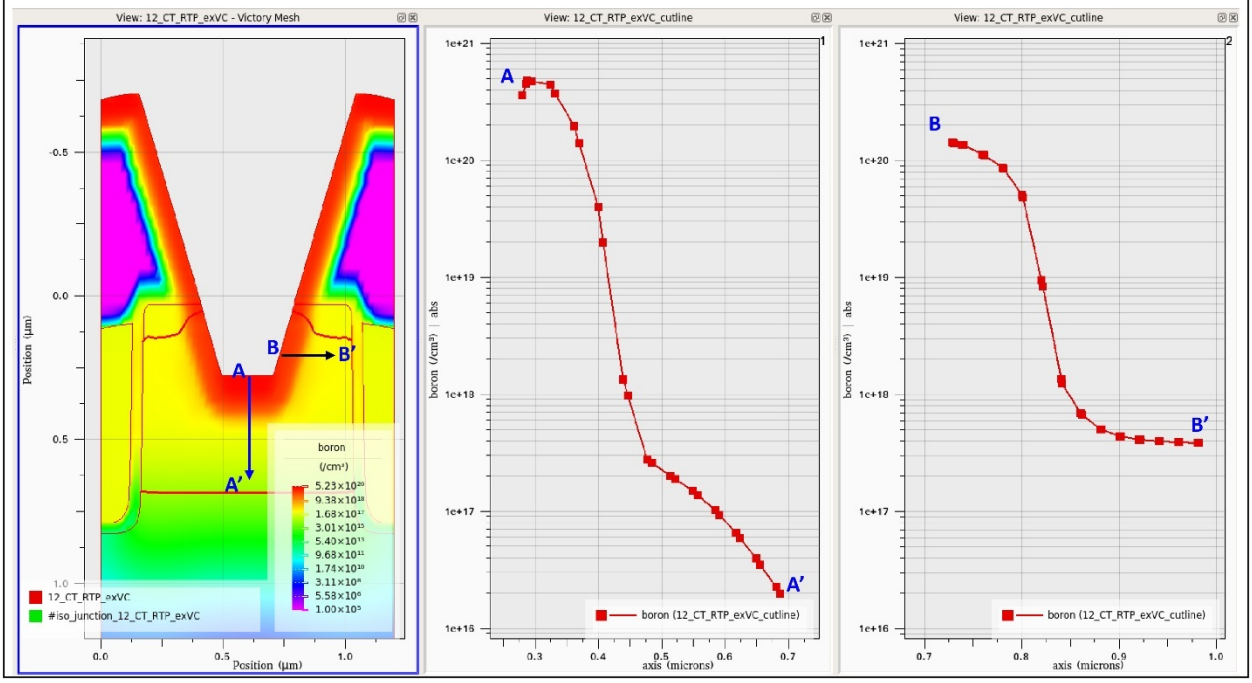
Monte Carlo Simulation: Ion Implantation (IMP) on MOSFET with 109°-tapered trench — Implant Species: BF2; Dose: 5 × 10^{15} cm^{-2}; Energy: 20 keV; Implant Angle: 90° (relative to epitaxial layer)



As can be seen from the left-hand figure, both the silicon at the bottom of the trench and the silicon of the trench sidewalls are sufficiently-doped to provide a p+ doping layer in the silicon - as the doping concentration is everywhere clearly higher than the minimum doping level of $5.0x10^{19}$ cm^{-3} required to create p+-doped silicon. Further, as the cross-sectional doping profiles along the lines A-A' and B-B' show, the doping concentration at-and-below the bottom of the trench is about $5.0x10^{20}$ cm^{-3}, while the doping concentration at-and-within the sidewall surfaces is about $2.0x10^{20}$ cm^{-3}; these results show that in the structure and with the methods taught by Hshieh ('384) (as well as, in fact, by the '634 patent), the p+ lateral

contact layer (on the trench sidewalls) will inevitably have less doping concentration than does the p+ base contact layer at the bottom of the trench. For completeness, I also had the simulation above extended, by including a post-implantation heat cycle of the type typically used in silicon processing - using the same software, and employing a typical (in fabrication) rapid thermal annealing at 1000°C for 15 seconds; as noted above, this sort of heat cycle is commonly-used to heal any damage done to the silicon crystal lattice by the ion implantation, and to activate the dopant atoms (i.e. to allow them to function as dopant atoms).

Monte Carlo Simulation: Ion Implantation (IMP) followed by Rapid Thermal Annealing (RTA) on MOSFET with 109°-tapered trench — Implant Species: BF_2; Dose: 5×10^{15} cm^{-2}; Energy: 20 keV; Implant Angle: 90° (relative to epitaxial layer); 1,000°C for 15 seconds



These simulation results further confirm that the heat cycle is used principally for the purposes described above (rather than to diffuse dopant atoms and spread them out in the silicon) - as with or without the heat cycle, the outcome (in terms of doping concentrations and locations) is the same: that is, once again, the lateral contact layer has a lower doping concentration than does the base contact layer, the lateral contact layer has higher doping concentration than does the base layer (i.e., the body region(s)), and both the base contact layer and the lateral contact layer have the p+ doping concentrations that are required for the provision of a low-resistance ohmic contact between these doped contact layers and the source contact metal. A POSITA would recognize this result as reflecting an inherent physical principle - as a direct consequence of the basic geometry involved in ion implantation into planar surfaces at differing angles of incidence.

341. With regard to the use of vertical-sidewall trenches (rather than tapered-sidewall trenches) for the source-body contact, Hshieh also considers this situation with respect to the creation of the p+-doped region that "surrounds" the source-body contact metal plug–and depicts this "surrounding" doped region as being created using angled ion implantation:

Ex. 1005 ('384 Hshieh)

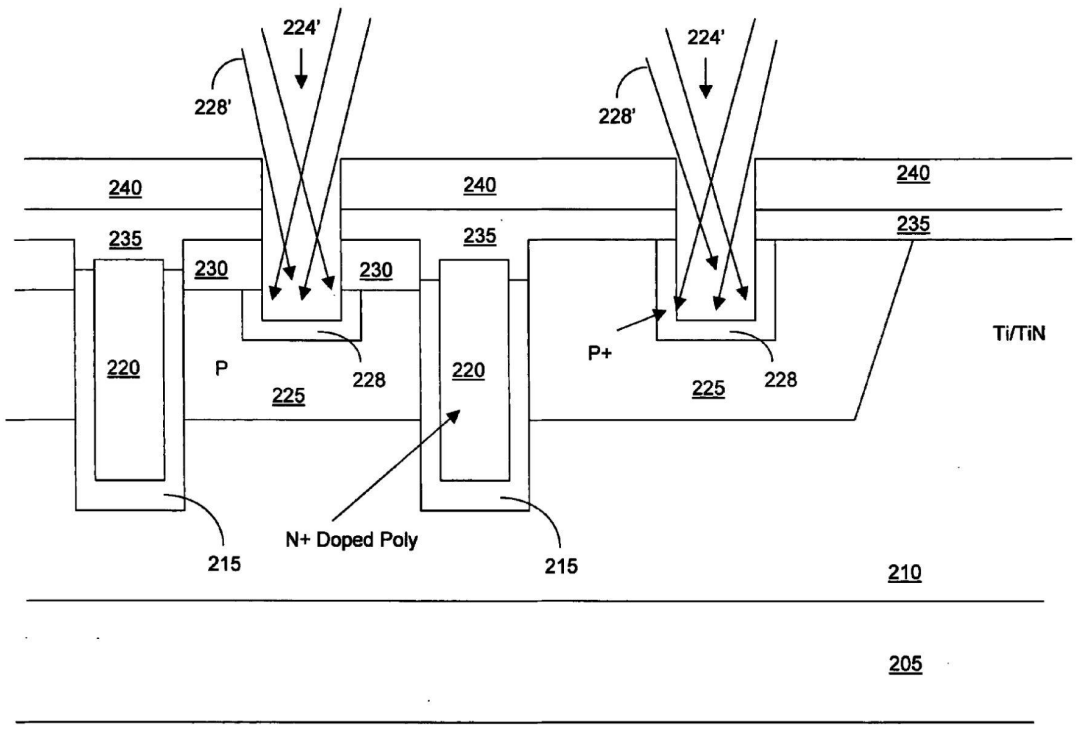


Fig. 9G'

Particularly in the early days of the use of trenches (both shallow trenches and deep trenches) in silicon, the reactive ion etching (RIE) processes that were in use produced trench sidewalls that were tapered rather than vertical (as can be seen in several references cited in Section VII.C); however, when the trenches were "deep" (that is, the trench depth was much larger than the trench width) and the sidewalls were thus quite vertical (since if the etch process produced shallow angles, it would be impossible to etch a deep trench), the angle of the sidewalls was too steep to allow for proper doping of the trench sidewalls via direct, straight-on ion implantation. This led to the use of angled ion implantation to dope trench

sidewalls - something that has long been known in the art. (*See* Ex. 1020, Genshu Fuse et al., *Indirect Trench Sidewall Doping by Implantation of Reflected Ions*, Applied Physics Letters Vol. 54, 1534-1536 (1989).)

342. However, even with the use of angled ion implantation, it has also long been known that it is difficult, using ion implantation, to produce doping concentrations that are uniform around the implanted sides of the trench (i.e., the bottom of the trench and the sidewalls of the trench will have different doping concentrations). A major mechanism that induces this problem is simply that some of the ions striking the sidewall of the trench will not penetrate into the silicon–but rather will "reflect" off the sidewall and travel on to elsewhere in the structure.

343. This problem has been detailed numerous times in the prior art literature.

344. This long-running problem is described nicely in Ex. 1021, S. E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 4 (2003):

> The most important difficulty in controlling the distribution and homogeneity of the dopant concentration is the scattering effect of ions at the trench sidewalls due to the impact of the ions with sidewall atoms.

345. Fuse et al., *Indirect Trench Sidewall Doping*, Vol. 54 Appl. Phys. Lett. at 1535 (1989), which was cited above and is prior art to the '634 patent,

considers this problem in detail–and depicts this reflection of ions off of the sidewalls of the trench, as described above:

Ex. 1020, Genshu Fuse et al., *Indirect Trench Sidewall Doping by Implantation of Reflected Ions*, Applied Physics Letters, vol. 54, 1534 Fig. 1 (1989)

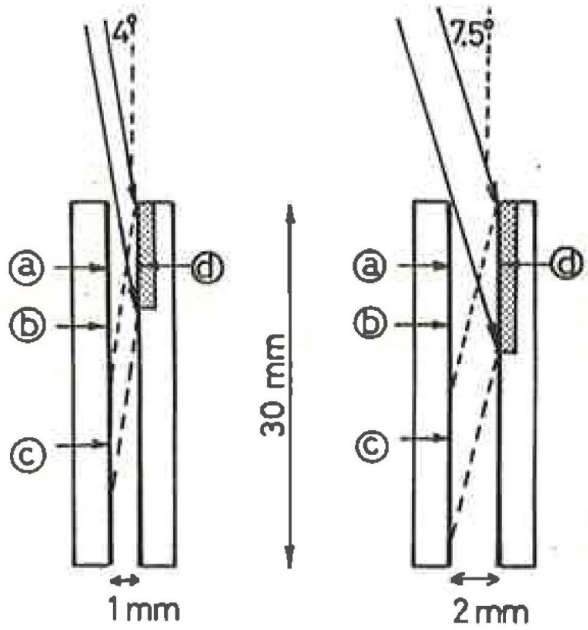


FIG. 1. Schematic arrangements of samples for depth profile measurement by complementary experiments of trench sidewall doping.

(*See* Ex. 1020, Genshu Fuse et al., *Indirect Trench Sidewall Doping by Implantation of Reflected Ions*, Applied Physics Letters, Vol. 54, 1534 Fig. 1 (1989).)

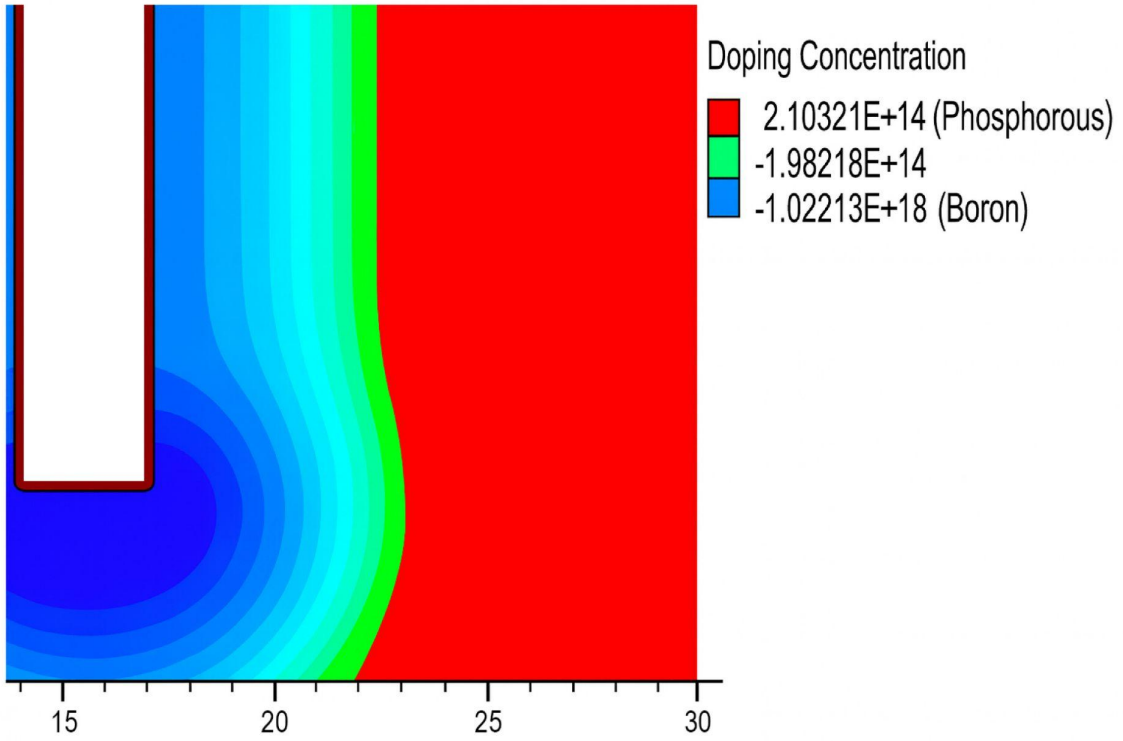
Note in particular that if the sidewall region that is being doped is the sidewall portion adjacent to the bottom of the trench, the reflected ions will be directed into the silicon at the bottom of the trench–increasing the doping

concentration there (while the "lost" ions will cause the doping of the sidewall regions to be lower).

346. It should also be noted that, by the time of the '634 Patent, the existence of differing doping concentrations between the vertical sidewalls and the bottom of a trench was well recognized in the field and had become a subject of focused research and optimization. As illustrated above in Fig. 1 of Fuse (1989), ion implantation naturally produces a non-uniform doping profile, with lower concentrations along the sidewalls due to the angle of incidence. This inherent profile was not only well known but also accepted as a feature of the process. Reflecting this recognition, researchers by the early 2000s were actively exploring how to leverage and refine these doping gradients for improved device performance. (*See* Ex. 1021, S.E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 5 (2003)) In that study, the authors propose an "optimized sidewall doped trench structure," and Fig. 8(a) clearly illustrates that their optimized profile includes a lower doping concentration along the trench sidewalls (light blue) relative to the trench bottom (dark blue). The researchers specifically identify this non-uniform profile—where the sidewall doping lies between that of the base contact region (dark blue) and the surrounding base layer (red)—as optimal for achieving effective device performance. This research confirms that varying

doping concentrations between trench sidewalls and trench bottoms were not only in existence prior to the ’634 Patent, but were actively studied and deliberately utilized in silicon process engineering.

Ex. 1021, S.E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 5 Fig. 8 (2003)



347. This body of research demonstrates that trench sidewalls with lower doping concentrations than the trench bottom were already well-understood and incorporated (either purposefully or simply tolerated as a consequence of the situation) into transistor design by the early 2000s. Such doping profiles—resulting from the geometric realities of ion implantation—were not only expected, but were

also considered advantageous in certain contexts. Researchers developed and explored various methods for refining and controlling this non-uniformity, recognizing its influence on device behavior. For example, one such technique involved outdiffusion from a borosilicate glass (BSG) layer deposited into the trench and subsequently removed after the diffusion process. (*See* B. Davari et al., A Variable-Sized Shallow Trench Isolation (STI) Technology with Diffused Sidewall Doping for Submicron CMOS, Proceedings of the International Electron Devices Meeting, pp. 92–95 (1988).) Another technique developed by at least 2006—originally referred to as "Plasma Immersion Ion Implantation" and now more commonly known as PLAD ("Plasma Doping")—was developed as a method of providing better control of doping profiles within trenches. (*See* Ex. 1025, S. Nizou et al., *Deep Trench Doping by Plasma Immersion Ion Implantation in Silicon*, Ion Implantation Technology: 16th International Conference on Ion Implantation Technology, 229–232 (2006).) These examples confirm that, by the time of the '634 Patent, the existence of lower doping concentrations along trench sidewalls (relative to doping concentration at the trench bottom) was widely known–and had become a focus of active research and process engineering. Given this understanding, it is clear that the '634 Patent merely describes an inherent and well-understood physical characteristic that naturally arises from conventional fabrication techniques that were in widespread use at the time of the invention.

348. As explicitly described in the ’634 Patent, the lateral contact layer is formed along the sidewalls of the source contact trench above the trench bottom within the base layer, while the base contact layer is formed at or beneath the trench bottom. (*See* Ex. 1001, ’634 Patent, 5:9–12; 3:50–55.) Because Hshieh (’384) discloses tapered trenches (e.g., the Fig. 3 embodiment), the sidewalls are angled rather than vertical–and as explained above, perpendicular ion implantation into these sidewalls results in a lower effective dopant dose per unit surface area than is the case at the horizontal trench bottom. This occurs because the effective flux density of the ion beam (*i.e.*, the number of ions striking per unit surface area) is reduced on angled surfaces relative to flat, horizontal surfaces—resulting in a lower concentration of implanted dopants on the trench sidewalls.

349. The trench bottom, by contrast, receives ions at a direct angle and thus, in effect, over a smaller area–which yields a higher doping concentration. Consequently, as also explained above, the P+ region along the sidewalls (i.e., the lateral contact layer) inherently receives less dopant per unit surface area than does the base contact region at the trench bottom. This result is dictated by general physical and mathematical/geometrical considerations, as well as the basic physics of ion implantation and trench geometry; as explained in Section V.A.5, this does not require explicit recognition in the prior art. Accordingly, Hshieh (’384)

inherently discloses a lateral contact layer with lower doping concentration than that of the base contact layer.

350. For completeness, it should be noted that–as described earlier–the goal for the entire region where the metal source contact plug meets the body region is to have present a p+ layer (or, in the pMOS transistor instance, an n+ layer) across that entire meeting surface. That this can be done in this situation is also well-known in the art–and thus would be obvious to a POSITA.

351. For a silicon region to be considered to be "heavily-doped" as either n+ or p+ (and thus having so many carriers that its electrical behavior is quasi-metallic rather than semiconducting), the doping concentration must be above a particular level (above a level of about 5×10^{19} atoms per square centimeter, with a level of about 1×10^{20} being what is typically implemented). As silicon doped more-strongly that this level will still be "p+"-doped, it would have been obvious to a POSITA that the entire contact layer (comprising both the base contact layer and the lateral contact layer) should be sufficiently-doped to allow the lateral contact layer to be considered to be "p+"–with the resulting higher doping concentration in the base contact layer also being "p+." It would be a simple matter for a POSITA to use the slope angle of the trench sidewall to calculate an ion implantation dose that would produce a suitably-p+ dopant concentration in the sidewalls–with the resulting higher doping at the bottom still providing a suitable

p+ layer there. In fact, this is exactly what the Monte Carlo process simulations results presented above show - that while the doping concentration on the sidewalls is less than the doping concentration on the bottom of the trench, both regions have a doping level that qualifies them as being "p+" - making both of them suitable for the provision of a p+ layer that will provide a low-resistance ohmic contact between the body region of the silicon and the metal of the source contact. Further, a POSITA would already know that a typical implant dose used to form a simple p+ pocket in silicon (such as for the source and the drain of a pMOS transistor) would be about 1E15 - 2E15 cm-2; however, for the tapered-trench scenario, the simulation results confirm that a higher implant dose (in the simulations, 5E15 cm-2) would be chosen to ensure the creation of a complete set of p+ layers on both the trench bottom and the trench sidewalls.

For these reasons limitation [2d] is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

4. Claim 3: "The trenched MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

352. Claim 3 is a dependent claim–and depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2 and Section

XI.A.3) that Claim 1 and Claim 2 of the ’634 Patent are either taught by Hshieh (’384) or rendered obvious by Hshieh (’384) and the knowledge of a POSITA.

353. The remainder of Claim 3 is taught by Hshieh (’384).

Ex. 1005 ('384 Hshieh)

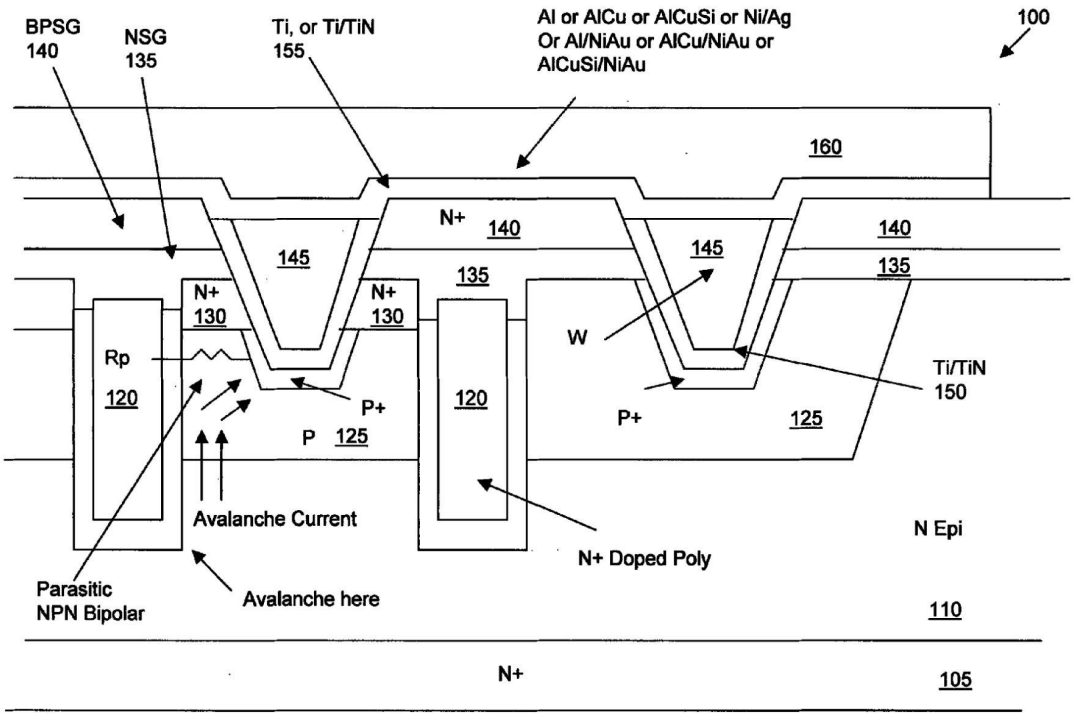


Fig. 3

a. [3a]: “barrier metal layer”.

354. Limitation *[3a]* is disclosed in Hshieh (’384), which provides a barrier metal layer corresponding to element ’634-110/210 of the ’634 Patent. The ’634 Patent describes the barrier metal layer as an intermediate conductive layer that lines the contact opening and surrounds the tungsten plug, functioning to prevent

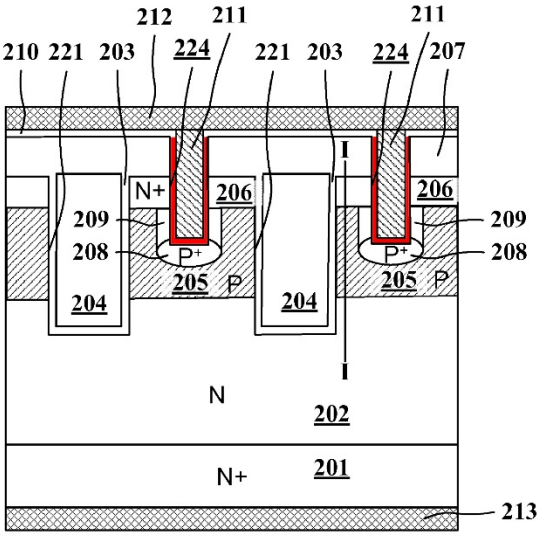
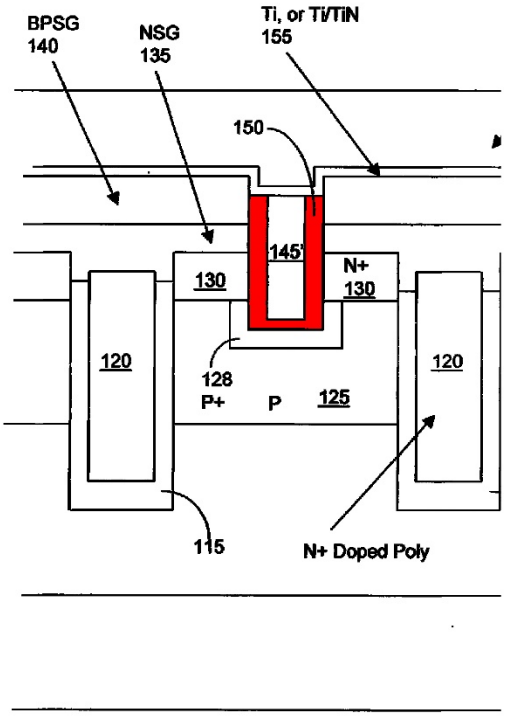
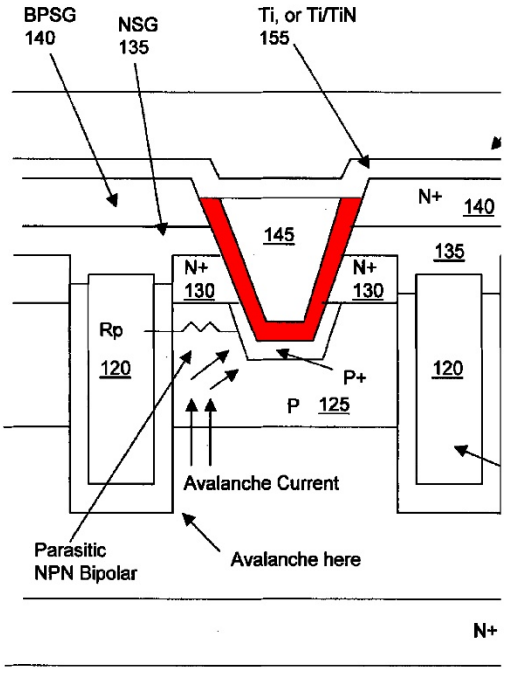
diffusion and also to maintain contact integrity (e.g. adhesion). (*See* Ex. 1001, '634 Patent, 4:9–23; *see also* Figs. 2F–2G.)

355. Hshieh ('384) discloses the same structural and functional element. Specifically, it describes a barrier layer 150 (or 245 in alternate embodiments), which surrounds the tungsten source plug (element 145/250) within the trenched source contact. Hshieh ('384) states that "a plurality of trenched source contact *[sic]* filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is formed. (*See* Ex. 1005, Hshieh ('384), ¶[0027]; *see also* Figs. 3–8, elements 145 and 150.) In an alternative embodiment, the barrier layer is labeled as element 245 surrounding tungsten plug 250. (*Id.* ¶[0035]; Figs. 9H–9J.)

<*This space intentionally left blank.*>

[3a]

barrier metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

356. To the extent that the ’634 barrier metal layer (’634-110/210) could be understood to extend over the interlayer oxide film (’634-107/207), as illustrated in figures such as Fig. 2G of the ’634 Patent, Hshieh (’384) discloses an identical structure. Specifically, Hshieh (’384) describes: “A low resistance metal layer 255 is deposited over the top surface. The low resistance metal layer may be composed of Ti or Ti/TiN to assure good electric contact is established.” (*Id.* ¶[0035]; *see also* Figs. 3–8, 9J, elements 155 and 255.)

357. The barrier layer in Hshieh (’384), made of Ti/TiN, performs the same role as does the ’634 Patent’s barrier metal layer–it prevents metal diffusion and improves adhesion of the plug to the structures below it by interposing this barrier metal layer–that is, the barrier layer provides both an adhesion layer (for the metal of the contact plug) and *physical* isolation of the plug, without affecting the electrical behavior of the plug. This structure matches both the placement and purpose of element ’634-110/210.

358. Accordingly, Hshieh (’384) discloses a barrier metal layer surrounding the tungsten plug and formed between it and surrounding materials and therefore teaches limitation *[3a]*.

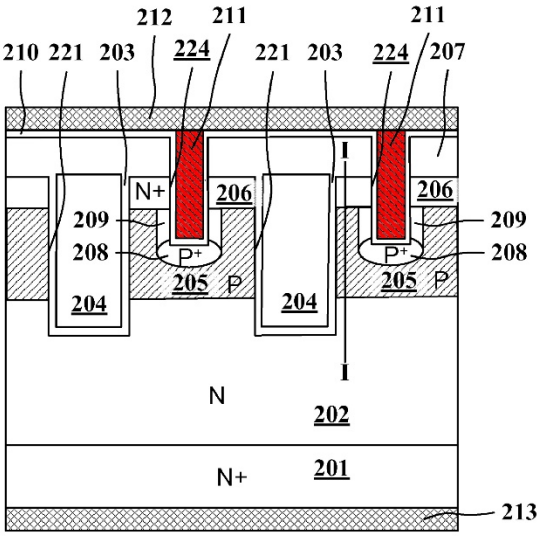
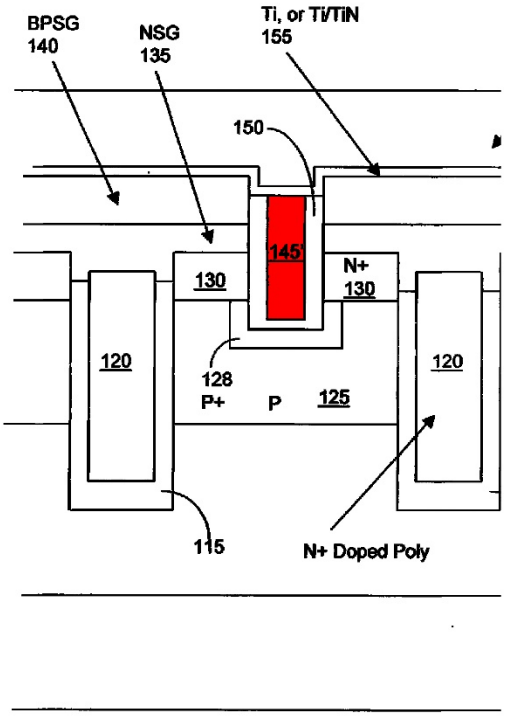
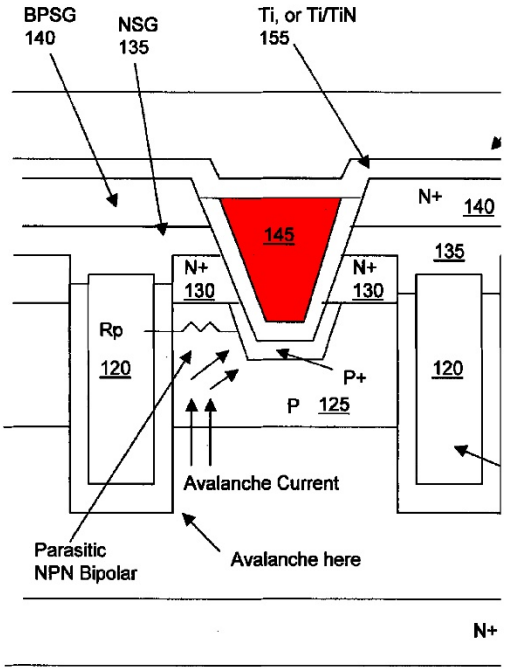
b. [3b]: "contact metal plugs".

359. Limitation *[3b]* is disclosed in Hshieh ('384), which provides contact metal plugs corresponding to element '634-111/211 of the '634 Patent. The '634 Patent identifies the contact metal plug as a conductive fill structure—typically tungsten—deposited within the source contact trench to electrically connect the underlying diffusion regions to the surface metal layer. (*See* Ex. 1001, '634 Patent, 4:13–27; Figs. 2F–2G, elements 111/211.)

<This space intentionally left blank.>

[3b]

contact metal plugs

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

360. Hshieh (’384) discloses the same feature. The patent describes “a plurality of trenched source contact[s] filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150.” (*See* Ex. 1005, Hshieh (’384), ¶[0027]; Figs. 3–8, elements 145 and 150.) In an alternative embodiment, the tungsten plug is referred to as element 250, which is surrounded by barrier metal layer 245. (*Id.* ¶[0035]; Figs. 9H–9J, elements 245 and 250.)

361. These tungsten plugs fill the source contact trenches and provide vertical conduction between the P+ contact regions in the body and the front-side source electrode. As in the ’634 Patent, the metal plugs in Hshieh (’384) are isolated from surrounding dielectric layers by a barrier metal film and are structurally and electrically integrated into the vertical current path.

362. Accordingly, Hshieh (’384) teaches contact metal plugs formed within the source contact trenches that perform the same structural and electrical function as element ’634-111/211 and therefore teaches limitation *[3b]*.

5. Claim 4: “The trenched MOSFET of claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is [t]ungsten.”

363. Claim 4 is a dependent claim–and depends from Claim 3, which depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2, Section XI.A.3, and Section XI.A.4) that Claim 1, Claim 2, and Claim 3 of

the ’634 Patent are either taught by Hshieh (’384) or rendered obvious by Hshieh (’384) and the knowledge of a POSITA.

364. The remainder of Claim 4 is also taught by Hshieh (’384). It was shown above that Hshieh (’384) teaches Claim 3–which requires the presence of “a barrier metal layer and a plurality of contact metal plugs.” In that analysis, it was shown that Hshieh (’384) teaches “a barrier metal layer” with a barrier metal layer of Ti or Ti/TiN, while Hshieh (’384) also teaches “a plurality of contact metal plugs” with a plurality of contact metal plugs that are composed of tungsten. Thus, the analysis of Claim 3 above, which demonstrated the specific use in Hshieh (’384) of particular materials to meet these two requirements, also serves to demonstrate that Hshieh (’384) teaches the use of the specific materials that are specified in Claim 4.

a. [4a]: “barrier metal layer is Ti/TiN.”

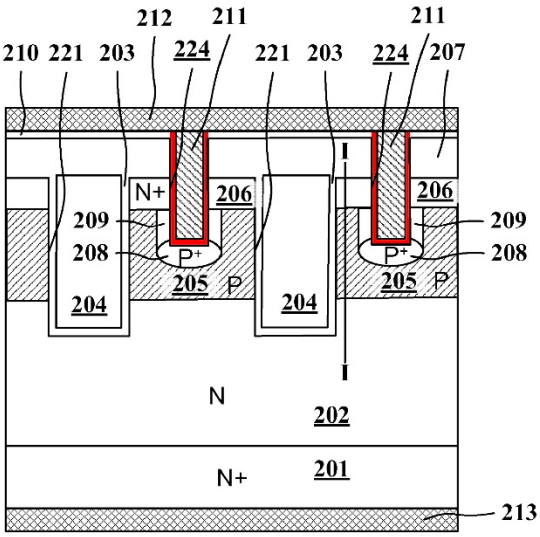
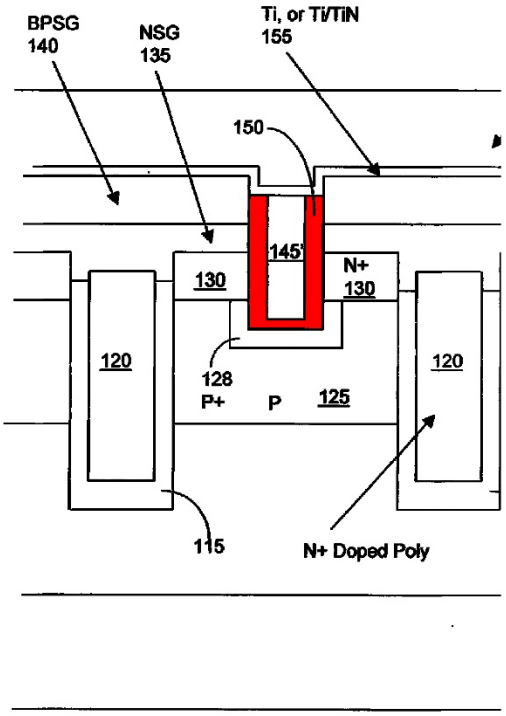
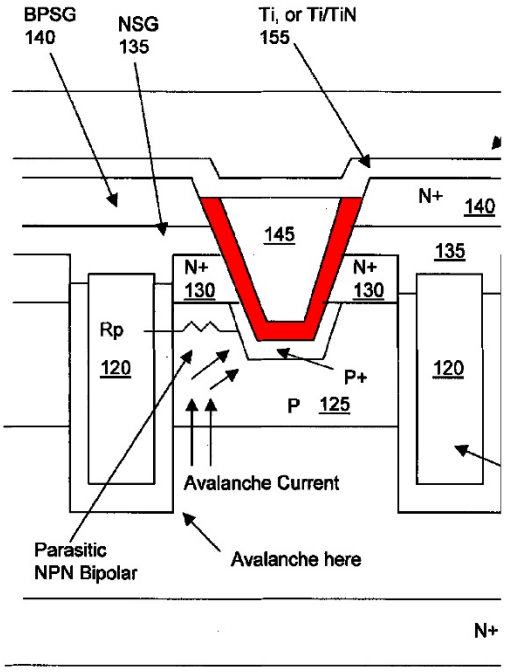
365. ***[4a]: “barrier metal layer is Ti/TiN.”*** Limitation *[4a]* is disclosed in Hshieh (’384), which provides a barrier metal layer of Ti/TiN, corresponding to element ’634-110/210 of the ’634 Patent. The ’634 Patent identifies the barrier metal layer as a conductive film that prevents diffusion and maintains structural integrity at the interface between the tungsten plug and the surrounding dielectric.

366. Hshieh ('384) discloses that the trenched source contact is "filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150." (*See* Ex. 1005, Hshieh ('384), ¶[0027]; *see also* Figs. 3–8, elements 145 and 150.) In an alternate embodiment, the Ti/TiN barrier is labeled as element 245, surrounding tungsten plug 250. (*Id*. ¶[0035]; Figs. 9H–9J.)

<This space intentionally left blank.>

[4a]

barrier metal layer is Ti/TiN

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

Thus, Hshieh ('384) expressly discloses a Ti/TiN barrier metal layer, satisfying limitation *[4a]*.

b. [4b]: "contact metal plug is [t]ungsten."

367. Limitation ***[4b]*** is disclosed in Hshieh ('384), which provides a tungsten contact metal plug, corresponding to element '634-111/211 of the '634 Patent.

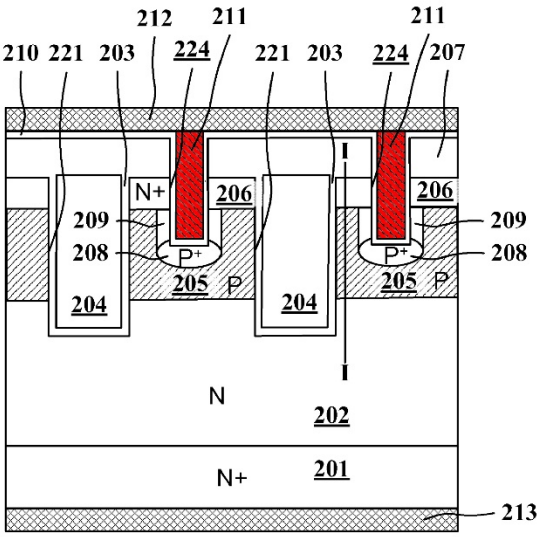
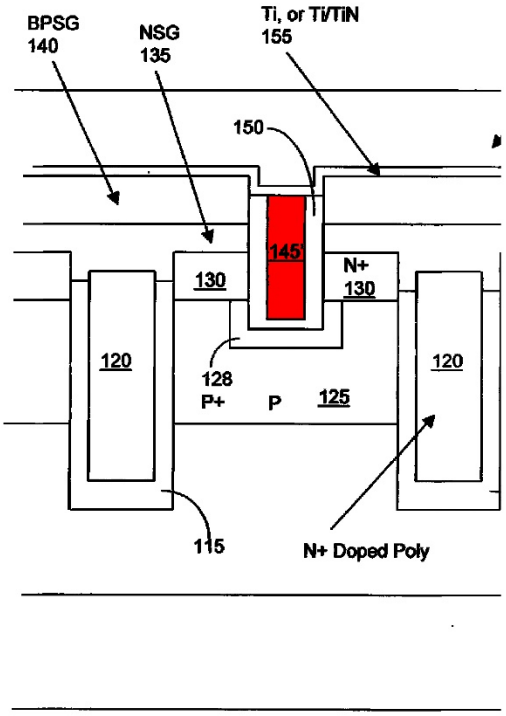
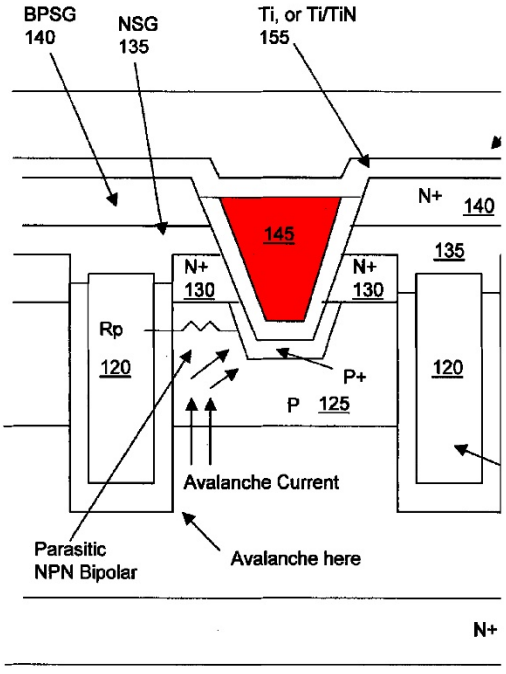
368. Hshieh ('384) states that "a plurality of trenched source contact[s] filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150" is formed. (*See* Ex. 1005, Hshieh ('384), ¶[0027]; *see also* Figs. 3–8, elements 145 and 150.) In an alternative embodiment, the contact plug is labeled as tungsten plug 250, surrounded by a barrier layer 245. (*Id*. ¶[0035]; Figs. 9H–9J.)

369. These plugs are explicitly identified as tungsten, consistent with the '634 Patent's description of the contact metal plug.

<*This space intentionally left blank.*>

[4b]

contact metal plug is Tungsten

Ex. 1001 ('634 Hsieh)	Ex. 1005 ('384 Hshieh)
 *Fig. 2G (Annotated)*	 *Fig. 4 (Annotated partial enlarged view)*
	 *Fig. 3 (Annotated partial enlarged view)*

Accordingly, Hshieh ('384) discloses a contact metal plug made of tungsten and therefore teaches limitation *[4b]*.

6. Claim 5: "The trenched MOSFET of claim 4, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

370. Claim 5 is a dependent claim–and depends from Claim 4, which depends from Claim 3, which depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2, Section XI.A.3, Section XI.A.4, and Section XI.A.5) that Claim 1, Claim 2, Claim 3, and Claim 4 of the '634 Patent are either taught by Hshieh ('384) or rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

371. The remainder of Claim 5 is also expressly taught by Hshieh ('384).

372. This limitation is disclosed in Hshieh ('384), which provides source contact trenches having a vertical shape or a tapered shape, consistent with element '634-124/224. As in the '634 Patent, the trench shape may be vertical or tapered. (*See* Ex. 1001, '634 Patent, 4:50–52.)

Ex. 1005 ('384 Hshieh)

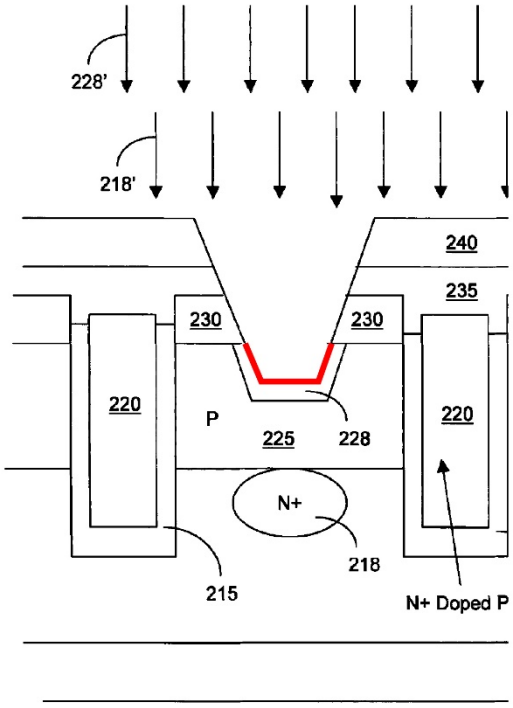


Fig. 9G (Annotated partial enlarged view)

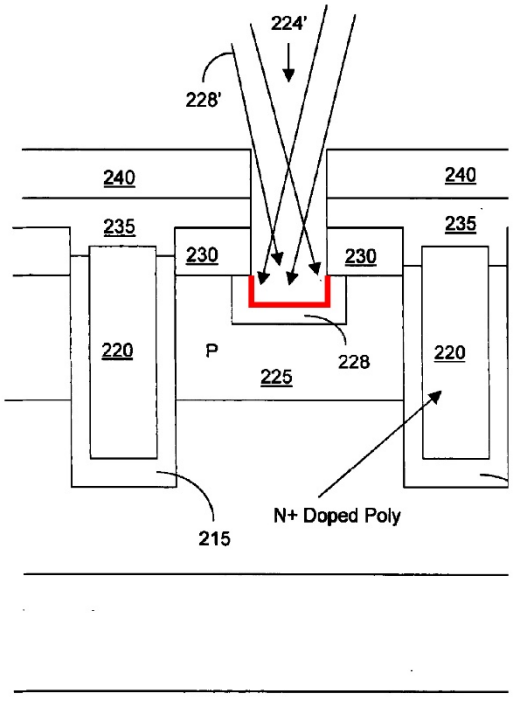


Fig. 9G' (Annotated partial enlarged view)

373. Hshieh ('384) discloses "trenched source contacts" (element 145) which are formed by etching a trench into the semiconductor body and then filling that trench with conductive material. Figures 4, 5, 7, 8, and 9G' illustrate a vertical trench configuration–while Figures such as 2, 6, and 9G–9J illustrate non-vertical, tapered sidewalls, as the trench width narrows from the top down toward the base. (*See* Ex. 1005 ¶34, FIGs 2, 4-8, G', 9G-9J.) As is evident from the figures presented in Section VII.C, a tapered trench profile has long been known to be produced by common etch processes–and falls squarely within the range contemplated by this claim.

Accordingly, Hshieh ('384) discloses both vertical and tapered source contact trenches, teaching *Claim 5*.

7. Claim 6: "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

374. Claim 6 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2) that Claim 1 of the '634 Patent is rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

375. The remainder of Claim 6 is also rendered obvious by Hshieh ('384) and the knowledge of a POSITA–and as will be detailed via the claim sub-elements below, Claim 6 in toto is identical in structure to Claim 2, except that it reverses the polarities (i.e., n and p) of the components as described in Claim 2. As noted in the discussion of Claim 2, that claim is basically identifying a MOSFET structure that is an n-type (i.e. nMOS) MOSFET transistor; Claim 6 simply changes the dopant polarity to describe what is a p-type (i.e., pMOS) MOSFET transistor.

376. To simplify the analysis, this claim will be split into claim elements.

a. ***[6a]: "wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof,"***

377. Claim 6 is identical to Claim 2–except that it reverses the polarities (n-to-p and vice-versa) of the determining dopant in each layer; this amounts to being a way of saying that while the teachings of Claim 2 describe what is well-known in the art as being an nMOS transistor, the teachings of Claim 6 describe what is well-known in the art as being a pMOS transistor.

378. As described in Section VII.B, the ability to use doping of silicon to produce either nMOS or pMOS transistors (which are electrical mirror-images of each other) has long been known in the art. For example, this well-known concept

is clearly illustrated in the following figures from Grove (1967), which demonstrate that the structural layout of a MOSFET remains the same regardless of whether it is configured as an n-channel or p-channel device, with the only difference being the polarity of the dopants used in each region.

Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 Fig. 11.8 (1967)

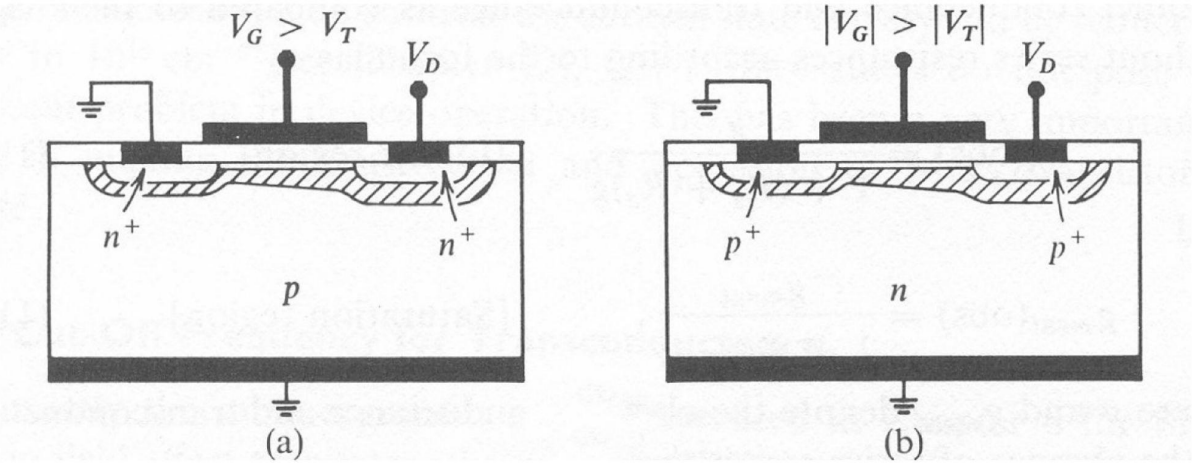


Fig. 11.8 (Annotated partial enlarged view)

379. It is therefore well known in the art that a trench-gated MOSFET could be implemented as either an n-channel or a p-channel device. This knowledge would have been readily understood by a POSITA. Notably, the structures disclosed in the ’634 Patent and Hshieh (’384) are structurally identical regardless of whether the device is implemented as an n-channel or p-channel MOSFET. By simply reversing the doping polarities—i.e., substituting P-type dopants for N-type dopants and vice versa—the same physical structure can be

used to fabricate a p-channel version of an otherwise n-channel transistor. This represents a straightforward and routine chemical substitution that does not alter the underlying geometry or layering of the device.

b. [6b]: "and the lateral contact layer has less doping concentration than the base contact layer at bottom."

380. Claim element *[6b]* is identical to claim element *[2b]*–which was already discussed earlier (in Section XI.A.3.b). For the reasons described there, this claim element is rendered obvious by Hshieh ('384) in combination with the knowledge of a POSITA.

8. Claim 7: "The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

381. Claim 7 is a dependent claim–and depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2 and Section XI.A.7) that Claim 1 and Claim 6 of the '634 Patent are either taught by Hshieh ('384) or rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

382. The remainder of Claim 7 is also taught by Claim 7 is identical to Claim 3, which was already discussed earlier (in Section XI.A.4); for the same reasons as those discussed there, Hshieh ('384) teaches Claim 7 of the '634 Patent.

9. Claim 8: "The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is [t]ungsten."

383. Claim 8 is a dependent claim–and depends from Claim 7, which depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2, Section XI.A.7, and Section XI.A.8) that Claim 1, Claim 6, and Claim 7 of the '634 Patent are either taught by Hshieh ('384) or rendered obvious by Hshieh ('384) and the knowledge of a POSITA.

384. The remainder of Claim 8 is also rendered obvious by Hshieh ('384) and the knowledge of a POSITA. Claim 8 is identical to Claim 4, which was already discussed earlier (in Section XI.A.5); for the same reasons as those discussed there, Hshieh ('384) teaches Claim 8 of the '634 Patent.

10. Claim 9: "The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

385. Claim 9 is a dependent claim–and depends from Claim 8, which depends from Claim 7, which depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.A.2, Section XI.A.7, Section XI.A.8, and Section XI.A.9) that Claim 1, Claim 6, Claim 7, and Claim 8 of the '634 Patent are either

taught by Hshieh (’384) or rendered obvious by Hshieh (’384) and the knowledge of a POSITA.

386. The remainder of Claim 5 is also taught by Hshieh (’384). Claim 9 is identical to Claim 5, which was already discussed earlier (in Section XI.A.6); for the same reasons as those discussed there, Hshieh (’384) teaches Claim 9 of the ’634 Patent.

B. Ground 2–Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being Obvious Over Uno (’864) in view of the knowledge of the POSITA

387. It is my conclusion and opinion that Claims 1-9 of the ’634 Patent are either taught by Uno (’864), or are rendered obvious by Uno (’864) in view of the knowledge of a POSITA.

388. As briefly noted earlier (in Section X.D), the knowledge of a POSITA at the time of the filing of the ’634 Patent (2008) can readily be ascertained by examination of some of the relevant technical literature (books, papers, patents, etc.) It was also noted there that this literature is vast and deep–and that a few references can be chosen from this vast sea to demonstrate the knowledge of a POSITA at the relevant time; this will be done as necessary below, in the claim-by-claim analysis.

1. A POSITA Would Have Had a Motivation and a Reasonable Expectation of Success

389. It is my conclusion and opinion that, based on my education, training, and experience, a person of ordinary skill in the art ("POSITA") would have been motivated, as of the Filing Date of the Challenged Patent, to implement the teachings of Uno (U.S. Patent No. 6,984,864) in view of his/her existing knowledge and routine engineering practices. Uno discloses trench-gated vertical-conduction-path MOSFET structures, and addresses challenges such as contact resistivity and device ruggedness in trench MOSFET configurations. A POSITA would have recognized that Uno offers concrete design benefits—for example, improved sidewall contact structures and reduced parasitic resistance—making it a solution to known issues in the field, thus providing a clear motivation to apply its teachings in the claimed context (consistent with what I understand are KSR International Co. and Federal Circuit precedent on "obvious-to-try" strategies).

390. Moreover, a POSITA would have had a reasonable expectation of success in implementing Uno's teachings without undue experimentation. The structures and fabrication techniques in Uno, such as trench sidewall shaping and source contact trench integration, were well-understood and predictably-operable using standard silicon processing flows at the relevant time. The reference's predictable compatibility with common device layouts provides the evidentiary

basis for concluding that success would have been expected—not speculative—even if certain minor elements were unstated or unlabeled in the disclosure.

391. Critically, my analysis is grounded on the state of the art as of the Filing Date—namely Uno itself along with general contemporaneous engineering knowledge, and does not rely on the Challenged Patent's teachings. The motivation and expectation-of-success arguments are based on concrete design incentives present in the art (e.g. improving ruggedness, contact resistance) rather than on hindsight reconstruction after reading the patent-in-suit.

2. Independent Claim 1

392. Claim 1 is an independent claim–and is the only independent claim of the '634 Patent; it is also an apparatus claim.

a. [1-preamble]: "A trenched MOSFET with trenched source contact, comprising:"

393. To the extent that a preamble is limiting, Uno ('864) teaches the preamble of Claim 1–as can easily be seen via simple examination of Uno ('864).

394. That Uno ('864) discloses a "trenched MOSFET" as can readily be seen via the specification of Uno ('864):

> Transistors that can be used for high power application of several watts or higher are referred to as power transistors, for which various structures have been studied.

> Among them, power MISFETs includes those referred to as a vertical type and lateral type and they are classified structure, for example, into a trench type and planer type in accordance with the Structure of a gate portion. (Ex. 1006, Uno ('864), 1:11-17).

The term "MISFET" and its relationship to the MOSFET art was explained earlier, in the overview discussion of Uno ('864) (in Section X.B).

395. Further, Uno ('864) also discloses a "trenched source contact":

> In an n-channel type power MISFET, a source electrode in contact with an n-semiconductor region (source region) and a p^+-semiconductor region (back gate contact region) is constituted with an Al film and an underlying barrier film comprised of $MoSi_2$, (Ex. 1006, Uno ('864) at Abstract.)

Both the "trenched MOSFET" and the "trenched source contact" of Uno ('864) are also evident in this annotated excerpt from Fig. 38 of Uno ('864):

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Ex. 1006 ('864 Uno)

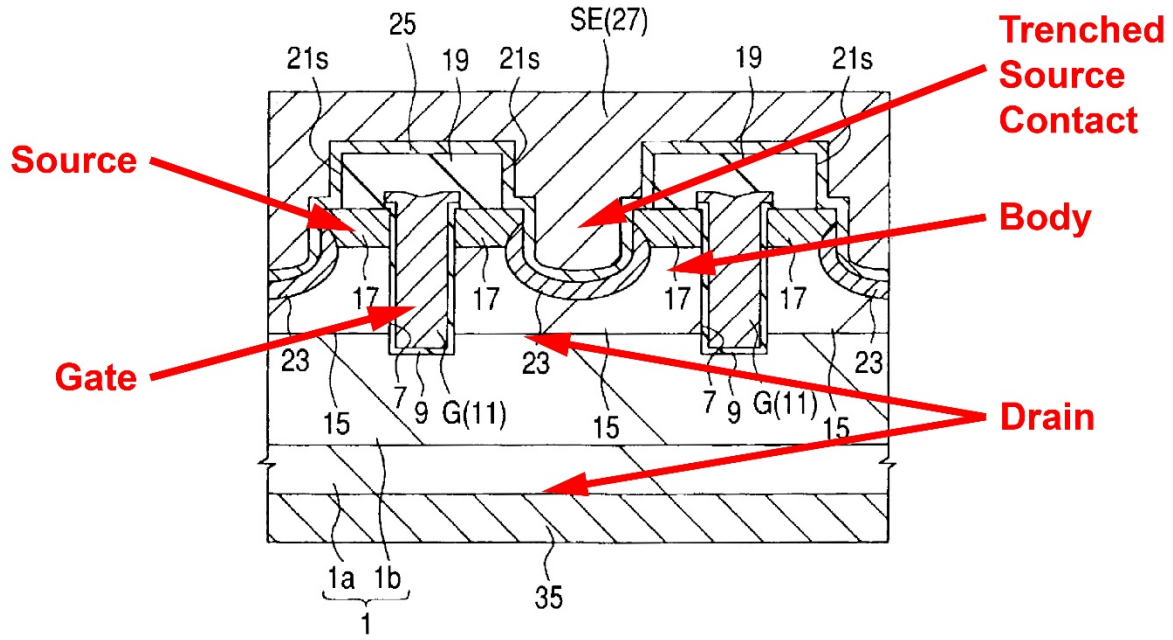


Fig. 38 (Annotated)

396. It should be noted that what the '634 Patent calls a "source contact" Uno also calls a "source contact" (*See* Ex. 1006, Uno ('864), 5:38, 6:8-9, 15:13); these are the same thing–as in both instances, the source of the MOS transistor and the body of the MOS transistor are connected together by that contact (as is evident in the annotated figure above); the connecting-together of the source and the body of a MOS transistor is a common and well-known practice in the art. (*See* Ex. 1013, Adel S. Sedra and Kenneth C. Smith, *Microelectronics Circuits*, 237 (5th ed. 2004).) Further, in some prior art instances (*See* Ex. 1014, U.S. Patent No. 4,980,747.), this same sort of contact is called simply a "substrate contact." Thus, in this Declaration, when these terms are used, they are intended (unless otherwise

noted) to mean the same thing–and any differences are due to the usage in the particular reference from which the particular term was drawn.

i. [1-preamble-1]: "trenched MOSFET."

397. ***[1-preamble-1]*: "trenched MOSFET. "** Uno ('864) discloses a "trenched MOSFET" (which I will refer to as *[1-preamble-1]*), for the reasons cited above and as further detailed below.

398. Uno ('864) describes semiconductor devices, specifically metal-insulator-semiconductor field-effect transistors (MISFETs). (Ex. 1006, Uno ('864), 1:06–10; 1:35–37.) As I explained earlier (in Section X.B), a POSITA would have understood that metal-oxide-semiconductor field-effect transistors (MOSFETs) are a well-known subclass of MISFETs. Because MOSFETs represent the most prevalent form of MISFETs in the relevant field, a POSITA would have reasonably understood that Uno's disclosure inherently encompasses a MOSFET structure. (*See* Section X.B.)

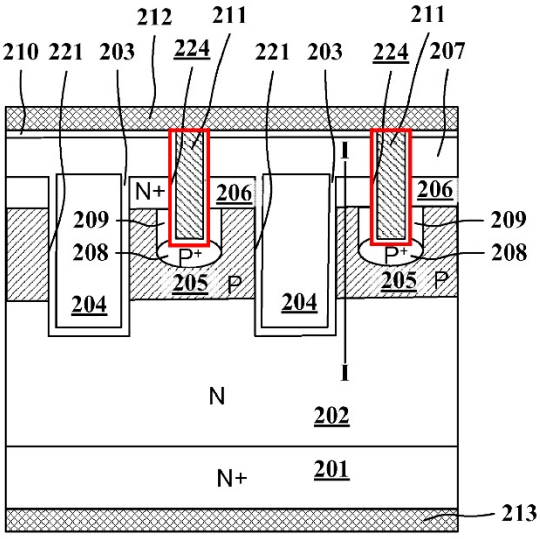
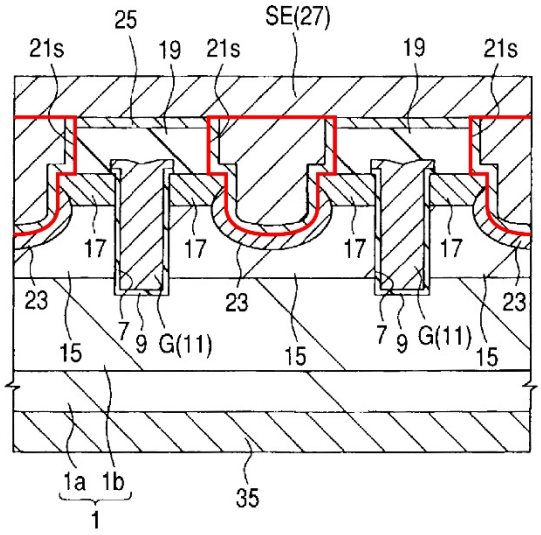
399. Accordingly, the disclosure in Uno ('864) teaches *[1-preamble-1]*, either explicitly or inherently, by virtue of its application to conventional MISFET—and thus MOSFET—devices.

400. Based on the above, it is my conclusion and opinion that Uno ('864) expressly discloses a trenched MOSFET structure, and thus teaches *[1-preamble-1]*–"trenched MOSFET" of the '634 Patent.

ii. [1-preamble-2]: "trenched source contact."

401. ***[1-preamble-2]*: "trenched source contact."** This limitation is disclosed in Uno ('864), which describes a trenched source contact structure that is consistent with the claimed element (i.e., '634-124/224).

[1-preamble-2]
trenched source contact

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

402. Uno ('864) explicitly refers to the formation of a "contact trench (source-contact) 21s" through etching of both the silicon oxide film and the

underlying semiconductor substrate regions. Specifically, Uno ('864) states: "For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p-Semiconductor region 15 and n-semiconductor region 17) are etched to form a contact trench (Source-contact) 21s." (Ex. 1006, Uno ('864), 15:31–35.)

403. Additional portions of the specification, along with numerous figures—such as Figs. 9, 12, 15, 16, 18, 20, 24, and 36–38—further illustrate and describe the structural configuration and fabrication process of the source-contact trench. (*Id.* at 5:33-38; 5:43–48; 5:52–62; 6:7–13; 6:22–27; 6:35–39; 6:64–67, element 21s.) Based on these disclosures, a POSITA would understand that Uno ('864) teaches a trenched source contact consistent with the claimed *[1-preamble-2]*, from both a structural and a process perspective.

404. For the reasons stated above and to the extent that the preamble is limiting, Uno ('864) teaches both the "trenched MOSFET" and the "trenched source contact" of the '634 Patent–and thus teaches the preamble of Claim 1.

b. [1a]: "a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;"

405. This claim element of Claim 1 of the ’634 Patent is taught by Uno (’864).

406. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [1a-1]: “a semiconductor region having a drain region, a body region and a source region, comprising,”

407. This claim sub-element is taught by Uno (’864). All of these “regions” are present in Uno (’864), as evidenced by this excerpt from the Summary of the Invention of Uno (’864):

> ***[1a-1-1]:*** a ***source portion*** comprising ***semiconductor region*** of a first conduction type on the surface of the semiconductor substrate and in the semiconductor substrate at the end of the gate portion;
>
> ***[1a-1-2]:*** a ***drain portion*** comprising a semiconductor region of the first conduction type; and
>
> ***[1a-1-3]:*** a ***channel portion*** arranged between the source portion and the drain portion,
>
> (Ex. 1006, Uno (’864) at 2:22-29; *emphases added*.)

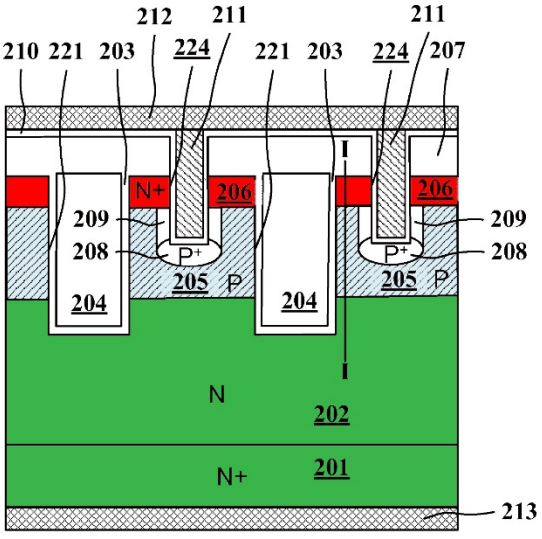
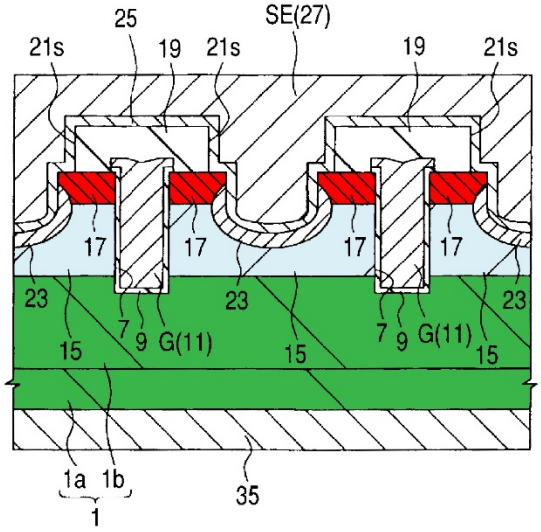
What Uno (’864) calls the “source portion,” the “drain portion,” and the “channel portion” correspond, respectively, to what the ’634 Patent calls the “source region,” the “drain region,” and the “body region.” By definition, a MOSFET includes a source region, a body region, and a drain region that are all

formed together in a unitary sample of a semiconductor material (i.e., a semiconductor region).

1) [1a-1-1]: "semiconductor region."

408. ***[1a-1-1]: "semiconductor region."*** The limitation *[1a-1-1]*– "semiconductor region" is disclosed in Uno ('864), which describes a semiconductor region comprising a drain region, body region, and source region—consistent with the layered structure recited in the '634 Patent (i.e., '634-101/201, '634-102/202, '634-105/205, and '634-106/206).

[1a-1-1]
semiconductor region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

409. Specifically, Uno ('864) states that "In an n-channel type power MISFET … an npn-type parasitic bipolar transistor PB constituted with an n-semiconductor region (source region) 17, a p-semiconductor region (channel region) 15, and a drain (1a, 1b) is present inside…" (Ex. 1006, Uno ('864), Fig. 20; 8:24–28.) Here, Uno identifies the regions via a description of an inherent (and possibly parasitic) bipolar transistor structure that inherently exists in a MOSFET structure.

410. Uno ('864) further explains that "a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a" (*Id*. at 4:55-58), corresponding to the silicon substrate ('634-101/201) and epitaxial layer ('634-102/202). The p-type region 15 and n^+-type region 17 correspond to the body and source regions, respectively (*Id*. at 5:35-36). These structural components are illustrated and labeled consistently across multiple figures (e.g., Figs. 8–9, 11–16, 18, 20, 36–38, elements 1a, 1b, 15, and 17). In the annotated figures above, the drain region (elements 1a, 1b) has been shaded green, the body region (element 15) has been shaded light blue, and the source region (element 17) has been shaded red, to clearly illustrate the layered structure. Taken together, Uno ('864)'s describes a vertically layered semiconductor structure comprising, in order from bottom to top:

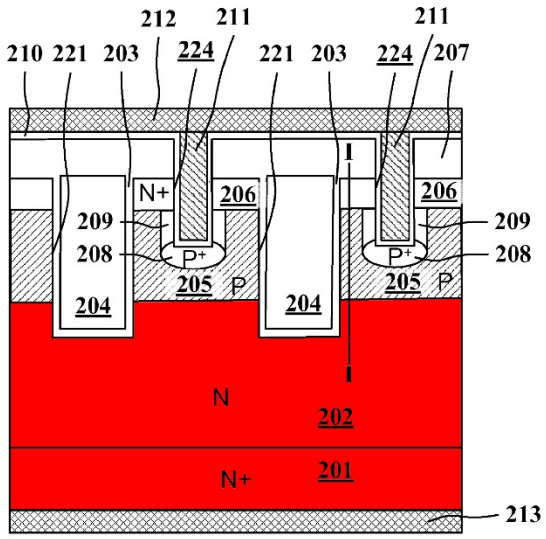
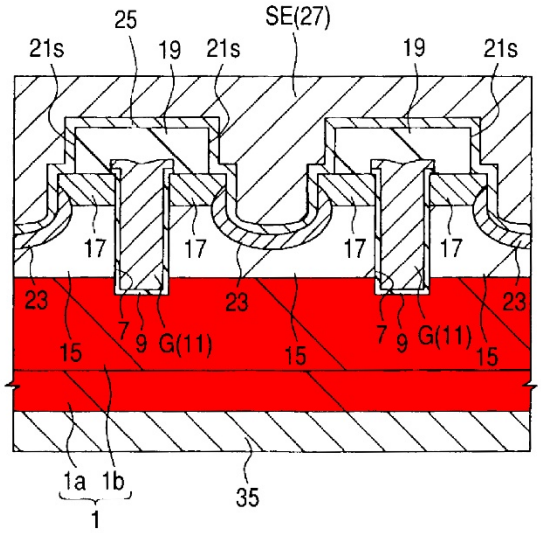
(1) an N+ silicon substrate (element 1a), (2) an N-type epitaxial layer (element 1b), (3) a P-type body region (element 15), and (4) an N+ source region (element 17).

411. Thus, Uno ('864) clearly discloses the layered semiconductor structure comprising the drain, body, and source regions and therefore teaches limitation ***[1a-1-1]*** of the '634 Patent; this configuration corresponds directly to the multi-layered semiconductor region recited in limitation ***[1a-1-1]***of the '634 Patent. Therefore, it is my conclusion and opinion that Uno ('864) discloses limitation *[1a-1-1]–"semiconductor region"–*of the '634 Patent.

2) [1a-1-2]: "drain region."

412. ***[1a-1-2]: "drain region."*** This limitation is disclosed in Uno ('864), which clearly teaches a drain region consistent with the structure recited in the '634 Patent. The '634 Patent describes the epitaxial layer ('634-102/202) as comprising the drain region. However, the language of claim 1 is ambiguous as to whether the underlying silicon substrate is included within the claimed "drain region" or whether the drain is confined solely to the epitaxial layer. (*See* Ex. 1001, Hshieh ('634), claim 1.) While this ambiguity raises questions about the precise bounds of the claimed drain region, it is nevertheless clear that both the epitaxial layer and the substrate—whether considered collectively or separately—are present in Uno ('864).

[1a-1-2]
drain region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

413. Specifically, Uno (’864) teaches a structure in which a single crystal silicon layer 1b, doped with an n-type impurity such as phosphorus or arsenic, is epitaxially grown on the surface of an n-type single crystal silicon substrate 1a. (*See* Ex. 1006, Uno (’864), 4:55–58.) The epitaxial layer 1b corresponds to the ’634 Patent’s element ’634-102/202, and the substrate 1a corresponds to ’634-101/201. These two layers together form a continuous vertical conduction path, consistent with a drain region extending from the body regions downward through the epitaxial layer into the substrate. In fact, Uno (’864) refers to these elements as “drain (1a, 1b)”. (*Id*. at 7:27, 8:27, 10:10.) This configuration is further supported

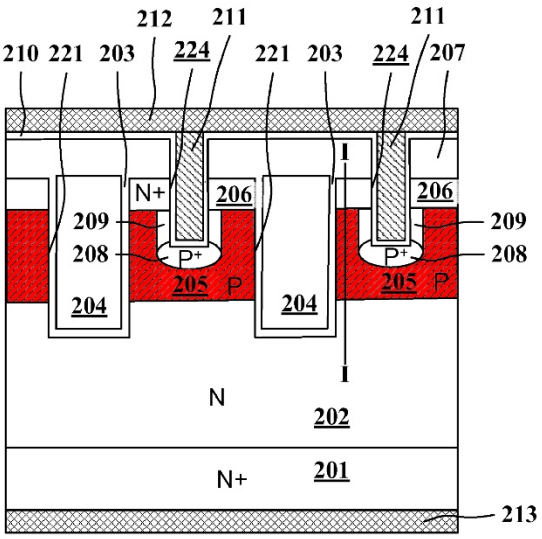
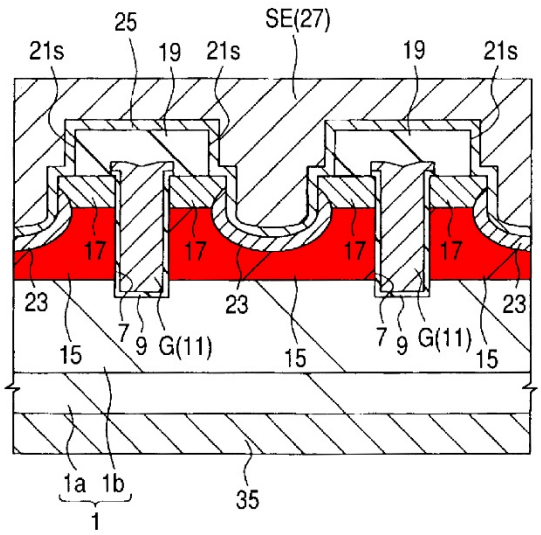
by the structural depictions in Uno (’864), see annotated figures above, including Figures 1, 3, 5, 6, 8, 9, 11–18, 20 and 38.

414. It is my conclusion and opinion that the arrangement disclosed in Uno (’864) mirrors the layered architecture of the drain region as recited in the ’634 Patent. Accordingly, it is my conclusion and opinion that Uno (’864) discloses a drain region comprising both an epitaxial layer and a substrate that together provide a continuous vertical path for current conduction. This structure corresponds to the plain and ordinary meaning of “drain region” as that term would be understood by a POSITA at the time of the invention. Therefore, limitation *[1a-1-2]*–“drain region”–is taught in Uno (’864).

3) [1a-1-3]: “body region.”

415. ***[1a-1-3]: “body region.”*** Uno (’864) discloses a “body region,” which I will refer to as *[1a-1-3]*–“body region.” Uno (’864) teaches a base layer and its corresponding subset of body regions in the same way that these features are recited in the ’634 Patent (i.e., ’634-105/205).

[1a-1-3]
body region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

416. Specifically, Uno (’864) describes a “p–semiconductor region (channel region) 15” that is positioned between the source and drain regions and functions as the channel through which current flows. (*See* Ex. 1006, Uno (’864), 5:67; Figs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38, element 15.) This p-type channel region 15 is both structurally and functionally equivalent to the P-type body region disclosed in the ’634 Patent–both of which provide the gate-controlled conduction surface region that is located between the source and the drain.

417. This interpretation is further supported by the express disclosure in Uno (’864) of “a channel portion [being] arranged between the source portion and the drain portion,” aligning with the typical function and placement of the body

region in trench-type MOSFETs–or, indeed, in any type of MOSFET. (*Id.* at 2:28–30.) Moreover, Uno ('864) discloses an alternative embodiment featuring an "n-semiconductor region (channel region, well) 215," demonstrating that the channel region may be either P-type or N-type, depending on the device polarity. (*Id.* at 9:30-32; Fig. 24, element 215; claim 1.) Regardless of polarity, both embodiments describe a region that functions as the gate-controlled surface conduction path between the source and the drain—corresponding to the body region as recited in the '634 Patent.

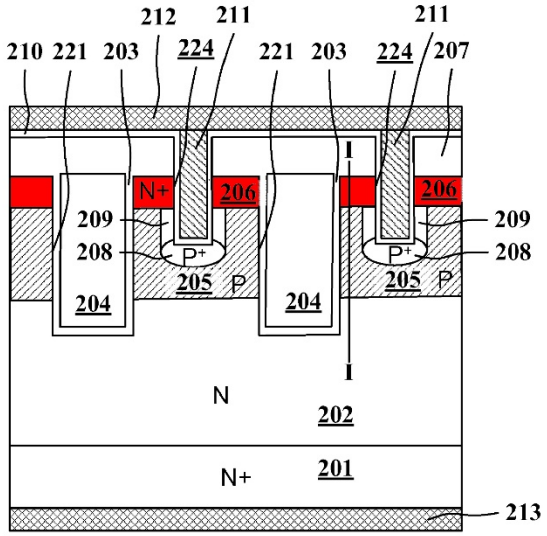
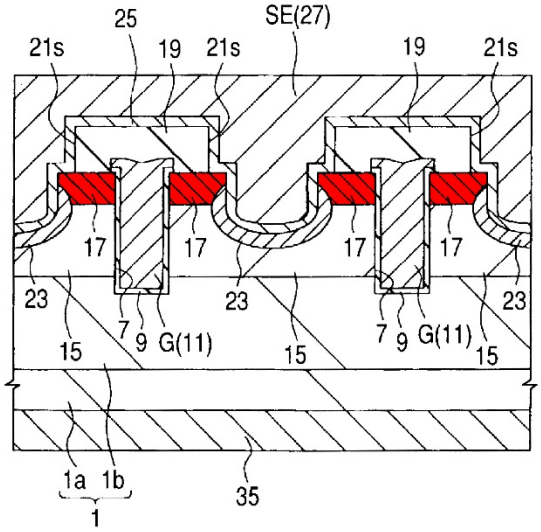
418. Accordingly, it is my conclusion and opinion that the "channel region" disclosed in Uno ('864) fulfills the same structural and functional purpose as the claimed body region that is recited in the '634 Patent; the vertical arrangement and role of this body region are consistent with the base layer (and its subset of body regions) that are described in the '634 Patent claims. Therefore, limitation *[1a-1-3]*–"body region"–is taught by Uno ('864).

4) [1a-1-4]: "source region."

419. ***[1a-1-4]: "source region."*** Uno ('864) teaches a source region (17) (which I will refer to as *[1a-1-4]*–"source region") that is consistent with the structure and function of element 106/206 of the '634 Patent. The '634 Patent describes a heavily doped N^+ source region positioned above the P-type body region and forming part of the vertical conduction path of the MOSFET device.

(Ex. 1001, 3:33-40.) Uno (’864) teaches a source region 17 corresponding to element ’634-106/206 of the ’634 Patent.

[1a-1-4]
source region

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated)*	 *Fig. 38 (Annotated)*

420. Specifically, Uno (’864) states that “an n-impurity (for example, As) is implanted into the substrate 1 between the trenches 7 to form an n-semiconductor region (source region) 17.” (Ex. 1006, Uno (’864), 5:26–29.) The source region 17 is further characterized as an “n^+-semiconductor region,” consistent with the heavy doping concentration typically used in source layers of trench-type MOSFETs. (*Id.* at 5:47, 6:10-11, 6:26, 8:26, 8:60.)

421. Moreover, the source region 17 is described as being formed above the p-type semiconductor region 15–which is the same source-to-body

configuration disclosed in the ’634 Patent. (*Id.* at 5:26–32.) These structural relationships are repeatedly illustrated and described throughout Uno (’864), with element 17 consistently identified as the source region. (*Id.* at 5:29-30, 5:57, 8:26, 15:64; Figs. 5, 6, 8–9, 11–18, 20–22, 24–25, 36–38, element 17.) This vertical relationship is consistent with the vertical trench MOSFET architecture disclosed in the ’634 Patent.

422. Accordingly, it is my conclusion and opinion that Uno (’864) clearly discloses a source region that performs the same structural and functional role as the source regions which are subsets of the source layer, as recited in the ’634 Patent, thereby meeting the requirements of *[1a-1-4]*–“source region”.

ii. [1a-2]: “a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

423. This claim sub-element is taught by Uno (’864).

424. This is readily seen via an annotated version of Fig. 38 of Uno (’864):

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Ex. 1006 ('864 Uno)

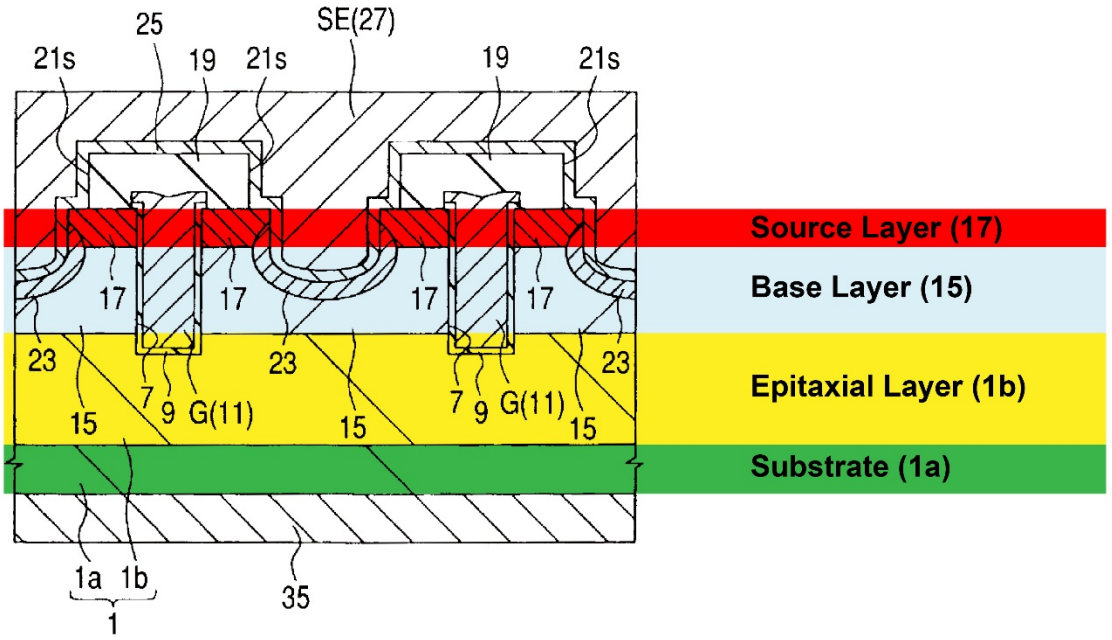


Fig. 38 (Annotated)

425. Uno (’864) identifies 1a as being a “substrate” (Ex. 1006, Uno (’864) at 4:58), 1b as being an “epitaxial layer” (Ex. 1006, Uno (’864), 4:56-59), 15 as being a “body region” (which, as noted above, Uno (’864) refers to as a “channel region”) (Ex. 1006, Uno (’864), 5:20-23), and 17 as being a “source region” (Ex. 1006, Uno (’864), 5:29-30); further, these layers are configured in the layering-order specified in the claim sub-element.

426. In Uno (’864), the “channel region” 15 refers to the body region of individual MOSFET structures, while the larger-and-universal layer that includes such channel regions (i.e., body regions) corresponds to the “base layer” recited in

the claim sub-element—i.e., the channel regions / body regions represent discrete segments of the overall base layer.

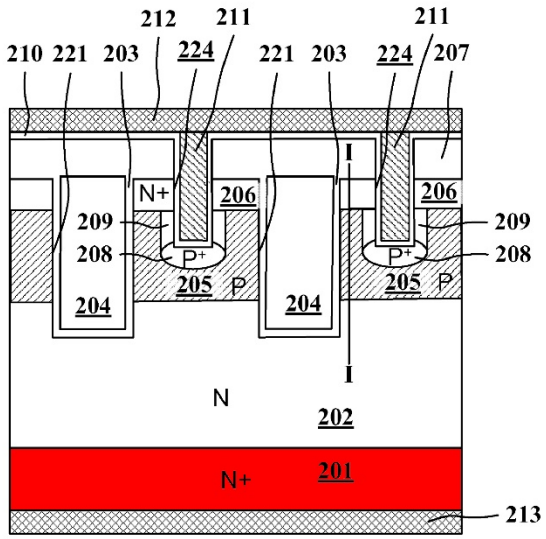
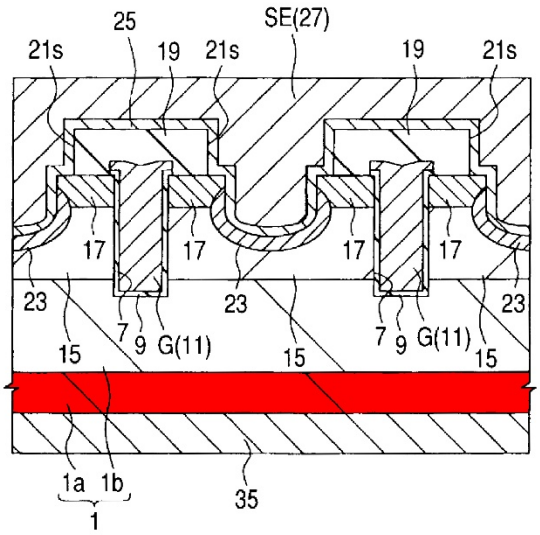
427. Similarly, in Uno ('864) the source region 17 refers to the source region of particular MOSFET structures, while the larger-and-universal layer that includes such source regions corresponds to the "source layer" of the claim sub-element–with the source regions corresponding to the separated pieces of the overall source layer.

1) [1a-2-1]: "silicon substrate."

428. ***[1a-2-1]: "silicon substrate."*** Limitation *[1a-2-1]–"silicon substrate"*–is disclosed in Uno ('864), which teaches a silicon substrate corresponding to element '634-101/201 of the '634 Patent.

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[1a-2-1]
silicon substrate

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

429. Uno (’864) expressly describes “an n-single crystal silicon substrate 1a” that serves as the foundational layer of the device. (*See* Ex. 1006, Uno (’864), 4:58; Figs. 1, 3, 5, 6, 8, 9, 11–18, 20, 36–38, element 1a.)

430. The specification of Uno (’864) further clarifies that “as shown in FIG. 1, a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus or arsenic) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a” is provided. (*Id.* at 4:55–59.) This n-type substrate 1a functions as the base upon which the epitaxial and subsequent device layers are formed, thereby mirroring the structural and

functional role of the silicon substrate in the ’634 Patent. Accordingly, Uno (’864) discloses a silicon substrate consistent with element ’634-101/201, thus teaching *[1a-2-1]*–“silicon substrate”.

431. This conclusion is further supported by the structural context of the disclosure. A doped N^+ substrate with an N-type epitaxial layer grown on top, has long been known as a commonly-used approach in MOS transistor manufacturing. (*See* Ex. 1015, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 1, 124 (1986); Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era* Vol. 2, 385-387 (1990).); in particular, “Either n-epi on n+ substrates or p-epi on p+ substrates can be used.” *Id.* at 386. This includes its use in trenched-gate MOS transistors–as evidenced by its use in the Texas Instruments 4Mb DRAM that was discussed in Section VII.C (using a doped P+ substrate and a P-type epitaxial layer grown on top–which is what is described in both Uno (’864) and the ’634 Patent, but with the doping polarities reversed.) Thus, whether implemented for an nMOS transistor or for a pMOS transistor, the layered structure—a heavily doped substrate with a lighter epitaxial layer on top of it—remains a conventional and functionally-equivalent structure.

Ex. 1016, Ashwin H. Shah et al., *A 4-Mbit DRAM with Trench-Transistor Cell*, IEEE Journal of Solid-State Circuits, vol. 21, 619 Fig. 1 (1986)

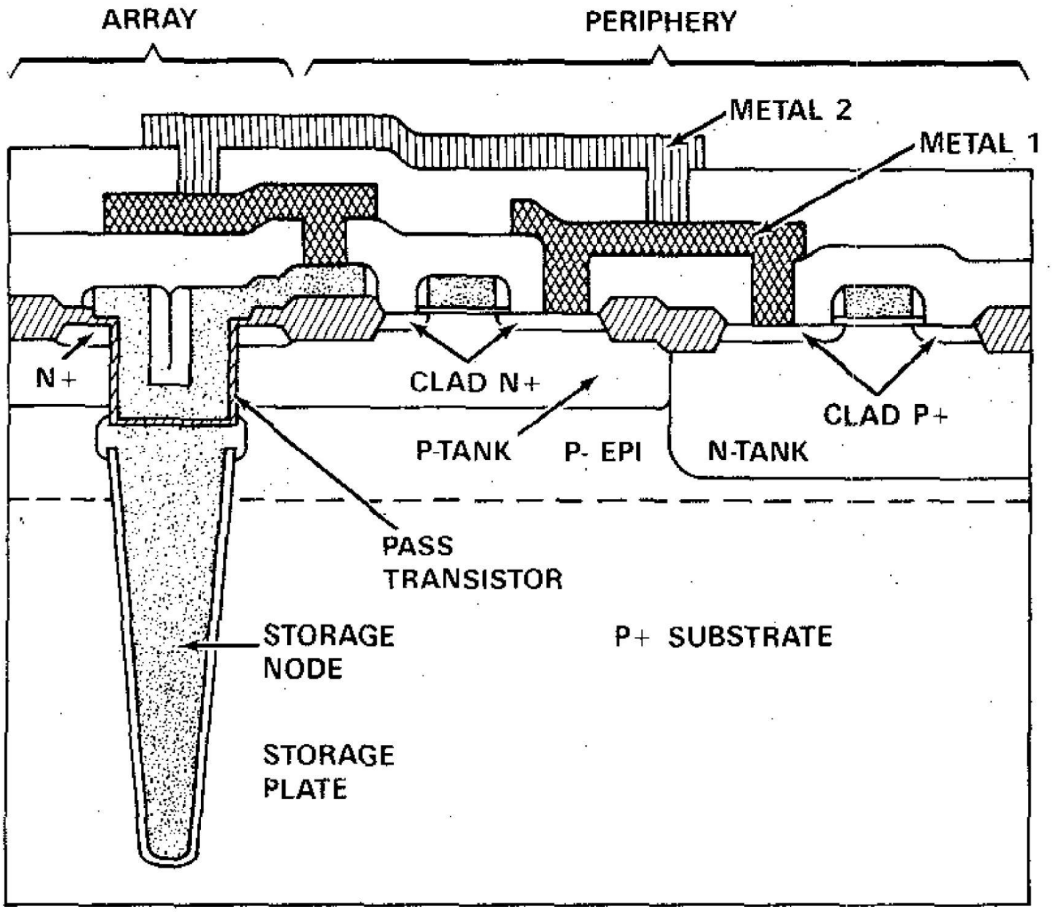


Fig. 1. Typical cross section of process topography.

432. Notably, Uno ('864) expressly describes the swapping of dopant polarities to form a pMOS transistor instead of an nMOS transistor. (*See* Ex. 1006, Uno ('864), 9:20–29.)

433. This all serves to demonstrate that the use of a lighter-doped epitaxial layer deposited on top of a heavily-doped substrate has long been a well-known

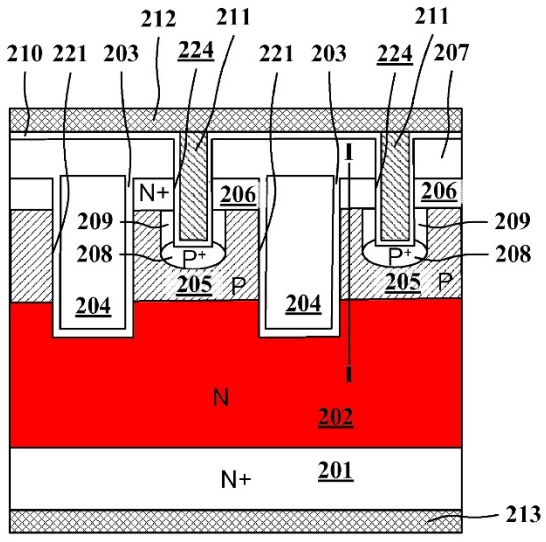
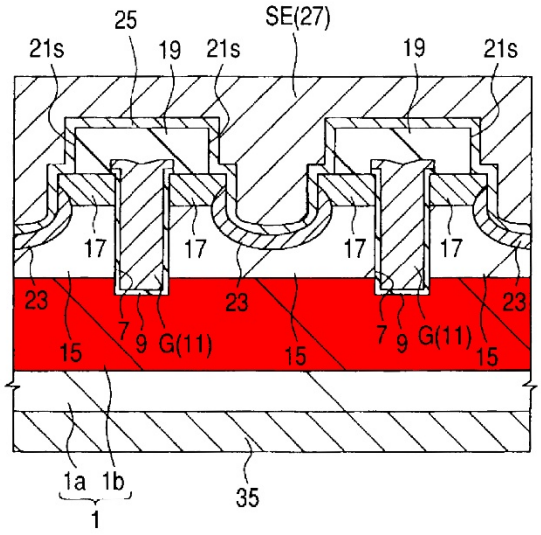
technique in the MOS transistor manufacturing art–and would have been known to a POSITA.

434. Accordingly, it is my conclusion and opinion that Uno ('864) discloses a silicon substrate that serves as the foundation for the semiconductor device–which is consistent with the "silicon substrate" recited in the '634 Patent. Therefore, Uno ('864) teaches limitation *[1a-2-1]*–"silicon substrate."

2) [1a-2-2]: "epitaxial layer."

435. ***[1a-2-2]: "epitaxial layer."*** Uno ('864) describes an epitaxial layer, which I will refer to as limitation *[1a-2-2]*–"epitaxial layer".

[1a-2-2]
epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

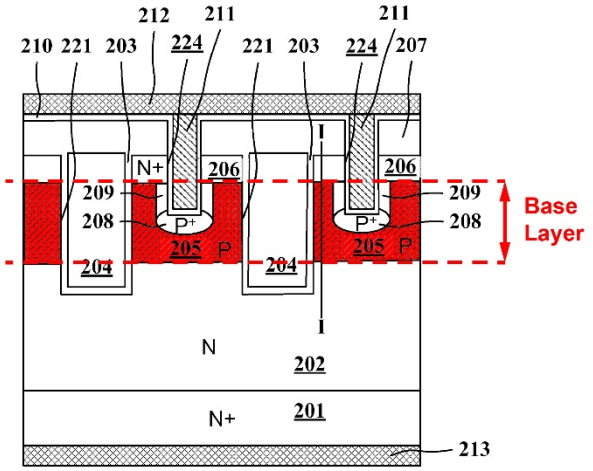
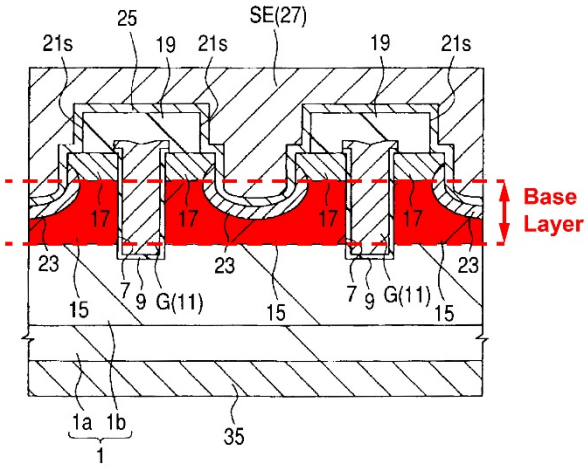
436. Uno (’864) teaches an epitaxial layer corresponding to the drain region, consistent with element ’634-102/202 of the ’634 Patent. Specifically, Uno (’864) states that “a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus or arsenic) is epitaxially grown on the surface of an n-type single crystal silicon substrate 1a (hereinafter simply referred to as ‘substrate’).” (*See* Ex. 1006, Uno (’864), 4:55-59.) This epitaxially-grown layer 1b is formed directly above the substrate 1a, and serves as part of the drain region within the device structure. The configuration and functional relationship between the epitaxial layer and the underlying substrate mirror the arrangement described in the ’634 Patent–where the epitaxial layer provides a vertical conduction path for the drain. These structural features are consistently illustrated throughout the Uno (’864) disclosure. (*Id.* Figs. 1, 3, 5, 6, 8, 9, 11–18, 20, 36-38, element 1b; claim 1.) Accordingly, Uno (’864) discloses an epitaxial layer disposed above a silicon substrate and forming part of the drain region, and therefore teaches limitation *[1a-2-2]*–“epitaxial layer”.

437. Accordingly, it is my conclusion and opinion that Uno (’864) discloses an epitaxial layer positioned above the semiconductor substrate and forming part of the drain region, consistent with the structure recited in the ’634 Patent. These disclosures teach limitation *[1a-2-2]*–“epitaxial layer”.

3) [1a-2-3]: “base layer.”

438. ***[1a-2-3]: "base layer."*** This limitation is disclosed in Uno ('864), which teaches a base layer consistent with element '634-105/205 of the '634 Patent.

[1a-2-3]
base layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

439. Uno ('864) describes "a p–semiconductor region (channel region) 15," positioned between the source and drain regions, and functioning as the channel through which current flows. (*See* Ex. 1006, Uno ('864), 5:67-6:3; Figs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38, element 15.) This p-type region 15 is structurally and functionally equivalent to the body region disclosed in the '634 Patent, as it provides the location of the gate-controlled channel that provides conduction between the source and drain terminals.

440. In an alternative embodiment, Uno ('864) discloses an "n-semiconductor region (channel region, well) 215," demonstrating that the channel—or body—region may be formed from either p-type or n-type material depending on device polarity. (*Id.* at 9:32; Fig. 24, element 215; claim 1.) Notwithstanding the conductivity type, both embodiments describe regions that are subsets of the larger base layer, located between the source region and drain region, and which provide the location of the gate-controlled conduction channel. Accordingly, Uno ('864) discloses a base layer that corresponds in structure, function, and placement to the base layer recited in the '634 Patent and therefore teaches *[1a-2-3]*–"base layer".

441. My conclusion is further supported by the Patent Owner's admitted prior art, as illustrated in Fig. 1 (Prior Art) of the '634 Patent, which shows that the body regions are formed within the base layer. Specifically, the '634 Patent states that "the P-type base layer (205) [corresponds] to the body region of the trenched MOSFET." (Ex. 1001, '634 Patent, 5:1–2.)

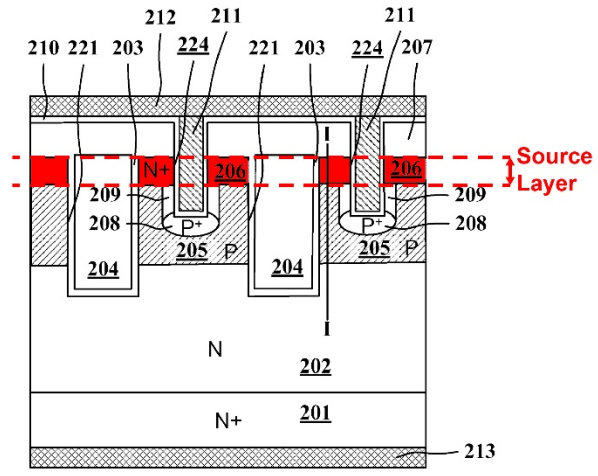
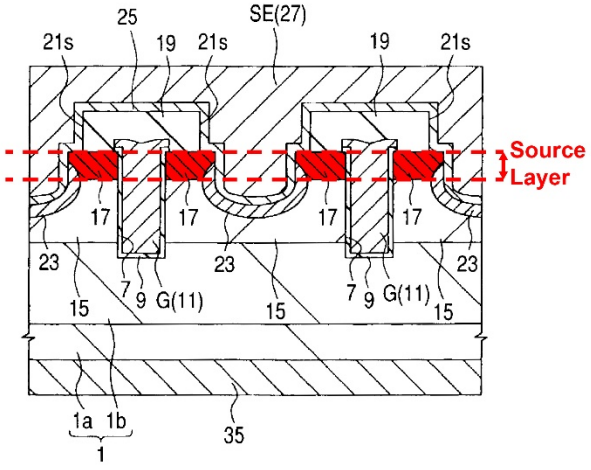
442. Accordingly, it is my conclusion and opinion that Uno ('864) discloses a P-type body region disposed above the epitaxial layer and below the source region, with these body regions being subsets of the base layer as recited in

the ’634 Patent–and that this would be obvious to a POSITA examining Uno (’864). These disclosures therefore teach limitation *[1a-2]*.

4) [1a-2-4]: “source layer.”

443. ***[1a-2-4]: “source layer.”*** Uno (’864) teaches a source region corresponding to the source layer recited in element ’634-106/206 of the ’634 Patent.

[1a-2-4]
source layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	***Fig. 38 (Annotated)***

444. Uno (’864) discloses “an n^+-semiconductor region (source region) 17,” which is formed above the p-type body region and functions as a highly doped source of the transistor. (*See* Ex. 1006, Uno (’864), 5:26–29, 5:43-45, 8:26, 15:64.)

This source region 17 is consistently depicted across various embodiments and is identified as the source region. (*Id.* at 5:55-58; Figs. 5, 6, 8–9, 11–18, 20–22, 24–25, 36–38, element 17.)

445. In an alternative embodiment, Uno ('864) further discloses a "p^+-semiconductor region (source region) 217," illustrating a conductivity type inversion for complementary polarity devices. (*Id*. at 9:33; Fig. 24, element 217; claim 1.) In both embodiments, the source region is highly doped, situated above the body region, and is configured to interface with the device's contact structure—attributes that align with the source regions and the source layer as described in the '634 Patent. Although Uno ('864) does not use the term "source layer," a person of ordinary skill in the art would understand that the consistently positioned source regions above the base and epitaxial layers reside within what the '634 Patent refers to as the "source layer." Accordingly, Uno ('864) discloses a source layer consistent in structure, function, and placement with the source layer (and its subdivision source regions) of the '634 Patent and therefore teaches limitation *[1a-2-4]*–"source layer".

446. My conclusion is further supported by the Patent Owner's admitted prior art, as illustrated in Fig. 1 (Prior Art) of the '634 Patent–which shows that the source regions are formed within the source layer. Specifically, the '634 Patent

states that "the N^+-type source layer (206) [is] corresponding to the source region of the trenched MOSFET." (Ex. 1001, '634 Patent, 4:66–5:1.) Moreover, the relative position of the source region in Uno ('864)—situated above the base layer, epitaxial layer, and silicon substrate—is consistent with the '634 Patent's structural disclosure that "[t]he N^+-type silicon substrate (101), the N-type epitaxial layer (102), the P-type base layer (105), and the N^+-type source layer (106) are stacked in sequence." (*Id.* at 1:29–32.)

447. Accordingly, it is my conclusion and opinion that Uno ('864) discloses a source region in a manner consistent with both the "source region" and the "source layer" as recited in the '634 Patent–and that this would be obvious to a POSITA examining Uno ('864). Thus, these disclosures in Uno ('864) teach limitation *[1a-2]*.

c. [1b]: "a front metal layer formed on the upper surface of said semiconductor region;"

448. This claim element is taught by Uno ('864).

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Ex. 1006 ('864 Uno)

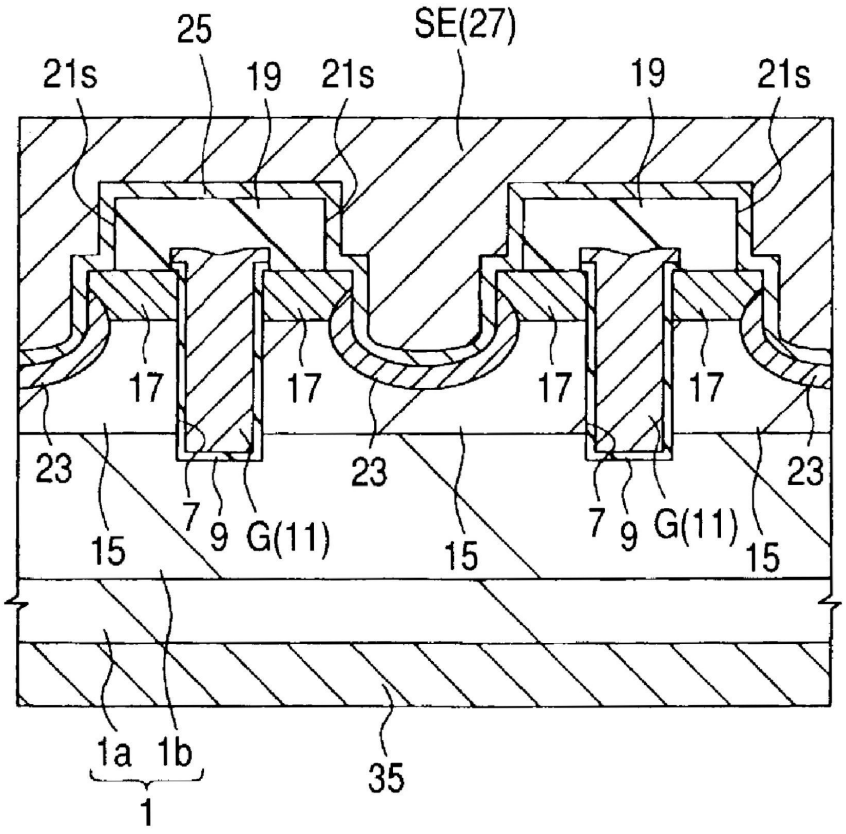


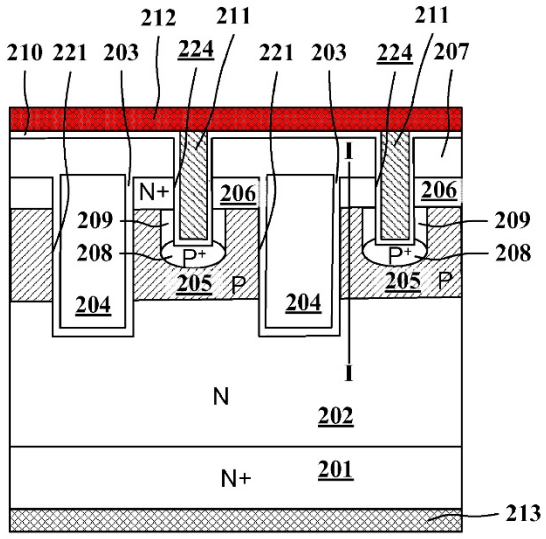
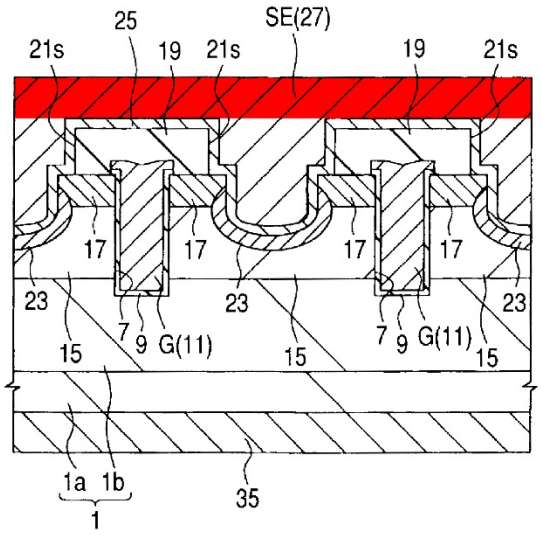
Fig. 38

449. Uno (864) identifies 27 / SE(27) as being "a source electrode SE comprising an aluminum film 27," (Ex. 1006, Uno ('864), 6:19-20); aluminum is a metal, and (as per the figure above) 27 is clearly "formed on the upper surface of said semiconductor region." Further, the use of aluminum (as recited in the excerpt above) was well-known in the art by the time of the '634 Patent (i.e. 2008) for its common use as an interconnect-wiring material that was widely in use for the

purpose of providing wiring between-and-among transistors (and other components) in integrated circuits.

450. ***[1b]: "front metal layer."*** This limitation is disclosed in Uno ('864), which teaches a front-side metal contact corresponding to the "front metal layer" identified as element '634-112/212 in the '634 Patent. Claim 1 of the '634 Patent recites "a front metal layer formed on the upper surface of said semiconductor region." (*See* Ex. 1001, '634 Patent, claim 1.)

[1b]
front metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

451. Uno ('864) discloses an analogous structure described as "a source electrode SE comprising an aluminum film 27" formed on the front surface of the

device. (*See* Ex. 1006, Uno ('864), 6:19–20; 7:1; Figs. 9, 11, 12, 15, 16, 18, 20, 24, 36–38, element 27.) Uno ('864) describes this aluminum film as being deposited in a single step–so that it provides both the contact plug (element 211 in the '634 Patent) *and* the front metal layer (element 212 in the '634 Patent). A POSITA familiar with integrated circuit manufacturing (particularly with the fabrication of the interconnect layers of an integrated circuit) would consider these to be two separate elements (the plug/via-fill, and the formation of the front metal layer) even if they are formed in the same step–since this type of approach was already well-known in the art by the time of the '634 Patent. In particular, this is what is done in copper metallization schemes–the via is filled and the metal line above is also filled at the same time (as can be seen in the description of copper metallization in Section VII.B). This "dual-damascene" method of building up the interconnect layers (where both the via-fill *and* the metal lines are copper) was already known by the time of the Filing Date of the '634 Patent. (*See* Ex. 1024, D. Edelstein et al., *Full Copper Wiring in a Sub-0.25 um CMOS ULSI Technology*, IEDM Technical Digest, 773-776 (1997). Although Uno ('864) does not use the term "front metal layer," a person of ordinary skill in the art would recognize that the aluminum film 27 corresponds to this structure–based on its location and function. Moreover, the use of aluminum in Uno ('864) is consistent with the '634 Patent's disclosure–which identifies AlSi and AlSiCu as preferred compositions

for the front metal layer. (AlSi and AlSiCu are alloys of aluminum that are commonly-used in metal interconnect layers–with small concentrations of silicon or silicon-and-copper added to the aluminum; this alloying technique has long been used in silicon process engineering–in order to make the aluminum lines more resistant to electromigration, and to mitigate some topographic problems. (*See* Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 191 (1990).)

Ex. 1006 ('864 Uno)

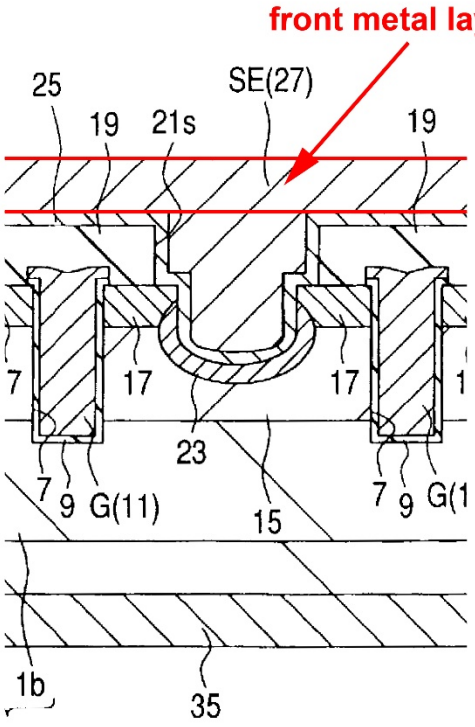


Fig. 38 (Annotated partial enlarged view)

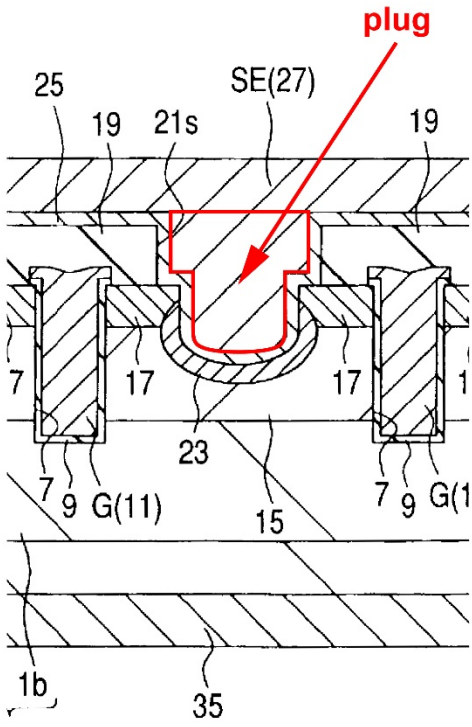


Fig. 38 (Annotated partial enlarged view)

452. Moreover, the function of Uno's aluminum film as a top-side, current-carrying layer is confirmed in multiple claims of the '864 patent, including claims

3, 5, 7, 9, 11, 14, 20, 27, and 31–34. These disclosures confirm that Uno (’864) includes a top-side metal structure that performs the same electrical and structural role and occupies the same location as the front metal layer of the ’634 Patent. This teaches the ’634 Patent requirement that the front metal layer be “formed on the upper surface of said semiconductor region.”

453. Accordingly, Uno (’864) discloses a front metal layer formed on the upper surface of the device that is both functionally and structurally equivalent to the front metal layer recited in the ’634 Patent. These disclosures teach limitation *[1b]*–“front metal layer”.

d. [1c]: “an interlayer oxide film formed between said source layer and said front metal layer,”

454. This claim element is taught by Uno (’864).

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Ex. 1006 ('864 Uno)

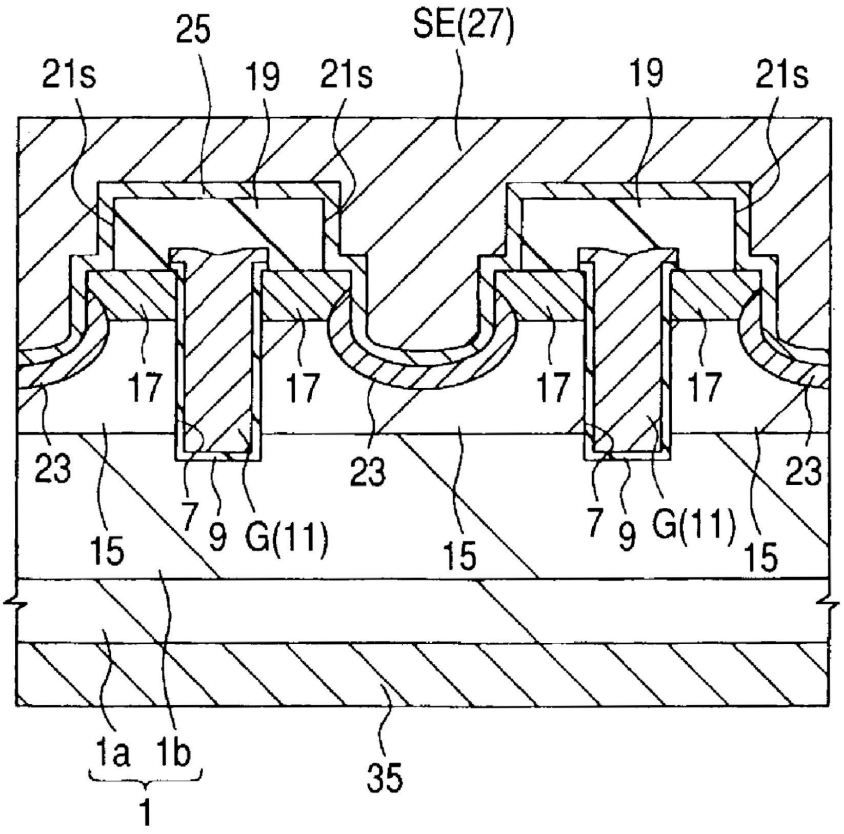


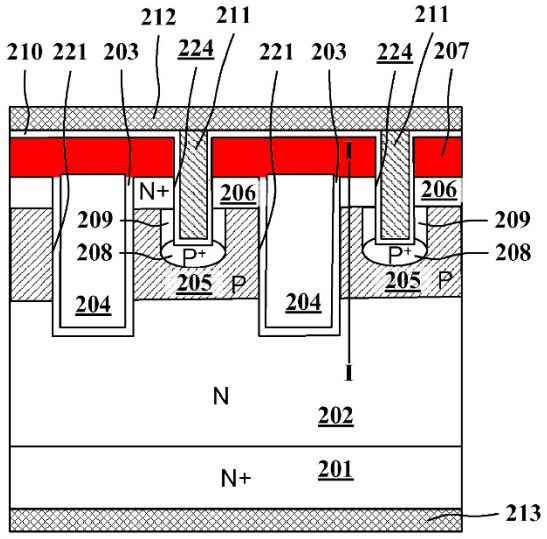
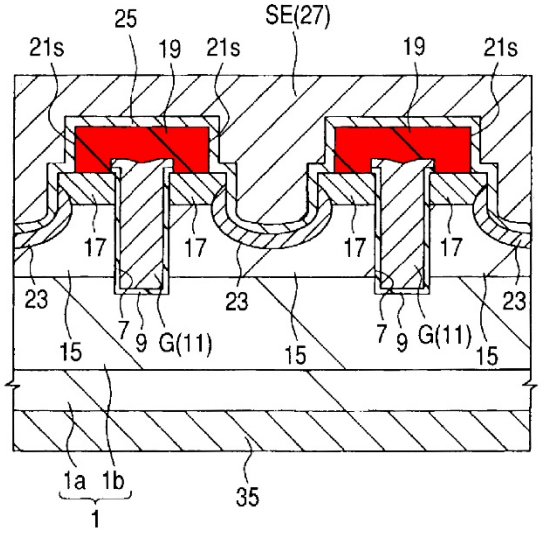
Fig. 38

455. ***[1c]: "interlayer oxide film."*** This limitation is disclosed in Uno ('864), which provides an interlayer oxide film corresponding to element '634-107/207 of the '634 Patent. The '864 patent discloses "silicon oxide film 19," which is formed over the semiconductor surface and functions as a dielectric insulating layer between the source region and the front metal contact. (*See* Ex. 1006, Uno ('864), 5:34, 5:49-50, 6:7-8, 6:65-66, 15:7, 15:10, 15:24-25, 15:31; Figs. 6, 8, 9, 11, 12, 14–16, 18, 20, 24, 36–38, element 19.) This identification is

repeated throughout the disclosure, and the silicon oxide film is clearly positioned between the source layer and the front metal layer. The function and placement of this oxide layer are consistent with long-standing practices in semiconductor device fabrication.

[1c]

interlayer oxide film

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

456. In the field of semiconductor engineering, the term silicon oxide is used interchangeably with silicon dioxide, a common insulating material widely used in semiconductor fabrication as an interlayer dielectric. As noted in the technical literature, "two dielectric workhorses in device fabrication are the silicon dioxide (SiO_2) and the silicon nitride (Si_3N_4). Aside from being used for masking purposes, the former is extensively used in electrical isolation." (*See* Ex. 1017,

Properties of SiO_2 and Si_3N_4 at 300K, Comprehensive Reference on EESEMI Semiconductor Manufacturing, https://eesemi.com/sio2si3n4.htm (last visited July 31, 2025).) Regardless of the specific oxide materials selected, such a choice would have been known to a POSITA at the time of the ’634 Patent filing and would yield the same functional result as the interlayer oxide film disclosed in the ’634 Patent. The admitted prior art depicted in Fig. 1 (Prior Art) of the ’634 Patent further confirms that a POSITA would have been motivated to implement the same interlayer oxide film structure claimed by the ’634 Patent.

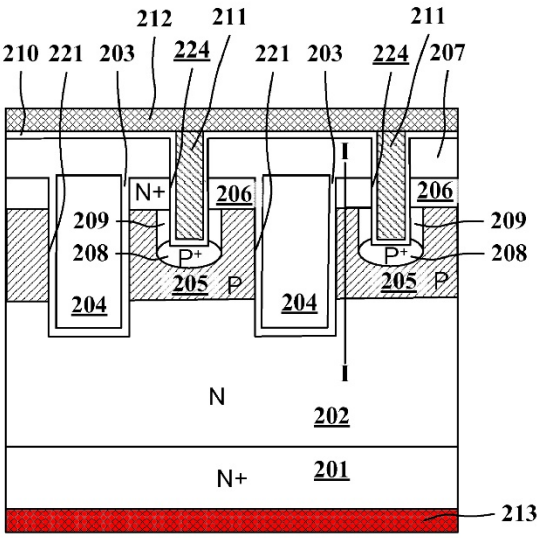
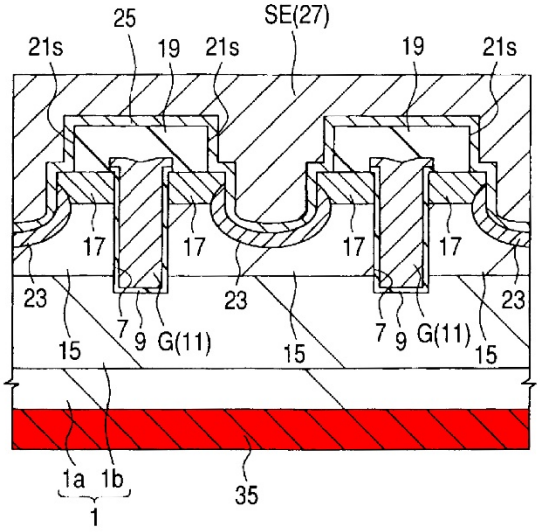
457. The positioning of oxide film ’864-19 above the source region and beneath the front metal layer confirms its function as an interlayer oxide film. These disclosures establish that Uno (’864) provides an interlayer oxide film consistent in both material composition and structural placement—situated between the source layer and the front metal layer—as recited in the ’634 Patent and therefore teaches limitation *[1c]–interlayer oxide film*.

e. [1d]: “a bottom metal layer formed on the lower surface of said semiconductor region;”

458. ***[1d]: “bottom metal layer.”*** This claim element is taught by Uno (’864).

[1d]

bottom metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

459. As can be seen, Uno (’864) element 35 is clearly formed on the lower surface of the semiconductor region. Uno (’864) identifies 35 as “a conductive film 35 forming a drain electrode” (Ex. 1006, Uno (’864), 6:20-21). Further, Uno (’864) also specifically identifies this “conductive film” as being composed of a metal of some type:

> Then, for example, an Ni (nickel) film, a Ti (titanium) film and a gold (Au) film are formed as conductive film successively on the rear face (1a) of the substrate 1 by sputtering to form a stacked film 35 thereof. The stacked film 35 forms a lead electrode (drain electrode DE) for the drain (1a, 1b). (Ex. 1006, Uno (’864) at 7:19-27.)

460. (Note that in the excerpt above, the term "lead" in "lead electrode" does not refer to the metallic element lead (i.e., Pb), but is instead pronounced "leed" and refers to a commonly used term in electronics denoting a wire or conductive path. In the context of semiconductor devices, "lead electrode" typically refers to a contact electrode used to electrically connect a specific terminal of a transistor to other components or circuitry. As further clarified in the excerpt, the "lead electrode" in this instance is more specifically identified as a "drain electrode," consistent with the interpretation set forth in the preceding paragraph.)

461. Thus, Uno ('864) clearly discloses a "bottom metal layer"–and thus teaches limitation *[1d]*.

462. Therefore, Uno ('864) discloses the entire claim element of "a bottom metal layer formed on the lower surface of said semiconductor region," consistent with the structure recited in the '634 Patent.

f. [1e]: "a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer, and"

463. This claim element is taught by Uno ('864).

Ex. 1006 ('864 Uno)

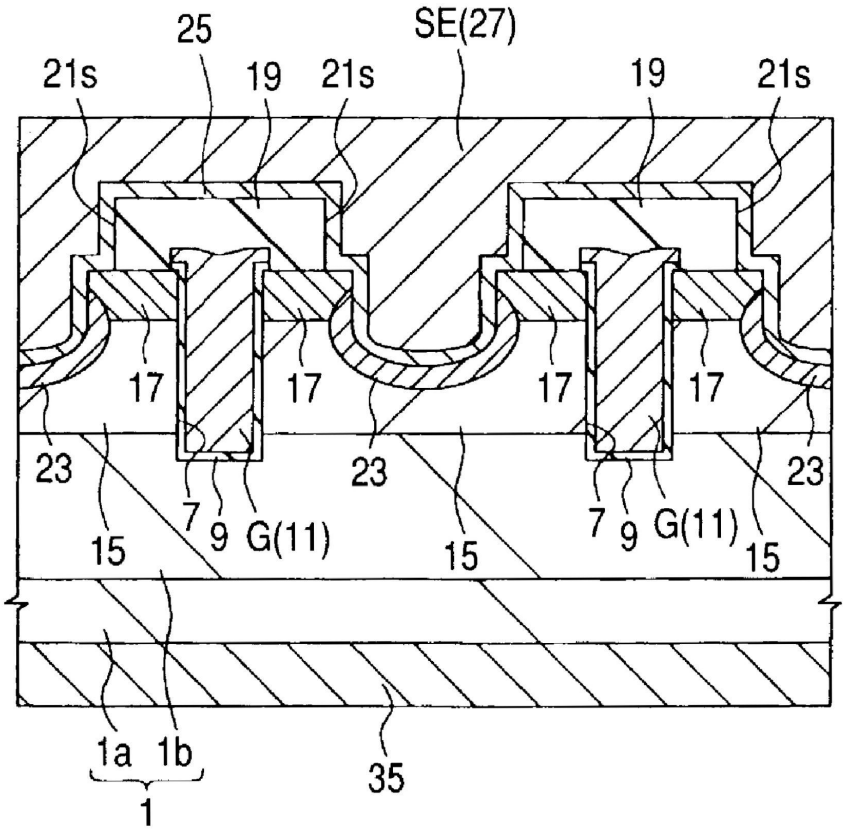


Fig. 38

464. Based upon the ordinary meaning of this claim as defined in Section XI.A.2.f, Uno ('864) also identifies 11 (G(11)) as being trenched gates, 19 as being an interlayer oxide film, 17 as the source regions that are formed in the larger-scale "source layer," 15 as the body regions that are formed in the larger-scale "base layer," 1b as an epitaxial layer; note that most of these layers were already identified in this way earlier. Further, these layers are arranged in the same manner as that required in the language of this claim element. Note further that the

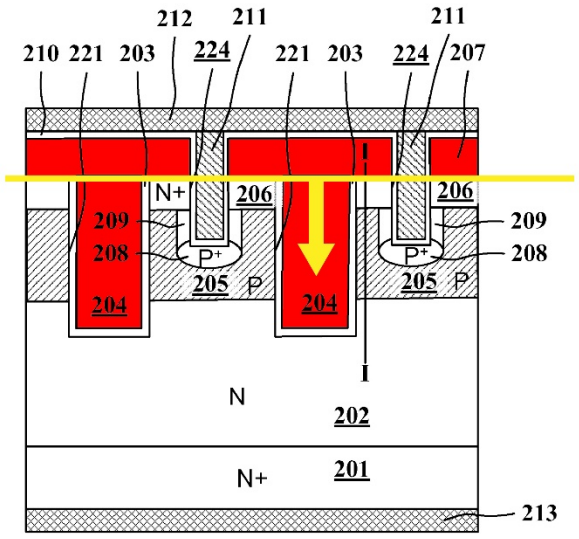
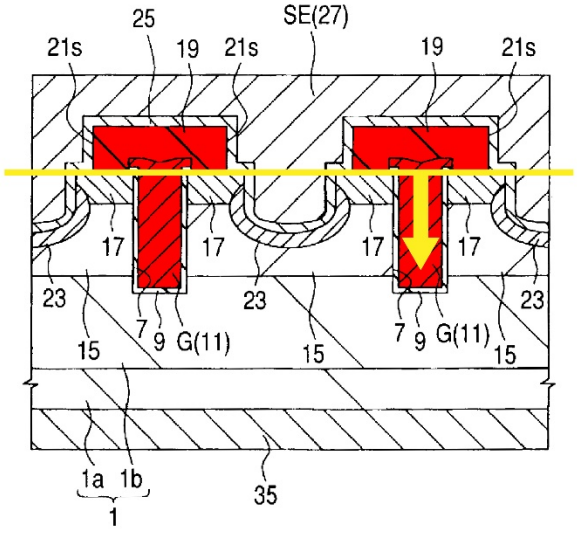
trenched gates extend downward from the top of the source layer, through the base layer to a portion of said epitaxial layer (that is, the trenched gate electrode extends downward so that the bottom is at a level that is below the bottom of the base layer and below the level of the top of the epitaxial layer–but does not extend further to the level of the bottom of the epitaxial layer).

465. This limitation is disclosed in Uno (’864), which provides trench gates corresponding to element ’634-104/204 of the ’634 Patent. These gates are covered by an interlayer oxide film (’634-107/207), are **“formed"** on top of the source layer (’634-106/206), and extend downwardly through the base layer (’634-105/205) to a portion of the epitaxial layer (’634-102/202).

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[1e]

a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

466. Uno ('864) discloses that "the polycrystal silicon film 11 in the trench forms a gate portion G of a power [device]," identifying the trench gate structure as comprising conductive material disposed within a trench. (*See* Ex. 1006, Uno ('864), 5:13-14; element 11.) The gate portion G is further described in connection with surrounding device regions, including the source, body, and drain layers, and is shown in numerous figures illustrating its vertical placement. (*Id.* 6:26-27, 6:59-60, 15:8, 15:18-19, 15:61-65; Figs. 5, 6, 8–9, 11–18, 20, 24, 36–38; claims 1, 12, 16–18, 25, 30–34, 37.) The oxide surrounding the gate within the trench corresponds to the interlayer oxide film and serves to insulate the gate from

adjacent semiconductor regions. The trench gate is formed above the source region and extends through the P-type channel/body region (’864-15) into the N-type epitaxial region (’864-1b), satisfying the vertical layer relationship recited in the ’634 Patent. Accordingly, Uno (’864) discloses trench gates with the structure and oxide insulation consistent with limitation *[1e]*.

467. Accordingly, it is my conclusion and opinion that Uno (’864) discloses limitation *[1e]*.

g. [1f]: “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer; wherein the bottom base of said trenches in said base layer are [sic] covered by the base contact layer.”

468. This claim element is taught by Uno (’864) or by Uno (’864) in combination with the knowledge of a POSITA.

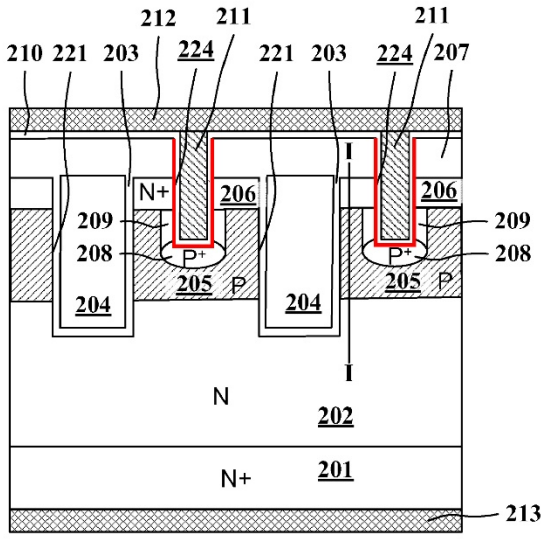
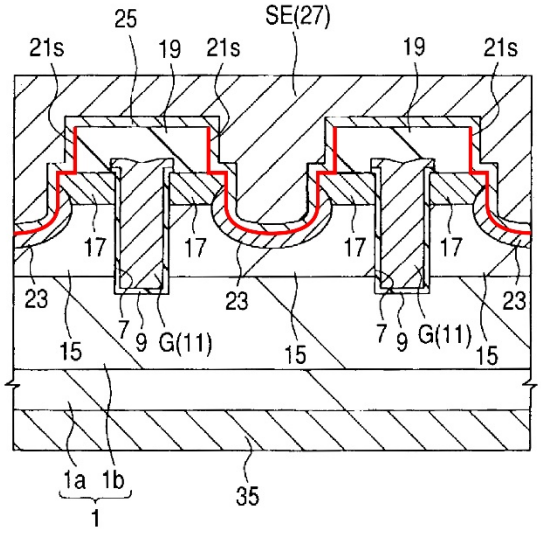
469. To simplify the analysis, this claim element will be split into claim sub-elements.

i. [1f-1]: “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer;”

470. This claim sub-element is taught by Uno (’864).

[1f-1]

a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

471. ***[1f-1]: "a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer".*** Limitation *[1f-1]* is disclosed in Uno ('864), which provides source contact trenches corresponding to elements '634-124/224 of the '634 Patent. Uno ('864) identifies layer 19 as the interlayer oxide film, layer 17 as the source regions formed within a larger-scale source layer, and layer 15 as the body regions formed within a larger-scale base layer—as previously described. These layers are arranged in the same vertical order and functional relationship as required by the language of this claim sub-element.

472. Uno (’864) further discloses that, following formation of the silicon oxide film 19, the film is etched in a patterned manner to form “contact trenches (source contact) 21s.” (*See* Ex. 1006, Uno (’864), 5:35-38; *see also* 5:45-48, 5:55-60, 6:22-27, 6:35-36, 15:10-15, 15:29-30, 15:35-36; Figs. 9, 12, 15, 16, 18, 20, 24, 36–38, element 21s.) These trenches are explicitly shown as being formed on top of the oxide film 19, which corresponds to the interlayer oxide film (’634-107/207), and extending downward through the source layer 17 and into a portion of the P-type base region 15 and therefore teaches limitation *[1f-1]*of the ’634 Patent.

473. For completeness, it should be noted that the “source contact trenches” are specifically identified via the annotations in the figure above. As detailed in Section XI.A.2a., the location and extent of the trench structures are defined when these trenches are etched and thus formed in the silicon; this clearly shows that the “source contact trenches” of this claim sub-element are both “formed on the top of said interlayer oxide film” and “[extend] downwardly through said source layer to a portion of said base layer.”

ii. [1f-2]: “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

474. This claim sub-element is taught by Uno (’864), or is rendered obvious by Uno (’864) in combination with the knowledge of a POSITA.

[1f-2]
wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer

Ex. 1006 ('864 Uno)

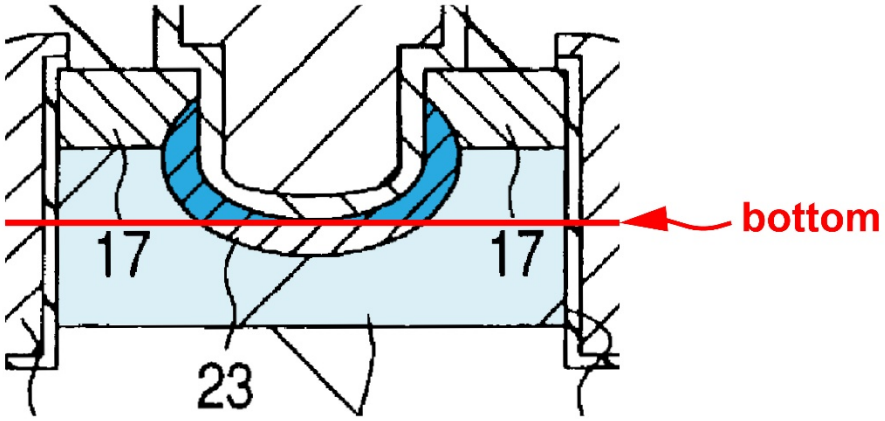


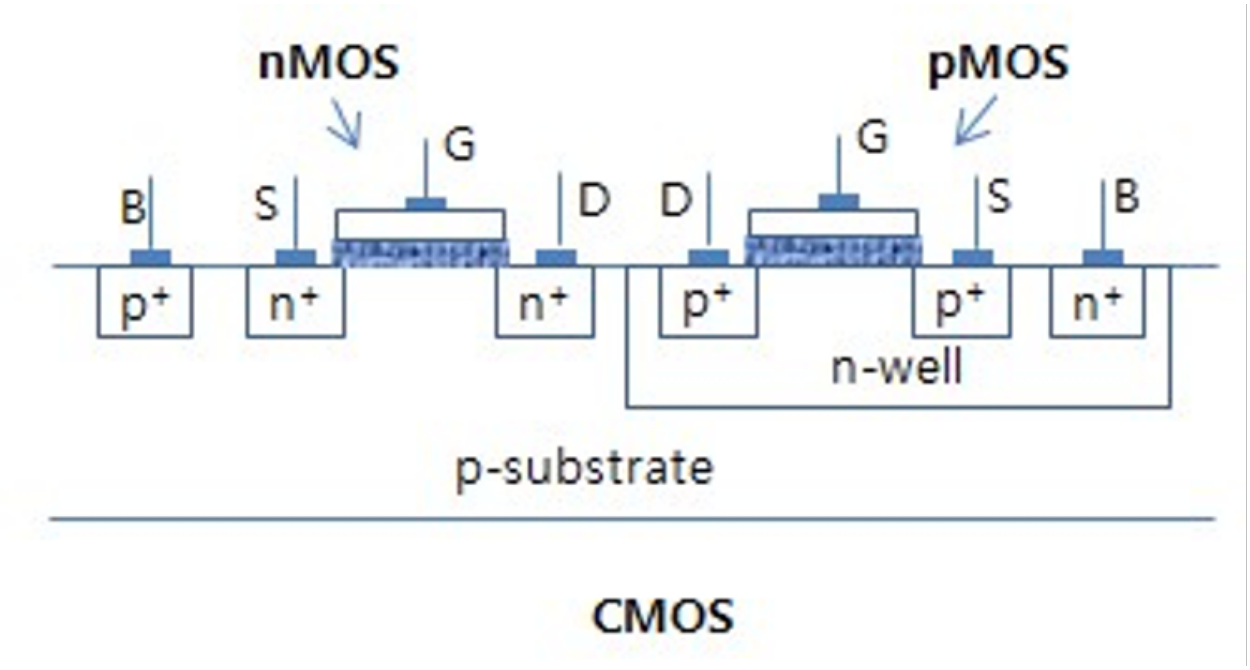
Fig. 38 (Annotated partial enlarged view)

475. ***[1f-2]:*** **"wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer".** Uno ('864) identifies 23 as a "p+-semiconductor region (back gate contact region)" (Ex. 1006, Uno ('864), 5:54-55.)–and further so-identifies 23 numerous other times in the specification. In the MOSFET art, "back gate contact" is another term for "body contact." The annotated portions of region 23 in Uno ('864) satisfy the claim sub-element requirement of providing a "lateral contact layer," as the lateral contact layer is positioned along the sidewalls of the source contact trenches. Although Uno ('864) does not explicitly label or describe the P^+ region (23) as comprising two

separately identifiable sub-regions, the portion of region 23 annotated above in darker blue corresponds to the "lateral contact layer" as defined in the '634 Patent.

476. To the extent that it must be shown why the shape of the entire contact layer is as depicted in Uno ('864), the reason for providing this form of body contact layer (in toto) was well-known in the art–and thus would have been well-known to a POSITA at the time of the '634 Patent.

477. As described above in the discussion associated with claim element *[1d]* of Ground 1 (in Section XI.A.2.e), it has long been common practice in transistor fabrication to place the body contact electrode on a pocket of heavily-doped silicon (doped either N+ or P+, as the situation requires); reprising the example provided there. (*See* illustrative image below.)



As explained earlier, the metal electrode body contact only comes into physical contact with the silicon within the heavily-doped pocket (either p+ or n+), as per the depiction above. As also explained earlier, this is specifically done to ensure that the body contact thus provided is a low-resistance ohmic contact–rather than the result were the contact to be placed in physical contact with the relatively-lightly-doped p-substrate or n-well, as this would produce either an ohmic contact with an unacceptably-large resistance or (worse) a non-ohmic contact (such as a Schottky contact). Anything other than a low-resistance ohmic contact would be detrimental to the electrical behavior and performance of the transistor.

478. In fact, Uno ('864) explicitly recognizes this situation–and clearly recognizes that a low contact resistance is important when a metallic material is used to provide contact to a semiconductor material (i.e., Ex. 1006, Uno ('864), 9:17-19)–and that the source contact should only come into contact with the body region via a surface layer that has been heavily-doped (i.e., p^+), for the reasons discussed in the prior paragraph. As explained in more detail above in Section XI.A.3 (where Ground 1 Claim 2 is considered), as long as both the labeled "P+" layer and the labeled "P*" layer have sufficient dopant concentrations to make both of them chemically "P+" material, they will provide the required low-resistance ohmic contact necessary for the trenched source contact to function properly when it comes in contact with the silicon of the body region.

479. Thus, a POSITA would understand that a structure in which the metal contact plug makes contact with the body region only through a layer of heavily-doped silicon is required–as per the commonly-used and well-known practice, as described above–and for reasons as described above and as also explicitly stated by Uno ('864).

480. In order for this p+-doped layer to "surround" the source-body contact, this doped layer must extend upward so that it is present in the sidewalls of the trench that are part of the body region; this is what is depicted in Uno ('864)–and thus, this is the "lateral contact layer" of this claim sub-element. Accordingly, Uno ('864) discloses "sidewalls of said trenches in said base layer are covered by the lateral contact layer," as required by *[1f-2]*.

iii. [1f-3]: "wherein the bottom base of said trenches in said base layer are [sic] covered by the base contact layer."

481. This claim sub-element is taught by Uno ('864), or is rendered obvious by Uno ('864) and the knowledge of a POSITA.

[1f-3]
wherein the bottom base of said trenches in said base layer are [sic] covered by the base contact layer

Ex. 1006 ('864 Uno)

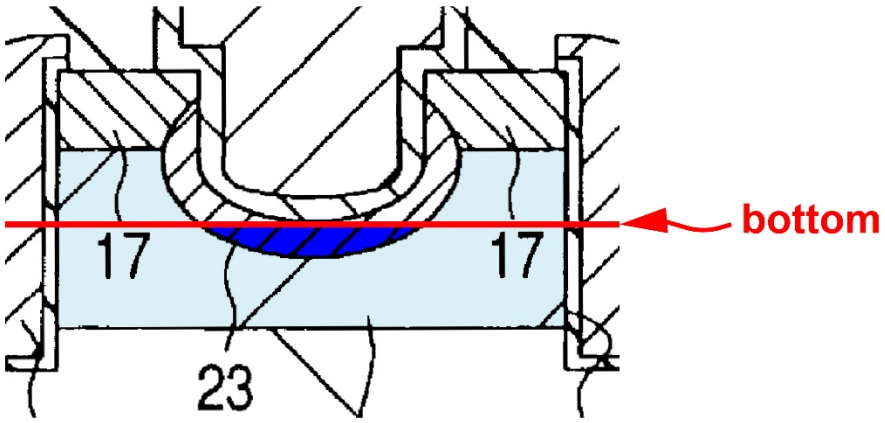


Fig. 38 (Annotated partial enlarged view)

482. The as-annotated portions 23 meet the claim sub-element requirement of providing a "base contact layer." As shown in the annotated Fig. 38 above, Uno provides the structure and function of trench 21s—extending into a portion of the base layer, with the base contact layer 23 covering the bottom of the trench in order to provide a low-resistance ohmic contact to the base layer 15. (Ex. 1006, Uno ('864), 15:10-13, 15:31-36, Fig. 6.) Although Uno ('864) does not label or describe the regions of the identified P+ layer as consisting of two separately-identifiable regions, the part of the P+ region annotated above in darker blue is a base contact layer.

483. As discussed in the claim construction analysis above, the ’634 Patent explicitly defines the “base contact layer” as existing at the bottom of the source contact trench within the base layer; this is what is depicted in Uno (’864).

484. To the extent it is necessary to explain why the contact layer in Uno (’864) is shaped as depicted—and why it is formed in that particular configuration—this issue has already been addressed above in the discussion of claim sub-element *[1f-2]*, in Section XI.A.2.g.ii. Accordingly, Uno (’864) discloses that “the bottom base of said trenches in said base layer [is] covered by the base contact layer,” as required by limitation *[1f-3]*.

h. Claim 1 Summary.

485. For all of the reasons described above, Claim 1 of the ’634 Patent is rendered obvious by Uno (’864) and the knowledge of a POSITA; some claim elements are taught by Uno (’864) alone, while others are rendered obvious by Uno (’864) in combination with the knowledge of a POSITA.

3. Claim 2: “The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type; the base layer and lateral contact layer are P-type; and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

486. Claim 2 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown

above (in Section XI.B.2) that Claim 1 of the '634 Patent is rendered obvious by Uno ('864) and the knowledge of a POSITA.

487. The remainder of Claim 2 is also rendered obvious by Uno ('864) and the knowledge of a POSITA.

488. To simplify the analysis, this claim will be split into claim elements.

a. [2a]: "wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;"

489. This claim element is taught by Uno ('864).

Ex. 1006 ('864 Uno)

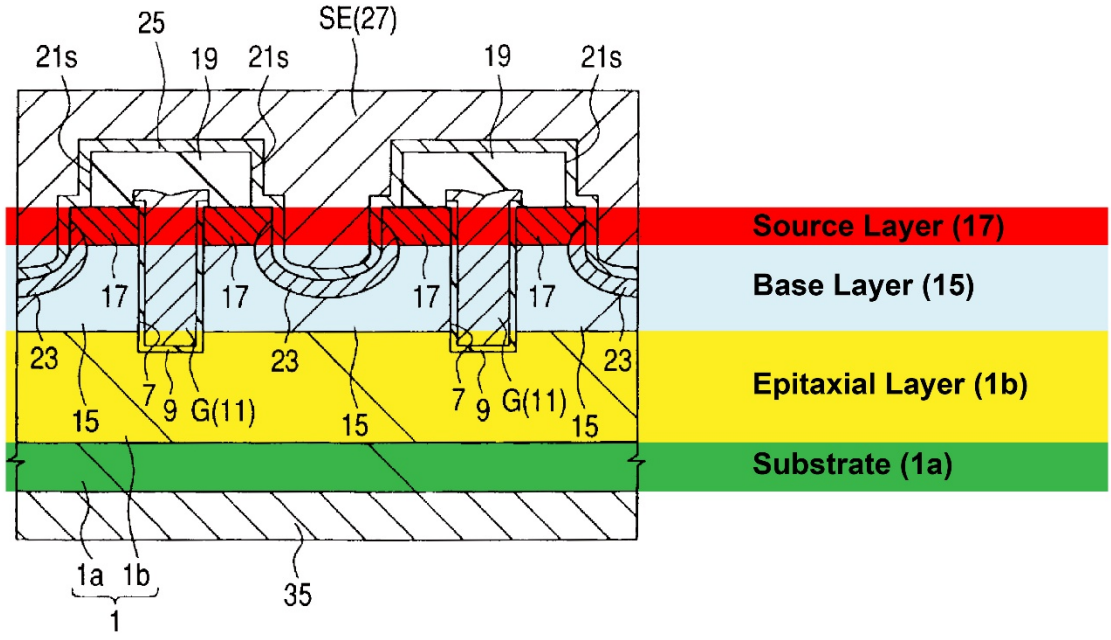
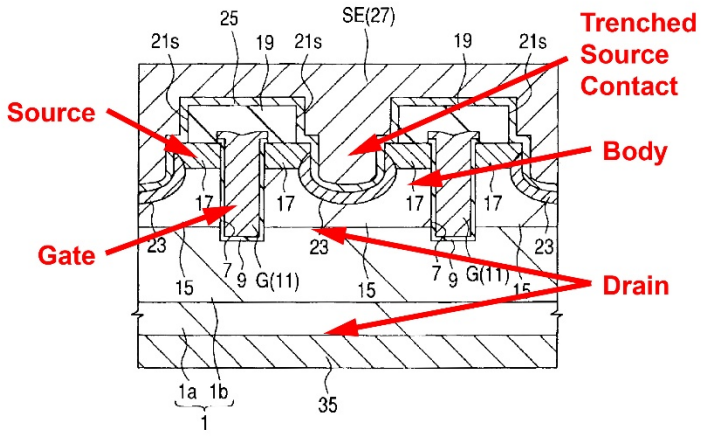
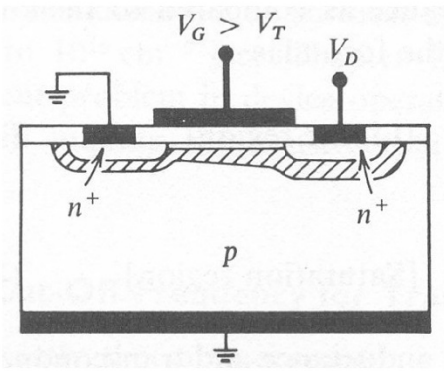


Fig. 38 (Annotated)

490. In this figure, Uno ('864) identifies the substrate 1a and the epitaxial layer 1b as being "N-type" (*see* Ex. 1006, Uno ('864), 4:55-59), and the source

layer (which here has been divided up into the source regions 17) as being "N-type" (*Id.* at 5:26-29), the base layer (which here has been divided up into the body regions 15) as being "P-type" (*Id.* at 7:21-23), and the lateral contact layer (as described in the discussion of claim sub-element *[1f-2]* (in Section XI.C.2.g.ii)) as being "P-type," and the source contact trenches as having a P-type base contact layer (as described in the discussion of claim sub-element *[1f-2]* (in Section XI.B.2.g.ii)) at the bottom of those trenches.

491. It should also be noted that the transistor depicted in Uno ('864) Fig. 38 is readily-identified as being an nMOS type of transistor.

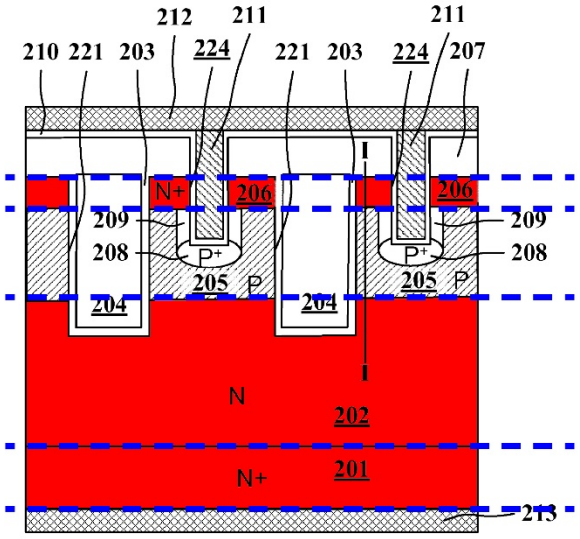
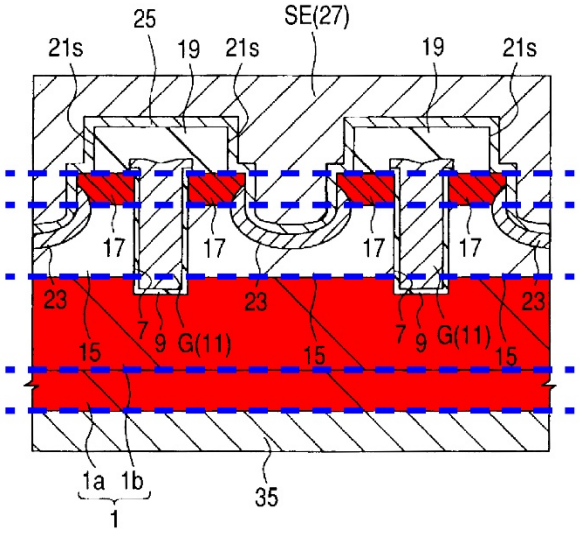
Ex. 1006 ('864 Uno)	**Ex. 1018, A. S. Grove, *Physics and Technology of Semiconductor Devices*, 330 (1967)**
 ***Fig. 38 (Annotated)***	 ***Fig. 11.8 (Annotated partial enlarged view)***

492. The claim element above is, among other things, a verbose way of stating that the transistor structure described therein is an nMOS transistor.

493. This limitation *[2a] [2a]* is disclosed in Uno ('864), which provides an N-type silicon substrate (1a), an N-type epitaxial layer (1b), and an N-type source layer (17), corresponding respectively to elements '634-101/201, '634-102/202, and '634-106/206 of the '634 Patent.

[2a]

N-type silicon substrate, epitaxial layer, & source layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

494. Uno ('864) discloses "an n-single crystal silicon substrate 1a," which forms the foundational layer of the device, and "a single crystal silicon layer 1b" epitaxially grown on top of the substrate. (*See* Ex. 1006, Uno ('864), 4:55-59; Figs. 1, 3, 5, 6, 8–9, 11–18, 20, 36–38, elements 1a and 1b.) The epitaxial layer 1b, grown on the N-type substrate 1a, serves as the drain-side region in the vertical device structure, consistent with the epitaxial layer in the '634 Patent.

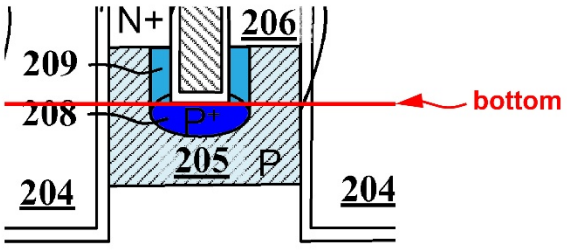
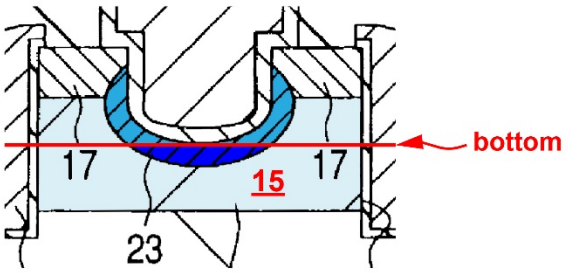
495. Above the epitaxial structure, Uno ('864) discloses "an n+-semiconductor region 17," which functions as the source layer. This highly doped N+ region is located above the P-type channel region 15 and is used for forming the source contact. (*Id*. at 5:29–31, 5:35–36, 5:43-44, 6:10-11, 6:26-27, 8:25-29, 8:44, 8:60-61; Figs. 5, 6, 8–9, 11–18, 20–22, 24–25, 36–38, element 17.)

496. Accordingly, Uno ('864) discloses a layered semiconductor structure comprising an N-type substrate, an epitaxial N-type drain layer, and an N-type source region and therefore teaches limitation *[2a]*.

b. [2b]: P-type base layer & P-type "lateral contact layer." Limitation

497. Limitation *[2a-2]* is disclosed in Uno ('864), which provides a P-type base layer and a lateral contact layer corresponding to elements '634-105/205 and '634-209 of the '634 Patent. The '634 Patent identifies the P-type base layer as corresponding to the body region of the MOSFET structure–where, as explained earlier (in Section VIII.A), the body regions are subsets of the larger base layer. Uno ('864) discloses a "p–semiconductor region (channel region) 15," which functions as the P-type base or body layer within the vertical structure. (*See* Ex. 1006, Uno ('864), 5:65; Figs. 5, 6, 8, 9, 11–16, 18, 20–22, 25, 36–38, element 15; *see also* claims 1, 12, 16, 18, 25, 29, 31, 33–36.)

[2b]
P-type base layer & lateral contact layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

498. Uno (’864) also discloses a “p+-semiconductor region (back gate contact region) 23” which is formed within the P-type base region. (*Id*. at 5:54-55; *see also* 5:57-60, 5:64-65, 6:11-13, 8:40-43, 8:52; Figs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38, element 23.) This P+-doped region, located along the sidewalls of the source contact trenches, corresponds to the “lateral contact layer” (’634-209) described in the ’634 Patent and provides ohmic contact between the base and the source contact structure.

499. As explicitly stated in the ’634 Patent, the lateral contact layer (’634-209) is formed along the sidewalls of the source contact trench above the trench bottom within the base layer, while the base contact layer (’634-108/208) is formed at or beneath the trench bottom. (*See* Ex. 1001, ’634 Patent, 5:9–12; 3:50–55.) This structural distinction confirms that the sidewall region in Uno (’864)—where P+-type region 23 is formed—must be located above the trench bottom (*See* Ex. 1006,

Uno ('864), 5:59-61), within the P-type base layer ('634-105/205), while any base contact layer would be situated deeper, at or below the trench floor and interfacing with deeper portions of the base.

500. As shown in Fig. 38, the source contact trenches in Uno ('864) are tapered, resulting in angled trench sidewalls. During ion implantation, this geometry increases the projected surface area of the sidewalls, which in turn reduces the effective dopant dose density compared to the trench bottom. The trench bottom receives ions at normal incidence over a smaller projected area, leading to a higher doping concentration. Therefore, even though region 23 is described as "P+," the doping concentration along the trench sidewalls must inherently be lower than that at the trench bottom—an outcome dictated by the physical geometry, not dependent on any express recognition in the prior art.

501. Accordingly, Uno ('864) discloses both a P-type base layer and a P-type lateral contact layer positioned along the trench sidewalls—above the trench bottom—with the lateral contact layer inherently exhibiting a lower doping concentration than the base contact layer due to geometric implantation effects. This teaches limitation *[2b]* as claimed and as discussed in the petition.

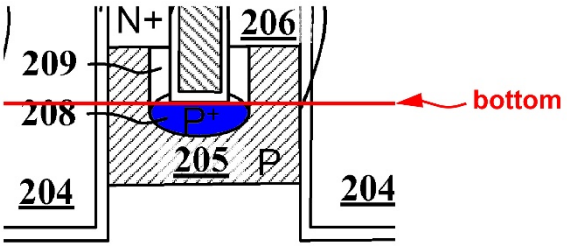
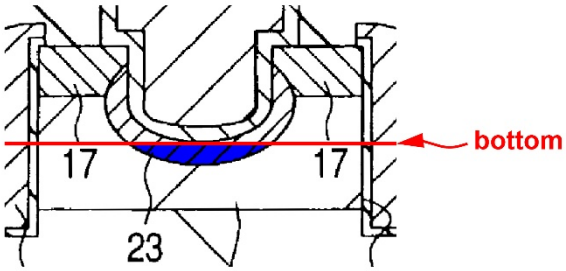
c. [2c]: P-type base contact layer at bottom of source contact trenches.

502. Limitation *[2c]* is disclosed in Uno (’864), which provides a P-type base contact layer corresponding to element ’634-108/208 of the ’634 Patent. The ’634 Patent defines the base contact layer as a P+-type diffusion region formed at or beneath the bottom of the source contact trench, providing direct ohmic contact to the deeper portion of the P-type base. (*See* Ex. 1001, ’634 Patent, 3:50–55; 5:9–12.)

503. Uno (’864) discloses a corresponding structure in the form of a “p+-semiconductor region (back gate contact region) 23,” which is formed within the P-type base region. (*See* Ex. 1006, Uno (’864), 5:54-55; *see also* 5:58-60, 5:63-64, 6:13, 8:40-42, 8:51-52; Figs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38, element 23.) Region 23 is situated beneath the source region (element 17) and at the bottom of the source contact trench (element 21s), making contact with the underlying P-type channel region (element 15). Its vertical position and function—providing ohmic connection to the body—correspond to the base contact layer (’634-108/208) in the ’634 Patent.

[2c]

P-type base contact layer at bottom of source contact trenches

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
 *Fig. 2G (Annotated partial enlarged view)*	 *Fig. 38 (Annotated partial enlarged view)*

504. Although Uno (’864) refers to this region as a “back gate contact region,” its structure and electrical role mirror those of the base contact layer in the ’634 Patent. It is located at or beneath the trench bottom, where it enables vertical conduction from the base region to the source electrode through the filled trench. This placement is distinct from the lateral contact layer, which the ’634 Patent identifies as being formed along the trench sidewalls.

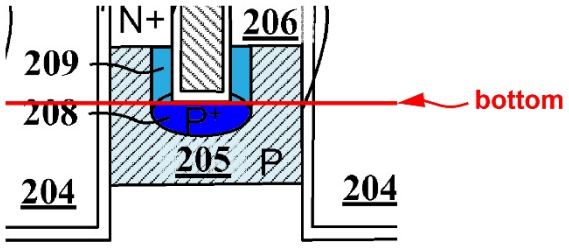
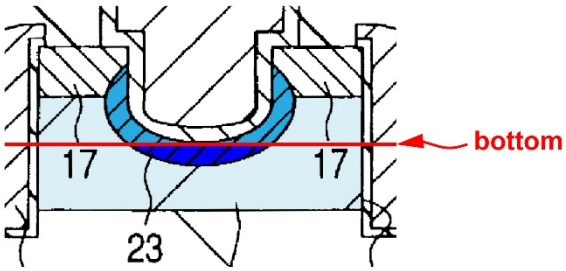
505. Accordingly, Uno (’864) discloses a P+-type base contact layer located at the bottom of the source contact trench, which provides ohmic contact to the P-type base region. This structure discloses both the spatial and functional characteristics of element ’634-108/208 and teaches limitation *[2c]*.

d. [2d]: "and the lateral contact layer has less doping concentration than the base contact layer at bottom."

506. This claim sub-element, which I refer to as limitation *[2d]*, is rendered obvious by Uno ('864) and the knowledge of a POSITA.

507. As explicitly described in the '634 Patent, the lateral contact layer is formed along the sidewalls of the source contact trench above the trench bottom within the base layer, while the base contact layer is formed at or beneath the trench bottom. (*See* Ex. 1001, '634 Patent, 5:9–12; 3:56-65.)

[2d]
lateral contact layer has less doping concentration than the base contact layer at bottom

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated partial enlarged view)	*Fig. 38 (Annotated partial enlarged view)*

508. Uno ('864) discloses the formation of a P+-type semiconductor region 23, referred to as the "back gate contact region," which is located within the base region 15 and in the vicinity of the source contact trench (element 21s). (*See* Ex. 1006, Uno ('864), 5:54-55, 5:58–5:64; Figs. 8–9, 11–12, 14–16, 18, 20–22, 25, 36–38.) Region 23 corresponds to both the "lateral contact layer" (as marked in

medium blue) when present on the trench sidewalls above the trench bottom within the base layer, and the "base contact layer" (as marked in dark blue) at or beneath the trench bottom.

509. In Uno ('864), the trenches are sloped (i.e. tapered). During ion implantation, this geometry causes the sloped sidewalls to receive a reduced dopant dose due to the increased projected surface area, while the trench bottom—being flat and perpendicular to the ion beam—receives a more-concentrated implant. As a result, even though the same P+ region 23 label is used, the doping concentration along the sidewalls is inherently lower than that at the trench bottom.

510. This differential in doping is a physical inevitability based on trench geometry and implantation physics–and under the doctrine of inherency, does not require explicit acknowledgment in the prior art. Accordingly, Uno ('864) inherently discloses a lateral contact layer that has lower doping concentration than does the base contact layer–and therefore teaches the limitations of the '634 Patent.

511. Support for this inherent physical principle is found in Uno ('864). Uno ('864) describes a method of forming a doped layer that results in a heavily doped region within the body regions of the transistor. This doped region is intended to ensure complete coverage of the surface area where the metal plug of the source contact physically contacts the body region—thereby promoting low-resistance ohmic contact. This disclosure aligns with and reinforces the analysis

provided in the discussion of claim sub-element *[1f-2]* in Section XI.B.2.g.ii, as illustrated in the following excerpt:

> [A] p-impurity, for example, boron fluoride (BF2) is implanted to the bottom of the contact trench 21S and diffused to form a p-semiconductor region (back gate contact region) 23. (Ex. 1006, Uno ('864) at 5:52-55; *see also* 6:11-13.)

512. Uno ('864) describes this process as involving both being "implanted" (i.e., ion implantation) and then being "diffused" (i.e., a heat cycle is used to activate the implant and to spread the dopant atoms out further from where they were right after the implant step was completed)–resulting in the p+ layer 23 depicted in Fig. 38; note that this (i.e., implantation followed by an activation and diffusion-causing heat cycle) is a common method of forming doped layers in silicon. (*See* Ex. 1022, Michael Quirk and Julian Serda, *Semiconductor Manufacturing Technology*, 475 (2001).)

513. However, it would be obvious to a POSITA that the concentration of dopants in this configuration would be less on the sidewalls of the trench than on the bottom of the trench–because of some very simple aspects of basic geometry. This topic was already considered in great detail earlier (in Section X.A.3.b)–and that discussion is incorporated by reference here.

514. As noted above, the concentration of dopant atoms at a surface decreases when the angle of implantation becomes steeper. Accordingly, it is

inherent in the teachings of Uno ('864) that the sidewalls of the trench—i.e., the lateral contact layer—will exhibit a lower dopant concentration than the trench bottom (i.e. base contact layer). This outcome is an inherent result of the geometry of angled implantation and would be present in the resulting structure even if not expressly recognized by Uno ('864) at the time of the invention. Under established principles of inherency, this claim element is considered taught by the prior art so long as it necessarily results from the disclosed process, regardless of whether-or-not it was appreciated by the inventor. Moreover, this inherent physical principle was well understood by POSITA at the time of the '634 Patent's filing, as evidenced by extensive research into the variations in doping profiles resulting from implantation into trench surfaces with different slopes. (*See* Ex. 1021, S.E. Berberich et al., *Trench Sidewall Doping for Lateral Power Devices*, Conference on European Solid-State Device Research Conference, 379-382 (2003).)

515. However, it has also long been known that it is difficult, using ion implantation, to produce doping concentrations that are uniform around the implanted sides of the trench (i.e., the bottom of the trench and the sidewalls of the trench will have different doping concentrations). A major mechanism that induces this problem is simply that some of the ions striking the sidewall of the trench will not penetrate into the silicon–but rather will "reflect" off the sidewall and travel on to elsewhere in the structure.

516. This situation was considered in detail earlier, also in Section (XI.A.3.b)–and that discussion is here incorporated by reference.

517. In summary, the trench bottom receives ions at a direct, perpendicular angle and, as a result, over a smaller effective surface area—yielding a higher doping concentration. Consequently, as also explained above, the P^+ region along the sidewalls (i.e., the lateral contact layer) inherently receives less dopant per unit surface area than the base contact region at the trench bottom. This outcome is dictated by general physical, mathematical, and geometrical principles, as well as the basic physics of ion implantation in trench geometries. As discussed in Section X.A.3, this result does not require explicit recognition in the prior art to satisfy inherency. Nevertheless, this effect was widely understood by a POSITA at the time. Accordingly, Uno ('864) inherently discloses a lateral contact layer with a lower doping concentration than that of the base contact layer.

4. Claim 3: "The trenched MOSFET of claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

518. Claim 3 is a dependent claim–and depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2 and Section

XI.B.3) that Claim 1 and Claim 2 of the '634 Patent are either taught by Uno ('864) or rendered obvious by Uno ('864) and the knowledge of a POSITA.

519. The remainder of Claim 3 is taught by Uno ('864), or Uno ('864) in view of the knowledge of a POSITA.

520. Uno ('864) specifically identifies 25 as being a "barrier film" (Ex. 1006, Uno ('864), 6:18-19), and 27 (SE27) as being "a source electrode SE comprising an aluminum film" (Ex. 1006, Uno ('864), 6:19-20).

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Ex. 1006 ('864 Uno)

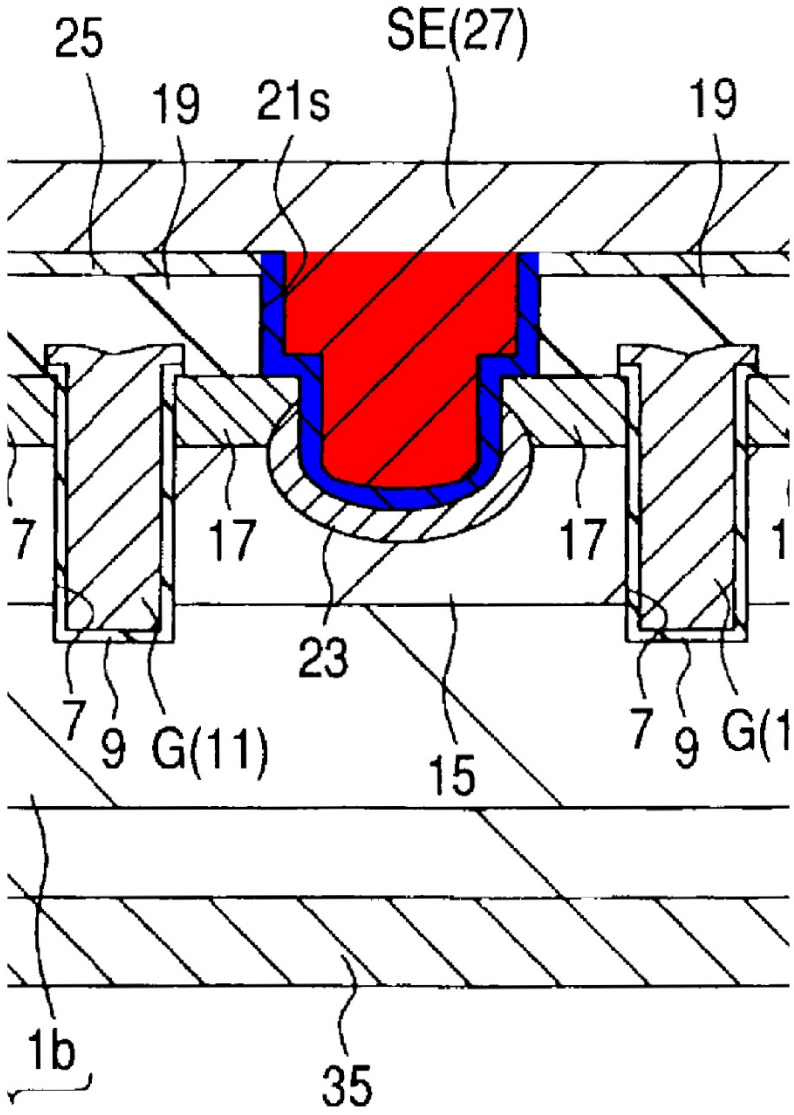


Fig. 38 (Annotated partial enlarged view)

521. The annotations above identify the portion of the "electrode" (27/SE27) that constitutes the "contact metal plugs" (annotated in red); this is the term that is commonly-used in the art for a contact that is formed in a via-type of hole that reaches down to whatever it is that the contact plug is contacting–and

the ’634 Patent, of course uses this language to describe this structure. Note also that aluminum is a metal. In addition, in this particular case, the trench bottom and the trench sidewalls are first covered with the also-identified barrier metal layer (annotated in blue)–for reasons explained earlier.

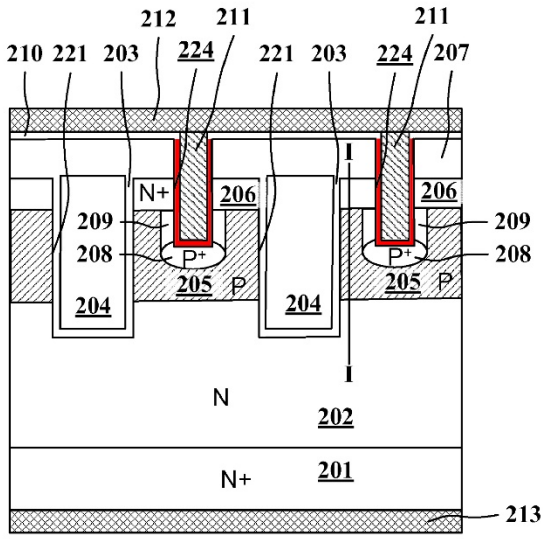
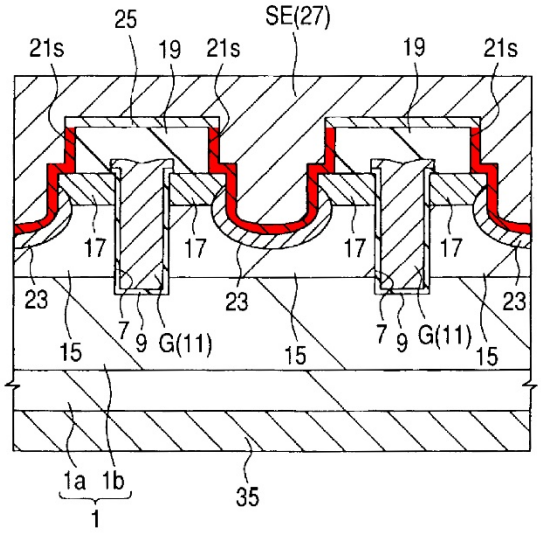
522. To the extent that a POSITA would regard the single aluminum layer of Uno (’864) as containing both the contact plug *and* the front metal layer in the same singlely-deposited aluminum layer, it was described earlier (in Section (XI.B.2.c) that this is how copper dual-damascene interconnects are formed in integrated circuits–and that this was already a well-known technique in the semiconductor fabrication art by the Filing Date of the ’634 Patent (2008); that earlier discussion is here incorporated by reference.

a. [3a]: “barrier metal layer.”

523. Limitation *[3a]* is disclosed in Uno (’864), which provides a barrier metal layer corresponding to element ’634-110/210 of the ’634 Patent. The ’634 Patent describes the barrier metal layer as a Ti/TiN or equivalent material interposed between the tungsten plug and the underlying oxide or silicon that is included to prevent diffusion and to maintain the integrity of the electrical contact (such as by serving as an adhesion layer). (*See* Ex. 1001, ’634 Patent, 5:15–20; 6:18–20; Figs. 2F–2G, 15.)

[3a]

barrier metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

524. Uno (’864) likewise discloses a barrier film (element 25) performing the same function. Specifically, Uno (’864) states: “Barrier films (barrier metal films) are formed to connection portions with wirings or semiconductor substrates for preventing formation of undesired reaction layers or deposition of underlayer material caused by the contact of material constituting them.” (*See* Ex. 1006, Uno (’864), 1:23-25; *see also* 15:18-20, 30-37.)

525. Uno (’864) further teaches the use of the same barrier metal materials as those disclosed in the ’634 Patent. Uno (’864) explains that “characteristics of the device can be improved by using different films for the respective barrier films, while using a metal having a relatively higher barrier height ΦB to n-Si (for

example, MoSi2) in the case of the n-channel type and using a metal having a relatively lower barrier height ΦB to the n-Si (for example, **TiN)** in the case of the p-channel type." (*Id*. at 14:61-67 (*emphasis added*).)

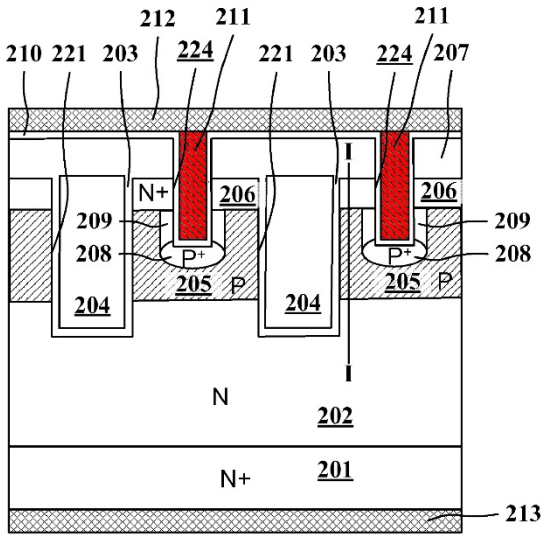
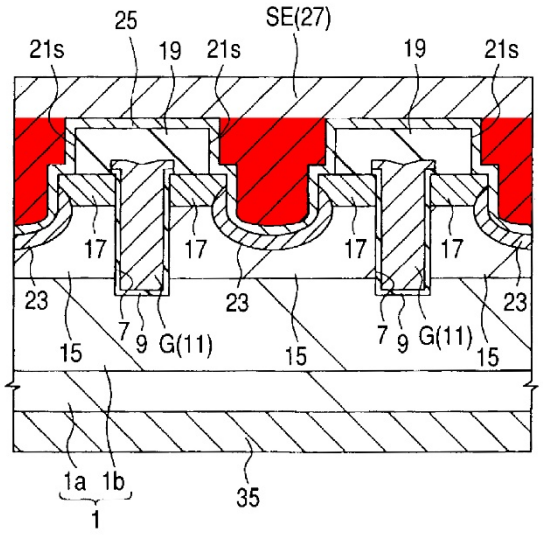
526. Accordingly, Uno ('864) discloses a barrier metal layer structurally and functionally consistent with element '634-110/210 and therefore teaches limitation *[3a]*.

b. [3b]: "contact metal plugs."

527. Limitation *[3b]* is disclosed in Uno ('864), which describes contact metal plugs corresponding to element '634-111/211 of the '634 Patent. The '634 Patent defines the contact metal plug as a conductive material, such as tungsten, deposited into the source contact trench to establish electrical connection between the buried contact regions and the upper metal interconnect. (*See* Ex. 1001, '634 Patent, 5:13–20, 5:44–46; Figs. 2F–2G, elements 111 and 211.)

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[3b]
contact metal plugs

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

528. Uno ('864) discloses a functionally and structurally identical element. Specifically, Uno ('864) states: "The embodiment described above may also be applied to a conductive portion connected electrically with the source or drain and well (for example, **plugs** or wiring portions)." (*See* Ex. 1006, Uno ('864), 16:12–15 (e*mphasis added*).)

529. Furthermore, a POSITA would understand that a structure in which the metal contact plug makes contact with the body region reflects a commonly used and well-known practice in the art, as described above and as explicitly stated by Uno ('864).

530. Accordingly, Uno (’864) discloses contact metal plugs that are consistent in both structure and function with element ’634-111/211 and therefore teaches limitation *[3b]*.

5. Claim 4: “The trenched MOSFET of claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is [t]ungsten.”

531. Claim 4 is a dependent claim–and depends from Claim 3, which depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2, Section XI.B.3, and Section XI.B.4) that Claim 1, Claim 2, and Claim 3 of the ’634 Patent are either taught by Uno (’864) or rendered obvious by Uno (’864) in view of the knowledge of a POSITA.

532. The remainder of Claim 4 is also rendered obvious by Uno (’864) and the knowledge of a POSITA.

533. It was shown above that Uno (’864)–or Uno (’864) in view of the knowledge of a POSITA teaches Claim 3–which requires the presence of “a barrier metal layer and a plurality of contact metal plugs.” However, Claim 3 describes only the structures while not identifying any specific materials that are used–while Claim 4 specifies that the barrier layer must be composed of “Ti/TiN” and the “contact metal plugs” must be composed of tungsten.

a. [4a]: "barrier metal layer is Ti/TiN."

534. Uno ('864) explicitly teaches the use of titanium (Ti) and titanium nitride (TiN) as materials for the barrier metal layer. As stated in the disclosure: "In addition to Ti, TiN (titanium nitride) may also be used." (Ex. 1006, Uno ('864), 13:9–10.) Although, Uno ('864) does not explicitly teach tungsten as a specific material for the contact metal plugs; it is my conclusion and opinion that a POSITA, confronted with Uno ('864) and pondering how to deploy Uno ('864) into a more "typical" process flow, would select Ti/TiN for the barrier metal layer and would use a tungsten plug rather than an aluminum plug–as the former has been typical for use as a barrier metal layer, and the latter is the typical plug material that is used (and formed separately from the overlying aluminum layer of the "front metal layer" that appears in both Uno ('864) and the '634 Patent.

535. With regard to the barrier metal layer, Uno ('864) identifies several materials for use (and under certain particular conditions–such as if the barrier metal layer is contacting n+ silicon or p+ silicon). For example, in addition to Ti and TiN, Uno ('864) describes the use of molybdenum silicide (MoSi2) (Ex. 1006, Uno ('864), 6:64-65), as well as the use (in an alternative embodiment) of TiW (Ex. 1006, Uno ('864), 7:56); Uno ('864) also provides tables (in Fig. 30 and Fig.

31) that contain possible other metallic materials that could be used to provide a "metal barrier layer."

536. Thus, as a POSITA using the more-typical Ti/TiN system for the barrier metal layer would not be discouraged from using the teachings of Uno ('864) if that POSITA had only a Ti/TiN process available to him/her; rather, such a POSITA would be motivated (by both this knowledge of an extant Ti/TiN system *and* by the explicit teachings of Uno) to substitute in the available Ti/TiN process–and would have a reasonable expectation of success, given that a Ti/TiN barrier metal is so commonly used throughout the industry–and has been for some time.

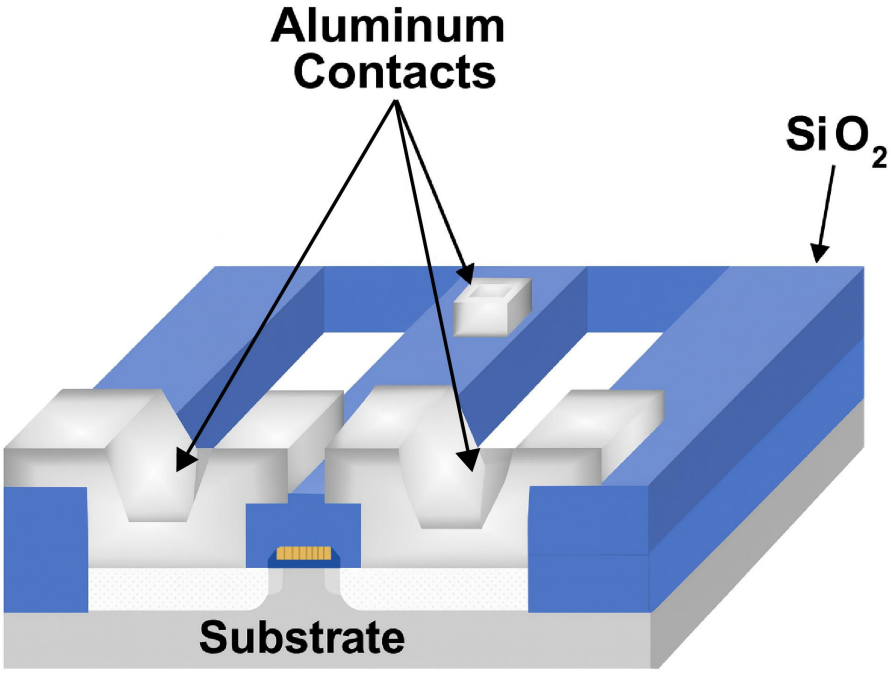
537. The same situation would occur if a POSITA were confronted by Uno ('864)'s use of a single layer of aluminum (27/SE27)–which provides both the metal contact plug (as per the annotated figure above) and the front metal layer. Such a POSITA would not be discouraged from using the teachings of Uno ('864) by the presence of this structure, particularly if that POSITA only had available the more typical metallurgy that is used when aluminum provides the material that is used for the interconnect wiring–which is the two-step use of a tungsten plug to provide the metal contact plug, topped by an aluminum interconnect wiring layer for the front metal layer. A POSITA would be motivated to substitute in the more-typical tungsten-contact-plug/aluminum-front-metal-layer approach due to its availability, and would also have a reasonable expectation of success due to the

long-running and well-known use of a tungsten contact plug and an aluminum front metal layer.

538. While those considerations (commonly availability of the W/Al system as compared with Uno (’864)’s all-aluminum system), there are further reasons to improve upon Uno’s (’864) all-aluminum system and toward the commonly-available W/Al system–which was described in Section VII.B, where an exemplary cross-sectional microphotograph of such a system was included).

539. In the early days of MOS transistors, aluminum was used as both the contact material for contact to the terminals of a transistor (source, gate, drain, and body) and as the interconnect wiring material (such as the “front metal layer” of the ’634 Patent and the upper part of 27/SE27 in Uno (’864)). (*See* illustrative image below.)

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540. However, particularly as transistor channel resistances decreased with the scaling-down of transistor dimensions, problems with the electrical behavior of aluminum contacts to silicon became difficult; e.g., (*See* illustrative image below.)

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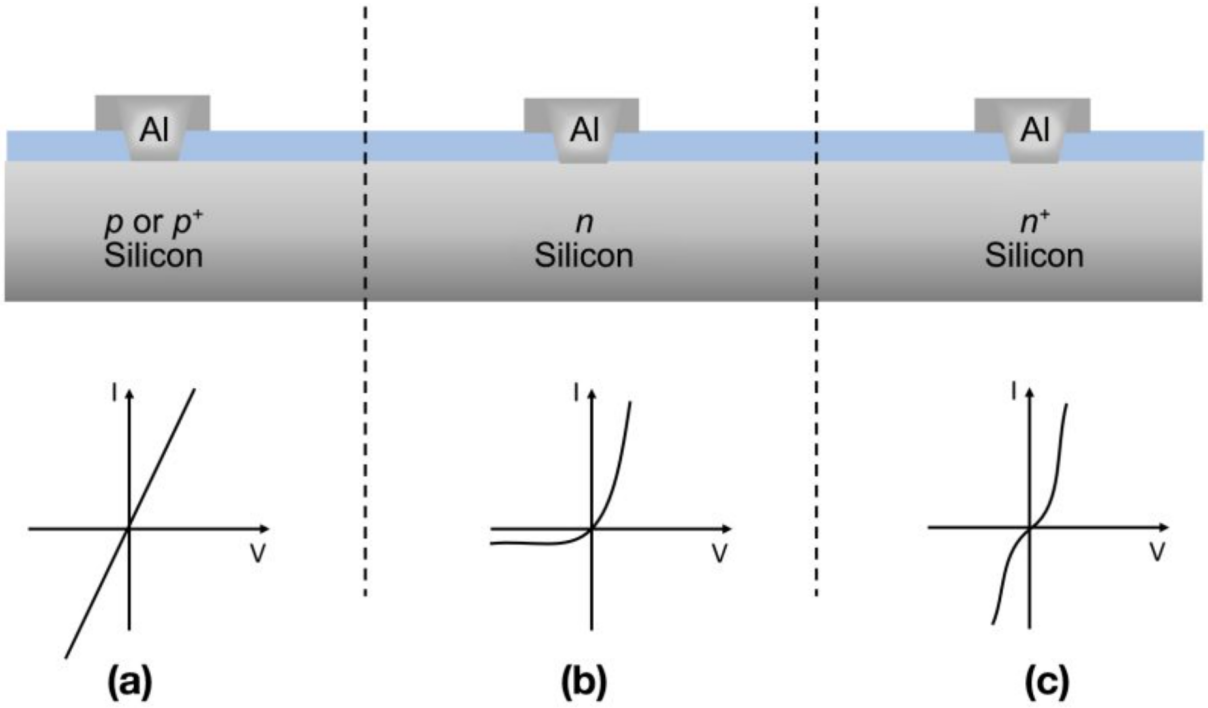


Figure 3. Aluminum contacts to silicon (a) ohmic contact; (b) rectifying (Schottky) contact; (c) tunneling contact.

The resulting non-ohmic contacts (non-ohmic for n+ silicon, and potentially a Schottky contact for n-silicon) became unacceptable.

541. In addition, aluminum contacts would sometimes "spike" downward into the silicon below–perhaps even breaching the depth of the p-n junction of the diffused diode, ruining the diode itself (permanently). (*See* illustrative image below.)

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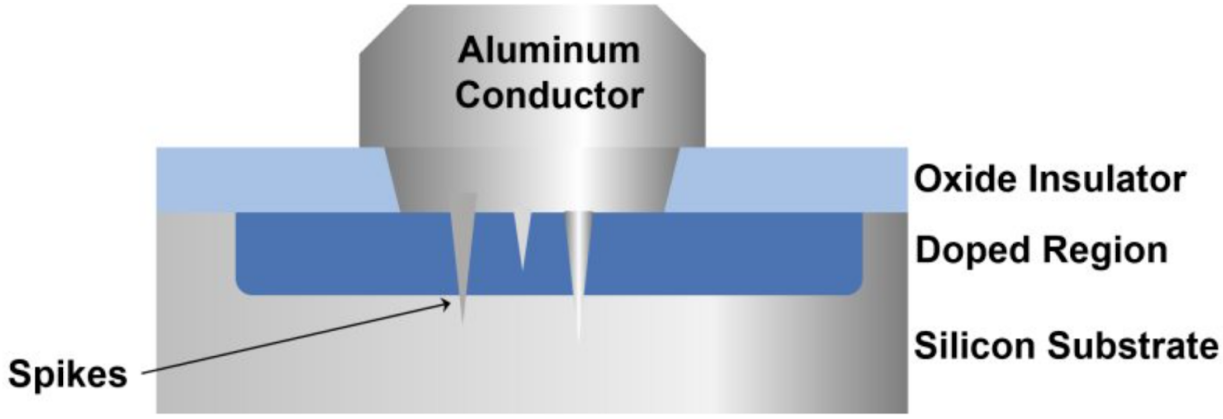
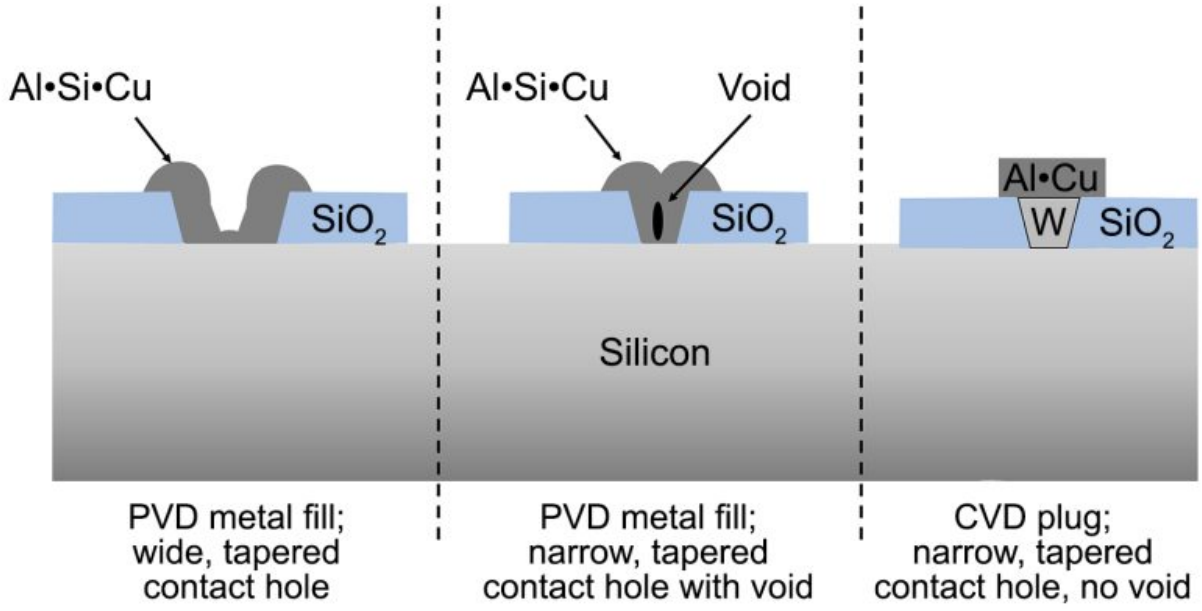
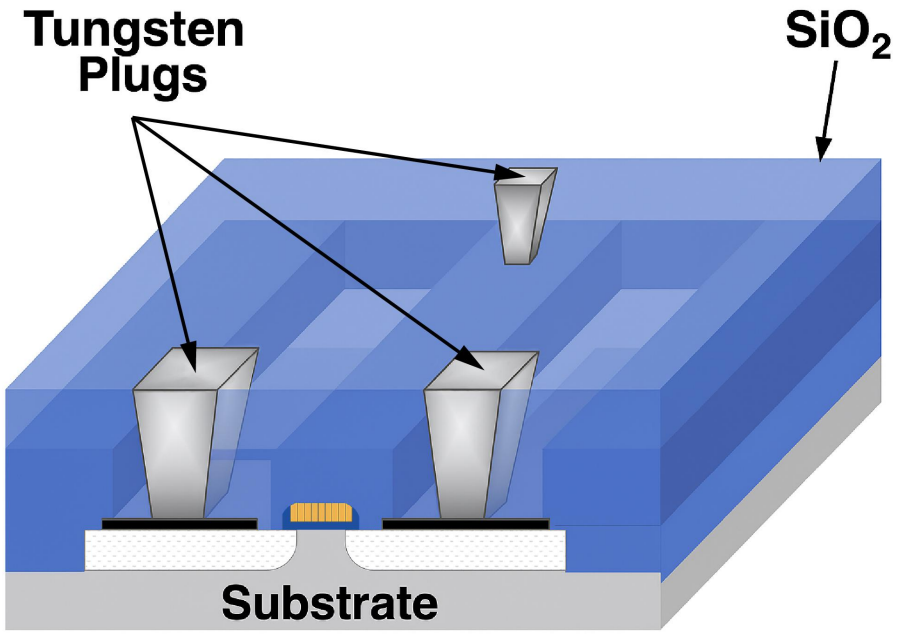


Figure 4. Pitting or spiking of aluminum through the p/n junction.

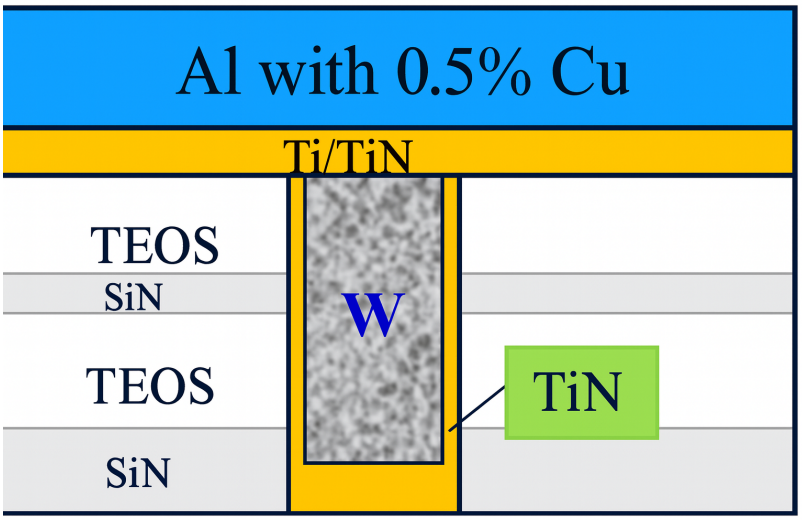
542. Yet another problem is that, when aluminum was deposited into a contact plug hole (particularly when scaling caused the aspect ratio of the plug hole to become large–that is, the depth of the plug hole became increasingly-larger than the width of the plug hole), it became difficult to form good aluminum contact plugs–as voids would form during the deposition of aluminum. (*See* illustrative image below.)



As the right-hand image above indicates, tungsten replaced aluminum as the contact plug material–while aluminum (or an alloy of aluminum, containing a small amount of copper) remained in use for the interconnect wiring layer (such as the aforementioned "front metal layer").



543. Thus, by the 1990s (*see* Ex. 1008, Stanley Wolf, *Silicon Processing for the VLSI Era*, Vol. 2, 281 (1990)), the use of the system of a tungsten plug and aluminum interconnect wiring was the most-commonly used system in the integrated circuit industry–and would have been both widely available and more common that the older all-aluminum system.



Note that Ti/TiN and TiN are used as barrier metal layers as well in this system.

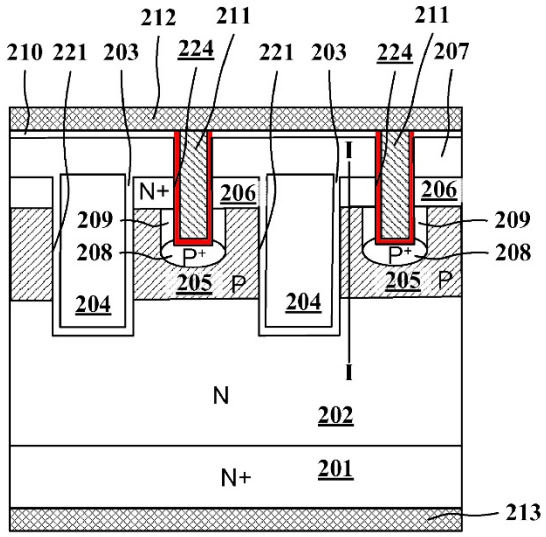
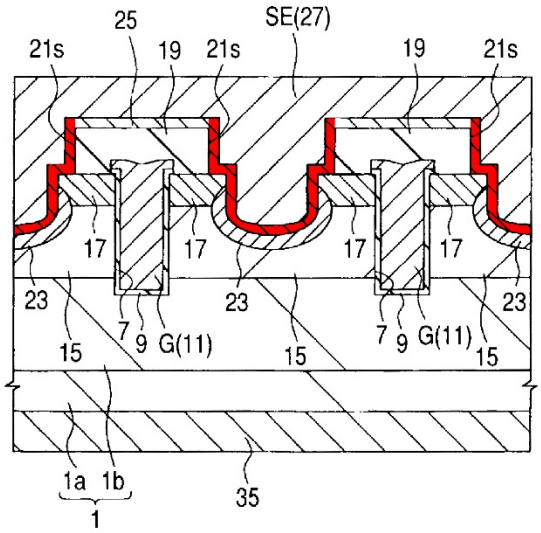
544. Further, this understanding is supported by the Patent Owner's admitted prior art, as illustrated in Fig. 1 (Prior Art) of the '634 Patent, which depicts the use of a barrier metal layer and contact plugs. As discussed above, these structures are consistent with the widely used material combination of Ti/TiN for the barrier metal layer and tungsten for the contact metal plugs. A POSITA would have been motivated to use these materials to form the structures shown in the admitted prior art, as they were standard in the field and known to provide reliable electrical performance, diffusion resistance, and process compatibility.

545. Therefore, a POSITA would have been further motivated–not only by the higher (and perhaps only) availability of the tungsten-aluminum system, but also to move in that direction due to the known shortcomings of the all-aluminum system.

546. Limitation *[4a]* is explicitly disclosed by Uno ('864)–for the reasons cited above. As stated in Uno's disclosure, with respect to the barrier metal layer, "In addition to Ti, TiN (titanium nitride) may also be used." (Ex. 1006, Uno ('864), 13:9–10.)

[4a]

barrier metal layer is Ti/TiN

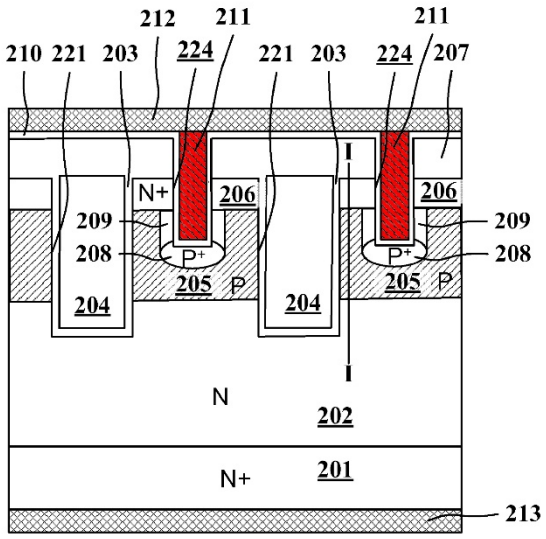
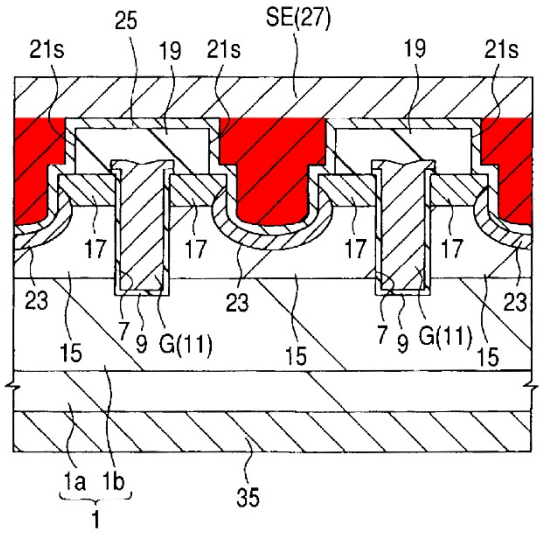
Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

b. [4b]: "contact metal plug is [t]ungsten."

547. Limitation ***[4b]*** is disclosed by Uno ('864) and the knowledge of a POSITA–for the reasons cited above.

[4b]

contact metal plug is Tungsten

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

6. Claim 5: "The trenched MOSFET of claim 4, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

548. Claim 5 is a dependent claim–and depends from Claim 4, which depends from Claim 3, which depends from Claim 2, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2, Section XI.B.3, Section XI.B.4, and Section XI.B.5) that Claim 1, Claim 2, Claim 3, and Claim 4 of the '634 Patent are either taught by Uno ('864) or rendered obvious by Uno ('864) in view of the knowledge of a POSITA.

549. Uno discloses that, following the formation of a silicon oxide film, element ’864-19 is etched in a patterned manner to form various shapes of “contact trenches (source contact) 21s.” Uno explicitly considers the shape of the contact trench to improve coverage. As shown in FIGs. 36–38 of Uno, the contact trench may have either a vertical profile or a tapered profile. (*See* Ex. 1006, 5:35-36; *see also* 15:2-5, 15:18-20, 15:29-30, 15:35-36; Figs. 9, 11, 12, 15, 16, 18, 20, 24, 36–38, element 21s.)

Ex. 1006 ('864 Uno)

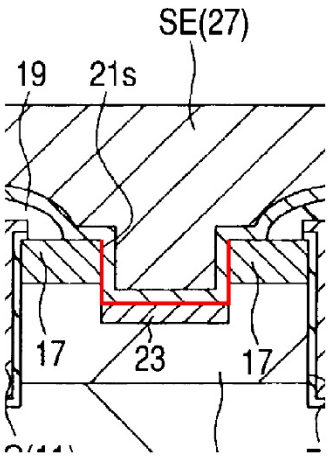


Fig. 36 (Annotated partial enlarged view)

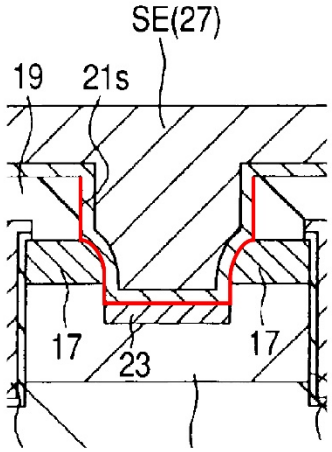


Fig. 37 (Annotated partial enlarged view)

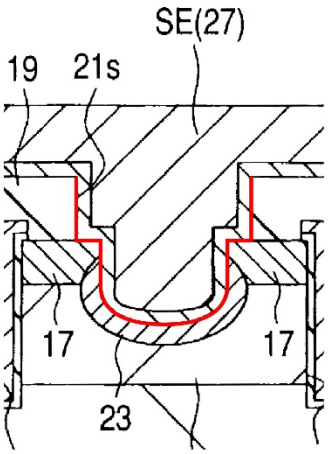


Fig. 38 (Annotated partial enlarged view)

550. The remainder of Claim 5 is also rendered obvious by Uno (’864) in view of the knowledge of a POSITA–as both vertical-shaped trenches and tapered-shaped trenches were both well-known in the art by the time of the ’634 Patent (2008). See the following illustrative examples of vertical and tapered shaped trenches.

Ex. 1010, U.S. Patent No. 5,395,786, Fig. 13

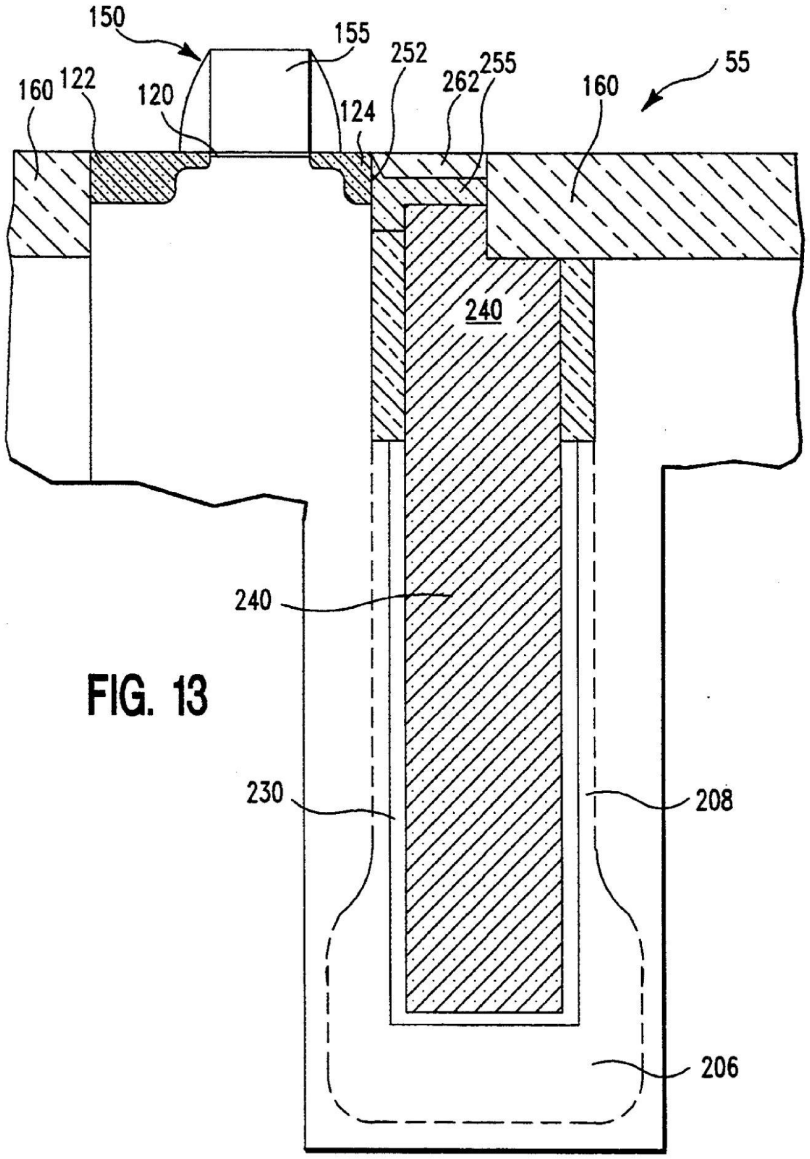


FIG. 13

Ex. 1011, H. Shichijo et al., *Trench Transistor DRAM Cell, IEEE Electron Device Letters*, vol. 7, 119 Fig. 1 (1986).

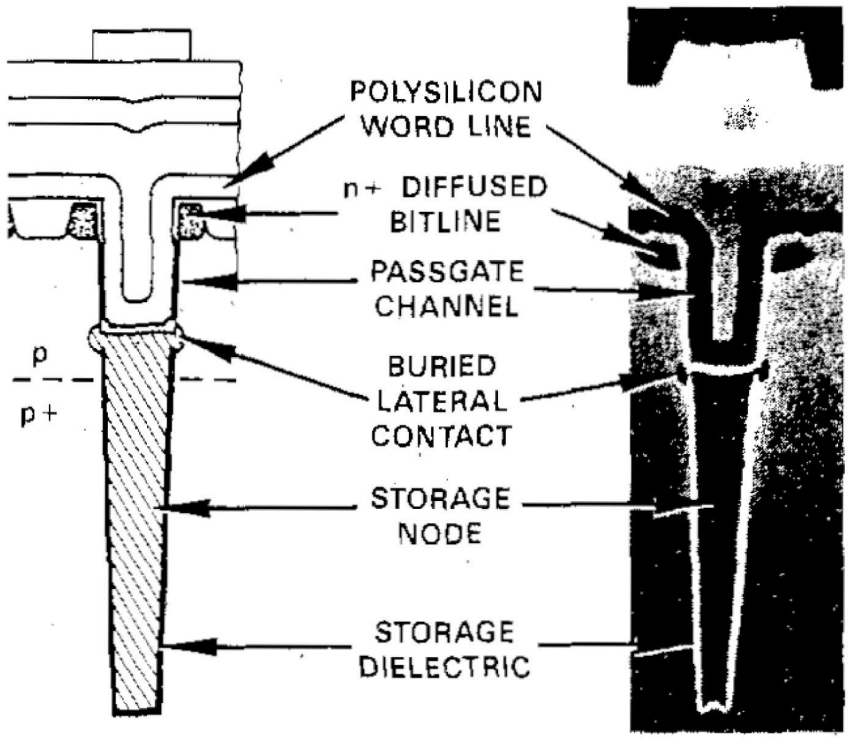


Fig. 1. TTC schematic diagram and SEM cross section.

7. Claim 6: "The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom."

551. Claim 6 is a dependent claim, and depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2) that Claim 1 of the '634 Patent is rendered obvious by Uno ('864) in view of the knowledge of a POSITA.

552. The remainder of Claim 6 is also rendered obvious by Uno ('864) and the knowledge of a POSITA–and as will be detailed via the claim sub-elements below, Claim 6 in toto is identical in structure to Claim 2, except that it reverses the polarities (i.e., n and p) of the components as described in Claim 2. As noted above in the discussion of Claim 2, that claim is basically identifying a MOSFET structure that is an n-type (i.e. nMOS) MOSFET transistor; Claim 6 simply changes the dopant polarity to describe what is a p-type (i.e., pMOS) MOSFET transistor.

553. To simplify the analysis, this claim will be split into claim elements.

a. ***[6a]: "wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof,"***

554. Claim 6 is identical to Claim 2–except that it reverses the polarities (n-to-p and vice-versa) of the determining dopant in each layer; this amounts to being a way of saying that while the teachings of Claim 2 describe what is well-known in the art as being an nMOS transistor, the teachings of Claim 6 describe what is well-known in the art as being a pMOS transistor.

555. Uno ('864) discloses this claim sub-element.

556. Uno ('864) describes (among other things) the fabrication of an n-channel trench-gated MOSFET–but also notes that it would be a simple matter to

reverse the polarity of the dopant atoms and create a p-channel trench-gated MOSFET using the same process techniques as described (by Uno ('864)) for the fabrication of an n-channel trench-gated MOSFET:

> While description has been made to an example of the n-channel type power MISFET, the leak *[sic]* current can be decreased also in a p-channel type power MISFET by properly selecting the material for the barrier film. FIG. 24 shows a cross sectional view for a main portion of a p-channel type power MISFET. In this case, while the conduction type of the impurity for each of the portions constituting the p-channel type power MISFET is different, it can be formed by the identical process for the n-channel type power MISFET. (Ex. 1006, Uno ('864), 9:20-29.)

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Ex. 1006 ('864 Uno)

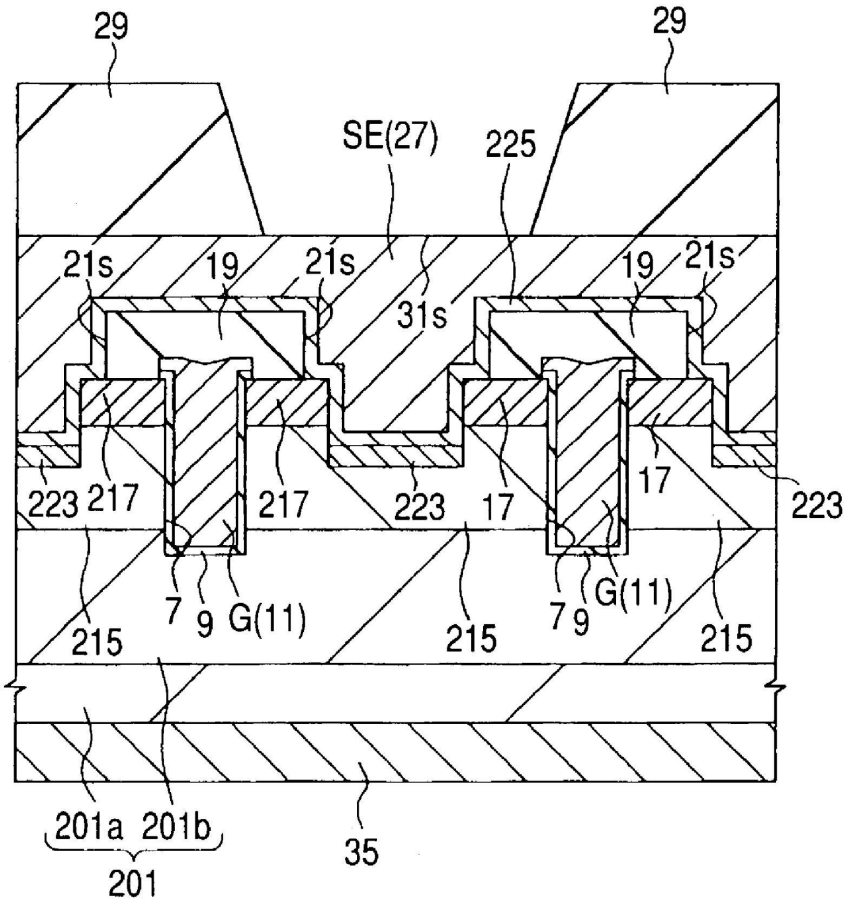


Fig. 24

Notably, this p-channel architecture is structurally-identical to the n-channel architecture depicted in Fig. 11:

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Ex. 1006 ('864 Uno)

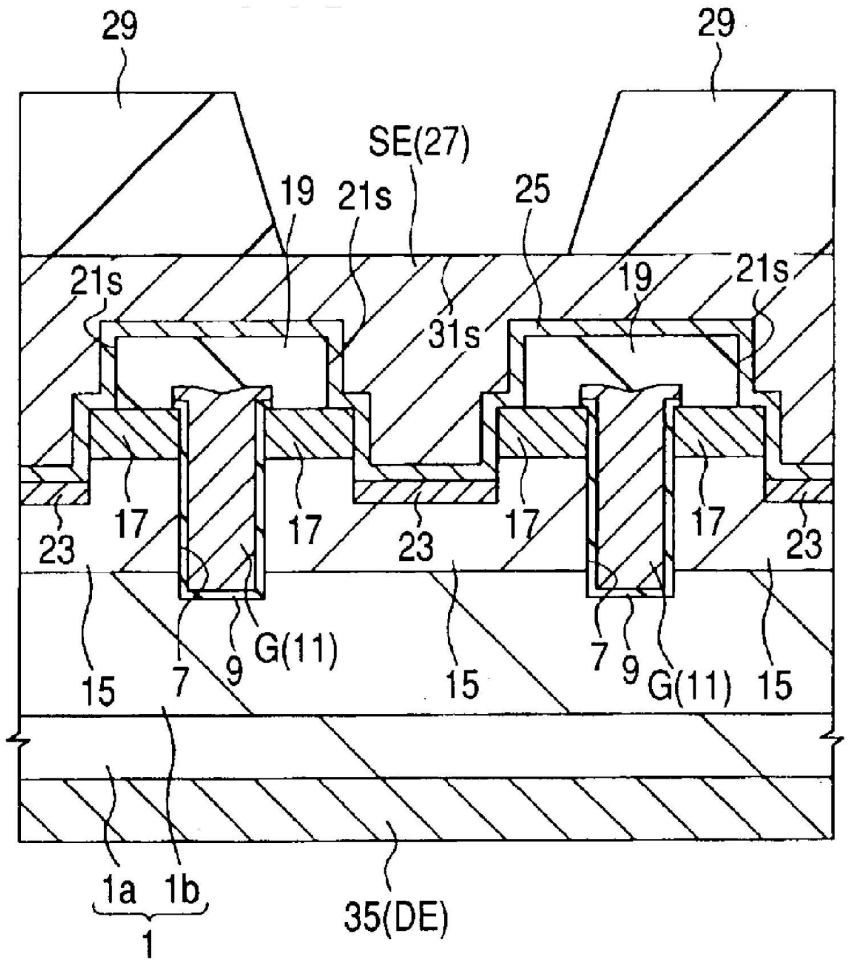


Fig. 11

557. By using the identical structure but making the "chemical" change of swapping the polarities of the dopant used in each region, a p-channel version of the n-channel transistor is easily created.

b. [6b]: "and the lateral contact layer has less doping concentration than the base contact layer at bottom."

558. Claim element *[6b]* is identical to claim element *[2b]*–which was already discussed earlier (in Section XI.B.3.b). For the reasons described there, this claim element is rendered obvious by Uno ('864) in view of the knowledge of a POSITA.

8. Claim 7: "The trenched MOSFET of claim 6, wherein further comprises a barrier metal layer and a plurality of contact metal plugs."

559. Claim 7 is a dependent claim–and depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2 and Section XI.B.7) that Claim 1 and Claim 6 of the '634 Patent are either taught by Uno ('864) or rendered obvious by Uno ('864) and the knowledge of a POSITA.

560. The remainder of Claim 7 is also taught by Uno ('864). Claim 7 is identical to Claim 3, which was already discussed earlier (in Section XI.B.4); for the same reasons as those discussed there, Uno ('864) teaches Claim 7 of the '634 Patent.

9. Claim 8: "The trenched MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is [t]ungsten."

561. Claim 8 is a dependent claim–and depends from Claim 7, which depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2, Section XI.B.7, and Section XI.B.8) that Claim 1, Claim 6, and Claim 7 of the '634 Patent are either taught by Uno ('864) or rendered obvious by Uno ('864) and the knowledge of a POSITA.

562. The remainder of Claim 8 is also rendered obvious by Uno ('864) and the knowledge of a POSITA. Claim 8 is identical to Claim 4, which was already discussed earlier (in Section XI.B.5); for the same reasons as those discussed there, Uno ('864) and the knowledge of a POSITA render obvious Claim 8 of the '634 Patent.

10. Claim 9: "The trenched MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape."

563. Claim 9 is a dependent claim–and depends from Claim 8, which depends from Claim 7, which depends from Claim 6, which depends from Claim 1; thus, to the extent necessary to meet the dependence requirement, it has already been shown above (in Section XI.B.2, Section XI.B.7, Section XI.B.8, and Section XI.B.9) that Claim 1, Claim 6, Claim 7, and Claim 8 of the '634 Patent are either

taught by Uno (’864) or rendered obvious by Uno (’864) and the knowledge of a POSITA.

564. The remainder of Claim 9 is also taught by Uno (’864). Claim 9 is identical to Claim 5, which was already discussed earlier (in Section XI.B.6); for the same reasons as those discussed there, Claim 9 of the ’634 Patent is rendered obvious by Uno (’864) and the knowledge of a POSITA.

C. Ground 3–Claims 1-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being Obvious Over Hshieh (’384) In View of Uno (’864) (and *vice versa*).

565. To the extent the Board may not fully agree with the obviousness analysis presented above with respect to the express teachings or application of the knowledge of a POSITA, it can also be shown—as set forth below—that Claims 1–9 of the ’634 Patent are rendered obvious by Hshieh (’384) in view of Uno (’864), or alternatively by Uno (’864) in view of Hshieh (’384).

566. As detailed above in Section XI.A and Section XI.B, the claim elements and claim sub-elements of the ’634 Patent are rendered obvious independently by either Hshieh (’384) or Uno (‘864)–as both simply just teach these claim elements and claim sub-elements. For Ground 3, I incorporate my analysis from Ground 1 by reference and further supplement it with the teachings of Uno (’864) from Ground 2, which provides additional disclosures overlapping with the obviousness of the claim limitations disclosed by Hshieh (’384) alone.

Together, Hshieh ('384) and Uno ('864) would have rendered the Challenged Claims obvious to a person of ordinary skill in the art (POSITA) at the time of the alleged invention.

567. As noted throughout Section XI.A, the claim elements and sub-elements are shown to be rendered obvious by Hshieh ('384), with appropriate referential support provided in each instance. To the extent that the PTAB looks for additional support, it would have been obvious to a POSITA to combine the teachings of Hshieh ('384) and Uno ('864)–and to thus independently arrive at the corresponding features of the '634 Patent. As such, the only claim sub-element further addressed in this Ground 3 analysis is limitation *[1d]* – which is the only sub-element not explicitly shown in the figures, but is nonetheless fully supported by the disclosure of Hshieh ('384).

1. A POSITA Would Have Had a Motivation to Combine and a Reasonable Expectation of Success

568. It is my conclusion and opinion that, based on my education, training, and experience, a person of ordinary skill in the art ("POSITA") would have been motivated, as of the Filing Date of the Challenged Patent, to combine the teachings of Hshieh (U.S. Patent No. 2006/0273384) and Uno (U.S. Patent No. 6,984,864) with his/her general knowledge and routine engineering practices. This motivation would have stemmed from the POSITA's familiarity with established

semiconductor device structures—particularly trench-gated vertical-conduction-path MOSFETs—and the routine engineering objective of improving device performance, reliability, and manufacturability through known design optimizations.

569. The teachings of Hshieh and Uno are complementary, and their combination would have involved the predictable application of known elements to achieve well-understood functions. A POSITA would have recognized that the features disclosed in Uno could be readily implemented in the context of Hshieh's architecture (or vice versa) without undue experimentation or inventive effort. The combination would have reflected the application of known principles to known problems, consistent with the design motivations and problem-solving approaches typical of a POSITA at the time.

570. Moreover, both Hshieh and Uno rely on conventional and well-understood techniques in silicon device fabrication, further reinforcing that a POSITA would have had a reasonable expectation of success in implementing the combination. The combination would have been viewed as yielding practical benefits—such as improved electrical characteristics or manufacturing efficiency—without departing from accepted design methodologies. These benefits would have provided additional motivation for a POSITA to pursue the combination in the ordinary course of semiconductor device development.

571. Importantly, my analysis is conducted from the perspective of a POSITA at the time of the alleged invention and is not based on any knowledge of the Challenged Patent or its claims. My conclusions are based solely on the teachings of the prior art and the state of the art as it existed at the relevant time, without reliance on hindsight. Accordingly, it is my conclusion and opinion that a POSITA would have been motivated to combine the teachings of Hshieh ('384) and Uno ('864), and would have had a reasonable expectation of success in doing so, thereby rendering the relevant claim elements obvious.

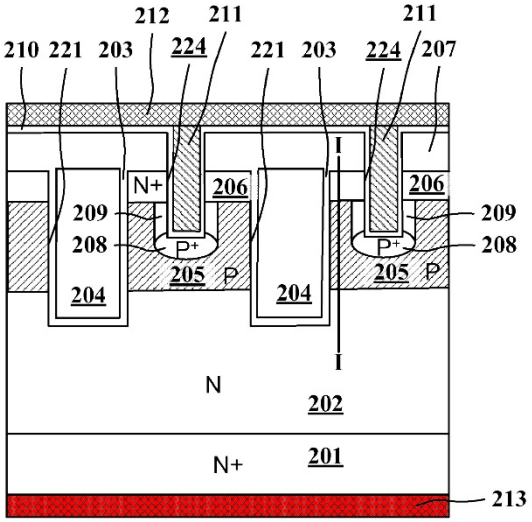
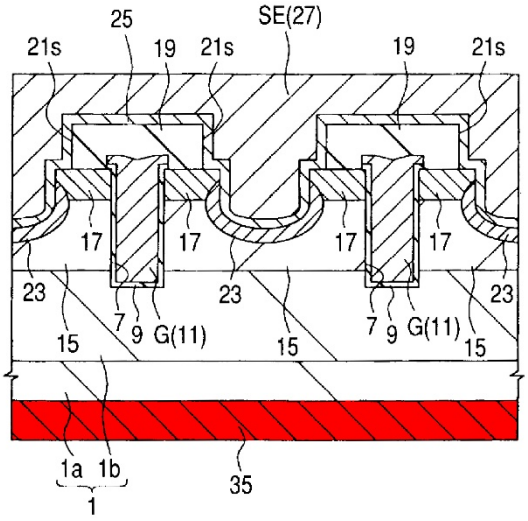
2. *[1d]*: "a bottom metal layer formed on the lower surface of said semiconductor region;"

572. This claim element (as limitation *[1d]*) is rendered obvious by Hshieh ('384) in combination with Uno ('864).

573. As discussed in Section XI.A.2.e, it would have been apparent to a person of ordinary skill in the art (POSITA) that Hshieh ('384)'s structure requires a drain contact to establish electrical connection with the drain region–since otherwise, there is no drain terminal included in the transistor.

574. Although Hshieh ('384) does not explicitly illustrate a drain contact, Uno ('864) explicitly depicts such a bottom metal layer as providing the drain electrode contact for his trenched-gate MOSFET structure:

[1d]
bottom metal layer

Ex. 1001 ('634 Hsieh)	Ex. 1006 ('864 Uno)
	
Fig. 2G (Annotated)	*Fig. 38 (Annotated)*

575. Uno ('864) specifically identifies layer 35 as "a conductive film 35 forming a drain electrode." (Ex. 1006, Uno ('864), 6:20). Uno ('864) further explains that "[t]he stacked film 35 forms a lead electrode (drain electrode DE) for the drain (1a, 1b)." (Ex. 1006, Uno ('864), 7:25-26). A person of ordinary skill in the art ("POSITA") would have been motivated to combine the teachings of Hshieh ('384) and Uno ('864) to implement a bottom metal layer functioning as a drain contact. (Note once again that "lead" above is not the metal lead (i.e., Pb) but rather is pronounced like "leed" and refers to the wiring contact to the drain electrode–using common industry parlance.) This modification would provide a

conventional and reliable means of forming an electrical connection to the drain region—as the simplest and most-straightforward way of adding a drain contact to a trenched-gate MOSFET. Accordingly, this element would have been obvious to a POSITA in view of the combined teachings of Hshieh ('384) and Uno ('864).

XII. SECONDARY CONSIDERATIONS

576. Based on my review of the '634 Patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims–nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '634 Patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the Challenged Claims are rendered obvious by those references in combination with what was clearly known in and obvious in the prior art. If I later become aware of arguments of any secondary consideration, I may assess those arguments when they arise, in order to reach conclusions and form opinions regarding their correctness; I reserve the right to file supplemental declarations should such circumstances occur.

XIII. CONCLUSION

577. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. §

1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

578. I declare under penalty of perjury that the foregoing is true and correct. Executed this 15th day of August, 2025 in Fletcher, Vermont.



Daniel Foty, Ph.D.