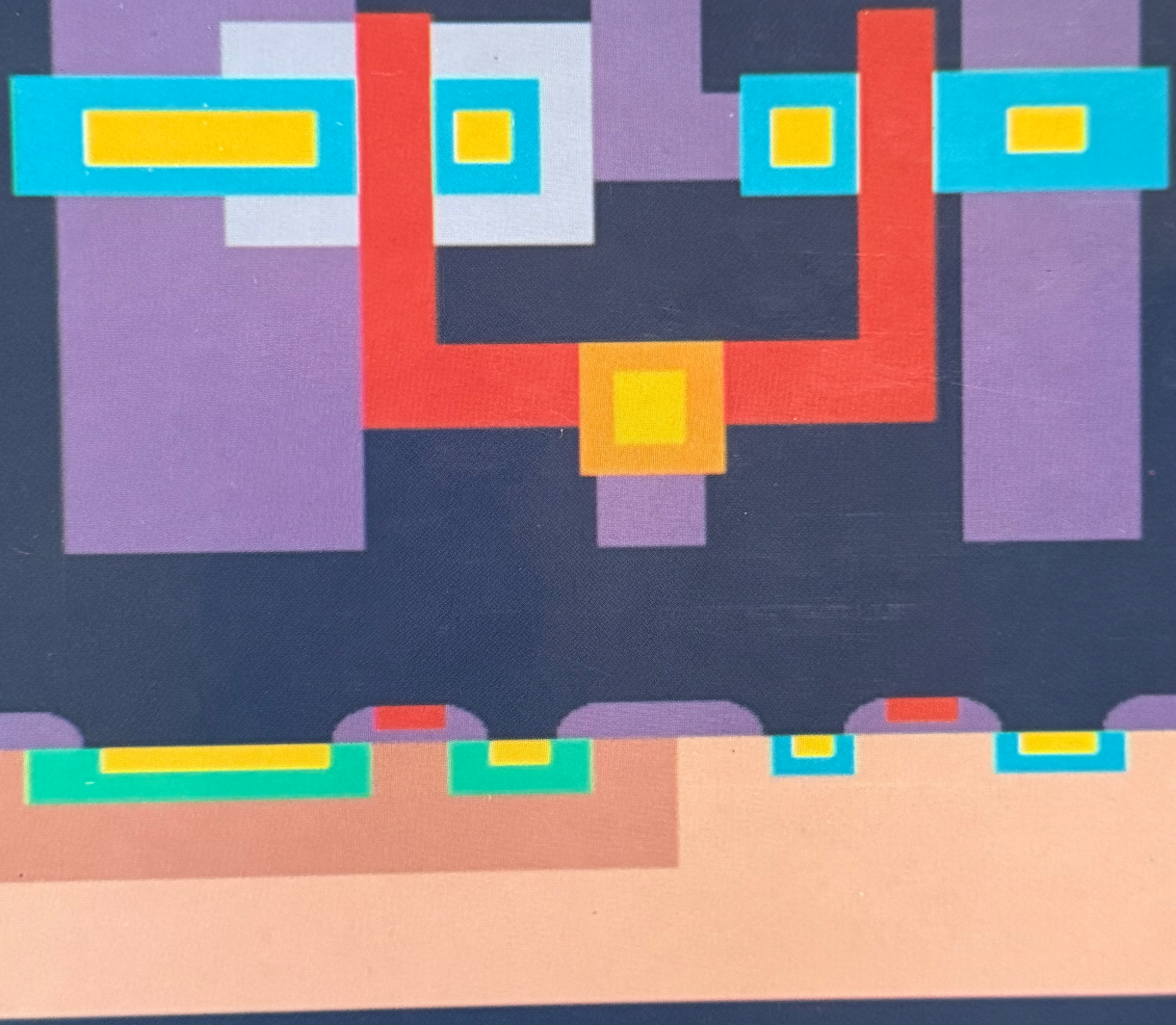
Silicon Processing

for the VLSI Era

Volume 2 - Process Integration



S. Wolf

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SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

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structures in NMOS technologies. (More information on the properties, formation, and patterning of polysilicon and polycides can be found in Vol. 1, chaps. 6 and 11, respectively.)

Various conductors have been proposed as local interconnect materials in CMOS technologies, including: dual-doped polysilicon, $TiSi_2$, Ti:W, TiN, and CVD W. Information on the characteristics of CMOS local interconnect materials is presented in chapter 3, section 3.11.2, as well as elsewhere in this volume.

4.3.1.3 Aluminum Metallization. Patterned aluminum thin films have been the most widely used interconnect structures in the manufacture of silicon ICs. As described in detail in chapter 3 of this volume and in Volume 1, chapter 10, the main reasons for the pervasiveness of Al are its low resistivity (2.7 $\mu\Omega$-cm) and its good adhesion to SiO_2 and Si. In addition, Al is generally used as the top level of metal in multilevel-metal systems because wire-bonding technology to Al thin films is a well-characterized process.

The main limitations of Al are its low melting temperature (660°C) and its low eutectic temperature with Si (577°C). In addition, Al thin films begin to form hillocks at relatively low processing temperatures (i.e., above 300°C), and they offer relatively poor resistance to electromigration effects and corrosion. (The electromigration and hillock problems are described in more detail in section 4.7.) The problems that arise when Al contacts are made to Si (i.e., related to the eutectic temperature of Al and Si) are considered in chapter 3, section 3.4.3.

Attempts to alleviate the above problems have generally involved the addition of alloy materials to Al or the formation of multilayer-Al conductor structures. The addition of Si to Al was discussed in chapter 3, section 3.4.3 as a technique for preventing junction spiking in Al contacts to Si. Electromigration and hillock resistance have been improved through the addition of such elements as Cu, Ti, Pd and Si to Al to form alloys. Another approach to overcoming the latter problems has involved the fabrication of multilayer-metal structures consisting of Al and other metal layers, such as the following: (1) Ti, Cr, and Ta layers sandwiched between Al layers; (2) Ti:W layers deposited below or on top of the Al film; and (3) W selectively deposited over the top and sidewalls of patterned Al lines. Such multilayer structures are also described in section 4.7. The addition of other metals to form Al alloys, however, generally degrades one or more of the Al characteristics (e.g., resistivity, corrosion resistance, etchability, or bondability).

Thin films of Al for VLSI interconnects are commonly deposited by dc magnetron sputtering (see Vol. 1, chap. 10). Although evaporation of Al films was carried out in the early days of IC fabrication, the need for Al-alloy films with tightly controlled alloy composition was the primary reason for the displacement of evaporation by sputtering. Sputtering generally allows more control over the alloy composition than evaporation (see Vol. 1, chap. 10). Some recent advances in sputter deposition are reviewed in reference 8. Research is also being conducted on CVD Al, as described in section 4.5.5.2.

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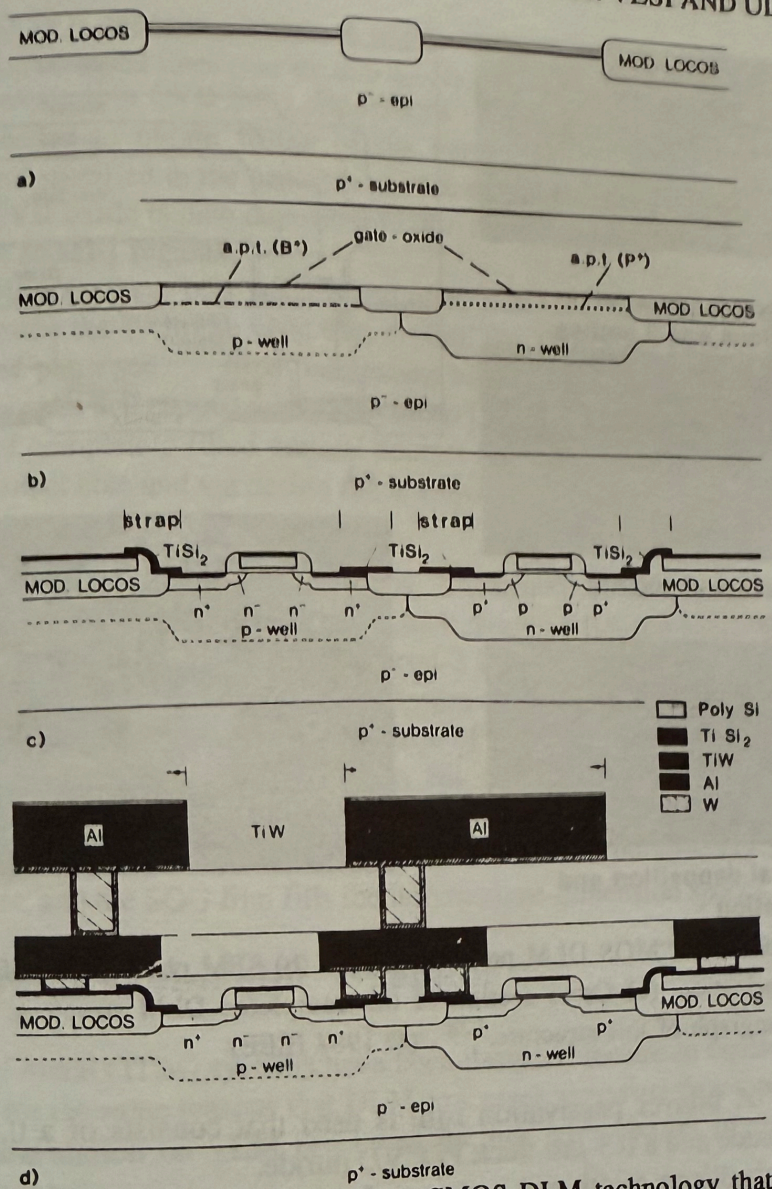


Fig. 4-59 Schematic cross section of submicron-CMOS DLM technology that uses: a fully planarized isolation structure; $TiSi_2$ over poly as a local interconnect; selective W as a contact hole plug; and Al:Cu for Metal 1 and Metal 2.[207] (© 1987 IEEE).

In this process, the substrate is completely planarized at the conclusion of the isolation formation procedure (Fig. 4-59). The PMD layer is likewise completely planarized, by means of a conformally deposited LPCVD TEOS process and a resist-etchback technique. Following the PMD resist etchback, a thin layer of BPSG is deposited for gettering and dielectric-layer integrity. An etchback SOG sandwich dielectric approach is used to planarize the intermetal dielectric. The vias are etched to give sidewalls with slopes of 80°, which allows adequate filling by the sputter-deposited Al:Cu Metal-2 film. The Ti:W etchstop layer under Metal 2 allows a 70% overetch step to be used with only 0.1-μm CD line loss in

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The source-to-well junction is essentially a one-sided *pn* junction with a built-in voltage of V_{bi} = 0. 82 V. From Fig. 5-20, we estimate that the depletion-region width extends into the *n*-well ~0.35 μm, since there is no applied voltage across the junction (i.e., both the source and the well are connected to V_{DD}). The *np*-junction to the substrate has a built-in voltage of 0.63 V, and the total depletion width of this junction at a 5 V bias is ~1.9 μm. We calculate that about 0.19 μm of this depletion region is in the *n*-well. The *n*-well must therefore be deep enough to accommodate the depth of the source junction (0.4 μm) as well as the sum of the depletion region widths in the well in order for vertical punchthrough to be avoided. While the total of these dimensions is 0.94 μm, it is good engineering practice to increase the depth of the well by about 50% to account for process variations. A reasonable well depth might therefore be 1.5 μm.

6.2.4 CMOS on Epitaxial Substrates

As will be described in the section dealing with latchup prevention (section 6.4.8.2), heavily doped substrates with a more lightly doped surface epitaxial layer have been utilized to suppress latchup in CMOS.[11] When such starting material is used with single-well CMOS, the epitaxial layer is doped to a concentration equal to that of the substrate in a nonepitaxial wafer used for that process. If a twin-well CMOS process is used, the epitaxial layer is doped to a level significantly lower than that required for building either the *p*- or *n*-channel MOSFETs (see section 6.2.5).

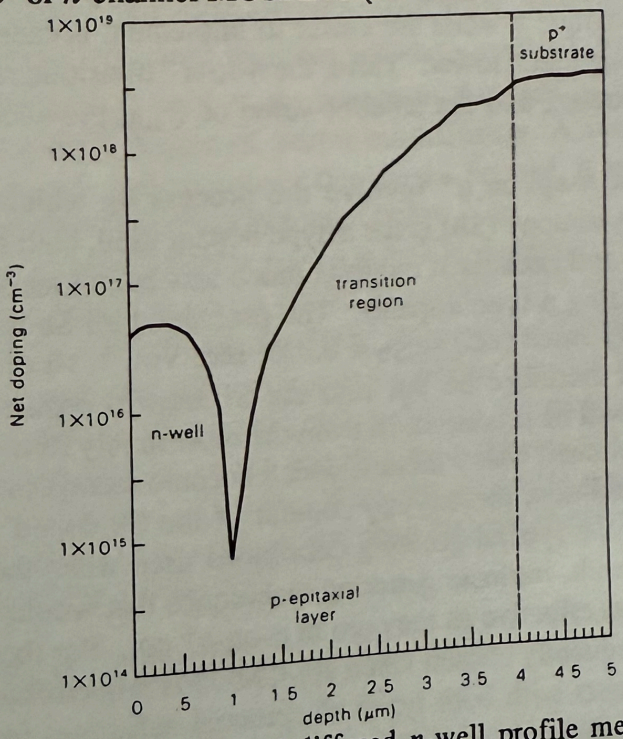


Fig. 6-9 A *p*-on-*p*-epi doping profile and diffused *n*-well profile measured after the entire CMOS process has been completed. The as grown epi thickness is 4 μm and the final lightly doped epi thickness is about 2 μm.[116] (© 1987 IEEE).

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The epitaxial layer is made thicker than the well depth, since the dopants in the heavily doped substrate under the epi layer diffuse toward the surface as the well dopants are diffused toward the bulk (Fig. 6-9). Thus, some of the epitaxial layer becomes more heavily doped during the CMOS process flow. The process is designed so that the bottom of the well is eventually adjacent to the heavily doped substrate region.

Either *n*-epi on n^+ substrates or *p*-epi on p^+ substrates can be used, with each method having advantages and drawbacks. Because the problems with *n*-epi on n^+ are more serious, *p*-epi on p^+ is more widely used. The major limitation of the latter approach is that the outdiffusion of boron from the p^+ is much more severe than it is in *n*-epi on n^+. (The reason for this is that boron diffuses much more rapidly than antimony, which is the most widely-used n^+ dopant material.) Thus, a thicker p^-- epitaxial layer must be used.

In addition, the transition region between the p^+ substrate and the p^-- epi layer is thicker, producing a larger series resistance (R_{sub}), which in turn reduces latchup immunity. On the other hand, the *p*-on-p^+ material is less sensitive to process-induced defects, and the *p*-type substrate provides higher conductivity under NMOS devices. Such additional conductivity is desirable, since it reduces the voltage drops caused by the substrate currents (generated as a result of the hot-carrier effects in short-channel devices). It is especially important in the regions containing NMOS devices, since the hot-electron substrate current is much higher in such devices than in PMOS devices.

The *n*-on-n^+ epitaxial substrates also offer some advantages. First, SRAMs are often built on *n*-type substrates, because the *p*-well to *n*-substrate junction provides protection from radiation-induced discharging of the memory's *n*-type storage nodes in the *p*-well.[12] Second, retrograde *p*-wells are easier to implement because their implantation energy requirements are much lower. Third, the *n*-to-n^+ transition region is smaller than that in *p*-on-p^+ substrates, and the smaller value of R_{sub} provides improved latchup protection.

The limitations of *n*-epi on n^+ involve the process by which the heavily doped substrate is grown. Antimony (Sb) is the *n*-type dopant used, both because its diffusion coefficient is so low and because it exhibits much less lateral autodoping than arsenic (the other slow-diffusing *n*-type dopant). The problem with Sb is that its segregation coefficient, k_o, is very small (i.e., $k_{o,Sb} = 0.023$; see, Vol. 1, chap. 1), and thus a large quantity of Sb must therefore be put into the Si melt to ensure that a sufficiently heavily doped ingot will be produced. In even the most highly refined Sb there are high concentrations of unwanted heavy metals, which become incorporated into the growing silicon crystal. In addition, the oxygen content of the Sb-doped crystal is relatively small, due in part to the special growing conditions used when the Sb-doped ingot is pulled.[7,9,10] As a result, intrinsic gettering techniques that would getter the metals in the substrate are not as effective as they are in *p*-on-p^+ epi. For these reasons, *n*-on-n^+ substrates are less frequently chosen when epi-CMOS is implemented.[12]

A problem that exists with both types of epitaxial substrates for CMOS is that the wells cannot be made too deep, since the lateral diffusion would then take up too much area. On the other hand, if the wells are too shallow, vertical punchthrough will ensue.[13] A second problem is that of leakage current. Appreciable leakage current can

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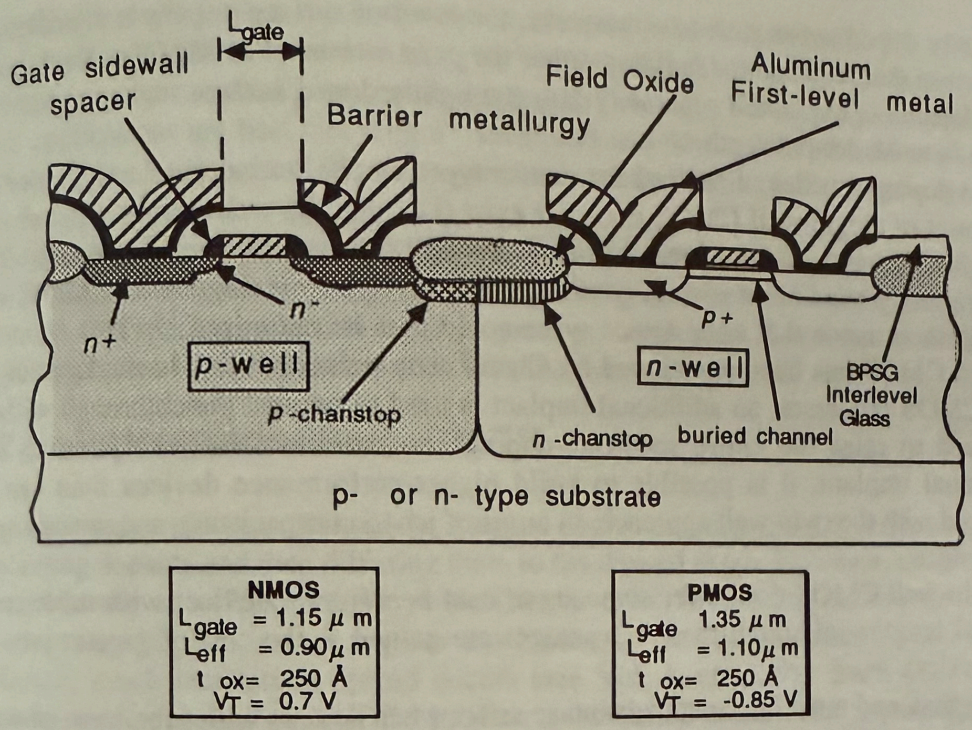


Fig. 6-10 Cross section of a twin-well 1.2-μm CMOS structure.[12] Reprinted with permission of Semiconductor International.

flow in the vertical path in two different situations. First, punchthrough can occur if the depletion regions of the p^+/n-well junction and the n-well/p^+-substrate junction touch each other. The problem is even more severe in the case of the heavily doped p^+ substrate, due to the high degree of boron outdiffusion. A major limitation is thus imposed on the minimum epitaxial-layer thickness. Second, it may be possible for the source regions to become biased to a potential below V_{SS}.

Another problem of epi-CMOS is back surface autodoping. For example p-type 20 Ω-cm (7×10^{14} boron/cm^3) epi on a 0.005 Ω-cm (2×10^{19} boron/cm^3) substrate is representative of epi for CMOS devices. If the substrate back is not sealed (e.g., using a sealing layer such as undoped silicon dioxide or silicon nitride), boron evaporation can contribute to autodoping on the front surface during the entire epi deposition cycle. This widens the epi/substrate interface and may even prevent the epi from reaching the 20 Ω-cm specified resistivity. Note that if silicon nitride is used as a sealing layer it should only be used in thin layers (e.g., less than 100 nm thick) since its high intrinsic stress causes it to bow the silicon.[113]

6.2.5 Twin-Well CMOS

With the twin-tub approach, two separate wells are formed for n- and p-channel transistors in a lightly doped substrate (Figs. 6-8c and 6-10). The substrate may be either a lightly doped wafer of n or p material, or a thin, lightly doped epitaxial layer on

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