

PHYSICS AND TECHNOLOGY OF SEMICONDUCTOR DEVICES

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Preface

The 1950's was a period of prominence and a most of the research. The 1960's can be characterized by devices and integrated germanium devices.

The purpose of this book is to describe the technology and technology of the technology. To be successful in the operation and the operation of the fabrication and the technology by other technology to be very difficult to concentrate on alloy germanium silicon diode. A characteristic of the observations on concentrated on alloy devices. in dealing with

n-channel device which we have already considered in Chapter 9 in connection with studies of semiconductor surfaces. This device is illustrated in Figure 11.1. It consists of a *p*-type silicon substrate into which two *n*⁺ regions, the *source* and the *drain*, are diffused. The region between the source and the drain is under the influence of a metal field plate or *gate*. If a large positive voltage is applied to the gate, the surface of the underlying *p*-type silicon can be inverted and a conductive *n*-type *channel* can be induced connecting source and drain. The conductivity of this channel can then be modulated by varying the gate voltage.

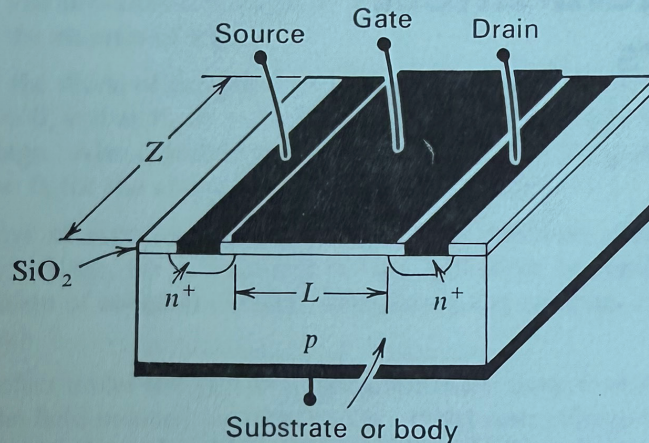


Fig. 11.1 *n*-Channel surface field-effect transistor.

We first consider the principles of the operation of such a surface field-effect transistor. Then we discuss some important characteristics of surface field-effect transistors: the current-voltage characteristics, the transconductance, and the gate leakage current. Finally, we consider the modifications of the simple theory. Insofar as possible, we attempt to maintain a parallelism between the treatment of the surface field-effect transistor and its sister device, the junction field-effect transistor discussed in Chapter 8.

11.1 PRINCIPLES OF OPERATION

Let us consider the situation when a large enough gate voltage is applied to induce an *n*-type inversion layer between the source and the drain regions, as shown in Figure 11.2. The cases of small and large drain voltages are considered separately. For small drain voltages, the channel induced between source and drain essentially behaves like a resistor. Its resistance, as shown in Chapter 9, is

$$R = - \frac{L}{Z\mu_n Q_n} \quad (11.1)$$

for $V_D \leq V_{Dsat}$. Note that a high mobility is desirable for a large cut-off frequency as in the case of junction field-effect transistors.

c. Source-to-Drain Resistance in Saturation⁵

We have seen in the previous section that after saturation the potential at the end of the inversion layer—at the point X —will be fixed at the value V_{Dsat} . As the drain voltage is increased further, the reverse bias across the drain junction will increase. As a result, the depletion region separating point X from the drain will widen and the point X will move toward the source, as indicated in Figure 11.2c. Thus the effective channel length will become shorter and, as a result, the drain current will increase slightly with increasing drain voltage, resulting in an upward tilting of the current-voltage characteristics beyond saturation. This phenomenon is particularly prominent for devices with small channel length L .

d. Effect of Series Resistance

The same considerations that were applied in the case of junction field-effect transistors lead to the conclusion that the effect of unmodulated series resistances near the source and the drain will be to lower the observed channel conductance and transconductance as compared to their values without series resistances according to the formulas

$$g(\text{obs}) = \frac{g}{1 + (R_s + R_d)g} \quad [\text{Linear region}] \quad (11.23)$$

and

$$g_{msat}(\text{obs}) = \frac{g_{msat}}{1 + R_s g_{msat}}, \quad [\text{Saturation region}] \quad (11.24)$$

where g and g_{msat} denote the channel conductance and transconductance in the absence of series resistances.

Because in a surface field-effect transistor of the type illustrated in Figure 11.1 all of the channel region is under the influence of the gate, the series-resistance effect is considerably less important than in junction field-effect transistors.

11.4 OTHER TYPES OF SURFACE FIELD-EFFECT TRANSISTORS

The preceding discussion so far was for an n -channel device of the type where we have to apply a positive voltage to the gate in order to bring

about the onset of channel conduction. By complete analogy, the discussion could have been applied to a p -channel device where a negative gate voltage would have been required to bring about channel conduction. Because with zero gate voltage applied neither of these devices conducts, such devices are called *normally "off"* MOS transistors.

By contrast, a *normally "on"* device can be made by suitable control of the flat-band voltage. Thus, if V_{FB} is sufficiently negative in the case of an n -channel device or positive in the case of a p -channel device, a conducting channel exists even with zero gate voltage applied. In such a case, the channel conductance can be both increased and decreased with suitable variation of the gate voltage.

The normally "off" n - and p -channel devices as well as a normally "on" n -channel device are illustrated in Fig. 11.8. In all three devices the conducting channel is induced by surface fields, whether the surface fields are due to a gate voltage or to charges within the oxide. Thus we may call these devices *field-induced channel* devices. It is also possible to build-in a channel metallurgically. Two examples of such *metallurgical channel* devices are shown in Figure 11.9. The first of these, illustrated in Figure 11.9a, is made by epitaxially growing an n -type film on a p -type substrate.⁶ The conductivity between the source and drain regions is then modulated

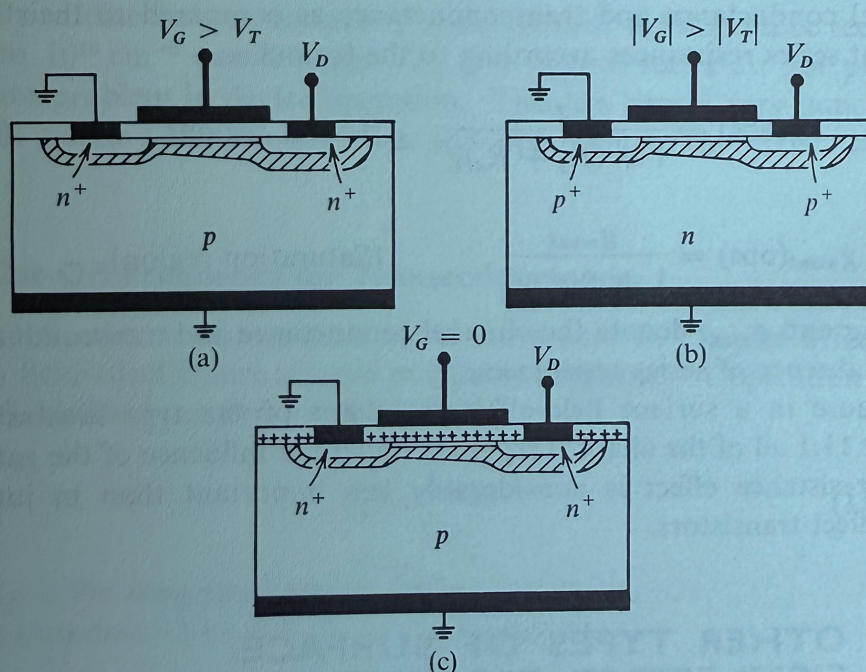


Fig. 11.8 Surface field-effect transistors with field-induced channels.

- (a) Normally "off" n -channel device.
- (b) Normally "off" p -channel device.
- (c) Normally "on" n -channel device.