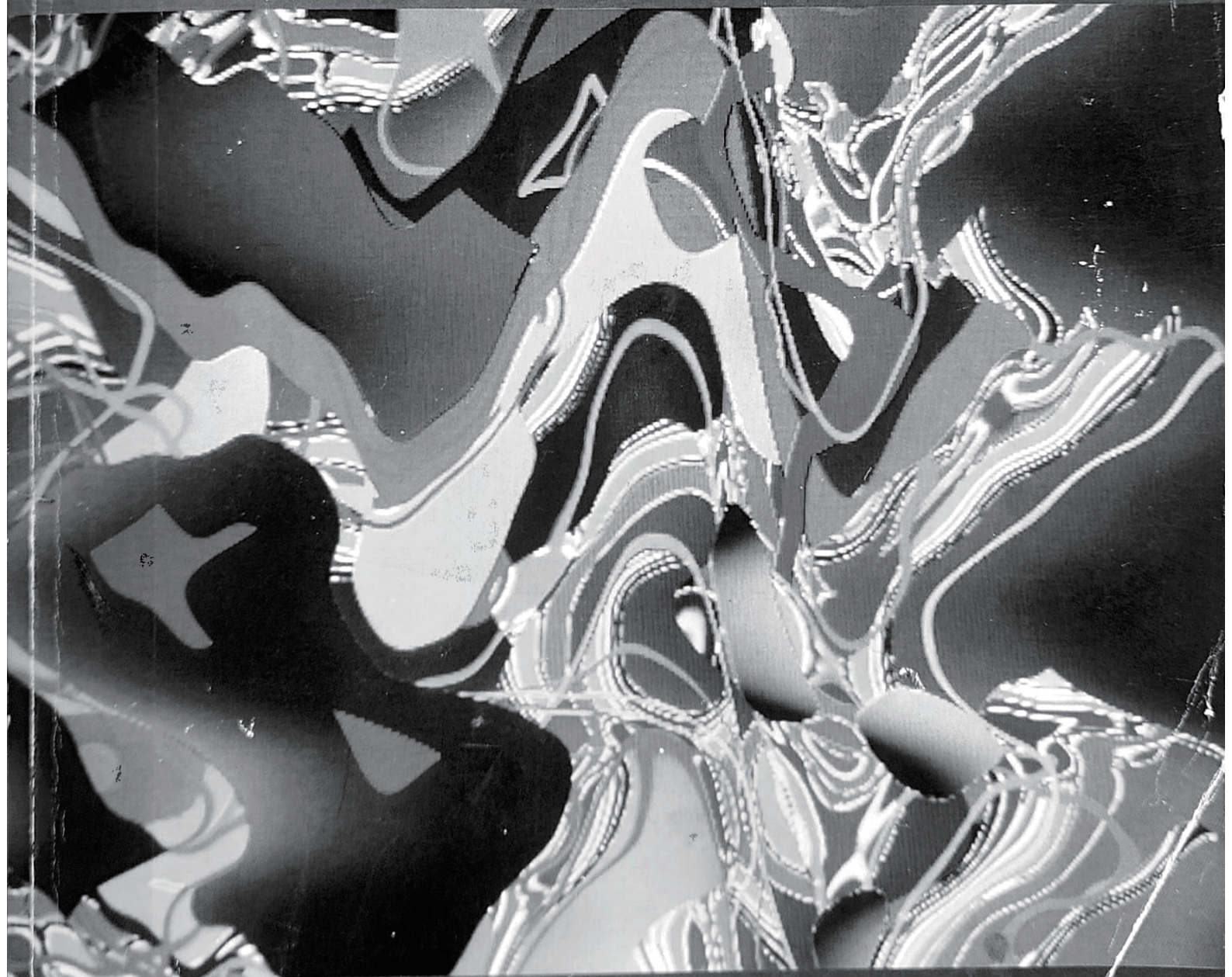


Semiconductor Manufacturing Technology



Michael Quirk
Julian Serda

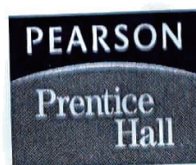
SEMICONDUCTOR MANUFACTURING TECHNOLOGY

MICHAEL QUIRK

STAKTEK CORPORATION

JULIAN SERDA

ADVANCED MICRO DEVICES



Pearson Education International

Library of Congress Cataloging-in-Publication Data

Quirk, Michael

Semiconductor manufacturing technology / Michael Quirk, Julian Serda.

p. cm.

ISBN 0-13-081520-9

1. Electronic industries. 2. Semiconductors—Design and construction. I. Serda, Julian.

II. Title.

TK7836.Q27 2001

00-041653

Vice President and Publisher: Dave Garza

Editor in Chief: Stephen Helba

Assistant Vice President and Publisher: Charles E. Stewart, Jr.

Production Editor: Alexandrina Benedicto Wolf

Production Coordination: Lithokraft II

Design Coordinator: Robin G. Chukes

Cover Designer: Linda Fares

Cover Image: John Foxx

Production Manager: Matthew Ottenweller

Marketing Manager: Barbara Rose

This book was set in Times Roman by Lithokraft II. It was printed and bound by R. R. Donnelley & Sons Company. The cover was printed by Phoenix Color Corp.

Copyright © 2001 by Prentice-Hall, Inc., Upper Saddle River, New Jersey 07458. All rights reserved. Printed in the United States of America. This publication is protected by Copyright and permission should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. For information regarding permission(s), write to: Rights and Permissions Department.

**Prentice
Hall**

10 9 8 7 6 5 4 3
ISBN 0-13-081520-9

CHAPTER 17

ION IMPLANT

Intrinsic silicon crystal structure is formed by silicon covalent bonds. As explained in Chapter 2, intrinsic silicon is a poor conductor. Silicon only becomes useful as a semiconductor when its structure and conductivity are altered by adding small amounts of impurities called dopants. This process is referred to as doping. The doping of silicon is fundamental to pn junction fabrication in semiconductor devices. Ion implantation is the primary method for doping wafers.

Doping is widely used throughout wafer fabrication. Dopants are precisely and uniformly placed into the device to alter its electrical performance. Silicon chips require doping with Group IIIA and Group VA dopants

for many different reasons, which will be discussed in this chapter.

The continual shrinking of chip critical dimensions and the subsequent increase in chip packing density force the scaling of all device elements. An example of this is the reduction of the polysilicon gate length to obtain a narrower channel region. A shorter channel length requires shallower junction depths for the source and drain doped regions. Junction depths are ultrashallow for chips designed at the 0.18 μm and below technology nodes. The junction depth requirements decrease to 30 ± 10 nm for devices with a CD of 0.1 μm .¹

OBJECTIVES

After studying the material in this chapter, you will be able to:

1. Explain the purpose and applications for doping in wafer fabrication.
2. Discuss the principles and process of dopant diffusion.
3. Provide an overview of ion implantation, including its advantages and disadvantages.
4. Discuss the importance of dose and range in ion implant.
5. List and describe the five major subsystems for an ion implanter.
6. Explain annealing and channeling in ion implantation.
7. Describe different applications of ion implantation.

INTRODUCTION

Doping is the introduction of a dopant into the crystal structure of a semiconductor material to modify its electronic properties (e.g., electrical resistivity). As discussed in Chapter 2, certain Group IIIA and VA elements are used as dopants in wafer fabrication. For review, Table 17.1 on page 476 highlights the four principal dopants used in semiconductor manufacturing.

Dopant species are also referred to as impurities but should not be confused with contaminating impurities. Dopants are introduced into the silicon and other fabrication materials for a variety of reasons. For instance, dopants such as boron and phosphorus are used to form the majority carriers in silicon devices, to form conductive layers in the wafer, or to alter material properties (e.g., doping SiO_2 to form borophosphosilicate glass, or BPSG). The polysilicon gate electrode is doped for conductivity.

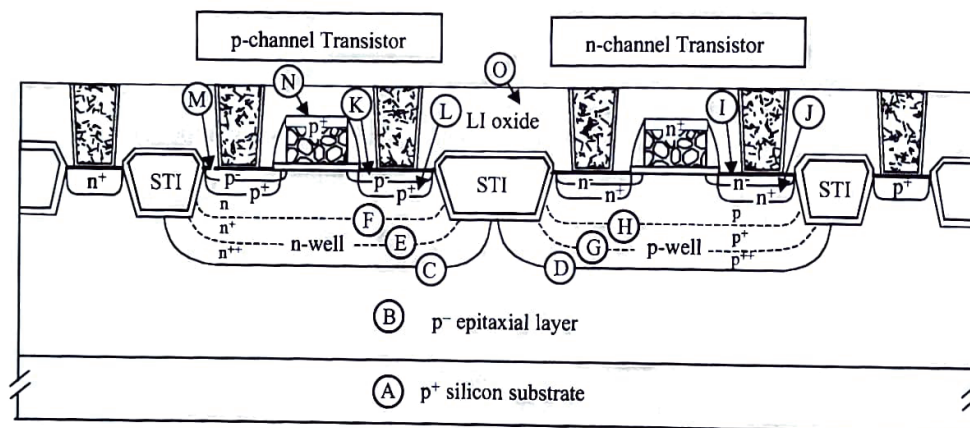
There are two techniques in wafer fabrication for introducing dopant elements to the wafer materials: thermal diffusion and ion implantation. *Thermal diffusion* uses high temperature to move the dopant through the silicon lattice structure. This method is dependent on time and temperature. *Ion implantation* introduces dopants into the substrate through a high-voltage ion bombardment. The dopants are implanted into the wafer through high-energy collisions at the atomic level. In the beginning of semiconductor manufacturing, thermal diffusion was the primary method for doping the wafer. However, due to shrinking critical dimensions and the corresponding scaling requirements, nearly all dopant processes in modern wafer fabrication are now done

TABLE 17.1 Common Dopants Used in Semiconductor Manufacturing

Acceptor Dopant Group IIIA (p-Type)		Semiconductor Group IVA		Donor Dopant Group VA (n-Type)	
Element	Atomic Number	Element	Atomic Number	Element	Atomic Number
Boron (B)	5	Carbon	6	Nitrogen	7
Aluminum	13	Silicon (Si)	14	Phosphorus (P)	15
Gallium	31	Germanium	32	Arsenic (As)	33
Indium	49	Tin	50	Antimony	51

Note: Common dopants are shaded.

with ion implantation (see Figure 17.1). Table 17.2 outlines some critical processes commonly doped with ion implantation versus the limited doping done by diffusion. Figure 17.1 shows these doped regions on a cross section drawing of a CMOS inverter. Note the dopant type (p or n) and concentration (– or +) are also shown. The different doped regions labeled A to O are defined in Table 17.2.

**FIGURE 17.1** CMOS Structure with Doped Regions**TABLE 17.2*** Common Dopant Processes CMOS Fabrication

Process Step	Common Dopant Species	Ion Implant or Diffusion	Remarks
A. p ⁺ Silicon Substrate	B	Diffusion	The monosilicon crystal is doped during the crystal growing process.
B. p [−] Epitaxial Layer	B	Diffusion	The epitaxial layer is doped by diffusion during epitaxial silicon growth.
C. Retrograde n-well	P	Ion Implant	Retrograde well has dopant profile with peak concentration buried at a certain depth. The dopant concentration decreases as it approaches the surface.
D. Retrograde p-well	B	Ion Implant	Retrograde well has dopant profile with peak concentration buried at a certain depth.
E. p-Channel Punchthrough	P	Ion Implant	Phosphorus implanted more laterally than source/drain implants to keep electric field of drain from punching through p-channel and reaching source region.

Process Step	Common Dopant Species	Ion Implant or Diffusion	Remarks
F. p-Channel Threshold Voltage (V_T) Adjust	P	Ion Implant	Implant phosphorus to adjust MOS V_T threshold voltage.
G. n-Channel Punchthrough	B	Ion Implant	Boron is implanted more laterally than source/drain implants to keep electric field of drain from punching through n-channel and reaching source region.
H. n-Channel V_T Adjust	B	Ion Implant	Implant boron through oxide layer to adjust MOS threshold voltage.
I. n-Channel Lightly Doped Drain (LDD)	As	Ion Implant	Low-dose implant of arsenic in region adjacent to the n-channel to improve electrical performance by reducing the peak electrical field and therefore hot carriers, which minimizes interface charges trapped in the gate oxide.
J. n-Channel Source/Drain (S/D)	As	Ion Implant	Higher implant dose of arsenic to form n-channel source and drain.
K. p-Channel LDD	BF_2	Ion Implant	Low-dose implant of boron in region adjacent to the p-channel to improve electrical performance between drain and channel region.
L. p-Channel S/D	BF_2	Ion Implant	Higher implant dose of boron to form p-channel source and drain.
M. Silicon	Si	Ion Implant	Implant with nondopant atom to amorphize silicon to reduce transient enhanced diffusion (TED) and channeling effects.
N. Doped Polysilicon	P or B	Ion Implant or Diffusion	Doping of polysilicon gate electrode to make conductive.
O. Doped SiO_2	P or B	Ion Implant or Diffusion	Doped oxide to obtain material benefits (e.g., create better flow and serve as getter).

*Adapted from E. Rimini, *Ion Implantation: Basics to Device Fabrication*, (Boston: Kluwer Academic Publishers, 1995).

Ion implantation typically follows photolithography in the general process flow (see Figure 17.2 on page 478); although, there may be some processes that call for the use of an etched-oxide layer to serve as a mask during either diffusion doping or ion implant. In this case, wafers could flow from etch to diffusion or ion implant. Ion implantation plays a crucial role in chip performance improvement because of the need for smaller dimensions. Transistor performance is increasingly dependent on precise doping profiles in the silicon that are achievable only with ion implant.

Doped Regions

Recall from Chapter 4 that a wafer is uniformly doped with dopant atoms during the crystal growth process to create a p-type or n-type wafer. The type of dopant depends on the manufacturer's specification. During wafer fabrication, dopants are selectively introduced to create the devices on the individual wafers. The selective introduction of dopants into masked openings on the wafer forms a *doped region* where dopants reside within the silicon crystal structure (see Figure 17.3 on page 478). The doped region is characterized by its *dopant profile*, which determines the amount of dopant actually added in the doped region as a function of depth.