

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

**FORCE MOS TECHNOLOGY, CO.,
LTD.,**

Plaintiff,

v.

ASUSTEK COMPUTER, INC.,

Defendant.

**Civil Action No. 2:22-cv-00460-JRG
JURY TRIAL DEMANDED**

EXPERT REPORT OF STANLEY R. SHANFIELD, PH.D.

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Ex. A	CV of Stanley R. Shanfield, PH.D.
Ex. B	Materials Considered by Stanley R. Shanfield, PH.D.
Ex. C	U.S. Patent No. 7,629,634 (“the ’634 Patent”) (FORCE-MOS0000001-14)
Ex. D	U.S. Patent No. 7,812,409 (“the ’409 Patent”) (FORCE-MOS0000027-38)
Ex. E	U.S. Patent No. 7,847,346 (“the ’346 Patent”) (FORCE-MOS0000015-26)
Ex. F	File History for the ’634 Patent (“’634 FH”) (FORCE-MOS0000039-124)
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Ex. H	File History for the ’346 Patent (“’346 FH”) (FORCE-MOS00000125-226)
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Ex. J	U.S. Patent Publication No. 2004/0021174 (“Kobayashi 174”) (ASUS_00000626-644)
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Ex. V	U.S. Patent No. 7,102,182 (“Takemori”) (ASUS_00000119-157)
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Ex. CC	U.S. Patent No. 6,621,107 (“Blanchard 107”) (ASUS_00015798-817)

I. INTRODUCTION

1. My name is Stanley R. Shanfield, Ph.D. I have been retained by Defendant ASUSTek Computer, Inc. (“ASUS” or “Defendant”) as an independent expert in *Force Mos Tech., Co., Ltd. v. ASUSTek Comput., Inc.*, No. 2:22-CV-460-JRG (E.D. Tex.). I expect to testify concerning the subjects outlined in this report.

2. As part of my engagement, I have been asked to provide analysis and expert opinions on the validity of certain claims of U.S. Patent Nos. 7,629,634 (the “634 Patent”), 7,847,346 (the “346 Patent”), and 7,812,409 (the “409 Patent”) (collectively, the “Asserted Patents”). I have been further asked to provide analysis and expert opinions on the unenforceability of the Asserted Patents.

3. This report is a description of the testimony I expect to offer in the litigation. I further respectfully reserve the right to supplement my analysis in response to any alternative opinions offered by Plaintiff Force Mos Technology, Co., Ltd. (“Force MOS” or “Plaintiff”). For example, it is my understanding that Force MOS may submit an expert report relating to the subject matter addressed in this report. I reserve the right to rebut any positions taken in Force MOS’s expert report. Further, to the extent that Force MOS offers new theories of infringement, I reserve the right to identify new prior art that invalidates the claims under Force MOS’s new infringement theories, as well as providing additional opinions regarding invalidity in view of additional prior art.

4. I reserve the right to modify or supplement my opinions, as well as the basis for my opinions, should any new documents, testimony, or other evidence emerge during this litigation, including depositions that have yet to be taken or deposition transcripts that have not yet been completed.

5. Throughout this report, I refer to specific pages of patents and other technical documents, articles, and standards. These citations are illustrative and are not intended to convey that they are the only sources to support the propositions for which they are cited. For example, I may refer to text describing a figure and in so doing incorporate the figure. Similarly, in citing to a figure I incorporate the corresponding text describing the figure.

6. If I am called upon to testify at trial or any other proceeding about this report, I may cite other documents or information similar to that specifically identified herein or such information that is responsive to any testimony or evidence provided by Force MOS. I may also prepare and use presentations, graphics, animations, demonstrations, and other aids to explain my analysis and opinions.

II. COMPENSATION

7. I am being compensated at \$395 per hour for testifying and non-testifying work, excluding reimbursement for reasonable and necessary out-of-pocket expenses incurred in connection to my engagement. My compensation is based solely on the amount of time that I devote to this proceeding and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

III. BASIS FOR OPINIONS

A. Educational Background and Professional Experience

8. I have personal knowledge or have developed knowledge of these technologies based upon education, training, or experience, of the matters set forth herein.

9. My curriculum vitae (“CV”) is attached hereto as Exhibit A and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My curriculum vitae also

includes information about my expert witness experience, with case numbers where available. Below is a short summary of my professional qualifications.

10. I have four decades of professional experience as a practicing engineer in the field of semiconductor fabrication, semiconductor device design and modeling, and circuit design.

11. I received my Bachelor of Science degree in Physics from the University of California, Irvine, in 1977. I earned my Ph.D. from the Massachusetts Institute of Technology (“MIT”) in 1981, with a dissertation on the physics of high field superconductors. During my doctoral program at MIT, I received a four-year scholarship from the Energy Research and Development Administration (now part of the United States Department of Energy).

12. After earning my Ph.D. in 1981, I began work as a Staff Scientist, then later as a Senior Staff Scientist, at Spire Corporation in Bedford, Massachusetts. At Spire Corporation, I developed new methods for low temperature deposition of epitaxial silicon using plasma-assisted chemical vapor deposition (“CVD”) epitaxial. I also built, operated, and characterized an ion-assisted deposition system for making coatings for semiconductors.

13. In 1985, I joined Raytheon Corporation, located in Lexington/Andover, Massachusetts, as a Section Manager in Semiconductors & Integrated Circuits. My work focused on developing processes for the fabrication of high power, high frequency planar MOSFETs and DMOSFETs, and multi-function integrated circuits using these devices. In 1992, I was promoted to Section Manager and then Research Laboratory Manager, where I led a 90-person team developing high performance semiconductor devices and circuits, including measurement, assembly, and wafer fabrication processes. My work then focused on the design, fabrication, and measurement of state-of-the-art complimentary metal-oxide semiconductor (“CMOS”) devices of the time, primarily for digital and mixed signal applications.

14. I have had several years of hands-on experience in the design, fabrication, and testing of silicon and SiC DMOSFETs in various development programs at Raytheon Research Division during the 1990s. This experience involved a focus on issues like optimizing power transistor layout and perfecting oxide growth, ion implantation, and ohmic contact formation. During this time, I also investigated CVD and MBE epitaxial growth methods in silicon and alternative materials systems. DMOSFETs developed during those years were used for switching power supply and S-band microwave RF power amplifiers in Raytheon products.

15. In 1996, I was promoted to Director of Semiconductor Operations. In this capacity, I was involved in multiple aspects of CMOS-based IC and MOSFET fabrication for commercial and military applications. I was also responsible for a custom silicon application-specific integrated circuit (“ASIC”) design and development group and the associated layout and simulation facilities. I was directly involved in the design of certain commercial products produced in the facility, including flip-chip modules for an AT&T wireless base station, and the transmit/receive modules for Iridium satellite handsets using chip-on-board (CoB).

16. After 14 years at Raytheon, I became part of the founding team for AXSUN Technologies, located in Bedford/Billerica, Massachusetts, as a Vice President of Operations in 1999. In this capacity, I designed a complete facility for semiconductor processing, including establishing a fabrication facility in Belfast, North Ireland for producing thick oxide silicon-on-insulator material. AXSUN was eventually sold to a larger technology company.

17. In 2003, I joined Draper Laboratory at MIT (“Draper”), located in Cambridge, Massachusetts, where I am still employed. I have taken roles such as Division Leader of Advanced Hardware Development and I am a Distinguished Member of Technical Staff and Technical Director. In my time at Draper, I have been responsible for in-house module and electronic system

designs, fabrication, and have been involved in CMOS foundry implementation for multiple ASIC designs.

18. I am not now and have never been an employee of the Defendant.

19. I have been a member of many professional societies and electrical engineering industry groups over the years, such as the Institute of Electrical and Electronics Engineers (IEEE) and the American Physical Society (APS).

20. I have received a number of academic awards and honors over the years, including awards and honors for the best Draper patent and most successful Draper development project.

21. I have also authored or co-authored over 25 technical papers covering various aspects of semiconductor devices and advanced semiconductor manufacturing.

22. I am a named inventor or co-inventor on multiple patents covering aspects of semiconductor devices, system and circuit design, and semiconductor manufacturing.

23. I have previously testified in patent and trade secret cases, some of which concerned semiconductor device design and processing, semiconductor equipment or electronic circuits and components, before various District Courts, the International Trade Commission and the Patent Trial and Appeal Board. I have been qualified in multiple courts to offer expert opinions on semiconductor issues.

B. Materials Considered and Methodology

24. To prepare this report, I have considered and reviewed the '634, '346, and '409 Patents and their file histories. I also considered the competing claim construction proposals of Force MOS and ASUS. To prepare this report, I also have relied upon my education, knowledge and experience with MOSFETs, any other relevant technologies, as well as my extensive background detailed above. As already discussed, Exhibit A to this report is a copy of my

curriculum vitae, which further sets forth my education and experience. Exhibit B sets forth a complete list of all materials I have considered to prepare this report.

25. To prepare this report, I also have relied upon my understanding of certain legal principals regarding invalidity and unenforceability of patents. I am not an expert in patent law. I therefore have relied upon the statement of legal principles set forth in this report, conversations with legal counsel as needed to further inform me about relevant legal principles, and also my experience as a technical expert in patent cases as it relates to anticipation and obviousness as determined by a person of ordinary skill in the art.

IV. LEGAL UNDERSTANDINGS

26. I am not an attorney. However, I have been informed of several principles of patent law, which I used in arriving at my conclusions. In this section I describe my understanding of certain legal standards. I have been informed of these legal standards by counsel for ASUS and have applied my understanding of these legal standards in my analysis as detailed below.

A. Claim Construction

27. I understand that there are certain claim terms in contention, and the judge assigned to this case has not yet issued a claim construction order regarding these terms. ASUS's and Force MOS's proposed constructions for these terms are set forth *infra* in Section V. I understand that when the judge issues the claim construction order for these terms, those constructions apply as a matter of law in this litigation. In the interim, I have applied the different claim constructions proposed by ASUS and Force MOS. As to terms that were not construed, I understand that those terms are to be given their plain and ordinary meaning as understood by one of ordinary skill in the art at the time of the claimed invention and in light of the intrinsic evidence, which I understand includes the patent specification and the prosecution history, including any references cited during prosecution, and including any post-grant proceedings at the Patent Office.

B. Anticipation

28. I understand that a patent claim is invalid as “anticipated” if all the limitations of that claim were present in a single device or method that was previously known of, used, or described in a single printed publication or patent such that a person having ordinary skill in the art, looking at the single reference, could make and use the claimed invention without undue experimentation.

29. I understand that a claim can be anticipated even if all the limitations of that claim are not expressly found in a prior art reference if the missing limitations are inherently present, i.e., if the prior art necessarily functions in accordance with, or includes, the claim limitations. It is acceptable to examine evidence outside the prior art reference (extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it, i.e., inherent.

30. I understand 35 U.S.C. § 102 sets forth bases under which a reference or system may be prior art, which is recited below:

35 U.S.C. § 102

A person shall be entitled to a patent unless —

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or
- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or
- (c) he has abandoned the invention, or
- (d) the invention was first patented or caused to be patented, or was the subject of an inventor’s certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor’s certificate filed more than twelve months before the filing of the application in the United States, or

- (e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language; or
- (f) he did not himself invent the subject matter sought to be patented, or
- (g) (1) during the course of an interference conducted under section 135 or section 291, another inventor involved therein establishes, to the extent permitted in section 104, that before such person's invention thereof the invention was made by such other inventor and not abandoned, suppressed, or concealed, or (2) before such person's invention thereof, the invention was made in this country by another inventor who had not abandoned, suppressed, or concealed it. In determining priority of invention under this subsection, there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

C. Obviousness

31. I understand that the types of 35 U.S.C. § 102 prior art described above can individually be a basis for invalidating a patent, or these references can be combined to show a patent is invalid as obvious under 35 U.S.C. § 103. I have been informed that it is established law that a rejection for obviousness under § 103 can be based on a reference which happens to anticipate the claimed subject matter.

32. I understand that even if a single reference does not contain every limitation of a patent claim, it can still invalidate that claim if it renders the claimed invention obvious when considered by a person having ordinary skill in the art considering other prior art references or devices including the knowledge of those skilled in the art at the time of the alleged invention. If the differences between the claimed invention and the prior art are such that the claimed invention,

as a whole, would have been obvious to a person having ordinary skill in the art at the time the invention was made, without the benefit of hindsight, then the claim is invalid.

33. I understand that a patent claim is obvious if, at the time the invention was made, it would have been obvious to one of ordinary skill in the art considering the teachings of the relevant prior art. I understand that the analysis of obviousness involves several factual inquiries including the scope and content of the prior art, the differences between the prior art and the claim, and the level of ordinary skill in the art at the time of the invention.

34. I understand that a reference qualifies as prior art for obviousness purposes when it is analogous to the claimed invention. The test for determining what art is analogous is: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.

35. I understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. In other words, when a claim simply arranges prior art elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, then such a combination is obvious. Moreover, when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another that is known in the field, the combination is likely to be obvious unless the combination yields an unpredictable result.

36. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If one of ordinary skill in the art can implement a predictable variation, such a variation is likely unpatentable. For the same reason, if a technique has been used to improve one device, and

one of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. One question to consider is whether the improvement is more than the predictable use of prior art elements according to their established functions.

37. I understand that it may often be necessary, in a validity analysis, to look to interrelated teachings of multiple patents; the effects of demands known to the design community (i.e., the goals considered by a typical practitioner in improving a product) or present in the marketplace; and the background knowledge possessed by one of ordinary skill in the art, all to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

38. I understand that a finding of obviousness can also be supported by some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

39. I understand that a validity analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim; it is appropriate to take account of the inferences and creative steps that one of ordinary skill in the art would employ. I understand that a person of ordinary skill is also a person of ordinary creativity.

40. I understand that a claim composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. I understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed invention does. Therefore, I understand that in determining whether a claimed combination is obvious, the correct question is whether the combination was obvious to one of ordinary skill in the art at the time the

patent application was filed. I understand that one of the ways in which subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims. I understand that any need or problem known in the field of endeavor at the time of alleged invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

41. I understand that one should not assume that a person of ordinary skill in the art attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem. Instead, I understand that since familiar items may have obvious uses beyond their primary purposes, in many cases one of ordinary skill in the art will be able to fit the teachings of multiple prior art references together like pieces of a puzzle.

42. I understand that, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, one of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, then it is likely not a product of innovation but of ordinary skill and common sense. I understand that, in such an instance, the fact that the combination was obvious to try may show that the combination is obvious.

43. I understand that, when determining whether a claimed combination is obvious, the correct analysis is not whether one of ordinary skill in the art, writing on a blank slate, would have chosen the particular combination of elements described in the claim. Instead, I understand the correct analysis considers whether one of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to selecting the combination claimed.

D. Secondary Considerations

44. It is my understanding that, in order to rebut a showing of obviousness over the prior art, Force MOS and its expert may attempt to show “secondary considerations” of non-obviousness, such as, for example, evidence of commercial success of the invention, long-felt but unsolved needs, failure of others, unexpected results, and evidence of industry acquiescence. I am further informed that, to support a finding of non-obviousness, the inventor must generally show a “nexus” between the secondary considerations and the features of the invention as claimed. For example, a secondary consideration such as commercial success is not relevant to nonobviousness unless the evidence shows that the commercial success was attributable to the merits and features of the claimed invention as opposed to being attributable to features that already existed in the prior art.

E. Persons of Ordinary Skill in the Art

45. I understand that the person of ordinary skill in the art (“POSA” or “POSITA”) is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill in the art may include: (a) type of problems encountered in the art; (b) prior art solutions to those problems; (c) rapidity with which innovations are made; (d) sophistication of the technology; and (e) educational level of active workers in the field. In a given case, every factor may not be present, and one or more factors may predominate. I understand that the hypothetical person having ordinary skill in the art to which the claimed subject matter pertains would, of necessity have the capability of understanding the scientific and engineering principles applicable to the pertinent art.

46. I understand that references which do not qualify as prior art because they post-date the claimed invention may be relied upon to show the level of ordinary skill in the art at or around the time the invention was made. I understand that documents not available as prior art, because

the documents were not widely disseminated, may be used to demonstrate the level of ordinary skill in the art. For example, a document may be relevant to establishing a motivation to combine which is implicit in the knowledge of one of ordinary skill in the art.

F. Written Description

47. I understand that the claims of a patent are unpatentable under 35 U.S.C. § 112 if the patent specification does not contain adequate written description of the claimed invention. Based on my involvement in the patent applications on which I am a named inventor, I am aware that in the patent application process, the Applicant may keep the originally filed claims, or change the claims between the time the patent application is first filed and the issuance of a patent. An Applicant may amend the claims or add new claims during prosecution but the written description requirement ensures that the issued claims correspond to the scope of the written description as provided in the original application.

48. I also understand that the written description requirement is satisfied if a POSITA reading the original patent application would have recognized that it describes the full scope of the claimed invention as it is finally claimed in the issued patent and that the inventor actually possessed that full scope by the filing date of the original application. The written description requirement may be satisfied by a combination of the words, figures and formulae contained in the patent application. The full scope of a claim or any particular requirement in a claim, need not be expressly disclosed in the original patent application if a POSITA would have understood that the full scope is in the written description in the as-filed patent application.

G. Enablement

49. It is my further understanding that a patent claim is invalid under 35 U.S.C. § 112 for lack of enablement if the specification does not contain a sufficiently full and clear description of how to make and use the full scope of the claimed invention. To be enabling, the patent must

permit a POSITA to make and use the full scope of the claimed invention at the time of original filing without having to conduct undue experimentation. In deciding whether a POSITA would have to experiment unduly in order to make and use the invention, I understand several factors, so-called *Wands* factors, may be considered including: (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims. *In re Wands*, 858 F.2d 731, 736–37 (Fed. Cir. 1988). I understand that no one or more of these factors alone is dispositive. Rather, whether the degree of experimentation required is undue requires weighing these factors in the context of the claimed invention and the state of the art at the time of the original application. I also understand that analysis of the *Wands* factors is not mandatory.

50. Furthermore, it is my understanding that the Supreme Court has explained that “if a patent claims an entire class of processes, machines, manufactures, or compositions of matter, the patent’s specification must enable a person skilled in the art to make and use the entire class. In other words, the specification must enable the full scope of the invention as defined by its claims. The more one claims, the more one must enable.” *Amgen, Inc. v. Sanofi*, 143 S. Ct. 1243, 1254 (2023).

H. Unenforceability of a Patent

51. I understand that inequitable conduct is an equitable defense to patent infringement that, if proven, bars enforcement of a patent.

52. I understand that inequitable conduct occurs when a patentee breaches his or her duty to the U.S. Patent and Trademark Office (“USPTO” or “Patent Office”) of candor, good faith,

and honesty. I understand that a party, including, for example, an applicant, an inventor, or the prosecuting attorney appearing before the USPTO, has a duty to disclose all information known to that individual to be material to patentability.

53. I understand that a party seeking to prove inequitable conduct must show that the patent applicant made misrepresentations or omissions material to patentability, and that he/she did so with the specific intent to mislead or deceive the USPTO, and that deceptive intent was the single most reasonable inference to be drawn from the evidence. I understand that a party can prove the element of materiality by showing that the patentee withheld or misrepresented information that, in the absence of the withholding or misrepresentation, would have prevented a patent claim from issuing. I understand that the specific intent to commit acts constituting inequitable conduct may be inferred from indirect and circumstantial evidence, but deceptive intent must be the single most reasonable inference drawn from the evidence.

54. I understand that prior art is material if there is a substantial likelihood that a reasonable Patent examiner would consider it important or material in deciding whether to allow the application to issue as a patent.

V. CLAIM CONSTRUCTION

55. It is my understanding that the judge has yet to issue a claim construction order. I understand that ASUS and Force MOS have agreed on the claim construction of the following terms and that I should apply these constructions in forming my opinion.

Term	Construction
“front” (‘634 Patent, cl. 1) (‘346 Patent, cl. 1)	The side of the three-dimensional device to which the photolithography was applied
“back” (‘346 Patent, cl. 1)	The side of the three-dimensional device opposite the “front”
“top” (‘634 Patent, cl. 1) (‘346 Patent, cls. 1, 2, 16)	Referring to the direction of the “front”

“upper” (‘634 Patent, cl. 1) (‘346 Patent, cl. 18)	(e.g., the top surface of a layer refers to the side of the layer that is facing toward the front of the device)
“bottom” (‘634 Patent, cls. 1, 17) (‘346 Patent, cls. 1, 17) “lower” (‘634 Patent cl. 1) “downwardly” (‘634 Patent, cl. 1)	Referring to the direction of the “back” (e.g., the bottom surface of a layer refers to the side of the layer that is facing toward the back of the device)

56. I understand that the terms that follow are disputed. I also understand that ASUS and Force MOS propose the following constructions that I should consider in formulating my opinions.

Patent and Claim No.	Claim Term	ASUS’s Proposed Construction	Force MOS’s Proposed Construction
’634 Patent, Claim 1	“a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer”	a plurality of trenched gates covered by said interlayer oxide film are formed on and extend from above said source layer through said base layer	Plain and ordinary meaning, <i>i.e.</i> : trenched gates are formed from top of source layer and extend down through the base layer (<i>i.e.</i> , gates need not “extend from above” said source layer)
’634 Patent, Claim 1	“the sidewalls of said trenches in said base layer”	entire sidewalls of said trenches in said base layer	Plain and ordinary meaning, <i>i.e.</i> : the portions of the source contact trenches’ sidewalls which are in the semiconductor material’s base layer, <i>i.e.</i> , no requirement that “entire” sidewalls of base layer be covered in lateral contact layer

'634 Patent, Claim 1	"lateral contact layer"	"requiring a region of dopant which is implanted into sidewalls of the source contact trenches, wherein implantation may occur before or after the source contact trenches are etched, the region to have a doping concentration between the base layer doping concentration and the base contact layer doping concentration"	"requiring a region of dopant which is implanted into sidewalls of the source contact trenches to have a dopant concentration between P and P+ ('P* doping') for an N-channel MOSFET or between N and N+ ('N* doping') in a P-channel MOSFET"
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Patent and Claim No.	Claim Term	ASUS's Proposed Construction	Force MOS's Proposed Construction
'409 Patent, Claim 1	"substantially square-shaped"	"from a top-view cross-sectional perspective, a square-shape that satisfies a design rule that the greatest difference between the longest distance and the shortest distance between the circular trench contacts and the trenched gates is significantly less than a predefined value"	Plain and ordinary meaning: "from a top-view cross-sectional perspective, having a largely or essentially square shaped, other than the recited 'rounded corners'"
'409 Patent, Claim 1	"rounded corners"	"corners that are truncated by design layout and then rounded"	Plain and ordinary meaning: "corners having a curved shape (i.e. like a portion of a circle or oval)"

'409 Patent, Claim 1	“circular trench contact”	“trench contact that is a circle by design layout”	Plain and ordinary meaning: “trench contact having a form shaped like a circle from a top-view cross-sectional perspective”
'409 Patent, Claim 1	“a top surface of said semiconductor substrate”	Indefinite or, in the alternative, “the top surface of the bottom base layer of the semiconductor power device”	Plain and ordinary meaning: “the top of the surface of the semiconductor material”
'409 Patent, Claim 1	“said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact”	“at all circumferential points along the sides of the circular trench contact, said source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates.”	Plain and ordinary meaning: “all around the circumference of a circular trench contact, from a cross-sectional perspective, source and body regions are located between the circular trench contact and the gate oxide lining of the trenched gates”

Patent and Claim No.	Claim Term	ASUS's Proposed Construction	Force MOS's Proposed Construction
'346 Patent, Claim 1	“plurality of source contact trenches . . . with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions”	a plurality of source contact trenches ... with vertical sidewalls substantially perpendicular to a top epitaxial surface within [entire/whole] said source regions	Plain and ordinary meaning, <i>i.e.</i> : in the second insulating layer and source layer, the source contact trench has sidewalls that are largely or essentially perpendicular to the top of the epitaxial layer (the surface of the semiconductor in which the trenches have been etched into), <i>i.e.</i> , no requirement as to “entire/whole” trench in source region being substantially perpendicular
'346 Patent, Claim 16	“a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions”	a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions within [entire/whole] said source regions	Plain and ordinary meaning, <i>i.e.</i> : substantially perpendicular to a top surface of said source regions” means essentially perpendicular to the top of the source regions (<i>i.e.</i> , the surface of the semiconductor in which the trenches have been etched into). No requirement that entire/whole source region have substantially perpendicular sidewalls.

'346 Patent, Claim 1	“plurality of source contact trenches . . . further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer”	a plurality of source contact trenches ... further extending into said body regions with tapered sidewalls [within entire/whole body regions] with respect to said top surface of said epitaxial layer	Plain and ordinary meaning, i.e.: as the source contact trench extends into the body region, it has sidewalls that are tapered (that is, the source contact trench in the body has narrower portions than portions in the source region), i.e., no requirement as to “entire/whole” trench in body region be tapered
'346 Patent, Claim 16	“a plurality of trench source contacts comprising a plurality of sidewalls, . . . two other sidewalls tapered with respect to said source regions”	a plurality of trench source contacts comprising a plurality of sidewalls, . . . two other sidewalls tapered with respect to said source regions within [entire/whole] said body regions	Plain and ordinary meaning, i.e.: tapered with respect to said source regions” means “sidewalls that are tapered with respect to the top of the source regions (i.e. the surface of the semiconductor in which the trenches have been etched into), that is, the source contact trench has narrower portions deeper in the trench. No requirement that entire/whole body region have tapered side walls.
'346 Patent, Claim 17	“P+ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions”	“P+ areas [completely encompassing/enclosing] [the two other sidewalls tapered within entire/whole body regions with respect to said source regions] and [a] bottom of [the plurality of trench source contacts] within said P-body regions”	Plain and ordinary meaning, i.e.: P+ region follow contours of sidewalls and bottom of trench source contact. No requirement that P+ regions completely encompass tapered sidewalls.

57. In interpreting the Asserted Patents, I have applied the constructions set forth in the tables above. For terms where alternate claim constructions are provided, I have applied these alternate claim constructions. For terms not construed, I have applied the plain and ordinary meaning as understood by one of ordinary skill in the art at the time of the claimed invention, in light of the intrinsic evidence, which I understand includes the patent specification and the prosecution history, including any prior art cited during the prosecution.

VI. PRIORITY DATES FOR THE ASSERTED PATENTS

58. I understand that Force MOS claims the earliest priority date for the '634 Patent is February 23, 2008, the filing date of U.S. Patent Application Serial No. 12/036,243. *See* Ex. F, 634 FH.

59. I understand that Force MOS claims the earliest priority date for the '409 Patent is December 4, 2006, the filing date of U.S. Patent Application Serial No. 11/633,366. *See* Ex. G, 409 FH.

I understand that Force MOS claims the earliest priority date for the '346 Patent is November 26, 2008, the filing date of U.S. Patent Application Serial No. 12/292,780. *See* Ex. H, 346 FH.

VII. LEVEL OF ORDINARY SKILL IN THE ART

60. It is my opinion that a POSITA in the field of the '634, '409, and '346 Patents at the time of the earliest effective priority date would have earned a Master's degree in electrical engineering (or a related field) and had at least two years of relevant work experience in the field of integrated circuit design and manufacturing. I consider myself a POSITA of the '634, '409, and '346 Patents because I had at least the level of a POSITA in the relevant timeframe.

VIII. STATE OF THE ART FOR THE ASSERTED PATENTS

61. At the effective filing dates of the Asserted Patents, a POSITA would have known that the development of MOSFETs, and specifically Power MOSFETs, focuses on the tradeoff between minimizing the ON-Resistance and maximizing the breakdown voltage capability, for a given device area.

62. The key evolutionary advancement of the Power MOSFET involves going from a planar DMOS (Double-Diffused MOS) to a trench MOSFET, where the gate and its associated channel of the transistor is folded vertically onto a trench into the silicon. While the use of a trench Power MOSFET reduces the ON-Resistance significantly through the reduction of the junction FET (JFET) component, the dopant profile optimization of the body region and the drift region continues to be the key feature in this optimization effort.

63. However, even for well-designed doping profiles in the drift region (N-region) and the body region (P-region) in an N-channel MOSFET that minimizes the channel resistance (R_{ch}) and achieves a target avalanche breakdown voltage strength, the breakdown voltage capability could nonetheless be degraded due to the phenomena of punch-through of the body region between the drain and the source.

64. This punch-through could come from the presence of a resistive contact of the body region to the source region. Any current that is generated from the reverse biased P-N junction (the junction between drift region and the body region) can trigger the lowering of the barrier between the drain and source of the transistor in the off-state, and causes premature breakdown or conduction of the device even before the target avalanche breakdown voltage is reached. The punch through phenomena connected with a DMOSFET doping profile is commonly described as the action of the “parasitic bipolar transistor” formed from the n-p-n configuration of nearby doped

layers. The punch-through is often viewed as the unwanted biasing of the base of the parasitic bipolar transistor, allowing “breakdown” current to flow between collector and emitter.

65. Thus, while most of the work in the field at this time focused on optimizing the doping profiles of the body region and the drift region, a significant portion of these efforts also focused on the doping profile around the source/body contact in order to generate a low resistive ohmic contact to connect both the N⁺ source and the P- body of the transistor.

66. With the further evolution of using a trenched source contact to contact both the source region and the P body region, the doping profiles of the body surrounding both the sides and the bottom of the trench have significant impact on the resistance of the ohmic contacts required to connect both the source and the body.

IX. SUMMARY OF OPINIONS

A. Summary of Invalidity Opinions for the '634 Patent

67. As I will further explain in detail, it is my opinion that claims 1-9 of the '634 Patent are invalid based on the grounds and prior art references identified below.

GROUND	Prior References	Basis (35 U.S.C.)	Invalid Claims
1	Hirler	§ 102(b)	1, 2, 6
2	Hirler and Kobayashi 174	§ 103	3-5, 7-9
3	Shiraishi	§ 102(b)	1, 2
4	Shiraishi and Kobayashi 174	§ 103	3-9
5	Kobayashi 174 and Shiraishi	§ 103	1-9
6	Hshieh 384	§ 102(b)	1-9
7	Hshieh 384 and Hirler	§ 103	2-9
8	Takemori	§ 102(b)	1
9	Takemori, Hirler, and Hshieh 384	§ 103	2-9

B. Summary of Invalidity Opinions for the '409 Patent

68. As I will further explain in detail, it is my opinion that claims 1 of the '409 Patent is invalid based on the grounds and prior art references identified below.

GROUND	References	Basis (35 U.S.C.)	Invalid Claim
1	Kobayashi 196	§ 102	1
2	Kobayashi 196 and Hshieh 914	§ 103	1
3	Kobayashi 196 and Hueting	§ 103	1
4	Hueting and Deboy	§ 103	1

C. Summary of Invalidity Opinions for the '346 Patent

69. As further explained in detail below, it is my opinion that claims 1-7 and 16-20 of the '346 Patent are invalid based on the grounds and prior art references identified below.

GROUND	References	Basis (35 U.S.C.)	Invalid Claims
1	Kobayashi 174, Zhang, Hshieh 382, Weidman, and Takemori	§ 103	1-7, 16-20
2	Kobayashi 174, Himelick, EESEMI, Hshieh 382, Weidman, and Takemori	§ 103	1-7, 16-20
3	Takemori, Zhang, Hshieh 382, Weidman, and Kobayashi 174	§ 103	1-7, 16-20
4	Uno, Himelick, Zhang/EESEMI, Hshieh 382, Weidman, Kobayashi 174, and Takemori	§ 103	1-7, 16-20

D. Summary of Invalidity Opinions Under 35 U.S.C. § 112

70. As I will further explain in detail, it is my opinion that the Asserted Claims in the Asserted Patents are invalid under 35 U.S.C. § 112 for lack of enablement and/or for lack of written description.

E. Summary of Opinions Relating to Inequitable Conduct

71. As I will further explain in detail, it is my opinion that the '634 Patent and the '409 Patent are unenforceable certain prior art references were not disclosed to the USPTO during prosecution. It is further my opinion that had these references been disclosed, they would have been material to the issue of patentability of the applications giving rise to the '634 Patent and the '409 Patent.

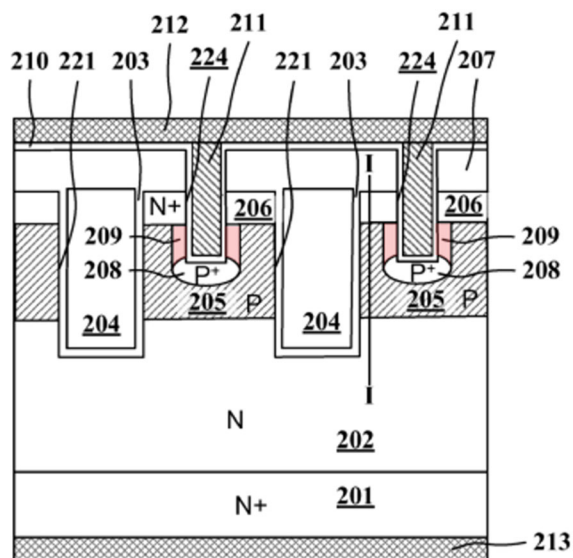
X. THE ASSERTED CLAIMS OF THE '634 PATENT ARE ANTICIPATED OR RENDERED OBVIOUS

A. Overview of the '634 Patent

72. The '634 Patent is directed to a trench Metal-Oxide-Semiconductor Field Effect Transistor ("MOSFET"), a type of semiconductor structure that is used to significantly reduce the surface area occupied by the channel of the transistor on the silicon, which in turn reduces the on-resistance of the device for a given device area. This type of semiconductor structure was well-known in the art and to the POSITA at the time of the filing date of the '634 Patent (February 23, 2008). Ex. C, '634 Patent at 1:5-9.

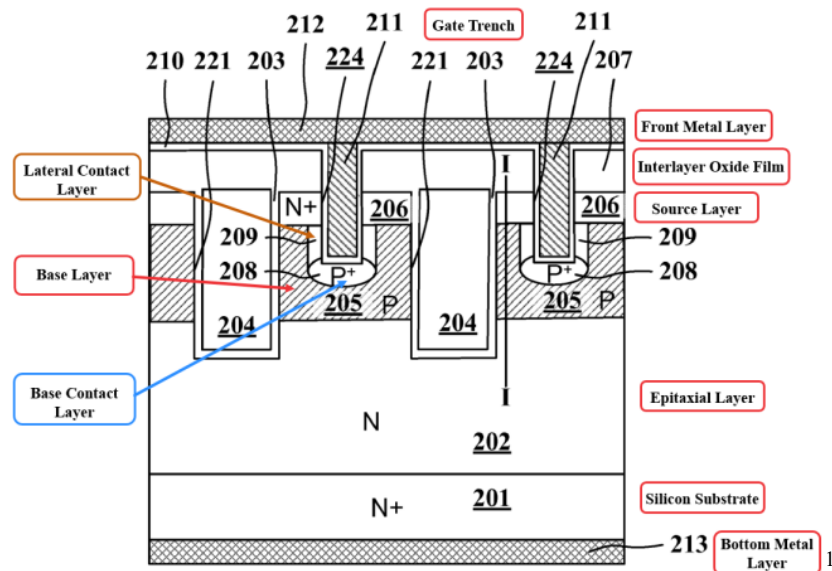
73. The '634 Patent addresses the issue of poor ohmic contact on the sidewall of the trench source contact to the body region due to a poorly engineered doping concentration profile. *Id.* at 1:35-45.

74. The '634 Patent, in particular, is directed to "a lateral contact layer" along the sidewalls within the base layer (205) of the source contact trenches. *Id.* at 1:5-9, 1:66-67, 2:23-26, 3:50-4:6, Fig. 2G. The lateral contact layer described in the '634 Patent is shown below in Figure 2G as 209. *Id.* at Fig. 2G, 3:50-4:6.



'634 Patent, Figure 2G (annotation added)

75. The '634 Patent describes the lateral contact layer (209) as being doped to P*-type, the base contact layer (208) at the bottom of the source contact trench is P⁺-type, and the body of the MOSFET (205) is P-type. *Id.* at 3:50- 56, 3:65-4:6, 5:9-15. Doping concentration P* is doped more heavily than P but less than P⁺. *Id.*



'634 Patent, Figure 2G (annotation added)

76. The '634 Patent also discloses that a trenched MOSFET with near-identical structure already existed in the prior art as of the effective filing date, including the claimed drain region, body region, source region, front metal layer, interlayer oxide film, bottom metal layer, trenched gates formed on top of the source layer and extending down through the base layer to a portion of the epitaxial layer, and source contact trenches formed on top of the source layer and extending down through the source layer to a portion of the base layer with a heavily doped base layer at the bottom of the trench. *Id.* at 1:5-9, 1:18-41, Fig. 1 (Prior Art). Figure 1 depicting the prior art as admitted by the '634 Patent is shown below.

¹ The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the '634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

C. The Asserted Claims

78. My understanding is that Force MOS has asserted Claims 1-9. I have reproduced independent Claim 1 below.

Claim 1:

[1.pre] A trench MOSFET with a trench source contact, comprising:

[1.a] a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;

[1.b] a front metal layer formed on the upper surface of said semiconductor region;

[1.c] an interlayer oxide film formed between said source layer and said front metal layer,

[1.d] a bottom metal layer formed on the lower surface of said semiconductor region;

[1.e] a plurality of trench gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and

[1.f] a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer; wherein the *sidewalls of said trenches in said base layer* are covered by the lateral contact layer; wherein the bottom base of said trenches in said base layer are covered by the base contact layer.

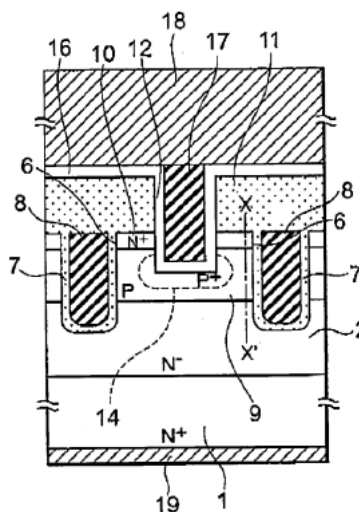
D. Priority Date of the '634 Patent

79. I understand that Force MOS claims the earliest priority date for the '634 Patent is February 23, 2008, the filing date of U.S. Patent Application Serial No. 12/036,243.

83. Additionally, Hirler discloses information surrounding the body amplification zone's allowance of "avalanche breakdown [to] be clamped between the transistor structures to achieve high dielectric strength while saving space without precisely defining the depth of the body contact zone. *Id.* at [0007-0008]. This disclosure alone is sufficient to inform a POSITA of the benefits inherent in forming a lateral contact layer along the sidewalls of the source contact trench – it would assist in achieving the designed avalanche breakdown target. Hirler also discusses how conductivity types can be reversed from n-type to p-type, which allows for the creation of complementary devices. This allows for the creation of N-channel and P-channel MOSFETs. *Id.* at [0001], [0005], [0028].

2. U.S. Patent Publication No. 2004/0021174 ("Kobayashi 174")

84. U.S. Patent Publication No. 2004/0021174 ("Kobayashi 174") was originally published on February 5, 2004. Because it was publicly available more than one year prior to the priority date of the '634 Patent, Kobayashi 174 is prior art at least under pre-AIA 35 U.S.C. §102(b). Ex. J, Kobayashi 174 at Cover. Kobayashi 174 was already considered during prosecution of the '634 patent, but it should be reconsidered here. Figure 5A from Kobayashi 174 is included for reference below:



Kobayashi 174, Figure 5A

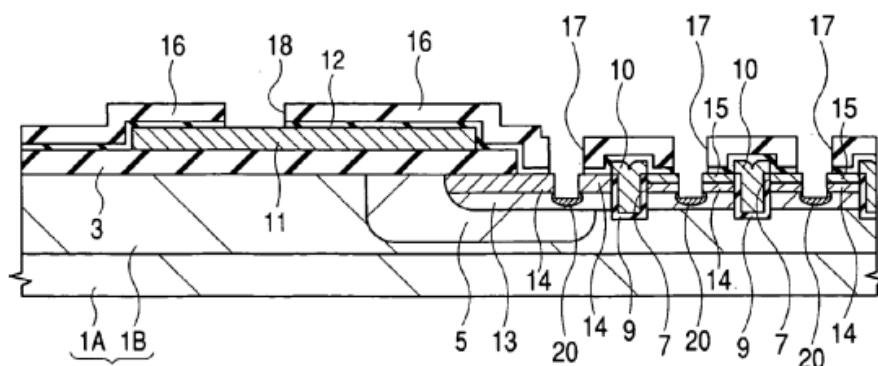
85. Similar to the '634 patent, the Kobayashi 174 prior art describes the tailoring of the depth of the trenched source contact, which is in contact with the base contact layer, with respect to the maximum base doping layer concentration profile. This tailoring is performed in view of the base doping concentration profile at both the sidewalls and the bottom of the trenched source contact. Kobayashi 174 discloses a trenched vertical MOSFET with the source contact trenches penetrating all the way to the base layer of the MOSFET. There is a p^+ -type base contact layer at the bottom of the trench. *Id.* at Cover, Fig. 10, [0018], [0052].

86. Kobayashi 174 discloses “an N^+ -type silicon substrate 1 and an N -type epitaxial layer 2 formed on one surface of the N^+ -type silicon substrate 1. A P-type base layer 9 and an N^+ -type source layer 10 are formed on a surface of the N -type epitaxial layer 2. . . . In each of trenches 6 reaching the N -type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled. On the polysilicon 8 to serve as a gate electrode or a trench gate, an interlayer oxide film 11 is formed. Between the trench gates adjacent to each other, a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 though the N^+ -type source layer 10. Directly under the contact hole 12, a barrier metal 16 is deposited to extend onto the interlayer oxide film 11. The contact hole 12, within which the barrier metal 16 is formed, is filled with W 17. On the surface of the W 17 and the barrier metal 16, a source electrode 18 is formed. On the other surface, of the N^+ -type silicon substrate 1, a drain electrode 19 is formed.” *Id.* at [0052].

87. Additionally, Kobayashi 174 also discloses “a base contact layer 14 under the bottom of the contact hole 12.” *Id.* at Fig. 5A, [0061], Claim 1 (“ . . . a base contact layer 14 formed within said base layer so as to enclose a bottom of said contact and to bring said base contact layer into contact with the bottom of said contact.”), Claim 3 (“ . . . said base contact layer is formed

3. U.S. Patent Publication No. 2005/0029584 (“Shiraishi”)

88. U.S. Patent Publication No. 2005/0029584 (“Shiraishi”) was originally published on February 10, 2005. Ex. K, Shiraishi at Cover. Because it was publicly available more than one year before the ’634 Patent’s priority date, it is prior art at least under pre-AIA 35 U.S.C. § 102(b). Figure 8 from Shiraishi is included below for reference:

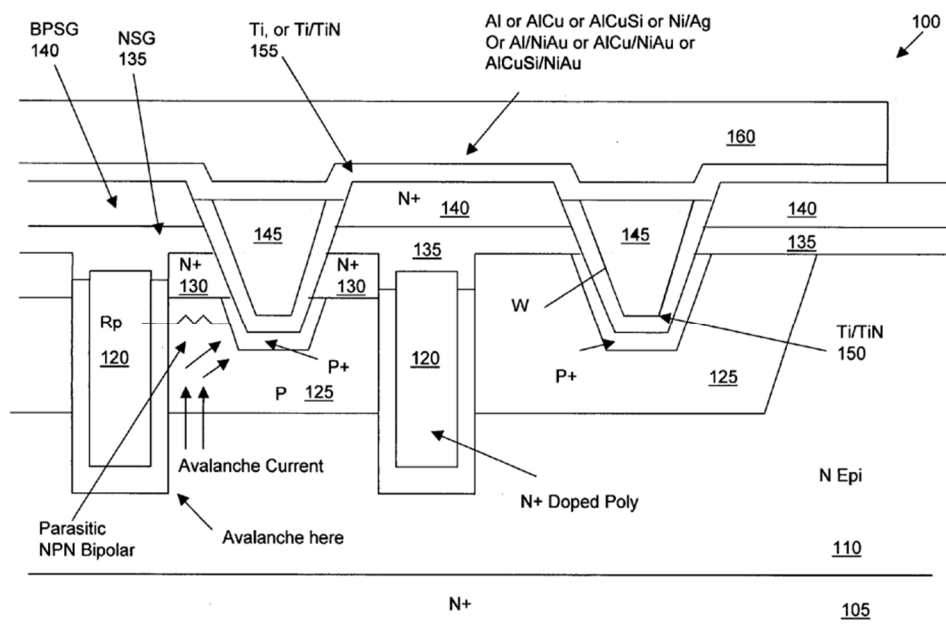


89. Similar to the '634 patent, Shiraishi generally discloses tailoring the doping profile in the base region of the Vertical Power MOSFET, which impacts the doping profile at the sidewalls of the source contact trenches. Shiraishi describes, in particular, a power Metal Insulator Semiconductor Field Effect Transistor ("MISFET") with source contact trenches with a p⁺-type base contact layer 20 located at the bottom of the trench. *Id.* at Abstract, Fig. 8, [0075]. Shiraishi also describes an additional p-type semiconductor layer 14 below the source layer and along the sidewalls of the source contact trench, which can be doped such that the impurity concentration is less than that of the p⁺ base contact layer 20 but higher than the p-type body layer. *Id.* at Fig. 8, [0073], [0075], [0084].

90. Shiraishi also generally describes the p-type semiconductor layer 14 as a “punch-through stopper layer” for the power MISFET. *Id.* at [0073], [0080], [0085]. The additional p-type semiconductor layer 14 allows for reduction of base resistance of a parasitic npn bipolar transistor and for enhancement of avalanche yield strength. *Id.* at [0084].

4. U.S. Patent Publication No. 2006/0273384 (“Hshieh 384”)

91. U.S. Patent Publication No. 2006/0273384 (“Hshieh 384”) was originally published on December 7, 2006. Ex. X, Hshieh 384 at Cover. Because it was publicly available more than one year before the ’634 Patent’s priority date, it is prior art at least under pre-AIA 35 U.S.C. § 102(b). Figure 3 from Hshieh 384 is included below for reference:



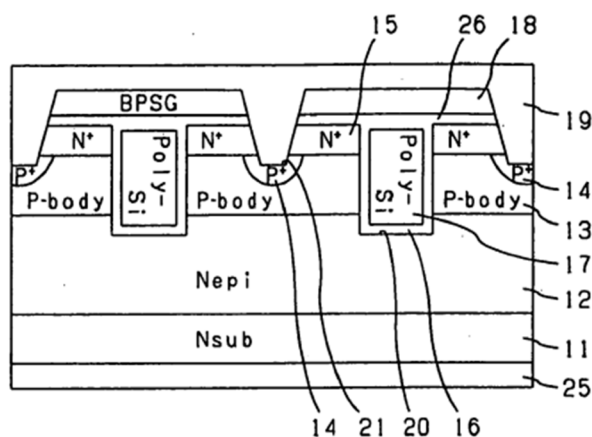
Hshieh 384, Figure 3

92. Similar to the ’634 patent, Hshieh 384 generally discloses a trenched metal oxide semiconductor field effect (“MOSFET”) transistor cell. The MOSFET of Hshieh 384 includes a source-body contact trench with substantially vertical sidewalls. Further, a body-resistance reduction region is “formed to surround the source-body contact trench to reduce a body-region resistance between the source-body contact metal and the trenched gate to improve an avalanche

capability.” *Id.* at Abstract. Hshieh 384 teaches that “[t]he P⁺ doped region 128 is formed to enhance avalanche current before triggering parasitic N+PN bipolar, i.e., the N⁺ source 130 with a P-body 125 and the N-epitaxial layer 110.” *Id.* at [0028]. The source-body contact trench is further surrounded by a barrier layer and may be opened with a slope. *Id.*

5. U.S. Patent No. 7,102,182 (“Takemori”)

93. U.S. Patent No. 7,102,182 (“Takemori”), was filed on November 27, 2002, published on September 2, 2004, and issued on September 5, 2006. Because it was publicly available more than one year before the ’634 Patent’s priority date, it is prior art to the ’634 Patent at least under 35 U.S.C. § 102(b). Figure 3 from Takemori is included below for reference:

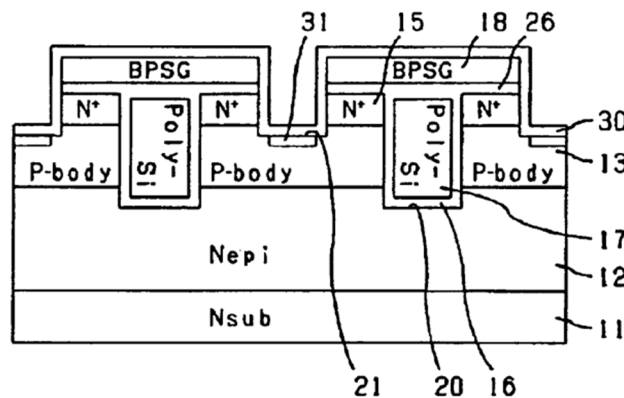


Takemori, Figure 3

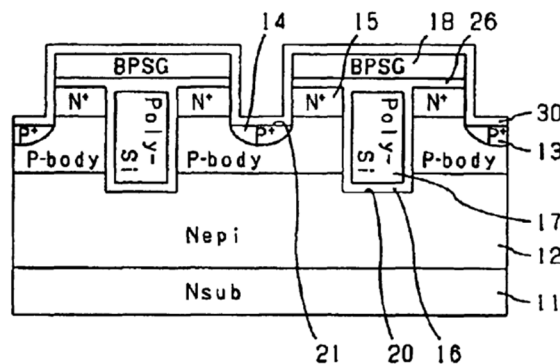
94. Takemori teaches a trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. *See* Ex. V, Takemori.

95. As shown in Figure 3 above, Takemori further discloses source trenches that are “formed so as to reach to a comparatively shallow site of P-type body layer 13.” *Id.* at 15:62-63. “In addition, buried P⁺-type diffusion region 14 is formed so as to be exposed on the bottom surface

of source trench 21.” *Id.* at 15:64-66. Furthermore, as illustrated in Figures 14 and 15 below, “boron ions (B^+) are injected into the bottom surface of source trench 21. Next, the boron ions are diffused by heating boron ion injection section 31 to form buried P^+ -type diffusion region 14 as shown in FIG. 15.”

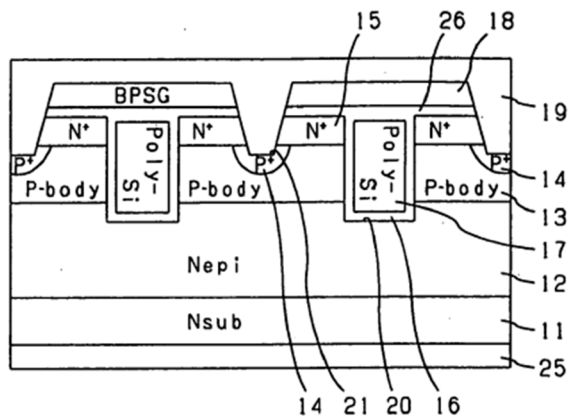


Takemori, Figure 14

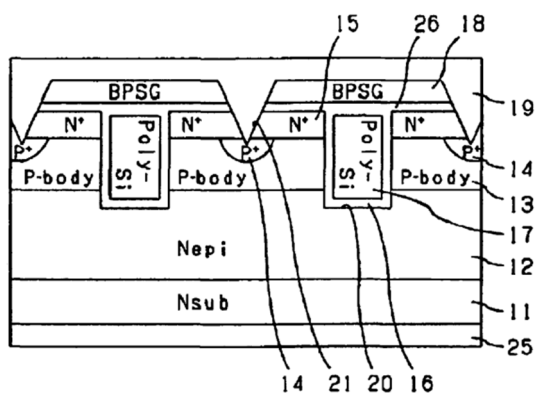


Takemori, Figure 15

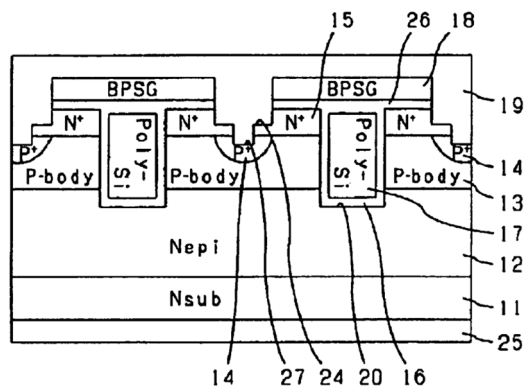
96. Moreover, Takemori teaches various source trenches. Figures 3-6 from Takemori are included below for reference. As shown below, in each embodiment, the buried P^+ -type diffusion region 14 covers the bottom the source trench and the sidewalls of the source trench within the body region.



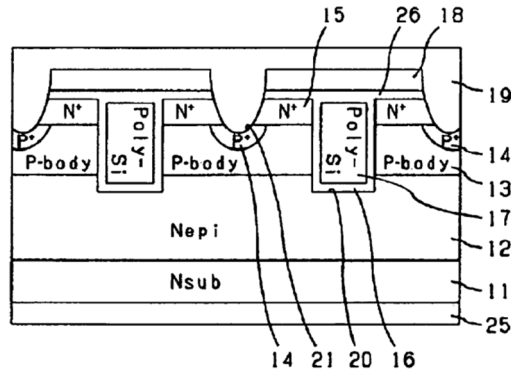
Takemori, Figure 3



Takemori, Figure 4



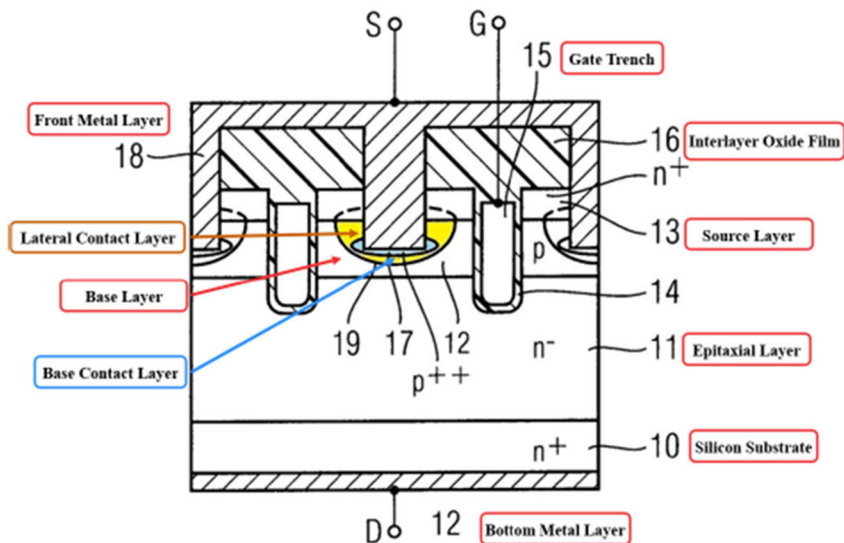
Takemori, Figure 5



Takemori, Figure 6

F. Claims 1-2, and 6 of the '634 Patent Are Unpatentable as Anticipated by Hirler

97. I contend that, under the legal principles described herein, Claims 1-2, and 6 of the '634 Patent are unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated entirely by Hirler. Hirler discloses and anticipates every single limitation of Claim 1, all of which are specifically disclosed in Figure 2F of the same, which is annotated below for reference.



Hirler, Figure 2F (annotated)

1. Claim 1

a) [1.pre]. “A trenched MOSFET with trenched source contact, comprising:”

² The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the '634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

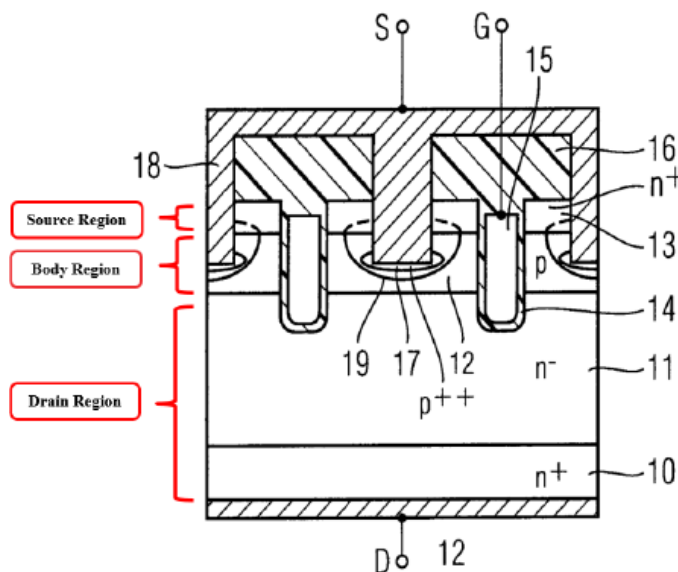
98. The preamble of Claim 1, which may be limiting, is disclosed in Hirler, as Hirler describes a trenched MOSFET with source code trenches: “The present invention relates to a MOS power transistor arrangement having a vertical transistor structure . . . wherein the body zone has a contact zone at the base of a contact trench.” Ex. I, Hirler at Fig. 2F, [0001], Abstract. A POSITA would understand that the “contact trench” described above specifically means a source contact trench since the trench must extend through the source region and into the body region, which is clearly seen to occur in Figure 2F.

b) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, [1] a silicon substrate, [2] an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, [3] a base layer corresponding to said body region disposed on the top of said epitaxial layer, and [4] a source layer corresponding to said source region disposed on the top of said base layer;”

99. This element of Claim 1 is similarly disclosed in Hirler, which describes a vertical trenched MOSFET with a drain region, body region, and a source regions, all of which are features that any POSITA would have understood as necessary for the operation of all MOSFETs. *Id.* at Fig. 2F, [0001].

100. Specifically, Hirler discloses “The starting point is an n+ substrate 10 of silicon, an n- drift zone 11, p-body zone areas 12 as well as n+ source zone areas 13.” *Id.* at [0018], [0001], Fig. 1A, Fig. 2F. A POSITA would have understood that Figure 2F (which is re-illustrated with different annotations below), illustrates a MOSFET with a drain region forming the bottom portion of the MOSFET, and layered as is described in the claim language: wherein (1) the “n+ substrate 10 of silicon” corresponds with “a silicon substrate,” (2) the “n- drift zone 11” corresponds with “an epitaxial layer corresponding with a drain region,” (3) the “p-body zone areas 12” corresponds with “a base layer corresponding to a said body region,” and (4) “n+ source zone areas 13”

corresponds with “a source layer corresponding to said source region” as provided in Claim 1 of the ’634 Patent. *Id.* at [0018], Fig. 1A, Fig. 2F.



Hirler, Figure 2F (annotation added)

3

c) [1.b]. “a front metal layer formed on the upper surface of said semiconductor region”

101. Hirler discloses a metal layer (18), positioned on the upper surface of the MOSFET, to form a source connection. “The metallization 18 forms a source connection S.” *Id.* at Fig. 2F, [0022]. This feature was also well-known in the art and would have been familiar to any POSITA.

d) [1.c]. “an interlayer oxide film formed between said source layer and said front metal layer”

102. Hirler discloses a silicon oxide layer (16) formed between the source layer (13) and the metal layer (18). *Id.* at Fig. 2F, Fig. 1A, [0018] (“The silicon oxide layer 16 covers the entire structure”). A POSITA would have understood that the “silicon oxide layer 16” corresponds to an interlayer oxide film. This was a feature well-known in the art.

³ The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the ’634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

e) [1.d]. “a bottom metal layer formed on the lower surface of said semiconductor region;”

103. Hirler discloses a metal layer (12) that is positioned on the bottom surface of the MOSFET to form a drain connection, an example of which is marked as “D” in Figure 2F. *Id.* at Fig. 2F, [0022] (“an unspecified metallization of, for example, aluminum is applied, which forms a drain connection D.”). This feature was well-known in the art and would have been understood by a POSITA.⁴

f) [1.e]. “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”

104. The broader construction of this term would instruct that trenched gates are formed from the top of source layer and extend down through the base layer. In this construction, the gates need not come from above the source layer. Hirler describes a plurality of gate trenches (14, 15), annotated as “G”, which are covered by the silicon oxide layer, extend from the top of the source layer, and extend down through the body layer and into the epitaxial, drift layer, a feature which would be commonly understood by a POSITA. *Id.* at Fig. 2F, [0018] (“The trench gates with a gate oxide 14 and a gate electrode 15 extend through the source zone areas 13 and the body zone 12 into the drift zone 11.”).

105. Even if the more narrow construction is applied, where the gates must extend from above the source layer, this element is still disclosed in Hirler. Hirler describes a plurality of gate trenches (14, 15), referred to as “G”, covered by the silicon oxide layer, beginning above the source layer, and extending down through the body layer and into the epitaxial, drift layer, a feature which would have been commonly understood by a POSITA. *Id.* at Fig. 2F, [0018] (“The trench gates

⁴ As a point of clarification: The bottom metal layer in Figure 2F is mislabeled. Both the body region and the bottom metal layer are labeled as (12) in Figure 2F. However, a POSITA would have understood from the description and from Figure 1A that (12) refers to the body region, which would not be located at the drain connection.

with a gate oxide 14 and a gate electrode 15 extend through the source zone areas 13 and the body zone 12 into the drift zone 11.”)

g) [1.f]. “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”

106. Hirler generally describes a plurality of source contact trenches that are formed on top of the silicon oxide layer and which further “penetrat[e] through the source zones areas 13 to the body zone areas 12” *Id.* at [0020], [0019], Fig. 2F. Similar to the above, this is something that would be commonly understood by a POSITA.

h) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer”

107. The broader construction of this term would instruct that only a portion of the sidewalls need be covered by the lateral contact layer. Hirler discloses this element as well. Hirler describes “body amplification zones” (19), which are implanted along at least a portion of the sidewalls of the contact trench in the base layer. *Id.* at Fig. 2F, [0030], [0033]. A POSITA would have understood that the “body modification zone” or “body enhancement zone” as it is disclosed in Hirler, is the same as the “lateral contact layer” that is referenced in the ‘634 Patent. This is clear, not only because the body amplification zone is located in the same position along the sidewalls of the contact trench, but the purpose of the body amplification zone is also the same as the lateral contact layer — i.e., to achieve the intended avalanche breakdown voltage capability, without such being degraded due to the turning on the of NPN parasitic bipolar transistor. Ex. I, Hirler at [0007]-[0008]; Ex. C, ’634 Patent at 1:35-42, 2:23-33.

108. Even if the more narrow construction is applied, where the entire sidewall must be covered by the lateral contact layer, this element is still disclosed by Hirler. Hirler describes “body amplification zones” (19), which are implanted along the entirety of the sidewalls of the contact

trench in the base layer. Ex. I, Hirler at Fig. 2F, [0030], [0033]. A POSITA would have understood that the “body modification zone” or “body enhancement zone” as it is disclosed in Hirler is the same as the “lateral contact layer” that is referenced in the ’634 Patent. This is clear, not only because the body amplification zone is located in the same position along the sidewalls of the contact trench, but also since the purpose of the body amplification zone is also the same as the lateral contact layer — i.e., to achieve the intended avalanche breakdown voltage capability, without such being degraded due to the turning on the of NPN parasitic bipolar transistor. *Id.* at [0007]-[0008]; Ex. C, ’634 Patent at 1:35-42, 2:23-33.

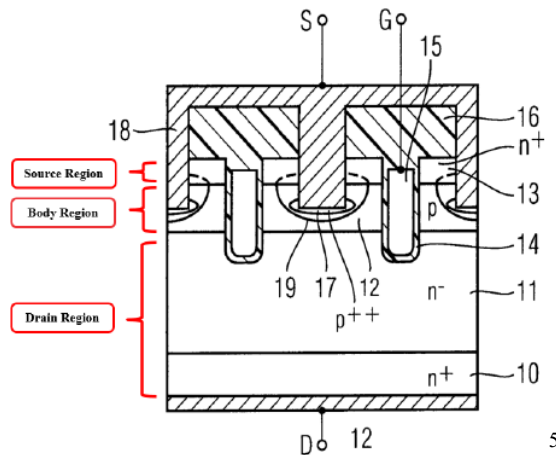
i) [1.h]. “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

109. Hirler discloses a P++ type “body contact zone 17” at the bottom of the contact trench. Ex. I, Hirler at Fig. 2F, Fig. 1D, [0021]. A POSITA would have understood that the “body contact zone” disclosed in Hirler is the same as the “base layer” that is described in the ’634 Patent.

2. Claim 2

a) [2.a]. “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

110. Claim 2 is dependent on Claim 1, so all of the present elements discussed above are similarly taught with regards to Claim 2 are taught by Hirler. However, Hirler also teaches the additional limitations introduced by Claim 2. As shown in Figure 2F, reproduced below, Hirler describes a trench MOSFET, wherein the conductivity type of the silicon substrate, the epitaxial layer, and the source layer are N-type. *Id.* at Fig. 2F, [0018]. These are features of an N-channel MOSFET, which were well-known in the field of art and therefore to the POSITA.



Hirler, Figure 2F (annotation added)

b) [2.b]. “the base layer and lateral contact layer are P-type;”

111. This element is similarly described in Hirler. As is shown in Figure 2F above, Hirler describes a trench MOSFET, wherein the conductivity type of the body layer is P-type. *Id.* In addition, Hirler discloses that the conductivity type of the body amplification layer (the lateral contact layer) is also p-type — i.e., p+. *Id.* at [0030].

c) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

112. As is shown in Figure 2F above, *supra* X.F.2(a), Hirler describes a trench MOSFET, wherein the body contact layer/base contact layer is P-type (p++). *Id.* at Fig. 2F, [0018]. In addition, Hirler discloses that the doping concentration of the body amplification zone is larger than the doping concentration of the body zone and smaller than the doping concentration of the body contact zone. *Id.* at [0009], [0031], Claim 2. The POSITA would have clearly understood, upon reviewing the ’634 Patent and its prior art, that this disclosure suggests that the layer at the bottom of the contact trench has a higher doping concentration of P-type than the layer at the sidewalls of the trench, which in turn has a higher doping concentration than the body region.

⁵ The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the ’634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

3. **Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.**

113. Claim 6 is dependent on Claim 1, so all of the present elements discussed above are similarly taught with regards to Claim 6 by Hirler. The additional elements are also disclosed by Hirler. Hirler introduces a MOSFET with layers of either N or P-type conductivity: “The present invention relates to a MOS power transistor arrangement having a vertical transistor structure in which a drift zone of the first conductivity type [e.g., P-type] and a body zone of a second conductivity type opposite to the first conductivity type [e.g., N-type] and a source zone of the first conductivity type [e.g., P-type] are successively provided on a semiconductor substrate of a first conductivity type [e.g., P-type], and in which a trench gate extends through the source zone and the body zone into the drift zone, wherein the body zone has a contact zone at the base of a contact trench with a high doping concentration compared with the doping concentration of the body zone [e.g., N-type].” *Id.* at [0001]. Based on this, the POSITA would have understood that the conductivity type options were limited to P-type and N-type and see that Hirler has disclosed a trench MOSFET, whether the first conductivity type is P-type or N-type.

114. Additionally, Hirler specifically describes an embodiment in the prior art where “a trench MOS power transistor in which a p-type layer [sic], an n⁺ type body amplification zone [i.e., lateral contact layer], an n-type body region and an n⁺⁺ type body contact zone [i.e., base contact layer] are provided on the edge of a gate trench, one above the other from the base of the trench.” *Id.* at [0005]. The POSITA would have understood this to disclose a P-channel MOSFET, where the source and drain regions would be P-type and where the body region would be N-type. Further, it would have been clear to a POSITA that a MOSFET with an N-type first conductivity

must correspond to an N-channel MOSFET, while a MOSFET with a P-type first conductivity must correspond to a P-channel MOSFET.

G. Claims 3-5 and 7-9 Are Unpatentable as Obvious over Hirler in View of Kobayashi 174

1. Motivation to Combine

115. I contend that it would have been obvious to a POSITA, prior to the effective filing date of the '634 Patent (February 23, 2008), to combine Hirler and Kobayashi 174 in such a way that one would arrive at the subject matter of Claims 3-5 and 7-9, rendering those claims invalid under pre-AIA 35 U.S.C. § 103.

116. Specifically, a POSITA would have been motivated to combine the barrier metal layer technology of Kobayashi 174 with the MOSFET described in Hirler, obtaining a reasonable likelihood of success that they arrive at the subject matter described in Claims 3-5 and Claims 7-9. Further, a POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi 174 with the MOSFET disclosed in Hirler. The use of a barrier metal layer (in particular made of materials such as Ti and TiN) to encourage adhesion of the tungsten contact plug to the contact area of the source contact trenches, is a well-known concept in the art and therefore to the POSITA. Furthermore, the deposition of TiN and Ti was known to provide uniform sidewall (step) coverage within the source, resulting in uniform thickness coverage of the n⁺, p and p⁺ regions of the source contact hole. Uniform thickness insures that the contact resistance between the n⁺ and the p-regions is minimized, avoiding any voltage drop that could trigger the parasitic bipolar transistor inherent in the MOSFET design.

117. Hirler, Kobayashi 174, and the '634 Patent are all analogous pieces of art that seek to solve similar design problems. Hirler, Kobayashi 174, and the '634 Patent are in the same field of endeavor, i.e., Vertical Power MOSFET structures. All are based in the same methods to

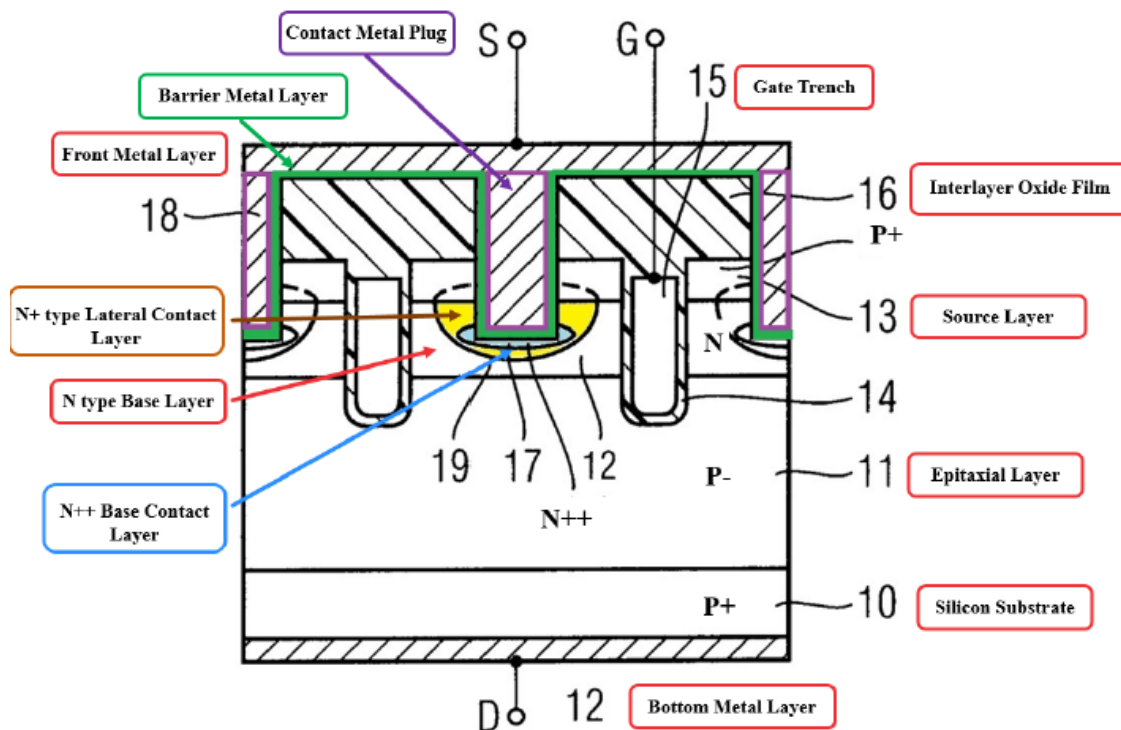
improve the performance tradeoff in the on-state (on-resistance and speed) and off-state (breakdown voltage). Hirler, Kobayashi 174, and the '634 Patent all disclose a similar doping technique, i.e., dopant ion implantation, which allows for formation of a low resistance source contact, located at the bottom of the base region and/or on the sidewall of the trenched contact region, either of which with minimal impact to the threshold voltage or the on-resistance of the power MOSFET.

118. Further, a POSITA would have been motivated to combine the barrier metal layer disclosed in Kobayashi 174 with the MOSFET disclosed in Hirler. A POSITA would have known that the use of a barrier metal layer (in particular made of materials such as Ti and TiN) would encourage adhesion of the tungsten contact plug to the contact area of the source contact trenches. A Ti and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition process of W, from seeping into the underlying silicon surface, which degrades the performance of the transistor.

119. The use of a tungsten contact plug alongside a barrier metal layer, to fill contact holes or trench with high aspect ratio, is well known to a POSITA. When manufacture of MOSFETs scale to smaller dimension, there is an increased need for an interconnect process with good planarization. One must fill contact holes that have high aspect ratio, like a trench, and achieve smooth top planar surface. This is achieved by the use of chemical vapor deposition ("CVD") of tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio and produces a planar top surface after the CVD tungsten is etched back. It also would have been obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the use of a barrier metal layer. The barrier metal layer will act as a diffusion barrier - preventing

unwanted interactions between the CVD W and the silicon. A POSITA would have found it obvious to use Ti/TiN, as the common barrier metal layer material is Ti/TiN layer.

120. Therefore, the combination of Hirler and Kobayashi 174 renders obvious Claims 3-5 and 7-9, as illustrated below in a hypothetical diagram, based on Hirler's Figure 2, that demonstrates how the barrier metal layer from Kobayashi 174 might be added to the contact metal from Hirler, depicted as both n-channel and p-channel MOSFETs.



Hirler, Figure 2F (annotated)

2. Claim 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

121. All of the elements of Claim 3 are disclosed via Hirler and Kobayashi 174, and would have been combined based on knowledge of the POSITA. Claim 3 is dependent on Claim 2, the elements of which are disclosed by Hirler as discussed above. Additionally, Hirler discloses

⁶ The annotations on these figure were originally used to support the Petition for *Inter Partes* Review of the ‘634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

that the source contact trench can be “filled with a conductive stopper” - i.e. contact metal plugs, while Kobayashi 174 discloses the use of a barrier metal layer. Ex. I, Hirler, at [0023]; Ex. J, Kobayashi 174 at Fig. 5A, [0052]-[0053], [0062]. Use of barrier metal layers is something generally known to a POSITA, as is the fact that a deposition of CVD Tungsten is typically preceded by such usage of a barrier metal layer. The barrier metal layer acts as a diffusion barrier – preventing any unwanted interactions between the CVD W and underlying silicon.

3. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

122. All of the elements of Claim 4 are disclosed via Hirler and Kobayashi 174, and would have been combined based on knowledge of the POSITA. Claim 4 is dependent on Claim 3, the elements of which are disclosed by Hirler and Kobayashi 174 as discussed above. In addition to this, Hirler discloses that the source contact trench can be “filled with a conductive stopper made of, for example, polycrystalline silicon or tungsten,” while Kobayashi 174 discloses the use of a barrier metal layer that is made of Ti and TiN. Ex. I, Hirler, at [0023]; Ex. J, Kobayashi 174 at [0062]. A POSITA would have understood that the common barrier metal layer material would be comprised of Ti/TiN.

4. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

123. All of the elements of Claim 5 are disclosed via Hirler and Kobayashi 174 and would have been combined based on knowledge of the POSITA. Claim 5 is dependent on Claim 4, the elements of which are disclosed by Hirler and Kobayashi 174 as discussed above. Additionally, Hirler discloses a trench MOSFET with a vertical source contact trench. Ex. I, Hirler at Fig. 2F. A POSITA would have been aware that the shape of a trench is governed by the etching chemistry being used. A source contact trench can be selected to be of a vertical or tapered

design, based on this chemistry. Similarly, the gate trench can be selected from these two shapes, with the tapered shape commonly referred to as VMOS, and the vertical referred to as U MOS.

5. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

124. All of the elements of Claim 7 are disclosed via Hirler and Kobayashi 174, and would have been combined based on knowledge of the POSITA. Claim 7 is dependent on Claim 6, the elements of which are disclosed by Hirler as discussed above. Based on the basics of the science underlying MOSFET technology, a POSITA would have understood that inverting the conductivity types allows for the formation of either an N-channel MOSFET or a P-channel MOSFET. The inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including the use of the same conductive material for the barrier metal layer and the contact metal plugs.

6. Claim 8: The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

125. All of the elements of Claim 8 are disclosed via Hirler and Kobayashi 174, and would have been combined based on knowledge of the POSITA. Claim 8 is dependent on Claim 7, the elements of which would have been understood by a POSITA, as discussed above. Any POSITA would have understood that the inversion of conductivity types would not affect the previous disclosure and analysis.

7. Claim 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”

126. All of the elements of Claim 9 are disclosed via Hirler and Kobayashi 174, and would have been combined based on knowledge of the POSITA. Claim 9 is dependent on Claim

8, the elements of which would be commonly understood by a POSITA, as discussed above. Any POSITA would have understood that the inversion of conductivity types would not affect the previous disclosure and analysis.

H. Claims 1 and 2 Are Unpatentable as Anticipated by Shiraishi

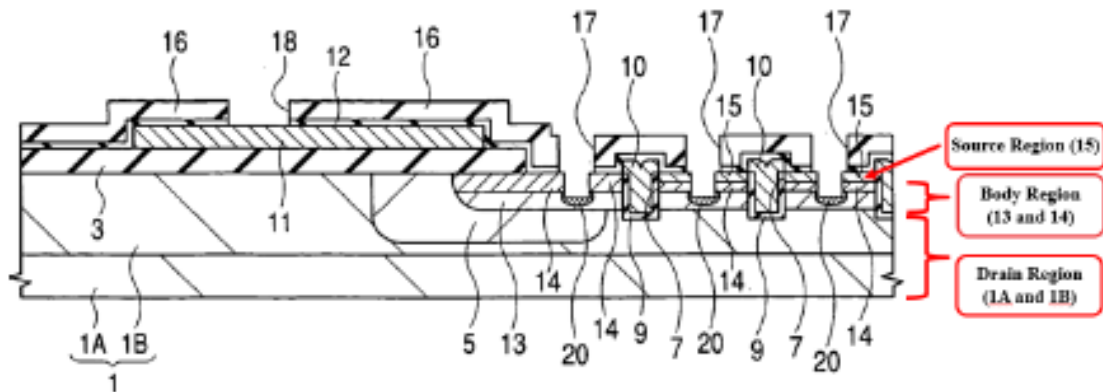
1. Claim 1

a) [1.pre]. “A **trenched MOSFET with trenched source contact, comprising:**”

127. To the extent the preamble is limiting, it is disclosed in Shiraishi, as it describes a trenched MISFET with source contact trenches. Ex. K, Shiraishi at [0005], [0074], Fig. 8. A POSITA would have known that a MISFET is interchangeable with the term MOSFET. In fact, a MOSFET (Metal-Oxide-Semiconductor FET) is a specific type of MISFET (Metal-Insulator-Semiconductor FET) wherein the insulator is an oxide.

b) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

128. Claim 1.a is also shown via Shiraishi’s Figure 8 (copied below with color annotations), the disclosed MISFET has a drain region, a body region, and a source region. *Id.* at Fig. 8, Fig. 35, [0012], [0067], [0072], [00073]. Moreover, the drain region is oriented at the bottom of the figure with a silicon substrate (1A), an epitaxial layer (1B), a body layer (13), and a source layer (15) layered on top. *Id.* at Fig. 8, Fig. 35, [0067], Claim 22.



Shiraishi, Figure 8 (annotated in regards to Claim element 1.a)

129. Shiraishi discloses that “[t]he n+type single crystal silicon substrate 1A and the n-type single crystal silicon layer 1B [i.e., epitaxial layer] may serve as a drain region for the respective power MISFETs.” *Id.* at [0067], Claim 22. A POSITA would have understood that the silicon substrate (1A) corresponds to a silicon substrate, and would have understood the silicon layer (1B) corresponds to a epitaxial layer.

130. Shiraishi also discusses that “the p-type semiconductor region 13 [i.e., base layer] may serve as a channel layer for the respective power MISFETs.” *Id.* at [0072]. A POSITA would have understood that the channel layer (13) corresponds to a body region or base layer. Shiraishi also discloses that “the source region in the n+type semiconductor region 15.” *Id.* at [0073]. A POSITA would have understood that this region corresponds to a source region.

c) [1.b]. "a front metal layer formed on the upper surface of said semiconductor region"

131. Claim 1.b is disclosed in Shiraishi, wherein a source pad (22) is located on top of the source region. *Id.* at Fig. 9, [0077] (“a source pad (a first electrode) 22 electrically connected to the n+type semiconductor region 15 serving as the source region for the respective power MISFETS”). A POSITA would have understood that the disclosed electrode or “source pad”

⁷ The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the '634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

corresponds to, and is equivalent to, a front metal layer. This is a feature that would have been well-known in the art and well-known to the POSITA.

d) [1.c]. “an interlayer oxide film formed between said source layer and said front metal layer;”

132. Claim 1.c is disclosed in Shiraishi, as it describes where an insulating film (16 and 12) is formed between the source region (15) and the source electrode (22). *Id.* at Fig. 9, [0074]-[0075]. A POSITA would have understood that the “insulating film” between the source layer and the source pad corresponds to and is equivalent to an interlayer oxide film. This is a feature that would have been well-known in the art and well-known to the POSITA.

e) [1.d]. “a bottom metal layer formed on the lower surface of said semiconductor region;”

133. Claims 1.d is disclosed in Shiraishi, wherein an “electrically conductive film” may be deposited over the back surface of the silicon substrate (1A), which would then act as an extraction or drain electrode. *Id.* at [0097]. A POSITA would have understood that the “electrically conductive film” on the back surface of the silicon substrate forms a bottom metal layer. This is a feature that would have been well-known in the art and well-known to the POSITA.

f) [1.e]. “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”

134. The broader construction of this term would instruct that trenched gates are formed from the top of source layer and extend down through the base layer. In this construction, the gates need not come from above the source layer. As demonstrated in Figure 8, Shiraishi discloses a plurality of gate electrodes (10) that are covered by the insulating film (16 and 12) and extends downward through the source layer (15), the channel layer (13), and then into a portion of the epitaxial layer (1B). *Id.* at Fig. 8, [0070], [0074]. This is a feature that would have been well-known in the art and well-known to the POSITA.

135. Even if the more narrow construction is applied, where the gates must extend from above the source layer, this element is still disclosed in Shiraishi. As demonstrated in Figure 8, Shiraishi discloses a plurality of gate electrodes (10) that are covered by the insulating film (16 and 12) and extends downward through the source layer (15) (coming in from above the source layer), the channel layer (13), and then into a portion of the epitaxial layer (1B). *Id.* at Fig. 8, [0070], [0074]. This is a feature that would have been well-known in the art and well-known to the POSITA.

g) [1.f]. “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”

136. Claim 1.f is disclosed in Shiraishi. As shown in Figure 8, Shiraishi discloses source contact trenches (17) formed on top of the insulating film (16 and 12) that extend down through the N⁺-type source layer (15) to the P-type body region (13 and 14). *Id.* at Fig. 8, [0074]. A POSITA would have understood that the additional semiconductor layer (14) is a part of the body layer (13 and 14). *Id.* at [0073] (“the p-type semiconductor region 14 inside the p-type semiconductor region 13”), [0092] (“the p-type semiconductor region 14 may be implemented in the p-type semiconductor region 13”). The body layer is designated by the layers with opposite conductivity to the source and drain regions. This is a feature that would have been well-known in the art and well-known to the POSITA.

h) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

137. The broader construction of this term would instruct that only a portion of the sidewalls need be covered by the lateral contact layer. This is disclosed by Shiraishi. As demonstrated in Figure 8, Shiraishi describes an additional semiconductor layer (14) along at least a portion the sidewalls of the contact trench. *Id.* at Fig. 8; [0073], [0080], [0084]-[0085], [0092]

(“The localized formation of the p-type semiconductor region 14 may be implemented in the p-type semiconductor region 13, as discussed herein throughout [sic].”) . Shiraishi discloses, and a POSITA would have understood, that this region acts as a lateral contact layer to prevent any punch-through. *Id.* at [0073].

138. Even if the more narrow construction is applied, where the entire sidewall must be covered by the lateral contact layer, this element is still disclosed by Shiraishi. As demonstrated in Figure 8, Shiraishi describes an additional semiconductor layer (14) along the entirety of the sidewalls of the contact trench. *Id.* at Fig. 8; [0073], [0080], [0084]-[0085], [0092] (“The localized formation of the p-type semiconductor region 14 may be implemented in the p-type semiconductor region 13, as discussed herein throughout [sic].”) Shiraishi discloses, and a POSITA would have understood, that this region acts as a lateral contact layer to prevent any punch-through. *Id.* at [0073].

i) [1.h]. “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

139. Claim 1.h is disclosed in Shiraishi, in which the bottom of the contact trench is covered by a semiconductor region (20). *Id.* at Fig. 8, [0075] (“forming a p⁺type semiconductor region (a fourth semiconductor layer) 20 in such a way as to cover the respective bottom of the contact grooves 17.”). This is a feature that would have been well-known in the art and well-known to the POSITA.

2. Claim 2

a) [2.a]. “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

140. Claim 2 depends on Claim 1, which is fully disclosed in Shiraishi as discussed above. In addition, Claim 2.a is also disclosed in Shiraishi. Shiraishi describes a trench MISFET, wherein the silicon substrate, the epitaxial layer, and the source layer are all N-type. *Id.* at [0067],

[0073]. These are features of an N-channel MOSFET that were well-known in the art and to the POSITA.

b) [2.b]. “the base layer and lateral contact layer are P-type;”

141. Claim 2.b is disclosed in Shiraishi. In reference to regions shown in Figure 8, Shiraishi discusses a “p-type semiconductor region 14 [i.e., the lateral contact layer] inside the p-type semiconductor region 13.” *Id.* at Fig. 8, [0073]. These are features of an N-channel MOSFET that were well-known in the art and would have been well-known to the POSITA.

c) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

142. Claim 2.c is disclosed in Shiraishi, which discloses that “p-type semiconductor region 14 [i.e., lateral contact layer] may be locally higher in impurity concentration than the p-type semiconductor region 13.” *Id.* at Fig. 8, [0080]. Shiraishi additionally discloses that “[i]mpurity concentration in the p+type semiconductor region 20 [i.e., base contact layer] may be rendered higher than that in the p-type semiconductor region 14 [i.e., lateral contact layer].” *Id.* at Fig. 8, [0075]. A POSITA would have understood that Shiraishi here discloses a lateral contact layer of p-type conductivity - with a P-type doping concentration that is higher than the underlying base layer - but lower than the P-type doping concentration of the base contact layer.

I. Claims 3-9 Are Unpatentable as Obvious over Shiraishi in View of Kobayashi 174

1. Motivation to Combine

143. I contend that it would have been obvious to a POSITA, prior to the effective filing date of the '634 Patent (February 23, 2008), to combine Shiraishi and Kobayashi 174 in such a way that one would arrive at the subject matter of Claims 3-9, rendering those claims invalid under 35 U.S.C. § 103.

144. Specifically, a POSITA would have been motivated to combine the metal contact plug and the barrier metal layer from Kobayashi 174, with the MISFET of Shiraishi, obtaining a reasonable likelihood of success that they arrive at the subject matter of Claims 3-5. Additionally, a POSITA would have been motivated to combine Kobayashi 174 with Shiraishi in order to invert the P/N types of Shiraishi, which would teach the subject matter of Claims 6-9. P-channel and N-channel MOSFETs using inversion layers are well-known concepts in the art and therefore to the POSITA.

145. Shiraishi, Kobayashi 174, and the '634 Patent are all analogous art seeking to solve similar problems. Shiraishi, Kobayashi 174, and the '634 Patent are all in the same field of endeavor, i.e., Vertical Power MOSFET structures. All are based in the same methods to improve the performance tradeoff in the ON-state (ON-Resistance and speed) and OFF-state (breakdown voltage). Moreover, Shiraishi, Kobayashi 174, and the '634 Patent disclose a similar doping technique, i.e., dopant ion implantation, which allows for formation of a low resistance source contact, located at the bottom of the base region and/or on the sidewall of the trenched contact region, either of which with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

146. Additionally, Kobayashi 174 expressly teaches that the contact metal plug is beneficial because it “allows the resistance component of the source electrode 18 [to be] reduced” by creating a flat surface for the source electrode. Ex. J, Kobayashi 174 at [0066]; *id.* at Claim 4 (claiming use of a metal contact plug to provide a flattened surface and a source electrode deposited on said flattened surface). Kobayashi 174 further teaches the source electrode “having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.” *Id.* at [0066]. Lastly, “it is possible to

perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface.” *Id.* In particular, Kobayashi 174 teaches the use of tungsten metal contact plugs. The POSITA would therefore have been motivated to combine the metal contact plugs taught by Kobayashi 174 with the disclosures of Shiraishi.

147. The POSITA would also have been motivated to combine the barrier metal layer disclosed in Kobayashi 174 with the MISFET disclosed in Shiraishi. A POSITA would commonly know that the use of a barrier metal layer, made of materials such as Ti and TiN, would promote the adhesion of the tungsten contact plug from Kobayashi 174 to the contact area of the source contact trenches. The Ti and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition process of W, from seeping into the underlying silicon surface, which would degrade the performance of the transistor.

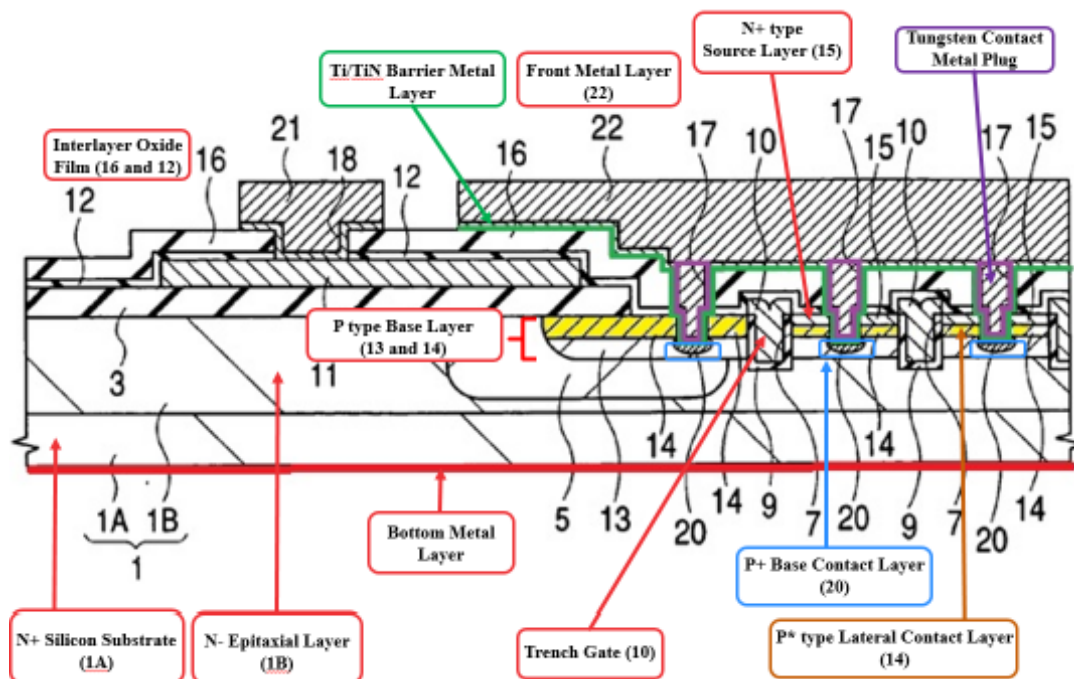
148. Specifically, the use of a tungsten contact plug alongside a barrier metal layer to fill contact holes or trench with high aspect ratio is well known to a POSITA. When manufacture of MOSFETs scale to smaller dimension, there is an increased need for an interconnect process with good planarization. One must fill contact holes that have high aspect ratio, like a trench, and achieve smooth top planar surface. This is achieved by the use of chemical vapor deposition (“CVD”) of tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio, and produces a planar top surface after the CVD tungsten is etched back. It is also obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the use of a barrier metal layer. The barrier metal layer will act as a diffusion barrier - preventing unwanted interactions between the CVD W and the silicon. A POSITA would have found it obvious to use Ti/TiN, as the common barrier metal layer material is Ti/TiN layer.

149. Shiraishi expressly teaches a lateral contact layer along the entire sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. K, Shiraishi at Fig. 8, [0073], [0080], [0084]-[0085]. A POSITA would therefore have been motivated to combine the distinct lateral contact layer of Shiraishi with a P doping concentration that is greater than the P-type doping concentration of the underlying base layer, but less than the P-type concentration of the base contact layer, with the disclosure of Kobayashi 174 to optimize the MOSFET and prevent any punch-through.

150. Shiraishi also expressly teaches the doping concentration profiles of the lateral contact layer and base contact layer that would prevent such punch-through. *Id.* at Abstract, [0073]. Therefore, the POSITA would have been motivated to experiment with these doping concentration profiles, as opposed to the doping dosing as disclosed in Kobayashi 174, to achieve an anti-punch-through result.

151. Moreover, inverting the P- or N-type regions of the MOSFET is commonly known in the art. A POSITA would generally invert the regions to create either a P- or N- channel MOSFET, as required by the specific product the transistor is supporting. Both Kobayashi 174 and Shiraishi disclose a general MOSFET that can be tailored to be P- or N- channel. In particular, the POSITA would have understood that the inversion of the P- and N- types would not affect the disclosure of contact metal plugs or barrier metal layers. The inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including the use of the same conductive material for the barrier metal layer and the contact metal plugs.

152. Therefore, the combination of Shiraishi and Kobayashi 174 renders obvious Claims 3-9, as illustrated below in a hypothetical diagram based on Shiraishi's Figure 9 with the addition of the tungsten (W) source contact plugs (in purple) and Ti/TiN barrier metal layer (in green) according to disclosures in Kobayashi 174.



8

Shiraishi, Figure 9 (annotated)

2. Claim 3: “The trenched MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

153. Claim 3 is dependent on Claim 2, which is fully disclosed in Shiraishi, as is discussed above. The remaining elements of Claim 3 are also disclosed in Shiraishi and Kobayashi 174. Shiraishi describes a “TiW (titanium tungsten) film serving as a barrier conductor film” *Id.* at [0076]. Kobayashi 174 describes the use of a plurality of contact metal plugs. Ex. J, Kobayashi 174 at [0052], [0066], Fig. 5A, Claim 4. Use of contact metal plugs and the barrier metal layer are generally known to a POSITA. When manufacture of MOSFETs scale to smaller

⁸ The annotations on this figure were originally used to support the Petition for *Inter Partes* Review of the ‘634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

dimension, there is an increased need for an interconnect process with good planarization. One must fill contact holes that have high aspect ratio, like a trench, and achieve smooth top planar surface. This is achieved by the use of chemical vapor deposition (“CVD”) of tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio, and produces a planar top surface after the CVD tungsten is etched back. It is also obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the use of a barrier metal layer. The barrier metal layer will act as a diffusion barrier - preventing unwanted interactions between the CVD W and the silicon. A POSITA would have found it obvious to use Ti/TiN as the common barrier metal layer material is Ti/TiN layer.

154. Kobayashi 174 also teaches that the contact metal plug is beneficial to the operation of the MOSFET. The plug “allows the resistance component of the source electrode 18 [to be] reduced” by creating a flat surface for the source electrode. *Id.* at [0066], Claim 4 (claiming a contact hole filled with “a metal which serves as said contact and has a flattened surface, said source electrode being formed on the flattened surface of said metal . . .”).

155. Kobayashi 174 teaches that the source electrode “having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.” *Id.* at [0066]. A POSITA would have generally understood that eventually the source metal layer, connected to the contact metal plug, will eventually be connected through bonding to a chip package - which will be mounted to a circuit board. Two types of bonding techniques, bonding through a wire or bonding through a copper clip, are commonly used. The main difference between wire bonding and clip bonding is that clip employs a larger surface area for the bonding conducting material. However, in either bonding

technique, a flat metal source electrode or pad, would offer a better surface area for achieving low resistance bonding.

156. Finally, “it is possible to perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface.” *Id.* at [0066]. The POSITA would therefore have been motivated to combine the source contact plugs with the disclosure of Shiraishi.

3. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

157. Claim 4 is dependent on Claim 3, the elements of which are discussed above. The remaining elements of Claim 4 are disclosed in Shiraishi and Kobayashi 174. Shiraishi discusses the uses of a barrier metal layer that is made of TiW (titanium-tungsten). Ex. K, Shiraishi at [0076]. Kobayashi 174 discusses the use of the contact metal plug that is made of tungsten (W). Ex. J, Kobayashi 174 at [0052], [0066], Fig. 5A. Kobayashi 174 also discusses the use of a barrier metal layer that is made of Ti and TiN. *Id.* at [0062]. A POSITA would also have known that the common barrier metal layer material is Ti/TiN.

4. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

158. Claim 5 is dependent on Claim 4, the elements of which are discussed above. The remaining elements of Claim 5 are disclosed in Shiraishi, which describes a trench MISFET with a plurality of vertical source contact trenches. Ex. K, Shiraishi at Fig. 8. Kobayashi 174 also discloses source contact trenches with a U-shape, V-shape, or rectangular shape. Ex. J, Kobayashi 174 at [0072], Figs. 9A, 9B. A POSITA would generally know that the shape of the trenches is a function of the etching chemistry. In fact, not only can the source contact trench be selected from one of a vertical shape and tapered shape, the gate trench can also be selected from the two shapes as well, with the tapered shape commonly known as VMOS, while the vertical shape is commonly known as UMOS.

- 5. Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

159. Claim 6 is dependent on Claim 1, the elements of which are discussed above. The remaining elements of Claim 6 are disclosed in Shiraishi and Kobayashi 174. Shiraishi discloses the formation of a trench MOSFET with semiconductor layers of “a first conductivity type [e.g., N-type] ” and “second conductivity type opposite to the first conductivity type [e.g., P-type],” along with specific embodiments of an n-channel MOSFET. *See, e.g.*, Ex. K, Shiraishi at [0017], [0028], [0067], Claim 1. Kobayashi 174 similarly discloses a trench MOSFET with semiconductor layers of a first conductivity type and a second conductivity type opposite to the first conductivity type, along with specific embodiments of n-channel MOSFETs. *See, e.g.*, Ex. J, Kobayashi 174 at Claim 1, [0062]. In particular, Kobayashi 174 discusses “inverting the conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure.” *Id.* at [0072]. A POSITA would have generally understood that the conductivity type options are limited to P-type or N-type channel MOSFETs. A POSITA would also have known that there are only two conductivity types and would know how to alter a design to account for P-channel or N-channel MOSFET as needed.

- 6. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”**

160. Claim 5 is dependent on Claim 6, the elements of which are discussed above. The remaining elements of Claim 7 are disclosed in Shiraishi and Kobayashi 174 and the knowledge of the POSITA, as is described above in relation to Claim 3. *Supra* X.I.2.

161. A POSITA would have understood that simply inverting the conductivity types allows for the formation of either an N-channel MOSFET or a P-channel MOSFET. The inversion

of conductivity types is a fundamental concept when forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including the use of the same conductive material for the barrier metal layer and the contact metal plugs.

7. Claim 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

162. Claim 8 is dependent on Claim 7, the elements of which are discussed above. The remaining elements of Claim 8 are disclosed in Shiraishi and Kobayashi 174, as is described above in relation to Claim 4. *Supra* X.I.3. A POSITA would have known that the inversion of conductivity types would not affect the previous disclosure and analysis.

8. Claim 9: The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”

163. Claim 9 is dependent on Claim 8, the elements of which are discussed above. The remaining elements of Claim 9 are disclosed in Shiraishi and Kobayashi 174, as is described above in relation to Claim 5. *Supra* X.I.4. A POSITA would have known that the inversion of conductivity types would not affect the previous disclosure and analysis.

J. Claims 1-9 Are Unpatentable as obvious over Kobayashi 174 in View of Shiraishi

1. Motivation to Combine

164. I contend that it would have been obvious to a POSITA, prior to the effective filing date of the '634 Patent (February 23, 2008) to combine Kobayashi 174 and Shiraishi in such a way that they would arrive at the subject matter of Claims 1-9, rendering those claims invalid under pre-AIA 35 U.S.C. § 103.

165. Specifically, a POSITA would have been motivated to combine the lateral contact layer and doping concentration profiles taught by Shiraishi with the MOSFET featured in Kobayashi 174 in order to arrive at the subject matter of Claims 1-2 and 3-9. Additionally, a POSITA would have been motivated to combine Shiraishi with Kobayashi 174 in order to invert the P/N types of Kobayashi 174, which would teach the subject matter of Claims 6-9. P-channel and N-channel MOSFETs using inversion layers are well-known concepts in the art and therefore to the POSITA.

166. Shiraishi, Kobayashi 174, and the '634 Patent are all analogous art seeking to solve similar problems. Shiraishi, Kobayashi 174, and the '634 Patent are all in the same field of endeavor, i.e., Vertical Power MOSFET structures. All are based in the same methods to improve the performance tradeoff in the ON-state (ON-Resistance and speed) and OFF-state (breakdown voltage). Moreover, Shiraishi, Kobayashi 174, and the '634 Patent disclose a similar doping concentration engineering technique, i.e., dopant ion implantation, which allows for formation of a low resistance source contact, located at the bottom of the base region and/or on the sidewall of the trenched contact region, either of which with minimal impact to the threshold voltage or the ON-Resistance of the Power MOSFET.

167. Additionally, Kobayashi 174 expressly teaches that the contact metal plug is beneficial because it “allows the resistance component of the source electrode 18 [to be] reduced” by creating a flat surface for the source electrode. Ex. J, Kobayashi 174 at [0066]; *id.* at Claim 4 (claiming use of a metal contact plug to provide a flattened surface and a source electrode deposited on said flattened surface). Kobayashi 174 further teaches the source electrode “having a flat surface assures a wide contact area in wire bonding or clip bonding carried out for the surface so that a total on-resistance after mounting can be reduced.” *Id.* at [0066]. Lastly, “it is possible to

perform chip mounting by bump connection, which is difficult when the source electrode has an irregular surface.” *Id.* In particular, Kobayashi 174 teaches the use of tungsten metal contact plugs. The POSITA would therefore have been motivated to combine the metal contact plugs taught by Kobayashi 174 with the disclosures of Shiraishi.

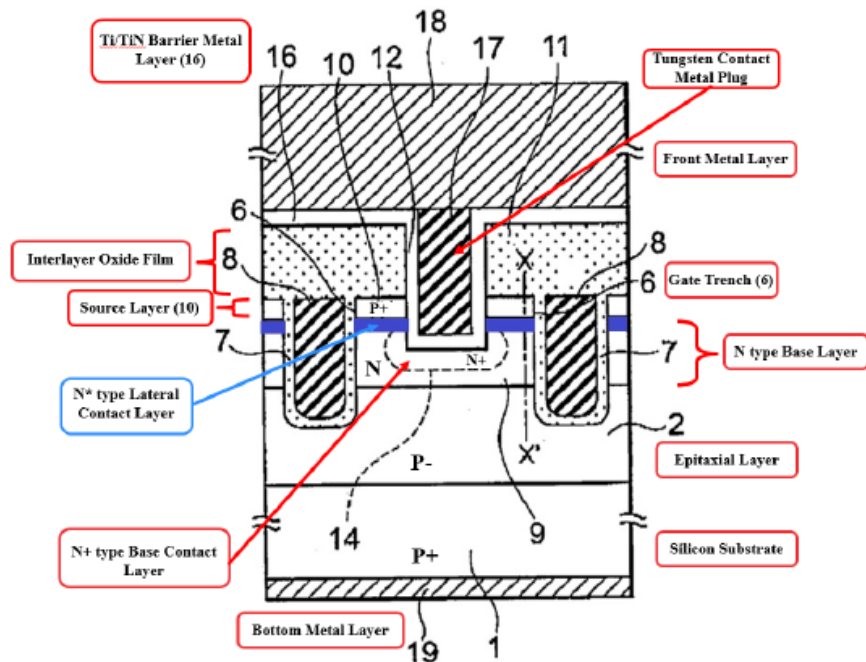
168. The POSITA would also have been motivated to combine the barrier metal layer disclosed in Kobayashi 174 with the MISFET disclosed in Shiraishi. A POSITA would commonly know that the use of a barrier metal layer, made of materials such as Ti and TiN, would promote the adhesion of the tungsten contact plug from Kobayashi 174 to the contact area of the source contact trenches. The Ti and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition process of W, from seeping into the underlying silicon surface, which would degrade the performance of the transistor.

169. Specifically, the use of a tungsten contact plug alongside a barrier metal layer to fill contact holes or trench with high aspect ratio is well known to a POSITA. When manufacture of MOSFETs scale to smaller dimension, there is an increased need for an interconnect process with good planarization. One must fill contact holes that have high aspect ratio, like a trench, and achieve smooth top planar surface. This is achieved by the use of chemical vapor deposition (“CVD”) of tungsten. The CVD tungsten process is able to conformally fill contact holes with a high aspect ratio, and produces a planar top surface after the CVD tungsten is etched back. It is also obvious to a POSITA that the deposition of CVD tungsten is typically preceded by the use of a barrier metal layer. The barrier metal layer will act as a diffusion barrier - preventing unwanted interactions between the CVD W and the silicon. A POSITA would have found it obvious to use Ti/TiN, as the common barrier metal layer material is Ti/TiN layer.

170. Shiraishi expressly teaches a lateral contact layer along the entire sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. K, Shiraishi at Fig. 8; [0073], [0080], [0084]-[0085]. A POSITA would therefore have been motivated to combine the distinct lateral contact layer of Shiraishi with a P doping concentration that is greater than the P-type doping concentration of the underlying base layer, but less than the P-type concentration of the base contact layer, with the disclosure of Kobayashi 174 to optimize the MOSFET and prevent any punch-through.

171. Shiraishi also expressly teaches the doping concentration profiles of the lateral contact layer and base contact layer that would prevent such punch-through. *Id.* at Abstract, [0073]. Therefore, the POSITA would have been motivated to experiment with these doping concentration profiles, as opposed to the doping dosing as disclosed in Kobayashi 174, to achieve an anti-punch-through result.

172. Therefore, the combination of Kobayashi 174 and Shiraishi renders obvious Claims 1-9, as is illustrated below in the hypothetical diagrams based on Kobayashi 174’s Figure 5A with the addition of the lateral contact layer (in blue) according to disclosure in Shiraishi. N-channel and p-channel MOSFETs are both depicted.



9

Kobayashi 174, Figure 5A (annotations added)

2. Claim 1

a) [1.pre]. “A *trenched MOSFET with trenched source contact, comprising:*”

173. To the extent the preamble is limiting, it is disclosed in Kobayashi 174, which describes a trenched MOSFET with source contact trenches. Ex. J, Kobayashi 174 at Fig. 5A, [0052].

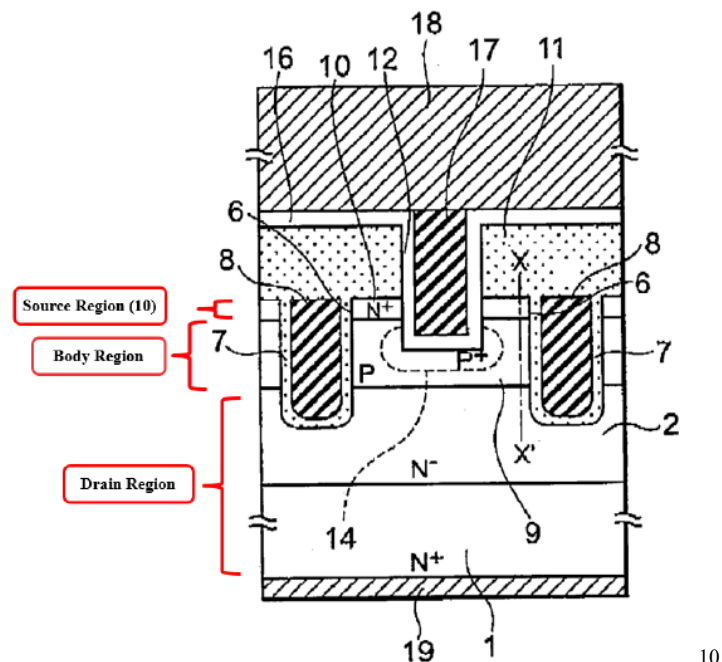
b) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

174. Claim 1.a is disclosed in Kobayashi 174, which describes a vertical trenched MOSFET with a drain region, a body region, and a source region— all of which are features that a POSITA would know are universal to MOSFETs. *Id.* at Fig. 5A, [0018] (disclosing “Structure

⁹ The annotations on these figures were originally used to support the Petition for *Inter Partes* Review of the ‘634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

1. A vertical MOSFET (or a UMOSFET) comprising: a semiconductor layer (1, 2, 9, 10) having first and second surface opposite to each other and . . . a unit cell formed in a region of the semiconductor layer surrounded by the pair of trench gates, the unit cell comprising a base layer (9) and a source layer (10) formed on the base layer . . .”), [0052]. A POSITA would have understood that, for example in Figure 5A, Kobayashi 174 depicts a MOSFET with a N^+ -type drain region at 1, a P-type body region at 7, and a N^+ -type source region at 10. A POSITA would also have known that a base layer corresponds to and is equivalent to a body layer.

175. Specifically, Kobayashi 174 discloses an arrangement where “an N^+ -type silicon substrate 1 and an N^- -type epitaxial layer 2 formed on one surface of the N^+ -type silicon substrate 1. A P-type base layer 9 and an N^+ -type source layer 10 are formed on a surface of the N^- -type epitaxial layer 2. . . .” *Id.* at [0052].



Kobayashi 174, Figure 5A (annotated in regards to Claim element 1a)

¹⁰ The annotations on these figures were originally used to support the Petition for *Inter Partes* Review of the ‘634 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0093). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

c) [1.b]. “a front metal layer formed on the upper surface of said semiconductor region”

176. Claim 1.b is disclosed in Kobayashi 174, wherein a “source electrode 18” is located on the surface of the barrier metal layer and source contact plug. *Id.* at Fig. 5A, [0052] (“On the surface of the W 17 and the barrier metal 16, a source electrode 18 is formed.”), [0018] (. . . “a source electrode (18) formed on the contact [hole]”). A POSITA would have generally understood that the “source electrode” corresponds to, and is equivalent to, a “front metal layer.” This is a feature that is well-known in the art and would have been well-known to the POSITA.

d) [1.c]. “an interlayer oxide film formed between said source layer and said front metal layer;”

177. Claim 1.c is disclosed by Kobayashi 174, wherein an interlayer oxide film (11) is created atop the gate trenches and in between the source region (10) and the source electrode (18). *Id.* at Fig. 5A, [0052] (“On the polysilicon 8 to serve as a gate electrode or a trench gate, an interlayer oxide film 11 is formed”). This is a feature that is well-known in the art and would have been well-known to the POSITA.

e) [1.d]. “a bottom metal layer formed on the lower surface of said semiconductor region;”

178. Claim 1.d is disclosed by Kobayashi 174, wherein a “drain electrode 19” is created on the surface of the N⁺-type silicon substrate (1). *Id.* at Fig. 5A, [0052] (“On the other surface of the N⁺-type silicon substrate 1, a drain electrode 19 is formed.”), [0018]. A POSITA would have understood that the “drain electrode” corresponds to and is equivalent to a “bottom metal layer.” This is a feature that is well-known in the art and would have been well-known to the POSITA.

f) [1.e]. “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”

179. The broader construction of this term would instruct that trenched gates are formed from the top of source layer and extend down through the base layer. In this construction, the gates

need not come from above the source layer. As is demonstrated in Figure 5A, Kobayashi 174 teaches a plurality of trench gates (6) which are covered by the interlayer oxide film (11) and which extend downward through the source layer (10), the base layer (9), and into the epitaxial layer (2). *Id.* at Fig. 5A, [0052], [0055]-[0058]. This is a feature that is well-known in the art and would have been well-known to the POSITA. Specifically Kobayashi 174 teaches that “[i]n each of trenches 6 reaching the N⁻-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled.” *Id.* at [0052].

180. Even if the more narrow construction is applied, where the gates must extend from above the source layer, this element is still disclosed in Kobayashi 174. As is demonstrated in Figure 5A, Kobayashi 174 teaches a plurality of trench gates (6) which are covered by the interlayer oxide film (11) and which extend downward through the source layer (10), the base layer (9), and into the epitaxial layer (2). *Id.* at Fig. 5A, [0052], [0055]-[0058]. This is a feature that is well-known in the art and would have been well-known to the POSITA. Specifically Kobayashi 174 teaches that “[i]n each of trenches 6 reaching the N⁻-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled.” *Id.* at [0052].

g) [1.f]. “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”

181. Claim 1.f is disclosed by Kobayashi 174. Specifically, as illustrated in Fig. 5A, Kobayashi 174 teaches “contact holes 12” formed on top of the interlayer oxide film, which extend down through the N⁺-type source layer to the P-type base layer. *Id.* at Fig. 5A, [0052]. The POSITA would have understood that “contact holes” correspond to and are equivalent to “source contact trenches.” This is a feature that is well-known in the art and would have been well-known to the POSITA. Specifically Kobayashi 174 discloses “[b]etween the trench gates adjacent to each other,

a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 though the N⁺-type source layer 10.” *Id.* at [0052].

h) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

182. The broader construction of this term would instruct that only a portion of the sidewalls need be covered by the lateral contact layer. This is disclosed by Kobayashi 174 and Shiraishi. Kobayashi 174 teaches a base contact layer which covers the bottom of the source contact trench and which extends partially up along the sidewalls of the source contact trenches. *Id.* at Fig. 5A, [0061], Claim 1 (“... a base contact layer 14 formed within said base layer so as to enclose a bottom of said contact and to bring said base contact layer into contact with the bottom of said contact.”), Claim 3 (“... said base contact layer is formed within said base layer so as to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”); *see* Ex. D, ’409 Patent at Fig. 1B.

183. Meanwhile, Figure 8 from Shiraishi discloses an additional semiconductor layer (14) (i.e., lateral contact layer) along at least a portion of the sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. K, Shiraishi at Fig. 8; [0073] (“the p-type semiconductor region 14 may serve as a punch-through stopper layer for the respective power MISFETs”), [0080], [0084]-[0085]. A POSITA would have understood that a punch-through stopper is helpful in preventing current punch-through from the source layer through the body layer and to the silicon substrate or drain region.

184. Specifically, a POSITA would have generally understood that punch-through is an undesirable phenomenon, and can occur in a structure with two junctions, wherein a layer of a second polarity is sandwiched between two layers of a first polarity (for example, an N-P-N structure), as pictured in Figure 5A in Kobayashi 174 and Figure 8 in Shiraishi. Punch-through

occurs when the middle second polarity layer, the body layer, can no longer act as a conduction barrier between the two first-polarity end layers - the source and drain regions. This can occur when the doping concentration of the middle layer is light, with high voltage on one of the end layer causing the depletion region to reach all the way to the layer at the other end, i.e. “punch-through.” The unwanted punch-through current causes the MOSFET to malfunction and unintentionally turn “on” when the transistor should otherwise be “off.” As discussed above, the POSITA would have been motivated to combine the lateral contact layer of Shiraishi with the other necessary disclosures of Kobayashi 174.

185. Even if the more narrow construction is applied, where the entire sidewall must be covered by the lateral contact layer, this element is still disclosed by Kobayashi 174 and Shiraishi. Kobayashi 174 teaches a base contact layer which covers the bottom of the source contact trench and which extends partially up along the sidewalls of the source contact trenches. Ex. J, Kobayashi 174 at Fig. 5A, [0061], Claim 1 (“... a base contact layer 14 formed within said base layer so as to enclose a bottom of said contact and to bring said base contact layer into contact with the bottom of said contact.”), Claim 3 (“... said base contact layer is formed within said base layer so as to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”); *see* Ex. D, ’409 Patent at Fig. 1B.

186. Meanwhile, Figure 8 from Shiraishi discloses an additional semiconductor layer (14) (i.e., lateral contact layer) along the entirety of the sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. K, Shiraishi at Fig. 8, [0073] (“the p-type semiconductor region 14 may serve as a punch-through stopper layer for the respective power MISFETs”), [0080], [0084]-[0085]. A POSITA would have understood that a punch-through

stopper is helpful in preventing current punch-through from the source layer through the body layer and to the silicon substrate or drain region.

187. Specifically, a POSITA would have generally understood that punch-through is an undesirable phenomenon, and can occur in a structure with two junctions, wherein a layer of a second polarity is sandwiched between two layers of a first polarity (for example, an N-P-N structure), as pictured in Figure 5A in Kobayashi 174 and Figure 8 in Shiraishi. Punch-through occurs when the middle second polarity layer, the body layer, can no longer act as a conduction barrier between the two first-polarity end layers - the source and drain regions. This can occur when the doping concentration of the middle layer is light, with high voltage on one of the end layer causing the depletion region to reach all the way to the layer at the other end, i.e. “punch-through.” The unwanted punch-through current causes the MOSFET to malfunction and unintentionally turn “on” when the transistor should otherwise be “off.” As discussed above, the POSITA would have been motivated to combine the lateral contact layer of Shiraishi with the other necessary disclosures of Kobayashi 174.

i) [1.h]. “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

188. Claim 1.h is disclosed by Kobayashi 174, in which the bottom of the source contact trench is covered by a base contact layer (14). Ex. J, Kobayashi 174 at Fig. 5A, [0061], Claim 3 (“... said base contact layer is formed within said base layer so as to enclose only the bottom of said contact and to bring said base contact layer into contact with only the bottom of said contact.”). This is a feature that is well-known in the art and would have been well-known to the POSITA.

3. Claim 2

a) [2.a]. “The trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

189. Claim 2 is dependent on Claim 1, elements of which are discussed above. This element is additionally disclosed in Kobayashi 174. Kobayashi 174 describes a trench MOSFET wherein the silicon substrate, the epitaxial layer, and the source layer are N-type. *Id.* at Fig. 5A, [0052] (“... an N⁺-type silicon substrate 1 and an N⁻-type epitaxial layer 2 formed on one surface of the N⁺-type silicon substrate 1. A P-type base layer 9 and an N⁺-type source layer 10 are formed on a surface of the N⁻-type epitaxial layer 2.”). This is a feature that is well-known in the art and would have been well-known to the POSITA.

b) [2.b]. “the base layer and lateral contact layer are P-type;”

190. Claim 2.b is disclosed in Kobayashi 174, Shiraishi, and the knowledge of the POSITA, as discussed above in Section X(E)(h). The remaining elements are disclosed in Kobayashi 174 and Shiraishi respectively. Kobayashi 174 discloses a P-type base layer and P⁺-type base contact layer. *Id.* at Fig. 5A, [0052], [0061]. Additionally, Shiraishi discloses a P-type semiconductor region 14 (lateral contact layer) that serves as an anti-punch-through layer. Ex. K, Shiraishi at [0073]. This is a feature that is well-known in the art and would have been well-known to the POSITA.

c) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

191. Claim 2.c is disclosed in Kobayashi 174 and Shiraishi. Specifically, Kobayashi 174 discusses a P⁺-type base contact layer at the bottom of the source trenches. Ex. J, Kobayashi 174 at Fig. 5A, [0061]. Shiraishi then discloses an additional semiconductor layer (14) (i.e. lateral contact layer) along the sidewalls of the contact trench in the base layer that serves as “a punch-through stopper layer.” Ex. K, Shiraishi at Fig. 8; [0073], [0080], [0084]-[0085]. Specifically, Shiraishi discloses that the “p-type semiconductor region 14 [i.e., lateral contact layer] may be locally higher in impurity concentration than the p type semiconductor region 13.” *Id.* at [0080].

In addition, Shiraishi teaches that “[i]mpurity concentration in the p+type semiconductor region 20 [i.e., base contact layer] may be rendered higher than that in the p-type semiconductor region 14 [i.e., lateral contact layer].” *Id.* at [0073]. Therefore, a POSITA would have been motivated to combine the doping concentration profile with the relevant disclosures from Kobayashi 174.

4. Claim 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

192. Claim 3 is dependent on Claim 2, elements of which are discussed above. The remaining elements of Claim 3 are taught by Kobayashi 174, which discloses the use of contact metal plugs and a barrier metal layer. Ex. J, Kobayashi 174 at [0052]-[0053], [0066], Fig. 5A.

5. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

193. Claim 4 is dependent on Claim 3, the elements of which are discussed above. The remaining elements of Claim 4 are taught by Kobayashi 174, which discloses the use of tungsten contact metal plugs. *Id.* at [0052], [0066], Fig. 5A. Kobayashi 174 also describes the use of a barrier metal layer that is made of Ti and TiN. *Id.* at [0062].

6. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

194. Claim 5 is dependent on Claim 4, the elements of which are discussed above. The remaining elements of Claim 5 are taught by Kobayashi 174, which discloses a MOSFET with a source contact trench with a U-shape, V-shape, or rectangular shape. *Id.* at [0072], Figs. 5A, 9A, 9B. A POSITA would generally know that the shape of the trenches is a function of the etching chemistry. A source contact trench can be selected to be of a vertical or tapered design, based on this chemistry. Similarly, the gate trench can be selected from these two shapes, with the tapered shape commonly referred to as VMOS, and the vertical referred to as UMOS.

7. Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and

lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

195. Claim 6 is dependent on Claim 1, elements of which are discussed above. The remaining elements of Claim 6 are taught by Kobayashi 174 and Shiraishi. Kobayashi 174 describes a trench MOSFET with layers of a first conductivity type and second conductivity type opposite to the first conductivity type, along with specific embodiments of n-channel MOSFETs. *See, e.g., Id.* at Claim 1, [0062]. Kobayashi 174 also describes “inverting the conductive type, [such that] this invention is also applicable to a P-channel MOSFET structure.” *Id.* at [0072]. Shiraishi similarly discusses a trench MOSFET with semiconductor layers of a first conductivity type and of a second conductivity type opposite to the first conductivity type, along with specific embodiments of an n-channel MOSFET. *See, e.g., Ex. K, Shiraishi* at [0017], [0028], [0067], Claim 1. A POSITA would have generally understood that there are only two conductivity types and would know how to alter designs to account for P-channel or N-channel MOSFETs as needed.

8. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

196. Claim 7 is dependent on Claim 6, the elements of which are discussed above. The remaining elements of Claim 7 are taught by Kobayashi 174, as described above in relation to Claim 3. A POSITA would have known that simply inverting the conductivity types allows for the formation of either an N-channel MOSFET or a P-channel MOSFET. The inversion of conductivity types is the fundamental basis in forming Complementary Metal-Oxide-Silicon (CMOS) Field Effect Transistors. The metallurgy for contacting and interconnecting the source and drain regions is the same for either N-channel MOSFET or P-channel MOSFET, including the use of the same conductive material for the barrier metal layer and the contact metal plugs..

9. Claim 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

197. Claim 8 is dependent on Claim 7, the elements of which are discussed above. The remaining elements of Claim 8 are taught by Kobayashi 174, as is described above. A POSITA would have generally understood that the inversion of conductivity types would not affect the previous disclosure and analysis.

10. Claim 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”

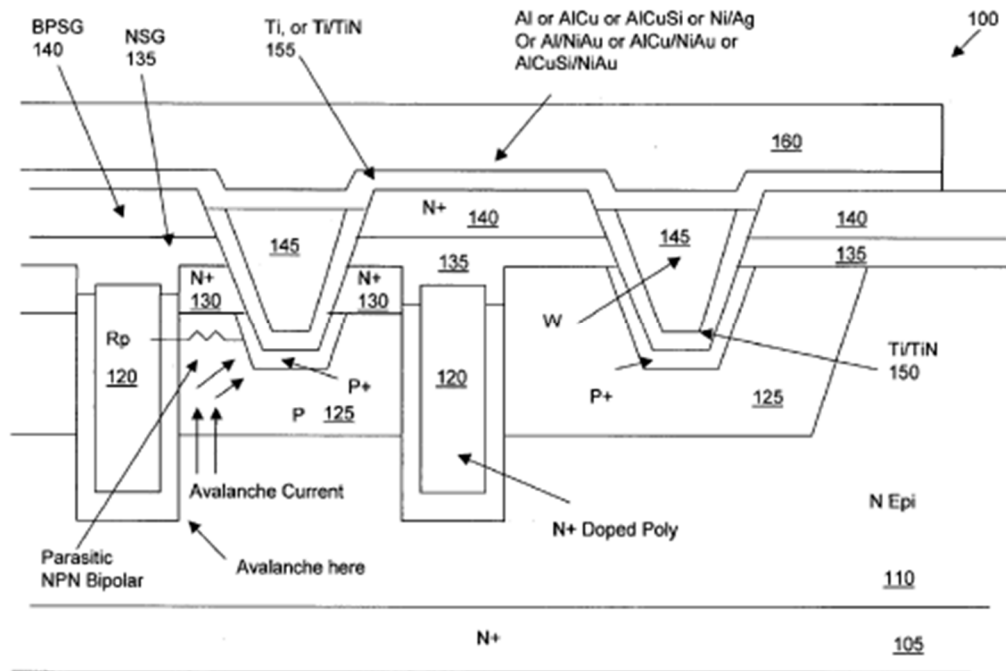
198. Claim 9 is dependent on Claim 8, the elements of which are discussed above. The remaining elements of Claim 9 are taught by Kobayashi 174, as described above in relation to Claim 5. *Supra* X.J.6. A POSITA would have generally understood that the inversion of conductivity types would not affect the previous disclosure and analysis.

K. Claim 1 is Unpatentable as Anticipated by Hsieh 384

1. Claim 1

a) [1.pre]. “A trench MOSFET with trench source contact, comprising:”

199. Hsieh 384 discloses a trench MOSFET with a trench source contact. Figure 3, reproduced below, shows a “metal oxide semiconductor field effect transistor (MOSFET) device 100.” Ex. X, Hsieh 384 at [0026]. The MOSFET includes “a plurality of trench source contact filled with a tungsten plug 145.” *Id.* at [0027].



Hshieh 384, Figure 3

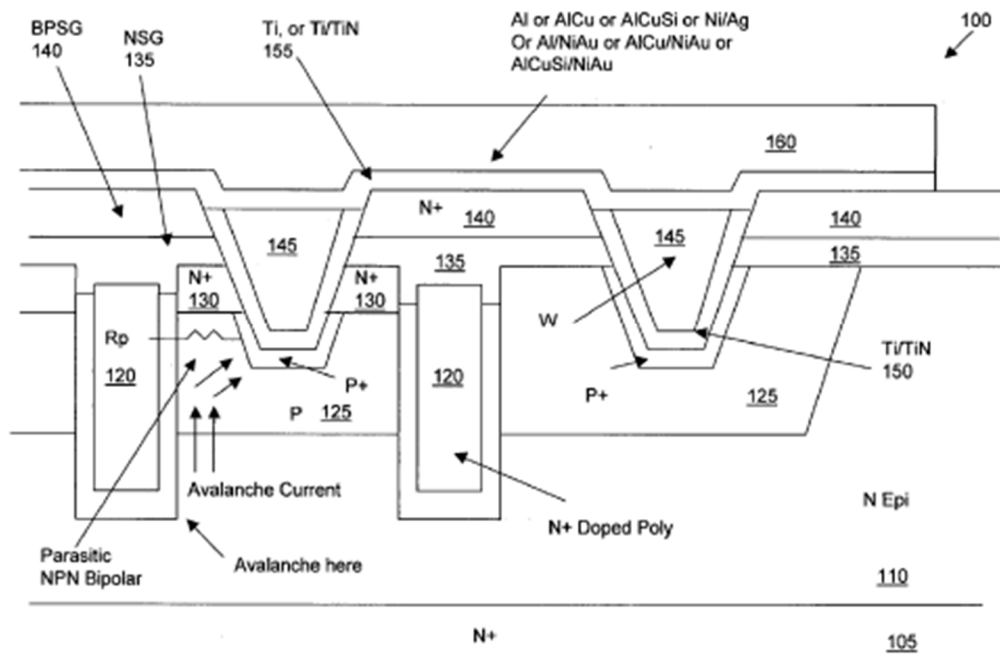
b) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

200. Hshieh 384 discloses a semiconductor region having a drain region comprising a silicon substrate and an epitaxial layer. As shown in Figure 3, reproduced above, Hshieh 384 discloses a MOSFET device 100 that is “supported on a N+ substrate 105 formed with an N epitaxial layer 110.” *Id.* at [0026].

201. Hshieh 384 further discloses a body region comprising a base layer disposed on top of the epitaxial layer and a source region comprising a source layer disposed on the top of the base layer. As shown in Figure 3 above, the P-body regions 125 are formed on top of the N epitaxial layer 110 and the N+ source regions 130 are formed on top of the P-body regions. *See also Id.* at [0026].

c) [1.b]. “a front metal layer formed on the upper surface of said semiconductor region”

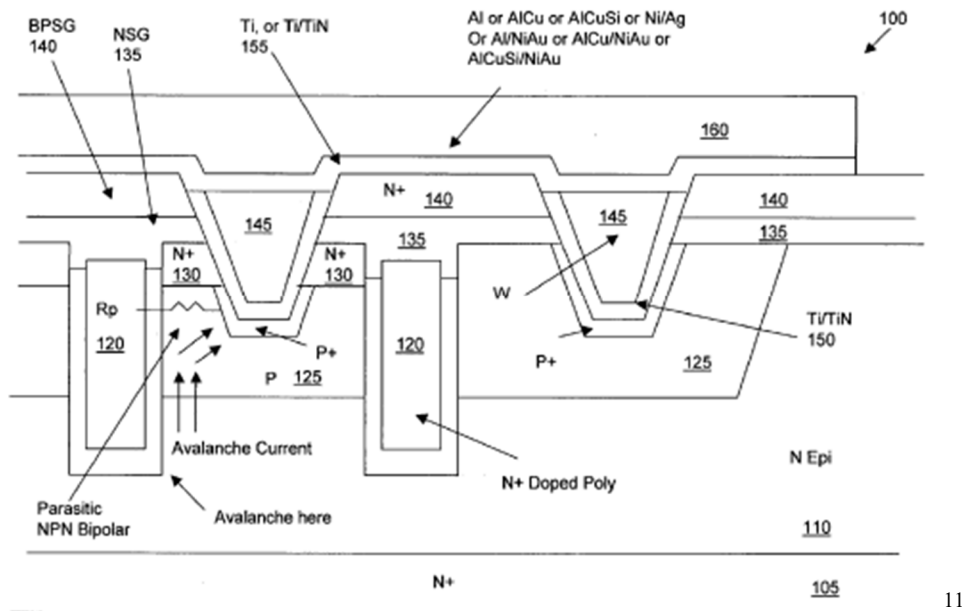
202. Hshieh 384 discloses a front metal layer formed on the upper surface of a semiconductor region. As shown in Figure 3, reproduced below, Hshieh 384 teaches “[a] top contact layer 160 [that] is then formed on top of the source contact layer 155.” *Id.* at [0027].



Hshieh 384, Figure 3

d) [1.c]. “an interlayer oxide film formed between said source layer and said front metal layer;”

203. Hshieh 384 discloses an interlayer oxide film formed between the source layer and the front metal layer. Hshieh 384 teaches that “the P body regions 125 and the source regions 130 are covered with a NSG and a BPSG protective layers 135 and 140 respectively.” *Id.* at [0026]. The source contact layer 155 is formed above the interlayer oxide films 135 and 140, and “[a] top contact layer 160 is then formed on top of the source contact layer 155.” *Id.* at [0027]. Figure 3, reproduced below, illustrates the disclosed structure.



Hshieh 384, Figure 3

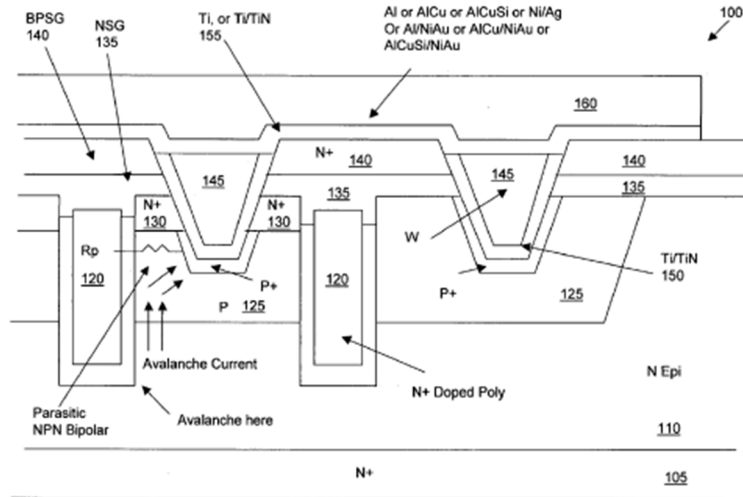
e) [1.d]. “a bottom metal layer formed on the lower surface of said semiconductor region;”

204. Hshieh 384 discloses a bottom metal layer formed on the lower surface of a semiconductor region.

f) [1.e]. “a plurality of *trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and*”

205. Hsieh 384 discloses a plurality of trench gates that are covered by an interlayer oxide film, formed from top of the source layer, and extend down through the base layer to a portion of the epitaxial layer. Hsieh 384 teaches “a plurality of trench source contact filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150. The contact trenches are opened through the NSG and BPSG protective layers 135 and 140 to contact the source regions 130 and the P-body 125.” *Id.* at [0027]. As shown in Figure 3, reproduced below, the trench gates 120 reach the N-epitaxial layer 110.

¹¹ Figure 3 mislabels interlayer oxide film 140 as being “N+.” Hsieh 384 teaches that interlayer oxide films 135 and 140 are NSG and BPSG protective layers respectively. Ex. X, Hsieh 384 at [0026].



Hshieh 384, Figure 3

206. Figure 9A, reproduced below, further illustrates the fabrication steps of the MOSFET device shown in Figure 3 above. “A photoresist 206 is applied to open a plurality of trenches 208 in an epitaxial layer 210 supported on a substrate 205.” *Id.* at [0034].

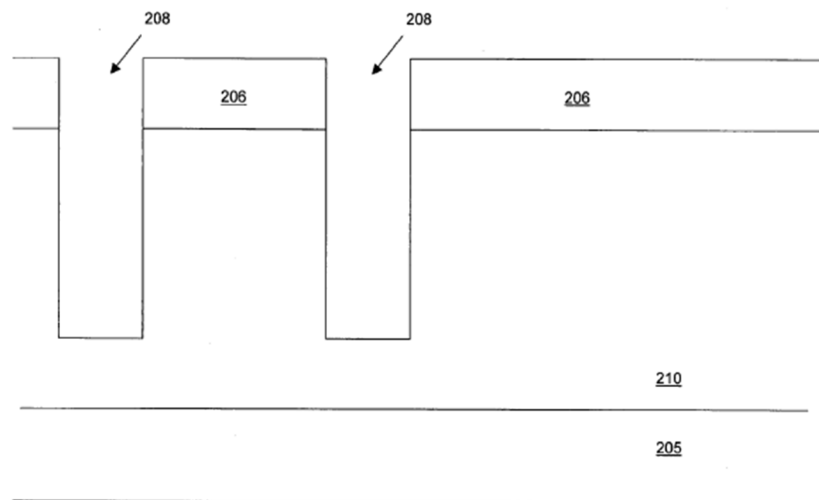


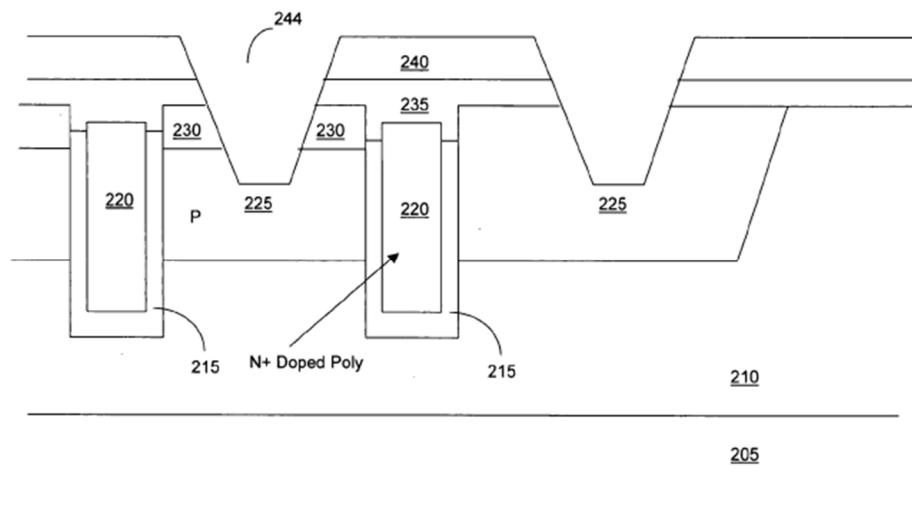
Fig. 9A

Hshieh 384, Figure 9A

g) [1.f]. “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”

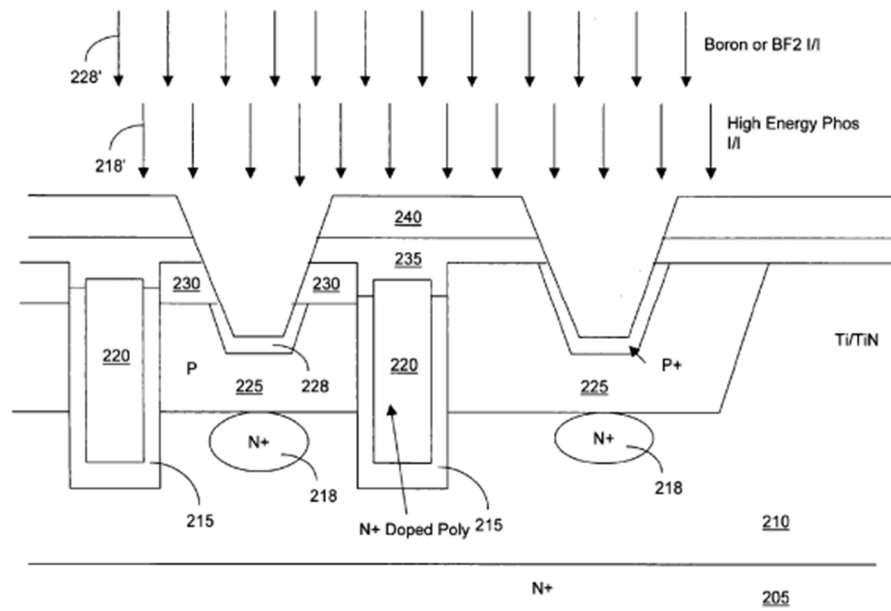
207. Hshieh 384 discloses a plurality of source contact trenches that are formed on the top of the interlayer oxide film and extend down through the source layer to a portion of the base

208. Figure 9F, reproduced below, illustrates the fabrication of the source contact trenches. “a contact mask 242 is applied to carry out a contact etch to open the contact opening 244 by applying an oxide etch through the BPSG and NSG layers followed by a silicon etch to open the contact openings 242 further deeper into the source regions 230 and the body regions 225.” *Id.* at [0034].



h) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

FORCEMOS Ex. 2009
EMC v. Force MOS, IPR2025-01433



Hshieh 384, Figure 9G

i) [1.h]. “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

210. Hshieh 384 teaches Claim 1.h. based on the same evidence and analysis as described above for Claim 1.g. *Supra* X.K.1(h).

2. Claim 2

211. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Hsieh
384 as discussed above.

a) [2.a]. "The *trenched MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;*"

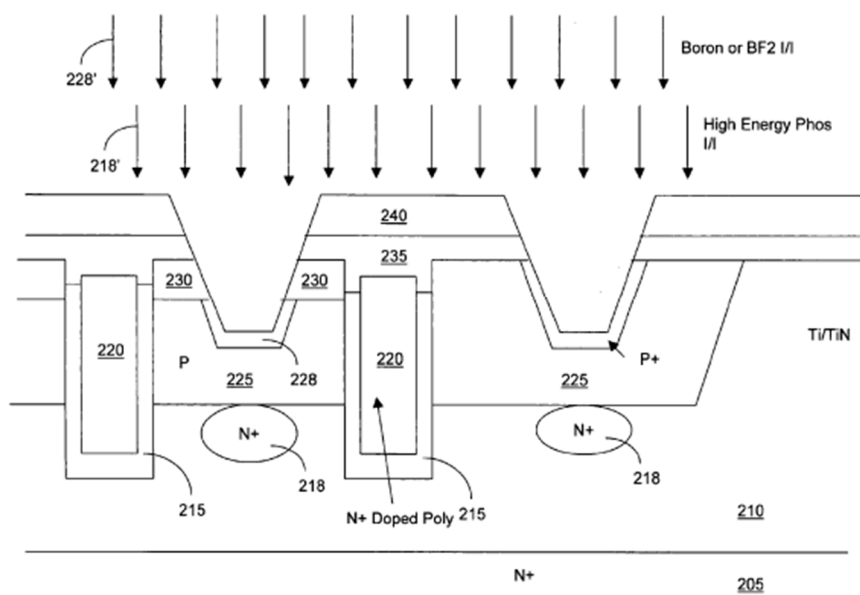
212. Hshieh 384 teaches Claim 2.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* X.K.1(b).

b) [2.b]. “the base layer and lateral contact layer are P-type;”

213. Hshieh 384 teaches Claim 2.b. based on the same evidence and analysis as described above for Claim 1.g-h. *Supra* X.K.1(h)-(i).

c) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

214. Hsieh 384 discloses a lateral contact layer that has less doping concentration than the base contact layer at the bottom. As shown in Figure 9G below, Hsieh 384 teaches a P⁺ doped region that covers both the bottom of the source contact trench and the sidewalls of the source contact trench within the base layer. Hsieh 384 further teaches that “a boron or BF₂ implant with P⁺ ions 228' is first performed to form the P⁺ doped region 228 to surround the trenches 224. The implantation is carried out along a direction of zero degree relative to a perpendicular direction relative to the substrate top surface because the sloped sidewalls of the contact trenches 244.” Ex. X, “Hsieh 384” at [0035]. As known to the POSITA at the time of Hsieh 384's priority date, silicon wafers are usually found in one of three orientations, each with associated ion channeling angles. A POSITA would therefore have known that a nominally perpendicular implantation angle on a circular, typically dry etched sidewall slope, as shown in Fig. 9G, results in a less doping concentration at the sidewalls of the source contact trench as opposed to the bottom of the trench.

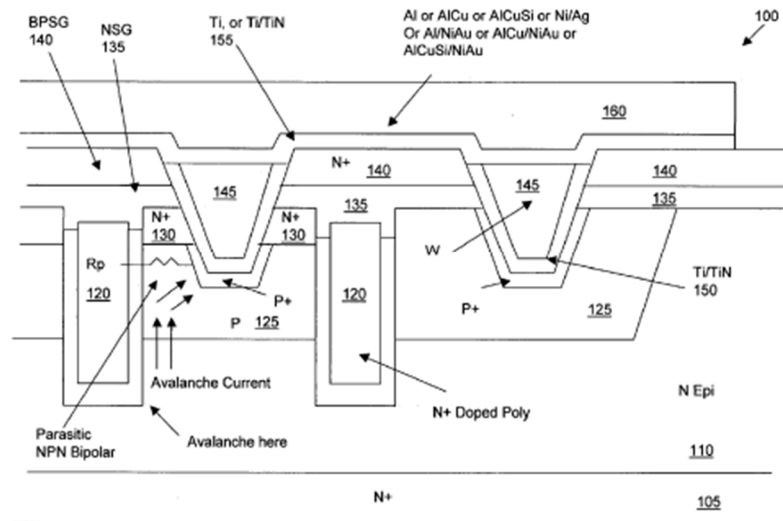


Hshieh 384, Figure 9G

3. Claim 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

215. Claim 3 is dependent on Claim 2, the elements of which are disclosed by Hshieh 384 as discussed above.

216. Hshieh 384 discloses a barrier metal layer and a plurality of contact metal plugs. As shown in Figure 3 below, Hshieh 384 discloses “a plurality of trench source contact filled with a tungsten plug 145 surrounded by a barrier layer Ti/TiN 150.” Ex. X, “Hshieh X”, at [0027]. Hshieh 384 further teaches that “a conductive layer 155 is formed over the top surface to contact the trench source contact 145 and 150.” *Id.* “The conductive layer 155 sandwiched between the top wire-bonding layer 160 and the top of the trench source-plug contact is formed to reduce the resistance by providing greater area of electrical contact.” *Id.*

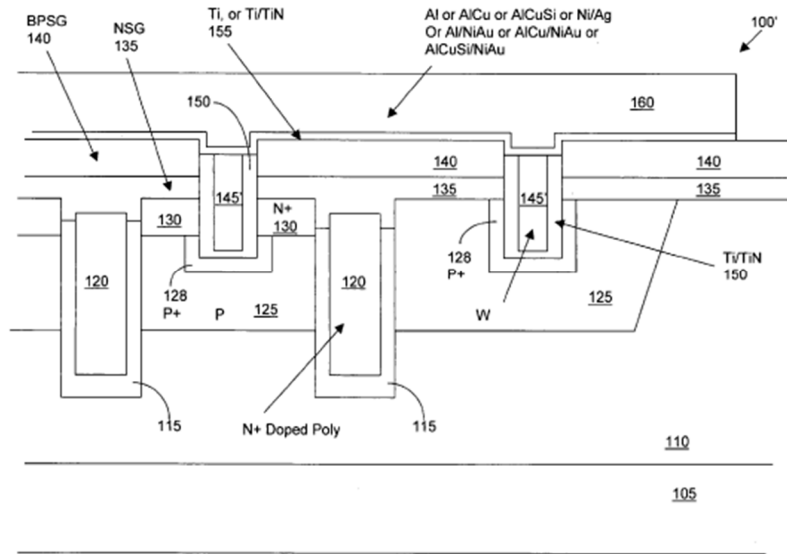


Hshieh 384, Figure 3

4. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

217. Claim 4 is dependent on Claim 3, the elements of which are disclosed by Hshieh 384 as discussed above.

As shown in Figure 4 below, Hsieh 384 teaches that “a source contact plug 145' composed of tungsten surrounded by conductive barrier layer Ti/TiN 150'.” *Id.* at [0029].



Hshieh 384, Figure 4

5. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

219. Claim 5 is dependent on Claim 4, the elements of which are disclosed by Hshieh
384 as discussed above.

220. Hshieh 384 discloses both source contact trenches with a vertical shapes and tapered shapes. As shown in Figure 3 below, “the source-body trenched contact 145 surrounded by the barrier layer 150 as shown are *opened with a slope relative to the regular perpendicular direction* for contacting a P+ doped region 128 surrounding the source-body trenched contact.” *Id.* at [0028] (emphasis added). In addition, Figure 4, also reproduced below, teaches that “the sidewalls are formed with a perpendicular sidewalls.” *Id.* at [0029]. Hshieh 384 further explains that “The only difference [between the embodiments depicted in Figures 3 and 4] is the shape of the trench for disposing the source contact plug 145'.” *Id.*

- 6. Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”**

221. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Hsieh 384 as discussed above.

222. Hsieh 384 discloses the MOSFET of claim 1 wherein the silicon substrate, the epitaxial layer, and the source layer are P-type. Hsieh 384 claims a MOSFET cell of Claim 1 further comprising a P-channel MOSFET cell. *Id.* at [Claim 18].

- 7. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”**

223. Claim 7 is dependent on Claim 6, the elements of which are disclosed by Hsieh 384 as discussed above.

224. Hsieh 384 teaches Claim 7 based on the same evidence and analysis as described above for Claims 3 and 6. *Supra* X.K.3, 6.

- 8. Claim 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”**

225. Claim 8 is dependent on Claim 7, the elements of which are disclosed by Hsieh 384 as discussed above.

226. Hsieh 384 teaches Claim 8 based on the same evidence and analysis as described above for Claims 4 and 6. *Supra* X.K.4, 6.

- 9. Claim 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”**

227. Claim 9 is dependent on Claim 8, the elements of which are disclosed by Hsieh 384 as discussed above.

228. Hshieh 384 teaches Claim 9 based on the same evidence and analysis as described above for Claims 5 and 6. *Supra* X.K.5, 6.

L. Claims 2-9 are Unpatentable as Obvious Over Hshieh 384 in view of Hirler

1. Motivation to Combine

229. I contend that it would have been obvious to a POSITA, prior to the effective filing date of the '634 Patent (February 23, 2008), to combine Hshieh 384 and Hirler in such a way that one would arrive at the subject matter of Claims 2-9, rendering those claims invalid.

230. Specifically, a POSITA would have been motivated to combine the lateral contact layer of Hirler, which has less doping concentration than the base contact layer at the bottom of the source contact trench, with the trenched MOSFET disclosed in Hshieh 38, obtaining a reasonable likelihood of success that they arrive at the subject matter of claims 2-9. Additionally, a POSITA would have been motivated to add in the barrier metal and contact plugs from Hsieh 38 to further chances of success for arriving at the subject matter of claims 2-9. The use of a barrier metal layer (in particular made of materials such as Ti and TiN) to encourage adhesion of the tungsten contact plug to the contact area of the source contact trenches, is a well-known concept in the art and therefore to the POSITA.

231. The '634 Patent, Hshieh 384, and Hirler are all analogous art seeking to solve similar problems. The '634 Patent, Hshieh 384, and Hirler are all in the same field of endeavor, i.e., Vertical Power MOSFET structures. The '634 Patent relates to “a trenched MOSFET with trenched source contact.” Ex. X, the '634 Patent.. Similarly, Hshieh 384 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) cell.” Ex. X, Hshieh 384. Hirler also relates to a “MOS power transistor arrangement having a vertical transistor structure.” *Id.*

232. Further, the '634 Patent, Hshieh 384, and Hirler are directed to similar problems. The '634 Patent is directed to the problem of “parasitic N+/P/N” causing breakdowns in trenched

MOSFETs. Ex. C, '634 Patent at 1:35-41. Hshieh 384 is also directed to the problem of “limited avalanche current due to the concerns of inadvertent triggering parasitic N+PN bipolar parasitically exists between the source disposed next to the P-body with the P-body further adjacent to the N-epitaxial layer” among others. Ex. X, Hshieh 384 at [0008]. Finally, Hirler is directed to the problem of breakdowns caused by parasitic bipolar 268.

233. Additionally, the '634 Patent relates to “a trench MOSFET with a trench source contact.” See Ex. C, '634 Patent. Hshieh 384 specifically relates to a “trench metal oxide semiconductor field effect transistor (MOSFET) cell.” Ex. X, Hshieh 384. Hirler specifically relates to a “MOS power transistor arrangement having a vertical transistor structure.” See Ex. I, Hirler at [0001].

234. Therefore, the combination of Hshieh 384 and Hirler renders obvious Claims 2-9 as well. *Id.* at [0002].

2. Claim 2

235. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Hshieh 384 as discussed above. *Supra* X.K.1.

d) [2.a]. “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

236. Hshieh 384 teaches Claim 2.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* X.K.1(b).

e) [2.b]. “the base layer and lateral contact layer are P-type;”

237. Hshieh 384 teaches Claim 2.b. based on the same evidence and analysis as described above for Claim 1.g-h. *Supra* X.K.1(h)-(i).

f) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

238. Hirler teaches Claim 2.c based on the same evidence and analysis as described above for Claim 2.c. *Supra* X.F.2(c).

239. Hshieh 384 also teaches Claim 2.c based on the same evidence and analysis as described above for Claim 2.c. *Supra* X.K.2(c).

3. Claim 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

240. Claim 3 is dependent on Claim 2, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

241. Hshieh 384 teaches Claim 3 based on the same evidence and analysis as described above for Claim 3. *Supra* X.K.3.

4. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

242. Claim 4 is dependent on Claim 3, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

243. Hshieh 384 also teaches Claim 4 based on the same evidence and analysis as described above for Claim 4. *Supra* X.K.4.

5. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

244. Claim 5 is dependent on Claim 4, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

245. Hshieh 384 also teaches Claim 5 based on the same evidence and analysis as described above for Claim 5. *Supra* X.K.5.

6. Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

246. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

247. Hshieh 384 also teaches Claim 4 based on the same evidence and analysis as described above for Claim 4. *Supra* X.K.6.

7. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

248. Claim 7 is dependent on Claim 6, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

249. Hshieh 384 teaches Claim 7 based on the same evidence and analysis as described above for Claims 3 and 6. *Supra* X.K.3, 6.

8. Claim 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

250. Claim 8 is dependent on Claim 7, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

251. Hshieh 384 teaches Claim 8 based on the same evidence and analysis as described above for Claims 4 and 6. *Supra* X.K.4, 6.

9. Claim 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”

252. Claim 9 is dependent on Claim 8, the elements of which are disclosed by Hshieh 384 and Hirler as discussed above.

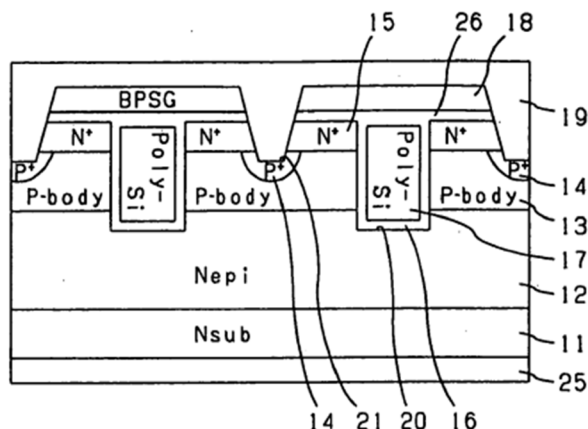
253. Hshieh 384 teaches Claim 9 based on the same evidence and analysis as described above for Claims 5 and 6. *Supra* X.K.5, 6.

M. Claim 1 is Anticipated by Takemori

1. Claim 1

a) [1.pre]. “A trench MOSFET with a trench source contact, comprising:”

254. To the extent the preamble is limiting, Takemori discloses a trench MOSFET with a trench source contact. Figure 3, reproduced below, shows a semiconductor device with a source trench 21. *See* Ex. V, Takemori at [0098].



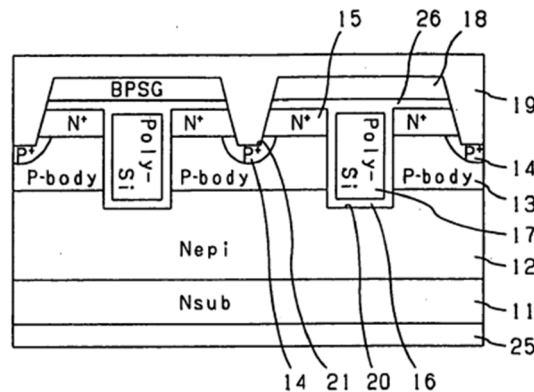
Takemori, Figure 3

- b) [1.a]. “a semiconductor region having a drain region, a body region and a source region, comprising, a silicon substrate, an epitaxial layer corresponding to said drain region disposed on the top of said silicon substrate, a base layer corresponding to said body region disposed on the top of said epitaxial layer, and a source layer corresponding to said source region disposed on the top of said base layer;”

255. Takemori discloses claim 1.a as shown in Figure 3 above. Takemori discloses a drain region comprising a silicon substrate and an epitaxial layer. Takemori teaches that the semiconductor device disclosed in Takemori “forms a drain layer in the form of N⁻-type epitaxial layer 12 on one of the primary sides of N⁺-type silicon substrate 11.” *Id.* at 15:33-35. Takemori further discloses a body region comprising a body region disposed on top of the epitaxial layer. A “P-type body layer 13 is formed on N⁻-type epitaxial layer 12.” *Id.* at 15:35-36. Takemori also discloses a source region comprising a source layer disposed on the base layer. Takemori teaches that an “N⁺-type source region 15 is formed over the range of a fixed depth from the surface of P-type body layer 13.” *Id.* at 15:36-38.

- c) [1.b]. “a front metal layer formed on the upper surface of said semiconductor region”

256. Takemori discloses a front metal layer formed on the upper surface of the semiconductor region. Takemori teaches that “source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18.” *Id.* at 16:27-28. As shown in Figure 3 below, this places the front metal layer 19 on the upper surface of the semiconductor region.



Takemori, Figure 3

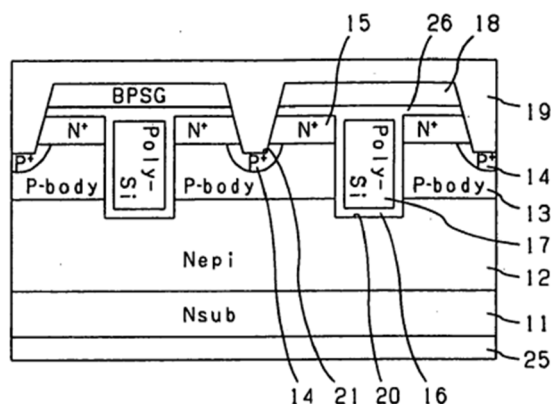
d) [1.c]. “an interlayer oxide film formed between said source layer and said front metal layer;”

257. Takemori discloses an interlayer oxide film formed between the source layer and the front metal layer as shown in Figure 3 above. Takemori teaches that “insulating film 26 is formed so as to cover gate insulating film 16, gate electrode film 17 and the surface of N⁺-type source region 15. Insulating film 26 is a silicon oxide film.” *Id.* at 15:49-41. In addition, Takemori teaches that “a different insulating film in the form of BPSG film 18 is formed on the surface of insulating film 26.” *Id.* at 15:54-56. Further, Takemori teaches that “source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18.” *Id.* at 27-28.

e) [1.d]. “a bottom metal layer formed on the lower surface of said semiconductor region;”

258. Takemori discloses a bottom metal layer formed on the lower surface of the semiconductor region. As shown in Figure 3 below, Takemori teaches that “source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18. Moreover, drain electrode

film 25 is formed on the other side of N⁺-type silicon substrate 11. Furthermore, source electrode film 19 and drain electrode film 25 are preferably formed using, for example, Al—Si or Al—Si—Cu.” *Id.* at 16:28-32.



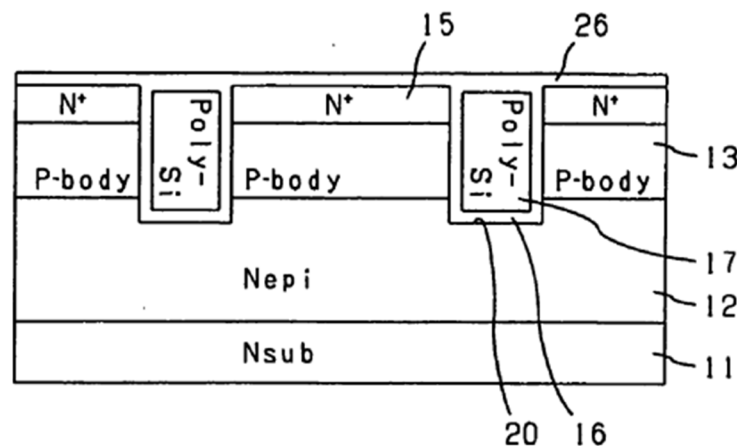
Takemori, Figure 3

f) [1.e]. “a plurality of trenched gates covered by said interlayer oxide film are formed on top of said source layer extending downwardly through said base layer to a portion of said epitaxial layer; and”

259. Takemori teaches Claim 1.e. Takemori discloses a plurality of trenched gates covered by the interlayer oxide film. Takemori teaches that “P-type body layer 13 is opened at predetermined intervals to alternately form gate trench 20 and source trench 21. Gate trench 20 is formed so that its tip section reaches to a comparatively shallow site of N⁻-type epitaxial layer 12.” *Id.* at 15:39-43. “In addition, insulating film 26 is formed so as to cover gate insulating film 16, gate electrode film 17 and the surface of N⁺-type source region 15.” *Id.* at 15:48-51.

260. Takemori teaches a plurality of trenched gates that are formed by etching from above through the epitaxial layer, the upper portions of which are formed into the base and source layer. As illustrated by Figure 9 below, Takemori teaches that the process of forming a trench-type gate electrode structure includes “first forming N⁻-type epitaxial layer 12 by epitaxial growth on the surface of N⁺-type silicon substrate 11. Next, a silicon oxide film not shown is formed on N⁻-type epitaxial layer 12. Next, a predetermined site in this silicon oxide film is opened by etching

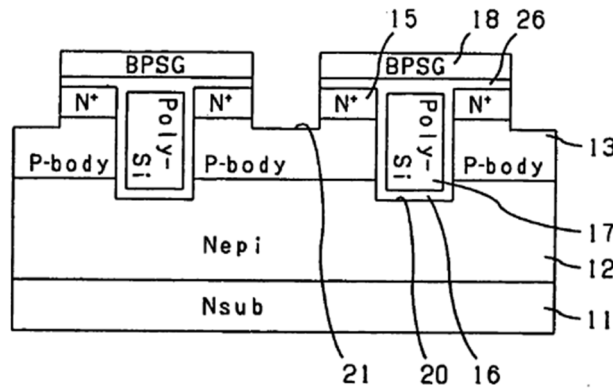
to expose N⁻-type epitaxial layer 12, after which this N⁻-type epitaxial layer 12 is opened by etching to form gate trench 20. Next, after removing the aforementioned silicon oxide film, gate insulating film 16 is formed so as to cover the surface of gate trench 20. Moreover, gate electrode film 17 is deposited and formed on the surface of gate insulating film 16 and on the surface of N⁻-type epitaxial layer 12 followed by removing gate electrode film 17 on the surface of N⁻-type epitaxial layer 12 by etching. Furthermore, in the aforementioned manufacturing process, the formation of P-type body layer 13 and N⁺-type source region 15 may also be carried out prior to forming a silicon oxide film not shown on N-type epitaxial layer 12.” *Id.* at 17:8-21.



Takemori, Figure 9

g) [1.f]. “a plurality of source contact trenches formed on the top of said interlayer oxide film extending downwardly through said source layer to a portion of said base layer”

261. Takemori discloses a plurality of source contact trenches that are formed from above the interlayer oxide film and extend through the source layer into a portion of the base layer. “[E]tching is performed to P-type body layer 13 using BPSG film 18 and insulating film 26 as masks to form source trench 21.” *Id.* at 17:47-49. As shown in FIG. 12, reproduced below, source contact trench 21 extends through source region 15 and into P-type body layer 13.



Takemori, Figure 9

h) [1.g]. “wherein the sidewalls of said trenches in said base layer are covered by the lateral contact layer;”

262. Takemori discloses sidewalls of source contact trenches that are covered by the lateral contact layer. As shown in Figure 2A below, Takemori discloses a buried P⁺-type diffusion region. “The buried P⁺-type diffusion region 14 is formed so as to be exposed on the bottom surface of source trench 21.” *Id.* at 15:64-65.

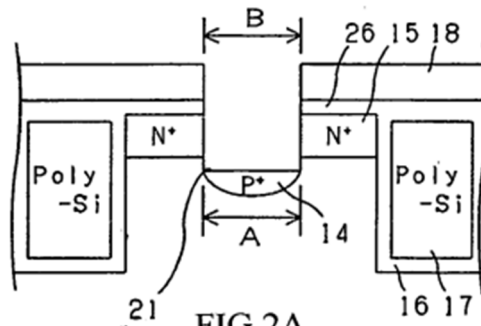
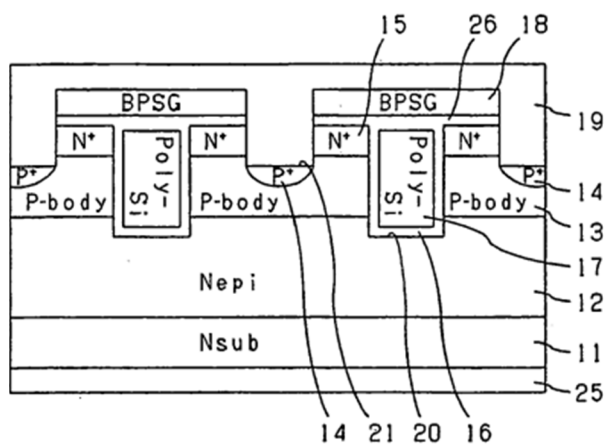


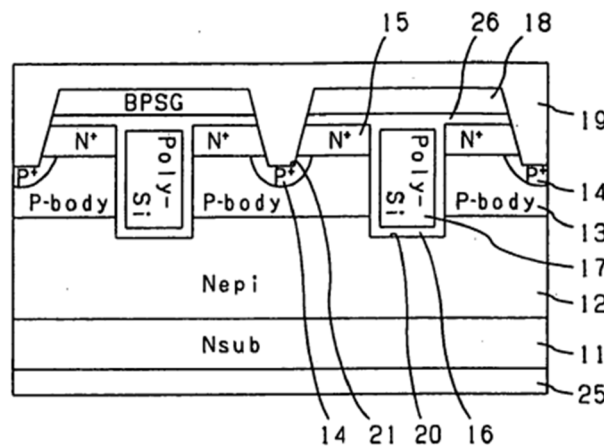
FIG. 2A
Takemori, Figure 2A

263. “[T]he width A of buried P⁺-type diffusion region 14 is made to be roughly the same as width B of the opening of source trench 21.” In addition, Takemori teaches that, other than the source trench, constituents of the embodiments shown in Figures 3-6 are the same as those shown in Figure 1, reproduced below. *Id.* at 18:61-63; 19:14-15; 19:29-31; 19:45-46.

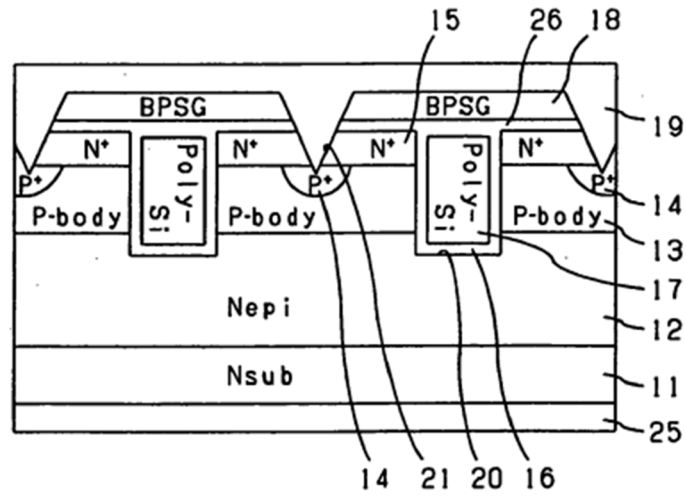


Takemori, Figure 1

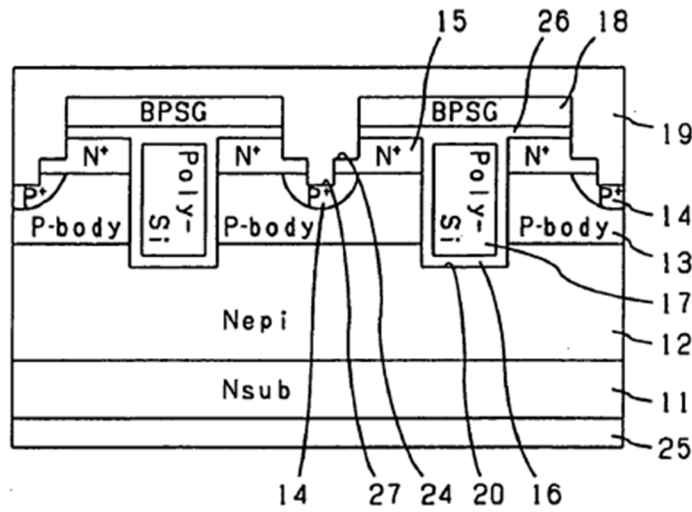
264. As shown in Figures 3-6, reproduced below, when applied to the different shapes for the source contact trench 21, the P⁺-type diffusion region covers not only the bottom surface of the source contact trench within the P-type body layer 13 but also the sidewalls therein. The P⁺-type diffusion region encompasses the entire sidewalls of the source contact trench within the base layer.



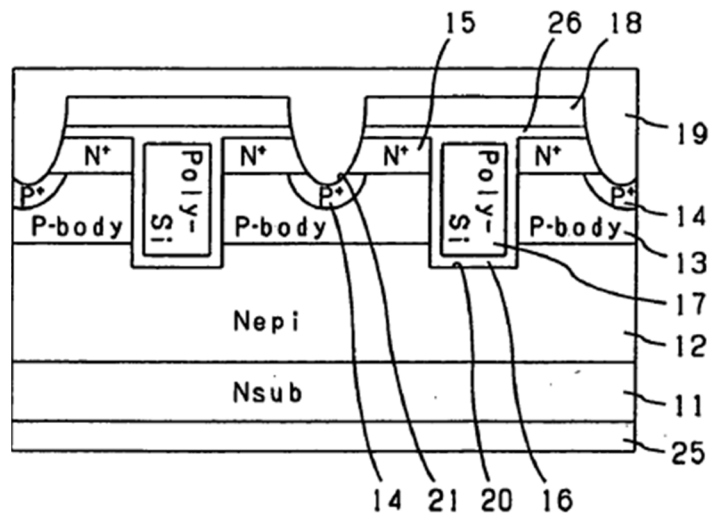
Takemori, Figure 3



Takemori, Figure 4



Takemori, Figure 5



Takemori, Figure 6

i) [1.h]. “wherein the bottom base of said trenches in said base layer are covered by the base contact layer.”

265. Takemori teaches Claim 1.h based on the same evidence and analysis as described above for Claim 1.g. *Supra* X.M.1(h).

N. Claims 2-9 Are Unpatentable as obvious over Takemori in View of Hirler and Hshieh 384

1. Motivation to Combine

266. I contend that it would have been obvious to a POSITA, prior to the effective filing date of the '634 Patent (February 23, 2008), to combine Takemori, Hshieh 384, and Hirler in such a way that one would arrive at the subject matter of Claims 2-9, rendering those claims invalid.

267. Specifically, a POSITA would have been motivated to combine the lateral contact layer of Hirler, which has less doping concentration than the base contact layer at the bottom of the source contact trench, with the trenched MOSFET disclosed in Hshieh 38, obtaining a reasonable likelihood of success that they arrive at the subject matter of claims 2-9. Takemori further teaches the motivation for such combinations in its disclosure of issues surrounding shifting threshold voltage. Threshold voltage, which describes the voltage at which the transistor can be “shut off,” is a well-known concept for a POSITA. If threshold voltage can be maintained with greater precision within MOSFETs on a wafer, as taught by Takemori, it directly increases the yield of circuitry on that wafer using that MOSFET. Therefore, a POSITA is strongly motivated to combine the method of Takemori, which prevents variation in threshold voltage, with Hirler and Hshieh 384.

268. The '634 Patent, Takemori, Hshieh 384, and Hirler are all analogous art seeking to solve similar problems. The '634 Patent, Takemori, Hshieh 384, and Hirler are all in the same field of endeavor, i.e., Vertical Power MOSFET structures. All are directed towards solving similar performance problems. The '634 Patent is directed to the problem of “parasitic N+/P/N” causing

breakdowns in trench MOSFETs. Ex. C, '634 Patent, at 1:35-41. Takemori is directed to the problem of shifting threshold voltage. Ex. V, "Takemori", at 2:1-37. Hsieh 384 is directed to the problem of "limited avalanche current due to the concerns of inadvertent triggering parasitic N+PN bipolar parasitically exists between the source disposed next to the P-body with the P-body further adjacent to the N-epitaxial layer" among others. Ex. X, "Hsieh 384" at [0008]. Finally, Hirler is directed to the problem of breakdowns caused by parasitic bipolar as well. Ex. I, Hirler at [0002].

269. Additionally, the '634 Patent relates to "a trench MOSFET with trench source contact." *See* Ex. C, '634 Patent. Takemori specifically relates to "a semiconductor device having the constitution of a power MOSFET." *See* Ex. V, "Takemori". Hsieh 384 specifically relates to a "trenched metal oxide semiconductor field effect transistor (MOSFET) cell." *See* Ex. X, "Hsieh 384". Hirler specifically discloses a "MOS power transistor arrangement having a vertical transistor structure." *See* Ex. I, Hirler at [0001].

270. A POSITA would have been motivated to combine the lateral contact layer of Hirler, which has less doping concentration than the base contact layer at the bottom of the source contact trench, and the Ti/TiN barrier layer of Hsieh 384 that surrounds a tungsten core as a source-body contact metal with the trench MOSFET disclosed in Takemori to arrive at the subject matter of claims 2-9 of the '634 Patent. A POSITA would commonly know that the use of a barrier metal layer, made of materials such as Ti and TiN, would promote the adhesion of the tungsten contact plug. The Ti and TiN barrier layer also prevents unwanted elements, such as fluorine from the deposition process of W, from seeping into the underlying silicon surface, which would degrade the performance of the transistor. The CVD W deposition process commonly uses WF_6 as a constituent gas to obtain good conformal coverage, and the deposition of metallic W from WF_6 leaves residual fluorine, which can reduce the activation level of other dopants in silicon.

The inclusion of TiN as a barrier is commonly included in the W deposition sequence, preventing the diffusion of fluorine into the underlying doped silicon layers.

271. Therefore, the combination of Takemori, Hshieh 384, and Hirler renders obvious Claims 2-9.

2. Claim 2

272. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Takemori as discussed above.

a) [2.a]. “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are N-type;”

273. Takemori teaches Claim 2.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* X.M.1(b).

b) [2.b]. “the base layer and lateral contact layer are P-type;”

274. Takemori teaches Claim 2.b based on the same evidence and analysis as described above for Claim 1.g. *Supra* X.M.1(h).

c) [2.c]. “and each of the source contact trenches further has a P-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

275. Hirler teaches Claim 2.c based on the same evidence and analysis as described above for Claim 2.c. *Supra* X.F.2(c).

276. Hshieh 384 also teaches Claim 2.c based on the same evidence and analysis as described above for Claim 2.c. *Supra* X.K.2(c).

3. Claim 3: “The trench MOSFET of Claim 2, wherein further comprises a barrier metal layer and a plurality of contact metal plugs.”

277. Claim 3 is dependent on Claim 2, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

278. Hshieh 384 teaches Claim 3 based on the same evidence and analysis as described above for Claim 3. *Supra* X.K.3.

4. Claim 4: “The trench MOSFET of Claim 3, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

279. Claim 4 is dependent on Claim 3, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

280. Hshieh 384 teaches Claim 4 based on the same evidence and analysis as described above for Claims 3 and 4. *Supra* X.K.3-4.

5. Claim 5: “The trench MOSFET of Claim 4, wherein the source contact trench is selected from one of a vertical shape and a taper shape.”

281. Claim 5 is dependent on Claim 4, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

282. Hshieh 384 teaches Claim 4 based on the same evidence and analysis as described above for Claim 5. *Supra* X.K.5.

283. Takemori also teaches Claim 4 based on the same evidence and analysis as described above for Claim 1.g. *Supra* X.M.1(h).

6. Claim 6: “The trench MOSFET of claim 1, wherein the silicon substrate, the epitaxial layer, and the source layer are P-type; the base layer and lateral contact layer are N-type; and each of the source contact trenches further has a N-type base contact layer at a bottom thereof, and the lateral contact layer has less doping concentration than the base contact layer at bottom.”

284. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Takemori as discussed above.

285. Hshieh 384 teaches Claim 6 based on the same evidence and analysis as described above for Claim 6. *Supra* X.K.6.

7. Claim 7: “The trench MOSFET of claim 6, wherein further comprises a barrier metal layer and contact metal plugs.”

286. Claim 7 is dependent on Claim 6, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

287. Hshieh 384 teaches Claim 6 based on the same evidence and analysis as described above for Claims 3 and 6. *Supra* X.L.3, 6.

8. Claim 8: “The trench MOSFET of claim 7, wherein the barrier metal layer is Ti/TiN and the contact metal plug is Tungsten.”

288. Claim 8 is dependent on Claim 7, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

289. Hshieh 384 teaches Claim 8 based on the same evidence and analysis as described above for Claims 4 and 6. *See* Sections X.K.4, 6.

9. Claim 9: “The trench MOSFET of claim 8, wherein the source contact trench is selected from one of a vertical shape and a tapered shape.”

290. Claim 9 is dependent on Claim 8, the elements of which are disclosed by Takemori, Hirler, and Hshieh 384 as discussed above.

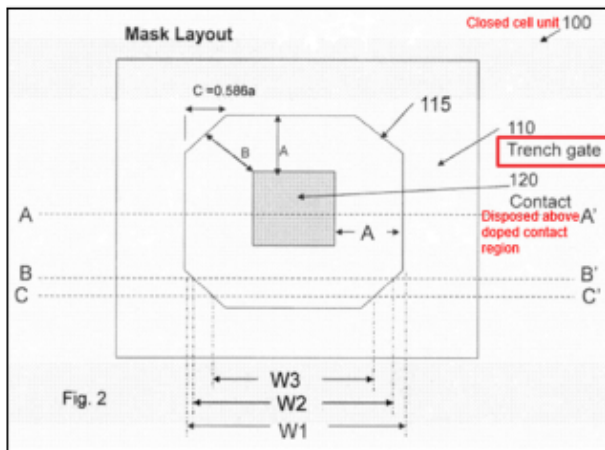
291. Hshieh 384 teaches Claim 9 based on the same evidence and analysis as described above for Claims 5 and 6. *Supra* X.K.5, 6.

XI. THE ASSERTED CLAIMS OF THE '409 PATENT ARE ANTICIPATED OR RENDERED OBVIOUS

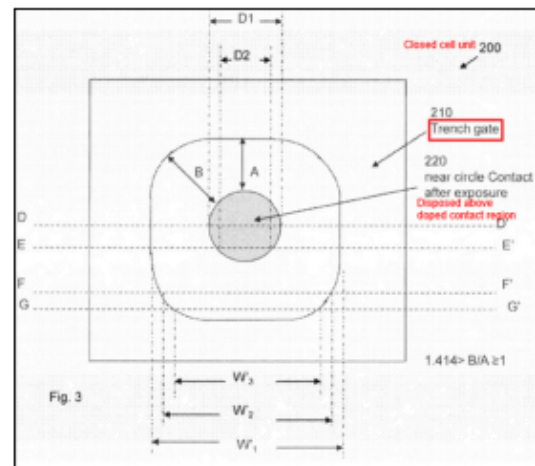
A. Overview of the '409 Patent

292. The '409 Patent relates to a trench semiconductor power device. Ex. D, '409 Patent at 1:7-13 (“This invention relates generally to the cell structure, device configuration and fabrication process of power semiconductor devices.”). The '409 Patent states in the “Description of the Related Art” that trench semiconductor power devices already existed in products and disclosures. *Id.* at 1:14-17. This type of semiconductor structure was well-known in the art and to the POSITA at the time of filing date of the '409 Patent (December 4, 2006).

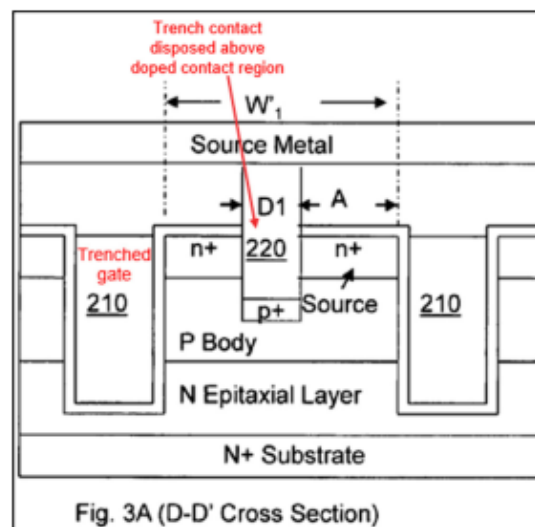
293. The '409 Patent discloses a trenched semiconductor power device with a “closed cell unit” 200/100 of a MOSFET device, which includes a trenched gate 210/110 surrounding a metal contact 220/120. The metal contact 220/120 is disposed above a doped contact region, as shown below in Figures 2, 3, and 3A of the '409 Patent. *Id.* at 4:4-7.



'409 Patent, Figure 2 (annotated)



'409 Patent, Figure 3 (annotated)

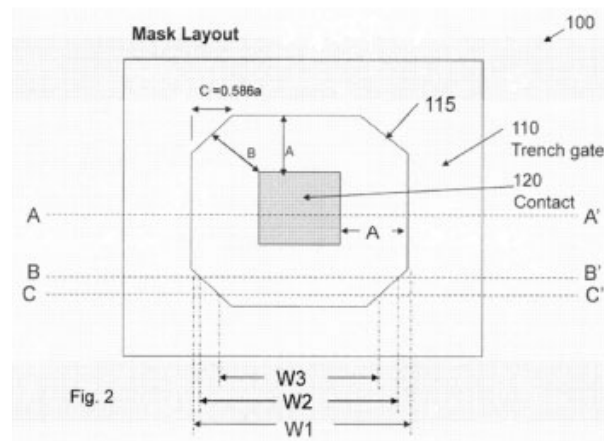


'409 Patent, Figure 3A (annotated)

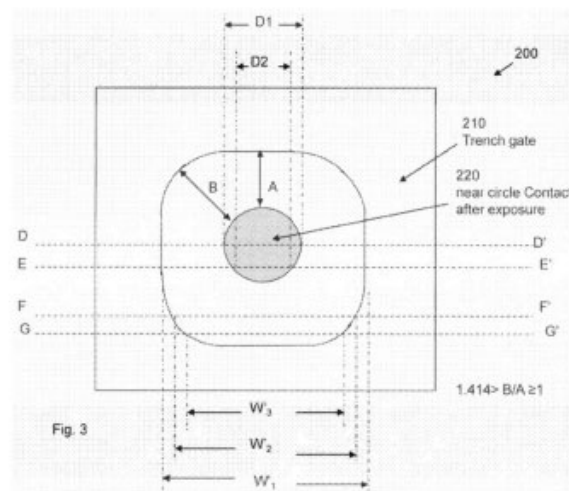
12

¹² The annotations on these figures were originally used to support the Petition for *Inter Partes* Review of the '409 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0094). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

294. The '409 Patent discloses closed cells with substantially square-shaped cells with truncated corners. *Id.* at 4:57-62, Fig. 2. The “truncated corners are formed by design layout not process.” *Id.* During the lithography process, the truncated corners naturally become rounded from exposure. *Id.* (“It is by nature that truncated corners in layout as that shown in FIG. 2 and becomes rounded as shown in FIG. 3.”). Figure 3 also shows that the square contact 120 of Figure 2 naturally becomes a circular shaped contact 220 as a result of exposure. *Id.* at 4:53-57.



'409 Patent, Figure 2

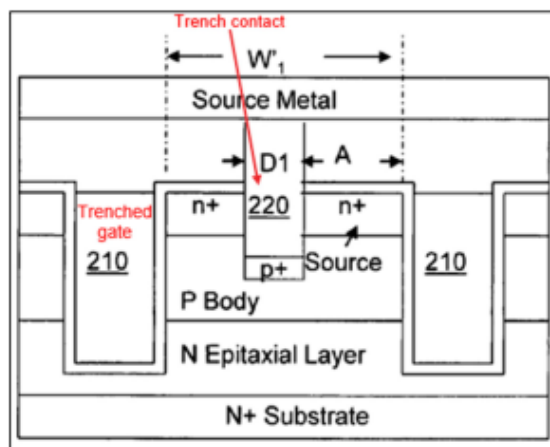


'409 Patent, Figure 3

13

¹³ The annotations on these figures were originally used to support the Petition for *Inter Partes* Review of the '409 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0094). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

295. The '409 Patent discloses a circular trench contact 220 that is “extended into the body region through the source region of the closed semiconductor power cell” and is “in contact with a p+ contact dopant region disposed immediately below the [circular] trench contact.” *Id.* at 4:25-33, Fig. 3A. Meanwhile, the trenched gates 210 and the gate oxide lining of the trenched gates 210 are disposed at a distance away from the circular trench contact 220. *Id.* The source and body regions are disposed between the gate oxide lining and all circumferential points of the circular trench contact 220. *Id.* The source and body regions are in contact with the circular trench contact 220. *Id.*



'409 Patent, Figure 3A (annotated)

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296. Finally, the circular trench contact 220 is filled with a contact metal plug that is connected to a source metal. *Id.* at Figure 3A, 5:26-7; *see also id.* at Fig. 1C.

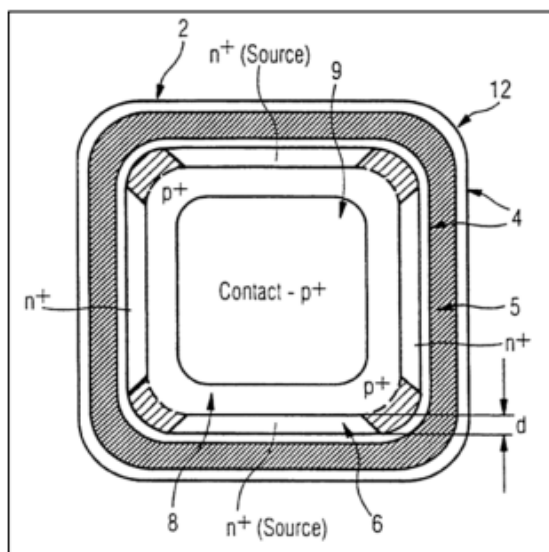
B. The '409 Patent File History

297. U.S. Patent Application No. 11/633,366 (the “’366 Application”), titled “TRENCH MOSFET WITH CELL LAYOUT, RUGGEDNESS, TRUNCATED CORNERS,” was filed on December 4, 2006 and issued as the '409 Patent on October 12, 2010. Ex. D, '409 Patent at Cover;

¹⁴ The annotations on these figures were originally used to support the Petition for *Inter Partes* Review of the '409 Patent, filed by Inergy Technology, Inc. (Inter Partes Review No. IPR2024-0094). I have considered the annotations here and find them to be technically accurate and useful as inclusions in this report.

Ex. G, 409 FH at FORCE-MOS0000250. The '366 Application was initially filed with eighteen claims with Fu-Yuan Hsieh as the inventor. *Id.* at FORCE-MOS0000 235-38. In response to an office action mailed on October 6, 2008, claims 14-18 were withdrawn. *Id.* at FORCE-MOS0000264.

298. The '366 application received its first rejection on January 26, 2009, rejecting all pending claims for anticipation and obviousness. *Id.* at FORCE-MOS0000275-86. In response, the applicant amended claim 1 to include a square shaped closed cell with rounded corners and a circular trench contact disposed in the center of the closed cell. Claim 13, which issued as Claim 6 in the '409 Patent, was also amended to include truncated corners and a circular trench contact. *Id.* at FORCE-MOS0000305. These amendments were made to overcome U.S. Patent No. 6,541,818 ("Pfirsch"). Applicant admitted that Pfirsch disclosed "a closed cell with square trench gate with rounded corner [2] and square contact with rounded corner [9]." *Id.* Figure 2 of Pfirsch is reproduced below for reference.



Pfirsch, Figure 2

299. The '366 application received its first final office action on July 15, 2009, rejecting all pending claims for indefiniteness and obviousness. *Id.* at FORCE-MOS0000315-24. In

response, the applicant amended the claims to include a circular trench contact disposed at a distance away from a gate oxide lining of a trench gate from all circumferential points of the circular trench contact. *Id.* at FORCE-MOS0000338. This amendment was made to overcome U.S. Patent Pub. No. 2022/0006703 (“Pfirsch 703”), in view of U.S. Patent No. 6,867,083 (“Iman”).

300. The ’366 application received another office action on January 10, 2010, rejecting all pending claims for obviousness. *Id.* at FORCE-MOS0000355-64. In response, the applicant amended Claim 1 to further include a circular trench contact comprising a hole opened from a top surface of a semiconductor surface, sidewalls surrounded by and in contact source and body regions, and source and body regions disposed between the hole and trenched gates and claim 5, which issued as Claim 2 in the ’409 Patent, to further include a contact resistance reduction metal layer disposed above a contact metal plug and below a bottom surface of a source metal. *Id.* at FORCE-MOS0000369-71. This amendment was made to overcome Pfirsch 703 in view of the U.S. Patent No. 6,621,107 (“Blanchard”). *Id.* at FORCE-MOS0000358.

301. The ’409 Patent issued on October 12, 2010. *Id.* at FORCE-MOS0000395.

302. The ’409 Patent expired on October 12, 2018 due to non-payment of the 7.5 year maintenance fees. *Id.* at FORCE-MOS0000422. Four years later, on July 12, 2022, the applicant petitioned for acceptance of delayed payment of maintenance fees. *Id.* at FORCE-MOS0000405-09. This petition was dismissed for failure to meet petition requirements. *Id.* At FORCE-MOS0000432-34. Subsequently, the applicant submitted a second petition. *Id.* at FORCE-MOS0000442-47. The second petition was also dismissed for (1) failure to meet petition requirements and (2) nonpayment of the 11.5 Year maintenance fee. *Id.* at FORCEMOS-0000488-94. The applicant then submitted a third petition. This petition was also dismissed for (1) failure

to meet petition requirements and (2) non-payment of the 11.5 Year maintenance fee. The applicant submitted a fourth petition on February 14, 2023. This petition was granted on May 24, 2023.

C. The Asserted Claim

303. My understanding is that Force MOS has asserted Claim 1 of the '409 Patent. I have reproduced that claim below.

Claim 1:

[1.pre] A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:

[1.a] said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;

[1.b] each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;

[1.c] said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug wherein sidewalls of said hole are surrounded by and in contact said source and body regions and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates and all circumferential points of the circular trench contact; and

[1.d] said contact metal plug connected to a source metal disposed on top of said circular trench contact.

D. Priority Date of the '409 Patent

304. I understand that Force MOS claims the earliest priority date for the '409 Patent is December 4, 2006, the filing date of U.S. Patent Application Serial No. 11/633,366.

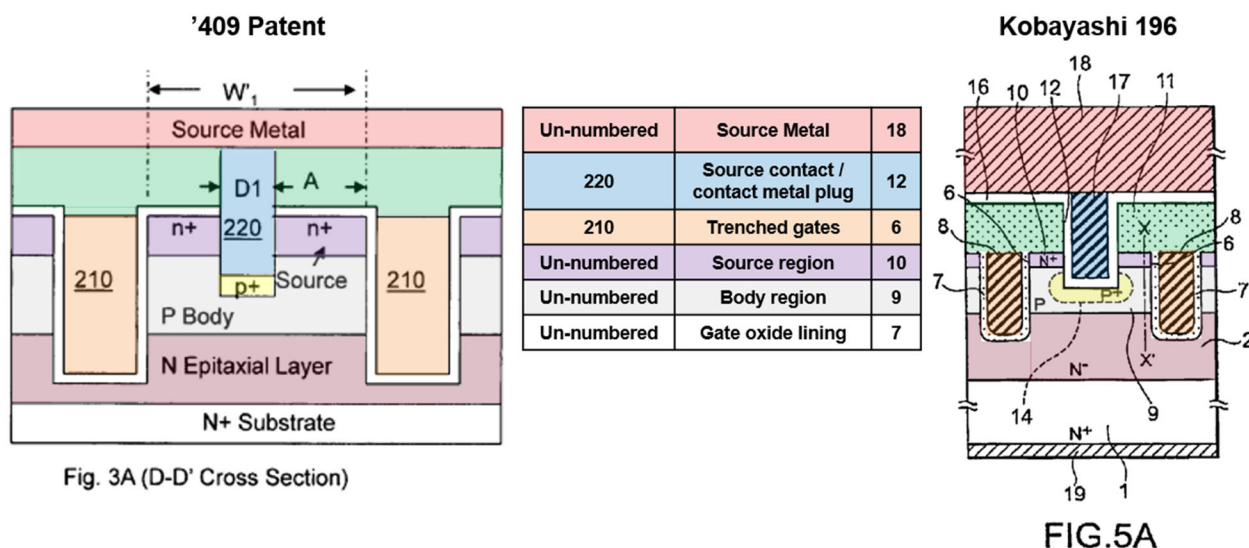
E. Overview of the Prior Art Relied Upon

305. I have relied on the following prior art in my invalidity analysis of the '409 Patent.

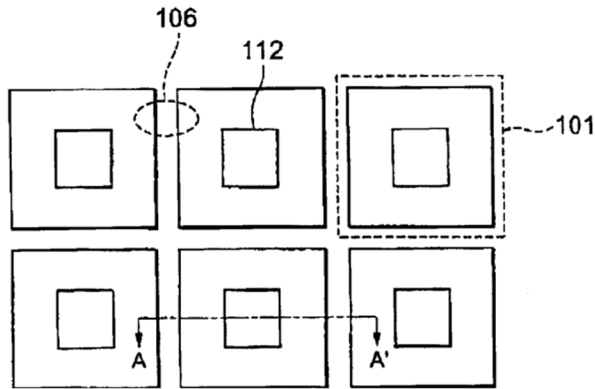
1. U.S. Patent No. 6,888,196 (“Kobayashi 196”)

306. U.S. Patent No. 6,888,196 to Kobayashi (“Kobayashi 196”) issued on May 3, 2005. Because Kobayashi 196 issued more than one year prior to the ’409 Patent’s priority date – December 4, 2006 – it is prior art to the ’409 Patent at least under pre-AIA 35 U.S.C. § 102(b). Ex. L, Kobayashi 196 at Cover. Kobayashi 196 was not considered during the prosecution of the ’409 Patent.

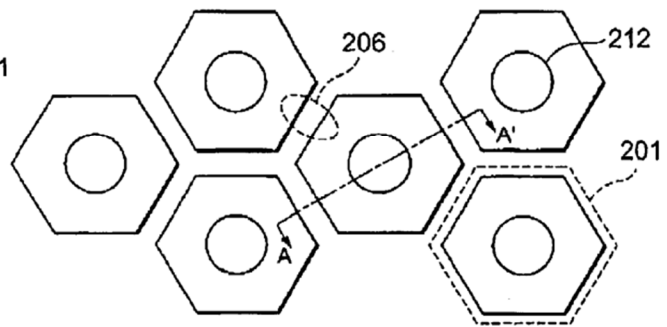
307. Kobayashi 196 discloses a trench semiconductor power device. *Id.* As shown below in the comparison of Figure 3A from the ’409 patent and Figure 5A from Kobayashi 196, Kobayashi 196 teaches a MOSFET device similar to that of the ’409 patent.



308. Kobayashi 196 further discloses various cell layouts of the semiconductor device. For example, as shown below, Figure 3A discloses a plurality of square cells with square contacts that are arranged in a matrix. *Id.* at 6:26-27. Figure 4A discloses a plurality of hexagonal cells with circular contacts. *Id.* at 6:29-30.

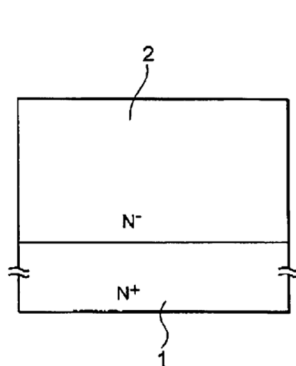


Kobayashi 196, Figure 3A

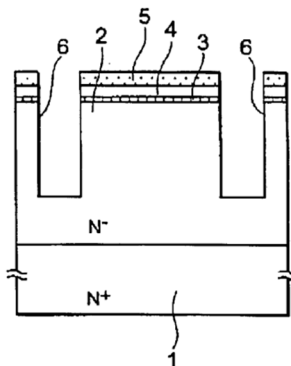


Kobayashi 196, Figure 4A

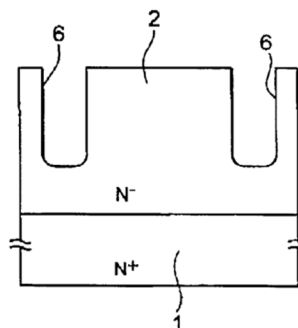
309. Kobayashi 196 also teaches the manufacturing process of trench gates as illustrated in Figures 6A-C, reproduced below. Kobayashi teaches that first an epitaxial layer is grown on a silicon substrate. *Id.* at 7:21-23. Next, a composite film of oxide film 3, nitride film 4, and oxide film 5 is sequentially deposited by CVD and then patterned by photolithography. *Id.* at 7:34-40. The composite film is used as a mask for silicon etching that forms the trenches 6 in the epitaxial layer. *Id.* at 7:40-55.



Kobayashi 196, Figure 6A

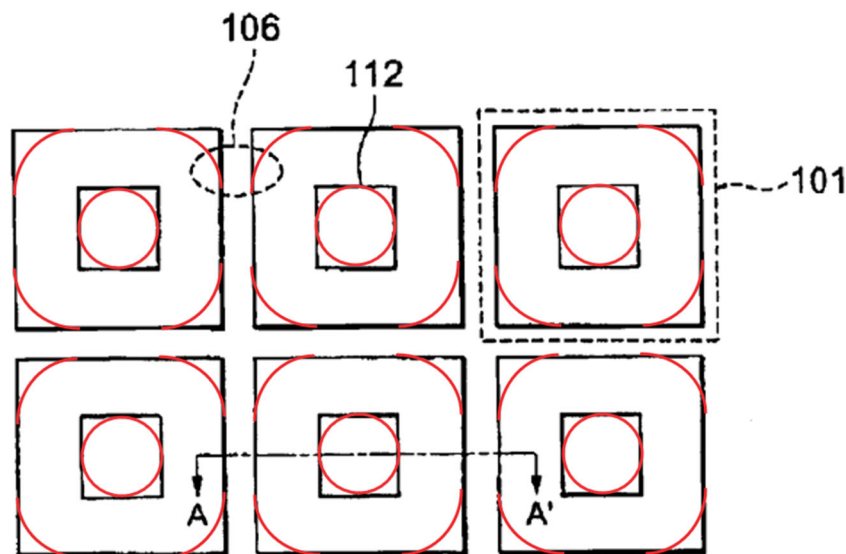


Kobayashi 196, Figure 6B



Kobayashi 196, Figure 6C

310. “[A]fter the composite film is removed by etching, corners of each trench 6 at the bottom are rounded. In this event, corners of each trench 6 at an opening portion may also be rounded.” *Id.* at 7:57-60. As a result, the corners of the cell layout seen from the top view will be rounded as shown below in annotated Figure 3A.



Kobayashi 196, Figure 3A (annotation added)

2. U.S. Patent No. 5,763,914 (“Hshieh 914”)

311. U.S. Patent No. 5,763,914 to Hshieh et al. (“Hshieh 914”) was issued on June 9, 1998. Ex. M, Hshieh 914 at Cover. Because Hshieh 914 issued more than one year prior to the ’409 Patent’s priority date – December 4, 2006 – it is prior art to the ’409 Patent at least under pre-AIA 35 U.S.C. § 102(b). *Id.* Hshieh 914 was not considered during the prosecution of the ’409 Patent.

312. Hshieh 914 discloses trenched semiconductor power devices. Hshieh 914 teaches various cell layouts including non-orthogonal parallelogram, regular square, rectangular, and hexagonal shapes. *Id.* at 4:35-38. Figure 8A is reproduced below as an example.

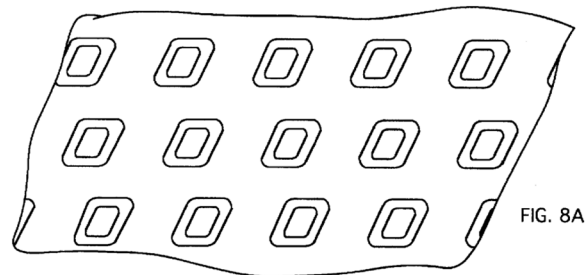


FIG. 8A

Hshieh 914, Figure 8A

313. Hshieh 914 further teaches a “trenched power transistor cell supported on a semiconductor substrate.” *Id.* at 7:45-48; *see id.* at 7:26-8:5 (“Figures 10A and 10B are the top view and cross sectional view of a power device 200 which include an array of trenched MOSFET cells 204. Each of these cells 204 includes a trenched gate 225 surround by a source region 240 which are in source contact 270. A deeper p-body region 230 surrounds the source region and extends outwardly toward the outer boundary of the transistor cell. The trenched gate 225 includes a trench opened in the substrate and filled with a dielectric material such as polysilicon.”)

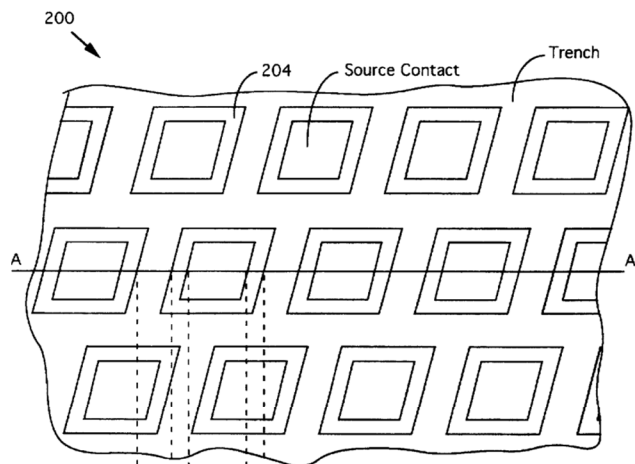


FIG. 10A

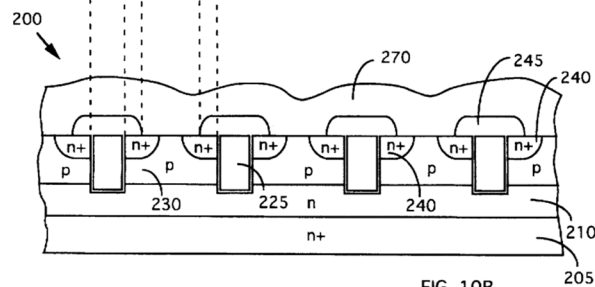


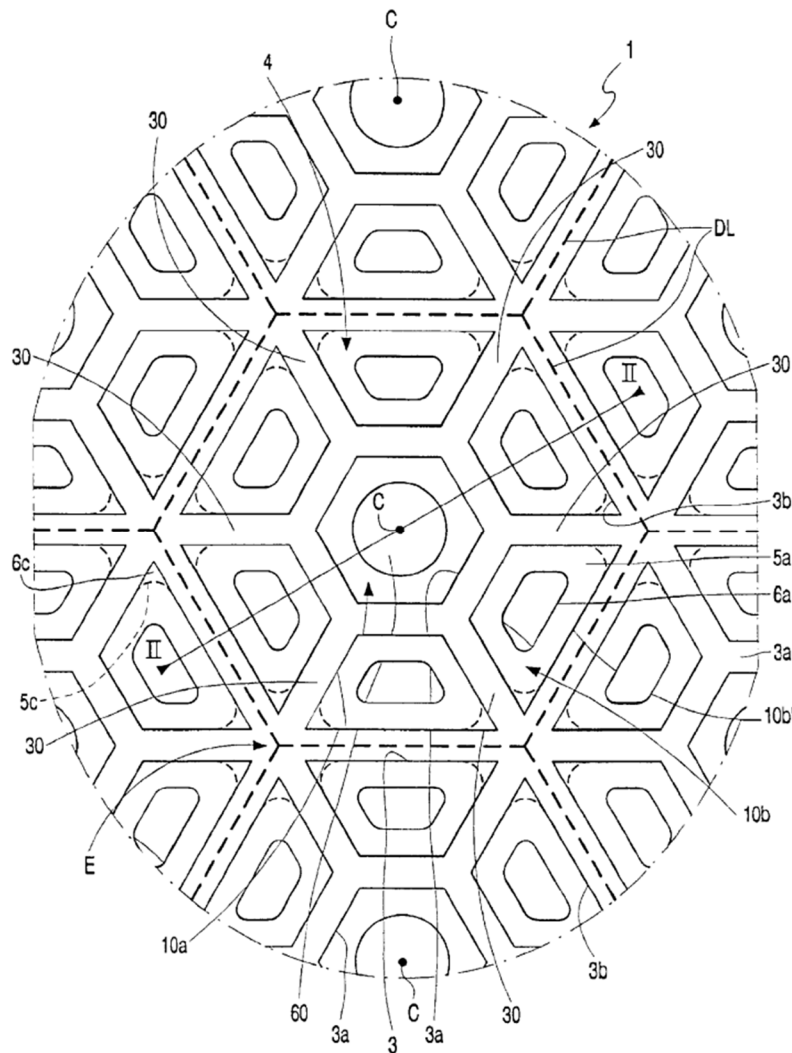
FIG. 10B

Hshieh 914, Figures 10A-B

3. U.S. Patent No. 6,320,223 (“Hueting”)

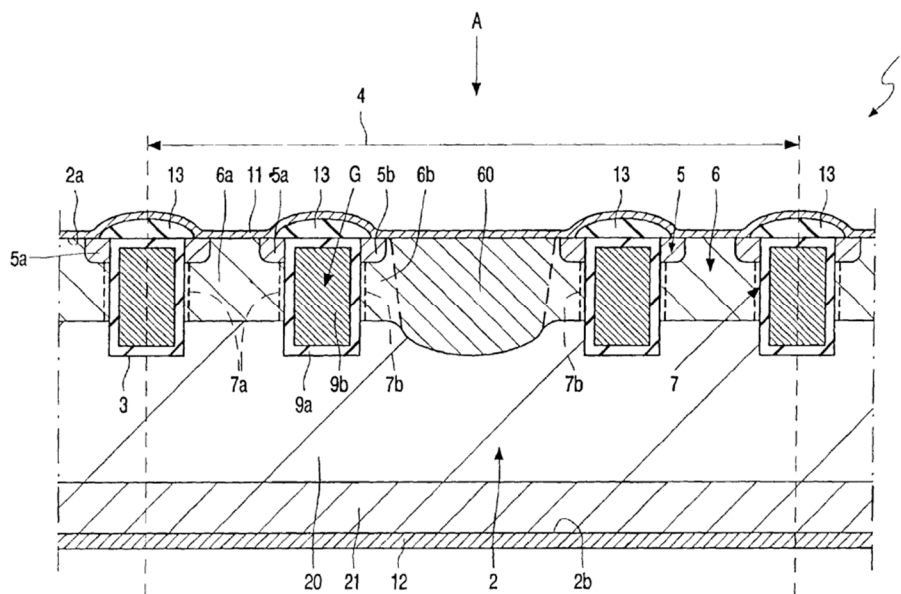
314. U.S. Patent No. 6,320,223 to Hueting et al. (“Hueting”) was issued on November 20, 2001. Ex. N, Hueting at Cover. Because Hueting issued more than one year prior to the ’409 Patent’s priority date – December 4, 2006 – it is prior art to the ’409 Patent at least under pre-AIA 35 U.S.C. § 102(b). Hueting was not considered during the prosecution of the ’409 Patent.

315. Hueting discloses trench gate field effect device. Hueting teaches a regular array of polygonal source cells. *Id.* at 2:16-31. Figure 1, reproduced below, shows an array of polygonal unit cells 4 that are each bounded by trenched gates 3.



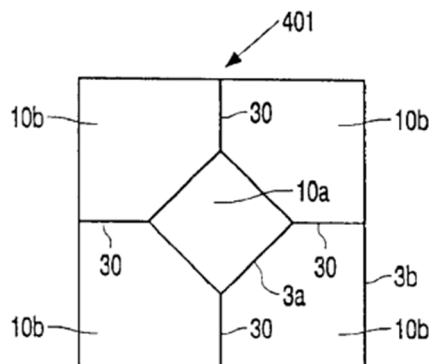
Hueting, Figure 1

316. As shown in Figure 2 below, each polygonal unit cell 4 comprises a source region 5, a body region 6 having a different type of conductivity than the source region 5, trench gates 3, and contact regions 60.



Hueting, Figure 1

317. Hueting further discloses square configurations for the trench boundaries 3a and 3b. *Id.* at 11:44-49. For example, Figure 6 below, shows a unit cell with a square layout. *Id.* Hueting teaches that “sharp angles between the edges of the outer trench boundary are undesirable because of the likelihood of high fields occurring at the sharp corners.” *Id.* at 11:62-65. In addition, Hueting teaches that “the inner trench boundaries 3a in FIGS. 6 to 11 may be circular as discussed above and need not necessarily be polygonal.” *Id.* at 12:35-37.

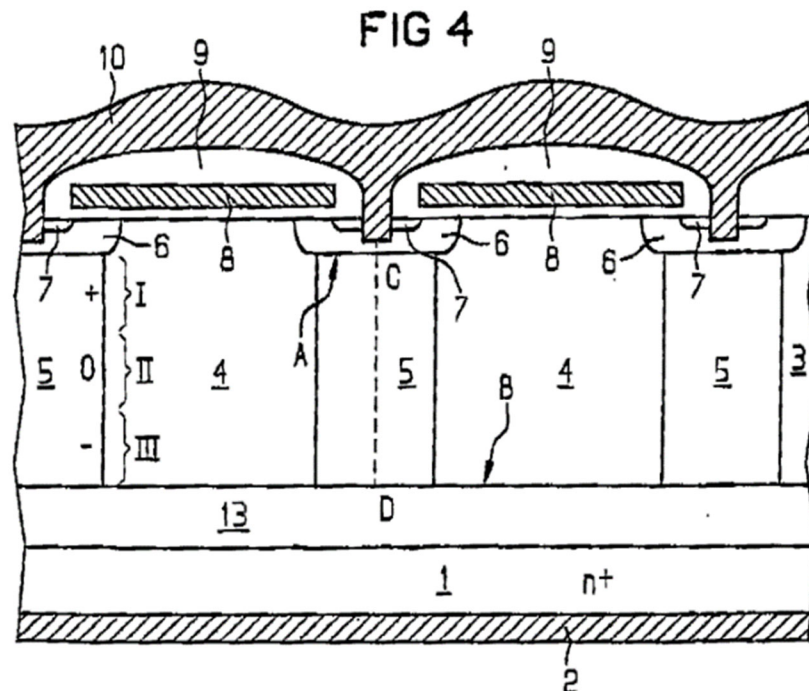


Hueting, Figure 6

4. U.S. Patent No. 6,630,698 (“Deboy”)

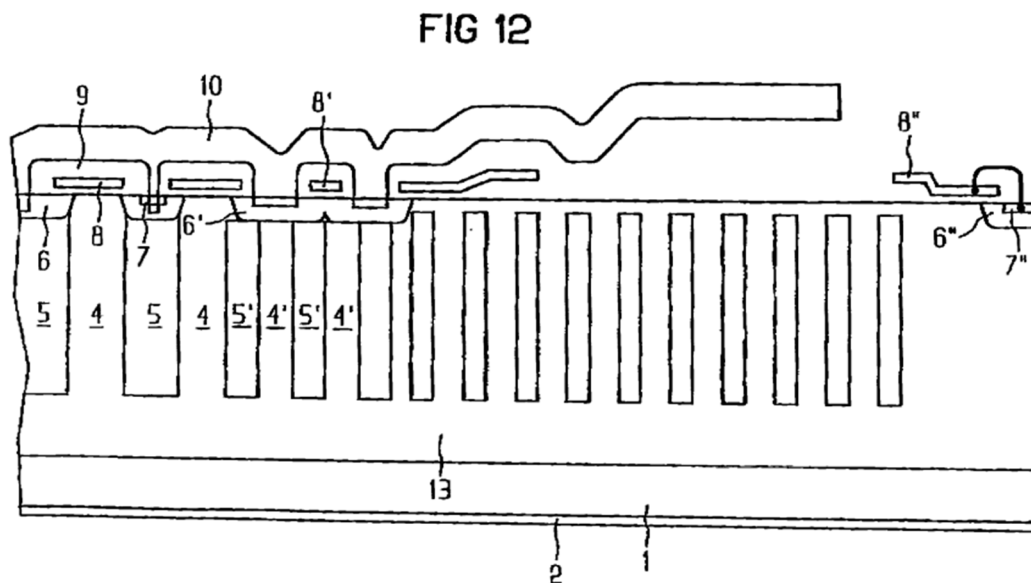
318. U.S. Patent No. 6,630,698 to Deboy et al. (“Deboy”) was issued on October 7, 2003. Ex. O, Deboy at Cover. Because Deboy issued more than one year prior to the ’409 Patent’s priority date—December 4, 2006—it is prior art to the ’409 patent at least under pre-AIA 35 U.S.C. § 102(b). Deboy was not considered during the prosecution of the ’409 Patent.

319. Deboy discloses trenched semiconductor power devices. *Id.* at 1:17-22. Figure 4, reproduced below, shows a cross-section through an exemplary n-channel MOS transistor. *Id.* at 8:47-49. The transistor comprises “an n^+ -conductive silicon semiconductor substrate 1, a drain electrode 2, a first n-conductive layer 13, the second layer 3 with n-conductive areas 4 and p-conductive areas 5, p-conductive zones 6, n-conductive zones 7, gate electrodes 8 made, for example, from polycrystalline silicon or metal, which are embedded in an isolating layer 9 made, for example, from silicon dioxide, and a source metalization 10 made, for example, from aluminum.” *Id.* at 10:5-12.



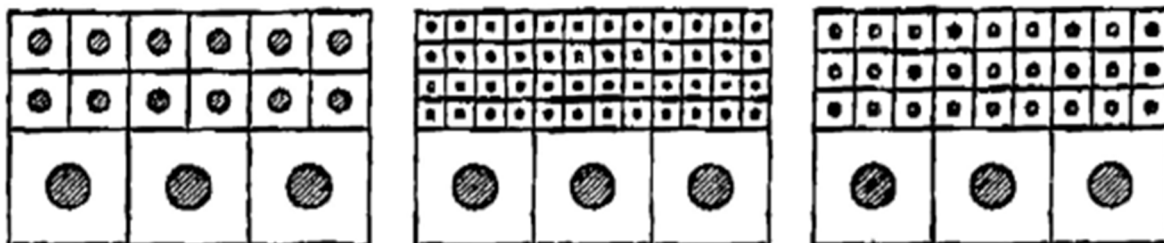
Deboy, Figure 4

320. Figure 12, reproduced below, shows another exemplary n-channel MOS transistor with an edge structure layout. *Id.* at 8:65-67.



Deboy, Figure 12

321. As shown in Figures 9A-C below, Deboy further teaches square-shaped cell layouts with circular contact zones with varying widths for the floating zones.



Deboy, Figures 9A-C

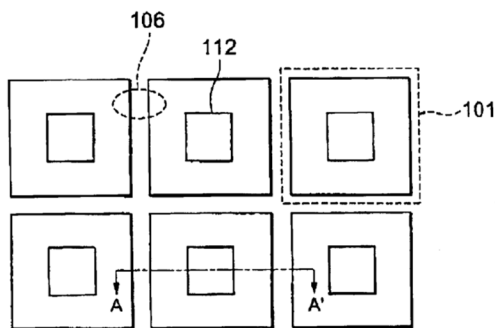
F. Claim 1 Is Unpatentable as Anticipated by Kobayashi 196

1. Claim 1

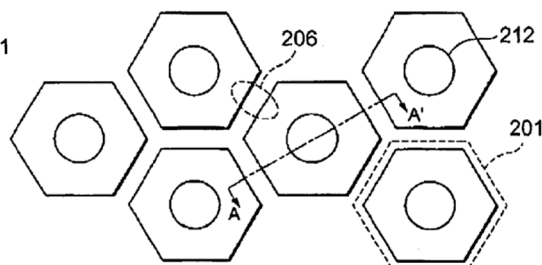
a) [1.pre]. "A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:"

322. Kobayashi 196 discloses a trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate. The vertical MOSFET disclosed in Kobayashi 196 comprises "a unit cell formed in a

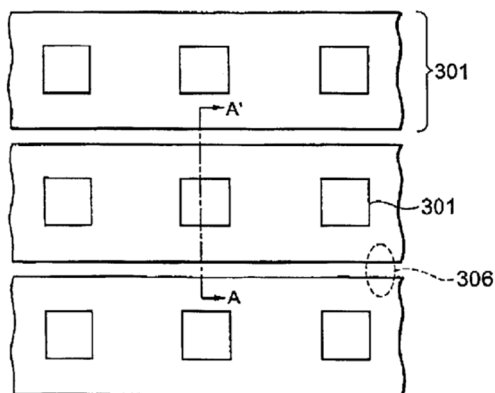
region of the semiconductor layer surrounded by the trench gates.” Ex. L, Kobayashi 196 at 4:12-33. The trench gates are formed in trenches form on a surface of the semiconductor layer. *Id.* Figures 3A, 4A, and 4B, reproduced below, show “unit cells 101, 201, and 301 [where] each figure can be defined as structural units separated by trenches 106, 206, and 306 where gate electrodes are to be formed.” *Id.* at 6:51-56.



Kobayashi 196, Figure 3A



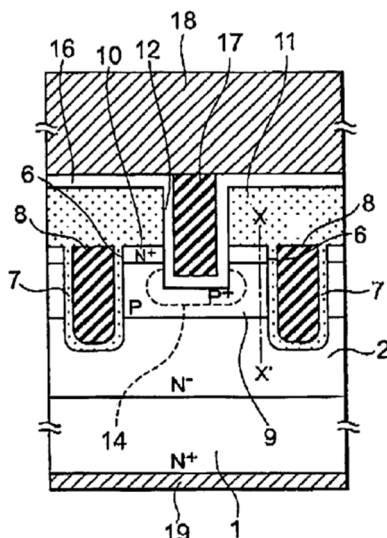
Kobayashi 196, Figure 4A



Kobayashi 196, Figure 4A

323. Figure 5A, also reproduced below, further shows the cross section along the line A-A' shown in Figures 3A, 4A, and 4B. The cross section shows a plurality of trenched gates surrounding a transistor cell formed in a semiconductor substrate. *See id.* at 6:51-60 (“A combination of the substrate 1 and the layers 2, 9, and 10 constitutes a silicon layer having Silicon Surface opposite to each other. In each of trenches 6 reaching the N-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled. On the polysilicon 8 to serve as a gate electrode or a trench gate, an interlayer oxide film 11 is formed. Between the trench

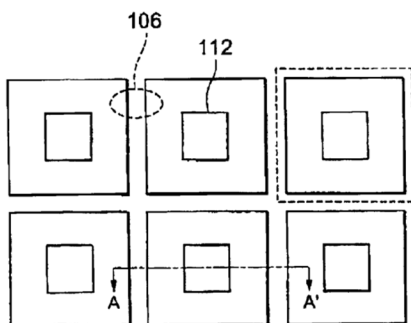
gates adjacent to each other, a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 through the N'-type source layer 10.”)



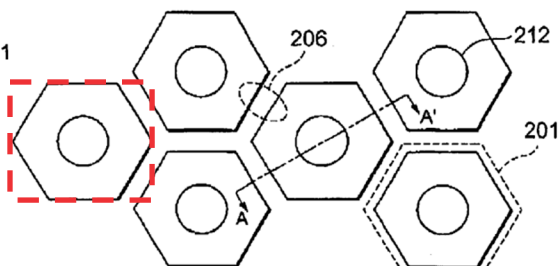
Kobayashi 196, Figure 5A

b) [1.a]. “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

324. Kobayashi 196 discloses trenched gates surrounding transistor cells as closed cells constituting substantially square-shaped cells with rounded corners. As shown in Figure 3A below, “a plurality of square cells are arranged in a matrix.” *Id.* at 6:27; *see also id.* at 6:51-56 (“unit cells 101, 201, and 301 in each figure can be defined as structural units separated by trenches 106, 206, and 306 where gate electrodes are to be formed.”) Kobayashi 196 also discloses square-shaped cells with truncated corners. *Id.* at Figure 4A.



Kobayashi 196, Figure 3A



Kobayashi 196, Figure 4A (annotation added)

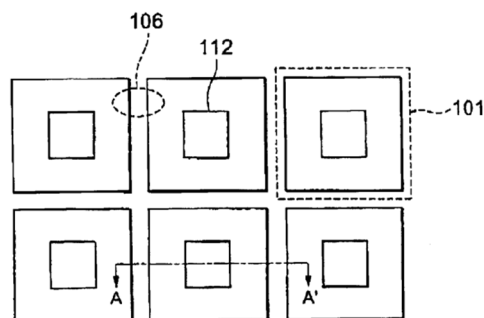
A diagram showing a 2x3 grid of squares. The top row consists of three squares. The first square has a dashed circle around its top edge, labeled 106. The second square has a label 112 pointing to its top edge. The third square is enclosed in a dashed rectangular border, labeled 101. The bottom row consists of three squares. The first square has a downward-pointing arrow labeled A. The second square is enclosed in a solid blue rectangular border. The third square has a downward-pointing arrow labeled A'. A horizontal dashed line connects the arrow A to the arrow A'.

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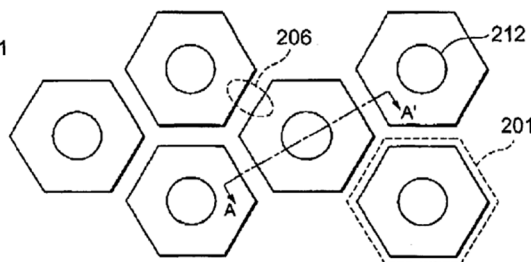
326. Furthermore, when a feature is designed having corners in a MOSFET design layout, as provided in Kobayashi, it would be readily apparent to a POSITA that the resulting corners would become rounded. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing the photolithography. Accordingly, the corners of a closed transistor cell that is non-circular in design layout become rounded as a natural result of the photolithography process.

c) [1.b]. “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”

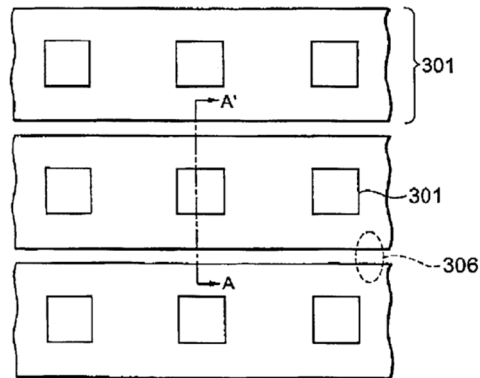
327. Kobayashi 196 discloses a circular trench contact disposed substantially in the central portion of closed cells, penetrating through a source region surrounding trenched gates and extending into a body region encompassing said source region. Figures 3A, 4A, and 4B, reproduced below, each show “At the centers of unit cells 101, 201, and 301, contact holes 112, 212, and 312.” *Id.* at 6:35-36. Kobayashi 196 teaches that “The contact holes may have any desired shape, such as a square shape, a hexagonal shape, an octagonal shape, and a *circular shape*.” *Id.* at 6:37-39 (emphasis added). Kobayashi 196 further teaches that “If the contact hole is sufficiently small, the contact hole has a generally circular shape without any angle.” *Id.* at 6:39-41. As an example, Figure 4A shows a circular trench contact disposed substantially in a central portion of closed cells.



Kobayashi 196, Figure 3A

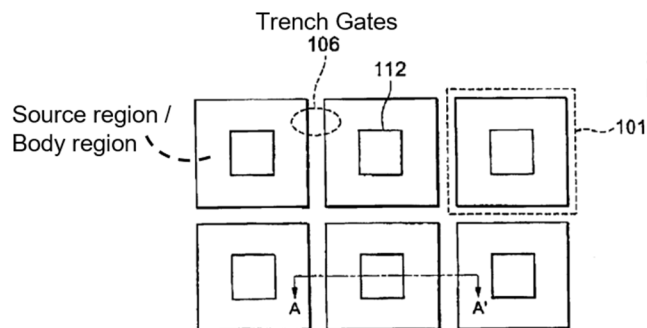


Kobayashi 196, Figure 4A

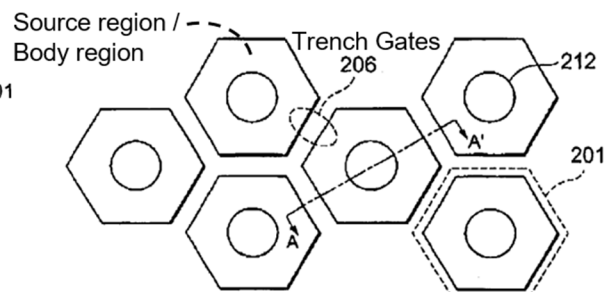


Kobayashi 196, Figure 4A

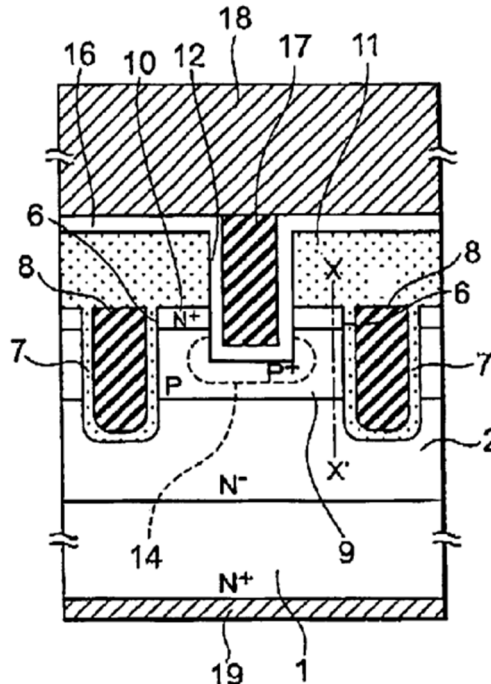
328. Kobayashi 196 further discloses a circular trench contact penetrating through a source region surrounding the trenched gates and extending into a body region encompassing said source region. In Kobayashi 196's vertical MOSFET, "A P-type base layer 9 and an N^+ -type source layer 10 are formed on a surface of the N^- -type epitaxial layer 2." *Id.* at 6:49-51. "A contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 *through the N^+ -type source layer 10.*" *Id.* at 6:58-60 (emphasis added). As shown in the annotated Figures 3A and 4A below, a source region surrounds the trenched gates. Furthermore, Figure 5A shows a body region 9 encompassing said source region 10.



Kobayashi 196, Figure 3A



Kobayashi 196, Figure 4A

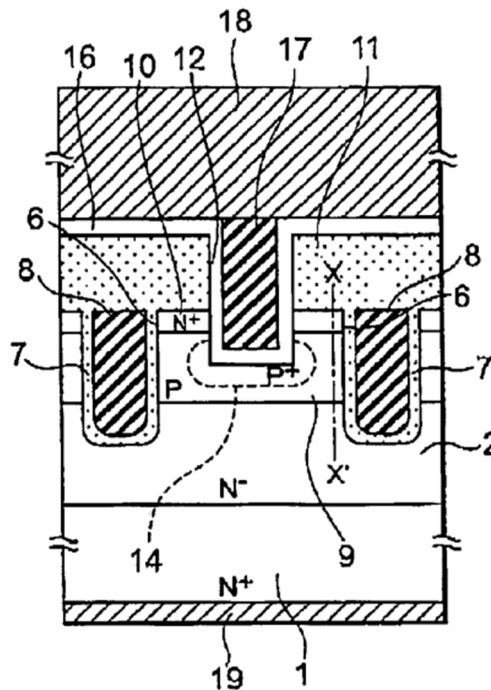


Kobavashi 196, Figure 4A

329. Furthermore, when a source trench contact is designed with a non-circular layout and has minimum feature size, as provided in Kobayashi, it would be readily apparent to a POSITA that the resulting source trench contact would be circular in shape. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing photolithography. When the feature size is small enough, one rounded corner abuts the next rounded corner, resulting in a circular shaped feature. A POSITA would readily appreciate that the source trench contact in Kobayashi is a minimum feature size, and therefore its resulting shape after photolithography would be a circular shape. Accordingly, a source trench contact that is non-circular in design layout becomes circular in shape as a natural result of the photolithography process and the minimum feature size.

d) [1.c]. "said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug"

330. Kobayashi 196 discloses a circular trench contact comprising a hole opened from a top surface of a semiconductor substrate and is filled with a metal plug. A cross section of Kobayashi 196's vertical MOSFET is shown in Figure 5A, reproduced below. The vertical MOSFET of Kobayashi 196 "comprises an N-type silicon Substrate 1 and an N-type epitaxial layer 2 formed on one surface of the N-type silicon substrate 1. A P-type base layer 9 and an N-type source layer 10 are formed on a surface of the N-type epitaxial layer 2. A combination of the substrate 1 and the layers 2, 9, and 10 constitutes a silicon layer having Silicon Surface opposite to each other." *Id.* at 6:47-53. Further, "a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 through the N'-type source layer 10. Directly under the contact hole 12, a barrier metal 16 is deposited to extend onto the interlayer oxide film 11. The contact hole 12, within which the barrier metal 16 is formed, is filled with W 17." *Id.* at 6:58-64.



Kobayashi 196, Figure 4A

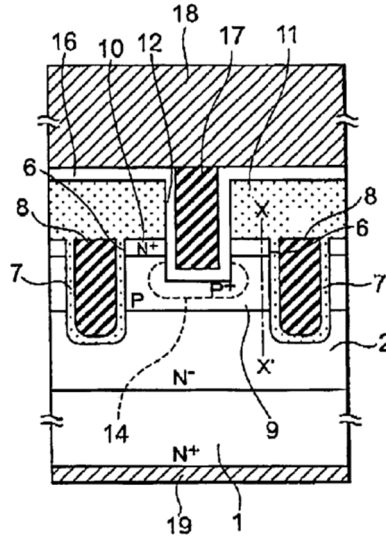
331. Accordingly, Kobayashi 196 teaches claim 1[c].

e) [1.d]. "wherein sidewalls of said hole are surrounded by and in contact said source and body regions"

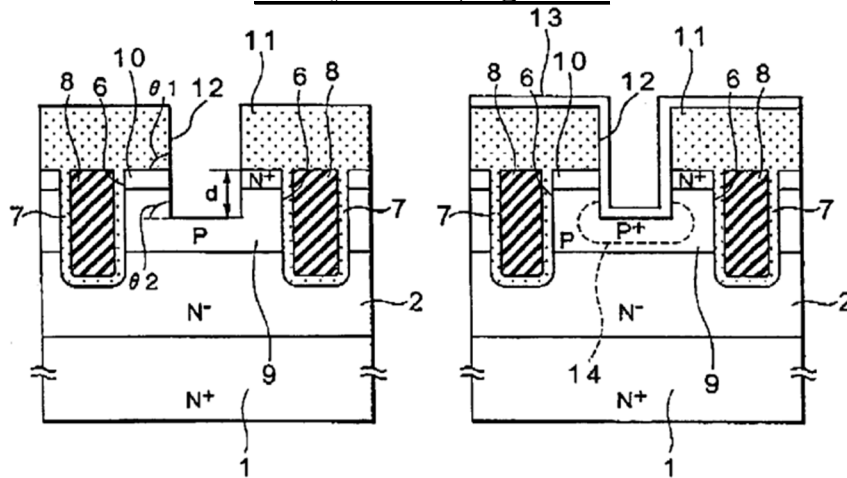
332. Kobayashi 196 discloses a circular contact trench wherein its sidewalls are surrounded by and in contact with source and body regions. As shown in Fig. 5A, reproduced above, “a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 through the N'-type source layer 10.” *Id.* at 6:58-60. Kobayashi 196 further teaches that “The silicon is etched to the depth reaching the P-type base layer 9 through the interlayer oxide film 11 and the N'-type source layer 10. Thus, the contact hole 12 is formed.” *Id.* at 53-55. It follows that, as shown in Figure 5 above, the sidewalls of the contact trench are surrounded by an in contact with source and body regions.

f) [1.e]. “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates at all circumferential points of the circular trench contact;”

333. Kobayashi 196 discloses a circular trench contact that is separate from trenched gates with source and body regions disposed between gate oxide linings of the trenched gates at all circumferential points of the circular trench contact. Figure 5A, reproduced below, shows “[i]n each of trenches 6 reaching the N-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled.” *Id.* at 6:545-56. Kobayashi 196 further teaches that “[b]etween the trench gates adjacent to each other, a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 through the N'-type source layer 10.” *Id.* at 58-60. As shown in Figures 7C and 7D, the resulting circular trench contact 12 is separate from the trenched gates 6 with source regions 10 and body regions 9 disposed between the gate oxide lining 7 of the trenched gates 6.



Kobayashi 196, Figure 5A

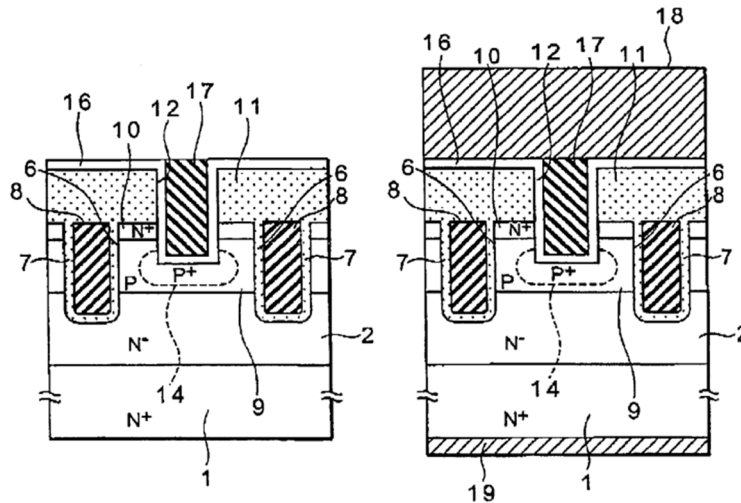


Kobayashi 196, Figure 7C

Kobayashi 196, Figure 7D

g) [1.f]. “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”

334. Kobayashi 196 discloses a contact metal plug connected to a source metal disposed on top of a circular trench contact. Figures 8B and 8C, reproduced below, illustrate the process of forming a contact metal plug in a contact trench and a source metal on top of the contact trench. Kobayashi 196 teaches that “W 17 is deposited by CVD” in the contact trench 12 and “the W 17 is etched back to be left in the contact hole 12 in a plug-like shape.” *Id.* at 9:32-36. Further, “AlSi (aluminum Silicon) or AlSiCu (aluminum copper Silicon) is deposited by sputtering to form the source electrode 18.” *Id.* at 9:36-38.



Kobayashi 196, Figure 8B Kobayashi 196, Figure 8C

G. Claim 1 Is Obvious over Kobayashi 196 in View of Hshieh 914

1. Motivation to Combine

335. A POSITA would have been motivated to combine Kobayashi 196 and Hshieh 914 to arrive at the subject matter of claim 1 of the '409 patent. The '409 patent, Kobayashi 196, and Hshieh 914 are analogous art relating to the same field. The '409 patent relates to semiconductor power device configurations and cell layouts. *See, e.g.*, Ex. D, '409 Patent at 1:7-12. Similarly, Kobayashi 196 relates to “a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size.” Ex. L, Kobayashi 196 at 1:8-10. Hshieh 914 relates to a “MOSFET cell topology.” Ex. M, Hshieh 914 at 2:59-63.

336. Further, the '409 patent, Kobayashi 196, and Hshieh 914 are directed to similar problems. The '409 patent is directed to the problem of “parasitic bipolar NPN latch up” that are “especially pronounced near the trench corners.” Ex. D, '409 Patent at 1:15-20. Similarly, Kobayashi 196 is directed to the problem of “reduc[ing] the on-resistance while maintaining a breakdown voltage of a required level.” Ex. L, Kobayashi 196 at 1:25-28. Hshieh 914 is also directed to the problem of “maintain[ing] a low level of on-resistance” among others. Ex. M, Hshieh 914 at 1:29-34.

337. A POSITA would have been motivated to combine the blunted or rounded corners in unit cell layouts of Hshieh 914 with the vertical MOSFET disclosed in Kobayashi 196 to arrive at the subject matter of claim 1 of the '409 patent. Hshieh 914 expressly teaches the advantages of blunted or rounded corners in square-shaped cell layouts. *See* Ex. M, Hshieh 914 at 2:24-34 (“The three dimensional diffusion effect which often leads to vulnerable punch-through weak points in the corners of a square cell is circumvented by blunting the sharp corners in the square cells. The ninety degree corners of the polysilicon is made blunt by adding a short linear segment and replacing a 90-degree with two 135-degree corners. The cell topology thus renders the three-dimensional diffusion phenomenon less problematic at the corners when the shallow junctions are formed for high density power transistor cells with channel length reduced to a range between 0.5 to 0.75 microns.”). Hshieh 914 discloses that such advantages were already known in the art. *Id.* Further, Hshieh teaches and applies a known technique – truncating the corners in order to achieve rounding. *Id.* As such a POSITA would reasonably expect improved ruggedness and resistance from combining Hshieh 914 and Kobayashi 196.

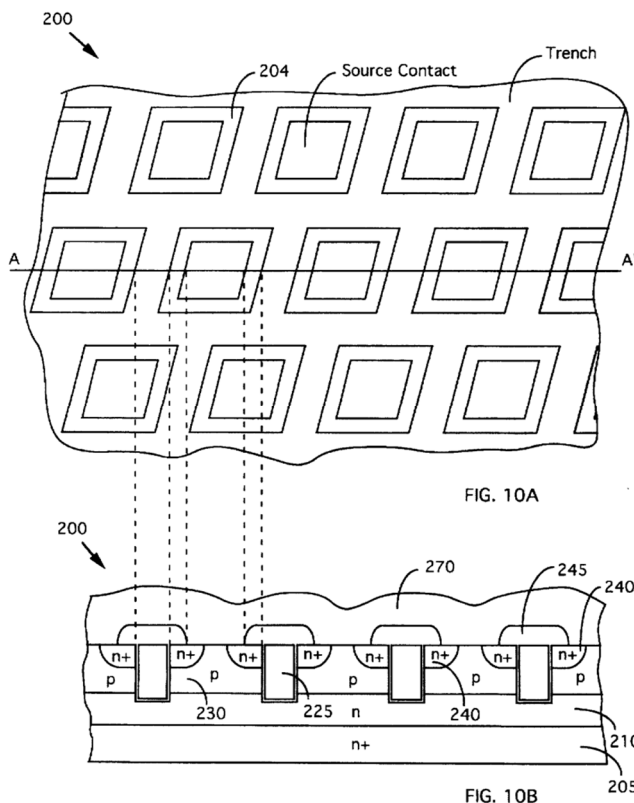
2. Claim 1

a) [1.pre]. “A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”

338. As already explained in Section XI.F.1(a), Kobayashi 196 teaches Claim 1[pre]. I incorporate by reference the same evidence and analysis as described in Section XI.F.1(a) for Claim 1[pre].

339. Hshieh 914 also teaches Claim 1.pre. Hshieh 914 discloses “a power device 200 which include an array of trenched MOSFET cells 204. Each of these cells 204 includes a trenched gate 225 surround by a source region 240 which are in source contact 270. A deeper p-body region 230 surrounds the source region and extends outwardly [sic] toward the outer boundary of the

transistor cell. The trenched gate 225 includes a trench opened in the substrate and filled with a dielectric material such as polysilicon.” *Id.* at 7:27-34. Figures 10A and 10B, reproduced below, show the power device 200.



Hshieh 914, Figure 10A-B

b) [1.a]. “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

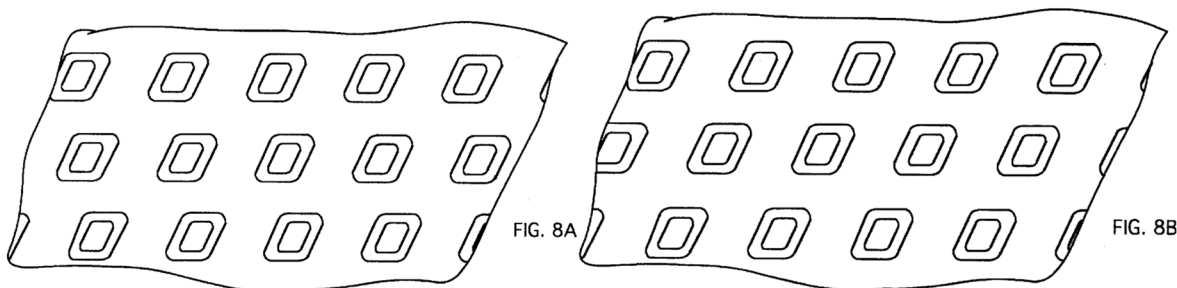
340. As already explained in Section XI.F.1(b), Kobayashi 196 teaches Claim 1.a. based on the same evidence and analysis as described in Section XI.F.1(b).

341. Hshieh 914 also teaches Claim 1.a. Hshieh 914 discloses trenched gates surrounding transistor cells as closed cells constituting substantially square-shaped cells with rounded corners. Hshieh 914 discloses transistor cells with a non-orthogonal parallelogram shape. *Id.* at 4:34-37. Further, “In order to prevent the corner vulnerability where punch through weak points may be formed at the sharp corners due to a three-dimension diffusion effect, similar to that discussed

above in U.S. Pat. No. 5,304,831 by Yilmaz et al., the sharp corners of the polysilicon openings can be either blunted or rounded as that shown in [Figures] 6A and 6B respectively.” *Id.* at 5:3-9. In addition, “[Figures] 8A and 8B illustrate the power devices which include transistor cells of rounded non-orthogonal parallelogram cells arranged respectively in parallelogram centered at lattice points of a hexagonal lattice and parallelogram centered at lattice points of a parallelogram lattice configurations.” *Id.* at 23-28. Figures 6A, 6B, 8A, and 8B are reproduced below.



Hshieh 914, Figure 6A-B



Hshieh 914, Figure 8A-B

342. Furthermore, when a feature is designed having corners in a MOSFET design layout, as provided in Hshieh 914, it would be readily apparent to a POSITA that the resulting corners would become rounded. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing the photolithography. Accordingly, the corners of a closed transistor cell that is non-circular in design layout become rounded as a natural result of the photolithography process.

- c) [1.b]. “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”

343. As already explained in Section XI.F.1(c), Kobayashi 196 teaches Claim 1.b based on the same evidence and analysis as described in Section XI.F.1(c).

d) [1.c]. “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug”

344. As already explained in Section XI.F.1(d), Kobayashi 196 teaches Claim 1.c based on the same evidence and analysis as described in Section XI.F.1(d).

e) [1.d]. “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”

345. As already explained in Section XI.F.1(e), Kobayashi 196 teaches Claim 1.d based on the same evidence and analysis as described in Section XI.F.1(e).

f) [1.e]. “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates at all circumferential points of the circular trench contact;”

346. As already explained in Section XI.F.1(f), Kobayashi 196 teaches Claim 1.e based on the same evidence and analysis as described in Section XI.F.1(f).

g) [1.f]. “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”

347. As already explained in Section XI.F.1(g), Kobayashi 196 teaches Claim 1.f based on the same evidence and analysis as described in Section XI.F.1(g).

H. Claim 1 is Obvious over Kobayashi 196 in View of Hueting

1. Motivation to Combine

348. A POSITA would have been motivated to combine Kobayashi 196 and Hueting to arrive at the subject matter of Claim 1 of the '409 patent. The '409 patent, Kobayashi 196, and Hueting are analogous art relating to the same field. The '409 patent relates to semiconductor power device configurations and cell layouts. *See, e.g.*, Ex. D, '409 Patent at 1:7-12. Similarly, Kobayashi 196 relates to “a vertical MOSFET (Metal Oxide Semiconductor Field Effect

Transistor) reduced in cell size.” Ex. L, Kobayashi 196 at 1:8-10. Hueting relates to “a trench gate field effect device.” Ex. N, Hueting at 2:13.

349. Further, the ’409 patent, Kobayashi 196, and Hueting are directed to similar problems. The ’409 patent is directed to the problem of “parasitic bipolar NPN latch up” that are “especially pronounced near the trench corners.” Ex. D, ’409 Patent at 1:15-20. Similarly, Kobayashi 196 is directed to the problem of “reduc[ing] the on-resistance while maintaining a breakdown voltage of a required level.” Ex. L, Kobayashi 196 at 1:25-28. Hueting is also directed to the problem of providing “rugged[ness] whilst also providing for a reduced specific ON resistance.” Ex. N, Hueting at 2:14-15. The ruggedness of Hueting allows a balance between avoiding parasitic bipolar latchup, which is done by creating additional contact area between the p and p+ regions to suppress base-to-emitter voltage, while still maintaining low specific on-resistance by controlling the amount of contact area displaced from contacting the n+ region. Hueting further uses rounded corners in the layout of source electrodes to reduce gate-source field. *Id.* at 11:25-33. This further enhances the device breakdown voltage.

350. A POSITA would have been motivated to combine the polygonal unit cells, including square-shaped cells, with rounded corners and circular contact regions of Hueting and the vertical MOSFET disclosed in Kobayashi 196 to arrive at the subject matter of claim 1 of the ’409 patent. Hueting expressly teaches and applies various polygonal cell layouts, including square-shaped layouts, and circular contact regions. *See id.* at 11:10-18, 44-47; 12:35-37. Hueting also expressly teaches problems associated with sharp corners and advantages of rounded corners cell layouts. *See id.* at 2:19-43 (“The problem of high fields at the sharp corners in FIG. 1 may be overcome or at least alleviated by modifying the mask used to introduce the source regions 5 so that, as indicated by the dashed lines 5c in FIG.1, source regions 5 do not extend completely into

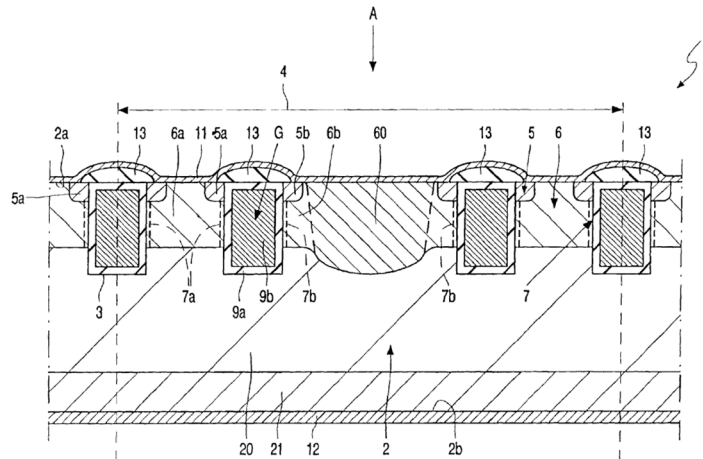
the sharp corners of the peripheral subsidiary source cells 10b. This should avoid or at least reduce the problem of high electric fields at the sharp corners for the loss of a very small amount of the overall channel width.”) As such a POSITA would reasonably expect improved ruggedness and resistance from combining Hueting and Kobayashi 196.

2. Claim 1

a) [1.pre]. “A trench semiconductor power device comprising a plurality of trench gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”

351. As already explained in Section XI.F.2(a), Kobayashi 196 teaches Claim 1[pre]. I incorporate by reference the same evidence and analysis as described in Section XI.F.2(a) for Claim 1.pre.

352. Hueting also teaches Claim 1.pre. Hueting discloses “A trench gate field effect device has a semiconductor body (2) with a trench (3) extending into a first major surface (2a) so as to define a regular array of polygonal source cells (4). Each source cell contains a source region (5a, 5b) and a body region (6a, 6b) with the body regions separating the source regions from a common further region (20). A gate (G) extends within and along said trench (3) for controlling a conduction channel through each of the body regions. Each source cell (4) has a central semiconductor region (60) which is more highly doped than said body regions, is of opposite conductivity type to the further region and forms a diode with the further region.” *Id.* at Abstract. Figure 2 showing the elements discussed above is reproducing below.

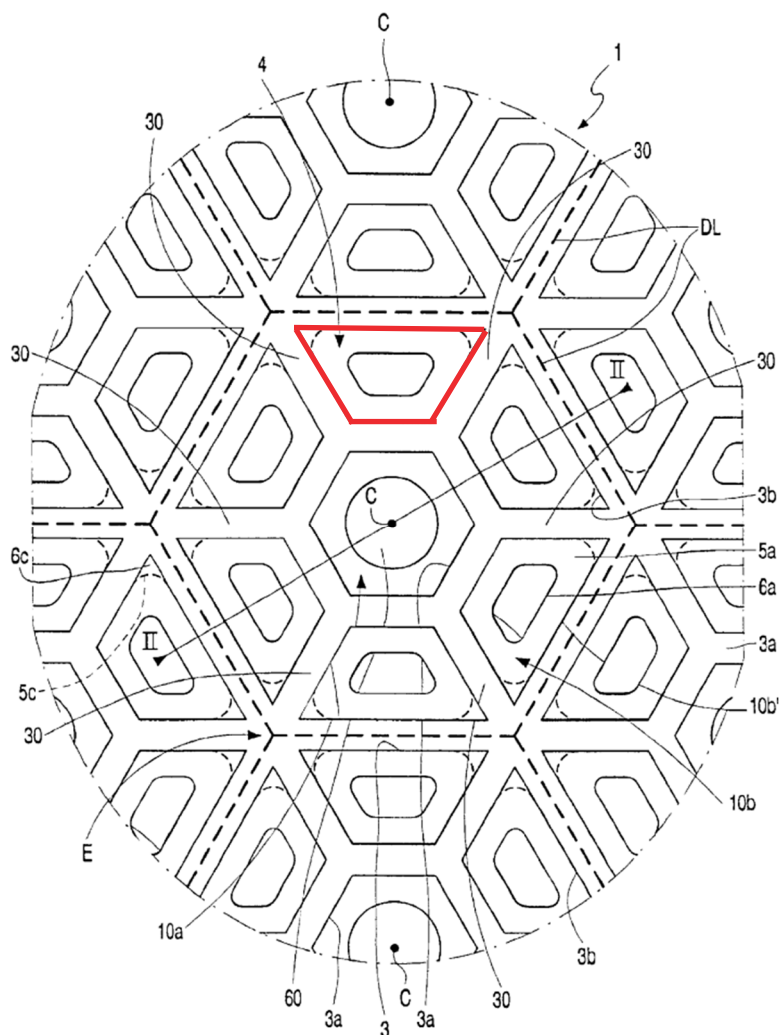


Hueting, Figure 2

b) [1.a]. “said trench gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

353. As already explained in Section XI.F.1(b), Kobayashi 196 teaches Claim 1.a based on the same evidence and analysis as described in Section XI.F.1(b).

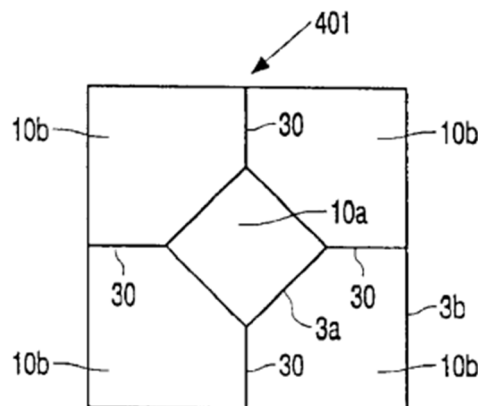
354. Hueting also teaches Claim 1.a. Hueting discloses trench gates surrounding transistor cells as closed cells constituting substantially square-shaped cells with rounded corners. Figure 1, annotated and reproduced below, shows “a regular array of polygonal source or *unit cells* 4 each bounded by the trench 3. *Id.* at 6:11-13 (emphasis added).



Hueting, Figure 1 (annotation added)

355. Hueting teaches various other source or unit cell configurations. *Id.* at 11:45. “[I]n each case, each of the inner and outer trench boundaries 3a and 3b is of square (rectangular) configuration.” *Id.* at 45-47. For example, the unit cell 401 of Figure 6 is reproduced below. Hueting further teaches that “the disadvantage that the sharp angles between the edges of the outer trench boundary are undesirable because of the likelihood of high fields occurring at the sharp corners.” *Id.* at 11:62-65. “[T]he problem of high fields at these sharp corners can be avoided or at least alleviated by shaping the source regions 5 so that they do not extend into the sharp corners.” *Id.* at 12:56-59.

356. Furthermore, when a feature is designed having corners in a MOSFET design layout, as provided in Hueting, it would be readily apparent to a POSITA that the resulting corners would become rounded. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing the photolithography. Accordingly, the corners of a closed transistor cell that is non-circular in design layout become rounded as a natural result of the photolithography process.

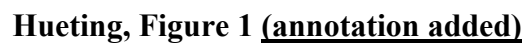


Hueting, Figure 6

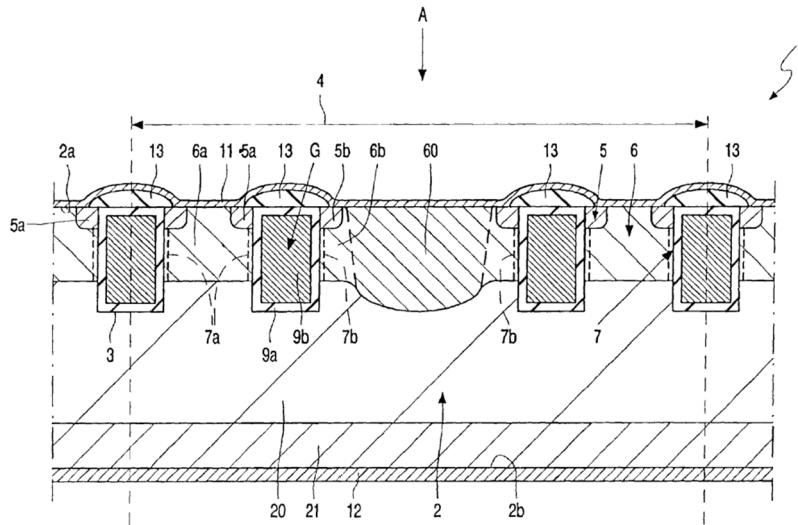
c) [1.b]. “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”

357. As already explained in Section XI.F.1(c), Kobayashi 196 teaches Claim 1.b based on the same evidence and analysis as described in Section XI.F.1(c).

358. Hueting also teaches Claim 1.b. Hueting discloses a circular trench contact disposed substantially in a central portion of closed cells. As shown in Figure 1 below, Hueting discloses a circular, central semiconductor region 60. *Id.* at 6:35.



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360. Furthermore, referring to the various source or unit cell configurations, Hueting teaches that “the inner trench boundaries 3a in [Figures] 6 to 11 may be circular as discussed above and need not necessarily be polygonal.” *Id.* at 12:35-37. For example, the inner trench boundaries 3a in Figure 6 may be circular as shown below.

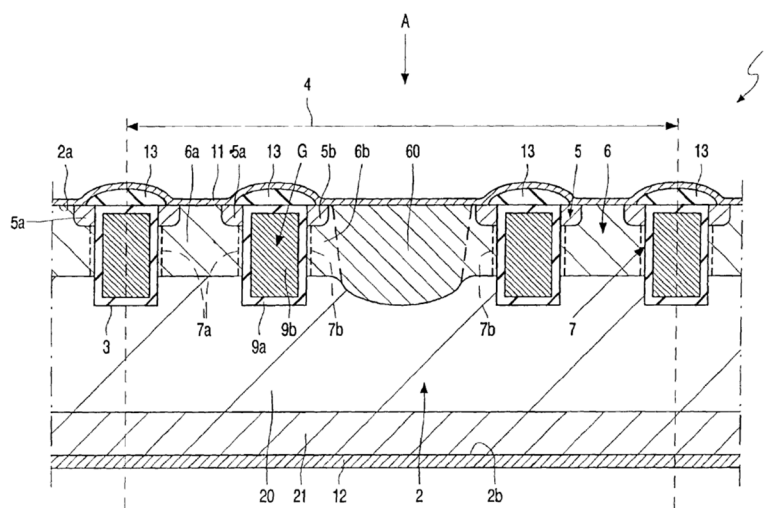
361. Furthermore, when a source trench contact is designed with a non-circular layout and has minimum feature size, as provided in Hueting, it would be readily apparent to a POSITA that the resulting source trench contact would be circular in shape. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing photolithography. When the feature size is small enough, one

rounded corner abuts the next rounded corner, resulting in a circular shaped feature. A POSITA would readily appreciate that the source trench contact in Hueting is a minimum feature size, and therefore its resulting shape after photolithography would be a circular shape. Accordingly, a source trench contact that is non-circular in design layout becomes circular in shape as a natural result of the photolithography process and the minimum feature size.

d) [1.c]. “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug”

362. As already explained in Section XI.F.1(d), Kobayashi 196 teaches Claim 1.c based on the same evidence and analysis as described in Section XI.F.1(d).

363. Hueting also teaches Claim 1.c. Hueting discloses a circular trench contact comprising a hole opened from a top surface of a semiconductor substrate. “As shown in [Figure] 2, the central semiconductor region 60 extends further into the semiconductor body from the first major surface 2b than the body regions 6 and may extend to or beyond the bottom 31 of the trench 3. The central semiconductor region 60 may however be of the same depth as the body regions 6.”
Id. at 7:27-32.



Hueting, Figure 2

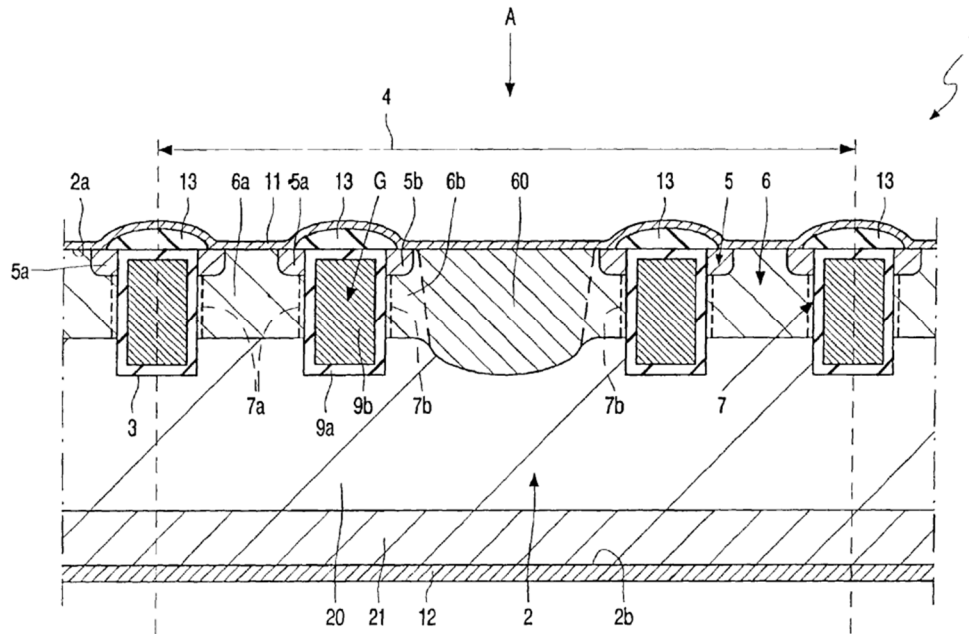
e) [1.d]. “wherein sidewalls of said hole are surrounded by and in contact said source and body regions”

364. As already explained in Section XI.F.1(e), Kobayashi 196 teaches Claim 1.d based on the same evidence and analysis as described in Section XI.F.1(e).

f) [1.e]. “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates at all circumferential points of the circular trench contact;”

365. As already explained in Section XI.F.1(f), Kobayashi 196 teaches Claim 1.e based on the same evidence and analysis as described in Section XI.F.1(f).

366. Hueting also teaches Claim 1.e. Hueting discloses a circular trench contact that is separate from trenched gates with source and body regions disposed between a gate oxide lining of the trenched gates at all circumferential points of the circular trench contact. “As shown in FIG. 2, in the device shown in FIGS. 1 and 2 the central subsidiary cell 10« of each unit cell also forms a subsidiary source cell having a subsidiary source region 5b formed within a subsidiary body region 6b defining a conduction channel area 7b from the subsidiary source region 5b to the drain drift region 20.” *Id.* at 9:24-29. “[T]he source metallisation 11 shorts the subsidiary source regions 5a, 5b to their corresponding subsidiary body regions 6a, 6b in conventional manner so as to inhibit parasitic bipolar action.” *Id.* at 9:43-46.

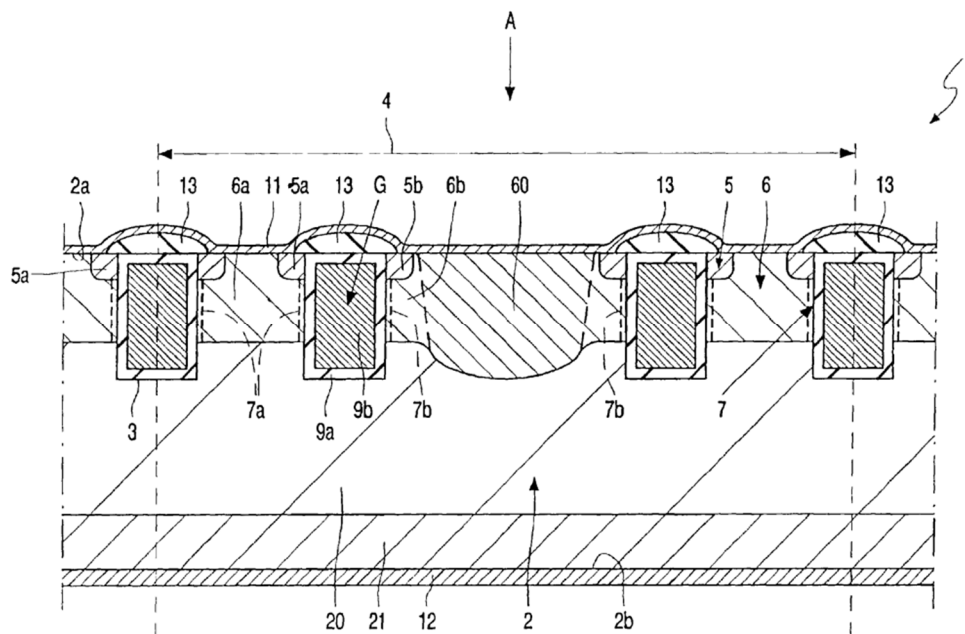


Hueting, Figure 2

g) [1.f]. “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”

367. As already explained in Section XI.F.1(g), Kobayashi 196 teaches Claim 1.f based on the same evidence and analysis as described in Section XI.F.1(g).

368. Hueting also teaches Claim 1.f. Hueting discloses a circular trench contact that is connected to a source metal disposed on top of the circular trench contact. separate from trenched gates with source and body regions disposed between a gate oxide lining of the trenched gates at all circumferential points of the circular trench contact. Figure 2, reproduced below, shows source metallisation 11 disposed on top of the circular trench contact 60. Further, “the source metallisation 11 shorts the subsidiary source regions 5a, 5b to their corresponding subsidiary body regions 6a, 6b in conventional manner so as to inhibit parasitic bipolar action.” *Id.* at 9:43-46.



Hueting, Figure 2

I. Claim 1 Is Obvious Over Hueting in View of Deboy

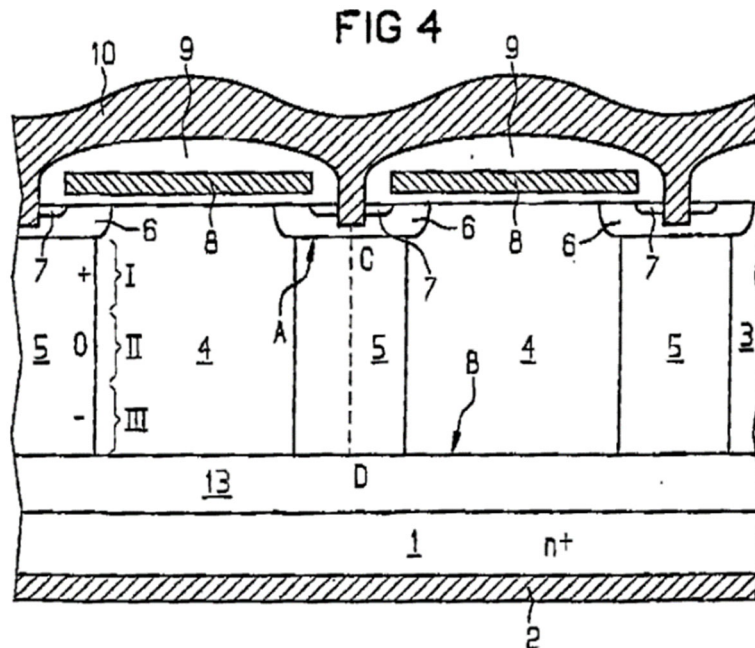
1. Motivation to Combine

369. A POSITA would have been motivated to combine Hueting and Deboy to arrive at the subject matter of Claim 1 of the '409 patent. The '409 patent, Hueting, and Deboy are analogous art relating to the same field. The '409 patent relates to semiconductor power device configurations and cell layouts. *See, e.g.*, Ex. D, '409 Patent at 1:7-12. Similarly, Hueting relates to “a trench gate field effect device.” Ex. N, Hueting at 2:13. Deboy relates to compensation devices such as n- or p-channel MOS field effect transistors. Ex. O, Deboy at 1:19.

370. Further, the '409 patent, Hueting, and Deboy are directed to similar problems: achieving maximal breakdown voltage while maintaining low on-resistance in the MOSFET. The '409 patent is directed to the problem of “parasitic bipolar NPN latch up” that are “especially pronounced near the trench corners.” Ex. D, '409 Patent, at 1:15-20. Similarly, Hueting is directed to the problem of providing “rugged[ness] whilst also providing for a reduced specific ON resistance.” Ex. N, Hueting at 2:14-15. In both cases, the latch-up phenomena is associated with

the “turn-on” of the parasitic bipolar transistor located near the top surface of the MOSFET structure. Deboy is also directed to the problem of “robustness with regard to avalanche and short circuit in the high-current operation with high source-drain voltage.” Ex. O, Deboy at 1:28-30. Deboy teaches a second way to enhance breakdown voltage in the MOSFET without increasing on-resistance, obtained by specifying alternating p- and n- doping layers in the drift region. This drift region configuration, if engineered as taught in Deboy, maintains below critical breakdown field in the drift region without substantially increasing MOSFET on-resistance. The combination of parasitic bipolar latch-up suppression near the gate channel (Huetting; ’409 patent) and maximized avalanche breakdown potential in the drift region (Deboy) results in a device with enhanced power transistor performance characteristics.

371. A POSITA would have been motivated to combine the semiconductor body and source contact of Deboy and the trench gate field effect device disclosed in Huetting to arrive at the subject matter of claim 1 of the ’409 patent. Deboy expressly teaches a various structures for an n-channel MOS transistor, including an exemplary structure with a source trench surrounded by n-conductive regions which are encompassed within a p-conductive zones. *See id.* at 10:4-33; Figure 4. Deboy also the advantages of such structures. *See id.* at 1:64-2:30. As such a POSITA would reasonably expect improved ruggedness and minimal on-resistance from combining Huetting and Deboy.



Deboy, Figure 4

2. Claim 1

a) [1.pre]. “A trenched semiconductor power device comprising a plurality of trenched gates surrounding a plurality of transistor cells formed in a semiconductor substrate, wherein:”

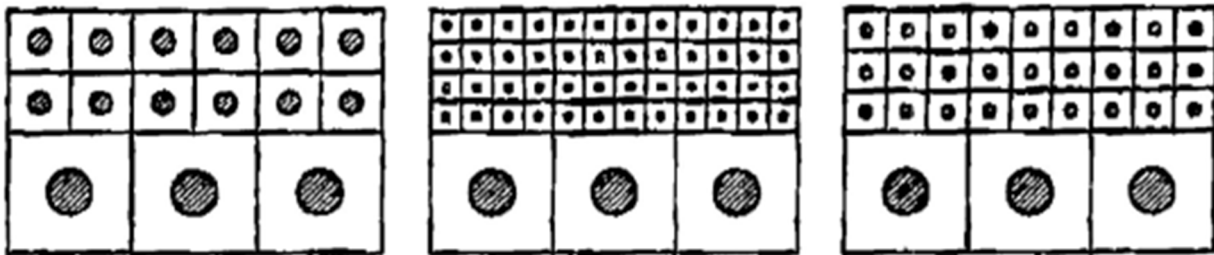
372. As already explained in Section XI.H.2(a), Hueting teaches Claim 1.pre based on the same evidence and analysis as described in Section XI.H.2(a).

b) [1.a]. “said trenched gates surrounding said transistor cells as closed cells constituting substantially square-shaped cells with rounded corners;”

373. As already explained in Section XI.H.2(b), Hueting teaches Claim 1.a based on the same evidence and analysis as described in Section XI.H.2(b).

374. Deboy also teaches Claim 1[a]. Deboy discloses trenched gates surrounded the transistor cell as closed cells that are substantially square-shaped with rounded corners. As shown in Figure 12 below, “[t]he transistor is built in known fashion with an n⁺-conductive silicon semiconductor substrate 1, a drain electrode 2, a first n-conducting layer 13, a second layer with n-conducting areas 4 and p-conductive areas 5, p-conductive zones 6, n-conductive zones 7, gate

375. Further, Figures 9A through 9C show various square-shaped layouts.



376. When a feature is designed having corners in a MOSFET design layout, as provided in Deboy, it would be readily apparent to a POSITA that the resulting corners would become rounded. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing the

photolithography. Accordingly, the corners of a closed transistor cell that is non-circular in design layout become rounded as a natural result of the photolithography process.

c) [1.b]. “each of said closed cells further includes a circular trench contact disposed substantially in a central portion of said closed cells, penetrating through a source region surrounding said trenched gates and extending into a body region encompassing said source region;”

377. As already explained in Section XI.H.2(c), Huetting teaches Claim 1.b based on the same evidence and analysis as described in Section XI.H.2(c).

378. Deboy also teaches Claim 1[b]. Deboy discloses circular trench contacts disposed substantially in a central portion of closed cells penetrating through a source region and extending into a body region. As shown in Figure 12 above, “[t]he transistor is built in known fashion with an n⁺-conductive silicon semiconductor substrate 1, a drain electrode 2, a first n-conducting layer 13, a second layer with n-conducting areas 4 and p-conductive areas 5, p-conductive zones 6, n-conductive zones 7, gate electrodes 8 made, for example, from polycrystalline silicon or metal, which are embedded in an insulation layer 9 made, for example, from silicon dioxide, and a source metalization 10 made, for example, of aluminum.” *Id.* at 11:26-35. “The regions 5', 4' lying adjacent the regions 4, 5 are connected to a p-conductive zone 6', which connects via a contact hole with the source metalization 10.” *Id.* at 11:42-44.

379. Further, Figures 9A through 9C show various square-shaped layouts with circular trench contacts disposed substantially in a central position.

380. Furthermore, when a source trench contact is designed with a non-circular layout and has minimum feature size, as provided in Deboy, it would be readily apparent to a POSITA that the resulting source trench contact would be circular in shape. This is because during manufacturing, the MOSFET undergoes photolithography, which necessarily rounds or curves the corners of features undergoing photolithography. When the feature size is small enough, one

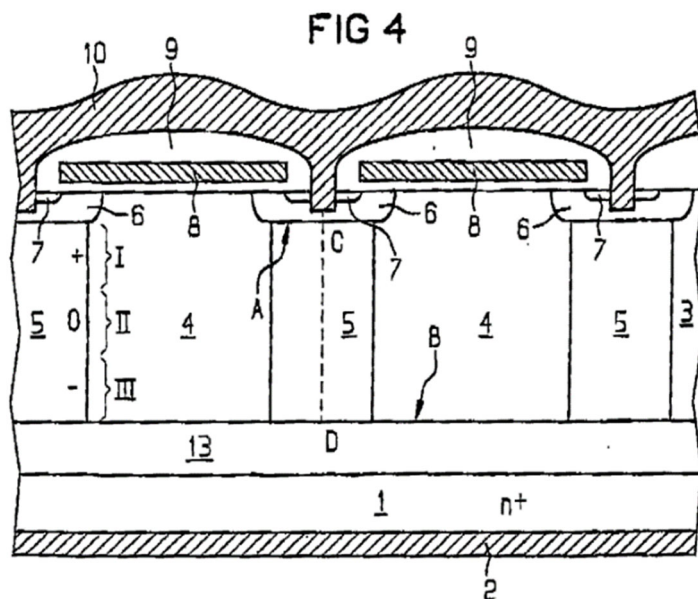
d) [1.c]. “said circular trench contact comprises a hole opened from a top surface of said semiconductor substrate and is filled with a contact metal plug”

382. Deboy also teaches Claim 1[c]. Deboy discloses in Figure 12, reproduced below, “[t]he regions 5', 4' lying adjacent the regions 4, 5 are connected to a p-conductive zone 6', which connects via a contact hole with the source metalization 10.” *Id.* at 11:42-44.



384. Deboy also teaches Claim 1[d]. Deboy discloses a contact hole with sidewalls that are surrounded by and in contact with source and body regions. Figure 4, reproduced below,

“depicts a cross-section through an n-channel MOS transistor with an n⁺-conductive silicon semiconductor substrate 1, a drain electrode 2, a first n-conductive layer 13, the second layer 3 with n-conductive areas 4 and p-conductive areas 5, p-conductive zones 6, n-conductive zones 7, gate electrodes 8 made, for example, from polycrystalline silicon or metal, which are embedded in an isolating layer 9 made, for example, from silicon dioxide, and a source metalization 10 made, for example, from aluminum.” *Id.* at 10:4-17.



Deboy, Figure 4

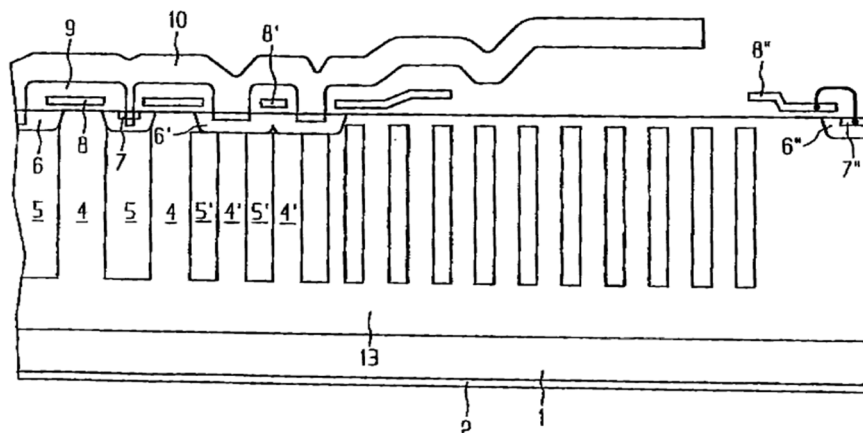
f) [1.e]. “and said circular trench contact is separate from said trenched gates with said source region and body region disposed between a gate oxide lining of said trenched gates at all circumferential points of the circular trench contact;”

385. As already explained in Section XI.H.2(f), Hueting teaches Claim 1.e based on the same evidence and analysis as described in Section XI.H.2(f).

g) [1.f]. “and said contact metal plug connected to a source metal disposed on top of said circular trench contact.”

386. As already explained in Section XI.H.2(g), Hueting teaches Claim 1.f based on the same evidence and analysis as described in Section XI.H.2(g).

387. Deboy also teaches Claim 1[e]. Deboy discloses in Figure 12, reproduced below, “[t]he regions 5', 4' lying adjacent the regions 4, 5 are connected to a p-conductive zone 6', which connects via a contact hole with the source metalization 10.” *Id.* at 11:42-44.



Deboy, Figure 12

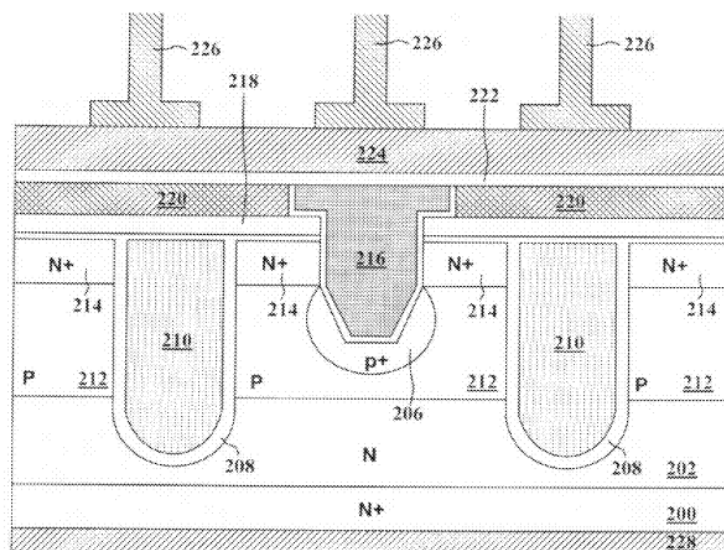
XII. THE ASSERTED CLAIMS OF THE '346 PATENT ARE ANTICIPATED OR RENDERED OBVIOUS

A. Overview of the '346 Patent

388. The '346 Patent relates to a trench Metal-Oxide-Semiconductor Field Effect Transistor (“MOSFET”), a type of semiconductor structure that is used to significantly reduce the surface area occupied by the channel of the transistor on the silicon, which in turn reduces the ON-resistance of the device for a given device area. This type of semiconductor structure was well-known in the art and to the POSITA at the time of the filing date of the '346 Patent (November 26, 2008).

389. The '346 Patent also discusses the use of copper wire bonding in the trench source contact structure. To connect the front electrode to source regions of the power cells a source contact trench of a particular shape is used. The source contact trench used to connect to the power cells has vertical sidewalls in one area and tapered sidewalls in a separate area. A copper wire is

then connected to the front metal. The use of copper was well-known in the art and to the POSITA at the time of filing. The purported invention is shown in Fig. 2:



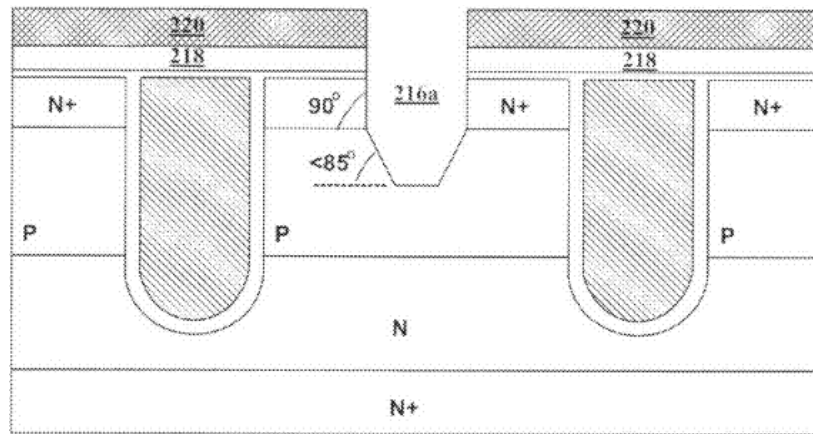
'346 Patent, Figure 2

390. Gates 210 control the flow of current from front metal 224 to rear metal 228. The front metal 224 is connected to the source region 214 and body region 212 by a metal plug in source contact trench 216. Ex. E, '346 Patent at 4:15-21, 34-36. The N+ substrate serves as the drain of the transistor. *Id.* at 3:27-29. The patent describes the shape of the plug within the source contact trench 216 as follows:

Especially, the sidewalls of source-body contact trench are perpendicular to the front surface of epitaxial layer within insulating layer and N+ source region 114 while is oblique within P-body region 212 with a taper angle less than 85 degree. . . . When etching through the second insulating layer and N+ source region, sidewalls of source-body contact trench 216a are substantially vertical (90+/- 5 degree) along the N+ source region while etching into P-body regions, sidewalls of source contact trench 216a has taper angle (less than 85 degree) respect to top surface of epitaxial layer, as shown in FIG. 3C.

Id. at 3:38-41, 4:15-21.

391. The actual formation of the source contact trench of this particular shape is shown in Fig. 3C:



'346 Patent, Figure 3C

Trench 216 is shown formed with vertical sidewalls (“90°” with respect to the top surface of the epitaxial layer (N)) in the source regions (N+) and tapered side walls (“<85°” with respect to the top surface of the epitaxial layer (N)) in the body region (P). *See also id.* at 4:15-21.

B. The '346 Patent File History

392. I understand that U.S. Patent Application No. 12/292,780 (the “’780 Application”), titled “TRENCH MOSFET WITH TRENCH SOURCE CONTACT HAVING COPPER WIRE BONDING,” was filed on November 26, 2008, and issued on December 7, 2010. Ex. E, ’346 Patent at Cover; Ex. H, 346 FH at FORCE-MOS0000125. The application was filed with 15 original claims and listed Ming-Tao Chung and Fu-Yuan Hsieh as the inventors. *Id.* at FORCE-MOS0000134-36, 150. On December 8, 2009, the Examiner issued a Requirement for Election/Restriction, to which Force MOS responded by electing Claims 1-7 for examination. *Id.* at FORCE-MOS0000154-62. Force MOS then added new Claims 16-20 with a later amendment on July 6, 2010. *Id.* at FORCE-MOS0000191-93.

393. I also understand that, on April 6, 2010, the examiner issued a non-final rejection of the pending claims under 35 U.S.C. § 103 as being unpatentable over Hsieh et al. (5,629,543) in view of Lin et al. (2008/0080112). *Id.* at FORCE-MOS0000167-70. On December 30, 2008, the applicant responded to the examiner’s rejection by distinguishing the claimed inventions from the

Hshieh reference. *Id.* at FORCE-MOS0000196. Specifically, the applicant stated, “Hshieh’s P+ deep region lacks the claimed, ‘penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into P-body regions with tapered sidewalls with respect to said top surface of said epitaxial layer.’” *Id.* On October 1, 2010, the examiner was persuaded by the applicant’s arguments over the prior art and allowed the pending claims. *Id.* at FORCE-MOS0000208.

C. The Asserted Claims

394. My understanding is that Force MOS has asserted claims 1-7 and 16-20. As relevant, I have reproduced Claim 1, Claim 16, and Claim 17 below.

Claim 1:

[1.pre] A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:

[1.a] a substrate of said first type conductivity;

[1.b] an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;

[1.c] a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;

[1.d] a first insulating layer lining said trenches as gate oxide;

[1.e] a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;

[1.f] a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;

[1.g] a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;

[1.h] a front metal disposed on the front surface of said trench MOSFET as said source metal;

[1.i] a backside metal disposed on the backside of said substrate as a drain metal;

[1.j] at least one copper wire electrically bonded to said source metal.

Claim 16:

[16.pre] A trench MOSFET comprising:

[16.a] a substrate;

[16.b] a drain metal below said substrate;

[16.c] an n epitaxial layer formed on said substrate;

[16.d] P-body regions formed on said n epitaxial layer;

[16.e] N⁺ source regions formed on said P-body regions;

[16.f] a plurality of insulating layers formed on said N⁺ source regions;

[16.g] a source metal formed on said insulating layers;

[16.h] trench gates extending through said N⁺ source regions, said P-body regions and said n epitaxial layer;

[16.i] a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N⁺ source regions, said P-body regions and said n epitaxial layer; and

[16.j] copper wire electrically bonded to said source metal.

Claim 17

[17.a] The trench MOSFET of claim 16, further comprising P⁺ areas wrapping said sidewalls and bottom of said trench source contacts within said P-body regions and an angle between said trench source

contact sidewalls and said source region is 90 ± 5 degrees within said source regions, and is less than 85 degrees within said P-body regions.

D. Priority Date of the '346 Patent

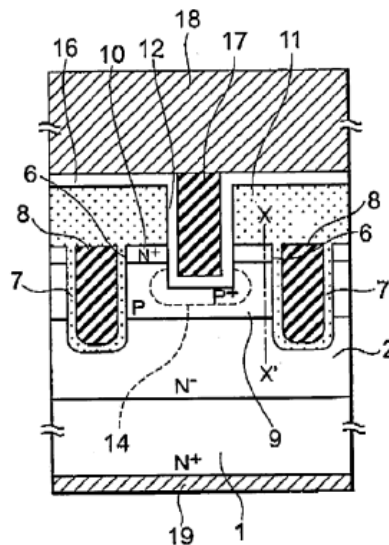
395. I understand that Force MOS claims the earliest priority date for the '346 Patent is November 26, 2008, the filing date of U.S. Patent Application Serial No. 12/292,780.

E. Prior Art Relied Upon

396. I have relied upon the following prior art in my invalidity analysis for the '346 Patent.

1. U.S. Patent Publication No. 2004/0021174 ("Kobayashi 174")

397. U.S. Patent Publication No. 2004/0021174 ("Kobayashi 174") was filed on April 24, 2003, published on February 5, 2004, and issued on May 3, 2005. Because it was publicly available more than one year prior to the priority date of the '346 Patent – November 26, 2008 – it is prior art to the '346 Patent at least under pre-AIA 35 U.S.C. § 102(b). Figure 5A from Kobayashi 174 is included for reference below:

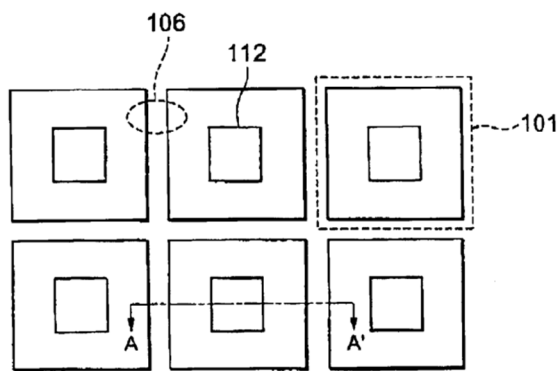


Kobayashi, Figure 5A

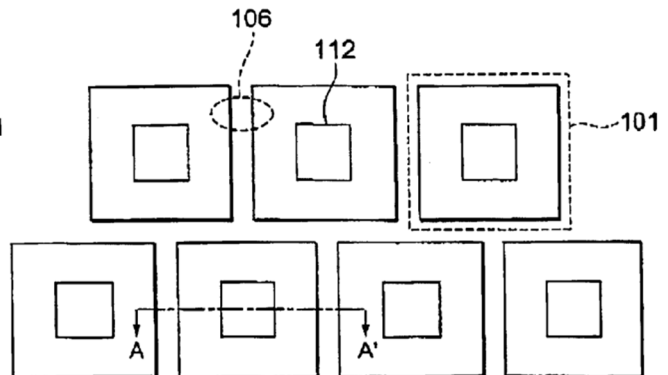
398. Similar to the '346 patent, the Kobayashi 174 prior art describes the tailoring of the depth and dimension of the trenched source contact - with respect to the maximum base doping layer concentration profile - that is in contact with the base contact layer. This tailoring is performed in view of the base doping concentration profile at both the sidewall, and at the bottom of the source contact structure. Kobayashi 174 discloses a trenched vertical MOSFET, with the source contact trenches penetrating all the way to the base layer of the MOSFET as well. There is a p⁺-type base contact layer at the bottom of the trench. Ex. J, Kobayashi 174 at Cover, Fig. 10, [0018], [0052].

399. Kobayashi 174 discloses a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. Kobayashi 174 discloses: "an N⁺-type silicon substrate 1 and an N⁻-type epitaxial layer 2 formed on one surface of the N⁺-type silicon substrate 1. A P-type base layer 9 and an N⁺-type source layer 10 are formed on a surface of the N-type epitaxial layer 2. . . . In each of trenches 6 reaching the N⁻-type epitaxial layer 2 through the P-type base layer 9, a gate oxide film 7 and a polysilicon 8 are filled. On the polysilicon 8 to serve as a gate electrode or a trench gate, an interlayer oxide film 11 is formed. Between the trench gates adjacent to each other, a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 though the N⁺-type source layer 10. Directly under the contact hole 12, a barrier metal 16 is deposited to extend onto the interlayer oxide film 11. The contact hole 12, within which the barrier metal 16 is formed, is filled with W 17. On the surface of the W 17 and the barrier metal 16, a source electrode 18 is formed. On the other surface, of the N⁺-type silicon substrate 1, a drain electrode 19 is formed." *Id.* at [0052].

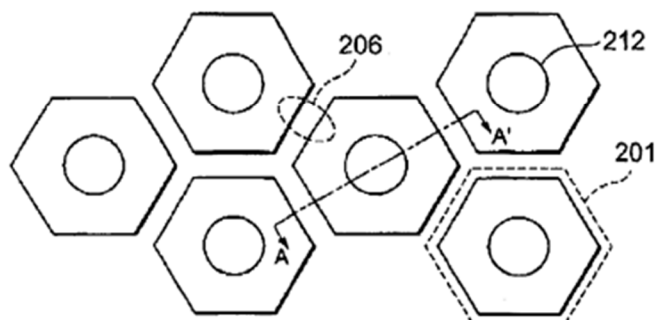
400. Additionally, Kobayashi 174 also discloses arrangements of cells, comprised by plurality of trench gates. In FIG 3A, a plurality of square cells are arranged in a matrix. In FIG. 3B, the square cells are arranged in a matrix and the cells in adjacent lines are offset in position from each other. In FIG. 4A, a plurality of hexagonal cells are arranged. In FIG. 4B, a plurality of elongated cells are arranged in a column direction.



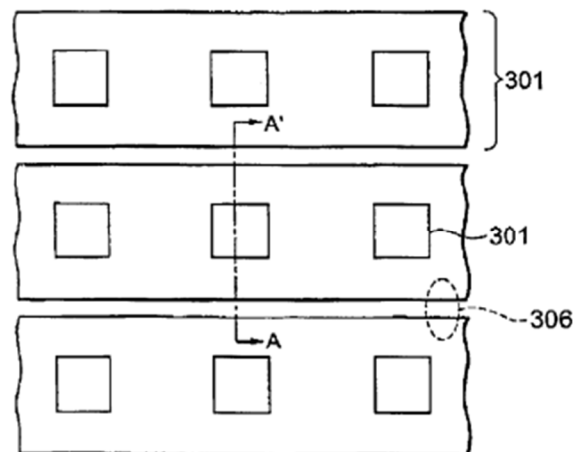
Kobayashi, Figure 3A



Kobayashi, Figure 3B



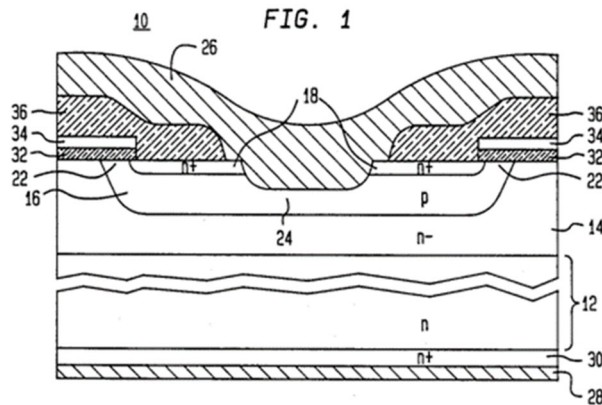
Kobayashi, Figure 4A



Kobayashi, Figure 4B

2. U.S. Patent No. 4,853,345 (“Himelick”)

401. U.S. Patent No. 4,853,345 (“Himelick”) was filed on August 22, 1988 and published and issued on August 1, 1989. Because it was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent at least under pre-AIA 35 U.S.C. § 102(b). Figure 1 from Himelick is included below for reference.



Himelick, Figure 1

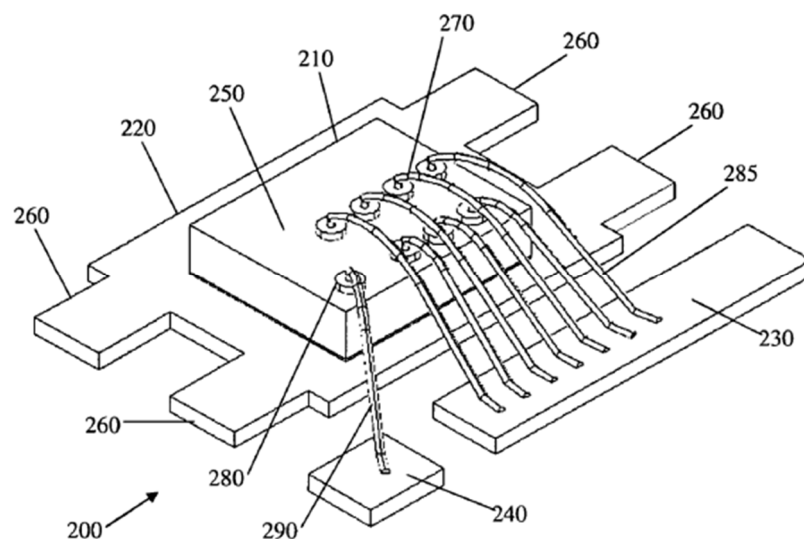
402. Similar to the '346 patent, the Himelick prior art discusses trench MOSFETs, comprised of a plurality of semiconductor power cells, with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. Himelick similarly discloses, teaches, or otherwise inherently includes an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate. *See* Ex. P, Himelick at 2:18-57.

403. Additionally, Himelick discloses, teaches, or otherwise inherently includes a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer. It describes: “an n-channel vertical DMOS transistor 10 which is part of a silicon chip whose bulk 12 is of n – type conductivity. Transistor 10 is designed for use as a power transistor. Typically this chip was part of a wafer of much larger surface area in which many like transistors were formed simultaneously. In the interest of simplicity, it is convenient to show the processing of only a single transistor, but it should be understood that normally many such transistors will be formed in a wafer by a common set of

steps. Typically the bulk (substrate) 12 of the chip is a moderately low resistivity n – type monocrystalline silicon substrate 12 on which has been grown epitaxially a higher resistivity n – type layer 14. Within this layer 14 there is formed a diffused p-type well 16. Well 16 in turn includes on a front surface thereof a relatively low resistivity n+ type annular island source region 18. A via through source region 18 exposes a central portion (region) 24 of the well 16. The portion of well 16 between vertical outer edges of region 18 and layer 14 defines a p-type annular portion (region) 22 of well 16 between the n+ type island region 18 and the n- type layer 14.” *Id.* at 2:18-40.

3. U.S. Patent No. 7,511,361 (“Zhang”)

404. U.S. Patent No. 7,511,361 (“Zhang”) was filed on June 10, 2005 as U.S. Application No. 11/150,489 and issued on March 31, 2009. The ’489 Application published on July 6, 2006 as U.S. Patent Publication No. 2006/0145318 (“Zhang 318”). Accordingly, Zhang is prior art to the ’346 Patent under at least pre-AIA 35 U.S.C. § 102(e).¹⁵ Figure 2A from Zhang is included below for reference:



Zhang, Figure 2A

¹⁵ In addition, alternatively, because Zhang 318 was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under at least pre-AIA 35 U.S.C. § 102(a)-(b).

405. Zhang discloses the use of copper wires in connecting to the source. “The source lead 230 (FIG. 2A) may be larger than in conventional semiconductor packages to enable the use of an increased number of source wires 285 which preferably are formed from gold or copper. Increasing the number of source wires 285 advantageously decreases the semiconductor package 200 resistance significantly.” Ex. Q, Zhang at 4:21-26; Ex. Y, Zhang at [0035].

4. EESEMI, *Copper Wirebonding* (“EESEMI”) (Published 2005)

406. EESemi is a publication hosted online (<https://www.eesemi.com/index.php>), which serves as a reference for general principles of semiconductor manufacturing. EESemi published an article on Copper Wirebonding (<https://www.eesemi.com/wirebond-copper.htm>) as early as 2005. Because it was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under at least pre-AIA 35 U.S.C. § 102(b).

407. “Copper is rapidly gaining a foothold as an interconnection material in semiconductor packaging because of its obvious advantages over gold. These advantages include: 1) cost reduction of up to 90%; 2) superior electrical and thermal conductivity; 3) less intermetallic growths; 4) greater reliability of the bond at elevated temperatures; and 5) higher mechanical stability.” Ex. R, EESEMI at 1.

5. U.S. Patent Publication No. 2006/0273382 (“Hshieh 382”)

408. U.S. Patent Publication No. 2006/0273382 (“Hshieh 382”) was filed on August 15, 2005 and published on December 7, 2006. Because it was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under pre-AIA 35 U.S.C. § 102(b). Figure 2 from Hshieh 382 is included below for reference.

6. U.S. Patent No. 7,514,353 (“Weidman”)

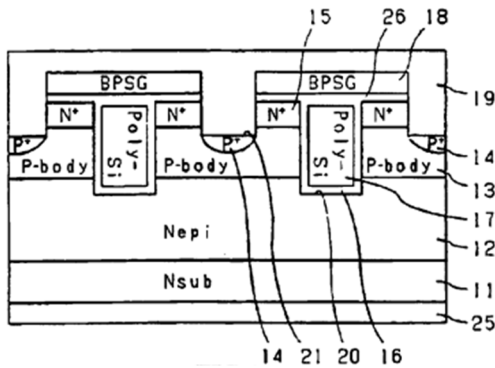
410. U.S. Patent No. 7,514,353 (“Weidman”) was filed on March 20, 2006 as U.S. Patent Application No. 11/385,344 and issued on April 7, 2009. The ’344 Application published on November 9, 2006 as U.S. Patent Publication No. 2006/0251800 (“Weidman 800”). Accordingly, Weidman is prior art to the ’346 Patent under at least pre-AIA 35 U.S.C. § 102(e).¹⁶

411. Weidman teaches methods of filling contact level features that may be found in semiconductor devices. “In general the cobalt containing layer (not shown) is a binary alloy or ternary alloy, such as cobalt boride (CoB), cobalt phosphide (CoP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt molybdenum phosphide (CoMoP), cobalt molybdenum boride (CoMoB), cobalt rhenium boride (CoReB), cobalt rhenium phosphide (CoReP), derivatives thereof, or combinations thereof.” Ex. T, Weidman at 6:64-7:4; Ex. U, Weidman 800 at [0032]. “A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer” Ex. T, Weidman at 9:27-31; Ex. U, Weidman 800 at [0040].

7. U.S. Patent No. 7,102,182 (“Takemori”)

412. U.S. Patent No. 7,102,182 (“Takemori”), was filed on November 27, 2002, published on September 2, 2004, and issued on September 5, 2006. Because it was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under 35 U.S.C. § 102(a), (b), and (e). Figure 1 from Takemori is included below for reference:

¹⁶ In addition, alternatively, because Weidman 800 was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under at least pre-AIA 35 U.S.C. § 102(a)-(b).

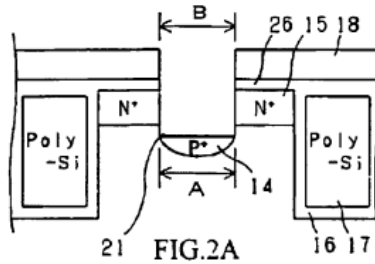


Takemori, Figure 1

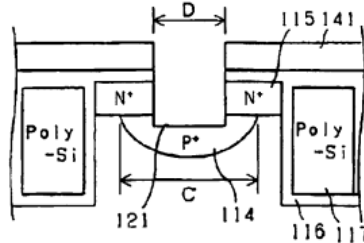
413. Takemori teaches a trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. Ex. V, Takemori at 15:10-31.

414. Takemori further discloses “The semiconductor device according to a first embodiment of the present invention forms a drain layer in the form of N⁻-type epitaxial layer 12 on one of the primary sides of N⁺-type silicon substrate 11. Moreover P-type body layer 13 is formed on N⁻-type epitaxial layer 12. In addition, N⁺-type source region 15 is formed over the range of a fixed depth from the surface of P-type body layer 13.” *Id.* at 15:33-39.

415. Takemori also discloses a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity. “In addition, FIGS. 2A and 2B are explanatory views showing a source trench and its vicinity in a semiconductor device according to a first embodiment of the present invention along with the constitution of said section of a semiconductor device according to the prior art for comparison, with FIG. 2A showing a source trench and its vicinity in a semiconductor device according to a first embodiment of the present invention, and FIG. 2B showing the constitution of said section of a semiconductor device according to the prior art for comparison.” *Id.* at 15:14-24.



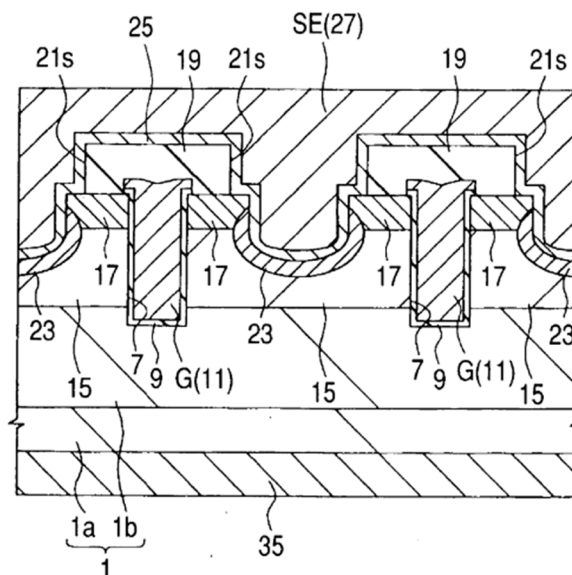
Takemori, Figure 2A



Takemori, Figure 2B (Prior Art)

8. U.S. Patent No. 6,984,864 (“Uno”)

416. U.S. Patent No. 6,984,864 (“Uno”) was filed as U.S. Application No. 10/463,771 on June 18, 2003 and initially published as U.S. Patent Publication No. 2004/0012050 on January 22, 2004. Uno issued on January 10, 2006. Because it was publicly available more than one year prior to the priority date of the ’346 Patent – November 26, 2008 – it is prior art to the ’346 Patent under at least 35 U.S.C. § 102(b). Figure 38 from Uno is included below for reference.



Uno, Figure 38

417. Uno teaches a trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. “[A]s shown in FIG. 1, a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” Ex. W, Uno at 4:55-59.

418. Uno also discloses how “[f]urther, in FIG. 38, the bottom of the contact trench 21s is rounded. For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof.” *Id.* at 15:29-36.

F. Claims 1-7 and 16-20 Are Obvious over Kobayashi 174 in view of Zhang, Hsieh 382, Weidman, and Takemori

1. Motivation to Combine

419. A POSITA would have been motivated to combine Kobayashi 174 and Zhang to arrive at the subject matter of claims 1-2, 6-7, 16, and 18-20 of the '346 patent. The '346 patent, Kobayashi 174, and Zhang are analogous art relating to the same field. The '346 patent relates to trench MOSFET cells with trench source contact structures. *See, e.g.*, Ex. E, '346 Patent at 1:8-13. Similarly, Kobayashi 174 relates to a “vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size.” Ex. J, Kobayashi 174 at [0001]. Zhang relates to “semiconductor packages.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0002].

420. Further, the '346 patent, Kobayashi 174, and Zhang are directed to similar problems. The '346 patent is directed to the problem of “reduc[ing] the spreading resistance and

device area” that are “especially pronounced near the trench corners.” Ex. E, ’346 Patent at 1:55-58. Similarly, Kobayashi 174 is directed to the problem of providing “a vertical MOSFET reduced in cell size without increasing V_t or a source resistance.” Ex. J, Kobayashi 174 at [0015]. Zhang is also directed to the problem of “reduc[ing] electrical resistance and improv[ing] thermal properties.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0002].

421. A POSITA would have been motivated to combine the source wires of Zhang and the vertical MOSFET disclosed in Kobayashi to arrive at the subject matter of claims 1-2 of the ’346 patent. Zhang expressly teaches that copper source wires are preferable over gold source wires. Ex. Q, Zhang at 4:21-24; Ex. Y, Zhang 318 at [0035]. In addition, a POSITA would have known that copper wires have the advantages of reduced costs, reduced electrical resistance, and improved thermal conductivity. Zhang also benefits from increased thermal performance, as the contact area between the encapsulant and the source bonding area and wires. Ex. Q, Zhang at 3:63-65; Ex. Y, Zhang 318 at [0031]. As such a POSITA would reasonably expect improved electrical and thermal conductivity alongside reductions in costs from combining Zhang and Kobayashi 174.

422. A POSITA would be further motivated to combine the insulating layers of Hshieh 382 with the vertical MOSFET disclosed in Kobayashi and the source wires of Zhang to arrive at the subject matter of claims 3-4 of the ’346 patent. The ’346 patent, Kobayashi 174, and Hshieh 382 are analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” Ex. S, Hshieh 382 at Abstract. Further, the ’346 patent, Kobayashi 174, and Hshieh 382 are directed to similar problems. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of an insulating layer

that is a combination of a non-doped oxide, silicate glass (NSG) layer and a borophosphosilicate glass (BPSG) layer. *Id.* at [0024]. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the advantage of reduced porosity, resulting in being a more effective passivation layer. As such a POSITA would have been motivated to combine Hshieh 382 with Kobayashi 174 and Zhang.

423. A POSITA would be further motivated to combine the insulating layers of Hshieh 382 with the vertical MOSFET disclosed in Kobayashi and the source wires of Zhang to arrive at the subject matter of claims 3-4 of the '346 patent. The '346 patent, Kobayashi 174, and Hshieh 382 are analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” *Id.* at Abstract. Further, the '346 patent, Kobayashi 174, and Hshieh 382 are directed to similar problems. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of an insulating layer that is a combination of a non-doped oxide, silicate glass (NSG) layer and a borophosphosilicate glass (BPSG) layer. *Id.* at [0024]. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the advantage of reduced porosity, resulting in being a more effective passivation layer. As such a POSITA would have been motivated to combine Hshieh 382 with Kobayashi 174 and Zhang.

424. A POSITA would be further motivated to combine the Co/TiN/W plug of Weidman with the vertical MOSFET disclosed in Kobayashi and the source wires of Zhang to arrive at the subject matter of claim 5 of the '346 patent. The '346 patent, Kobayashi 174, and Weidman are analogous art relating to the same field. Weidman relates to semiconductor devices and methods

of filling contact level features therein.” Ex. T, Weidman at Abstract; Ex. U, Weidman 800 at Abstract. Further, the ’346 patent, Kobayashi 174, and Weidman are directed to similar problems. Weidman is also directed to the problem of providing “an improved contact level device that is void free, that has a low electrical resistance, that has good electromigration performance, that is reliable, and that can be reliably formed.” Ex. T, Weidman at 3:14-17; Ex. U, Weidman 800 at [0012]. Moreover, Weidman expressly teaches that “the contact level aperture 1510 can be filled with a metal, such as copper (Cu), nickel (Ni), cobalt (Co), ruthenium (Ru), tungsten (W) or combinations thereof.” Ex. T, Weidman at 10:7-10, Figure 5D; Ex. U, Weidman 800 at [0043]. Weidman further expressly teaches that “the barrier layer 1521 may contain a multilayer stack of metals, such as, Ti, TiN, Ti/TiN/W. Ti/TiN, Ti/W, Ta/TaN/W. Ta/W, Ni/W, and Co/W that have an additional catalytic layer deposited on the top surface so that an electroless layer can be deposited thereon. A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer.” Ex. T, Weidman at 9:22-34, Figure 2C-G; Ex. U, Weidman 800 at [0040]. In addition, a POSITA would have known that a contact plug stacking Co/TiN/W has the advantage of maintaining the effective barrier properties of TiN. As such a POSITA would have been motivated to combine Weidman with Kobayashi 174 and Zhang.

425. A POSITA would be further motivated to combine the P+ areas of Takemori with the vertical MOSFET disclosed in Kobayashi and the source wires of Zhang to arrive at the subject matter of claim 17 of the ’346 patent. The ’346 patent, Kobayashi 174, and Takemori are analogous art relating to the same field. Takemori relates to a “Power MOSFET semiconductor devices having a trench gate.” Ex. V, Takemori at 1:18-19. Further, the ’346 patent, Kobayashi 174, and Takemori are directed to similar problems. Takemori is also directed to the problem of shifting

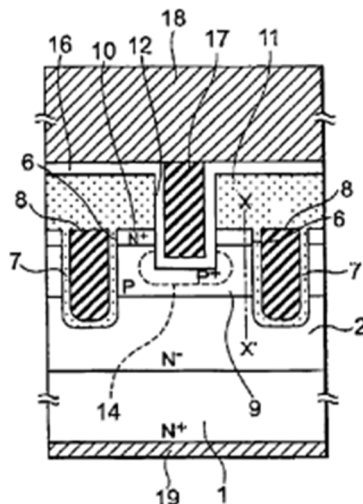
threshold voltage in power MOSFETs with source contact trenches. *Id.* at 2:1-37. Moreover, Takemori expressly teaches methods of forming buried P+ diffusion regions that encompass the entire sidewalls of the source contact trench within P-body regions. *Id.* at 3:1-13, Figures 3-6; 18:42-19:50. In addition, a POSITA would have known that P+ areas enclosing the entire sidewalls of the source contact trench within P-body regions has the advantage of providing lower contact resistance between the p-layer and the source thereby reducing the likelihood of activating the parasitic bipolar transistor. As such a POSITA would have been motivated to combine Takemori with Kobayashi 174 and Zhang.

2. Claim 1

a) [1.pre]. “A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:”

426. Kobayashi 174 discloses “a vertical MOSFET compris[ing]: “a semiconductor layer (1, 2, 9, 10) having first and second surfaces opposite to each other and trenches (6) formed on the first surface; trench gates (8) formed in the trenches; a unit cell formed in a region of the semiconductor layer surrounded by the trench gates, the unit cell comprising a base layer (9) and a source layer (10) formed on the base layer and having the first surface as a principal semiconductor surface, the unit cell having a contact hole (12) formed on a center of the principal semiconductor surface and extending from the principal semiconductor surface through the source layer to an inside of the base layer; a contact (17) formed in the contact hole; a source electrode (18) formed on the contact; and a drain electrode (19) formed on the second surface, the contact is formed to a depth different to a peak depth which is a position having a maximum impurity-concentration in a depth direction of the base layer. The unit cell further comprises a base contact

layer (14) formed within the base layer so as to enclose a bottom of the contact and to bring the base contact layer into contact with the bottom contact.” Ex. J, Kobayashi 174 at Abstract. Figure 5A, reproduced below shows a unit cell as disclosed in Kobayashi 174.



Kobayashi 174, Figure 5A

b) [1.a]. “a substrate of said first type conductivity,”

427. Kobayashi 174 discloses a substrate of first type conductivity. Figure 5A, reproduced above, shows an N⁺-type silicon substrate 1. Kobayashi 174 teaches an embodiment that “comprises an N⁺-type silicon substrate 1 and an N⁻-type epitaxial layer 2 formed on one surface of the N⁺-type silicon substrate 1.” *Id.* at [0052].

c) [1.b]. “an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;”

428. Kobayashi 174 discloses an epitaxial layer of first type conductivity disposed over a substrate and having a lower doping concentration than the substrate. As seen in Figure 5A, reproduced above, Kobayashi 174 teaches an embodiment that “comprises an N⁺-type silicon substrate 1 and an N⁻-type epitaxial layer 2 formed on one surface of the N⁺-type silicon substrate 1. A P-type base layer 9 and an N⁺-type source layer 10 are formed on a surface of the N⁻-type

d) [1.c]. “a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;”

[illegible]

e) [1.d]. “a first insulating layer lining said trenches as gate oxide;”

FORCEMOS Ex. 2009
EMC v. Force MOS, IPR2025-01433

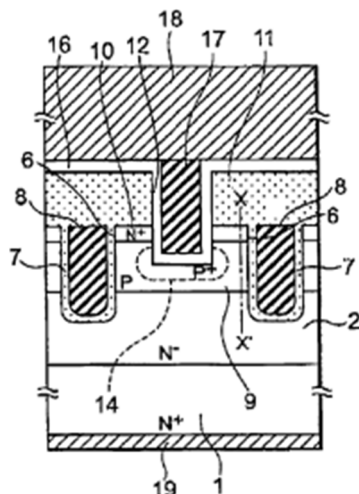
f) [1.e]. “a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;”

[illegible]

g) [1.f]. “a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;”

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EMC v. Force MOS, IPR2025-01433

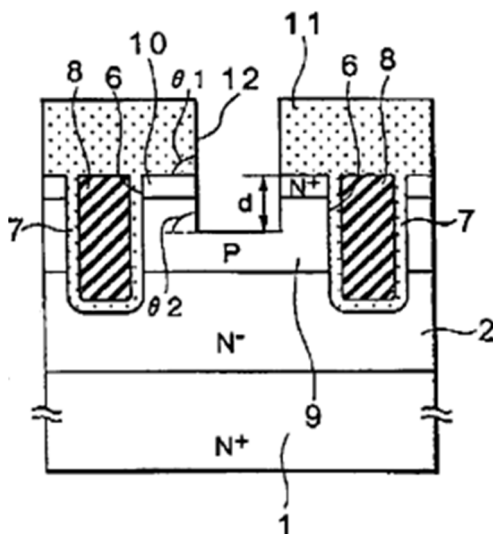
interlayer oxide film 11 is deposited by CVD to the thickness of 0.5-1 μm . Generally, the interlayer oxide film comprises SiO_2 or BPSG (borophosphosilicate glass) using a TEOS (tetra ethoxy silane) gas.” *Id.* at [0059]. Furthermore, “[d]irectly under the contact hole 12, a barrier metal 16 is deposited to extend onto the interlayer oxide film 11.” *Id.* at [0052]. “[T]he barrier metal 16 compris[es] Ti and TiN (titanium nitride).” *Id.* at [0062].



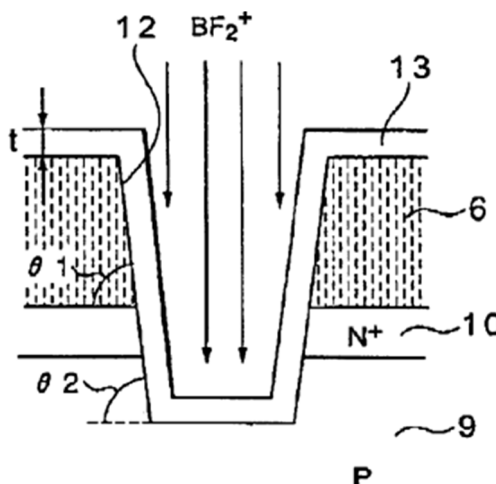
Kobayashi 174, Figure 5A

h) [1.g]. “a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;”

433. For each unit cell Kobayashi 174 discloses “a contact hole 12 having a predetermined depth is formed to reach the P-type base layer 9 through the N⁺-type source layer 10.” *Id.* at 6:57-60. Kobayashi 174 teaches that “patterning is carried out by photolithography and the interlayer oxide film 11 is etched. The silicon is etched to the depth reaching the P-type base layer 9 through the interlayer oxide film 11 and the N⁺-type source layer 10. Thus, the contact hole 12 is formed.” *Id.* at [0059]. As seen in Figure 7C, reproduced below, Kobayashi 174 teaches vertical sidewalls substantially perpendicular to a top epitaxial surface within source regions 10.



Kobayashi 174, Figure 7C



Kobayashi 174, Figure 9A

434. Kobayashi 174 further discloses source contact trenches extending into body regions with tapered sidewalls with respect to the top surface of the epitaxial layer. Kobayashi 174 teaches and illustrates in Figure 9A, reproduced above, that “in the contact hole 12, the top surface of the N⁺-type source layer 10 as the silicon surface and the contact hole 12 form a taper angle $\theta 1$ preferably smaller than 90° ($\theta 1 < 90^\circ$). The bottom and the side wall of the contact hole 12 form a taper angle $\theta 2$ preferably smaller than 90° ($\theta 2 < 90^\circ$). The taper angles within the above-mentioned range are favorable taking into account the coverage when the source electrode or a filling material connected thereto is filled later. As the angles $\theta 1$ and $\theta 2$ are smaller, filling is easy. However, if the angles $\theta 1$ and $\theta 2$ are excessively small, a void is produced in the filling material. Furthermore, a space between the trench 6 and the contact hole 12 is narrowed so that gate-source short circuiting will easily be caused to occur. In view of the above, the allowable ranges are $\theta 1 > 80^\circ$ and $\theta 2 > 80^\circ$.”
Id. at [0060].

i) [1.h]. “a front metal disposed on the front surface of said trench MOSFET as said source metal;”

435. Kobayashi 174 discloses a front metal disposed on the front surface of the trench MOSFET as a source metal. As seen in Figure 5A, reproduced above, Kobayashi 174 discloses

“[t]he contact hole 12, within which the barrier metal 16 is formed, is filled with W 17. On the surface of the W 17 and the barrier metal 16, a source electrode 18 is formed. On the other surface of the N⁺-type silicon substrate 1, a drain electrode 19 is formed.” *Id.* at [0052]. In addition, Kobayashi 174 discloses an embodiment where “AlSi (aluminum silicon) or AlSiCu (aluminum copper silicon) is deposited by sputtering to form the source electrode 18. The source electrode 18 is preferably as thick as possible in order to reduce the resistance component of AlSi or AlSiCu. Practically, the source electrode 18 has a thickness on the order of 4-6 um.” *Id.* at [0062].

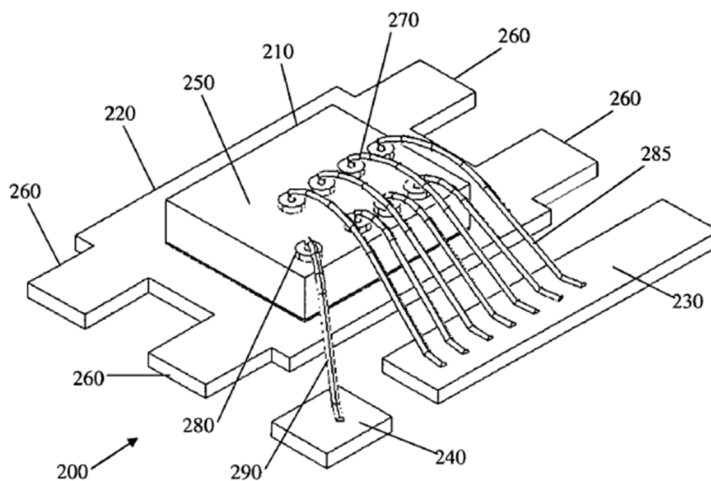
j) [1.i]. “a backside metal disposed on the backside of said substrate as a drain metal;”

436. Kobayashi 174 discloses a backside metal disposed on the backside of the substrate as a drain metal. As seen in Figure 5A, reproduced above, Kobayashi 174 discloses “[t]he contact hole 12, within which the barrier metal 16 is formed, is filled with W 17. On the surface of the W 17 and the barrier metal 16, a source electrode 18 is formed. On the other surface of the N⁺-type silicon substrate 1, a drain electrode 19 is formed.” *Id.* at [0052]. In addition, Kobayashi 174 discloses an embodiment where “the other surface of the N⁺-type silicon substrate 1 is ground by a desired thickness. Several kinds of metals are deposited by vapor deposition to form the drain electrode 19.” *Id.* at [0062].

k) [1.j]. “at least one copper wire electrically bonded to said source metal.”

437. Zhang discloses at least one copper wire electrically bonded to a source metal. Zhang “generally provides a power MOSFET DFN semiconductor package exhibiting improved electrical characteristics.” Ex. Q, Zhang at 3:59-61; Ex. Y, Zhang 318 at [0031]. Zhang further teaches that “[p]ower MOSFET die 250 may include a patterned active area including a source bonding area 270 and a gate bonding area 280. A bottom portion of the power MOSFET die 250

(not shown) may include a drain bonding area.” Ex. Q, Zhang at 4:10-13; Ex. Y, Zhang 318 at [0033]. The power MOSFET is illustrated in Figure 2A, reproduced below.



Zhang, Figure 2A

438. Zhang continues to teach that “The source lead 230 (FIG. 2A) may be larger than in conventional semiconductor packages to enable the use of an increased number of source wires 285 which preferably are formed from gold or copper. Increasing the number of source wires 285 advantageously decreases the semiconductor package 200 resistance significantly. Additionally, as the DFN semiconductor package 200 has no external leads, the overall size of the package is reduced allowing for the use of shorter source lead 230, drain leads 260 and gate lead 240 thereby reducing package resistance and inductance.” Ex. Q, Zhang at 4:21-30; Ex. Y, Zhang 318 at [0035].

3. Claim 2: “The trench MOSFET of claim 1, wherein the angle between said source contact trench walls and said top surface of said epitaxial layer is 90+/-5 degrees within said source regions, and is less than 85 degrees within said body regions.”

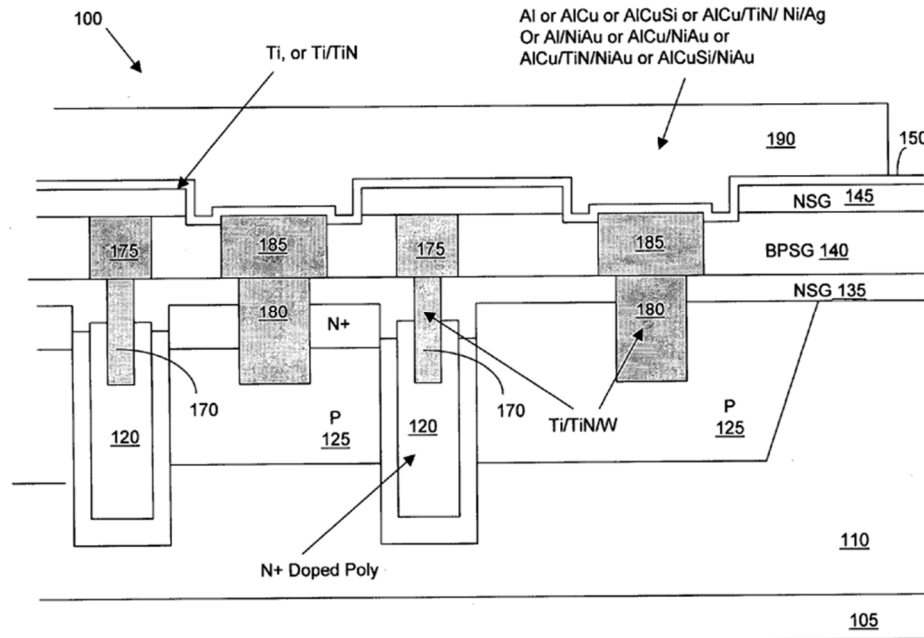
439. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

440. Kobayashi 174 teaches Claim 2 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h).

4. Claim 3: “The trench MOSFET of claim 1, wherein said second insulating layer is a combination of SRO and PSG or BPSG to further reduce source contact resistance, and each of said source contact trenches has a wider contact width in said PSG or said BPSG than in said SRO.”

441. Claim 3 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

442. Hsieh 382 discloses a second insulating layer that is a combination of SRO and PSG or BPSG to further reduce source contact resistance. Hsieh 382 discloses “a metal oxide semiconductor field effect transistor (MOSFET) device 100 [that] is supported on a substrate 105 formed with an epitaxial layer 110. The MOSFET device 100 includes a trenched gate 120 disposed in a trench with a gate insulation layer 115 formed as a liner layer covering the walls of the trench. A body region 125 that is doped with a dopant of second conductivity type, e.g., P-type dopant, extends between the trenched gates 120. The P-body regions 125 encompassing a source region 130 doped with the dopant of first conductivity, e.g., N⁺ dopant. The source regions 130 are formed near the top surface of the epitaxial layer surrounding the trenched gates 125. The top surface of the semiconductor substrate extending over the top of the trenched gate, the P body regions 125 and the source regions 130 are covered with a NSG layer 135, a BPSG protective layers 140 and another insulation NSG layer 145.” Ex. S, Hsieh 382 at [0020]. Hsieh 382’s MOSFET device is illustrated in Figure 2, reproduced below.



Hshieh 382, Figure 2

443. Hshieh 382 further discloses source contact trenches with wider contact width in the BPSG than in the SRO. As shown in Figure 2, reproduced above, “the gate contact trenches 170 and 175 and source contact trenches 180 and 185 are formed first with an oxide dry-etch followed by a silicon etch. The oxide etch process opens the trenches that first penetrate through the BPSG layer 140 and the NSG layer 135 to form the upper portion of the trenches 175 and 185. The silicon etch process then opens the trench through the trenched polysilicon gate 170 and the body and source regions 130 and 125 to form the lower portion 170 and 180.” *Id.* at [0021].

5. Claim 4: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Ti/TiN/W.”

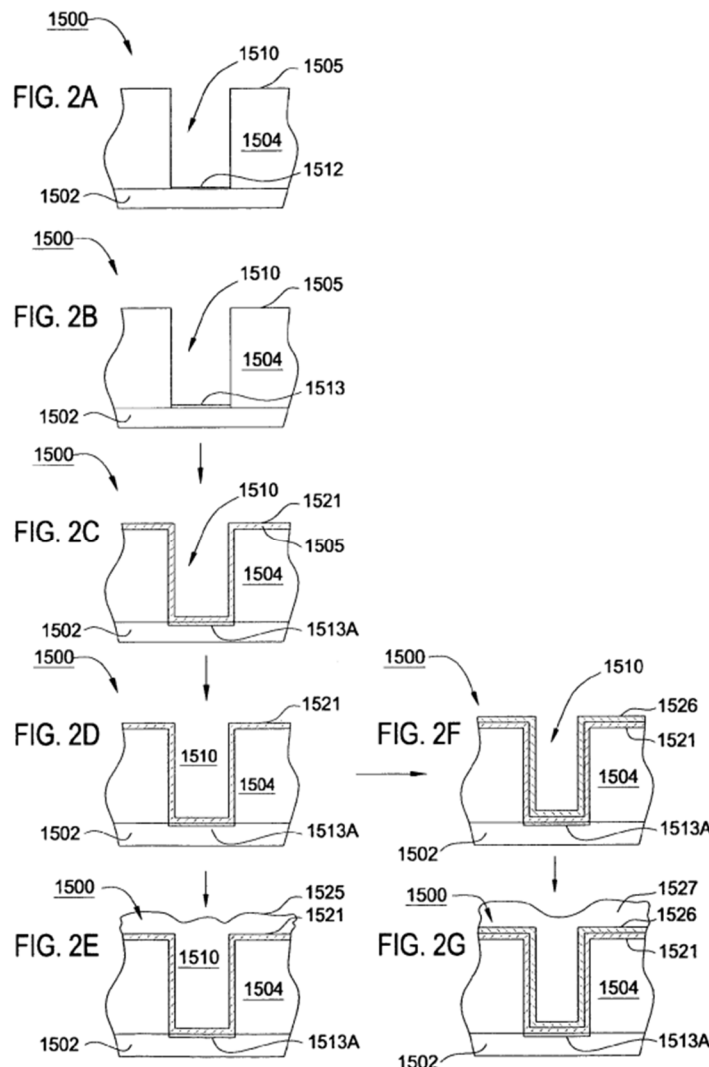
444. Claim 4 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

445. Hshieh 382 discloses source contact trenches filled with Ti/TiN/W. Hshieh 382 teaches that “the source contact trenches 180 and 185 are filled with a barrier layer composed of Ti and TiN and a tungsten plug.” *Id.* at [0021].

6. Claim 5: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Co/TiN/W.”

446. Claim 5 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

447. Weidman discloses source contact trenches filled with Co/TiN/W. Weidman provides “methods of filling contact level features formed in a semiconductor device.” Ex. T, Weidman at 4:53-55; Ex. U, Weidman 800 at [0025]. Weidman further teaches multilayer stacks that are deposited in the contact level aperture 1510. Ex. T, Weidman at 8:62-9:22; Ex. U, Weidman 800 at [0039]. Figures 2A-G, reproduced below, illustrate Weidman’s method.



Weidman, Figures 2A-G

448. Specifically, “the barrier layer 1521 may contain a multilayer stack of metals, such as, *Ti*, *TiN*, *Ti/TiN/W*, *Ti/TiN*, *Ti/W*, *Ta/TaN/W*, *Ta/W*, *Ni/W*, and *Co/W* that have an additional catalytic layer deposited on the top surface so that an electroless layer can be deposited thereon. A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), *cobalt* (*Co*), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer.” Ex. T, Weidman at 9:23-30; Ex. U, Weidman 800 at [0040] (emphasis added). *See also* Ex. T, Weidman at 9:2-10; Ex. U, Weidman 800 at [0039] (“The nomenclature used hereinto define a multilayer stack is intended to describe a barrier layer 1521 that contains discrete layers that may be arranged in a [sic] any desired order (e.g., Ni/Co=Ni on Co or Co on Ni) as long as the final exposed surface of the barrier layer 1521 is catalytically active to enable a subsequent electroless deposition process or can be readily rendered catalytically active by performing a activation process (e.g., palladium activation).”). Weidman further discloses that “In general the contact level aperture 1510 can be filled with a metal, such as copper (Cu), nickel (Ni), cobalt (Co), ruthenium (Ru), tungsten (W) or combinations thereof.” Ex. T, Weidman at 10:7-10; Ex. U, Weidman 800 at [0043].

7. Claim 6: “The trench MOSFET of claim 1, wherein said source metal is Al alloys, Ti/Ni/Ag or Cu.”

449. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

450. Kobayashi 174 teaches Claim 6 based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

8. Claim 7: “The trench MOSFET of claim 1, wherein said source metal Al alloys have thicknesses larger than 3 μm .”

451. Claim 7 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

452. Kobayashi 174 teaches Claim 6 based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

9. Claim 16

a) [16.pre]. “A trench MOSFET comprising:”

453. Kobayashi 174 teaches Claim 16.pre based on the same evidence and analysis as described above for Claim 1.pre. *Supra* XII.F.2(a). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

b) [16.a]. “a substrate”

454. Kobayashi 174 teaches Claim 16.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* XII.F.2(b). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

c) [16.b]. “a drain metal below said substrate;”

455. Kobayashi 174 teaches Claim 16.b based on the same evidence and analysis as described above for Claim 1.i. *Supra* XII.F.2(j). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

d) [16.c]. “an n epitaxial layer formed on said substrate;”

456. Kobayashi 174 teaches Claim 16.c based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

e) [16.d]. “P-body regions formed on said n epitaxial layer;”

457. Kobayashi 174 teaches Claim 16.d based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

f) [16.e]. “N+ source regions formed on said P-body regions;”

458. Kobayashi 174 teaches Claim 16.e based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

g) [16.f]. “a plurality of insulating layers formed on said N+ source regions;”

459. Kobayashi 174 teaches Claim 16.f based on the same evidence and analysis as described above for Claims 1.d and 1.f. *Supra* XII.F.2(e), (g). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

h) [16.g]. “a source metal formed on said insulating layers;”

460. Kobayashi 174 teaches Claim 16.g based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

i) [16.h]. “trench gates extending through said N+ Source regions, said P-body regions and said n epitaxial layer;”

461. Kobayashi 174 teaches Claim 16.h based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.F.2(d). To the extent there are minor differences in the

wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

j) [16.i]. “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N+ Source regions, said P-body regions and said n epitaxial layer, and”

462. Kobayashi 174 teaches Claim 16.j based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

k) [16.j]. “copper wire electrically bonded to said source metal.”

463. Zhang teaches Claim 16.h based on the same evidence and analysis as described above for Claim 1.j. *Supra* XII.F.2(k). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

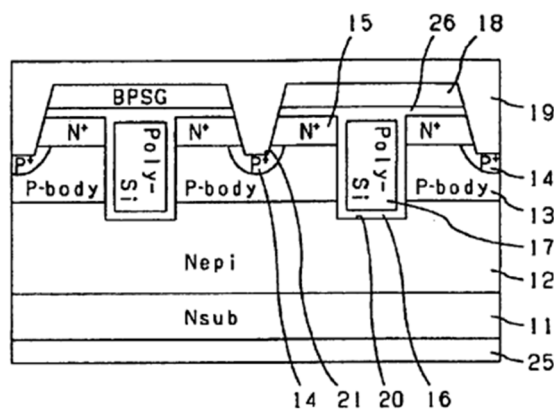
10. Claim 17: “The trench MOSFET of claim 16, further comprising P+ areas wrapping said sidewalls and bottom of said trench Source contacts within said P-body regions and an angle between said trench source contact sidewalls and said source region is 90+/-5 degrees within said source regions, and is less than 85 degrees within said P-body regions.”

464. Claim 17 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

465. Kobayashi 174 teaches Claim 17 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h).

466. Takemori also teaches Claim 17. Takemori discloses P+ areas wrapping the sidewalls and bottom of trench source contacts within P-body regions. Figure 3, reproduced below,

shows a buried P⁺-type diffusion region 14 that completely encompasses the sidewalls within the entire P-body region 13.



11. Claim 18: “The trench MOSFET of claim 16, further comprising an interconnection layer between said source metal and an upper insulating layer.”

467. Claim 18 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

468. Kobayashi 174 teaches Claim 18 based on the same evidence and analysis as described above for Claim 1.f. *Supra* XII.F.2(g). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

12. Claim 19: “The trench MOSFET of claim 16, wherein said source metal vertically connects to said N+ source regions and said P-body regions.”

469. Claim 19 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

470. Kobayashi 174 teaches Claim 19 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

13. Claim 20: “The trench MOSFET of claim 16, wherein said trench source contact narrows towards the P+ areas.”

471. Claim 20 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and Zhang as discussed above.

472. Kobayashi 174 teaches Claim 20 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

G. Claims 1-7 and 16-20 Are Obvious over Kobayashi 174 in view of Himelick, EESEMI, Hshieh 382, Weidman, and Takemori.

1. Motivation to Combine

473. A POSITA would have been motivated to combine Kobayashi 174, Himelick, and EESEMI to arrive at the subject matter of Claims 1-2 of the '346 patent. The '346 Patent, Kobayashi 174, Himelick, and EESEMI are analogous art relating to the same field. The '346 Patent relates to trench MOSFET cells with trench source contact structures. *See, e.g.*, Ex. E, '346 Patent at 1:8-13. Similarly, Kobayashi 174 relates to a “vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size.” Ex. J, Kobayashi 174 at [0001]. Himelick relates to a “process for forming a vertical n-channel DMOS transistor.” Ex. P, Himelick at Abstract. EESEMI relates to wire bonding processes employed in semiconductor manufacturing. Ex. R, EESEMI, at 1.

474. Further, the '346 Patent, Kobayashi 174, Himelick, and EESEMI are each directed to similar problems. The '346 Patent is directed to the problem of “reduc[ing] the spreading resistance and device area” that are “especially pronounced near the trench corners.” Ex. E, '346 Patent at 1:55-58. Similarly, Kobayashi 174 is directed to the problem of providing “a vertical MOSFET reduced in cell size without increasing V_t or a source resistance.” Ex. J, Kobayashi 174

at [0015]. Himelick is directed to the problem of reducing the costs and complexity of manufacturing DMOS transistors. Ex. P, Himelick at 1:12-51. EESEMI is also directed to the problem of reducing costs, improving electrical and thermal conductivity, and more. Ex. R, EESEMI, at 1.

475. A POSITA would have been motivated to combine the contact trench of Himelick and the vertical MOSFET disclosed in Kobayashi 174 to arrive at the subject matter of claims 1-2 of the '346 Patent. Himelick expressly teaches that a “plasma etch is chosen to provide a via 72 which substantially conforms in area to the area originally defined by the edge of the opening 71A in the photoresist masking layer 70.” Ex. P, Himelick at 5:1-10. Himelick further teaches that “curved sloping in the sidewalls of the via 72 is desirable to permit better filling of the via 72 by the subsequent metallization.” *Id.* at 5:7-9. As such a POSITA would reasonably expect improved electrical and thermal conductivity alongside reductions in costs from combining EESEMI and Kobayashi 174.

476. A POSITA would be further motivated to combine the copper wirebonding of EESEMI and the vertical MOSFET disclosed in Kobayashi 174 to arrive at the subject matter of Claims 1-2 of the '346 patent. EESEMI expressly teaches that “copper is rapidly gaining a foothold as an interconnection material in semiconductor packaging because of its obvious advantage over gold.” Ex. R, EESEMI, at 1. EESEMI further teaches that such advantages include “1) cost reduction of up to 90%; 2) superior electrical and thermal conductivity; 3) less intermetallic growths; 4) greater reliability of the bond at elevated temperatures; and 5) higher mechanical stability.” *Id.* As such a POSITA would reasonably expect improved electrical and thermal conductivity alongside reductions in costs from combining EESEMI and Kobayashi 174.

477. A POSITA, based on the same evidence and analysis as described above in Section XII.F.1, would be further motivated to combine the insulating layers of Hsieh 382 with the vertical MOSFET disclosed in Kobayashi and the copper wirebonding of EESEMI to arrive at the subject matter of Claims 3-4 of the '346 Patent.

478. A POSITA, based on the same evidence and analysis as described above in Section XII.F.1, would be further motivated to combine the Co/TiN/W plug of Weidman with the vertical MOSFET disclosed in Kobayashi and the copper wirebonding of EESEMI to arrive at the subject matter of Claim 5 of the '346 Patent.

479. A POSITA, based on the same evidence and analysis as described above in Section XII.F.1, would be further motivated to combine the P⁺ areas of Takemori with the vertical MOSFET disclosed in Kobayashi and the copper wirebonding of EESEMI to arrive at the subject matter of Claim 17 of the '346 Patent.

2. Claim 1

a) [1.pre]. “A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:”

480. Kobayashi 174 teaches Claim 1.pre based on the same evidence and analysis as described above for Claim 1.pre. *Supra* XII.F.2(a).

b) [1.a]. “a substrate of said first type conductivity,”

481. Kobayashi 174 teaches Claim 1.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* XII.F.2(b).

c) [1.b]. “an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;”

482. Kobayashi 174 teaches Claim 1.b based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c).

d) [1.c]. “a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;”

483. Kobayashi 174 teaches Claim 1.c based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.F.2(d).

e) [1.d]. “a first insulating layer lining said trenches as gate oxide;”

484. Kobayashi 174 teaches Claim 1.d based on the same evidence and analysis as described above for Claim 1.d. *Supra* XII.F.2(e).

f) [1.e]. “a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;”

485. Kobayashi 174 teaches Claim 1.e based on the same evidence and analysis as described above for Claim 1.e. *Supra* XII.F.2(f).

g) [1.f]. “a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;”

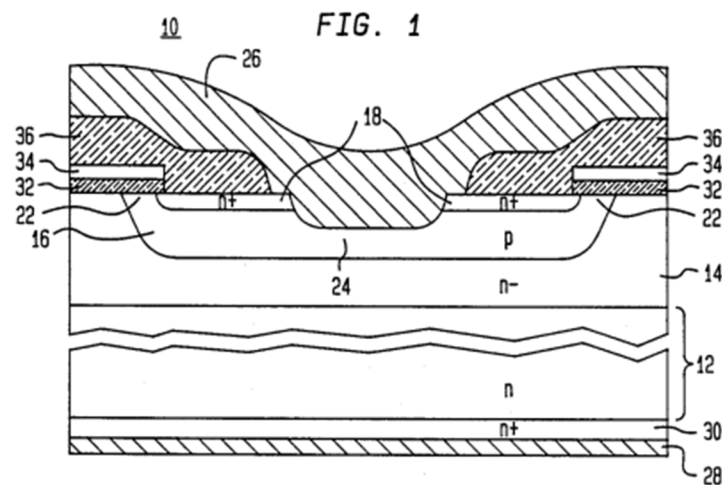
486. Kobayashi 174 teaches Claim 1.f based on the same evidence and analysis as described above for Claim 1.f. *Supra* XII.F.2(g).

h) [1.g]. “a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;”

487. Kobayashi 174 teaches Claim 1.g based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h).

488. Himelick also teaches Claim 1.g. Himelick discloses Double-diffused MOSFETs (“DMOS”). Himelick’s DMOS comprises an n-type silicon substrate 12 with moderately low

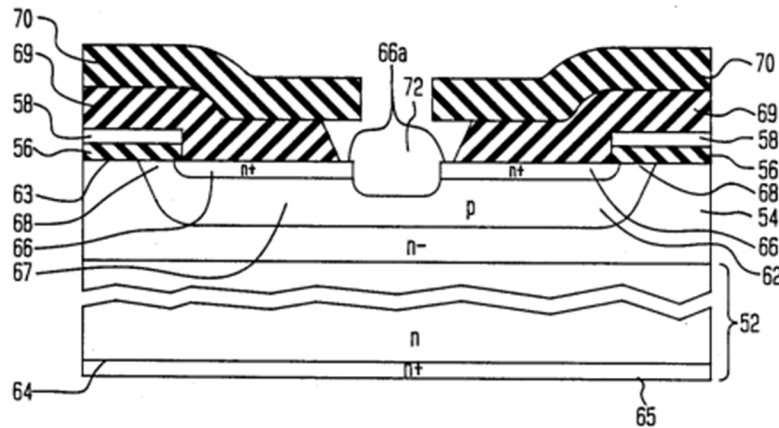
resistivity on which an n-type layer with higher resistivity 14 is grown epitaxially. Within the epitaxial layer 14, a diffused p-type region 16 is formed. The p-type region 16 in turn includes an n^+ -type region 18. Ex. P, Himelick at 2:28-34. Figure 1, reproduced below, illustrates the disclosed DMOS.



Himelick, Figure 1

489. Himelick further teaches that a contact trench is formed through source region 18, exposing a central region of the p-type region 16. The vertical outer edges of the source region 18 and the epitaxial layer define the annular region 22 of the p-type region 16. *Id.* at 2:34-46.

490. Himelick discloses substantially perpendicular, vertical sidewalls within source regions and tapered sidewalls extending into body regions. As seen in Figure 2G, reproduced below, the contact trench has substantially perpendicular sidewalls in the source regions and curved sidewalls in the body region. Further illustrative is Himelick's process for forming the contact trench. A trench 72 is formed by plasma etching. "It is chosen also to leave sloping curved walls in the via which are less vertical than would result from a more anisotropic reactive ion etch. Such curved sloping in the sidewalls of the via 72 is desirable to permit better filling of the via 72 by the subsequent metallization. A known SF₆ plasma is useful to provide such etching." *Id.* at 5:4-10.



Himelick, Figure 2G

i) [1.h]. “a front metal disposed on the front surface of said trench MOSFET as said source metal;”

491. Kobayashi 174 teaches Claim 1.h based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

j) [1.i]. “a backside metal disposed on the backside of said substrate as a drain metal;”

492. Kobayashi 174 teaches Claim 1.i based on the same evidence and analysis as described above for Claim 1.i. *Supra* XII.F.2(j).

k) [1.j]. “at least one copper wire electrically bonded to said source metal.”

493. EESEMI teaches Claim 1.j. EESEMI discloses that “Copper is rapidly gaining a foothold as an interconnection material in semiconductor packaging because of its obvious advantages over gold. These advantages include: 1) cost reduction of up to 90%; 2) superior electrical and thermal conductivity; 3) less intermetallic growth; 4) greater reliability of the bond at elevated temperatures; and 5) higher mechanical stability.” Ex. R, EESEMI, at 1.

3. Claim 2: “The trench MOSFET of claim 1, wherein the angle between said source contact trench walls and said top surface of said epitaxial layer is 90+/-5 degrees within said source regions, and is less than 85 degrees within said body regions.”

494. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

495. Kobayashi 174 teaches Claim 2 based on the same evidence and analysis as described above for Claim 2. *Supra* XII.F.3.

496. Himelick also teaches Claim 2 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.G.2(h).

4. Claim 3: “The trench MOSFET of claim 1, wherein said second insulating layer is a combination of SRO and PSG or BPSG to further reduce source contact resistance, and each of said source contact trenches has a wider contact width in said PSG or said BPSG than in said SRO.”

497. Claim 3 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

498. Hshieh 382 also teaches Claim 3 based on the same evidence and analysis as described above for Claim 3. *Supra* XII.F.4.

5. Claim 4: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Ti/TiN/W.”

499. Claim 4 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

500. Hshieh 382 also teaches Claim 4 based on the same evidence and analysis as described above for Claim 4. *Supra* XII.F.5.

6. Claim 5: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Co/TiN/W.”

501. Claim 5 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

502. Weidman also teaches Claim 5 based on the same evidence and analysis as described above for Claim 5. *Supra* XII.F.6.

7. Claim 6: “The trench MOSFET of claim 1, wherein said source metal is Al alloys, Ti/Ni/Ag or Cu.”

503. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

504. Kobayashi 174 teaches Claim 6 based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

8. Claim 7: “The trench MOSFET of claim 1, wherein said source metal Al alloys have thicknesses larger than 3 μm .”

505. Claim 7 is dependent on Claim 1, the elements of which are disclosed by Kobayashi 174, Himelick and EESEMI as discussed above.

506. Kobayashi 174 teaches Claim 6 based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

9. Claim 16

l) [16.pre]. “A trench MOSFET comprising:”

507. Kobayashi 174 teaches Claim 16.pre based on the same evidence and analysis as described above for Claim 1.pre. *Supra* XII.F.2(a). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

m) [16.a]. “a substrate”

508. Kobayashi 174 teaches Claim 16.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* XII.F.2(b). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

n) [16.b]. “a drain metal below said substrate;”

509. Kobayashi 174 teaches Claim 16.b based on the same evidence and analysis as described above for Claim 1.i. *Supra* XII.F.2(j). To the extent there are minor differences in the

wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

o) [16.c]. “an n epitaxial layer formed on said substrate;”

510. Kobayashi 174 teaches Claim 16.c based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

p) [16.d]. “P-body regions formed on said n epitaxial layer;”

511. Kobayashi 174 teaches Claim 16.d based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

q) [16.e]. “N+ source regions formed on said P-body regions;”

512. Kobayashi 174 teaches Claim 16.e based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.F.2(c). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

r) [16.f]. “a plurality of insulating layers formed on said N+ source regions;”

513. Kobayashi 174 teaches Claim 16.f based on the same evidence and analysis as described above for Claims 1.d and 1.f. *Supra* XII.F.2(e), (g). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

s) [16.g]. “a source metal formed on said insulating layers;”

514. Kobayashi 174 teaches Claim 16.g based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

t) [16.h]. “trench gates extending through said N+ Source regions, said P-body regions and said n epitaxial layer;

515. Kobayashi 174 teaches Claim 16.h based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.F.2(d). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

u) [16.i]. “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N+ Source regions, said P-body regions and said n epitaxial layer, and”

516. Kobayashi 174 teaches Claim 16.j based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.G.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

v) [16.j]. “copper wire electrically bonded to said source metal.”

517. EESEMI teaches Claim 16.h based on the same evidence and analysis as described above for Claim 1.j. *Supra* XII.F.2(k). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

10. Claim 17: “The trench MOSFET of claim 16, further comprising P+ areas wrapping said sidewalls and bottom of said trench Source contacts within said P-body regions and an angle between said trench source contact

sidewalls and said source region is 90+/-5 degrees within said source regions, and is less than 85 degrees within said P-body regions.”

518. Claim 17 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and EESEMI as discussed above.

519. Kobayashi 174 and Takemori teach Claim 17 based on the same evidence and analysis as described above for Claim 17. *Supra* XII.F.10. To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

11. Claim 18: “The trench MOSFET of claim 16, further comprising an interconnection layer between said source metal and an upper insulating layer.”

520. Claim 18 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and EESEMI as discussed above.

521. Kobayashi 174 teaches Claim 18 based on the same evidence and analysis as described above for Claim 1.f. *Supra* XII.F.2(g). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

12. Claim 19: “The trench MOSFET of claim 16, wherein said source metal vertically connects to said N+ source regions and said P-body regions.”

522. Claim 19 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and EESEMI as discussed above.

523. Kobayashi 174 teaches Claim 19 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

13. Claim 20: “The trench MOSFET of claim 16, wherein said trench source contact narrows towards the P+ areas.”

524. Claim 20 is dependent on Claim 16, the elements of which are disclosed by Kobayashi 174 and EESEMI as discussed above.

525. Kobayashi 174 teaches Claim 20 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.F.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

H. Claims 1-7 and 16-20 Are Obvious over Takemori in view of Zhang, Hsieh 382, Weidman, and Kobayashi 174

1. Motivation to Combine

526. A POSITA would have been motivated to combine Takemori and Zhang to arrive at the subject matter of Claims 1-2, 6-7, 16, and 18-20 of the '346 Patent. The '346 Patent, Takemori, and Zhang are analogous art relating to the same field. The '346 Patent relates to trench MOSFET cells with trench source contact structures. *See, e.g.*, Ex. E, '346 Patent at 1:8-13. Similarly, Takemori relates to “a semiconductor device having the constitution of a power MOSFET.” Ex. V, Takemori at 1:18-20. Zhang relates to “semiconductor packages.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0001].

527. Further, the '346 Patent, Takemori, and Zhang are directed to improving the same device. The '346 Patent is directed to the problem of “reduc[ing] the spreading resistance and device area” that are “especially pronounced near the trench corners.” Ex. E, '346 Patent at 1:55-58. Similarly, Takemori is also directed to the problem of shifting threshold voltage in power MOSFETs with source contact trenches. Ex. V, Takemori at 2:1-37. Zhang is also directed to the problem of “reduc[ing] electrical resistance and improv[ing] thermal properties.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0001].

528. A POSITA would have been motivated to combine the source wires of Zhang and the power MOSFET disclosed in Takemori to arrive at the subject matter of Claims 1-2 of the '346 Patent. Zhang expressly teaches that copper source wires are preferable over gold source wires. Ex. Q, Zhang at 4:21-24; Ex. Y, Zhang 318 at [0033]. In addition, a POSITA would have known that copper wires have the advantages of reduced costs, reduced electrical resistance, and improved thermal conductivity. As such a POSITA would reasonably expect improved electrical and thermal conductivity alongside reductions in costs from combining Zhang and Takemori.

529. A POSITA would be further motivated to combine the insulating layers of Hshieh 382 with the power MOSFET disclosed in Takemori and the source wires of Zhang to arrive at the subject matter of Claim 4 of the '346 patent. The '346 Patent, Takemori, and Hshieh 382 are analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” Ex. S, Hshieh 382 at Abstract. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of an insulating layer that is a combination of a non-doped oxide, silicate glass (NSG) layer and a borophosphosilicate glass (BPSG) layer. *Id.* at [0024]. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the advantage of reduced porosity, resulting in being a more effective passivation layer. As such a POSITA would be motivated to combine Hshieh 382 with Takemori and Zhang.

530. A POSITA would be further motivated to combine the Ti/TiN/W plug of Hshieh 382 with the power MOSFET disclosed in Takemori and the source wires of Zhang to arrive at the subject matter of Claims 3-4 of the '346 Patent. The '346 Patent, Takemori, and Hshieh 382 are

analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” *Id.* at Abstract. Further, the ’346 patent, Takemori, and Hshieh 382 are directed to similar problems. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of Ti/TiN/W source contact. *Id.* at [0024], Figure 2. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the advantage of reduced porosity, resulting in being a more effective passivation layer. As such a POSITA would be motivated to combine Hshieh 382 with Takemori and Zhang.

531. A POSITA would be further motivated to combine the Co/TiN/W plug of Weidman with the power MOSFET disclosed in Takemori and the source wires of Zhang to arrive at the subject matter of Claim 5 of the ’346 Patent. The ’346 Patent, Takemori, and Weidman are analogous art relating to the same field. Weidman relates to semiconductor devices and methods of filling contact level features therein.” Ex. T, Weidman at Abstract; Ex. U, Weidman 800 at Abstract. Further, the ’346 Patent, Takemori, and Weidman are directed to similar problems. Weidman is also directed to the problem of providing “an improved contact level device that is void free, that has a low electrical resistance, that has good electromigration performance, that is reliable, and that can be reliably formed..” Ex. T, Weidman at 3:14-17; Ex. U, Weidman 800 at [0012]. Moreover, Weidman expressly teaches that “the contact level aperture 1510 can be filled with a metal, such as copper (Cu), nickel (Ni), cobalt (Co), ruthenium (Ru), tungsten (W) or combinations thereof.” Ex. T, Weidman at 10:7-10, Figure 5D; Ex. U, Weidman 800 at [0043]. Weidman further expressly teaches that “the barrier layer 1521 may contain a multilayer stack of

metals, such as, Ti, TiN, Ti/TiN/W. Ti/TiN, Ti/W, Ta/TaN/W. Ta/W, Ni/W, and Co/W that have an additional catalytic layer deposited on the top surface so that an electroless layer can be deposited thereon. A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer.” Ex. T, Weidman at 9:22-34, Figure 2C-G; Ex. U, Weidman 800 at [0040]. In addition, a POSITA would have known that a contact plug stacking Co/TiN/W has the advantage of maintaining the effective barrier properties of TiN. As such a POSITA would have been motivated to combine Weidman with Takemori and Zhang.

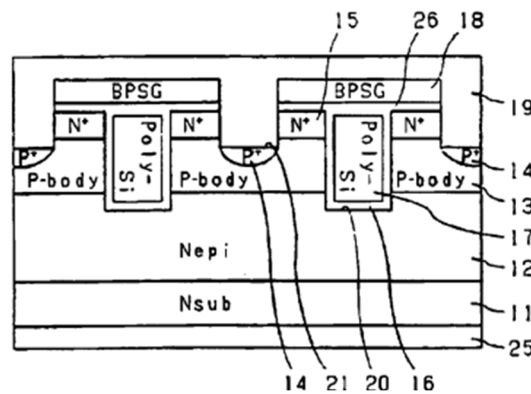
532. A POSITA would be further motivated to combine the Al alloy source metal having thicknesses larger than 3 μm of Kobayashi 174 with the power MOSFET disclosed in Takemori and the source wires of Zhang to arrive at the subject matter of Claim 7 of the '346 Patent. The '346 Patent, Kobayashi 174, and Takemori are analogous art relating to the same field. Kobayashi 174 relates to a “vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size.” Ex. J, Kobayashi 174 at [0001]. Further, the '346 Patent, Kobayashi 174, and Takemori are directed to similar problems. Kobayashi 174 is directed to the problem of providing “a vertical MOSFET reduced in cell size without increasing V_t or a source resistance.” *Id.* at [0015]. Moreover, Kobayashi 174 expressly teaches methods of forming Al alloy source metals that have a thickness on the order of 4-6 μm . *Id.* at 9:30-53; Figures 8A-C. In addition, a POSITA would have known that Al alloy source metals with a certain thickness have the advantage of providing lower device access resistance. As such a POSITA would be motivated to combine Kobayashi 174 with Takemori and Zhang.

2. Claim 1

- a) *[1.pre]. “A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity*

above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:

533. Takemori discloses a semiconductor devices having trench gates. As shown in Figure 1 below, “reference symbol 11 indicates an N⁺-type silicon substrate, 12 an N⁻-type epitaxial layer, 13 a P-type body layer, 14 a buried P⁺-type diffusion region, 15 an N⁺-type source region, 16 a gate insulating film, 17 a gate electrode film, 18 a borophosphosilicate glass (BPSG) film, 19 a source electrode film, 20 a gate trench, 21 a source trench, 25 a drain electrode film, and 26 an insulating film.” Ex. V, Takemori at 15:24-31.



Takemori, Figure 1

b) [1.a]. “a substrate of said first type conductivity,”

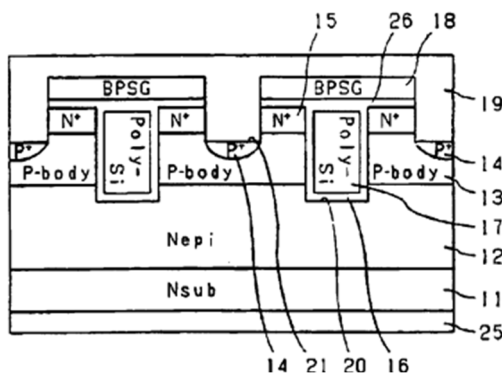
534. Takemori teaches Claim 1.a. Takemori discloses an N⁺-type silicon substrate 11 as shown in Figure 1, reproduced above.

c) [1.b]. “an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;”

535. Takemori teaches Claim 1.b. Takemori discloses an N⁻-type epitaxial layer 12 as shown in Figure 1, reproduced above. The N⁻-type epitaxial layer 12 has a lower doping concentration than the N⁺-type silicon substrate 11.

d) [1.c]. “a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;”

536. Takemori teaches Claim 1.c. Takemori discloses gate trenches 20 as shown in Figure 1, reproduced above. “Gate trench 20 is formed so that its tip section reaches to a comparatively shallow site of N⁻-type epitaxial layer 12.” *Id.* at 15:42-44. As shown in Figure 1 below, “source trench 21 is formed so as to reach to P-type body layer 13 to enable it to make stable contact with P-type body layer 13.” *Id.* at 16:3-5. In addition, N⁺-type source region 15 is adjacent to the source trench, surrounding the gate trenches. *Id.* at 16:3-5.



Takemori, Figure 1

e) [1.d]. “a first insulating layer lining said trenches as gate oxide;”

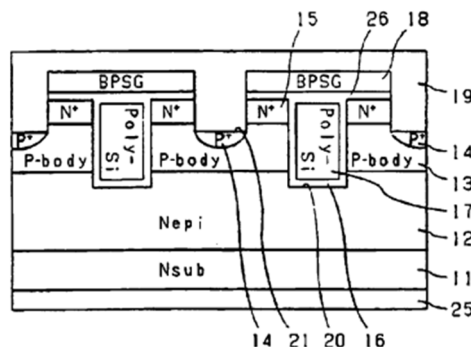
537. Takemori discloses a gate insulating film 16 as shown in Figure 1 above. Takemori further teaches that “gate insulating film 16 is adhered and formed on the peripheral and bottom surfaces of gate trench 20.” *Id.* at 15:44-46. Takemori, in further describing the manufacturing process of the disclosed semiconductor device, teaches that “after removing the aforementioned silicon oxide film, gate insulating film 16 is formed so as to cover the surface of gate trench 20.” *Id.* at 14-17.

f) [1.e]. “a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;”

538. Takemori discloses a gate electrode film 17 as shown in Figure 1 above. Takemori teaches that “[g]ate electrode film 17 is comprised by depositing polysilicon, and is formed so as to fill in the space surrounded by gate insulating film 16.” *Id.* at 15:46-48.

g) [1.f]. “a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;”

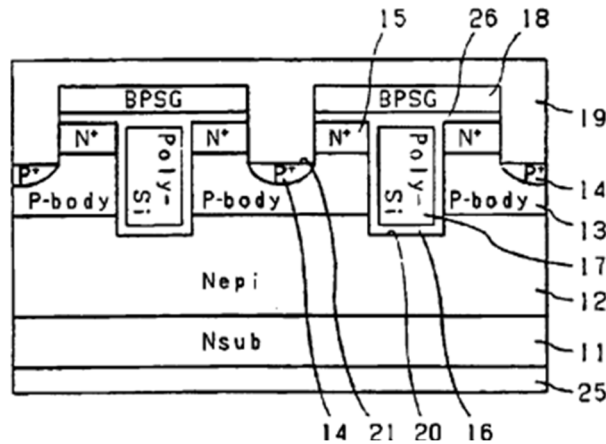
539. Takemori discloses an insulating film 26 as shown in Figure 1 below. Takemori teaches that “insulating film 26 is formed so as to cover gate insulating film 16, gate electrode film 17 and the surface of N⁺-type source region 15. Insulating film 26 is a silicon oxide film, and although it is integrally formed with gate insulating film 16, as will be described later, it is formed in a separate step from gate insulating film 16. Moreover, a different insulating film in the form of BPSG film 18 is formed on the surface of insulating film 26.” *Id.* at 15:50-57.



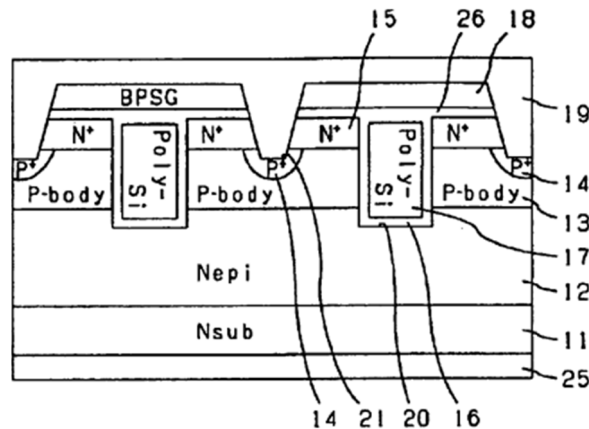
Takemori, Figure 1

h) [1.g]. “a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;”

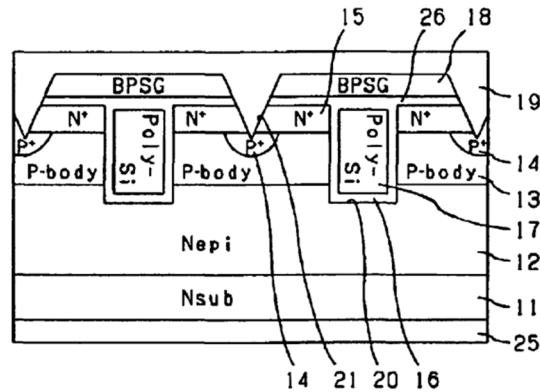
540. Takemori discloses a unit cell with a source trench 21. Takemori teaches that “P-type body layer 13 is opened at predetermined intervals to alternately form gate trench 20 and source trench 21.” *Id.* at 15:39-41. “Source trench 21 is formed so as to reach to a comparatively shallow site of P-type body layer 13.” *Id.* at 15:62-63. As shown in Figure 1, reproduced below, source trench 21 is formed through the second insulating layer, comprising BPSG film 18 and insulating film 26, and N⁺-type source regions 15 with substantially perpendicular, vertical sidewalls within source regions 15.



541. Takemori further discloses source trench 21 further extending into P-type body layer 13 with tapered sidewalls. As shown in Figures 3, 4, and 6, reproduced below, source trench 21 extends into P-type body layer 13 with tapered or curved sidewalls. Referring to Figure 3, Takemori teaches that “source trench 22 is formed by inclining its peripheral surface so that the width of source trench 22 becomes narrower towards the bottom.” *Id.* at 18:51-53.

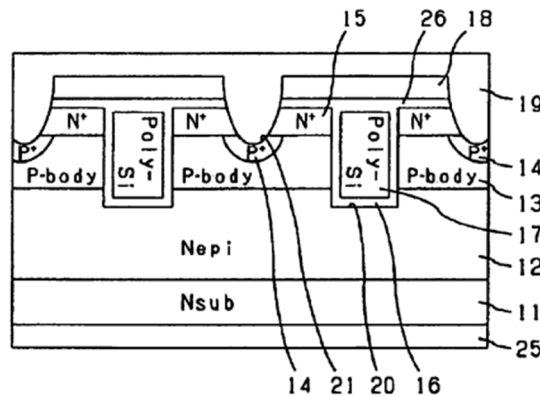


542. Referring to Figure 4, Takemori teaches that “the peripheral surface of source trench 23 is inclined, and the cross-section of source trench 23 is formed roughly into the shape of the letter ‘V.’” *Id.* at 19:6-8.



Takemori, Figure 4

543. Referring to Figure 5, Takemori teaches that “the inner surface of source trench 21 is formed to be a curved surface in which the bottom surface and side surface are integrated.” *Id.* at 19:40-42.

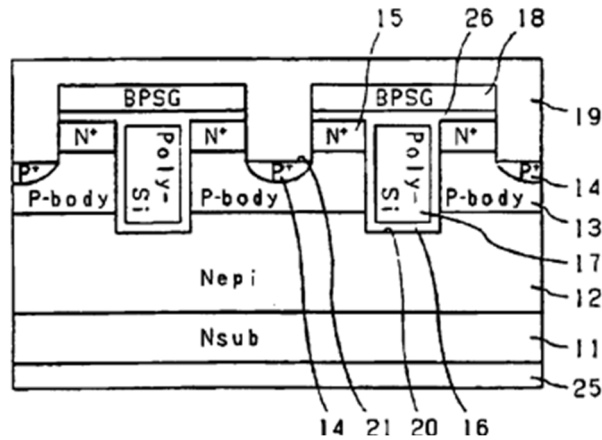


Takemori, Figure 6

544. In addition, “a buried P⁺-type diffusion region 14 is formed so as to be exposed on the bottom surface of the source trench 21.” *Id.* at 15:65-66. As shown in Figures 3, 4, and 6, the buried P⁺-type diffusion region 14 also completely encompasses the sidewalls within the P-type body layer 13.

i) [1.h]. “a front metal disposed on the front surface of said trench MOSFET as said source metal;”

545. Takemori teaches Claim 1.h. Takemori discloses a front metal as a source metal. As shown in Figure 1 below, “source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18.” *Id.* at 16:27-28.



Takemori, Figure 1

j) [1.i]. “a backside metal disposed on the backside of said substrate as a drain metal;”

546. Takemori teaches Claim 1.i. Takemori discloses a backside metal as a drain metal. As shown in Figure 1 above, “In addition, source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18. Moreover, drain electrode film 25 is formed on the other side of N⁺-type silicon substrate 11.” *Id.* at 16:27-30.

k) [1.j]. “at least one copper wire electrically bonded to said source metal.”

547. Zhang teaches Claim 1.j based on the same evidence and analysis as described above for Claim 1.j. *Supra* XII.F.2(k).

3. Claim 2: “The trench MOSFET of claim 1, wherein the angle between said source contact trench walls and said top surface of said epitaxial layer is 90+/-5 degrees within said source regions, and is less than 85 degrees within said body regions.”

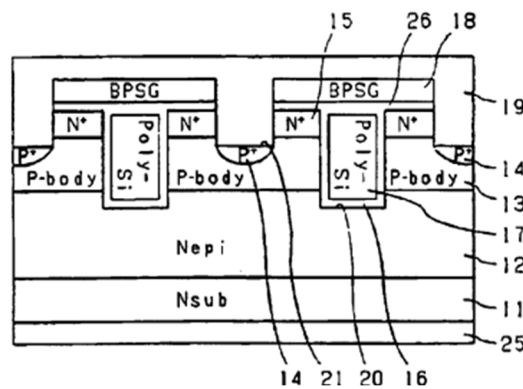
548. Claim 2 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

549. Takemori teaches Claim 2 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.H.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

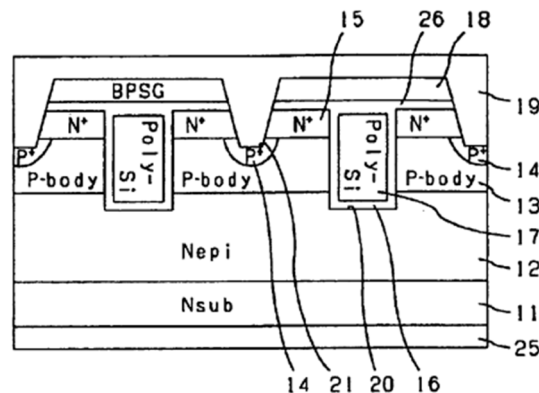
4. **Claim 3: “The trench MOSFET of claim 1, wherein said second insulating layer is a combination of SRO and PSG or BPSG to further reduce source contact resistance, and each of said source contact trenches has a wider contact width in said PSG or said BPSG than in said SRO.”**

550. Claim 3 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

551. Takemori teaches Claim 3. Takemori discloses “power MOSFET semiconductor devices with trench gates as shown in Figures 1 and 3 below.



Takemori, Figure 1



Takemori, Figure 3

552. Takemori discloses an insulating layer that is a combination of SRO and BPSG. As shown in Figures 1 and 3 above, a “BPSG film 18 is formed on the surface of insulating film 26.” *Id.* at 15:56-57. “Insulating film 26 is a silicon oxide film, and although it is integrally formed with gate insulating film 16, as will be described later, it is formed in a separate step from gate insulating film 16.” *Id.* at 15:51-54.

553. Takemori further discloses a source contact trench that has a wider contact width in the BPSG than in the SRO. As shown in Figure 3 above, the source contact trench 21 “becomes narrower towards the bottom.” *Id.* at 18:54.

5. Claim 4: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Ti/TiN/W.”

554. Claim 4 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

555. Hsieh 382 also teaches Claim 4 based on the same evidence and analysis as described above for Claim 4. *Supra* XII.F.5.

6. Claim 5: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Co/TiN/W.”

556. Claim 5 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

557. Weidman also teaches Claim 5 based on the same evidence and analysis as described above for Claim 5. *Supra* XII.F.6.

7. Claim 6: “The trench MOSFET of claim 1, wherein said source metal is Al alloys, Ti/Ni/Ag or Cu.”

558. Claim 6 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

559. Takemori teaches Claim 6. Takemori discloses a source metal that is Al alloys, Ti/Ni/Ag or Cu. Takemori teaches that “source electrode film 19 is formed inside source trench 21 and on the surface of BPSG film 18. Moreover, drain electrode film 25 is formed on the other side of N⁺-type silicon substrate 11. Furthermore, source electrode film 19 and drain electrode film 25 are preferably formed using, for example, Al—Si or Al—Si—Cu. *Id.* at 16:27-32. Figure 1 above shows the source electrode film 19.

8. Claim 7: “The trench MOSFET of claim 1, wherein said source metal Al alloys have thicknesses larger than 3 μm .”

560. Claim 7 is dependent on Claim 1, the elements of which are disclosed by Takemori and Zhang as discussed above.

561. Kobayashi 174 teaches Claim 6 based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.F.2(i).

9. Claim 16

a) [16.pre]. “A trench MOSFET comprising:”

562. Takemori teaches Claim 16.pre based on the same evidence and analysis as described above for Claim 1.pre. *Supra* XII.H.2(a). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

b) [16.a]. “a substrate”

563. Takemori teaches Claim 16.a based on the same evidence and analysis as described above for Claim 1.a. *Supra* XII.H.2(b). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

c) [16.b]. “a drain metal below said substrate;”

564. Takemori teaches Claim 16.b based on the same evidence and analysis as described above for Claim 1.i. *Supra* XII.H.2(j). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

d) [16.c]. “an n epitaxial layer formed on said substrate;”

565. Takemori teaches Claim 16.c based on the same evidence and analysis as described above for Claim 1.b. *Supra* XII.H.2(c). To the extent there are minor differences in the wording of

the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

e) [16.d]. “P-body regions formed on said n epitaxial layer;”

566. Takemori teaches Claim 16.d based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.H.2(d). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

f) [16.e]. “N+ source regions formed on said P-body regions;”

567. Takemori teaches Claim 16.d based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.H.2(d). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

g) [16.f]. “a plurality of insulating layers formed on said N+ source regions;”

568. Takemori teaches Claim 16.f based on the same evidence and analysis as described above for Claim 1.f. *Supra* XII.H.2(g). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

h) [16.g]. “a source metal formed on said insulating layers;”

569. Takemori teaches Claim 16.g based on the same evidence and analysis as described above for Claim 1.h. *Supra* XII.H.2(i). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

i) [16.h]. “trench gates extending through said N+ Source regions, said P-body regions and said n epitaxial layer;”

570. Takemori teaches Claim 16.h based on the same evidence and analysis as described above for Claim 1.c. *Supra* XII.H.2(d). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

j) [16.i]. “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N+ Source regions, said P-body regions and said n epitaxial layer, and”

571. Takemori teaches Claim 16.j based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.H.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

k) [16.j]. “copper wire electrically bonded to said source metal.”

572. Zhang teaches Claim 16.j based on the same evidence and analysis as described above for Claim 1.j. *Supra* XII.H.2(k). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

10. Claim 17: “The trench MOSFET of claim 16, further comprising P+ areas wrapping said sidewalls and bottom of said trench Source contacts within said P-body regions and an angle between said trench source contact sidewalls and said source region is 90+/-5 degrees within said source regions, and is less than 85 degrees within said P-body regions.”

573. Claim 17 is dependent on Claim 16, the elements of which are disclosed by Takemori and Zhang as discussed above.

574. Takemori teaches Claim 17 based on the same evidence and analysis as described above for Claim 17. *Supra* XII.H.2(h). To the extent there are minor differences in the wording of

the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

11. Claim 18: “The trench MOSFET of claim 16, further comprising an interconnection layer between said source metal and an upper insulating layer.”

575. Claim 18 is dependent on Claim 16, the elements of which are disclosed by Takemori and Zhang as discussed above.

576. Kobayashi 174 teaches Claim 1.f based on the same evidence and analysis as described above for Claim 1.f. *Supra* XII.F.2(g).

12. Claim 19: “The trench MOSFET of claim 16, wherein said source metal vertically connects to said N+ source regions and said P-body regions.”

577. Claim 19 is dependent on Claim 16, the elements of which are disclosed by Takemori and Zhang as discussed above.

578. Takemori teaches Claim 19 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.H.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

13. Claim 20: “The trench MOSFET of claim 16, wherein said trench source contact narrows towards the P+ areas.”

579. Claim 20 is dependent on Claim 16, the elements of which are disclosed by Takemori and Zhang as discussed above.

580. Takemori teaches Claim 20 based on the same evidence and analysis as described above for Claim 1.g. *Supra* XII.H.2(h). To the extent there are minor differences in the wording of the limitation, my reasoning for why the limitation is disclosed above applies equally to this limitation.

I. Claims 1-7 and 16-20 Are Obvious over Uno in view of Himelick, Zhang/EESEMI, Hshieh 382, Weidman, Kobayashi 174, and Takemori

1. Motivation to Combine

581. A POSITA would have been motivated to combine Uno and Zhang to arrive at the subject matter of Claims 1-2, 6-7, 16, and 18-20 of the '346 Patent. The '346 Patent, Uno, and Zhang are analogous art relating to the same field. The '346 Patent relates to trench MOSFET cells with trench source contact structures. *See, e.g.*, Ex. E, '346 Patent at 1:8-13. Similarly, Uno relates to “a semiconductor device having a power MISFET (Metal Insulator Semiconductor Field Effect Transistor.” Ex. W, Uno at 1:6-10. Zhang relates to “semiconductor packages.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0001].

582. Further, the '346 Patent, Uno, and Zhang are directed to similar problems. The '346 Patent is directed to the problem of “reduc[ing] the spreading resistance and device area” that are “especially pronounced near the trench corners.” Ex. E, '346 Patent at 1:55-58. Similarly, Uno is also directed to “...backwardly biasing the emitter and base of a parasitic bipolar transistor, making it less tending to turn-on...” Ex. W, Uno at Abstract. Zhang is also directed to the problem of “reduc[ing] electrical resistance and improv[ing] thermal properties.” Ex. Q, Zhang at 1:15-19; Ex. Y, Zhang 318 at [0001].

583. A POSITA would have been motivated to combine the source wires of Zhang and the power MISFET disclosed in Uno to arrive at the subject matter of Claims 1-2 of the '346 Patent. Zhang expressly teaches that copper source wires are preferable over gold source wires. *Id.* at 4:21-24. In addition, a POSITA would have known that copper wires have the advantages of reduced costs, reduced electrical resistance, and improved thermal conductivity. As such a POSITA would reasonably expect improved electrical and thermal conductivity alongside reductions in costs from combining Zhang and Takemori.

584. A POSITA would be further motivated to combine the insulating layers of Hshieh 382 with the power MISFET disclosed in Uno and the source wires of Zhang to arrive at the subject matter of claims 4 of the '346 Patent. The '346 Patent, Uno, and Hshieh 382 are analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” Ex. S, Hshieh 382 at Abstract. Further, the '346 Patent, Uno, and Hshieh 382 are directed to similar problems. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of an insulating layer that is a combination of a non-doped oxide, silicate glass (NSG) layer and a borophosphosilicate glass (BPSG) layer. *Id.* at [0024]. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the advantage of lower porosity for more effective device passivation. As such a POSITA would be motivated to combine Hshieh 382 with Uno and Zhang.

585. A POSITA would be further motivated to combine the Ti/TiN/W plug of Hshieh 382 with the power MISFET disclosed in Uno and the source wires of Zhang to arrive at the subject matter of Claims 3-4 of the '346 Patent. The '346 Patent, Uno, and Hshieh 382 are analogous art relating to the same field. Hshieh 382 relates to a “trenched metal oxide semiconductor field effect transistor (MOSFET) device that includes gate contact trenches and source contact trenches.” *Id.* at Abstract. Further, the '346 Patent, Uno, and Hshieh 382 are directed to similar problems. Hshieh 382 is also directed to the problem of “reduc[ing] the space occupied by the source contact and meanwhile [] reduc[ing] the gate resistance.” *Id.* at [0008]. Moreover, Hshieh 382 expressly teaches the use of Ti/TiN/W source contact. *Id.* at [0024], Figure 2. In addition, a POSITA would have known that an insulating layer that is a combination of silicon-rich oxide and BPSG has the

advantage of reduced porosity for a more effective passivation layer. As such a POSITA would be motivated to combine Hshieh 382 with Uno and Zhang.

586. A POSITA would be further motivated to combine the Co/TiN/W plug of Weidman with the power MISFET disclosed in Uno and the source wires of Zhang to arrive at the subject matter of Claim 5 of the '346 Patent. The '346 Patent, Uno, and Weidman are analogous art relating to the same field. Weidman relates to semiconductor devices and methods of filling contact level features therein.” Ex. T, Weidman at Abstract; Ex. U, Weidman 800 at Abstract. Further, the '346 Patent, Uno, and Weidman are directed to similar problems. Weidman is also directed to the problem of providing “an improved contact level device that is void free, that has a low electrical resistance, that has good electromigration performance, that is reliable, and that can be reliably formed..” Ex. T, Weidman at 3:14-17; Ex. U, Weidman 800 at [0012]. Moreover, Weidman expressly teaches that “the contact level aperture 1510 can be filled with a metal, such as copper (Cu), nickel (Ni), cobalt (Co), ruthenium (Ru), tungsten (W) or combinations thereof.” Ex. T, Weidman at 10:7-10, Figure 5D; Ex. U, Weidman 800 at [0043]. Weidman further expressly teaches that “the barrier layer 1521 may contain a multilayer stack of metals, such as, Ti, TiN, Ti/TiN/W. Ti/TiN, Ti/W, Ta/TaN/W. Ta/W, Ni/W, and Co/W that have an additional catalytic layer deposited on the top surface so that an electroless layer can be deposited thereon. A typical catalytic layer that is deposited on these multilayer stacks may be a ruthenium (Ru), cobalt (Co), nickel (Ni), rhodium (Rh), iridium (Ir), palladium (Pd) or platinum (Pt) containing layer.” Ex. T, Weidman at 9:22-34, Figure 2C-G; Ex. U, Weidman 800 at [0040]. In addition, a POSITA would have known that a contact plug stacking Co/TiN/W has the advantage of maintaining the effective barrier properties of TiN. As such a POSITA would be motivated to combine Weidman with Uno and Zhang.

587. A POSITA would be further motivated to combine the Al alloy source metal having thicknesses larger than 3 μm of Kobayashi 174 with the power MISFET disclosed in Uno and the source wires of Zhang to arrive at the subject matter of Claim 7 of the '346 Patent. The '346 Patent, Kobayashi 174, and Uno are analogous art relating to the same field. Kobayashi 174 relates to a “vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) reduced in cell size.” Ex. J, Kobayashi 174 at [0001]. Further, the '346 Patent, Kobayashi 174, and Uno are directed to similar problems. Kobayashi 174 is directed to the problem of providing “a vertical MOSFET reduced in cell size without increasing V_t or a source resistance.” *Id.* at [0015]. Moreover, Kobayashi 174 expressly teaches methods of forming Al alloy source metals that have a thickness on the order of 4-6 μm . *Id.* at 9:30-53, Figures 8A-C. In addition, a POSITA would have known that Al alloy source metals with a certain thickness have the advantage of providing lower device access resistance. As such a POSITA would have been motivated to combine Kobayashi 174 with Uno and Zhang.

588. A POSITA would be further motivated to combine the P⁺ areas of Takemori with the power MISFET disclosed in Uno and the source wires of Zhang to arrive at the subject matter of Claim 17 of the '346 Patent. The '346 Patent, Uno, and Takemori are analogous art relating to the same field. Takemori relates to a “Power MOSFET semiconductor devices having a trench gate.” Ex. V, Takemori at 1:18-19. Further, the '346 Patent, Uno, and Takemori are directed to similar problems. Takemori is also directed to the problem of shifting threshold voltage in power MOSFETs with source contact trenches. *Id.* at 2:1-37. Moreover, Takemori expressly teaches methods of forming buried P⁺ diffusion regions that encompass the entire sidewalls of the source contact trench within P-body regions. *Id.* at 3:1-13, Figures 3-6, 18:42-19:50. In addition, a POSITA would have known that P⁺ areas enclosing the entire sidewalls of the source contact

trench within P-body regions has the advantage of providing lower contact resistance between the p-layer and the source thereby reducing the likelihood of activating the parasitic bipolar transistor.

As such a POSITA would be motivated to combine Takemori with Uno and Zhang.

2. Claim 1

- 1) [1.pre]. “A trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate, said trench MOSFET further comprising:”*

589. The preamble of Claim 1, which may be limiting, is disclosed in Uno. Uno teaches a trench MOSFET comprising a plurality of semiconductor power cells with each cell comprising a plurality of trench gates surrounded by a plurality of source regions of a first type conductivity above a plurality of body regions of second type conductivity above a drain region disposed on a bottom surface of a substrate. Uno specifically discloses that “[a]t first, as shown in FIG. 1, a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” Ex. W, Uno at 4:55-59.

590. Examination of Figure 38 from Uno would illustrate to a POSITA that it teaches the formation of a contract trench, with each plurality of trench gates forming the cells that are described in the preamble. “For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof.” *Id.* at 15:29-36. Figure 38 from Uno is include below for visual reference.

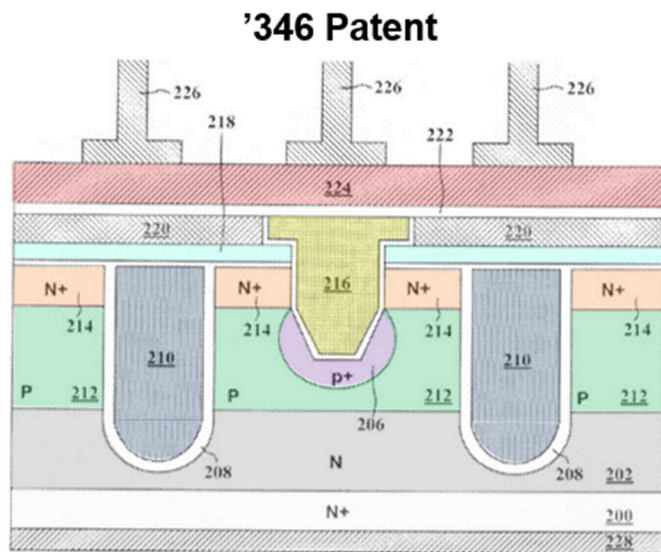


Fig. 2

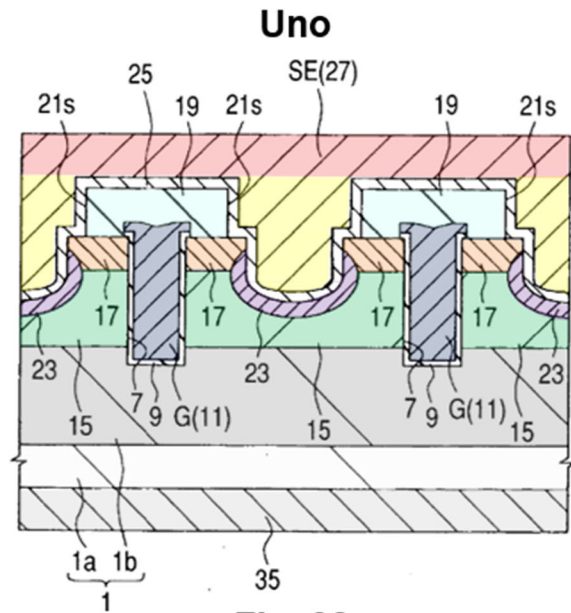


Fig. 38

224	Source metal	27
220	Barrier film	25
218	Silicon oxide film	19
216	Source contact trench	21s
214	Source region	17
206	P+ area	23
210	Trenched gates	11
212	P-body region	15
202	N epitaxial layer	1b
200	N+ substrate	1a
228	Drain metal	35

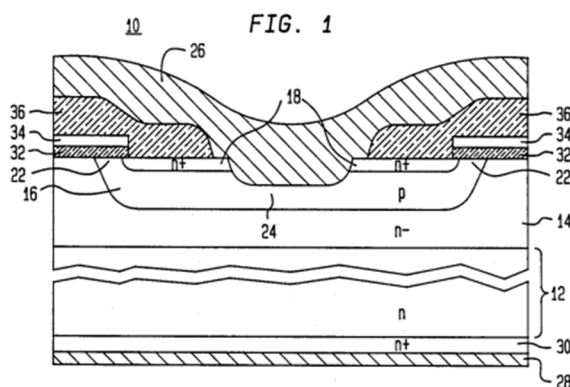
m) [1.a]. “a substrate of said first type conductivity,”

591. Uno also teaches the elements of a substrate of said first type conductivity. As stated in Uno, it discloses “a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” *Id.* at 4:55-59 . A POSITA would have understood that a selected substrate within a MOSFET will have a

given first conductivity, the conductivity of which should be the same for similarly selected elements.

n) [1.b]. “an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate;”

592. Uno, in view of Himelick, also teaches the elements of an epitaxial layer of said first type conductivity over said substrate, having a lower doping concentration than said substrate. “At first, as shown in FIG. 1, a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” *Id.* Himelick further describes the relevant doping concentration ratios for such a process, as seen by Figure 1 below.



Himelick, Figure 1

593. “Wafer 50 includes a moderately doped n – type substrate portion 52 (typically about 10^{18} donors per cubic centimeter) of sufficient thickness (typically about 25 mils) to provide mechanical strength and ruggedness to the wafer 50. An epitaxial layer 54 typically (1017 microns) of n – type conductivity (typically 10^{17} donors per cubic centimeter) is grown over wafer 50.” Ex. P, Himelick at 3:14-21. Further, a POSITA would have generally understood that the doping concentrations are a fundamental aspect of MOSFET design, and would have known that adjustment of doping ratios is an easy to implement tool in changing the design of a given product.

Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

o) [1.c]. “a plurality of trenches extending into said epitaxial layer, surrounded by a plurality of said source regions of said first type conductivity above said body regions of said second type conductivity;”

594. Uno also teaches the elements of Claim 1 described here. Examination of Figure 38 demonstrates the extension of the trenches (7) into the epitaxial layer that is described above. Further, it would be well understood by a POSITA that the source regions and the body regions would be of a different conductivity level, as this is a common principle in the manufacture of MOSFETs, and is critical to the design fundamentals of the same.

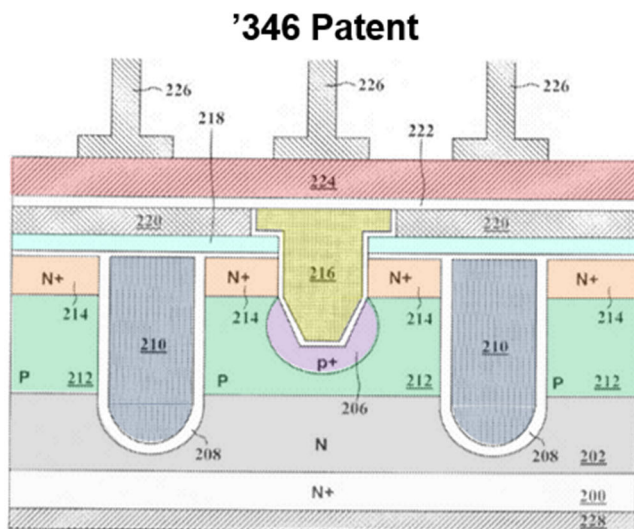


Fig. 2

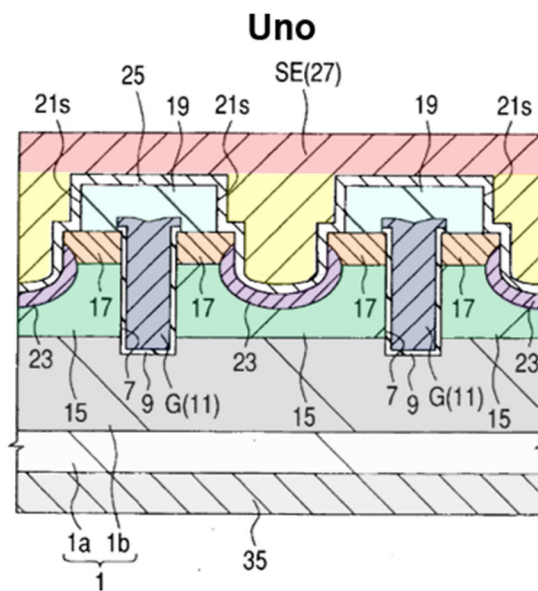
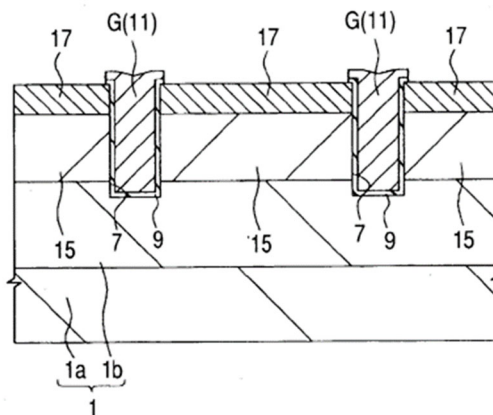


Fig. 38

224	Source metal	27
220	Barrier film	25
218	Silicon oxide film	19
216	Source contact trench	21s
214	Source region	17
206	P+ area	23
210	Trenched gates	11
212	P-body region	15
202	N epitaxial layer	1b
200	N+ substrate	1a
228	Drain metal	35

595. “For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof” Ex. W, Uno at 15:29-36.



Uno, Figure 5

596. *Id.* at Figure 5. “Then, as shown in FIG. 5, using a not illustrated resist film as a mask, a p-impurity is implanted and diffused into the substrate 1 between the trenches 7 to form a p⁻-semiconductor region (channel region, well) 15. The bottom of the trench 7 is at a position deeper than the p⁻-semiconductor region 15.” *Id.* at 5:20-25.

p) [1.d]. “a first insulating layer lining said trenches as gate oxide;”

597. Uno also teaches the elements of Claim 1 described here. Uno describes a process whereby “a heat treatment is applied to the substrate 1 to form a thermal oxide film 9 to the bottom and the side of the trenches 7. The thermal oxide film 9 forms a gate dielectric film for a power MISFET. Then, a polycrystal silicon film 11 of low resistance doped with an impurity is deposited to an extent of burying the trenches 7. In this process, the polycrystal silicon film 11 is deposited in a layerous form at the periphery of a device forming region not formed with the trench.” *Id.* at [0073]. A POSITA would have understood that the thermal oxide film described in the above

process is equivalent to the insulating gate oxide layer described in Claim 1, due to both the description within Uno as well as the general knowledge in the field.

q) [1.e]. “a doped polysilicon of said first type conductivity as said trench gates overlying said first insulating layer;”

598. Uno additionally teaches the elements of Claim 1 described here. Uno describes a process whereby a “a heat treatment is applied to the substrate 1 to form a thermal oxide film 9 to the bottom and the side of the trenches 7. The thermal oxide film 9 forms a gate dielectric film for a power MISFET. Then, a polycrystal silicon film 11 of low resistance doped with an impurity is deposited to an extent of burying the trenches 7. In this process, the polycrystal silicon film 11 is deposited in a layerous form at the periphery of a device forming region not formed with the trench.” *Id.* at 5:1-9. This process explicitly describes the doping of a polysilicon film that is applied atop the first insulating layer discussed above.

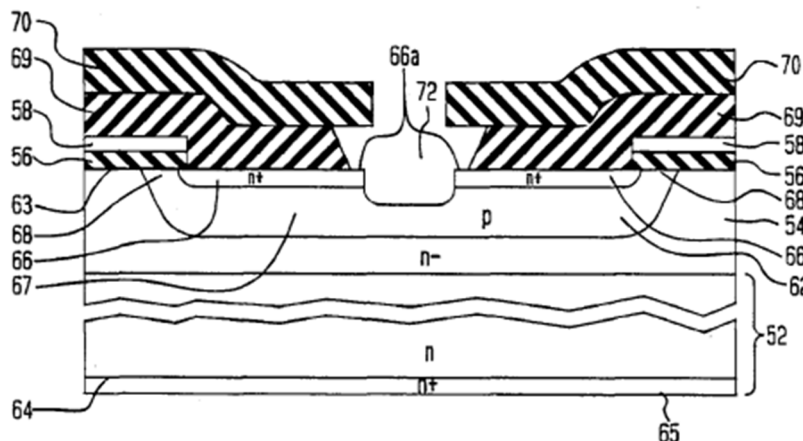
r) [1.f]. “a second insulating layer disposed over said epitaxial layer to isolate a source metal which contacts said both source and body regions, from said doped polysilicon as said trench gates;”

599. Uno teaches this element of Claim 1 as well. This element describes the second insulating layer being used to isolate a source metal contacting both the source and body regions, operating as the defined trench gates. Uno describes that “after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof.” *Id.* at 15:31-36. A POSITA would have understood that the trench formation as it is described in the prior art, and suggest by the claim language, necessarily requires the formation of the second insulating layer as part of the process. If this second insulating layer were not included, the gate node would become connected to the source node, preventing proper operation of the MOSFET.

s) [1.g]. “a plurality of source contact trenches penetrating through said second insulating layer and said source regions with vertical sidewalls substantially perpendicular to a top epitaxial surface within said source regions, and further extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer;”

600. Uno teaches the elements of Claim 1.g. As discussed above, Uno discloses the plurality of source contact trenches penetrating through the claimed design – “For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof.” *Id.*

601. Himelick also discloses a contact trench – “a via 72 (typically about 5 microns wide) through a central portion of the layer 66 [] exposes a central body diode portion of the p-type well 62.” *Id.* at 4:63-66. As shown in Figure 2G below, the via 72 penetrates through the phosphosilicate glass layer 69 and n⁺ type source regions 66 with vertical sidewalls. In the p-well, “[i]t is chosen also to leave sloping curved walls in the via which are less vertical than would result from a more anisotropic reactive ion etch. Such curved sloping in the sidewalls of the via 72 is desirable to permit better filling of the via 72 by the subsequent metallization.” *Id.* at 5:4-10.

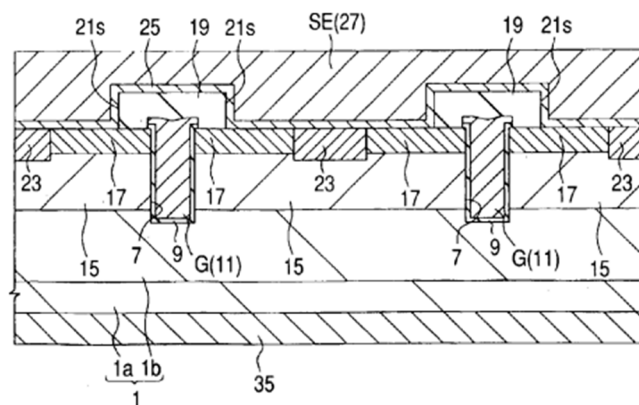


Himelick, Figure 2G

602. Himelick further describes the dimensions and reach of a contact trench. “[A] first feature of the preferred embodiment of the invention involves stripping the back surface of the wafer to bare such back surface earlier than was customary in the past. Subsequently, a common phosphorous diffusion operation can be used to form a heavily doped layer on the bared back surface, to dope the polysilicon gate electrode layer, and to form the n – type source region. This permits elimination of at least one mask operation from previous practice. Additionally, a second feature of the invention is the use of the source region contact mask as a shadow mask in the substantially anisotropic etching of a via through the n – type source region to the underlying body diode region of the underlying p – type well. This permits a later deposited source electrode to also serve as a shorting contact to this body diode region.” Ex. P, Himelick at 5:56-6:3. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

t) [1.h]. “a front metal disposed on the front surface of said trench MOSFET as said source metal;”

603. Uno singularly teaches the elements described in this portion of the claim. Examination of Figure 12 from Uno demonstrates the presence of front metal (SE27) disposed on the front surface of the trench MOSFET.



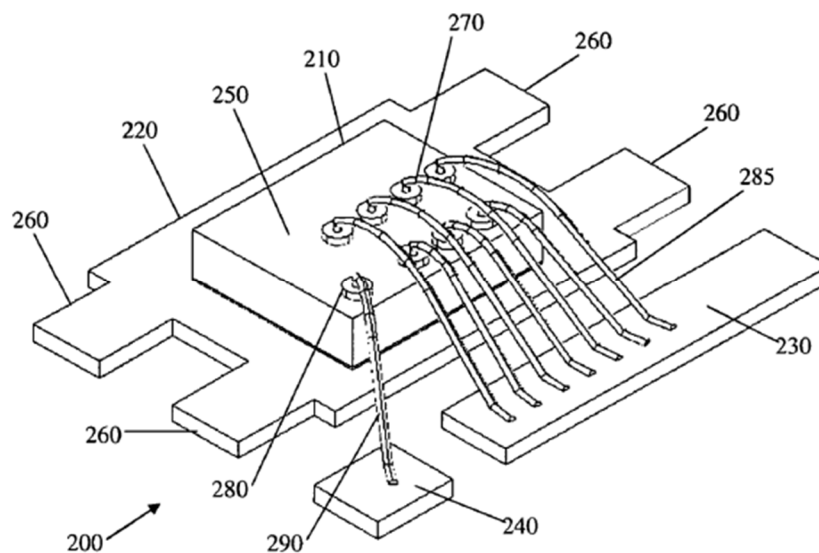
Uno, Figure 12

u) [1.i]. “a backside metal disposed on the backside of said substrate as a drain metal;”

604. Uno singularly teaches the elements described in this portion of the claim. Examination of Figure 12 from Uno demonstrates the presence of backside metal (35) disposed on the front surface of the trench MOSFET.

v) [1.j]. “at least one copper wire electrically bonded to said source metal.”

605. The bonding of at least one copper wire to the source metal is a common concept from within the field that would be understood by a POSITA, but that is also clearly demonstrated in a variety of publications, such as Zhang and the ESEMI article on “Copper Wirebonding.” Zhang discloses the use of copper wires in connecting to the source. “The source lead 230 (FIG. 2A) may be larger than in conventional semiconductor packages to enable the use of an increased number of source wires 285 which preferably are formed from gold or copper. Increasing the number of source wires 285 advantageously decreases the semiconductor package 200 resistance significantly.” Ex. Q, Zhang at 4:21-26; Ex. Y, Zhang 318 at [0035]. See Figure 2A from Zhang below.



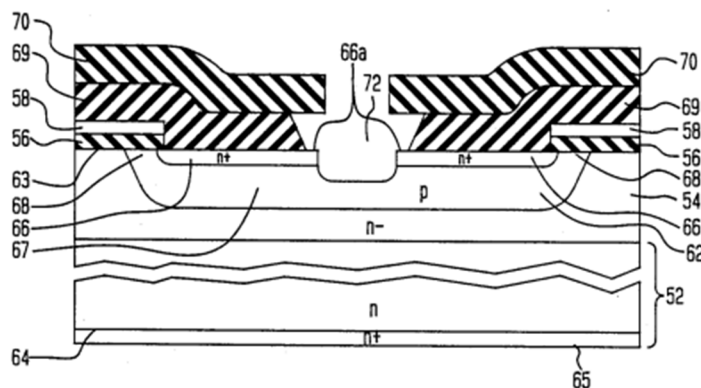
Zhang, Figure 2A

606. EESEMI also describes this concept, and its commonality within the field. “Copper is rapidly gaining a foothold as an interconnection material in semiconductor packaging because of its obvious advantages over gold. These advantages include: 1) cost reduction of up to 90%; 2) superior electrical and thermal conductivity; 3) less intermetallic growths; 4) greater reliability of the bond at elevated temperatures; and 5) higher mechanical stability.” Ex. R, EESEMI at 1. A POSITA would have a general understanding of selection of bonding wire materials and the impact that would have on design. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

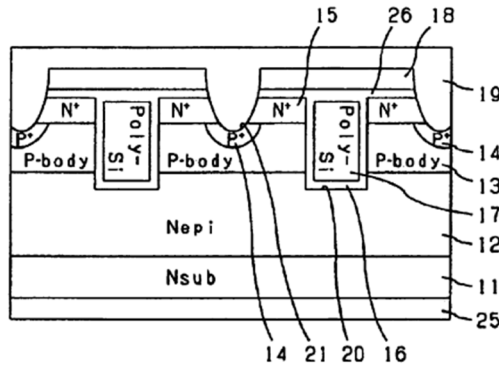
3. Claim 2: “The trench MOSFET of claim 1, wherein the angle between said source contact trench walls and said top surface of said epitaxial layer is $90^{\circ} \pm 5^{\circ}$ degrees within said source regions, and is less than 85° degrees within said body regions.”

607. Claim 2 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Takemori and Himelick.

608. Takemori and Himelick may both be considered, via review of the diagrams and depictions within, to see that the angle between the source contact trench walls and the epitaxial layer are approximately 90° within the source region and less than 85° in the body.



Himelick, Figure 2G



Takemori, Figure 6

Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

- 4. Claim 3: “The trench MOSFET of claim 1, wherein said second insulating layer is a combination of SRO and PSG or BPSG to further reduce source contact resistance, and each of said source contact trenches has a wider contact width in said PSG or said BPSG than in said SRO.”**

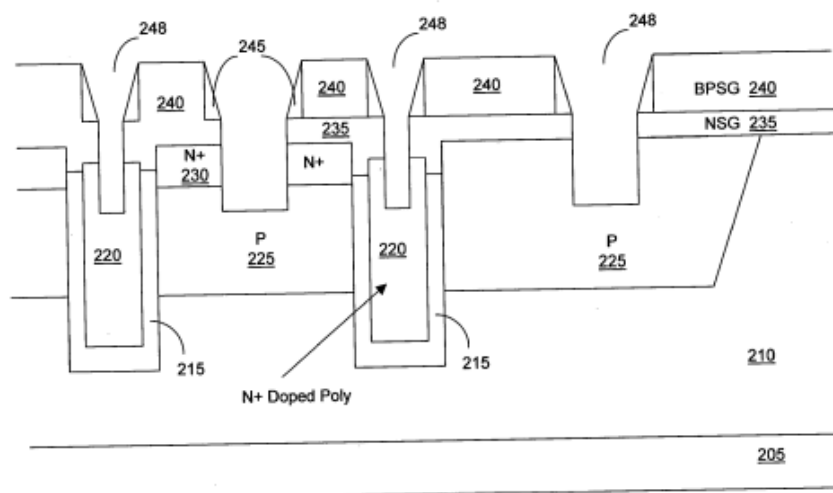
609. Claim 3 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Takemori, or Hsieh 382.

610. In multiple locations, Takemori discusses the use of different film materials, such as those mentioned in the claim above, in the design of a MOSFET device. “In the figures, reference symbol 11 indicates an N⁺-type silicon substrate, 12 an N⁻-type epitaxial layer, 13 a P-type body layer, 14 a buried P⁺-type diffusion region, 15 an N⁺-type source region, 16 a gate insulating film, 17 a gate electrode film, 18 a borophosphosilicate glass (BPSG) film, 19 a source electrode film, 20 a gate trench, 21 a source trench, 25 a drain electrode film, and 26 an insulating film.” *Id.* at 15:24-31. “Moreover, a different insulating film in the form of BPSG film 18 is formed on the surface of insulating film 26. Furthermore, gate trench 20 may be formed to be deeper as necessary, and conversely, and may be formed so that its depth is at about the same location or

slightly shallower than the interface between N⁻-type epitaxial layer 12 and P-type body layer 13.”
Id. at 15:54-62.

611. The use of further substitute materials, in order to achieve different source contact resistances by manipulating the cross-sectional shape of the source contact trench, is a common concept that a POSITA would have known and understood how to apply. It is common practice in dry etch optimization to use materials of varying density (porosity) as masking features to shape the underlying trench.

612. Hshieh 382 similarly discusses the use of such material in design of MOSFET devices. “The source regions 130 are formed near the top surface of the epitaxial layer surrounding the trenched gates 125. The top surface of the semiconductor substrate extending over the top of the trenched gate, the P body regions 125 and the source regions 130 are covered with a NSG layer 135, a BPSG protective layers 140 and another insulation NSG layer 145.” Ex. S, Hshieh 382 at [0020]. “In FIG. 3I, dry oxide etch is first carried out to etch through the NSG layer 235 followed by a silicon etch to etching into the gate polysilicon 220 and the body regions 225 in the epitaxial layer 210 to form a funnel-shaped trench 248 with a broad top and a narrow-bottom.” *Id.* at [0024]. Figure 3I from Hshieh 382 is included below for further reference.



Hshieh 382, Figure 3I

613. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

5. Claim 4: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Ti/TiN/W.”

614. Claim 4 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Hshieh 382.

615. Hshieh 382 explicitly teaches “For the purpose of improving the gate metal contact for reducing the gate resistance and improving the gate contact and also to reduce the source contact area, the gate contact trench 170 and 175 and the source contact trenches 180 and 85 are formed. The gate contact trench 170 and 175 and the source contact trenches 180 and 185 are filled with barrier layer composed of Ti/TiN and tungsten plug wherein the barrier layer composed of Ti/TiN surrounds the tungsten plug.” *Id.* at [0022]. Hshieh 382 also discusses the use of W in other processes within its described design. “Then an etch-back process is carried out to remove the Ti/TiN/W from the top of the contact plug trenches.” *Id.* at [0024]. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

6. Claim 5: “The trench MOSFET of claim 1, wherein said source contact trenches are filled with Co/TiN/W.”

616. Claim 5 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Weidman.

617. Weidman generally discusses the use of a variety of common materials in the MOSFET design process, which includes use of certain materials for filling the source contact trenches. “In general the deposited metal layer 1513 may contain one or more of the following elements nickel (Ni), titanium (Ti), tantalum (Ta), cobalt (Co), molybdenum (Mo) or tungsten (W).

The metal layer 1513 may be selectively or non-selectively deposited using a conventional ALD or CVD deposition process. Also, the metal layer 1513 may be non-selectively deposited using a conventional PVD deposition process.” Ex. T, Weidman at 6:4-11.

618. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter, and would have understood the selection of different elements to fill the source contact trenches is a common consideration in MOSFET design.

7. Claim 6: “The trench MOSFET of claim 1, wherein said source metal is Al alloys, Ti/Ni/Ag or Cu.”

619. Claim 6 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Uno.

620. Uno discusses the use of various elements for the creation of different films and layers in the design of its discusses MOSFETs. See, e.g. “Successively, an aluminum (Al) film 27, for example, is deposited as a conductive film to about 5 μm by sputtering. The barrier film is formed for preventing silicon in the substrate 1 from depositing into the Al film 27. The Al film may also comprise Al as a main ingredient and it may also contain other metals.” Ex. W, Uno at 7:1-6. “Among them, since Ti is a metal often used in the field of semiconductors and various studies have been made for the characteristics thereof, it is used suitably as the barrier film. Further, various film deposition methods have also been studied and films can be deposited easily, for example, by using a sputtering apparatus. Further, it is inexpensive to reduce the production cost of the apparatus. In addition to Ti, TiN (titanium nitride) may also be used.” *Id.* at 13:3-10.

621. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter, and they would have understood the selection of different elements to fill the source contact trenches is a common consideration in MOSFET design.

8. Claim 7: “The trench MOSFET of claim 1, wherein said source metal Al alloys have thicknesses larger than 3 μm .”

622. Claim 7 is dependent on Claim 1, so all of the present elements discussed above are similarly taught in regards to Claim 2, as explained by Uno, Takemori, Himelick, etc. The additional elements of this claim are further taught by Kobayashi 174.

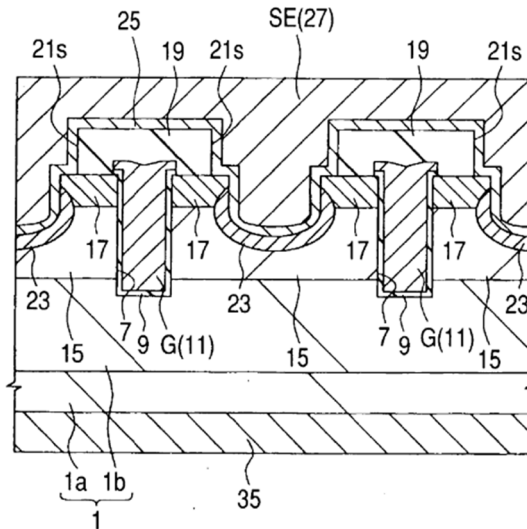
623. Kobayashi 174 discusses the selection of a source electrode thickness on the order of 4-6 μm , just above the 3 μm mentioned in the claim. “The source electrode 18 is preferably as thick as possible in order to reduce the resistance component of AlSi or AlSiCu. Practically, the source electrode 18 has a thickness on the order of 4-6 μm .” Ex. J, Kobayashi 174 at 9:38-43.

624. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter, and they would have understood the connotations of adjustments of the dimensions of different elements within the MOSFET to achieve specific design parameters.

9. Claim 16

1) [16.pre]. “A trench MOSFET comprising:”

625. The preamble of Claim 16, which may be limiting, is disclosed in Uno. Uno teaches the design of a trench MOSFET. “Then, the substrate 1 is etched to form trenches 7 by using a film patterned by using photolithography (not illustrated) as a mask. FIG. 2 shows an example of a pattern for the trenches 7. As shown in the drawing, trenches 7 are arranged so as to surround the periphery of plural octagonal patterns. The width of the trench 7 is, for example, about 0.5 μm . FIG. 1 corresponds, for example, to A-A cross section in FIG. 1.” Ex. W, Uno at 4:60-67. The whole of Uno is, in fact, teaches the development of a trench MOSFET. Figure 38 from Uno is included for visual reference.

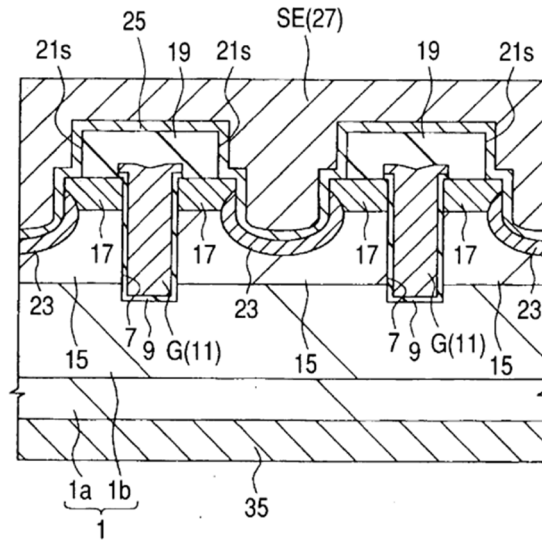


m) [16.a]. “a substrate”

626. Uno also teaches the elements of a substrate. As stated in Uno, it discloses “a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” *Id.* at 4:55-59. A POSITA would also commonly understand that MOSFET design involves the selection of substrates.

n) [16.b]. “a drain metal below said substrate;”

627. Uno also teaches the elements of a drain metal being found below said substrate. Examination of Figure 38 clearly demonstrates the presence of a drain region (1a, 1b). Further a POSITA would also commonly understand that MOSFET design involves the presence of a drain region.



Uno, Figure 38

o) [16.c]. “an n epitaxial layer formed on said substrate;”

628. Uno additionally teaches the elements of an epitaxial layer formed on the substrate. “At first, as shown in FIG. 1, a semiconductor substrate 1 in which a single crystal silicon layer 1b doped with an n-impurity (for example, phosphorus) is epitaxially grown on the surface of an n-single crystal silicon substrate 1a (hereinafter simply referred to as “substrate”) is provided.” *Id.*

p) [16.d]. “P-body regions formed on said n epitaxial layer;”

629. Uno additionally teaches the elements of a P-body region formed on the epitaxial layer. Examination of Figure 38 clearly demonstrates the presence of a body region, and a POSITA would also commonly understand that MOSFET design involves the presence of a body region. A POSITA would have generally understood that the conductivity type options are limited to P-type or N-type channel MOSFETs. A POSITA would also have known that there are only two conductivity types and would know how to alter a design to account for P-channel or N-channel MOSFET as needed.

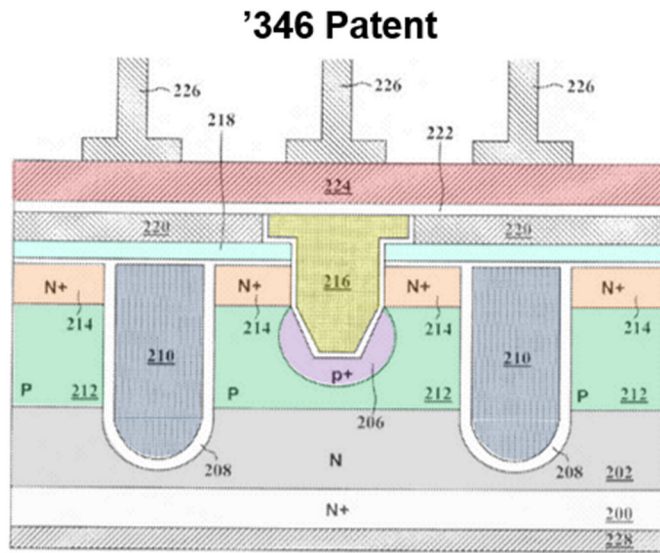


Fig. 2

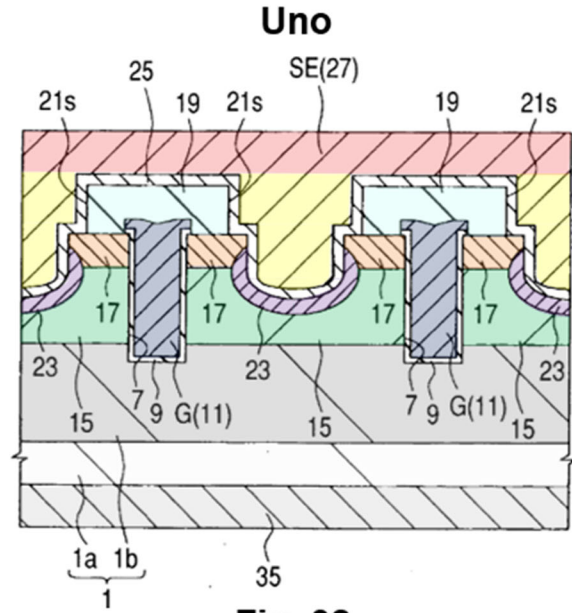


Fig. 38

224	Source metal	27
220	Barrier film	25
218	Silicon oxide film	19
216	Source contact trench	21s
214	Source region	17
206	P+ area	23
210	Trenched gates	11
212	P-body region	15
202	N epitaxial layer	1b
200	N+ substrate	1a
228	Drain metal	35

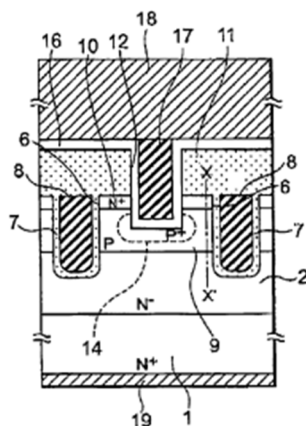
q) [16.e]. "N+ source regions formed on said P-body regions;"

630. Uno additionally teaches the elements of an N+ source region formed on the body region. Examination of Figure 38 clearly demonstrates the presence of a source region, and a POSITA would also commonly understand that MOSFET design involves the presence of a source region. A POSITA would have generally understood that the conductivity type options are limited to P-type or N-type channel MOSFETs. A POSITA would also have known that there are only

two conductivity types and would know how to alter a design to account for P-channel or N-channel MOSFET as needed.

r) [16.f]. “a plurality of insulating layers formed on said N⁺ source regions;”

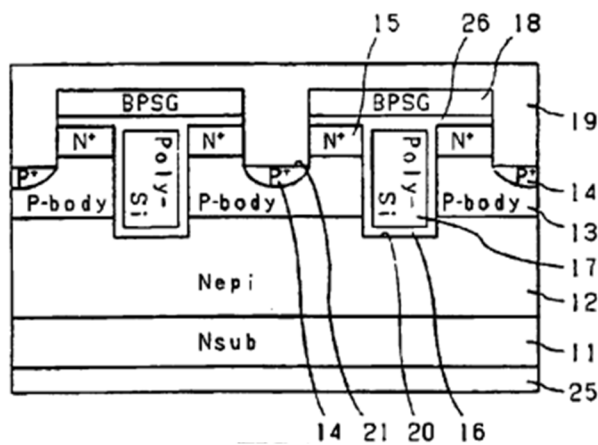
631. This element of the Claim is taught by both Kobayashi 174 and Takemori. Kobayashi 174 generally describes the formation of multiple insulation layers as it walks through the embodiment laid out in Figure 5A from the same. “Referring to FIG. 5A, a UMOSFET according to a first embodiment of this invention comprises an N⁺-type silicon substrate 1 and an N⁻-type epitaxial layer 2 formed on one surface of the N⁺-type silicon substrate 1. A P-type base layer 9 and an N⁺-type source layer 10 are formed on a surface of the N⁻-type epitaxial layer 2. A combination of the substrate 1 and the layer 2, 9, and 10 constitutes a silicon layer having silicon surface opposite to each other.” Ex. J, Kobayashi 174 at 6:46-53.



Kobayashi 174, Figure 5A

632. In walking through its Figure 1, Takemori similarly describes a multitude of layers. “In addition, FIGS. 2A and 2B are explanatory views showing a source trench and its vicinity in a semiconductor device according to a first embodiment of the present invention along with the constitution of said section of a semiconductor device according to the prior art for comparison, with FIG. 2A showing a source trench and its vicinity in a semiconductor device according to a

first embodiment of the present invention, and FIG. 2B showing the constitution of said section of a semiconductor device according to the prior art for comparison. In the figures, reference symbol 11 indicates an N^+ -type silicon substrate, 12 an N^- -type epitaxial layer, 13 a P-type body layer, 14 a buried P^+ -type diffusion region, 15 an N^+ -type source region, 16 a gate insulating film, 17 a gate electrode film, 18 a borophosphosilicate glass (BPSG) film, 19 a source electrode film, 20 a gate trench, 21 a source trench, 25 a drain electrode film, and 26 an insulating film.” Ex. V, Takemori at 15:14-32.



Takemori, Figure 1

633. Further, it would be obvious to a POSITA to combine these elements with the elements described in Uno to arrive at the given claim language.

s) [16.g]. “a source metal formed on said insulating layers;”

634. Uno singularly teaches this element of the claim. Examination of Figure 38 clearly demonstrates the presence of a source region, and a POSITA would also commonly understand that MOSFET design involves the presence of a source region, as well as the fact that such source region is situated against the insulating layers described above.

'346 Patent

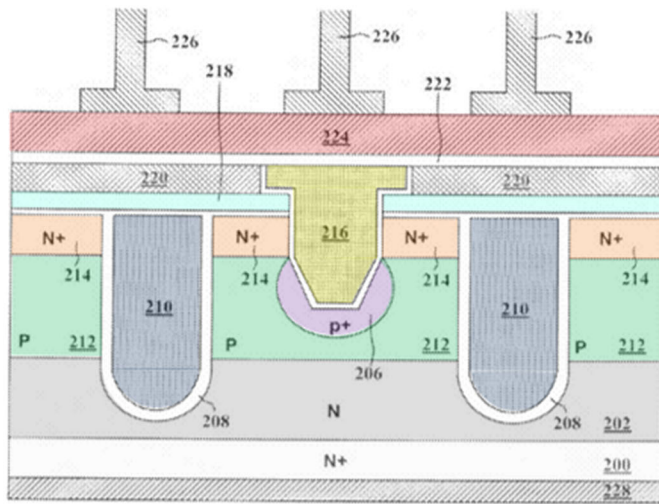


Fig. 2

Uno

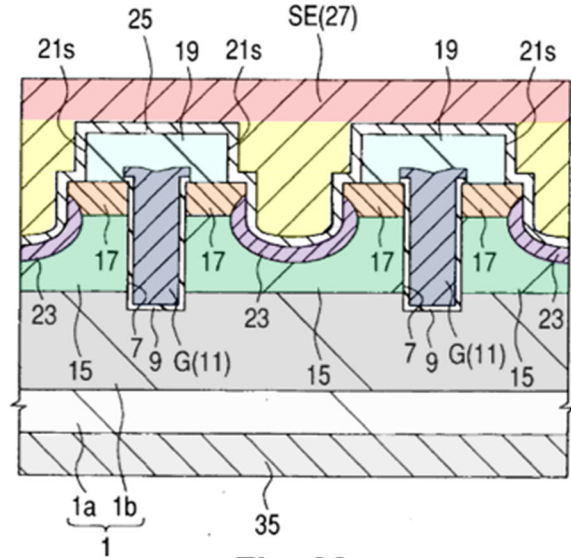


Fig. 38

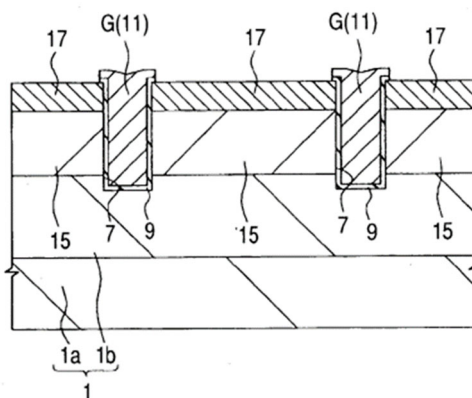
224	Source metal	27
220	Barrier film	25
218	Silicon oxide film	19
216	Source contact trench	21s
214	Source region	17
206	P+ area	23
210	Trenched gates	11
212	P-body region	15
202	N epitaxial layer	1b
200	N+ substrate	1a
228	Drain metal	35

t) [16.h]. “trench gates extending through said N+ Source regions, said P-body regions and said n epitaxial layer;

635. Uno also teaches the elements of Claim 16 described here. Examination of Figure 38 demonstrates the extension of the trenches (7) into the epitaxial layer that is described above. Further, it would be well understood by a POSITA that the source regions and the body regions would be of a different conductivity level, as this is a common principle in the manufacture of MOSFETs, and is critical to the design fundamentals of the same.

636. “For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact) 21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof” Ex. W, Uno at 15:31-36.

637. *Id.* at Figure 5. “Then, as shown in FIG. 5, using a not illustrated resist film as a mask, a p-impurity is implanted and diffused into the substrate 1 between the trenches 7 to form a p⁻-semiconductor region (channel region, well) 15. The bottom of the trench 7 is at a position deeper than the p⁻-semiconductor region 15.” *Id.* at 5:20-25.



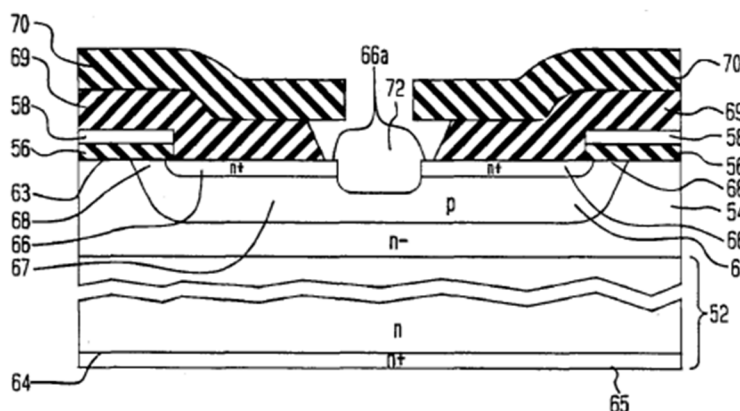
Uno, Figure 5

u) [16.i]. “a plurality of trench source contacts comprising a plurality of sidewalls, two of said sidewalls substantially perpendicular to a top surface of said source regions and two other sidewalls tapered with respect to said source regions, wherein said trench source contacts extend through said insulating layers, said N⁺ Source regions, said P-body regions and said n epitaxial layer, and”

638. Uno, when combined with Himelick under the knowledge of a POSITA, teaches the elements of Claim 16 described here. As discussed above, Uno discloses the plurality of source contact trenches penetrating through the claimed design – “For example, after forming a silicon oxide film 19 as shown in FIG. 6, the silicon oxide film 19 and the substrate 1 (p⁻-semiconductor region 15 and n⁺-semiconductor region 17) are etched to form a contact trench (source—contact)

21s and, further, the bottom of the contact hole 21s is isotropically etched to round the bottom thereof.” *Id.* at 15:31-36 .

639. Himelick also discloses a contact trench – “a via 72 (typically about 5 microns wide) through a central portion of the layer 66 [] exposes a central body diode portion of the p-type well 62.” *Id.* at 4:63-66. As shown in Figure 2G below, the via 72 penetrates through the phosphosilicate glass layer 69 and n+ type source regions 66 with vertical sidewalls. In the p-well, “[i]t is chosen also to leave sloping curved walls in the via which are less vertical than would result from a more anisotropic reactive ion etch. Such curved sloping in the sidewalls of the via 72 is desirable to permit better filling of the via 72 by the subsequent metallization.” *Id.* at 5:4-10.



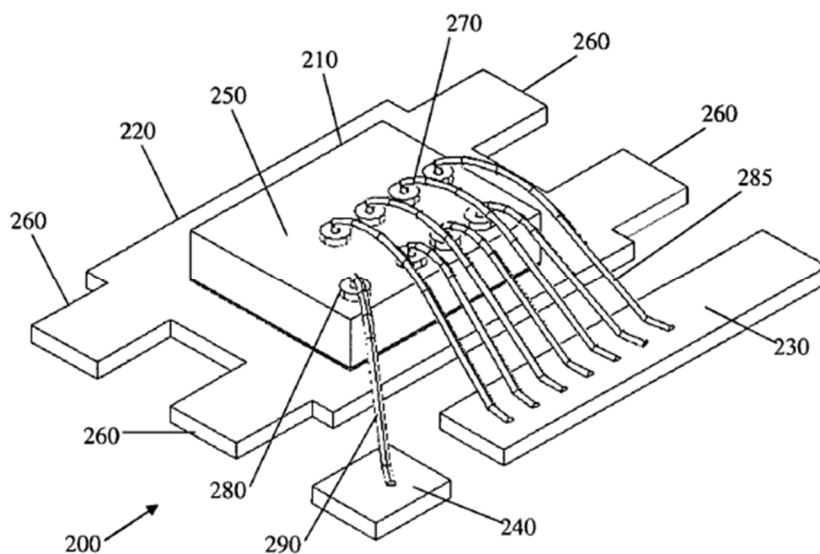
Himelick, Figure 2G

640. Himelick further describes the dimensions and reach of a contact trench. “[A] first feature of the preferred embodiment of the invention involves stripping the back surface of the wafer to bare such back surface earlier than was customary in the past. Subsequently, a common phosphorous diffusion operation can be used to form a heavily doped layer on the bared back surface, to dope the polysilicon gate electrode layer, and to form the n – type source region. This permits elimination of at least one mask operation from previous practice. Additionally, a second feature of the invention is the use of the source region contact mask as a shadow mask in the substantially anisotropic etching of a via through the n – type source region to the underlying body

diode region of the underlying p – type well. This permits a later deposited source electrode to also serve as a shorting contact to this body diode region.” Ex. P, Himelick at 5:56-6:3. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

v) ***[16.j]. “copper wire electrically bonded to said source metal.”***

641. The bonding of at least one copper wire to the source metal is a common concept from within the field that would be understood by a POSITA, but that is also clearly demonstrated in a variety of publications, such as Zhang and the ESEMI article on “Copper Wirebonding.” Zhang discloses the use of copper wires in connecting to the source. “The source lead 230 (FIG. 2A) may be larger than in conventional semiconductor packages to enable the use of an increased number of source wires 285 which preferably are formed from gold or copper. Increasing the number of source wires 285 advantageously decreases the semiconductor package 200 resistance significantly.” Ex. Q, Zhang at 4:21-26; Ex. Y, Zhang 318 at [0035]. Figure 2A from Zhang is reproduced below.



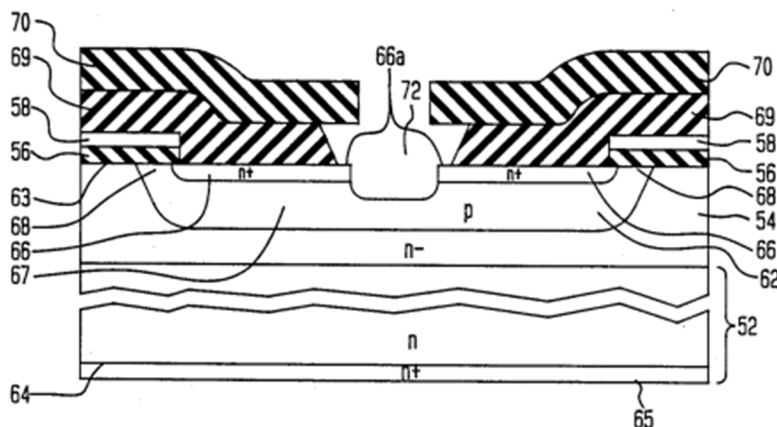
Zhang, Figure 2A

642. EESEMI also describes this concept, and its commonality within the field. “Copper is rapidly gaining a foothold as an interconnection material in semiconductor packaging because of its obvious advantages over gold. These advantages include: 1) cost reduction of up to 90%; 2) superior electrical and thermal conductivity; 3) less intermetallic growths; 4) greater reliability of the bond at elevated temperatures; and 5) higher mechanical stability.” Ex. R, EESEMI. A POSITA would have a general understanding of selection of bonding wire materials and the impact that would have on design. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

10. Claim 17: “The trench MOSFET of claim 16, further comprising P+ areas wrapping said sidewalls and bottom of said trench Source contacts within said P-body regions and an angle between said trench source contact sidewalls and said source region is $90^{\circ} \pm 5^{\circ}$ degrees within said source regions, and is less than 85° degrees within said P-body regions.”

643. Claim 17 is dependent on Claim 16 so all of the present elements discussed above are similarly taught in regards to Claim 16, as explained by Uno, Takemori, Kobayashi 174, etc. The additional elements of this claim are further taught by Takemori and Himelick.

644. Takemori and Himelick may both be considered, via review of the diagrams and depictions within, to see that the angle between the source contract trench walls and the epitaxial layer are approximately 90° within the source region and less than 85° in the body.



Himelick, Figure 2G

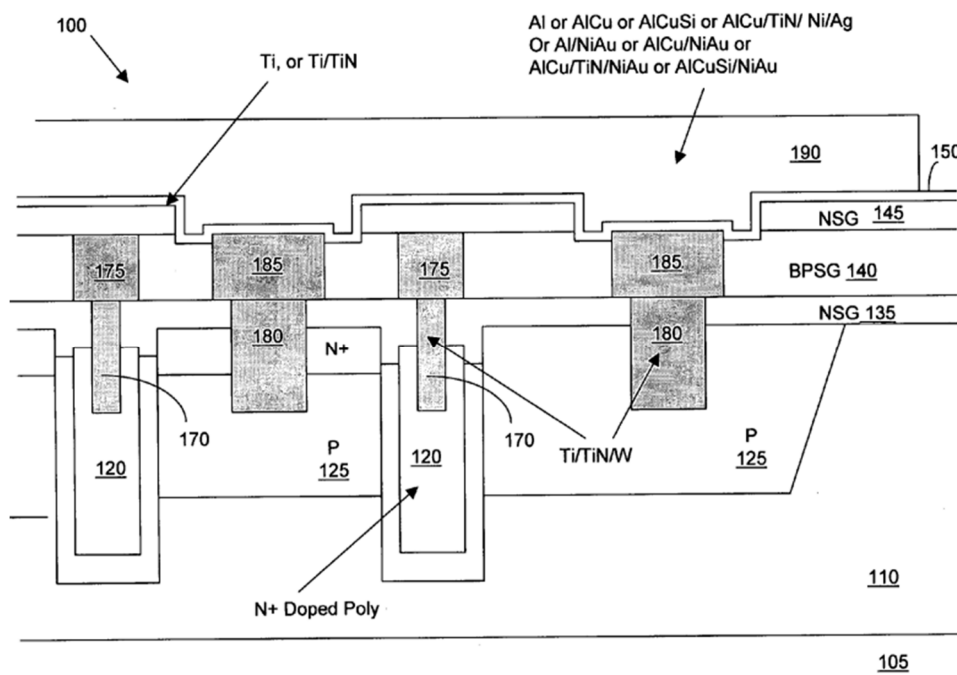


11. Claim 18: “The trench MOSFET of claim 16, further comprising an interconnection layer between said source metal and an upper insulating layer.”

647. Hshieh 382 teaches an interconnecting layer, as is described in Figure 2 of the same.

“Please refer to FIG. 2 for a cross sectional view of a preferred embodiment of this invention where a metal oxide semiconductor field effect transistor (MOSFET) device 100 is supported on a substrate 105 formed with an epitaxial layer 110. The MOSFET device 100 includes a trenched gate 120 disposed in a trench with a gate insulation layer 115 formed as a liner layer covering the walls of the trench. A body region 125 that is doped with a dopant of second conductivity type, e.g., P-type dopant, extends between the trenched gates 120. The P-body regions 125 encompassing a source region 130 doped with the dopant of first conductivity, e.g., N⁺ dopant. The source regions 130 are formed near the top surface of the epitaxial layer surrounding the trenched gates 125. The top surface of the semiconductor substrate extending over the top of the trenched gate, the P body regions 125 and the source regions 130 are covered with a NSG layer

135, a BPSG protective layers 140 and another insulation NSG layer 145.” Ex. S, Hshieh 382 at [0020].



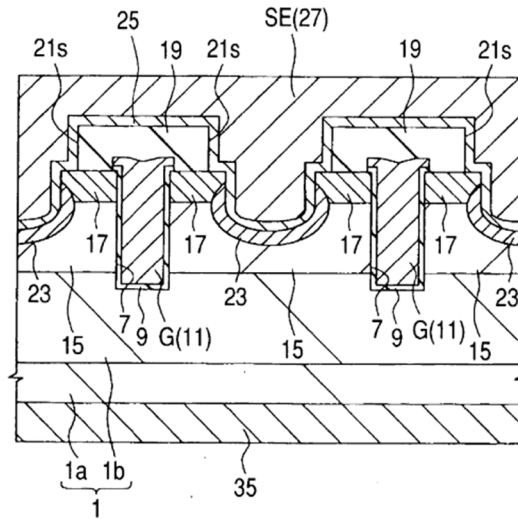
Hshieh 382, Figure 2

648. A POSITA would have understood that the NSG layer 135, the BPSG protective layers 140 the additional insulation NSG layer 145 are equivalent to the interconnections and upper insulating layers described in the claim. Further, it would have been obvious to a POSITA to combine the different elements here to form the claimed subject matter.

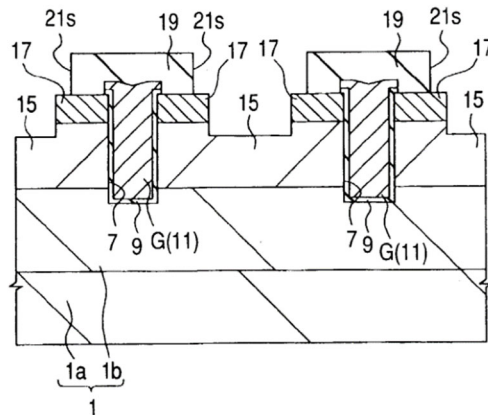
12. Claim 19: “The trench MOSFET of claim 16, wherein said source metal vertically connects to said N+ source regions and said P-body regions.”

649. Claim 19 is dependent on Claim 16 so all of the present elements discussed above are similarly taught in regards to Claim 16, as explained by Uno, Takemori, Kobayashi 174, etc. The additional elements of this claim are further taught by Uno.

650. Examination of both Figure 38 and Figure 6 demonstrate that the source metal from the embodiment described in Uno is vertically connected to the N+ source region and the P-body regions .



Uno, Figure 38

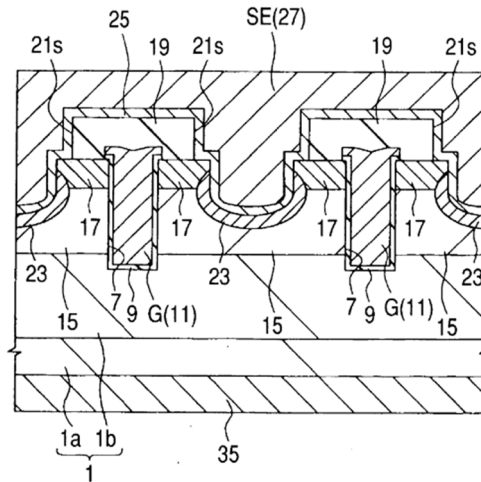


Uno, Figure 6

13. Claim 20: “The trench MOSFET of claim 16, wherein said trench source contact narrows towards the P+ areas.”

651. Claim 20 is dependent on Claim 16 so all of the present elements discussed above are similarly taught in regards to Claim 16, as explained by Uno, Takemori, Kobayashi 174, etc. The additional elements of this claim are further taught by Uno.

652. Uno describes a rounding of the contact trench, such that the contact would have to narrow as it approaches the P+ areas. “Further, in FIG. 38, the bottom of the contact trench 21s is rounded.” Ex. W, Uno at 15:29-30.



Uno, Figure 38

XIII. INVALIDITY UNDER 35 U.S.C. § 112

653. Claim 6 (and the claims dependent thereon) of the '634 Patent lack adequate written description and/or enablement at least because nothing from the figures or description provides embodiments where the doping polarities are reversed. The '634 Patent merely states at Col. 2, lines 16-20 and Col. 4, lines 46-49 that “by inverting the conductive type, this invention is also applicable to a P-channel MOSFET structure.” But this statement does not sufficiently disclose the features at claims 6-9 of the '634 patent. In particular, there is no disclosure or explanation as to how, why, or whether inverting the doping polarities would lead to the desired outcome of achieving avalanche improvement (*see, e.g.*, '634 Patent at Field of Invention; Col. 2, lines 23-34). Moreover, a person having ordinary skill in the art would be aware that reversing the doping polarity impacts mobility of holes and electrons. Accordingly, the disclosure of the '634 Patent does not reasonably convey to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date. And the disclosure of the '634 Patent does not enable those skilled in the art to make and use the full scope of the claimed invention without undue experimentation.

654. Claim 1 (and the claims dependent thereon) of the '346 Patent lack adequate written description and/or enablement at least at least for the following reasons. Claim 1 requires “a plurality of source contact trenches . . . extending into said body regions with tapered sidewalls with respect to said top surface of said epitaxial layer.” And claim 16 requires “two other sidewalls tapered with respect to said source regions.” However, the '346 Patent does not contain sufficient disclosure to teach those skilled in the art how to make and use the “tapered sidewalls” / “sidewalls tapered” without undue experimentation. And the disclosure of the '346 Patent does not reasonably convey to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.

XIV. INEQUITABLE CONDUCT

A. Failure to Disclose U.S. Patent Publication No. 2006/0273384 (“Hshieh 384”)

655. I understand that ASUS is asserting that the '634 Patent is unenforceable as a result of the failure of at least the named inventor, Fwu-Iuan Hshieh, to cite Hshieh 384 during prosecution of the '634 Patent.

656. I further understand that the application that resulted in the '634 Patent had not yet been filed as of the publication date of Hshieh 384. In particular, Hshieh 384 was published on December 7, 2006, and the application that resulted in the '634 Patent was filed on February 23, 2008. Hshieh 384 is titled, “Structure for Avalanche Improvement of Ultra High Density Trench MOSFET,” and names Fwu-Iuan Hshieh as its sole inventor. I understand Fwu-Iuan Hshieh and Fu-Yuan Hsieh (the named inventor of the '634 Patent) are the same person, despite the different spellings of the inventor’s first and last names.

657. As set forth in Sections X.K and X.L, I have reviewed Hshieh 384 as part of my invalidity opinions for the '634 Patent. Based on this, it is my opinion here that a reasonable

examiner at the USPTO would have wanted to know about it during the prosecution of the '634 Patent.

658. Similar to the '634 Patent, Hshieh 384 discloses the structure for a trenched MOSFET that provides “improve[d] avalanche capability.” Ex. X, Hshieh 384 at Abstract; *id.* at [0011-12]; Ex. C, '634 Patent at 1:6-8 (“This invention relates to a trenched MOSFET with trenched source contact and, in particular, to provide a lateral contact layer in the MOSFET for avalanche improvement.”). Specifically, Hshieh 384 discloses a trenched MOSFET that includes “a trenched gate surrounded by a source region encompassed in a body region above a drain region disposed on a bottom surface of a substrate” and further includes “a source-body contact trench opened with sidewalls substantially extend vertically relative to a top surface into the source and body regions and filled with contact metal plug.” Ex. X, Hshieh 384 at [0013].

659. Hshieh 384 further discloses the claimed invention of the '634 Patent—“sidewalls of said trenches in said base layer are covered by the lateral contact layer.” Ex. C, '634 Patent at cl. 1. Namely, Hshieh 384 states that “the sloped trenches allow the formation of heavily doped P+ doped regions 128 *along both the trench sidewalls and the bottom* through zero degree ion implantation of boron or BF-2.” *Id.* at [0028] (emphasis added). Figure 9G depicts “a boron or BF2 implant with P+ ions 228' is first performed to form the P+ doped region 228 to surround the trenches 224.” *Id.* at [0035]. Covering the sidewalls of the source contact trench with a heavy dopant contributes to the improved avalanche capability of both the '634 Patent and Hshieh 384.

660. Looking at the entire disclosure of Hshieh 384, it is my opinion that Hshieh 384 is not cumulative of any reference cited or relied on during the prosecution of the '634 Patent. During prosecution, the examiner cited a single reference, U.S. Patent No. 6,888,196 to Kobayashi (“Kobayashi 196”). Ex. H, 346 FH at FORCE-MOS0000065-67. I have analyzed both Kobayashi

196 and the patent publication that preceded it, U.S. Patent Publication No. 2004/0021174 (mentioned above as “Kobayashi 174”). It is my opinion that these references do not contain the same invalidating disclosures as Hshieh 384. For instance, the ’634 Patent describes the invention as a “trenched MOSFET with trenched source contact and, in particular, to provide a lateral contact layer in the MOSFET for avalanche improvement.” Ex. C, ’634 Patent at 1:6-8. Neither Kobayashi 197 nor Kobayashi 174 contain disclosures about a MOSFET structure that improves avalanche capability. Hshieh 384, on the other hand, does provide disclosures of a MOSFET structure that improves avalanche capability. *See* Ex. X, Hshieh 384 at [0003] (“[T]his invention relates to a novel and improved cell structure and improved process for fabricating a trenched semiconductor power device with improved avalanche capability.”); *id.* at [0011-12].

661. As explained above, it is my opinion that Hshieh 384 alone anticipates claims 1-9 of the ’634 Patent, and it also renders those claims obvious when combined with other prior art. It is further my opinion that this reference is material to the issue of patentability and should have been disclosed to the USPTO during prosecution. Mr. Hshieh knew or should have known about Hshieh 384 and its relevance to the patent application leading to the ’634 Patent, on which Mr. Hshieh is also a named inventor. Mr. Hshieh knew or should have known about the relevance of Hshieh 384 to patent applications having the same or similar field and technology. *See* Ex. X, Hshieh 384 at [0003] (“This invention relates generally to the cell structure and fabrication process of power semiconductor devices.”); Ex. C, ’634 Patent at 6-8 (“This invention relates to a trenched MOSFET with trenched source contact and, in particular, to provide a lateral contact layer in the MOSFET for avalanche improvement.”).

662. I do not understand why Mr. Hshieh did not disclose Hshieh 384 or other patents and publications that name him as an inventor, especially when those patents and publications

cover the same field and technology as the application leading to the '634 Patent. When I file a patent applications, I make sure to disclose anything that might be relevant, including any prior patents and publications where I am a named inventor.

B. Failure to Disclose U.S. Patent No. 5,763,914 (“Hshieh 914”)

663. I understand that ASUS is asserting that the '409 Patent is unenforceable as a result of the failure of at least the one of the named inventors, Fwu-Iuan Hshieh, to cite U.S. Patent No. 5,763,914 (“Hshieh 914”) during the prosecution of the '409 Patent.

664. I further understand that the application that resulted in the '409 Patent had not yet been filed as of the issuance of Hshieh 914. In particular, Hshieh 914 issued on June 9, 1998, and the application that resulted in the '409 Patent was filed on December 4, 2006. Hshieh 914 is titled, “Cell Topology for Power Transistors with Increased Packing Density” and names Fwu-Iuan Hshieh as one of its inventors, along with Danny Chi Nim. I understand Fwu-Iuan Hshieh is the same inventor as the '409 Patent.

665. As set forth in Section XI.G, I have reviewed Hshieh 914 as part of my invalidity opinions for the '409 Patent. Based on this, it is my opinion here that a reasonable examiner at the USPTO would have wanted to know about it during the prosecution of the '409 Patent.

666. Hshieh 914 discloses trenched semiconductor power devices having various cell layouts, including non-orthogonal parallelogram, regular square, rectangular, and hexagonal shapes. Hshieh 914 at 4:35-38. Hshieh 914 emphasizes the need to “blunt[] or round[]” corners “to prevent the corner vulnerability where punch through weak points may be formed at the sharp corners due to a three-dimension diffusion effect.” Figures 6A and 6B of Hshieh 914 are reproduced below.



Hshieh 914, Figures 6A-B

As shown, the corners of cells in Fig. 6A become blunted or rounded in Fig. 6B.

667. Similar to Hshieh 914, the '409 Patent also discloses blunting or rounding the corners as a part of the alleged invention. The '409 Patent states at 4:53-61, “The process for manufacturing the semiconductor power device as disclosed above thus includes a step of ‘exposure through the mask’ such that the square contact becomes approximately *circular shaped contact and truncated corners become smoother ... It is by nature that truncated corners in layout as that shown in FIG. 2 and becomes rounded as shown in FIG. 3*. Such configuration is formed after exposure because of the photolithography ...” Ex. D, '409 Patent at 4:53-61 (emphasis added)). The rounding or blunting of the sharp corners in Figure 2 is depicted in Figure 3.

668. Looking at the entire disclosure of Hshieh 914, it is my opinion that Hshieh 914 is not cumulative of any other reference relied on by the examiner during the prosecution of the '409 Patent. Although the '409 Patent lists a number of references on its face, the examiner relied only on U.S. Patent No. 6,541,818 to Pfirsch et al. (“Pfirsch 818”), U.S. Patent Publication 2002/0006703 to Pfirsch et al. (“Pfirsch 703”), U.S. Patent No. 6,867,083 to Imam et al. (“Imam 083”), and U.S. Patent No. 6,621,107 to Blanchard et al. (“Blanchard 107”) to invalidate the limitations recited in issued claim 1. I have analyzed Pfirsch 818, Pfirsch 703, Imam 083, Blanchard 107. It is my opinion that these references do not provide the same invalidating disclosures as Hshieh 914. The '409 Patent describes that the “present invention” is a “new and improved semiconductor power device configuration, such as a MOSFET device with a close cell unit configuration with the surrounding gate arranged with truncated corner or rounded corner

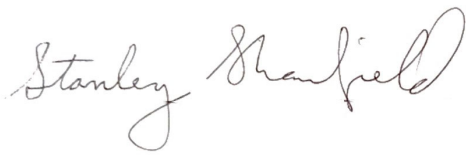
layout. The purpose of the truncated corners or rounded corners of the gate trenches is to make the space between the trenched gate and the metal contact more uniform in the closed cell to enhance the device ruggedness.” Ex. D, ’409 Patent at 1:66-2:7. Pfirsch 818, Pfirsch 703, Imam 083, Blanchard 107 do not contain disclosures about a MOSFET structure that contributes to enhanced device ruggedness. Hshieh 914, on the other hand, does provide such disclosures. Hshieh 914 states that the invention improves “cell topology to achieve higher packing density” by using “non-orthogonal parallelograms with sharper corner blunted or rounded.” Ex. M, Hshieh 914 at 1:10, 3:6-9. Hshieh 914 further states that the improved topology “prevent[s] the corner vulnerability where the punch through weak points may be formed at the sharp corners due to a three-dimension diffusion effect. . . the sharp corners can be either blunted or rounded.” *Id.* at 5:3-8.

669. As explained above, it is my opinion that Hshieh 914 renders claim 1 of the ’409 Patent obvious when combined with other prior art. It is further my opinion that this reference is material to the issue of patentability and should have been disclosed to the USPTO during prosecution. Mr. Hsieh knew or should have known about Hshieh 914 and its relevance to the patent application leading to the ’409 Patent, on which Mr. Hshieh is also a named inventor. Mr. Bo-In Lin, who was the prosecuting attorney for the ’409 Patent and Hshieh 914 knew or should have known about the relevance of the Hshieh 914 to patent applications having the same or similar field and technology. *See* Ex. M, Hshieh 914 at 1:7-9 (“This invention relates generally to the structure and fabrication process of the integrated circuit (IC) power transistors.”); Ex. D, ’409 Patent at 1:7-9 (“This invention relates generally to the cell structure, device configuration and fabrication process of power semiconductor devices.”).

670. I do not understand why Mr. Hshieh did not disclose Hshieh 914 or other patents and publications that name him as an inventor, especially when those patents and publications

cover the same field and technology as application leading to the '409 Patent. When I file patent applications, I make sure to disclose anything that might be relevant, including any prior patents and publications where I am a named inventor. In addition, I do not understand why the prosecuting attorney, Mr. Lin, did not disclose Hshieh 914 to the Patent Office during prosecution of the '409 Patent when he had previously worked on Hshieh 914.

Dated: May 20, 2024

By: 
Stanley R. Shanfield, Ph.D.