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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	06/16/2009	7547584	NAUP0863USA4	6448

27765 7590 05/27/2009
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 150 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ko-Ting Chen, Nan-Tou Hsien, TAIWAN;
Wen-Bin Lu, Hsin-Chu City, TAIWAN;
Chao-Hu Liang, Hsin-Chu City, TAIWAN;



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4	6448
27765 7590 05/15/2009 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER MULPURI, SAVITRI	
			ART UNIT 2812	PAPER NUMBER
			NOTIFICATION DATE 05/15/2009	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Response to Rule 312 Communication	Application No. 11/560,831	Applicant(s) CHEN ET AL.
	Examiner Savitri Mulpuri	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 17 April 2009 under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
 Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1)
 and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

Both replacement sheet of drawing and amendment to specification filed on 4/17/2009 was approved

/Savitri Mulpuri/
 Primary Examiner, Art Unit 2812

Electronic Patent Application Fee Transmittal				
Application Number:		11560831		
Filing Date:		16-Nov-2006		
Title of Invention:		METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		
First Named Inventor/Applicant Name:		Ko-Ting Chen		
Filer:		Winston Hsu		
Attorney Docket Number:		NAUP0863USA4		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt	
EFS ID:	5290713
Application Number:	11560831
International Application Number:	
Confirmation Number:	6448
Title of Invention:	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING
First Named Inventor/Applicant Name:	Ko-Ting Chen
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0863USA4
Receipt Date:	11-MAY-2009
Filing Date:	16-NOV-2006
Time Stamp:	03:36:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1810
RAM confirmation Number	5726
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	NAUP0863-4-E2-1-PTOL85b_PTO.pdf	43247	no	1
			1795f4b56c6266281616bb115aadcf49a30da210		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	31860	no	2
			0c1d4b5a637e7bcc7fa89f3f13096d04a18d3544		
Warnings:					
Information:					
Total Files Size (in bytes):			75107		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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27765 7590 02/10/2009

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Stephanie Lai	(Depositor's name)
/Stephanie Lai/	(Signature)
05/11/2009	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4	6448

TITLE OF INVENTION:

METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	No	\$1510	\$300	\$1810	05/11/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
MULPURI, SAVITRI	2812	438-128000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 Winston Hsu
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

UNITED MICROELECTRONICS CORP.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

No.3, Li-Hsin Road 2, Science-Based Industrial Park, Hsin-Chu City, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-3105.

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /WINSTON HSU/

Date 05/11/2009

Typed or printed name Winston Hsu

Registration No. 41,526

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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**METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED
CIRCUITS DURING SEMICONDUCTOR MANUFACTURING**

Appl. No.	:	11/560,831	Confirmation No.	6448
Applicant	:	Ko-Ting Chen et al.		
Filed	:	November 16, 2006		
TC/A.U.	:	2812		
Examiner	:	MULPURI, SAVITRI		
Docket No.	:	NAUP0863USA4		
Customer No.	:	27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

5 Sir:

Applicants received NOTICE OF ALLOWANCE AND FEE (S) DUE on February 10, 2009. According to **37 CFR 1.312**, Applicants would like to amend some typos, which merely embody **the correction of formal matters** without changing the scope of the claims. Please amend the above –identified applications as follow:

10

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Drawings begin on page 4 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Drawings:

Please replace Figure 8 to correct the reference numerals.

Attachment: Replacement Sheet

1 page(s)

REMARKS/ARGUMENTS

Applicants would like to amend paragraph [Para 11], [Para 45] and [Para 49] of the specification and FIG. 8 by correcting the typos as described above, which merely embody **the correction of formal matters** without changing the scope of the claims.

5

According to **37 CFR 1.312 Amendments after allowance**, “After the Notice of Allowance has been mailed, the application is technically no longer under the jurisdiction of the primary examiner. He or she can, however, make examiner's amendments (see MPEP § 1302.04) and has authority to enter amendments submitted after Notice of

10 Allowance of an application which embody merely the correction of formal matters in the specification or drawing, or formal matters in a claim without changing the scope thereof, or the cancellation of claims from the application, without forwarding to the supervisory patent examiner for approval.” Therefore, Applicants solicit for consideration of the Primary examiner to make examiner’s amendment. If making examiner’s amendments

15 is not feasible, please amend the above-identified application as described above to correct for the formal matters.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

20

Sincerely yours,

_____/Winston Hsu/

Date: _____04/17/2009_____

Winston Hsu, Patent Agent No. 41,526

25 P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

30 Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Amendments to the Specification:

Please replace paragraph [Para 0011] with the following amended paragraph:

In accordance with the claimed invention, a method of reducing charging damage to integrated circuits during semiconductor manufacturing is disclosed. A semiconductor substrate comprising thereon a number of integrated circuit dies is provided. The integrated circuit dies are separated from each other by scribe lanes surrounding each integrated circuit die. Each integrated circuit die comprises thereon at least a first device region, a second device region and a trench isolation dummy region. A first implant mask is formed over the semiconductor wafer, the first implant mask covers the second device region and the trench isolation dummy region, while exposing the semiconductor substrate within the first device region. Dopant species are implanted into the exposed semiconductor substrate within the first device region to form first doping regions therein. The first implant mask is stripped off. A second implant mask is formed over the semiconductor wafer. The second implant mask covers the first device region, while exposing the semiconductor substrate within the first second device region and a plurality of trench dummy features of the trench isolation dummy region. Dopant species are implanted into the exposed semiconductor substrate within the second device region to form second doping regions therein.

20

Please replace paragraph [Para 0045] with the following amended paragraph:

As shown in FIG. 9, using the photoresist layer 330 as an etching hard mask, another plasma etching process is carried out to etch the dielectric layer 310 through the opening 332 and dummy opening 336 to form via opening 342 and dummy via opening 346 in the lower portion of the dielectric layer 310. The photoresist layer 320 is then removed. Likewise, the purpose of the dummy opening-~~346~~ 336 is to increase the in-die shunt path current flow during the plasma etching process.

Please replace paragraph [Para 0049] with the following amended paragraph:

The contact hole 412 communicates with the underlying diffusion region 402 of a semiconductor device such as a transistor. The dummy-~~holes~~ openings-~~414~~ 424 and ~~416~~ 426 expose non-active regions such as shallow trench isolation (STI) region 404.

The dummy holes 414 and 416 increase the in-die shunt path current flow during the plasma etching of the contact hole. It is recommended that the exposed surface area of the opening 422 and dummy openings 424 and 426 is higher than 5% of the die area.

REPLACEMENT SHEET

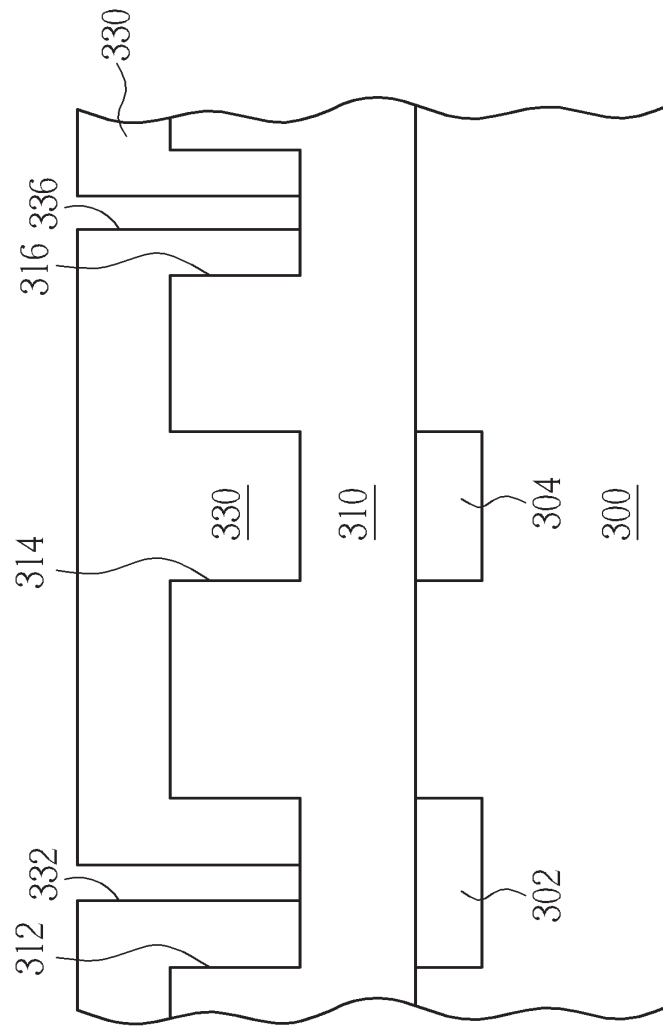


Fig. 8

Electronic Acknowledgement Receipt	
EFS ID:	5170458
Application Number:	11560831
International Application Number:	
Confirmation Number:	6448
Title of Invention:	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING
First Named Inventor/Applicant Name:	Ko-Ting Chen
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0863USA4
Receipt Date:	17-APR-2009
Filing Date:	16-NOV-2006
Time Stamp:	02:30:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	596316.PDF	65235 2a56896d6602d9896139bae9ee84029310a aedc3	no	1

Warnings:

Information:

2	Applicant Arguments/Remarks Made in an Amendment	596317.PDF	69213 2b74a4294f3702e7fc3f47b66e9e127cde208ce	no	2
Warnings:					
Information:					
3	Specification	596313.PDF	54007 6bfe7fe105ebc1f11ae2c22249c82626795bf232	no	2
Warnings:					
Information:					
4	Drawings-only black and white line drawings	596315.PDF	24337 85a6d4464e960972a4416a7505c5bd46925fbb58	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			212792		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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NOTICE OF ALLOWANCE AND FEE(S) DUE

27765 7590 02/10/2009
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
MULPURI, SAVITRI	
ART UNIT	PAPER NUMBER

2812
DATE MAILED: 02/10/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/560,831 11/16/2006 Ko-Ting Chen NAUP0863USA4 6448

TITLE OF INVENTION: METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$300 \$0 \$1810 05/11/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

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If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27765 7590 02/10/2009

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/560,831 11/16/2006 Ko-Ting Chen NAUP0863USA4 6448

TITLE OF INVENTION: METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/11/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
MULPURI, SAVITRI	2812	438-128000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:** Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4	6448
27765	7590	02/10/2009	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			MULPURI, SAVITRI	
			ART UNIT	PAPER NUMBER
			2812	
DATE MAILED: 02/10/2009				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 212 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 212 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<i>Index of Claims</i> 	Application/Control No. 11560831	Applicant(s)/Patent Under Reexamination CHEN ET AL.
	Examiner Savitri Mulpuri	Art Unit 2812

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM			DATE								
Final	Original		01/02/2009								
1	1	=									
2	2	=									
3	3	=									
4	4	=									
5	5	=									
6	6	=									

Issue Classification 	Application/Control No. 11560831	Applicant(s)/Patent Under Reexamination CHEN ET AL.
	Examiner Savitri Mulpuri	Art Unit 2812

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
438		128				H	0	1	L	21 / 44 (2006.0)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
438	462	638	710	453														

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
6	6														

NONE		Total Claims Allowed:	
		1	
(Assistant Examiner)		(Date)	
/Savitri Mulpuri/ Primary Examiner.Art Unit 2812		O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)		1	10
(Date)			

Search Notes 	Application/Control No. 11560831	Applicant(s)/Patent Under Reexamination CHEN ET AL.
	Examiner Savitri Mulpuri	Art Unit 2812

SEARCHED			
Class	Subclass	Date	Examiner
438	113,401,421,453	8/15/2008	SM
438	66,68,627	8/15/2008	SM
438	512,523,584	8/15/2008	SM
438	462, 584,638, 510,533	8/15/2008	SM
438	710,128	8/15/2008	SM

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	8/15/2008	SM

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
438	462,401,638	2/2/2009	SM

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BIB DATA SHEET

CONFIRMATION NO. 6448

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.	
11/560,831	11/16/2006	438	2812	NAUP0863USA4	
RULE					
APPLICANTS Ko-Ting Chen, Nan-Tou Hsien, TAIWAN; Wen-Bin Lu, Hsin-Chu City, TAIWAN; Chao-Hu Liang, Hsin-Chu City, TAIWAN; ** CONTINUING DATA ***** This application is a CIP of 10/908,815 05/27/2005 PAT 7,176,051 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/12/2007					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged /SAVITR MULPURI/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY TAIWAN	SHEETS DRAWINGS 13	TOTAL CLAIMS 6	INDEPENDENT CLAIMS 1
ADDRESS NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116 UNITED STATES					
TITLE METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING					
FILING FEE RECEIVED 1000	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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**REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)**

Application Number	11/560,831	Filing Date	2006-11-16	Docket Number (if applicable)	NAUP0863USA4	Art Unit	2812
First Named Inventor	Ko-Ting Chen			Examiner Name	MULPURI, SAVITRI		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____☐ Other _____☒ Enclosed☒ Amendment/Reply☐ Information Disclosure Statement (IDS)☐ Affidavit(s)/ Declaration(s)☐ Other _____**MISCELLANEOUS**☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)☐ Other _____**FEES****The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 503105**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED**☒ Patent Practitioner Signature☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (09-08)

Approved for use through 10/31/2008. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Signature of Registered U.S. Patent Practitioner			
Signature	/WINSTON HSU/	Date (YYYY-MM-DD)	2009-01-20
Name	Winston Hsu	Registration Number	41526

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED
CIRCUITS DURING SEMICONDUCTOR MANUFACTURING**

Appl. No.	: 11/560,831	Confirmation No.	6448
Applicant	: Ko-Ting Chen et al.		
Filed	: November 16, 2006		
TC/A.U.	: 2812		
Examiner	: MULPURI, SAVITRI		
Docket No.	: NAUP0863USA4		
Customer No.	: 27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

5 Sir:

In response to the Office action of November 18, 2008, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

10 **Remarks/Arguments** begin on page 4 of this paper.

Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 5 1. (Currently amended) A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:
- providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate
- 10 comprises thereon a dielectric layer;
- forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening, wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;
- 15 performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and
- 20 filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature, wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;
- 25 wherein ~~second opening~~ said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.
2. (Previously presented) The method according to claim 1 wherein an exposed surface area of said interconnect and dummy, non-interconnect openings is higher than
- 30 5% of a die area of each said integrated circuit die.
3. (Original) The method according to claim 1 wherein said mask comprises

photoresist.

4. (Previously presented) The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.

5

5. (Previously presented) The method according to claim 1 wherein said interconnect recessed trench is a contact hole.

6. (Original) The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.

10

REMARKS/ARGUMENTS

1. Request for Continued Examination:

5 The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

2. Rejections over claims 1-6 under 35 U.S.C. 102(e):

10 Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by Allman et al. (US 2006/0006538, hereinafter Allman).

 According to MPEP 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed
15 invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)

 Allman teaches a method of forming an extreme low-k circuit structure. Please see FIG. 12A and 12B of Allman, to form such extreme low-k circuit structure, the
20 thermally evaporatable material 105 between interconnect lines 120i or vias 120v is removed. In paragraph 29, Allman explicitly teaches that the openings 110 of FIG. 7, either on the right-hand side or left-hand side, are filled with conductive layer in order to form damascene “interconnect” 120i and via 120v. Allman explicitly states that the damascene metal structures in the openings 110 are “interconnect” lines and vias
25 (paragraph 30 and FIG. 12A). Since the structures 120i and 120v are for interconnect purposes, they will eventually connect with a conductive structure (e.g. structure 130 in FIG. 12A) somewhere.

 Allman teaches nothing about forming dummy, non-interconnect structures
30 concurrently with the interconnect structures for reducing charge damage during a plasma etching. The difference between the claimed invention of the instant application and the method disclosed by Allman can be more clearly seen through

FIGS. 12A-13. Particularly, in FIG. 12A or FIG. 12B, two interconnect lines 120i and 120I are formed in the same level, however, no dummy, non-interconnect features are formed between the two interconnect lines 120i and 120I. Because no dummy, non-interconnect features are concurrently formed with the interconnect lines 120i and 120I, the method taught by Allman is not capable of achieving the purpose of the claimed invention of the instant application, that is, to increase an in-die shunt path current flow during a plasma etching process, thereby reducing charge damage to said integrated circuit dies.

10 The applicant submits that Allman fails to anticipate or render obvious, the following limitations as required in claim 1:

forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening, wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said
15 integrated circuit die;

performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer;

20 filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature, wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate; and

25 said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

30 The applicant respectfully requests that the Examiner give patentable weight to the word “dummy” and the word “non-interconnect” recited in claim 1 because these two words (“dummy” and “non-interconnect”) convey the kernel concept of the claimed invention, which is not taught or anticipated by Allman.

In light of the above, the applicant believes that the distinct features as required in claim 1 distinguish the applicant's invention from the cited references.

Reconsideration of the amended claim 1 is politely requested. As Claims 2-6 are
5 dependent upon claim 1, they should be allowable if claim 1 is allowed.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

10 Sincerely yours,

/Winston Hsu/

Date: 01/20/2009

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

15 Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in
20 D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

Electronic Patent Application Fee Transmittal				
Application Number:		11560831		
Filing Date:		16-Nov-2006		
Title of Invention:		METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		
First Named Inventor/Applicant Name:		Ko-Ting Chen		
Filer:		Winston Hsu		
Attorney Docket Number:		NAUP0863USA4		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description		Fee Code	Quantity	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				810

Electronic Acknowledgement Receipt	
EFS ID:	4637571
Application Number:	11560831
International Application Number:	
Confirmation Number:	6448
Title of Invention:	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING
First Named Inventor/Applicant Name:	Ko-Ting Chen
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0863USA4
Receipt Date:	20-JAN-2009
Filing Date:	16-NOV-2006
Time Stamp:	02:28:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	9324
Deposit Account	503105
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	NAUP0863-4-R1-1-SB30e.pdf	767315	no	3
			6a450fd652cbbfc1f33c63be6d50bca42e21b8f1		
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	NAUP0863USA4_R1_1_AM.pdf	61260	no	1
			407fdcc5f2b28c413ebf248510a230c373524edf		
Warnings:					
Information:					
3	Claims	NAUP0863USA4_R1_1_CLMS.pdf	51785	no	2
			609b710c6a8fe3693ecfb579b8977c114c7af34b		
Warnings:					
Information:					
4	Applicant Arguments/Remarks Made in an Amendment	NAUP0863USA4_R1_1_RM.pdf	91375	no	3
			b4529a01da2bb3aaa5b34ca2785695b518e27368		
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	30365	no	2
			82970ef234966caa14a14c540a86110911dc99a		
Warnings:					
Information:					
Total Files Size (in bytes):			1002100		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/560,831		Filing Date 11/16/2006		☐ To be Mailed	
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APPLICATION AS FILED – PART I						OTHER THAN SMALL ENTITY			
(Column 1)		(Column 2)		SMALL ENTITY ☐		OR		SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A		N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A		N/A		N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A		N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =		OR	X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL		TOTAL				

APPLICATION AS AMENDED – PART II						OTHER THAN SMALL ENTITY					
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	01/20/2009	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X \$ =		OR	X \$2=	0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
☐ Application Size Fee (37 CFR 1.16(s))								OR			
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	

(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR		SMALL ENTITY	
AMENDMENT	Total (37 CFR 1.16(i))	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))								OR			
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								OR			
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/Anita J. Johnson/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4	6448
27765 7590 11/18/2008 NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			EXAMINER MULPURI, SAVITRI	
			ART UNIT 2812	PAPER NUMBER
			NOTIFICATION DATE 11/18/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.		Applicant(s)	
	11/560,831		CHEN ET AL.	
	Examiner		Art Unit	
	Savitri Mulpuri		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 18 September 2008.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1 and 2 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-2 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the applicant's communication filed on 9/18/2008

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 are rejected under 35 U.S.C. 102 (e) as being anticipated by Altman et al (US 2006/0006538).

Altman et al inherently teaches a method for reducing charging damage to integrated circuit during semiconductor manufacturing, comprising: providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer r;

forming a mask over said dielectric layer, and said mask comprising a first opening defining an interconnection pattern and a second opening defining a

dummy pattern, wherein said first and second openings both are formed within each said integrated circuit die (fig5-fig.9 and related description);

performing plasma etching process to etch said dielectric layer through said first and second openings of said mask, thereby forming an interconnect opening and a dummy non-interconnect opening in said dielectric layer (Para 0023); and

filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnection feature and dummy feature, wherein said interconnection electrically connects to an underlying conductive layer, while said dummy, non-interconnect is floating or ground to said semiconductor substrate 'fig. 10, and fig 11 and related description);

With respect to claims 2-6 Altman et al teaches inherently teach an exposed surface area of said first and second openings is higher than 5 % of die area of each said integrated circuit die (fig.6), wherein said mask comprises photoresist "107", wherein interconnection recessed feature is damascene opening "110", wherein interconnect recessed feature is a contact hole "110" and wherein said underlying conductive layer comprises metal wiring (101i)

It is concluded that Altman et al inherently teaches second opening increase an in-die shunt path current flow during said plasma etching process; thereby reducing charge damage to say integrated circuit dies. Because Altman et al also uses plasma etching of dielectric layers "102, 105" by plasma and holes or formed with a die and filling the opening with metal for interconnection connecting the wiring portion "101") and filling the second opening with a metal directly contacting the surface of the

substrate. In other word the process and the final structure is exactly same in the Altman as instantly claimed process , so Altman et al inherently second opening increase an in-die shunt path current flow during said plasma etching process; thereby reducing charge damage to said integrated circuit dies.

Response to Arguments

Applicant's arguments filed on 9/18/2008 have been fully considered but they are not persuasive. Applicant argues that Allman teaches that openings "110" are filled with conductive layer with damascene interconnect and via interconnect. However, Allman teaches two openings "110" and filling the openings with conductive material, wherein, the left side, conductive material "120" is connecting to doped region "101i " and, on the right side, connecting directly to substrate as shown Fig. 11, which is exactly same as instant invention, where conductive region "362,382" connecting to doped region "302" and 366, 386" are connected to substrate as shown in Fig. 10. In other words, the claimed process is same as Allman, only differed by an additional word "dummy, which doe not distinguish the process.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m. to 4.30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber, can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 11/560,831
Art Unit: 2812

Page 6

/Savitri Mulpuri/
Primary Examiner, Art Unit 2812

**METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED
CIRCUITS DURING SEMICONDUCTOR MANUFACTURING**

Appl. No. : 11/560,831 Confirmation No. 6448
Applicant : Ko-Ting Chen et al.
Filed : November 16, 2006
TC/A.U. : 2812
Examiner : MULPURI, SAVITRI
Docket No. : NAUP0863USA4
Customer No. : 27765

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

5 Sir:

In response to the Office action of August 15, 2008, please amend the above-identified application as follows:

Amendments to the Specification are reflected on page 2 of this paper.

10 **Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Amendments to the Specification

Please replace paragraph [0044] with the following context:

As shown in FIG. 8, after the formation of the trench opening 312 and dummy trench
5 openings 314 and 316, a photoresist layer 330 is coated over the substrate 300. The
photoresist layer 330 comprises an opening ~~332~~ 322 that is directly above the trench
opening 312 and a dummy opening ~~336~~ 326 that is directly above the dummy trench
opening 316. Since the conductive layer 304 is situated directly under the dummy trench
opening 314, it is forbidden to provide any dummy opening on the dummy trench
10 opening 314 in order to prevent communication between the dummy trench opening and
the conductive layer 304.

Please replace paragraph [0045] with the following context:

As shown in FIG. 9, using the photoresist layer 330 as an etching hard mask, another
15 plasma etching process is carried out to etch the dielectric layer 310 through the opening
~~332~~ 322 and dummy opening ~~336~~ 326 to form via opening 342 and dummy via opening
346 in the lower portion of the dielectric layer 310. The photoresist layer 320 is then
removed. Likewise, the purpose of the dummy opening 346 is to increase the in-die shunt
path current flow during the plasma etching process.

Electronic Acknowledgement Receipt	
EFS ID:	3947216
Application Number:	11560831
International Application Number:	
Confirmation Number:	6448
Title of Invention:	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING
First Named Inventor/Applicant Name:	Ko-Ting Chen
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0863USA4
Receipt Date:	18-SEP-2008
Filing Date:	16-NOV-2006
Time Stamp:	04:22:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Claims	NAUP0863USA4_A2_1_CLMS. pdf	55893 60799d258bf02b9d6673294f7fa5155e7307d6b1	no	2

Warnings:

Information:

2	Applicant Arguments/Remarks Made in an Amendment	NAUP0863USA4_A2_1_RM.pdf	108518 e9e75774dce55fa83c356d754fb8f1759ac9be9a	no	2
Warnings:					
Information:					
3	Amendment/Req. Reconsideration-After Non-Final Reject	NAUP0863USA4_A2_1_AM.pdf	72144 5c244fcc4dc68d9fe9cd97b6236fc4d4e1a8e347	no	1
Warnings:					
Information:					
4	Specification	NAUP0863USA4_A2_1_SPEC.pdf	72141 5145590d8b204339f145ca2b90689f3806ded56e	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			308696		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Amendments to the Claims:

1. (Currently amended) A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:
- 5 providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer;
- 10 forming a mask over said dielectric layer, said mask comprising ~~a first opening defining an interconnection pattern~~ an interconnect opening and a ~~second opening defining a dummy, non-interconnect pattern opening~~, wherein said ~~first and second openings~~ interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;
- 15 performing a plasma etching process to etch said dielectric layer through said ~~first interconnect opening~~ and ~~second~~ said dummy, non-interconnect openings of said mask, thereby forming an ~~interconnection~~ interconnect recessed feature trench and a ~~recessed-dummy feature~~ dummy recessed trench in said dielectric layer; and
- 20 filling said ~~interconnection recessed feature~~ interconnect recessed trench and said ~~recessed-dummy feature~~ dummy recessed trench with conductive materials to form an ~~interconnection~~ interconnect feature and a dummy, non-interconnect feature, wherein said ~~interconnection feature~~ interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;
- 25 wherein second opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.
2. (Currently amended) The method according to claim 1 wherein an exposed surface area of said ~~first interconnect~~ and ~~second~~ dummy, non-interconnect openings is higher

than 5% of a die area of each said integrated circuit die.

3. (Original) The method according to claim 1 wherein said mask comprises photoresist.

5

4. (Currently amended) The method according to claim 1 wherein said ~~interconnection-recessed feature~~ interconnect recessed trench is a damascene opening.

5. (Currently amended) The method according to claim 1 wherein said ~~interconnection-recessed feature~~ interconnect recessed trench is a contact hole.

10

6. (Original) The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.

REMARKS/ARGUMENTS

Reconsideration of the instant application is politely requested. In order to more particularly point out and distinctly claim that which the applicants regard as their invention, claim 1 has been amended. No new matter is introduced.

- 5 Claim 1 was rejected under 35 U.S.C. 102(e) as being anticipated by Allman et al. (US 2006/0006538, hereinafter Allman). The applicants respectfully submit that Allman et al. fails to anticipate or render obvious, the limitations of “forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening, wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die”, “performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer”, and “filling said interconnect recessed trench and said dummy recessed trench”
10 with conductive materials to form an interconnect feature and a dummy, non-interconnect feature, wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate”, as required by the amended claim 1.

- Allman discloses an extreme low-k circuit structure and method. Allman
20 explicitly teaches that the openings 110 are filled with conductive layer to form damascene **interconnect 120i and via 120v** (paragraph 29). Though FIGS. 7-11 of the cited reference show that the metal in the second opening 110 directly contacts the surface of the substrate, Allman et al. explicitly teaches that the damascene metal in the openings 110 are **interconnect lines and vias**. Accordingly, the interconnect structures
25 120i and the via structures 120v will surely connect with an underlying conductive structure 130 somewhere other than the cross sections through FIGS. 7-11 (paragraph 30 and FIG. 12A). According to MPEP 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed

Appl. No. 11/560,831
Amdt. dated September 18, 2008
Reply to Office action of August 15, 2008

invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)

Allman teaches nothing about “a dummy, non-interconnect opening”, as required in the amended claim 1. Reconsideration of claim 1 is therefore respectfully requested. As
5 Claims 2-6 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

10 Winston Hsu Date: 09/18/2008

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
15 e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/560,831		Filing Date 11/16/2006		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR		RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A				N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				N/A		
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*	X \$ =		OR		X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*	X \$ =				X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)		SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	09/18/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 6	Minus	** 20	= 0	X \$ =		OR	X \$50=	0	
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X \$ =		OR	X \$210=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.											

Legal Instrument Examiner:
/DALE A. HALL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4	6448
27765	7590	08/15/2008		
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION			EXAMINER	
P.O. BOX 506			MULPURI, SAVITRI	
MERRIFIELD, VA 22116			ART UNIT	PAPER NUMBER
			2812	
			NOTIFICATION DATE	DELIVERY MODE
			08/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winstonhsu.uspto@gmail.com
Patent.admin.uspto.Rcv@naipo.com
mis.ap.uspto@naipo.com.tw

Office Action Summary	Application No.		Applicant(s)	
	11/560,831		CHEN ET AL.	
	Examiner		Art Unit	
	Savitri Mulpuri		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 16 November 2006.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-6 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)

Paper No(s)/Mail Date 11/24/2006.

4) ☐ Interview Summary (PTO-413)

Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the applicant's communication filed on 11/16/2006.

Information Disclosure Statement

The information disclosure statement, filed on 11/16/2006, was considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 are rejected under 35 U.S.C. 102 (e) as being anticipated by Altman et al (US 2006/0006538).

Altman et al inherently teaches a method for reducing charging damage to integrated circuit during semiconductor manufacturing, comprising: providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes

surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer r;

forming a mask over said dielectric layer, and said mask comprising a first opening defining an interconnection pattern and a second opening defining a dummy pattern, wherein said first and second openings both are formed within each said integrated circuit die (fig5-fig.9 and related description);

performing plasma etching process to etch said dielectric layer through said first and second openings of said mask, thereby forming an interconnection recessed feature and a recessed dummy feature in said dielectric layer (Para 0023); and

filling said interconnection recessed feature and said recessed dummy feature with conductive materials to form an interconnection feature and dummy feature, wherein said interconnection electrically connects to an underlying conductive layer, while said dummy feature is floating or ground to said semiconductor substrate (fig. 10, and fig 11 and related description);

With respect to claims 2-6 Altman et al teaches inherently teach an exposed surface area of said first and second openings is higher than 5 % of die area of each said integrated circuit die (fig.6), wherein said mask comprises photoresist "107", wherein interconnection recessed feature is damascene opening "110", wherein interconnect recessed feature is a contact hole "110" and wherein said underlying conductive layer comprises metal wiring (101i)

It is concluded that Altman et al inherently teaches second opening increase an in-die shunt path current flow during said plasma etching process; thereby reducing charge damage to said integrated circuit dies. Because Altman et al also uses plasma etching of dielectric layers "102, 105" by plasma and holes or formed with a die and filling the opening with metal for interconnection connecting the wiring portion "101"i) and filling the second opening with a metal directly contacting the surface of the substrate. In other word the process and the final structure is exactly same in the Altman as instantly claimed process , so Altman et al inherently second opening increase an in-die shunt path current flow during said plasma etching process; thereby reducing charge damage to said integrated circuit dies.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Prior art teaches damascene process filling two holes.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m. to 4.30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber, can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Savitri Mulpuri/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 11/560,831		Applicant(s)/Patent Under Reexamination CHEN ET AL.	
	Examiner Savitri Mulpuri		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0006538	01-2006	Allman et al.	257/758
*	B	US-20080174022	07-2008	Chen et al	257/752
*	C	US-6,521,487	02-2003	Chen et al.	438/133
*	D	US-7,176,051	02-2007	Chen et al.	438/68
*	E	US-7,259,091	08-2007	Schuehrer et al.	438/627
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

7039974517 From: Winston Hsu

NOV 24 2006

Approved for use through 09/30/2006. OMB 0651-0031
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Complete if Known

(Use as many sheets as necessary)

1

Attorney Docket Number NAUP0863USA4

Examiner Signature	/Savitri Mulpuri/ (08/08/2008)	Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.87 and 1.88. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PAGE 4/25 * RCVD AT 11/24/2006 3:04:22 AM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/11 * DNIS:2738300 * CSID:7039974517 * DURATION (mm-ss):09-00

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3450	blum.xp.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:12
L2	220063	"438"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:13
L3	118	l1 and l2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:13
L4	0	reduc\$3 adj charg \$3 adj damage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:19
L5	0	reduc\$3 adj charge adj damage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:20
L6	10107	reduc\$3 adj charge	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:20
L7	196	l6 with damag\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:20

L8	2207	winston.att. and hsu.att.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:21
L9	0	I7 and I8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:21
L10	14526	dummy.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:29
L11	5	I1 and I10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:30
L12	42	I6 and I10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:31
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L14	89	luhrs.xa.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:43
L15	10	lulis.xa.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:48

L16	738	mulpuri.xa,xp.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:50
L17	2	I10 and I16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:50
L18	50159	interconnect.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:51
L19	18	I16 and I18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 15:51
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L28	14	"5998282"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 16:51
L29	3596	438/128-132.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 16:55
L30	8	I6 and I29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 16:55
L31	76	dies and I29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/08/07 16:56

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/560,831	11/16/2006	Ko-Ting Chen	NAUP0863USA4

CONFIRMATION NO. 6448

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA22116

Title: METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING

Publication No. US-2007-0093057-A1

Publication Date: 04/26/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
11/560,831	11/16/2006	2812	1000	NAUP0863USA4	13	6	1

CONFIRMATION NO. 6448

27765
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA22116

FILING RECEIPT

Date Mailed: 01/12/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Ko-Ting Chen, Nan-Tou Hsien, TAIWAN;
Wen-Bin Lu, Hsin-Chu City, TAIWAN;
Chao-Hu Liang, Hsin-Chu City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 027765

Domestic Priority data as claimed by applicant

This application is a CIP of 10/908,815 05/27/2005

Foreign Applications

If Required, Foreign Filing License Granted: 01/12/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US11/560,831

Projected Publication Date: 04/26/2007

Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING
SEMICONDUCTOR MANUFACTURING

Preliminary Class

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOV 24 2006

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Customer No.: 27765

Art Unit: N/A

Tel : N/A

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From : Winston Hsu, Registration No. 41,526

Serial No. : 11/560,831

Attorney Docket No.: NAUP0863USA4

Subject: Information Disclosure Statement (IDS)

Total Pages : 25 pages (including cover page)

Winston Hsu NOV. 24 2006

NAUP0863USA4_D1_1

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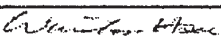
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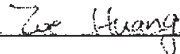
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	Filing Date	11/16/2006
	First Named Inventor	Ko-Ting Chen
	Art Unit	N/A
	Examiner Name	N/A
	Attorney Docket Number	NAUP0863USA4

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FEE TRANSMITTAL For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$)**0.00**

Complete if Known

Application Number 11/560,831
Filing Date 11/16/2006
First Named Inventor Ko-Ting Chen
Examiner Name N/A
Art Unit N/A
Attorney Docket No. NAUP0863USA4

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Small Entity Fee (\$)	Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180
Total Claims	Extra Claims	Fee (\$)
- 20 or HP =	x	=
HP = highest number of total claims paid for, if greater than 20.		
Indep. Claims	Extra Claims	Fee (\$)
- 3 or HP =	x	=
HP = highest number of independent claims paid for, if greater than 3.		

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets Extra Sheets Number of each additional 50 or fraction thereof Fee (\$)

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge):

SUBMITTED BY		Registration No.	Telephone
Signature	<i>Winston Hsu</i>	41,526	3027291562
Name (Print/Type)	Winston Hsu	Date	NOV. 24 2006

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METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING
SEMICONDUCTOR MANUFACTURING
DESCRIPTION

Cross Reference To Related Applications

[Para 1] This is a continuation-in-part of U.S. patent application Ser. No. 10/908,815, filed May 27, 2005.

Background of the Invention

[Para 2] 1. Field of the Invention

[Para 3] The present invention relates generally to the field of semiconductor fabrication and, more particularly, to a method of reducing charging damage to integrated circuits during semiconductor manufacturing. The present invention is particularly suited for ion implant processing in an ion implanter without employing a plasma flood system.

[Para 4] 2. Description of the Prior Art

[Para 5] Ion implanters and ion implant process are commonly used in the manufacture of semiconductor products for implanting dopant species into wafers or semiconductor substrates to change the conductivity of the material in such substrates. Ion implanters generally comprise an ion source for generating a beam of ions, a mass analyzer for

selecting a particular species of ions from the ion beam and means to direct the mass-selected ion beam through a vacuum chamber onto a target substrate supported on a substrate holder. A high-current ion implanter usually encompasses a plasma flood system used to neutralize positive ions.

[Para 6] Influence of ion implant process on wafers has been investigated. It has been revealed that when processing a wafer in plasma ambient or ion implant process environment, charging damage occurs due to surface charge build-up. Such charging damage to integrated circuits can result in costly losses of product.

[Para 7] Typically, damage to thin insulators such as gate oxide sandwiched between a conductive substrate and isolated conductive electrodes on the surface of a wafer (gates) occurs due to current flow through the insulator, driven by a potential difference between the surface electrode and the substrate. During wafer processing, wafer-scale potential differences are caused by global non-uniformities in plasma density and/or electron temperature or, in the case of ion-beam equipment, by spatially imperfect neutralization of the charging caused by the ion beam.

[Para 8] When devices are under the beam in a high-current ion implanter, they are exposed to positive charging from the high-energy ion beam, from “slow” ions (ionized background gases or the plasma used for charge neutralization), and from secondary electrons emitted from the surface of the wafer due to ionic impact. They are also exposed to negative charging from the “electron shower” or the plasma electrons from a plasma flood system used to neutralize positive charging. Therefore, the net positive charging when devices are under the beam is the sum of the positive and negative charging.

[Para 9] Lukaszek in U.S. Pat. No. 5,998,282 describes a method of reducing charging damage to integrated circuits in ion implant and plasma-based integrated circuit process equipment. Charging damage to integrated circuits during ion implantation and plasma processing of integrated circuit die in a semiconductor wafer is reduced by processing scribe lanes during wafer fabrication to facilitate the flow of current to and from the wafer substrate through the scribe lanes during integrated circuit fabrication and reduce current flow through integrated circuit components. Lukaszek also reveals that increasing shunt path current flow within the integrated circuit die is difficult due to circuit layout constraints.

Summary of the Invention

[Para 10] It is the primary object of the present invention to provide an improved method of reducing charging damage to integrated circuits during semiconductor manufacturing, wherein the difficulty of increasing shunt path current flow within the integrated circuit die is overcome.

[Para 11] In accordance with the claimed invention, a method of reducing charging damage to integrated circuits during semiconductor manufacturing is disclosed. A semiconductor substrate comprising thereon a number of integrated circuit dies is provided. The integrated circuit dies are separated from each other by scribe lanes surrounding each integrated circuit die. Each integrated circuit die comprises thereon at least a first device region, a second device region and a trench isolation dummy region. A first implant mask is formed over the semiconductor wafer, the first implant mask covers the second device region and

the trench isolation dummy region, while exposing the semiconductor substrate within the first device region. Dopant species are implanted into the exposed semiconductor substrate within the first device region to form first doping regions therein. The first implant mask is stripped off. A second implant mask is formed over the semiconductor wafer. The second implant mask covers the first device region, while exposing the semiconductor substrate within the first device region and a plurality of trench dummy features of the trench isolation dummy region. Dopant species are implanted into the exposed semiconductor substrate within the second device region to form second doping regions therein.

[Para 12] From one aspect of this invention, the claimed invention method includes the steps of providing a semiconductor substrate comprising thereon a number of integrated circuit dies, the integrated circuit dies being separated from each other by scribe lanes surrounding each integrated circuit die, wherein the semiconductor substrate comprises thereon a dielectric layer; forming a mask over the dielectric layer, the mask comprising a first opening defining an interconnection pattern and a second opening defining a dummy pattern, wherein the first and second openings both are formed within each integrated circuit die; performing a plasma etching process to etch the dielectric layer through the first and second openings of the mask, thereby forming an interconnection recessed feature and a recessed dummy feature in the dielectric layer; and filling the interconnection recessed feature and the recessed dummy feature with conductive materials to form an interconnection feature and a dummy feature, wherein the interconnection feature electrically connects to an underlying conductive layer, while the dummy feature is floating or grounded to the semiconductor substrate.

[Para 13] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[Para 14] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[Para 15] FIG. 1 is a schematic plan view of layout of a photoresist implant mask for implementing lightly doped drain (LDD) regions of high-voltage devices in an integrated circuit die;

[Para 16] FIG. 2 is a schematic plan view of layout of a photoresist implant mask for implementing LDD regions of high-voltage devices in an integrated circuit die according to one preferred embodiment of the present invention;

[Para 17] FIGS. 3–6 are schematic, cross-sectional diagrams showing the method of reducing charging damage to integrated circuits during semiconductor manufacturing in accordance with the preferred embodiment of the present invention;

[Para 18] FIGS. 7–10 are schematic, cross-sectional diagrams showing the method of reducing charging damage to integrated circuits during semiconductor manufacturing in accordance with another preferred embodiment of the present invention;

[Para 19] FIG. 11 illustrates another embodiment of this invention; and

[Para 20] FIGS. 12–13 illustrates still another embodiment of this invention.

Detailed Description

[Para 21] In describing the preferred embodiment of the present invention, reference will be made herein to FIGS. 1–2 of the drawings. Features of the invention are not drawn to scale in the drawings.

[Para 22] As previously described, high-current ion implanters are typically equipped with a plasma flood gun, which is an effective apparatus for suppressing positive charging of wafer. In some cases, however, the ion implanter is not equipped or operated with such plasma flood gun, for example, a medium-current ion implanter that is generally used to provide a dosage of about $1\text{E}11\sim1\text{E}14$ atoms/cm² and ion implant energy of about 10KeV~500KeV. Such medium-current ion implanters are typically employed to form lightly doped source/drain doping regions in the substrate.

[Para 23] FIG. 1 is a schematic plan view of layout of a photoresist implant mask 20 for implementing lightly doped drain (LDD) regions of high-voltage devices in an integrated circuit die. As shown in FIG. 1, the integrated circuit die 10 is surrounded with scribe lanes 12. A number of test key regions (not explicitly shown) are defined within the scribe lanes 12. Within the integrated circuit die 10, device ion wells, gate oxide layer, polysilicon gates, and shallow trench isolation (STI) region have been formed on the substrate such as a silicon substrate.

[Para 24] The photoresist implant mask 20, which masks a large surface area of the integrated circuit die 10, has small-area openings 22 located at the lower left-hand corner

of the integrated circuit die 10. The openings 22 expose the substrate surface of the high-voltage (HV) devices such as HV NMOS devices to be doped with a medium-current ion implanter.

[Para 25] Since the high-voltage devices occupy relatively small part of the die area, the area of the exposed substrate surface through the openings 22 is therefore very small, typically about 0.2%~2% of the die area. It has been found that the small-area openings 22 of the photoresist implant mask 20 during the LDD ion implant process is the root cause of device damage such as polysilicon gate bursting.

[Para 26] In light of the above, there is a need to provide an improved method for making integrated circuits that is able to overcome the above-mentioned LDD doping-related charging damage. Such a method must not, however, introduce any undesired side effects such as decreased device performance or excessively high manufacturing costs.

[Para 27] Please refer to FIG. 2. FIG. 2 is a schematic plan view of layout of a photoresist implant mask 20a for implementing LDD regions of high-voltage devices in an integrated circuit die according to one preferred embodiment of the present invention, wherein like numerals designate like elements, regions or devices.

[Para 28] As shown in FIG. 2, a semiconductor wafer 1 comprises thereon a number of integrated circuit dies 10 and scribe lanes 12 that separate the integrated circuit dies 10. A number of test key regions (not explicitly shown) are defined within the scribing lanes 12. Within the integrated circuit die 10, device ion wells, gate oxide layer, polysilicon gates, and

shallow trench isolation (STI) region have been formed on the substrate such as a silicon substrate.

[Para 29] The photoresist implant mask 20a comprises small-area openings 22 that expose the underlying substrate surface of the high-voltage (HV) devices such as HV NMOS devices to be doped with a medium-current ion implanter. The exposed substrate surface of the HV devices (hereinafter referred to as “exposed device substrate surface”) through the openings 22 is typically source/drain region isolated by STI. The photoresist implant mask 20a further comprises dummy openings 24 distributed within the die 10 on the rest of the die area. The scribe lanes 12 may be partly masked. Alternatively, the scribe lanes may be completely clear and opened (not covered by photoresist implant mask 20a).

[Para 30] The dummy openings 24 are deliberately provided for increasing the exposed substrate surface during the LDD ion implant. According to the preferred embodiment, the dummy openings 24 expose non-device area of the substrate surface (hereinafter referred to as “exposed non-device substrate surface”). For example, these dummy openings 24 may encompass the STI dummy patterns used to reduce loading effect during the fabrication of STI. The sum of the exposed device substrate surface and the exposed non-device substrate surface during the LDD ion implant through the openings 22 and 24 is preferably larger than 5% of the die area.

[Para 31] It is advantageous to use the present invention because the additional dummy openings 24 increase the shunt path current flow through the substrate within the integrated circuit die 10, thereby reducing the likelihood of charging damage to the high-voltage devices during LDD ion implant.

[Para 32] FIGS. 3–6 are schematic, cross-sectional diagrams showing the method of reducing charging damage to integrated circuits during semiconductor manufacturing in accordance with the preferred embodiment of the present invention. As shown in FIG. 3, the semiconductor substrate 100 comprises thereon a high-voltage device region 101, a low-voltage device region 102, a medium-voltage device region 103, and a STI dummy region 104. STI structure 110 is formed in the surface of the semiconductor substrate 100 to electrically insulate electrical components fabricated on the surface of the semiconductor substrate 100. Device ion wells such as P well or N well are not shown.

[Para 33] Within the high-voltage device region 101, high-voltage MOS transistors such as, for example, 5V MOS transistor devices are to be formed therein. A gate electrode 121 of an exemplary high-voltage NMOS transistor is shown in the high-voltage device region 101. The gate electrode 121 is stacked on a thick gate oxide layer 131 and is insulated from the underlying semiconductor substrate 100. Within the low-voltage device region 102, low-voltage MOS transistors such as, for example, 1.8V MOS transistor devices are to be formed therein. A gate electrode 122 of an exemplary low-voltage NMOS transistor is shown in the low-voltage device region 102. The gate electrode 122 is stacked on a gate oxide layer 132 that is thinner than the gate oxide layer 131 and is insulated from the underlying semiconductor substrate 100. Within the medium-voltage device region 103, medium-voltage MOS transistors such as, for example, 3.3V MOS transistor devices are to be formed therein. Gate electrodes 123 of three exemplary low-voltage NMOS transistors are formed within the low-voltage device region 103. Each of the gate electrodes 123 is stacked on a gate oxide layer 133 and is insulated from the underlying semiconductor substrate 100. Within the STI dummy region 104, a plurality of STI dummy features 124 are provided, as

previously mentioned, for the sake of loading effect during the fabrication of STI. The plurality of STI dummy features 124 provide exposed semiconductor substrate surface on which no active circuit or electrical component will be formed.

[Para 34] As shown in FIG. 4, an LDD implant photoresist mask 210 is formed over the semiconductor substrate 100. The LDD implant photoresist mask 210 covers the high-voltage device region 101, the low-voltage device region 102 and the STI dummy region 104, while exposing the medium-voltage device region 103. Since the medium-voltage device region 103 occupies a large part of the die area, a large surface area of the semiconductor substrate 100 within each die is exposed at this stage. The semiconductor substrate 100 is then subjected to an LDD ion implant process to implant dopants such as arsenic into the substrate, thereby forming LDD diffusion regions 143 in the medium-voltage device region 103. According to the preferred embodiment, in order to provide suitable dosages, the LDD ion implant process is carried out in a medium-current ion implanter without employing a plasma flood system or plasma flood gun. The LDD implant photoresist mask 210 is then stripped.

[Para 35] As shown in FIG. 5, another LDD implant photoresist mask 220 is formed over the semiconductor substrate 100. The LDD implant photoresist mask 220 covers the medium-voltage device region 103, the low-voltage device region 102, and exposes the high-voltage device region 101. As previously described, since the high-voltage devices occupy relatively small part of each die area, the exposed surface area of the high-voltage devices during the LDD implant is therefore very small, typically about 0.2%~2% of the die area. In order to increase the exposed surface area of the semiconductor substrate 100 during the

LDD implant and to reduce charging damage, the STI dummy region 104 and the plurality of STI dummy features 124 are also exposed through the LDD implant photoresist mask 220.

[Para 36] By doing this, the total exposed surface area of the semiconductor substrate 100 within each die increases up to larger than 5% of each die area. The semiconductor substrate 100 is then subjected to another LDD ion implant process to implant dopants such as arsenic into the substrate, thereby forming LDD diffusion regions 141 in the high-voltage device region 101. According to the preferred embodiment, in order to provide suitable dosages, this LDD ion implant process is also carried out in a medium-current ion implanter without employing a plasma flood system or plasma flood gun. The LDD implant photoresist mask 220 is then stripped.

[Para 37] As shown in FIG. 6, still another LDD implant photoresist mask 230 is formed over the semiconductor substrate 100. The LDD implant photoresist mask 230 now covers the medium-voltage device region 103, the high-voltage device region 101, and exposes the low-voltage device region 102, and, optionally, the STI dummy region 104. If the exposed surface area of the high-voltage devices during the LDD implant is small, for example, less than 5% of the die area, the STI dummy region 104 and the plurality of STI dummy features 124 are exposed through the LDD implant photoresist mask 230.

[Para 38] Likewise, the semiconductor substrate 100 is subjected to an LDD ion implant process to implant dopants such as arsenic into the substrate, thereby forming LDD diffusion regions 142 in the low-voltage device region 102. According to the preferred embodiment, in order to provide suitable dosages, this LDD ion implant process is also carried out in a medium-current ion implanter without employing a plasma flood system or

plasma flood gun. The LDD implant photoresist mask 230 is then stripped. The subsequent processes include sidewall spacer formation, heavily doped source/drain implant, and salicide processes are omitted. It is noted that the subsequent heavily doped source/drain implant is typically carried out using a high-current ion implanter.

[Para 39] It is to be understood that even the above exemplary embodiments reveal the present invention method of reducing charging damage to integrated circuits during LDD implant process of high-voltage MOS devices, this invention should not be limited thereto. The present invention may be applied in other applications such as for example plasma etching process. Furthermore, it is noted that the sequence of ion implanting the high-voltage device region 101, the low-voltage device region 102 and the medium-voltage device region 103 may be changed. For example, in accordance with another preferred embodiment, the LDD regions of the high-voltage device region 101 are implanted first.

[Para 40] FIGS. 7-10 are schematic cross-sectional diagrams illustrating a method of reducing charging damage to integrated circuits during plasma etching utilized in a dual damascene process in accordance with one exemplary embodiment of this invention.

[Para 41] As shown in FIG. 7, a substrate or a base layer 300 having thereon a conductive layer 302 and a conductive layer 304 is provided. The conductive layers 302 and 304 may be lower level metal wiring or doped diffusion regions. A dielectric layer 310 is deposited on the substrate 300 and covers the conductive layers 302 and 304. A photoresist layer 320 is coated on the dielectric layer 310. The photoresist layer 320 comprises an opening 322 and dummy openings 324 and 326, which are formed within each die area.

[Para 42] Subsequently, using the photoresist layer 320 as an etching hard mask, a plasma etching process is carried out to etch the dielectric layer 310 through the opening 322 and dummy openings 324 and 326 to form trench opening 312 and dummy trench openings 314 and 316 in the upper portion of the dielectric layer 310. The photoresist layer 320 is then removed. The trench opening 312 is directly above the conductive layer 302, while the dummy trench opening 314 is directly above the conductive layer 304.

[Para 43] The purpose of the dummy openings 324 and 326 is to increase the in-die shunt path current flow for the plasma etching process. It is recommended that the exposed surface area of the opening 322 and dummy openings 324 and 326 is higher than 5% of the die area.

[Para 44] As shown in FIG. 8, after the formation of the trench opening 312 and dummy trench openings 314 and 316, a photoresist layer 330 is coated over the substrate 300. The photoresist layer 330 comprises an opening 332 that is directly above the trench opening 312 and a dummy opening 336 that is directly above the dummy trench opening 316. Since the conductive layer 304 is situated directly under the dummy trench opening 314, it is forbidden to provide any dummy opening on the dummy trench opening 314 in order to prevent communication between the dummy trench opening and the conductive layer 304.

[Para 45] As shown in FIG. 9, using the photoresist layer 330 as an etching hard mask, another plasma etching process is carried out to etch the dielectric layer 310 through the opening 332 and dummy opening 336 to form via opening 342 and dummy via opening 346 in the lower portion of the dielectric layer 310. The photoresist layer 320 is then

removed. Likewise, the purpose of the dummy opening 346 is to increase the in-die shunt path current flow during the plasma etching process.

[Para 46] As shown in FIG. 10, using methods known to this industry, copper wiring 362 and copper via 382 are formed within the trench opening 312 and via opening 342, respectively. Concurrently, dummy copper features 364, 366 and 386 are formed within the dummy trench openings 314, 316 and dummy via opening 346, respectively. According to the preferred embodiment, the dummy copper features 364, 366 and 386 are floating. Alternatively, the dummy copper feature 366 and 386 may be grounded to the substrate.

[Para 47] The above exemplary embodiment is known as trench-first dual damascene process. It is understood that the present invention is also suited for other damascene processes such as via-first processes or any plasma etching processes where charge damage due to plasma etching is an issue. For example, this invention is also suited for contact hole etching process.

[Para 48] FIG. 11 illustrates another embodiment of this invention. As shown in FIG. 11, a semiconductor substrate 400 such as a silicon substrate having thereon a diffusion region 402 is provided. A dielectric layer 410 is deposited on the semiconductor substrate 400. A photoresist layer 420 is coated on the dielectric layer 410. The photoresist layer 420 comprises opening 422 and dummy openings 424 and 426. Using the photoresist layer 420 as an etch hard mask, a plasma dry etching process is carried to etch the dielectric layer 410 through the opening 422 and dummy openings 424 and 426, thereby forming contact hole 412 and dummy holes 414 and 416.

[Para 49] The contact hole 412 communicates with the underlying diffusion region 402 of a semiconductor device such as a transistor. The dummy holes 414 and 416 expose non-active regions such as shallow trench isolation (STI) region 404. The dummy holes 414 and 416 increase the in-die shunt path current flow during the plasma etching of the contact hole. It is recommended that the exposed surface area of the opening 422 and dummy openings 424 and 426 is higher than 5% of the die area.

[Para 50] FIGS. 12-13 illustrates another embodiment of this invention. As shown in FIG. 12, a substrate or base layer 500 is provided. A conductive layer 502 is provided in the base layer 500. The conductive layer 502 may be a lower level metal wiring. A dielectric layer 510 is deposited on the base layer 500. A via 512 is formed in the dielectric layer 510. A metal layer 520 such as aluminum layer is formed on the dielectric layer 510. A photoresist layer 530 is coated on the metal layer 520. The photoresist layer 530 is then patterned using conventional lithographic methods to form interconnection pattern 532 and dummy patterns 534 and 536.

[Para 51] As shown in FIG. 13, using the interconnection pattern 532 and dummy patterns 534 and 536 as an etch hard mask, a plasma dry etching process is carried out to etch the metal layer 520 that is not covered with the interconnection pattern 532 and dummy patterns 534 and 536, thereby forming interconnection wiring 522 and dummy features 524 and 526. These dummy features 524 and 526 increase the in-die shunt path current flow during the subsequent plasma enhanced chemical vapor deposition (PECVD) process and help to reduce charge damage.

[Para 52] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

[Claim 1] 1. A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:

providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer;

forming a mask over said dielectric layer, said mask comprising a first opening defining an interconnection pattern and a second opening defining a dummy pattern, wherein said first and second openings both are formed within each said integrated circuit die;

performing a plasma etching process to etch said dielectric layer through said first and second openings of said mask, thereby forming an interconnection recessed feature and a recessed dummy feature in said dielectric layer; and

filling said interconnection recessed feature and said recessed dummy feature with conductive materials to form an interconnection feature and a dummy feature, wherein said interconnection feature electrically connects to an underlying conductive layer, while said dummy feature is floating or grounded to said semiconductor substrate;

wherein second opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

[Claim 2] 2. The method according to claim 1 wherein an exposed surface area of said first and second openings is higher than 5% of a die area of each said integrated circuit die.

[Claim 3] 3. The method according to claim 1 wherein said mask comprises photoresist.

[Claim 4] 4. The method according to claim 1 wherein said interconnection recessed feature is a damascene opening.

[Claim 5] 5. The method according to claim 1 wherein said interconnection recessed feature is a contact hole.

[Claim 6] 6. The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.

ABSTRACT

An integrated circuit die includes thereon a first device region, a second device region and a non-active region. A first implant mask, which covers the second device region and the non-active region, while exposing the first device region, is formed over the semiconductor substrate. Dopant species are implanted into the exposed semiconductor substrate within the first device region to form first doping regions therein. A second implant mask is formed over the semiconductor substrate. The second implant mask covers the first device region, while exposing the second device region and a portion of the non-active region. Dopant species are implanted into the exposed semiconductor substrate within the second device region to form second doping regions therein.

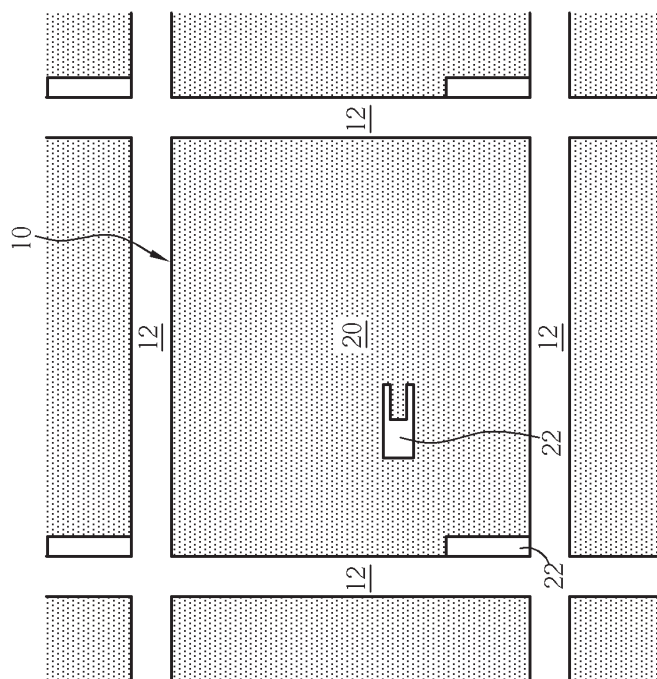


Fig. 1



Fig. 2

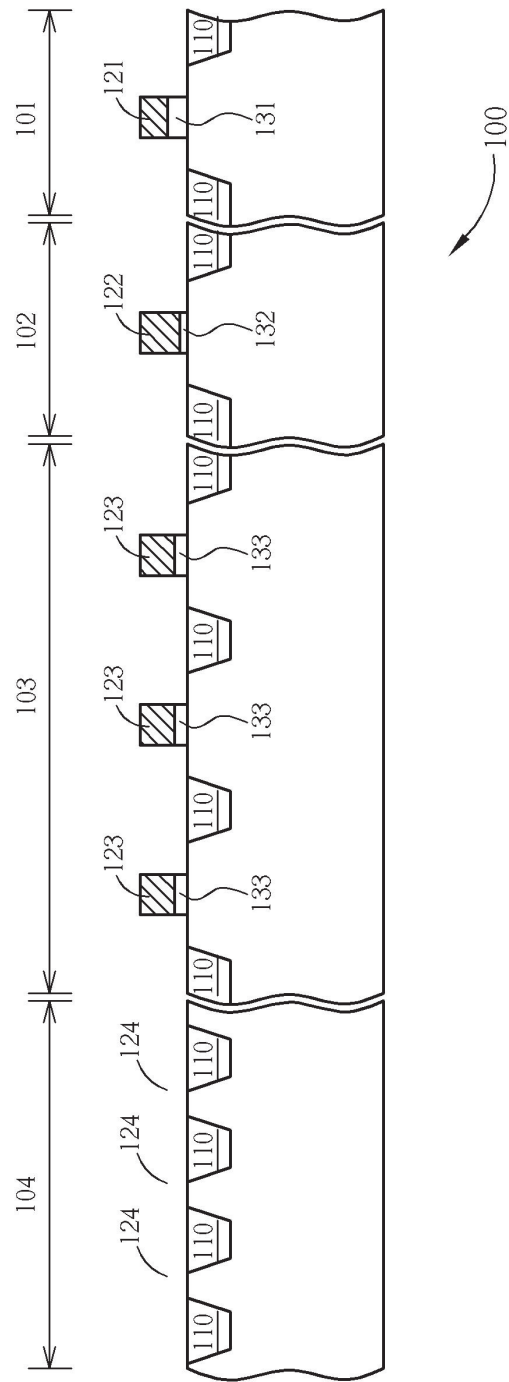


Fig. 3

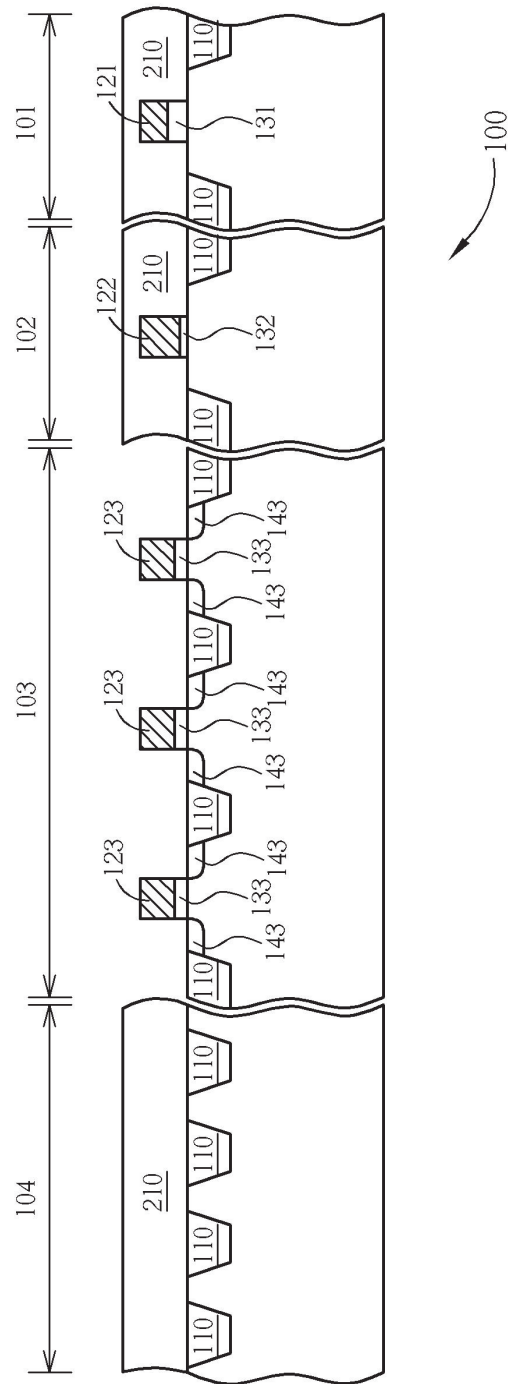


Fig. 4

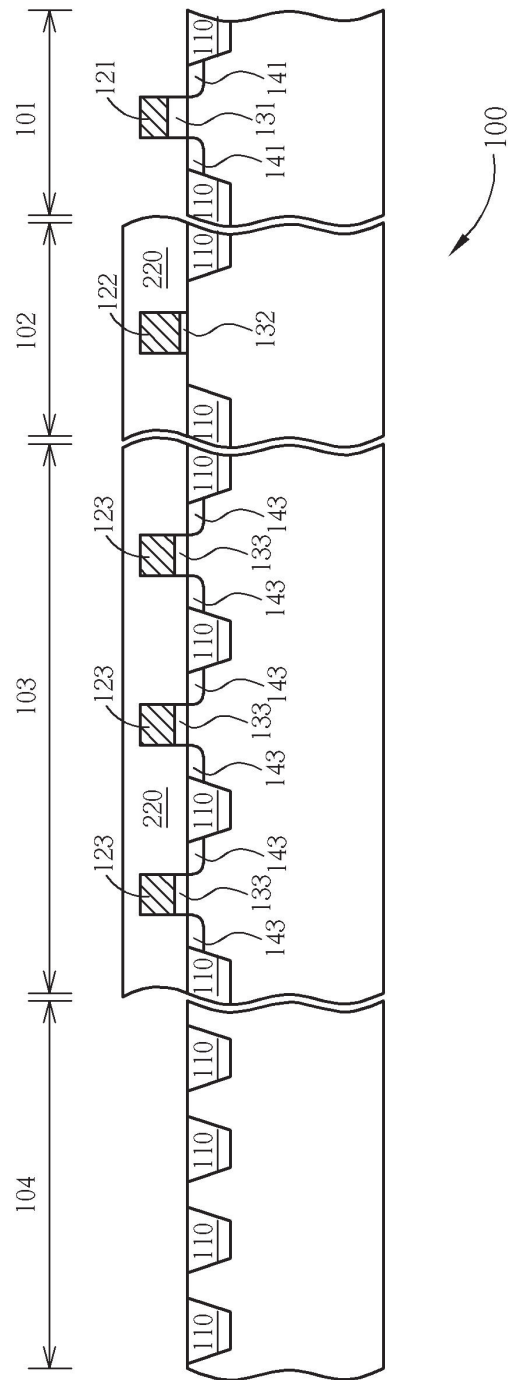


Fig. 5

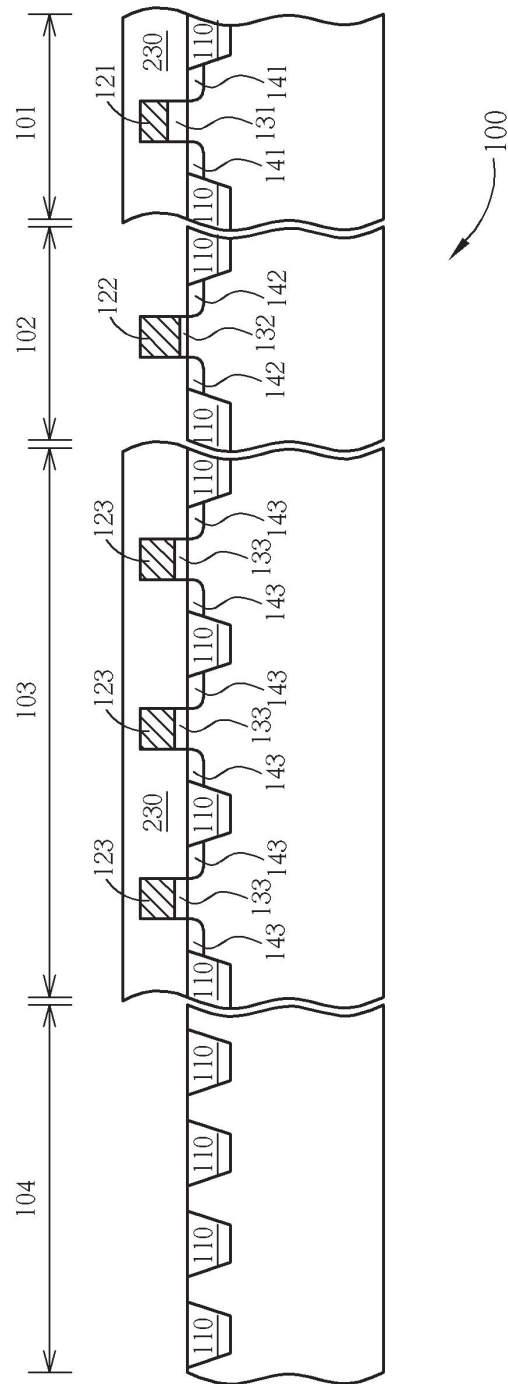


Fig. 6

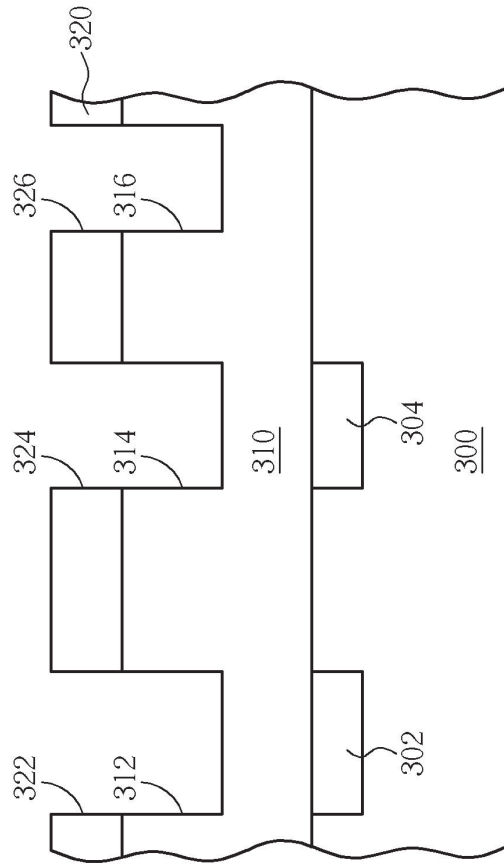
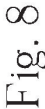


Fig. 7



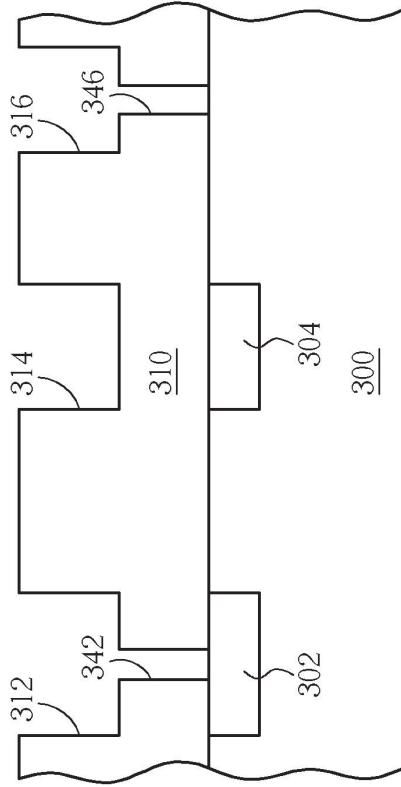


Fig. 9

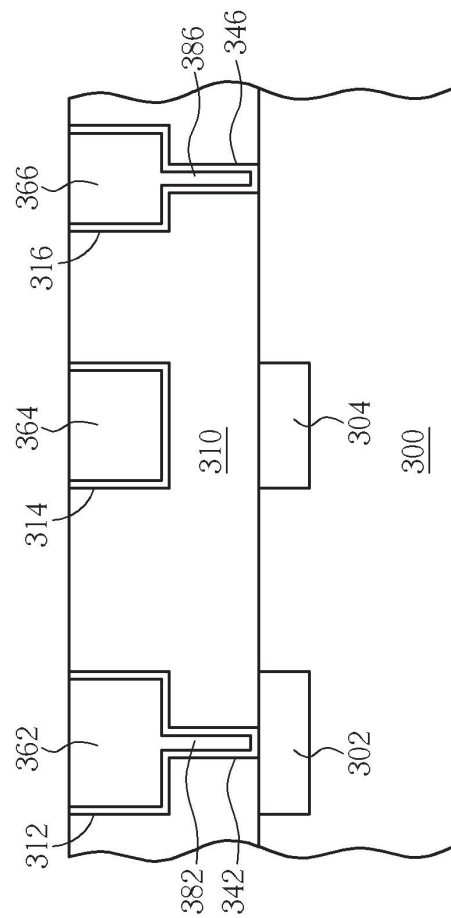


Fig. 10

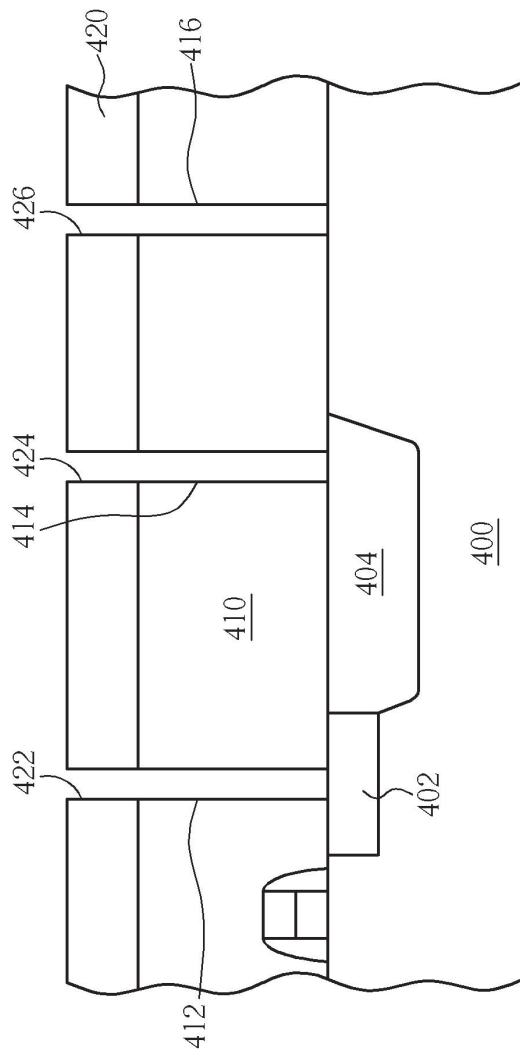


Fig. 11

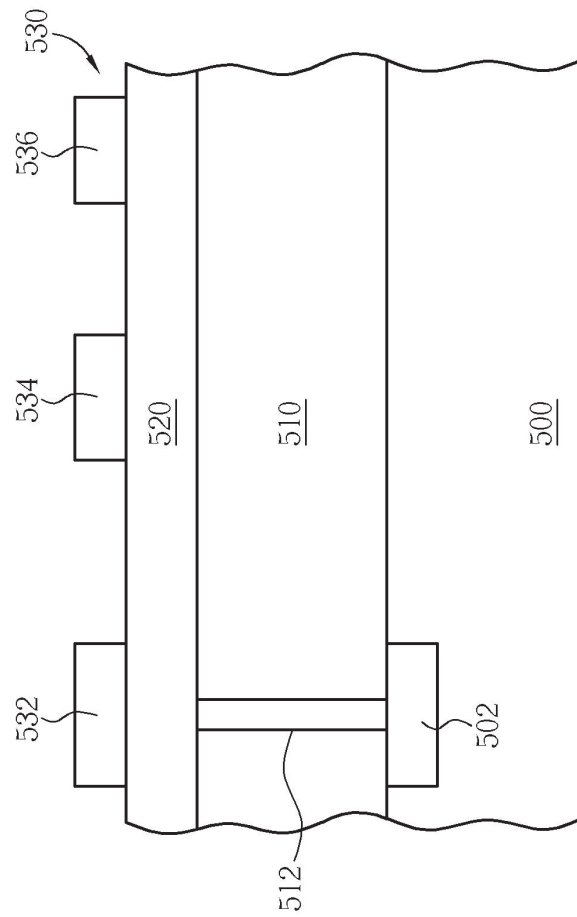


Fig. 12

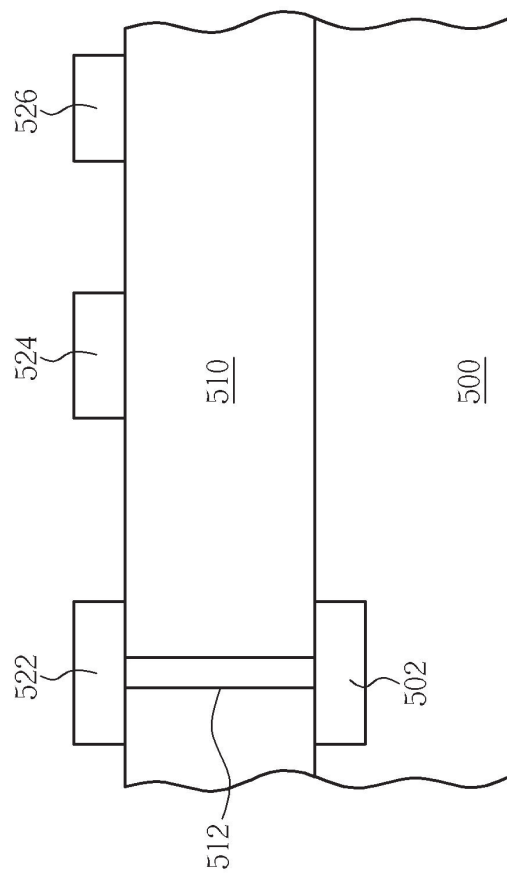


Fig. 13

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING"

+ The specification for the above entitled invention is filed herewith.

_____ The specification for the above entitled invention was filed previously
with application serial number: _____ Filing Date: _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of the invention disclosed in this application in accordance with Title 37, Code of Federal Regulations, Section 1.56 (a). I further acknowledge the duty in any continuation-in-part application to disclose to the Patent and Trademark Office all information known to be material to the patentability of the invention disclosed in this application, as defined in 1.56, which became available to me between the filing date of the prior application and the filing date of this application.

PRIORITY CLAIM

_____ There is no claim of priority

+ Claim of priority is based on the following:

(1) This is a Continuation in part of U.S. application No.:10/908,815, filed 2005/05/27.

**POWER OF ATTORNEY and
CORRESPONDENCE ADDRESS INDICATION**

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint the practitioners associated with the Customer Number: 027765 as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to the address associated with the above-mentioned Customer Number.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	<u>NOV 13 2006</u>	<u>Ko-Ting Chen</u>
	Printed Name:	<u>Ko-Ting Chen</u>
	Post Office Address:	<u>No. 38, Chongchi Rd., Kanding Village, Chongliao</u>
	and Residence	<u>Hsiang, Nan-Tou Hsien, Taiwan, R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>NOV 13 2006</u>	<u>Wen-Bin Lu</u>
	Printed Name:	<u>Wen-Bin Lu</u>
	Post Office Address:	<u>5F-2, No. 88, Dahsue Rd., Hsin-Chu City, Taiwan,</u>
	and Residence	<u>R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>NOV 13 2006</u>	<u>Chao-Hu Liang</u>
	Printed Name:	<u>Chao-Hu Liang</u>
	Post Office Address:	<u>1F, No. 10-2, Lane 179, Wuling Rd., Hsin-Chu City,</u>
	and Residence	<u>Taiwan, R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor , I hereby declare that :

I believe I am the sole (if only one name appears below) , or joint (if more than one name appears) , original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled :

"METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING"

+ The specification for the above entitled invention is filed herewith.

_____ The specification for the above entitled invention was filed previously
with application serial number: _____ Filing Date: _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Please recognize or change the correspondence address for the above-identified application to the address associated with the above-mentioned Customer Number.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued hereon.

(請發明人務必簽署日期)

Date:	<u>NOV 13 2006</u>	<u>Ko-Ting Chen</u>
	Printed Name:	<u>Ko-Ting Chen</u>
	Post Office Address:	<u>No. 38, Chongchi Rd., Kanding Village, Chongliao</u>
	and Residence	<u>Hsiang, Nan-Tou Hsien, Taiwan, R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>NOV 13 2006</u>	<u>Wen-Bin Lu</u>
	Printed Name:	<u>Wen-Bin Lu</u>
	Post Office Address:	<u>5F-2, No. 88, Dahsue Rd., Hsin-Chu City, Taiwan,</u>
	and Residence	<u>R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>
Date:	<u>NOV 13 2006</u>	<u>Chao-Hu Liang</u>
	Printed Name:	<u>Chao-Hu Liang</u>
	Post Office Address:	<u>1F, No. 10-2, Lane 179, Wuling Rd., Hsin-Chu City,</u>
	and Residence	<u>Taiwan, R.O.C.</u>
	Citizen of:	<u>R.O.C.</u>

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0863USA4
		Application Number	
Title of Invention	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Ko-Ting		Chen		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Nan-Tou Hsien		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ			TW		
Mailing Address of Applicant:					
Address 1	No. 38, Chongchi Rd., Kanding Village, Chongliao				
Address 2	Hsiang				
City	Nan-Tou Hsien		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Wen-Bin		Lu		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Hsin-Chu City		Country Of Residenceⁱ	TW	
Citizenship under 37 CFR 1.41(b)ⁱ			TW		
Mailing Address of Applicant:					
Address 1	5F-2, No. 88, Dahsue Rd.				
Address 2					
City	Hsin-Chu City		State/Province		
Postal Code			Countryⁱ	TW	
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Chao-Hu		Liang		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Hsin-Chu City		Country Of Residenceⁱ	TW	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0863USA4	
		Application Number		
Title of Invention	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING			
Citizenship under 37 CFR 1.41(b) i		TW		
Mailing Address of Applicant:				
Address 1	1F, No. 10-2, Lane 179, Wuling Rd.			
Address 2				
City	Hsin-Chu City	State/Province		
Postal Code		Countryi	TW	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	27765		
Email Address	winstonhsu@naipo.com	Add Email	Remove Email

Application Information:

Title of the Invention	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		
Attorney Docket Number	NAUP0863USA4	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	
Publication Information:			
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)			
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not been and will not be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.			

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ US Representative (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0863USA4	
		Application Number		
Title of Invention	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING			
Customer Number	027765			

Domestic Priority Information:

This section allows for the applicant to claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c). Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	10908815	2005-05-27
Additional Domestic Priority Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Remove				
Assignee 1				
If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee Data may be generated within this form by selecting the Add button.				Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NAUP0863USA4
		Application Number	
Title of Invention	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		

Signature	/WINSTON HSU/		Date (YYYY-MM-DD)	2006-11-16	
First Name	WINSTON	Last Name	HSU	Registration Number	41526

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING		
First Named Inventor/Applicant Name:		Ko-Ting Chen		
Filer:		Winston Hsu		
Attorney Docket Number:		NAUP0863USA4		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	300	300
Utility Search Fee	1111	1	500	500
Utility Examination Fee	1311	1	200	200
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	1319575
Application Number:	11560831
International Application Number:	
Confirmation Number:	6448
Title of Invention:	METHOD OF REDUCING CHARGING DAMAGE TO INTEGRATED CIRCUITS DURING SEMICONDUCTOR MANUFACTURING
First Named Inventor/Applicant Name:	Ko-Ting Chen
Customer Number:	27765
Filer:	Winston Hsu
Filer Authorized By:	
Attorney Docket Number:	NAUP0863USA4
Receipt Date:	16-NOV-2006
Filing Date:	
Time Stamp:	23:07:17
Application Type:	Utility

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	940
Deposit Account	503105
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
1	Specification	221770.PDF	57351	no	16
Warnings:					
Information:					
2	Claims	221771.PDF	19582	no	2
Warnings:					
Information:					
3	Abstract	221772.PDF	17000	no	1
Warnings:					
Information:					
4	Drawings	221773.PDF	148178	no	13
Warnings:					
Information:					
5	Oath or Declaration filed	NAUP0863USA4_A1_1_NP003.PDF	139866	no	2
Warnings:					
Information:					
6	Power of Attorney	NAUP0863USA4_A1_1_NP007.PDF	139866	no	2
Warnings:					
Information:					
7	Application Data Sheet	NAUP0863USA4_A1_1_NP075.PDF	1087694	no	5
Warnings:					
Information:					
8	Fee Worksheet (PTO-875)	fee-info.pdf	8406	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1617943		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number	
Substitute for Form PTO-875				11/560,831	
APPLICATION AS FILED – PART I					
(Column 1)		(Column 2)		(Column 3)	
FOR	NUMBER FILED	NUMBER EXTRA			
BASIC FEE (37 CFR 1.16(a), (b), or (c))					
SEARCH FEE (37 CFR 1.16(k), (l), or (m))					
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))					
TOTAL CLAIMS (37 CFR 1.16(i))	6	minus 20 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 =			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.					
APPLICATION AS AMENDED – PART II					
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				
(Column 1)		(Column 2)		(Column 3)	
SMALL ENTITY		SMALL ENTITY		OTHER THAN SMALL ENTITY	
RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
			300		
			500		
			200		
X\$25=		X\$50			
X\$100=		X\$200=			
N/A		N/A			
TOTAL		TOTAL	1000		
SMALL ENTITY		SMALL ENTITY		OTHER THAN SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
X =		X =		X =	
X =		X =		X =	
N/A		N/A		N/A	
TOTAL		TOTAL		TOTAL	
ADD'T FEE		ADD'T FEE		ADD'T FEE	
SMALL ENTITY		SMALL ENTITY		OTHER THAN SMALL ENTITY	
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
X =		X =		X =	
X =		X =		X =	
N/A		N/A		N/A	
TOTAL		TOTAL		TOTAL	
ADD'T FEE		ADD'T FEE		ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.					

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.