

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,

Petitioner

U.S. Patent No. 7,547,584

**DECLARATION OF STANLEY SHANFIELD, PH.D.,
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW**

TABLE OF CONTENTS

I.	INTRODUCTION	5
II.	QUALIFICATIONS	7
III.	RELEVANT LEGAL STANDARDS	11
IV.	FOCUSED ANALYSIS	12
A.	Level of Ordinary Skill in the Art	12
B.	Technology Background.....	13
1.	Dual Damascene Process	14
2.	Plasma Etching	17
3.	Shunt Current	18
C.	Overview of the '584 patent	19
1.	Summary	19
2.	Prosecution History	23
D.	Claim Construction.....	25
V.	DETAILED IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE.....	25
A.	Ground 1: Claims 1 and 3-5 are Obvious over Matsunaga	27
1.	Summary of Matsunaga	27
2.	Claim 1	31
3.	Claim 3	61
4.	Claim 4	62
5.	Claim 5	62
B.	Ground 2: Claim 2 is Obvious over Matsunaga and Jaso	62
1.	Summary of Jaso	62
2.	Obviousness Combination Matsunaga and Jaso	64

3. Claim 2	67
C. Ground 3: Claim 6 is Obvious over the combination of Matsunaga and Appel	
69	
1. Summary of Appel	69
2. Obviousness Combination Matsunaga and Appel	70
3. Claim 6	72
D. Ground 4: Claims 1 and 3-5 are Obvious over the combination of Matsunaga and Wolf	75
1. Summary of Wolf.....	75
2. Obviousness Combination Matsunaga and Wolf.....	76
3. Claim 1	78
4. Claim 3	92
5. Claim 4	92
6. Claim 5	93
E. Ground 5: Claim 2 is Obvious over the combination of Matsunaga, Wolf, and Jaso	93
1. Claim 2	93
F. Ground 6: Claim 6 is Obvious over the combination of Matsunaga, Wolf, and Appel.....	93
1. Claim 6	93
G. Ground 7: Claims 1 and 3-6 are Obvious over the combination of Eriguchi, Quirk, and Wolf.....	94
1. Summary of Eriguchi	94
2. Summary of Quirk.....	96
3. Obviousness Combination Eriguchi and Quirk	97

4.	Obviousness Combination Eriguchi and Wolf	101
5.	Claim 1	102
6.	Claim 3	129
7.	Claim 4	130
8.	Claim 5	130
9.	Claim 6	130
VI.	SECONDARY CONSIDERATIONS	132
VII.	DECLARATION	133

I. INTRODUCTION

1. I, Stanley Shanfield, Ph.D., have been retained by counsel for Taiwan Semiconductor Manufacturing Company Ltd. (TSMC or “Petitioner”) as a technical expert in connection with the proceeding identified above. I submit this Declaration in support of TSMC’s Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 7,547,584 (“the ’584 patent”).

2. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony. I have no personal or financial stake or interest in the outcome of this proceeding.

3. I have been asked to provide my opinions regarding whether the subject matter of Claims 1-6 (the “Challenged Claims”) of the ’584 patent would have been obvious to a person having ordinary skill in the art (“POSITA”) as of the earliest claimed priority date. It is my opinion that the Challenged Claims would have been obvious to a POSITA after reviewing the prior art, as discussed below.

4. In the preparation of this Declaration, I have considered:

- (1) the ’584 patent, Ex.1001;
- (2) the prosecution history of the ’584 patent, Ex.1002;

- (3) Silicon Processing for the VLSI Era Vol. 4 (2001) (“Wolf”), Ex.1004;
- (4) Certified English Translation of JP Publication JPH1174523A to Matsunaga (“Matsunaga”), Ex.1005;
- (5) U.S. Patent Pub. No. 2005/0006707 to Eriguchi et al. (“Eriguchi”), Ex.1007;
- (6) U.S. Patent No. 5,998,282 to Lukaszek, Ex.1008;
- (7) U.S. Patent No. 6,093,631 to Jaso *et al.* (“Jaso”), Ex.1009;
- (8) U.S. Patent No. 7,241,676, Ex.1010;
- (9) U.S. Patent Publication No. 2010/0108652A1, Ex.1011;
- (10) Quirk M. and Serda J., Semiconductor Manufacturing Technology (2001) (“Quirk”), Ex.1012;
- (11) Li S.H. and Miller R.O., Chemical Mechanical Polishing in Silicon Processing (2000), Ex.1013;
- (12) U Van Zant, Microchip Fabrication, 3rd Ed. (1997), Ex.1014;
- (13) Van Zant, Microchip Fabrication, 5th Ed. (2004), Ex.1015;
- (14) U.S. Patent Publication No. 2005/0233564A1, Ex.1016; and
- (15) U.S. Patent No. 5,605,861 (“Appel”), Ex.1017.

5. In forming the opinions expressed below, I have considered: the documents listed above; the relevant legal standards, including the standard for obviousness; and my own knowledge and experience based upon my work in the field of multimedia communications and stereoscopic display as described below, as well as any additional materials cited herein.

6. Unless otherwise noted, all emphasis in any quoted material has been added.

II. QUALIFICATIONS

7. The details of my background and education, and a listing of publications that I have authored, are provided in my *Curriculum Vitae*, a copy of which is submitted as Appendix A. I have four decades of professional experience as a practicing engineer in the field of semiconductor fabrication, process development, and semiconductor device and circuit design. The following is a brief summary of my relevant qualifications and professional experience.

8. I received my B.S. degree cum laude in Physics from the University of California, Irvine in 1977. I earned my Ph.D. in Physics from the Massachusetts Institute of Technology (“MIT”) in 1981, with a dissertation of the physics of high field superconductors. During my doctoral program I received a four-year scholarship from what is now the US Department of Energy (DOE).

9. After earning my Ph.D. in 1981, I worked as a Staff Scientist, then later as a Senior Staff Scientist at Spire Corporation in Bedford, Massachusetts. At Spire Corporation, I developed new methods for low temperature deposition of epitaxial silicon using plasma-assisted chemical vapor deposition (“CVD”). I also

built, operated, and characterized an ion-assisted deposition system, producing thin films for semiconductor devices, including doped dielectric layers.

10. In 1985, I joined Raytheon Corporation, located in Lexington/Andover Massachusetts, as a Section Manager in Semiconductor and IC fabrication. My work focused on developing semiconductor processes for specialized IC designs, including those requiring reactive ion etching (“RIE”) of through-silicon vias (“TSV”), self-aligned source-drain contacts, and experimental methods of forming dual damascene structures. I was later promoted to Research Laboratory Manager and one of the teams I led developed high-performance chemo-mechanical polishing (“CMP”) methodology, including planarization methods that permitted formation of multiple interconnect layers and high frequency structures. My work led to the fabrication of several then state-of-the-art CMOS integrated circuits for both commercial and government customers.

11. In 1996, I was promoted to Director of Semiconductor Operations. In this capacity I managed teams that implemented a 24/7 semiconductor manufacturing facility in Andover, Massachusetts. This facility produced then state-of-the-art CMOS integrated circuit products, including those with dual-damascene interconnect structures. The process sequence used the latest plasma etching technology and equipment, including methods of preventing flashover and charging

damage to CMOS transistors. Our integrated circuits and modules were used in AT&T wireless base stations, T/R modules for Iridium satellite handsets, and other mass-produced commercial products.

12. After 14 years at Raytheon, I became part of the founding team for AXSUN Technology, an electrooptical module manufacturing company located in Bedford/Billerica, Massachusetts, as Vice-President of Operations, starting in 1999. In this capacity I designed and led the implementation and operation of a complete facility for semiconductor processing, producing specialized components for AXSUN products. I also established a fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator material for AXSUN modules. AXSUN was eventually sold to a larger company.

13. In 2003, I joined Draper Laboratory (Draper/MIT), located in Cambridge, Massachusetts, where I am still employed. I have taken roles such as Division Leader of Advanced Hardware Development and I am a Distinguished Member of Technical Staff and a Technical Director. I have been responsible for Draper's in-house circuit fabrication facility, employing advanced interconnect technology for application in space vehicles and other government applications. I also support CMOS foundry implementation of customer Application-Specific Integrated Circuit ("ASIC") products, using specialized processing technology.

14. I have been a member of many professional societies and electrical engineering industry groups over the years, such as the Institute of Electrical and Electronics Engineers (IEEE) and the American Physical Society (APS).

15. I have received several academic awards and honors over the years, including award and honors for the best Draper patent and the most successful Draper development projects.

16. I have also authored or co-authored over 25 technical papers covering various aspects of semiconductor processing, semiconductor devices and semiconductor manufacturing methods.

17. I am named inventor or co-inventor on multiple patents covering semiconductor processes and devices, and semiconductor manufacturing. I have previously testified in patent and trade secret cases, many of which concerned semiconductor device design and processing and semiconductor equipment, before various District Courts, the International Trade Commission and the Patent Trial and Appeal Board. I have been qualified in multiple courts to offer expert opinions on semiconductor issues.

III. RELEVANT LEGAL STANDARDS

18. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '584 patent, I am relying on certain legal principles that counsel has explained to me.

19. I understand that prior art to the '584 patent includes patents and printed publications in the relevant art that predate the priority date of the '584 patent. For purposes of this Declaration, I am applying the earliest claimed priority date of May 27, 2005, as the priority date of the '584 patent.

20. I have been informed by TSMC's counsel that a claimed invention is unpatentable under 35 U.S.C. § 103 if the differences between the claimed invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA. I have also been informed by TSMC's counsel that the obviousness analysis considers factual inquiries, including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

21. I have been further informed by TSMC's counsel that there are several recognized rationales for combining references or modifying a reference to show obviousness. These rationales include: (a) combining prior art limitations according to known methods to yield predictable results; (b) simple substitution of one known

limitation for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art or to combine prior art teachings to arrive at the claimed invention.

22. Also, I have been informed and understand that obviousness does not require physical combination/bodily incorporation, but rather consideration of what the combined teachings would have suggested to a POSITA at the time of the alleged invention.

IV. FOCUSED ANALYSIS

A. Level of Ordinary Skill in the Art

23. I understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the level of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems.

24. A POSITA in the field of the '584 patent, as of the earliest claimed priority date of May 27, 2005, would have been someone with a working knowledge of the semiconductor fabrication art that is pertinent to the '584 patent. A POSITA would have had a master's degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing, including photolithography processing transistors. Additional work experience can substitute for specific educational background, and vice versa.

25. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my own experience and what a POSITA would have understood or known generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the relevant field as of the priority date of the '584 patent.

B. Technology Background

26. The '584 patent relates to semiconductor processing technology that was well-known as of the earliest claimed priority date. This section describes relevant background technology predating the '584 patent supported by appropriate citations below.

1. Dual Damascene Process

27. Dual damascene draws its name from the ancient art of metal inlaying and since the 1990's dual damascene techniques were used for semiconductor manufacturing. Ex.1012, 326. Dual damascene processing was used to form “both the vias and lines for each metal layer by etching holes and trenches in the [interlayer dielectric] ILD, depositing copper in the etched features and using chemical mechanical planarization to remove the excess copper.” Ex.1012, 326.

28. The following three different dual damascene processing sequences were known in the art: i. Trench-First Dual-Damascene ii. Via-First Dual-Damascene iii. Self-Aligned (or Buried-Via) Dual-Damascene. Ex.1004, 676.

i. Trench-First Dual-Damascene

29. In a trench-first sequence, trench patterns are defined in the ILD first. Ex.1004, 677. After forming a photoresist (PR) layer, a trench-pattern-mask is used to expose the photoresist and etching is performed to form openings within an underlying dielectric to an embedded etch-stop layer. Ex.1004, 677. A second photoresist layer is formed and a “via-pattern-mask is used to create openings in [the] resist layer – aligned to the trench that was etched previously.” Ex.1004, 677. “The resist protects the other parts of the wafer surface (including the etched

regions of the trenches) so that the vias can be etched without further etching the dielectric in the trenches.” Ex.1004, 677.

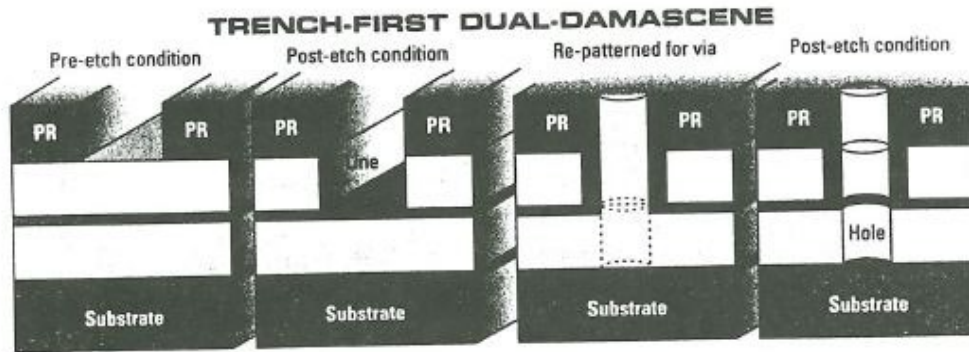


Fig. 15-5 In the trench-first approach, the vias are patterned & etched after trenches are etched.

Ex.1004, Fig. 15-5.

ii. Via-First Dual-Damascene

30. In a via-first sequence, the vias are defined first in the ILD, followed by patterning of the trenches. Ex.1004, 678. Referring to Figure 15-6 (reproduced below), “[t]he sequence ... begins by exposing the via patterns with the first mask” and “[a]fter etching the vias completely through the entire dielectric stack (except not through the barrier layer at the bottom of the dielectric stack) and stripping the resist, a second mask is used to pattern the trenches.” Ex.1004, 678. “The trenches are then created by etching the dielectric down to the embedded etch-stop layer.” Ex.1004, 678.

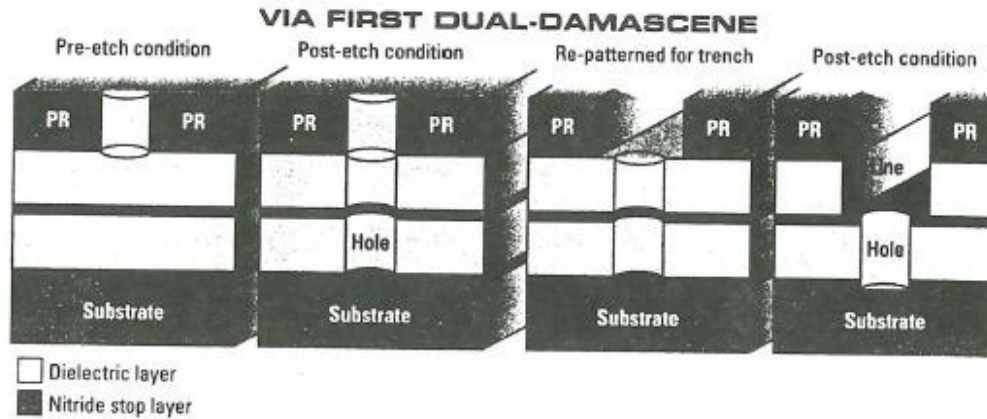


Fig. 15-6 In the via-first approach, the trench is patterned and etched after the via is formed.

Ex. 1004, Fig. 15-6.

iii. Self-Aligned (or Buried-Via) Dual-Damascene

31. In a self-aligned dual damascene sequence, (Fig. 15-7 reproduced below), “the via pattern is created in the embedded etch-stop layer with a lithography-and-etch sequence that is performed before the top dielectric layer of the stack is deposited.” Ex.1004, 679. “After the via pattern is thus etched, the top dielectric layer is deposited.” Ex.1004, 679. “Finally, the trench mask is aligned to the via openings in the embedded nitride layer, and both the trench and via are opened with a single etch step.” Ex.1004, 679.

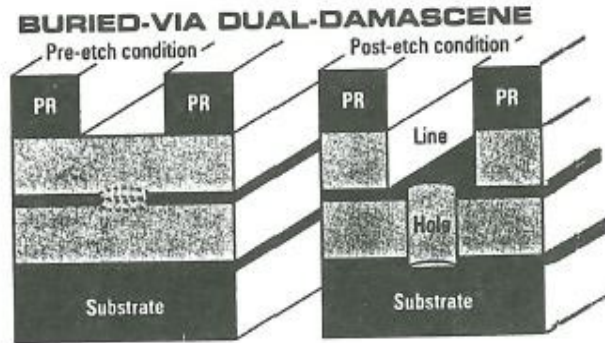


Fig. 15-7 In the self-aligned, or buried-via approach, a hard mask is patterned and etched. The trench and via can be etched in one step.

Ex. 1004, Fig. 15-7.

2. Plasma Etching

32. Plasma dry etching was known in the art as the primary method for etching devices. Ex.1012, 436. “Dry etch exposes the wafer surface to a plasma created in the gaseous state” and “[t]he plasma passes through the openings in the patterned resist and interacts physically or chemically (or both) with the wafer to remove the surface material.” Ex.1012, 436. Plasma etching was known to “improve[] anisotropic sidewalls for features.” Ex.1012, 450.

33. It was also known that plasma etching generates electrons and ions that “can cause plasma-induced damage to sensitive devices on the wafer surface.” Ex.1012, 442. “A major type of damage is nonuniform plasma that creates trapped charges on the gate electrode of a transistor, causing a breakdown of the thin gate

oxide.” Ex.1012, 442. Plasma-induced damages were so well known in the industry that a series of international symposiums were held, with the 5th International Symposium on Plasma Process-Induced Damage taking place in 2000. *See* Ex.1004, 134.

34. Contemporaneous prior art patent literature similarly noted that “[t]he charging of wafer surface in IC process equipment utilizing charged particles for their operation, such as ion implanters and plasma-based process equipment, is well documented.” Ex.1008, 1:13-16. “The build-up of this surface charge on MOS transistor gates and capacitors leads to increasing voltage across the gate oxides until the oxides begin to conduct, shunting the deposited charge to wafer substrate.” Ex.1008, 1:16-19. “[T]he passage of current through gate oxides is accompanied by charge trapping in the oxide, leading to oxide damage and MOS transistor performance degradation or failure.” Ex.1008, 1:27-32.

3. Shunt Current

35. To address this problem, prior art approaches sought to “increase the availability of alternate current shunt paths to facilitate the flow of the charging currents through the substrate, but not through MOS transistors.” Ex.1008, 1:66-2:6. For example, it was known in the art to “facilitate[] current shunting through [] scribe lanes, thus reducing the potential between the surface of the wafer and the

substrate.” Ex.1008, 2:7-15. The prior art also recognized that “[i]t may be desirable in the case of large die to introduce current ‘shunt-paths’ within the die, if the spacing between the scribe lanes is too large to be sufficient for adequate current shunting around the die.” Ex.1008, 3:50-53.

C. Overview of the ’584 patent

1. Summary

36. The ’584 patent generally relates techniques for forming a semiconductor device comprising an integrated circuit. Ex.1001, 7:12-13, Abstract. In particular, the ’584 patent discloses an embodiment for “reducing charging damage to integrated circuits during plasma etching utilized in a dual damascene process.” Ex.1001, 6:23-27. As already noted above in the Technology Background section, a damascene process is one in which etches are made into a layer. A “dual damascene” process is one in which etches are made into a layer, and then additional etches are made over or into the first set of etches. This is illustrated in the ’584 Patent, Figures 7-10 below, with the elements 312, 314, and 316 corresponding to a first set of etches and 332, 336, 342, and 346 corresponding to a second set of etches.

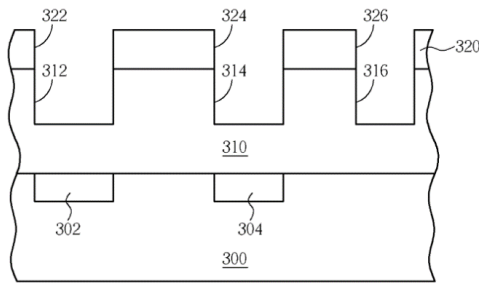


Fig. 7

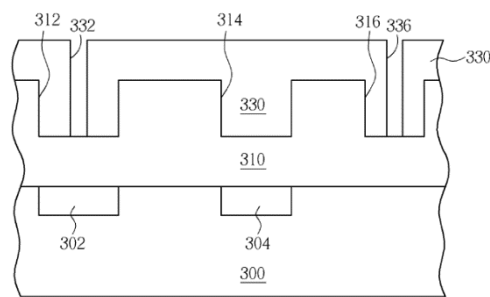


Fig. 8

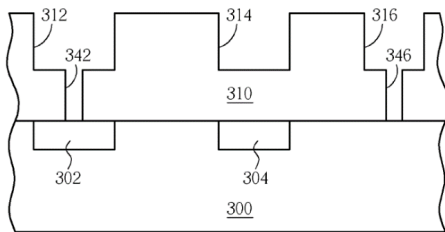


Fig. 9

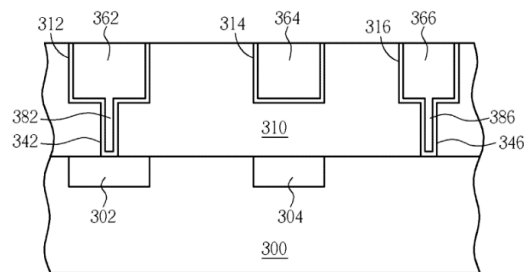


Fig. 10

Ex.1001, Figs. 7-10.

37. In more detail, referring to Figure 7, the method includes providing a substrate 300 that includes conductive layers 302 and 304. Ex.1001, 6:28-31. A dielectric layer is deposited over the substrate 300 and conductive layers 302 and 304. Ex.1001, 6:31-33. A photoresist layer 320 is coated on the dielectric layer 310 and includes an opening 322 and dummy openings 324 and 326. Ex.1001, 6:33-36. Using the photoresist layer 320 as an etching mask, a plasma etching process is carried to etch the dielectric layer 310 to form trench opening 312 and dummy trench openings 314 and 316. Ex.1001, 6:37-45. Referring now to Figure 8, after the photoresist layer 320 is removed, a photoresist layer 330 is coated over the

substrate 300. Ex.1001, 6:51-53. The photoresist layer 330 includes an opening 332 directly above the trench opening 312 and a dummy opening 336 directly above the dummy trench opening 316. Ex.1001, 6:53-56. The dummy opening 336 increases the in-die shunt path current flow during the plasma etching process, which reduces charge damage. Ex.1001, 6:62-7:2. As illustrated in Figure 9, using the photoresist layer 330 as an etching mask, another plasma etching process is performed to etch the dielectric layer 310 to form via opening 342 and dummy via openings 346. Ex.1001, 6:62-67. At Figure 10, copper wiring 362, copper via 382, and dummy copper features 364, 366 and 386 are formed. Ex.1001, 6:67-7:8. The dummy copper features 364, 366 and 386 may be floating or grounded. Ex.1001, 7:8-11.

38. Independent claim 1, which parallels the process of Figures 7-10, is reproduced below:

1. A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:

providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer;

forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening, wherein said interconnect opening and said dummy, non-interconnect

opening both are formed within each said integrated circuit die;

performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and

filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature, wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;

wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

39. I note that the processing illustrated at Figures 7-10 and recited in the claims “is known as trench-first dual damascene process” meaning that wider but shallower trenches are etched before narrower but deeper vias. Ex.1001, 7:12-13; *see also* Ex.1004, 676-679. As detailed in the Technology Background section, since the 1990’s dual damascene techniques were used for semiconductor manufacturing.

40. As I explain in detail below, there is nothing novel about the disclosure or claims of the ’584 patent. Using a dummy, non-interconnect, opening during

plasma etching to provide a shunt path that reduces charge damage to the integrated circuit, as well as the other claimed features, was already well known at the time the '584 patent was filed.

2. Prosecution History

41. The '584 patent was filed as a continuation-in-part of application 10/908,815, filed on May 27, 2005, now Pat. No. 7,176,051. Ex.1001, (63). In Response to an Office Action rejecting claims 1-6, the Applicant amended claims 1, 2, 4, and 5 to recite an interconnect opening and a dummy, non-interconnect opening:

1. (Currently amended) A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:

providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer;

forming a mask over said dielectric layer, said mask comprising ~~a first opening defining an interconnection pattern~~ an interconnect opening and a ~~second opening defining a dummy, non-interconnect pattern opening~~, wherein said ~~first and second openings~~ interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;

performing a plasma etching process to etch said dielectric layer through said ~~first interconnect opening~~ and ~~second~~ said dummy, non-interconnect openings of said mask, thereby forming an ~~interconnection~~ interconnect recessed ~~feature~~ trench and a ~~recessed-dummy feature~~ dummy recessed trench in said dielectric layer; and

filling said ~~interconnection-recessed feature~~ interconnect recessed trench and said ~~recessed-dummy feature~~ dummy recessed trench with conductive materials to form an ~~interconnection~~ interconnect feature and a dummy, non-interconnect feature, wherein said ~~interconnection feature~~ interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;

wherein second opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

Ex.1002, 47-61.

42. The Applicant then argued that the prior art does not teach a dummy non-interconnect opening because the prior art interconnect structures and via structures are all connected to an underlying structure. *See* Ex.1002, 47-54. The Examiner maintained the rejection and the Applicant filed an amendment with a request for continued examination, arguing that the prior art does not teach forming dummy non-interconnect structures concurrently with the interconnect structures

for reducing charge damages during a plasma etching. *See* Ex.1002, 28-46. The Examiner then subsequently issued a Notice of Allowance, allowing claims 1-6. *See* Ex.1002, 17-20. The '584 patent issued on June 16, 2009.

D. Claim Construction

43. It is my understanding that in order to properly evaluate the '584 patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called *Phillips* standard, under which claim terms are given their ordinary and customary meaning as would have been understood by a POSITA in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term.

44. I have applied the so-called *Phillips* standard in the unpatentability analysis. I have reviewed the '584 patent, as well as its prosecution history. It is my opinion that for purposes of applying the prior art presented herein to evaluate the patentability of the claims, the claim terms do not require express construction.

V. DETAILED IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

45. I have been asked to provide my opinion as to whether the Challenged Claims of the '584 patent would have been obvious in view of the prior art. The

discussion below provides a detailed analysis of how the prior art references I reviewed teach the limitations of the Challenged Claims of the '584 patent.

46. As part of my analysis, I have considered the scope and content of the prior art and any potential differences between the claimed subject matter and the prior art. I conducted my analysis as of the earliest claimed priority date of the '584 patent, May 27, 2005. I have also considered the level of ordinary skill in the pertinent art as of that date.

47. I describe in detail below the scope and content of the prior art, as well as any differences between the claimed subject matter and the prior art, on a limitation-by-limitation basis for the Challenged Claims of the '584 patent. This analysis supports my opinion that the differences between the Challenged Claims and the prior art discussed herein are such that the subject matter as a whole would have been obvious at the time of the filing of the '584 patent to a person having ordinary skill in the art to which the subject matter pertains. I note that my analysis and proposed prior art combinations rely on the teachings of the references—and not on physical incorporation of the elements.

48. Additionally, as part of my analysis, I have reviewed and appropriately cite to other prior art references as demonstrating knowledge in the art.

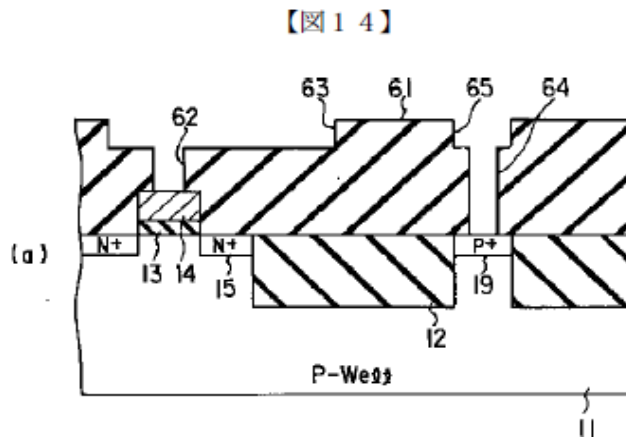
49. Unless otherwise noted, all emphasis in any quoted material has been added.

A. Ground 1: Claims 1 and 3-5 are Obvious over Matsunaga

50. Matsunaga renders obvious Claims 1 and 3-5 as discussed below.

1. Summary of Matsunaga

51. Like the '584 patent, JP Publication No. 11-74523A to Matsunaga (Ex. 1005, Ex.1006, "Matsunaga") generally discloses a method for forming integrated circuits ("ICs"), e.g., microprocessor circuits, comprising MOS transistors. Ex.1005, [0028]-[0029], Figs. 1, 12, 14-15. Also, like the '584 patent, Matsunaga's method utilizes a dual damascene process that provides an alternative path, i.e., via dummy connecting hole 64, for current discharge during an RIE plasma etching to prevent charging damage to the device. Ex.1001, 6:23-27, 6:62-7:18; Ex.1005, [0009], [0019], [0055]-[0056]. Matsunaga's Figure 14 (a) is reproduced below, illustrating the dummy connecting hole 64 that is formed in the dual damascene process:



Ex.1005, Fig. 14 (a).

52. In more detail, with respect to the above figure, Matsunaga discloses that connecting hole 62 and dummy connecting hole 64 are formed simultaneously in the RIE plasma process:

FIG. 14 (A) is that which depicts a state wherein an interlayer insulating film 61 is formed over a substrate whereon MOS transistors, or the like, are formed, and a **connecting hole 62 and interconnection groove 63** for forming an interconnection, in the so-called dual damascene structure, to the interlayer insulating film 61 are formed through an RIE process, but **in this case dummy connecting holes 64 and dummy interconnection grooves 65 are also formed at the same time through the RIE process.**

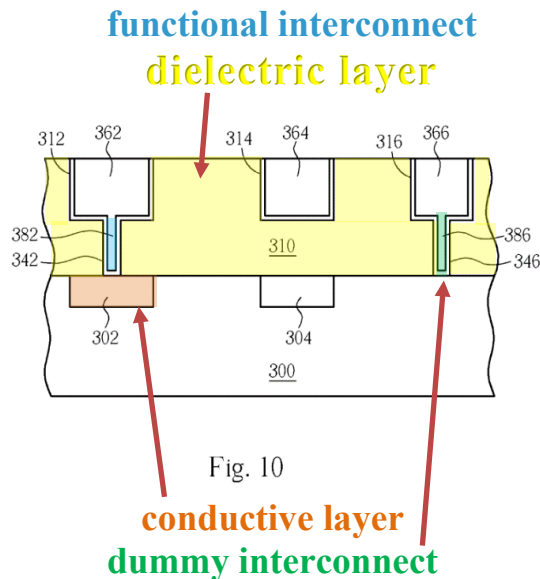
Because conventionally electric charges accumulate only on the gate 14 when the surface of the gate 14 is exposed

through an RIE process, there is a problem in that a large potential difference is produced between the gate 14 and the substrate (the P well 11) so that a strong electric field stress acts on the gate insulating film 13. In the present embodiment, the dummy connecting holes 64 and the dummy interconnection grooves 65 are also **formed simultaneously** in the RIE process, and thus not only are electric charges supplied to the gate, but also to the P+ dopant diffusion layer 19 that is formed in the substrate, which can reduce the potential difference between the electropotential of the gate and the electropotential of the substrate. Consequently, the electric field that acts on the gate insulating film 13 is weakened, making it possible to prevent charging damage.

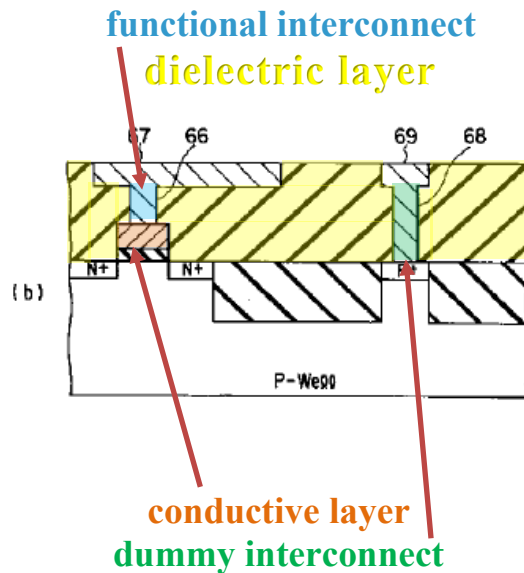
Ex.1005, [0055]-[0056]; *see also* Ex.1005, [0019] (“...the dummy interconnections will ultimately be formed...simultaneously in a plasma process, such as RIE, or the like, when processing the connecting holes and the interconnection grooves.”); Ex.1005, [0029]. As a result of supplying electric charges to the P+ dopant diffusion layer 19 during the RIE plasma process, “the electric field that acts on the gate insulating film 13 is weakened, making it possible to prevent charging damage.” Ex.1005, [0056]; *see also* Ex.1005, [0019] (“... prevent charging damage in the plasma processes, such as RIE, or the like, when processing the connecting holes or interconnection grooves, making it possible to prevent damage to the gate insulating films.”).

53. Matsunaga's finally formed semiconductor device has the same basic arrangement as the '584 patent's semiconductor device, namely: **(1)** a semiconductor substrate (Ex.1001, 6:28-30; Ex.1005, [0029]); **(2)** a dielectric layer (Ex.1001, 6:31-33; Ex.1005, [0055]); **(3)** a functional interconnect electrically connected to a conductive layer (Ex.1001, 7:3-11; Ex.1005, [0057]); and **(4)** a dummy interconnect, which is not used in circuit operation, that is grounded to the substrate (Ex.1001, 7:3-11; Ex.1005, [0029], [0057])

54. These elements are shown in a side-by-side comparison of the '584 patent's Figure 10 and Matsunaga's Figure 14 (b):

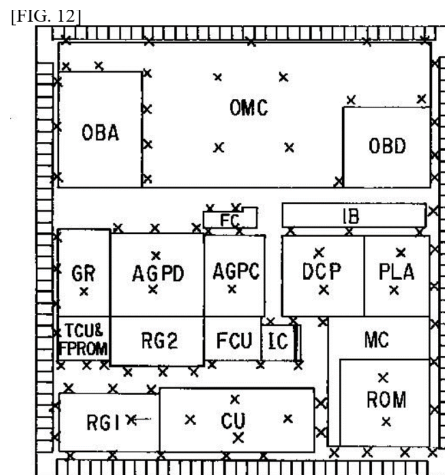


Ex.1001, Fig. 10 (annotated).



Ex.1005, Fig. 14 (b) (annotated).

55. Additionally, like the '584 patent, Matsunaga's method may be used to form an integrated circuit die, e.g., a microprocessor die illustrated below at Figure 12. Ex.1005, [0053], Fig. 12.



Ex.1005, FIG. 12.

56. Thus, Matsunaga's method, which utilizes a dual damascene process like the '584 patent, forms a semiconductor device that is substantially similar to the device of the '584 patent.

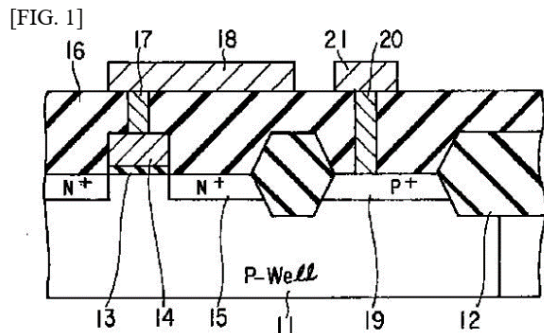
2. Claim 1

- a. [1.0] *A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:*

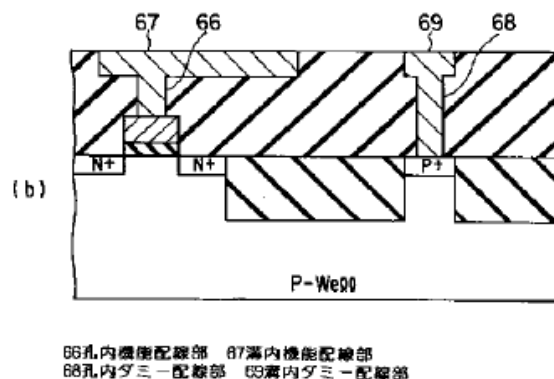
57. To the extent limiting, Matsunaga renders obvious the preamble.

58. First, Matsunaga teaches a “method for reducing charging damage...during semiconductor manufacturing.” In more detail, Matsunaga discloses “a semiconductor device, and manufacturing method thereof, enabling an interconnection structure that is able to prevent charging damage by a plasma process.” Ex.1005, [0009]. Matsunaga’s method provides “the ability to prevent charging damage in the plasma processes... making it possible to prevent damage to the gate insulating films” of a transistor. Ex.1005, [0019].

59. Second, Matsunaga discloses manufacturing “integrated circuits.” For example, Matsunaga’s method (which reduces or prevents charging damage) is used to manufacture a semiconductor device that includes “MOS transistors.” Ex.1005, [0055]. Matsunaga provides various figures illustrating exemplary MOS transistors, of which Figures 1 and 14 are reproduced below.

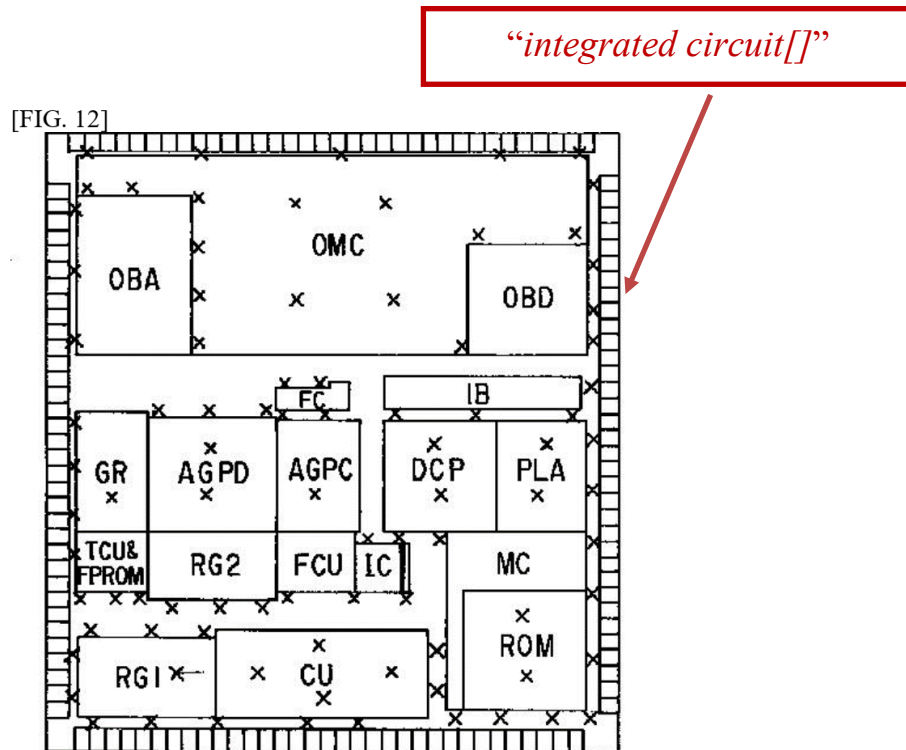


Ex.1005, FIG. 1.



Ex.1005, FIGS. 14 (b).

60. Additionally, Matsunaga in the context of Figure 12 discloses “a microprocessor circuit” that includes MOS transistors with the “X’ mark[ig] dummy interconnections.” Ex.1005, [0053].



Ex.1005, FIG. 12 (annotated).

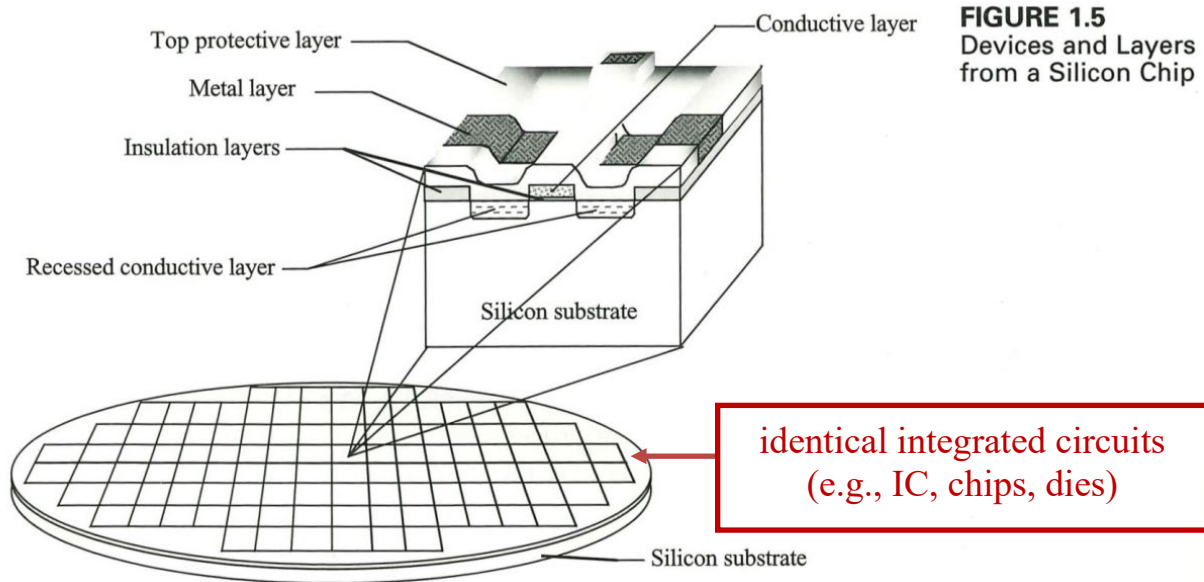
61. A POSITA would have understood that the OMC, OBD, ROM, etc., illustrated at Figure 12 include one or more MOS transistors that Matsunaga discloses in the context of its other figures. In note that the '584 patent's exemplary integrated circuit similarly includes a “MOS transistor.” Ex.1001, 4:52-5:11; *see also* Ex.1001, 6:11-15 (“[T]he above exemplary embodiments reveal the present

invention method of reducing charging damage to integrated circuits during LDD implant process of high-voltage MOS devices.”).

62. Furthermore, it was conventional for microprocessor circuits as disclosed by Matsunaga to be formed on a semiconductor substrate (e.g., silicon wafer) with other identical circuits to achieve scaling and to obtain related benefits, including cost reductions:

The chip is also referred to as a die (singular and **plural for chips or ICs**), while the silicon wafer is often called the substrate. The wafer diameter has evolved over the years from an initial diameter of less than 1”⁸ to the present common diameter of 8” (200 mm), which is undergoing a change to 12”, or 300 mm (see Figure 1.4). The cost of fabricating ICs drops dramatically if there are more chips on a wafer due to benefits from the economies of scale (more chips are produced from the same effort).

Ex.1012, 6; *see also* Ex.1012, 6 (“Tens or hundreds of identical chips are fabricated simultaneously on a silicon wafer.”), 8 (“The fabrication of microchips from wafers is the second stage, referred to as wafer fabrication....The completed wafers have a full complement of **integrated circuits**.”).



Ex.1012, FIG. 1.5 (annotated).

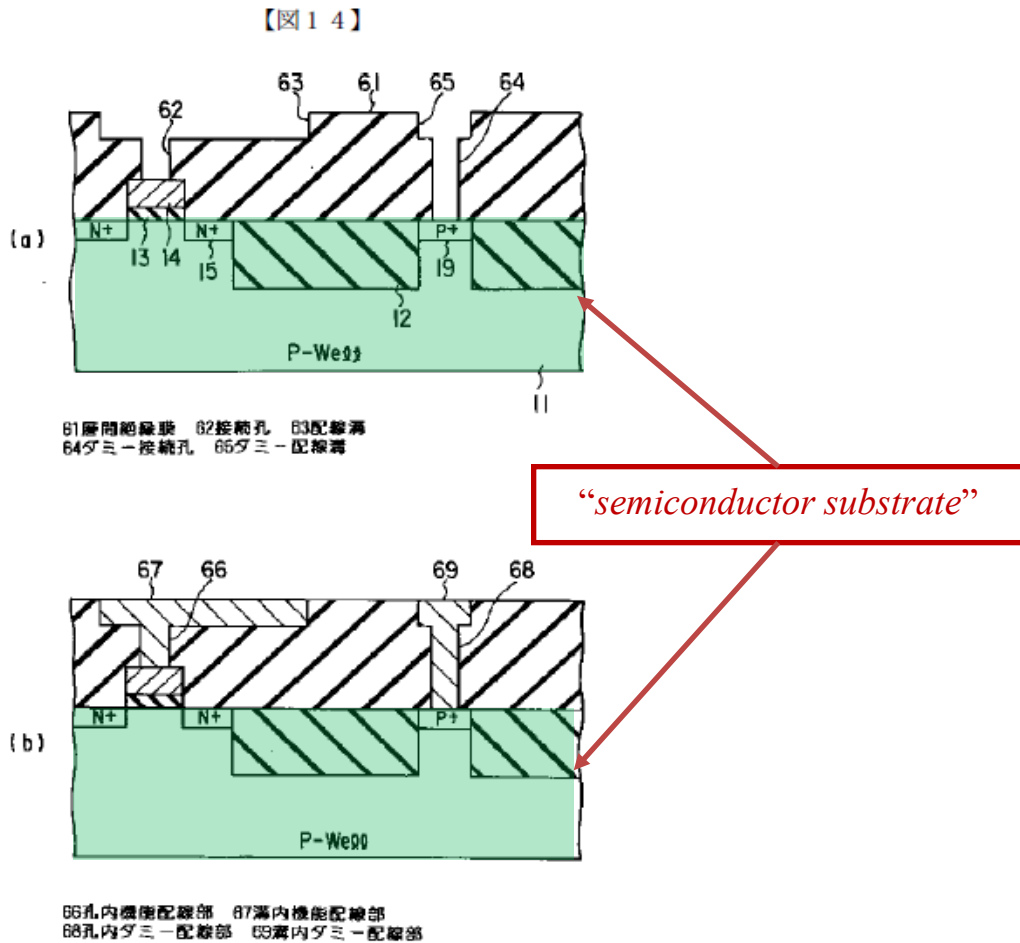
63. Consistent with conventional well-known techniques, it would have been obvious to a POSITA that Matsunaga's microprocessor circuit is formed on a semiconductor substrate (e.g., a silicon wafer) that includes a plurality of other identical microprocessor circuits, in line with conventional manufacturing processing. Ex.1012, 6, Figure 1.5. A plurality of Matsunaga's microprocessor circuits on the same semiconductor substrate correspond to "*integrated circuits*" as claimed.

64. Thus, Matsunaga discloses a method of preventing or reducing charging damage to microprocessor circuits during semiconductor manufacturing, which renders obvious “[a]method for reducing charging damage to integrated circuits during semiconductor manufacturing,” as recited in the preamble.

b. [1.1.1] *providing a semiconductor substrate comprising thereon a number of integrated circuit dies,*

65. Matsunaga renders obvious this limitation

66. First, Matsunaga discloses “providing a semiconductor substrate” by teaching that its device is “formed on a primary surface side of a **semiconductor substrate**” and that the device illustrated at Figure 1 “is formed in a **silicon substrate**.” Ex.1005, [0028]-[0029], Claim 1 (“...semiconductor substrate...”). A POSITA would have understood that Matsunaga’s “silicon substrate” is a “semiconductor substrate.” Ex.1012, 4. In Matsunaga’s Figure 14 (reproduced below), “structural elements that are substantially identical or corresponding to those in the first embodiment, depicted in FIG. 1, are assigned identical numbers, and detailed explanations thereof will be omitted.” Ex.1005, [0054].



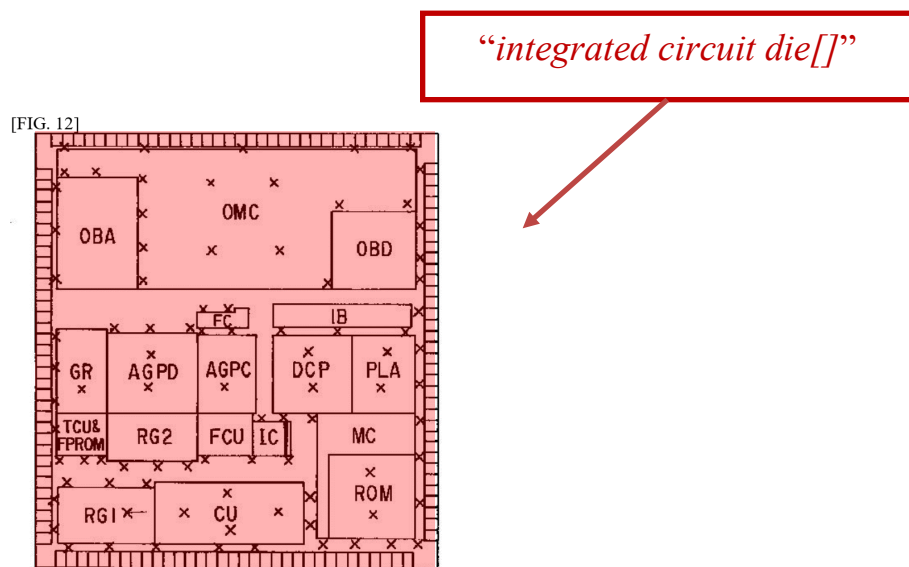
Ex.1005, FIGS. 14 (a) (b) (annotated).

67. Accordingly, the device illustrated at Figures 14(a), (b), which has a silicon substrate, is a “semiconductor substrate” as claimed.

68. The semiconductor substrate in the '584 patent is also silicon. Ex.1001, 7:19-22 (“...semiconductor substrate 400 such as a silicon substrate...”).

69. **Second**, consistent with the analysis at [1.0], it would have been obvious for Matsunaga’s semiconductor substrate to have “thereon a number of

integrated circuit dies.” A POSITA would have understood that the microprocessor circuit (“*integrated circuit*”) illustrated at Figure 12, reproduced below, corresponds to a “chip” or “die” with input/output connections on the periphery. Ex.1005, [0053]; Ex.1012, 6 (“**The chip is also referred to as a die.**”), 8 (“The fabrication of **microchips...integrated circuits.**”):



Ex.1005, FIG. 12 (annotated).

70. Furthermore, consistent with the analysis at [1.0], it would have been obvious to a POSITA for a plurality of Matsunaga’s microprocessor circuit (which are chips or dies) to be manufactured on a silicon wafer in accordance with well-known techniques, in which case it would be obvious for the wafer to contain multiples of such dies.

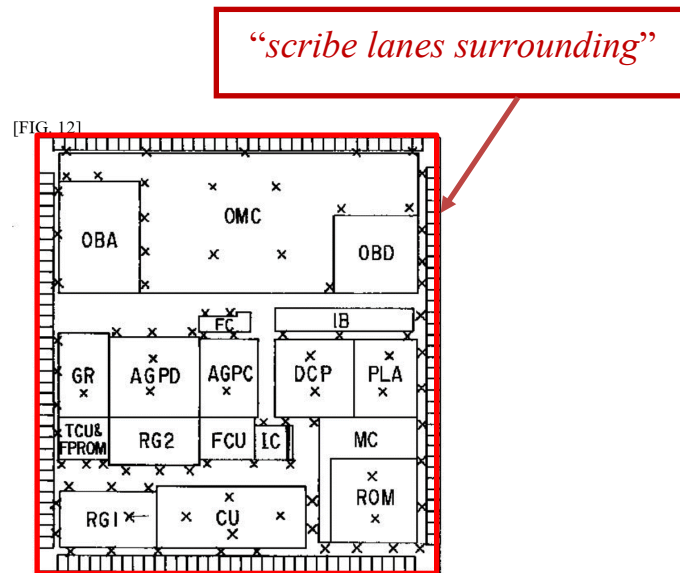
71. Thus, Matsunaga discloses a semiconductor substrate (e.g., silicon wafer) that includes a number of microprocessor circuit dies, which renders obvious “*providing a semiconductor substrate comprising thereon a number of integrated circuit dies,*” as claimed.

c. [1.1.2] *said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*

72. Matsunaga renders obvious this limitation.

73. **First**, as analyzed at limitation [1.1.1] Matsunaga renders obvious a plurality of microprocessor circuit dies, which correspond to the “*integrated circuit dies.*”

74. **Second**, it would have been obvious for the microprocessor circuit dies to be “*separated from each other by scribe lanes surrounding each*” microprocessor circuit die. As shown below at Figure 12, Matsunaga’s microprocessor circuit die has a straight cutline on the perimeter, which would have been understood by a POSITA to correspond to “*scribe lanes surrounding [] said integrated circuit die.*” See Ex.1004, 348-349; Ex.1008, 2:7-15, 3:63-66; Ex.1012, 9, 549, 575, Figures 1.3, 1.6, 20.5; Ex.1014, 101; Ex.1015, 72; Ex.1018, ¶¶99-143.



Ex.1005, FIG. 12 (annotated).

75. Furthermore, as illustrated below it was textbook knowledge that each integrated circuit “die, chip, and microchip” is surrounded and separated by “scribe lines,”

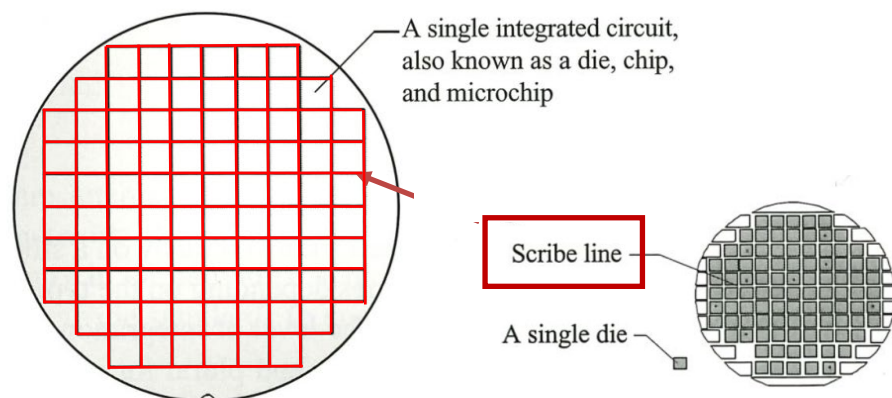


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3 (annotated).

Ex.1012, FIG. 1.6 (partial, annotated).

76. Furthermore, consistent with the analysis at limitations [1.0]-[1.1.1], it would have been obvious to a POSITA for a plurality of Matsunaga's microprocessor circuit chips or dies to be manufactured on a semiconductor substrate in accordance with well-known techniques, which would include using scribe lanes to surround and separate each microprocessor circuit chip or die so that they may later be cut out.

77. I also note that the purported inventive aspect of the '584 patent is not the use of scribe lanes. According to the '584 patent, prior art "U.S. Pat. No. 5,998,282 describes a method" where "[c]harging damage to integrated circuits during ion implantation and plasma processing of integrated circuit die in a semiconductor wafer is reduced by processing scribe lanes during wafer fabrication to facilitate the flow of current to and from the wafer substrate through the scribe lanes during integrated circuit fabrication and reduce current flow through integrated circuit components." Ex.1001, 1:59-2:1; Ex.1008, FIG. 3.

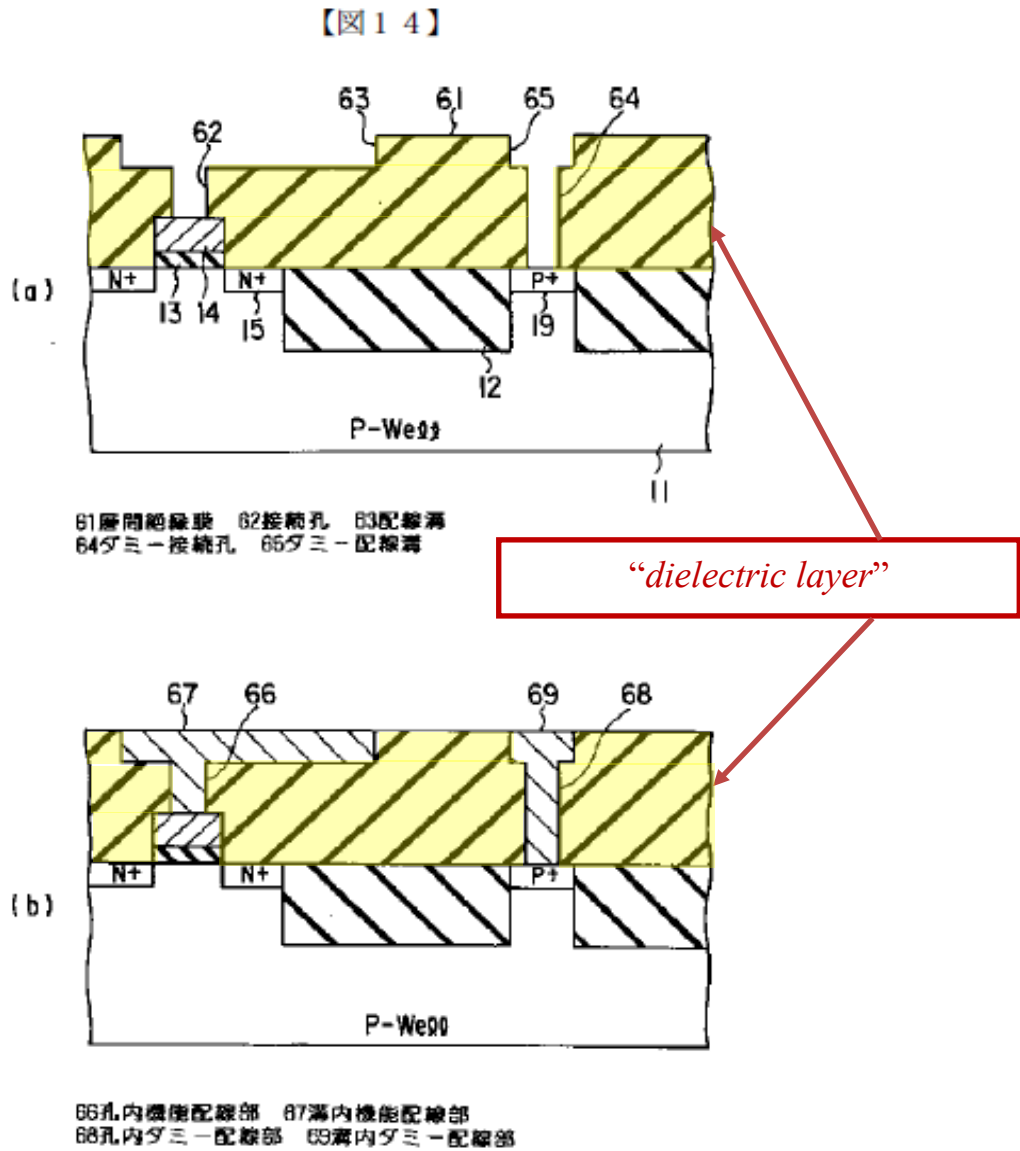
78. Thus, Matsunaga discloses that each microprocessor circuit die is separated and surrounded by scribe lanes, which renders obvious "*said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*" as claimed.

- a. [1.1.3] *wherein said semiconductor substrate comprises thereon a dielectric layer;*

79. Matsunaga renders obvious this limitation.

80. **First**, as analyzed at limitation [1.1.1], Matsunaga discloses a semiconductor substrate (e.g., silicon wafer), which corresponds to “*said semiconductor substrate.*”

81. **Second**, Matsunaga discloses “*a dielectric layer.*” Matsunaga, in the context of Figure 14, discloses that “an **interlayer insulating film 61 is formed over a substrate** whereon MOS transistors, or the like, are formed, and a connecting hole 62 and interconnection groove 63 for forming an interconnection, in the so-called dual damascene structure.” Ex.1005, [0055]. As illustrated below at Figure 14, Matsunaga’s interlayer insulating film 61 is formed on the semiconductor substrate and serves to insulate various conducting features from each other.



Matsunaga, FIGS. 14 (a) (b) (annotated).

82. It would have been understood that Matsunaga’s interlayer insulator film 61 is a dielectric layer (e.g., silicon oxide or silicon nitride) as these terms are used interchangeably in semiconductor devices. *See e.g.*, Ex.1007, [0118]

(“...interlayer insulating film...[may be] silicon oxide films or silicon nitride films.”); Ex.1009, 6:67 (“...a silicon dioxide as the dielectric...”); Ex.1014, 6, 141 (“When dielectrics are used in electrical circuits or devices they are referred to as insulators.”); *see also* Ex.1004, 639 (“...Low-K dielectric films are important in advanced IC applications because their use can significantly improve circuit performance characteristics...”); Ex.1012, 696, Fig. 15-21.

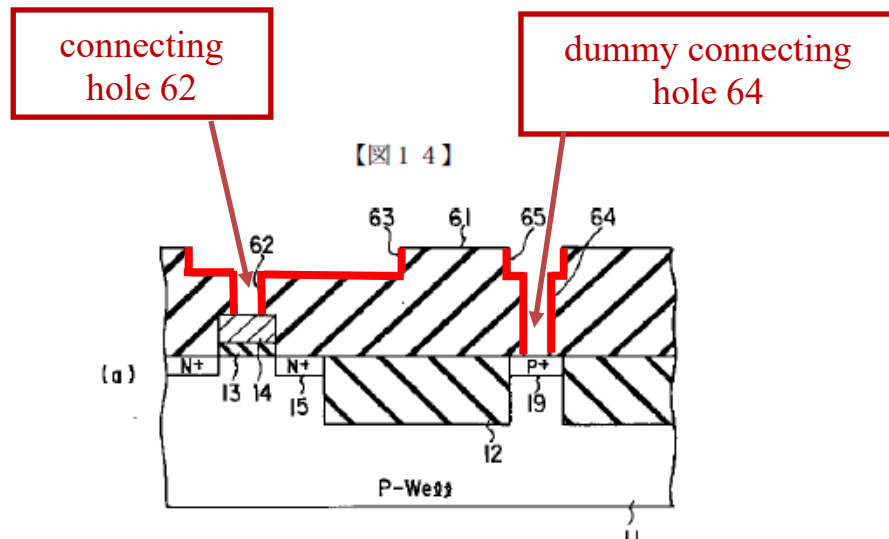
83. Thus, Matsunaga discloses forming a dielectric interlayer insulating film on the semiconductor substrate (e.g., wafer), which renders obvious that “*said semiconductor substrate comprises thereon a dielectric layer,*” as claimed.

b. [1.2.1] *forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,*

84. Matsunaga renders obvious this limitation.

85. First, as analyzed at [1.1.3], Matsunaga discloses an interlayer insulating film 61, which corresponds to the “*dielectric layer.*” Matsunaga further discloses that “a connecting hole 62 and interconnection groove 63” are formed in the interlayer insulating film 61 “in the so-called dual damascene structure” and that “dummy connecting holes 64 and dummy interconnection grooves 65 are also formed at the same time through the RIE process.” Ex.1005, [0055].

86. Matsunaga's Figure 14 (a), reproduced below, illustrates that its MOS transistor with a "dual damascene structure" (outlined in red) includes connecting hole 62 and dummy connecting hole 64:



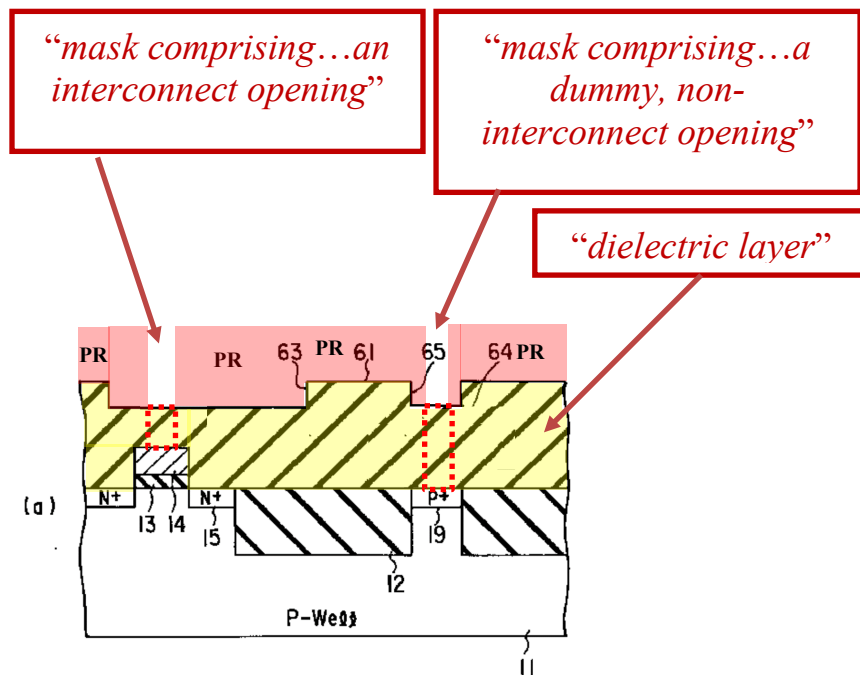
Ex.1005, FIG. 14 (a) (annotated).

87. **Second**, Matsunaga renders obvious “forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening.” Matsunaga discloses, relative to Figure 14, that its connecting hole 62 (interconnect opening) and dummy connecting hole 64 (dummy, non interconnect opening) are “formed at the same time through the RIE process.” Ex.1005, [0055]. The result of this step is a “dual damascene structure.” Id. Matsunaga further discloses, relative to Figure 13, that RIE etching is performed using a “resist” to provide the desired pattern. See e.g., Ex.1005, [0003] (“...when

patterning... [using] resist.”). Matsunaga accordingly discloses and renders obvious that when RIE etching is used to create the dual damascene structure of Figure 14, it uses resist masks as shown in the process of Figure 13.

88. Further underscoring the obviousness of this process, it was well-known that patterning for a “dual damascene structure” includes utilizing photoresist masks with corresponding openings. Ex.1004, 674-677, Fig. 15-3. Accordingly, it would have been obvious to a POSITA, considering Matsunaga’s MOS transistor with a “dual damascene structure,” to use a photoresist mask over interlayer insulating film 61, with the photoresist mask having an opening for connecting hole 62 and an opening for dummy connecting hole 64.

89. Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have implemented well-known photoresist techniques (either as disclosed relative to Matsunaga Fig. 13 or from the standard practice of a POSITA) to form connecting hole 62 and dummy connecting hole 64:



Ex.1005, FIG. 14 (a) (modified and annotated to show photoresist to form Matsunaga's MOS transistor with a dual damascene structure).

90. Thus, Matsunaga renders obvious a dual damascene process that includes forming over the interlayer insulating film a photoresist mask that comprises an interconnect opening and a dummy, non-interconnect opening, which renders obvious *“forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,”* as claimed.

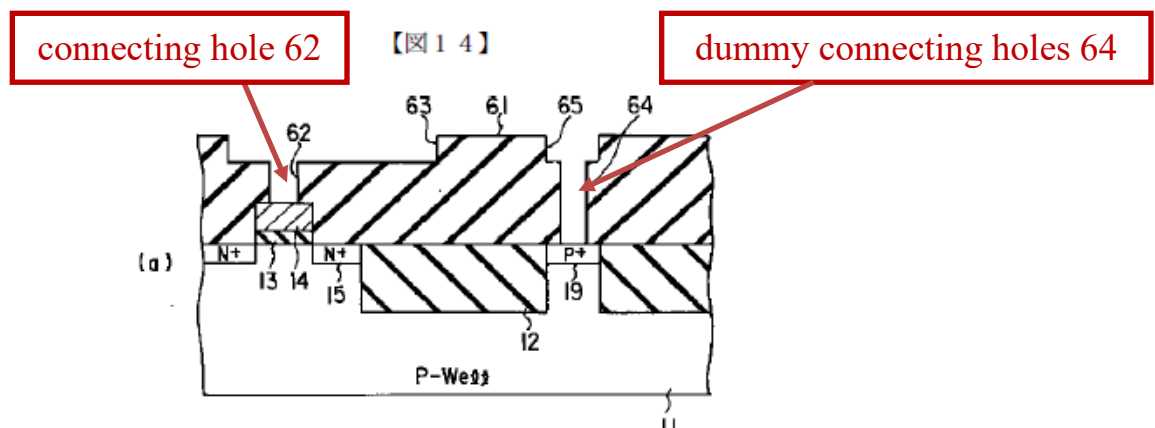
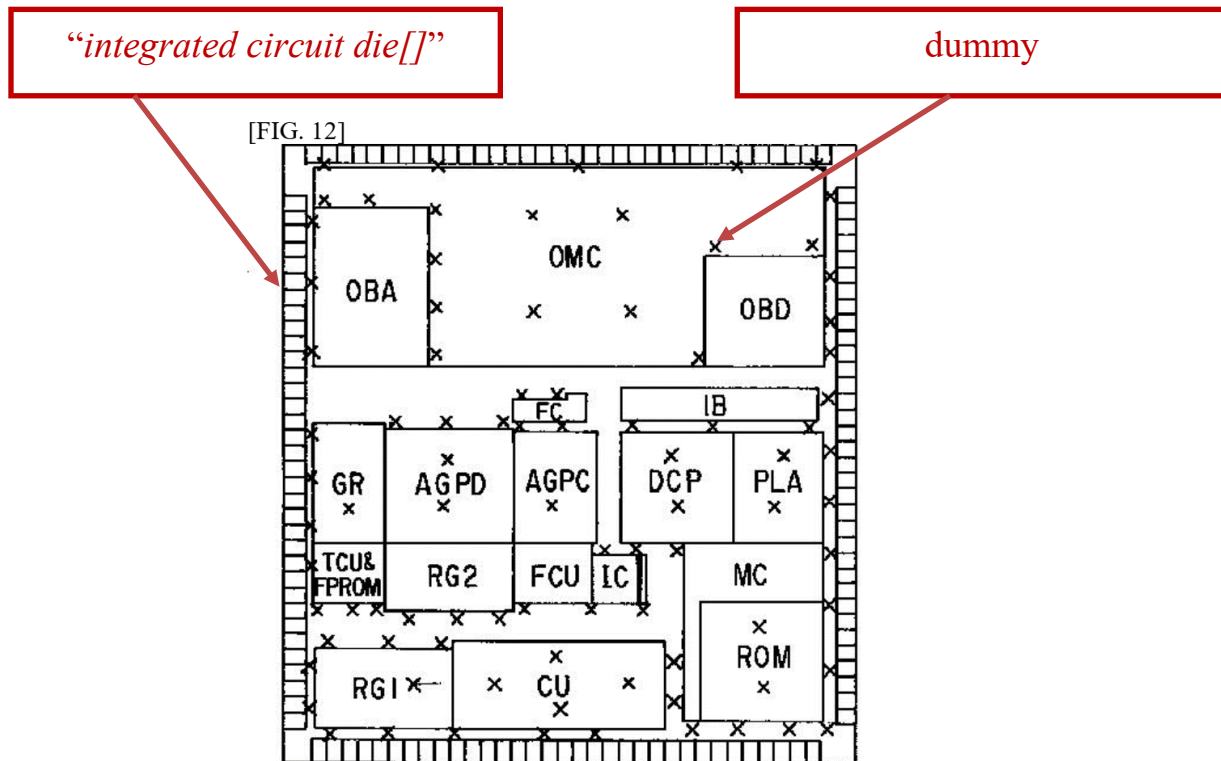
- a. [1.2.2] *wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;*

91. Matsunaga renders obvious this limitation.

92. First, as analyzed at limitation [1.1.1], Matsunaga renders obvious microprocessor circuits (chips or dies), with each individual microprocessor circuit corresponding to “*each said integrated circuit die*.” Further, as analyzed at limitation [1.2.1], Matsunaga discloses that the photoresist mask has an interconnect opening and a dummy, non-interconnect opening, which correspond to “*said interconnect opening and said dummy, non-interconnect opening*.”

93. Second, Matsunaga renders obvious that both openings “*are formed within each said integrated circuit die*.”

94. Consistent with the analysis in the preamble [1.0], Matsunaga’s MOS transistor teachings apply when manufacturing the microprocessor circuit illustrated at Figure 12. Ex.1005, [0053], Fig. 12. In more detail, Matsunaga discloses that “a dummy interconnection is applied to a microprocessor circuit... arranged at the locations indicated by the ‘X’ marks.” Ex.1005, [0053]. As illustrated below at Figure 12, Matsunaga’s microprocessor circuit (chip or die) (“*said integrated circuit die*”) has a dummy interconnection within the die area.



95. It would have been obvious to a POSITA for each microprocessor circuit (chip or die) illustrated at Matsunaga’s Figure 12 that is manufactured on a

silicon to include a MOS transistor illustrated at Figure 14. Ex.1015, 7 (describing that a chip's transistor count as of 2001 was "55,000,000."). In such instances, the microprocessor circuit (chip or die) of Figure 12 would be manufactured per the sequence analyzed at limitation [1.2.1], including forming a photoresist mask that has an interconnect opening (for connecting hole 62) and a dummy, non-interconnect opening (for dummy connecting hole 64). Moreover, it would have been obvious for the masking process to be also utilized when forming each microprocessor circuit (chip or die) on a semiconductor substrate (e.g., silicon wafer) as analyzed at limitations [1.1.1]-[1.1.2].

96. Thus, Matsunaga renders obvious that the photoresist mask interconnect opening and dummy, non-interconnect opening, are both formed within each microprocessor circuit (chip or die), which renders obvious "*said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die*" as claimed.

- b. ***[1.3] performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and***

97. Matsunaga renders obvious this limitation.

98. First, as analyzed at limitations p1.1.3], [1.2.1], Matsunaga renders obvious that over a dielectric layer (“*dielectric layer*”) is a photoresist mask with an interconnect opening and a dummy, non-interconnect opening, which correspond to “*said interconnect opening and said dummy, non-interconnect openings of said mask.*”

99. Second, during prosecution of the ’584 patent, Applicant contended that the plasma etching step requires “concurrently” etching of the “dummy, non-interconnect structures” and the “the interconnect structures.” Ex.1002, 31-32. The claims of the ’584 patent, however, do not require this “concurrently” etching step. Nevertheless, to the extent that “concurrently” etching is a claim requirement, Matsunaga discloses or renders it obvious.

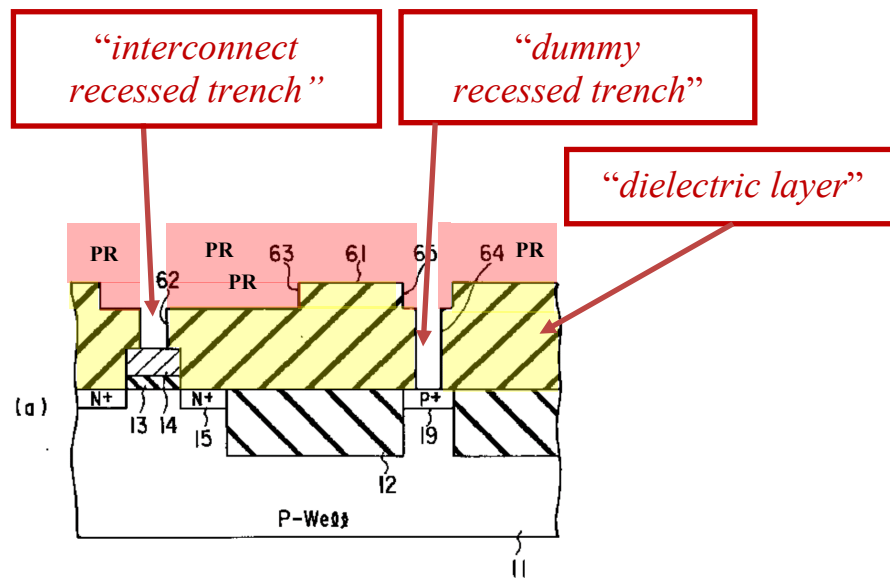
100. Matsunaga discloses “*performing a plasma etching process...thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer.*” Matsunaga discloses that forming the dual damascene structure MOS transistor with includes performing “**a plasma process such as RIE**” to etch the “interlayer insulating film 61,” thereby forming both the “connecting hole 62” and the “dummy connecting holes 64.” Ex.1005, [0009], [0030], [0055]-[0056]. Matsunaga makes clear that connecting hole 62 and dummy connecting hole 64 are formed “**at the same time through the RIE plasma process.**”

FIG. 14 (A) is that which depicts a state wherein an interlayer insulating film 61 is formed over a substrate whereon MOS transistors, or the like, are formed, and a **connecting hole 62 and interconnection groove 63** for forming an interconnection, in the so-called dual damascene structure, to the interlayer insulating film 61 are formed through an RIE process, but **in this case dummy connecting holes 64 and dummy interconnection grooves 65 are also formed at the same time through the RIE process.**

Ex.1005, [0055]; *see also* Ex.1005, [0056] (“In the present embodiment, the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed **simultaneously** in the RIE process.”). Because the same RIE plasma process is used, “electric charges supplied to the gate” through connecting hole 62 are “also [supplied] to the P+ dopant diffusion layer 19” through dummy connecting hole 64. Ex.1005, [0056]. “Consequently, the electric field that acts on the gate insulating film 13 is weakened, making it possible to prevent charging damage.” Ex.1005, [0056].

101. Moreover, consistent with conventional manufacturing techniques, analyzed at limitation [1.2.1], it would have been obvious that to form Matsunaga’s “dual damascene structure,” etching the interlayer dielectric layer is performed using the openings of the photoresist mask. Ex.1004, 675-677, FIG. 15-5. Provided

below is a modified Figure 14 (a) of Matsunaga, illustrating how Matsunaga's RIE plasma process ("a plasma etching process") etches through the mask openings to form connecting hole 62 ("interconnect recessed trench") and dummy connecting hole 64 ("dummy recessed trench") in the dielectric layer ("dielectric layer").



Ex.1005, FIG. 14 (a) (modified and annotated to show etching using a photoresist to form Matsunaga's MOS transistor with a dual damascene structure).

102. Thus, Matsunaga renders obvious damascene processing that uses an RIE plasma etch process to simultaneously etch interlayer insulating film through the photoresist mask conductor openings and dummy conductor openings, thereby forming a connecting hole and a dummy connecting hole in the interlayer insulating film, which renders obvious *"performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-*

interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer,” as claimed.

- c. **[1.4.1] filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,**

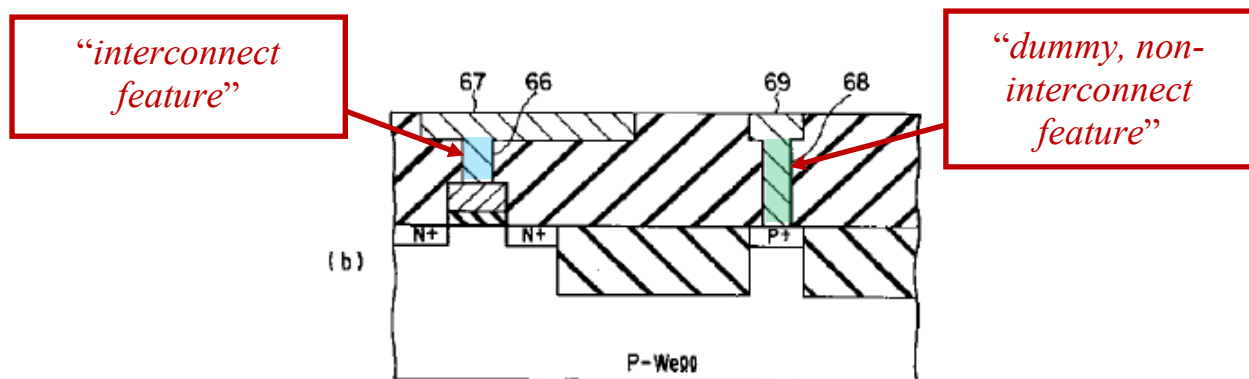
103. Matsunaga renders obvious this limitation.

104. **First**, as analyzed at limitation [1.3], Matsunaga discloses forming a connecting hole 62 and a dummy connecting hole 64, which respectively correspond to “*said interconnect recessed trench and said dummy recessed trench.*”

105. **Second**, Matsunaga discloses that the holes are “*fill[ed]*” with “*conductive materials to form an interconnect feature and a dummy, non-interconnect feature.*” In the context of Figure 14, Matsunaga explains that “[a]fter the RIE process has been completed, **metal** for a prescribed interconnection **is deposited over the entire surface.**” Ex.1005, [0057]. In this way, “**an interconnecting portion 66 [] is buried in the connecting hole 62 (hereinafter termed an in-hole functional interconnecting portion) and ... an interconnecting portion 68 [] is buried in the dummy connecting hole 64 (hereinafter termed an in-hole dummy interconnecting portion).**” Ex.1005, [0057].

106. A POSITA would have understood that depositing metal over the entire surface results in “*filling*” any open holes with “*conductive materials*” to form the functional interconnecting portion 66 and the dummy interconnecting portion 68. Matsunaga’s dummy interconnecting portion 68 is “*non-interconnect*” as that term is used in the ’584 patent since it is “**not used in actual circuit operation**” and grounded to the substrate. Ex.1005, [0029]; limitation [1.4.2] (“*non-interconnect feature is...grounded to said semiconductor substrate*”).

107. As illustrated below at Matsunaga’s Figure 14(b), after the metal deposition process, the MOS transistor’s connecting hole 62 has a buried functional interconnecting portion 66 (“*interconnect feature*”) and the dummy connecting hole 64 has a dummy interconnecting portion 68 (“*dummy, non-interconnect feature*”).



Ex.1005, FIG. 14 (b) (annotated).

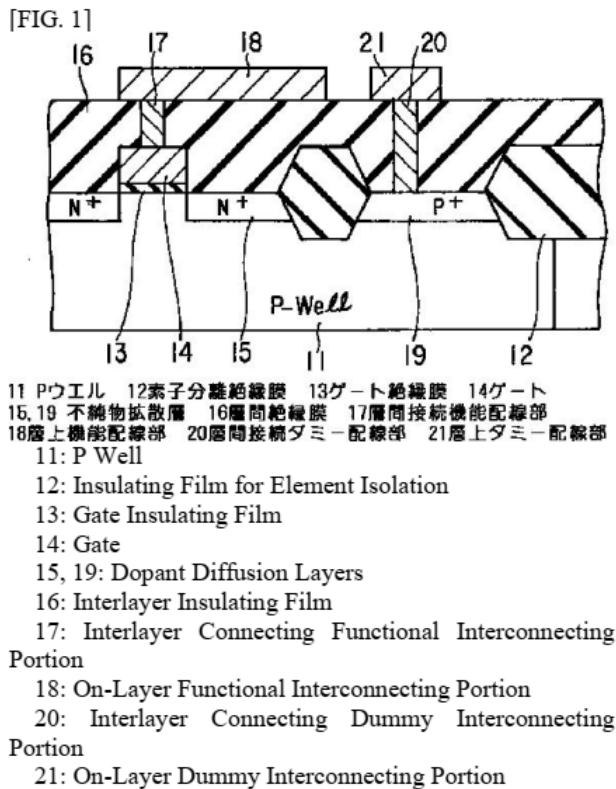
108. Thus, Matsunaga discloses filling the connecting hole and the dummy connecting hole with metal to form a functional interconnecting portion and a dummy interconnecting portion, which renders obvious “*filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,*” as claimed.

- d.** [1.4.2] *wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;*

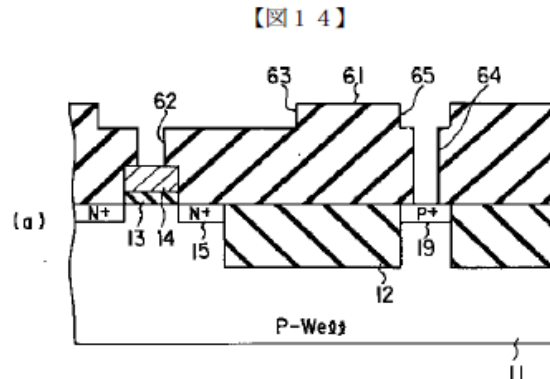
109. Matsunaga renders obvious this limitation.

110. First, as analyzed at limitation [1.1.1], Matsunaga discloses a semiconductor substrate (e.g., silicon wafer), which corresponds to “*said semiconductor substrate.*” And, as analyzed at limitation [1.4.1], Matsunaga discloses a functional interconnecting portion and a dummy interconnecting portion, which respectively correspond to “*said interconnect feature*” and “*said dummy, non-interconnect feature.*”

111. Second, as already noted above, in Matsunaga’s Figure 14, “structural elements that are substantially identical or corresponding to those in the first embodiment, depicted in FIG. 1, are assigned identical numbers, and detailed explanations thereof will be omitted.” Ex.1005, [0054].



Ex.1005, Fig. 1.



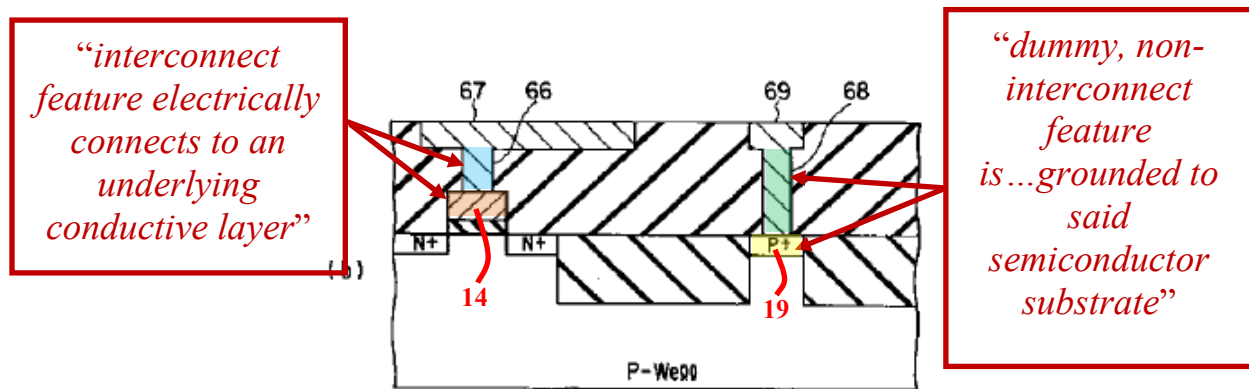
Ex.1005, Fig. 14 (a).

112. Matsunaga explains that the “functional interconnection 17 is used in actual circuit operation is connected to the gate 14” and that the “dummy interconnection that is not used in actual circuit operation...[and] is connected to the dopant diffusion layer 19 [in the substrate].” Ex.1005, [0029]; *see also* Ex.1005, Claim 1 (“a dummy interconnection... not used in circuit operation, [is] connected to the semiconductor substrate.”).

113. A POSITA would have understood that gate 14 is a “*conductive layer*” because it is used in circuit operation to switch the MOS transistor. Also, a POSITA

would have understood that connecting the dummy interconnect to the dopant diffusion layer 19 is to “ground[]” it to the substrate because the dopant diffusion layer 19 serves to electrically connect the dummy interconnect to the substrate.

114. As illustrated at Figure 14 (b), reproduced below, Matsunaga’s functional interconnecting portion 66 is electrically connected to underlying gate electrode 14 (“*underlying conductive layer*”) and dummy interconnecting portion 68 is connected to the substrate via P+ dopant diffusion layer 19 (“*grounded to said semiconductor substrate*”).



Ex.1005, FIG. 14 (b) (annotated).

115. Thus, Matsunaga discloses that the functional interconnecting portion is electrically connected to underlying gate electrode and that the dummy interconnecting portion is grounded to the semiconductor substrate, which renders obvious “*said interconnect feature electrically connects to an underlying*

conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate,” as claimed.

- e. ***[1.5] wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.***

116. Matsunaga renders obvious this limitation.

117. **First**, as analyzed at limitation [1.2.1], Matsunaga renders obvious a dual damascene process that uses a photoresist mask with a dummy opening, which corresponds to the “*dummy, non-interconnect opening.*” Further, as analyzed at limitation [1.3], the dummy opening in the photoresist mask is used in a RIE plasma process, which corresponds to the “*plasma etching process.*”

118. **Second**, Matsunaga discloses that because “the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed simultaneously in the RIE process” the “**electric charges supplied to the gate**” are also supplied “**to the P+ dopant diffusion layer 19 that is formed in the substrate**,” which can reduce the potential difference between the electropotential of the gate and the electropotential of the substrate.” Ex.1005, [0056]; *see also* Ex.1005, [0019], [0029]. A POSITA would have understood this passage as disclosing that the dummy opening provides a lower-resistance pathway for current to travel, thus (1)

increasing the current through the “*shunt path*” (i.e., the path that does not go through the integrated circuits); and (2) decreasing the voltage at the gate, thereby decreasing the current flow at the integrated circuits (such as the gate). Ex.1008, 1:66 - 2:6. That is, the shut path increases the current flow through the dummy connection while decreasing the current flow through the device connection. As such, Matsunaga’s disclosure that the dummy connecting hole 64 (which is defined by the mask dummy opening) supplies electric charges to the P+ dopant diffusion layer 19 during the RIE plasma process discloses “*increas[ing] an in-die shunt path current flow during said plasma etching process.*”

119. As noted above, Matsunaga teaches that, as a result of the dummy opening, the electrical potential at the gate is reduced. Ex.1005, [0056]; see also Ex.1005, [0019], [0029]. A POSITA would have understood that by reducing the electrical potential of the gate, the possibility for damage to the integrated circuit is reduced because less energy is being supplied to the gate during the RIE process. Matsunaga further explains that as a consequence of supplying electric charges to the P+ dopant diffusion layer 19 during the RIE plasma process, “the electric field that acts on the gate insulating film 13 is weakened, making it possible to **prevent charging damage**.” Ex.1005, [0056]; *see also* Ex.1005, [0019] (“... prevent charging damage in the plasma processes, such as RIE, or the like, when processing

the connecting holes or interconnection grooves, making it possible to **prevent damage to the gate insulating films.**”). Because, as analyzed above, the MOS transistors are within the microprocessor circuit die, preventing charge damage to the MOS transistor, e.g., gate insulating film, “*thereby reduc[es] charge damage to said integrated circuit dies,*” as claimed.

120. Thus, Matsunaga renders obvious that the photoresist mask dummy openings and dummy connecting holes increases an in-die shunt path current flow during the RIE plasma process, thereby preventing charge damage to MOS transistors of the microprocessor circuit dies, which renders obvious that “*said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies,*” as claimed.

3. Claim 3

a. [3.0] *The method according to claim 1 wherein said mask comprises photoresist.*

121. As analyzed at limitation [1.2.1], it would have been obvious to use a photoresist mask in a dual damascene process, which renders obvious that “*said mask comprises photoresist,*” as claimed.

4. Claim 4

- a. **[4.0] *The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.***

122. As analyzed at limitations [1.2.1]-[1.3], the connecting hole is a dual damascene opening, which renders obvious that “*said interconnect recessed trench is a damascene opening,*” as claimed.

5. Claim 5

- b. **[5.0] *The method according to claim 1 wherein said interconnect recessed trench is a contact hole.***

123. As analyzed at [1.3] and [1.4.1]-[1.4.2], the connecting hole is a contact hole, which renders obvious that “*said interconnect recessed trench is a contact hole,*” as claimed.

B. Ground 2: Claim 2 is Obvious over Matsunaga and Jaso

124. The combination of Matsunaga and Jaso renders obvious Claim 2 as discussed below.

1. Summary of Jaso

125. Like the '584 patent, U.S. Patent No. 6,093,631 to Jaso *et al.* (Ex.1009, “Jaso”) generally discloses a method of manufacturing a semiconductor device. Ex.1009, 2:7-10.

126. Jaso recognizes that when performing chemical mechanical polishing (“CMP”) “problems such as dishing occur causing a non-planar surface,” which results in “significant overpolish...erosion of dielectric...increased sheet resistance,” among other “problems at later steps in the fabrication process.” Ex.1009, 2:7-27. To address these problems, Jaso uses dummy metal pattern to “provid[e] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:2-5. Jaso defines a “pattern factor for a particular area or region...as the area covered by the metal divided by the total area of the particular area or region” and states that typically “the pattern factor is 50%.” Ex.1009, 3:5-13. In another example, Jaso discloses that “a method is provided to set a predetermined high pattern factor design limit of say 60-90%, preferably 70–80%.” Ex.1009, 3:38-40. In yet another example, Jaso discloses that “a predetermined low pattern factor design limit is set... for example, 20-50%.” Ex.1009, 3:44-47; *see also* Ex.1009, 7:24-8:18 (“determining the metal density for each region of each chip based on the circuit pattern... adding a dummy circuit pattern to each region on each chip to provide at least a minimum metal density... maximum metal density is about 60-90%... minimum metal density is about 20-50%.”).

2. Obviousness Combination Matsunaga and Jaso

127. A POSITA would have been motivated to combine the teachings of Matsunaga and Jaso, as discussed below.

a. Analogous Art

128. Jaso, like Matsunaga, is in the same field of endeavor as the '584 patent, pertaining to semiconductor manufacturing. Ex.1001, 1:15-18, 7:12-13; Ex.1005, [0055]; Ex.1009, 2:45-50. As such, a POSITA considering Matsunaga's semiconductor manufacturing method, would have also considered Jaso, which provides additional teachings applicable to Matsunaga.

b. Combination Rationale

129. A POSITA would have been motivated to combine the teachings of Jaso with Matsunaga to produce predictable results as discussed below.

130. Matsunaga teaches a process to make MOS devices that utilizes CMP. *See* Ex.1005, [0055]-[0057], FIG. 14 (b). Jaso teaches that CMP may cause “dishing” and other problems (e.g., over polishing, erosion of dielectrics, increased sheet resistance, etc.). Ex.1009, 2:7-27. To address the noted problems, Jaso teaches that it is important to “provid[es] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:3-5. Specifically, Jaso teaches that interconnect openings and dummy openings should be patterned such

that the area covered by metal divided by the total area has a high pattern factor design limit of 60-90% and low pattern factor design limit of 20-50%. Ex.1009, 3:10-47; Ex.1009, 7:20-8:18.

131. It would have been obvious to a POSITA to apply the teachings of Jaso, when implementing Matsunaga's method (which utilizes CMP), to ensure that sufficient metal surfaces are present in the dummy and interconnect areas (i.e., 20-90% coverage) to overcome dishing effects and other non-planarization problems (e.g., over polishing, erosion of dielectrics, increased sheet resistance, etc.). Ex.1009, 2:7-27 ("**The dishing effect is particularly serious** since the polishing needs to be carried out until the metal is cleared on the entire wafer...It has been found that a **significant overpolish** is typically needed which results in **erosion of dielectric...resulting in an increased sheet resistance...**"); 3:29-31 ("**To overcome the dishing effect and other non-planarization**, the invention decreases the differences in pattern factors for regions on the chip.").

132. The proposed combination is merely applying a known technique to a known device or method (e.g., Jaso's technique of controlling the interconnect openings and dummy openings pattern to have a low pattern factor design limit of 20%, with Matsunaga's method and semiconductor device) ready for improvement

(e.g., reduce dishing effects, over polishing, erosion of dielectrics, and increased sheet resistance, etc.) to yield predictable results.

133. These reasons, separately and together, would have motivated a POSITA to combine the teachings of Jaso with Matsunaga.

c. Reasonable Expectation of Success

134. The results would have been predictable and there would have been a reasonable expectation of success in the combination given that both Jaso and Matsunaga relate to semiconductor processing. Modifying Matsunaga's method and semiconductor device to have a low pattern factor design limit of 20% would have been a straightforward and simple matter of utilizing a computer algorithm to generate dummy patterns that meet the desired metallization lower limit. *See* Ex.1009, 3:65-4:2 ("Basically, the data defining the metal features on a given damascene level would be inputted into a computer and an algorithm used to generate dummy circuitry to increase the circuitry to at least a lower pattern factor limit for a particular region."); *see also* Ex.1007, [0106] ("The layout of the conductors [] can be set as appropriate, depending on the process characteristics in the CMP process or a design rule of the dummy conductors or the like."). The reasonable expectation of success is also supported by others that had implemented

similar pattern densities. See Ex.1016, [0035] (“[T]he density of the dummy patterns...is in the range of 10-25%.”).

3. Claim 2

- a. [2.0] *The method according to claim 1 wherein an exposed surface area of said interconnect and dummy, non-interconnect openings is higher than 5% of a die area of each said integrated circuit die.*

135. Matsunaga in combination with Jaso renders obvious this claim.

136. **First**, as analyzed at limitation [1.2.1], Matsunaga renders obvious forming over the interlayer insulating film a photoresist mask that comprises an “*interconnect opening*” (for connecting hole) and a “*dummy, non-interconnect opening*” (for dummy connecting hole).

137. **Second**, Jaso discloses a device that has interconnect openings 15 (a-d) and dummy openings 20. Ex.1009, 5:66-6:9, Figs. 11A-11D. Jaso utilizes dummy patterns to “provid[e] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:3-5. Jaso explains that a “pattern factor for a particular area or region may be defined as the **area covered by the metal divided by the total area** of the particular area or region” and states that typically “**the pattern factor is 50%.**” Ex.1009, 3:5-10. Jaso teaches that the area covered by metal in figure 11D is the same as the area of the interconnect openings

15 (a-d) and dummy openings 20 in figure 11B. Ex.1009, Figs. 11B, 11D. In another example, Jaso discloses that “a method is provided to set a predetermined **high pattern factor design limit of say 60-90%, preferably 70–80%.**” Ex.1009, 3:38-40; *see also* Ex.1009, 8:17-18. In yet another example, Jaso discloses that “a predetermined **low pattern factor design limit is set... for example, 20-50%.**” Ex.1009, 3:44-47; *see also* Ex.1009, 7:20-8:18.

138. It would have been obvious to a POSITA that to form patterns, per Jaso’s examples, such that a photoresist mask is patterned to have an exposed surface area of the interconnect openings and the dummy openings to be higher than 20% of the integrated circuit chip or die area. Ex.1009, 3:3-5 (“...uniform distribution of damascene metal line circuitry across each integrated circuit chip.”).

139. It would have been obvious to a POSITA to apply Jaso’s teachings to Matsunaga and provide a uniform distribution of metal line circuitry across each integrated circuit microprocessor to beneficially “overcome the dishing effect and other non-planarization” related problems, such as erosion of dielectrics, over polishing areas, increased sheet resistance, etc. Ex.1009, 2:11-32, 3:29-31; Obviousness Combination Matsunaga and Jaso.

140. In implementing the combination, a POSITA would have found it obvious for Matsunaga’s photoresist mask to be patterned to have an exposed

surface area of the interconnect opening (for connecting hole) and the dummy, non-interconnect opening (for dummy connecting hole), to be higher than 20% of the area of each microprocessor circuit (chip or die).

141. Thus, Matsunaga in combination with Jaso discloses that the dual damascene photoresist mask is patterned to have the interconnect opening (for connecting hole 62) and the dummy, non-interconnect opening (for dummy connecting hole 64) at least 20% of a die area of each of the microprocessor circuit (chip or die), which renders obvious “*wherein an exposed surface area of said interconnect and dummy, non-interconnect openings is higher than 5% of a die area of each said integrated circuit die,*” as claimed.

C. Ground 3: Claim 6 is Obvious over the combination of Matsunaga and Appel

142. The combination of Matsunaga and Appel renders obvious Claim 6 as discussed below.

1. Summary of Appel

143. U.S. Patent No. 5,605,861 to Appel (Ex.1017, “Appel”) generally pertains to semiconductor manufacturing. Ex.1017, Title, Abstract. In this context, Appel teaches forming a MOS transistor gate electrode by diffusing impurities in polysilicon. Ex.1017, 2:6-3:66, 4:13-55.

2. Obviousness Combination Matsunaga and Appel

144. A POSITA would have been motivated to combine the teachings of Appel with Matsunaga, as discussed below.

a. Analogous Art

145. Appel, like Matsunaga, is in the same field of endeavor as the '584 patent, pertaining to methods of semiconductor manufacturing, including MOS transistors. Ex.1001, 1:15-18, 4:52-54; Ex.1005, [0055]; Ex.1017, Title, Abstract. As such, a POSITA considering Matsunaga's method, which includes forming a MOS transistor, would have also considered Appel, which provides additional teachings applicable to Matsunaga's MOS transistor.

b. Combination Rationale

146. A POSITA would have been motivated to combine the teachings of Appel with Matsunaga to produce predictable results as discussed below.

147. Matsunaga teaches that its device includes a "MOS transistors" with a "gate 14." *See* Ex.1005, [0055]-[0056], FIGS. 1, 14. However, since MOS transistors were well-known in the art, Matsunaga provides limited detail regarding the formation of gate electrode 14. Appel provides this well-known technique and teaches the implementation details. In particular, Appel teaches forming a MOS transistor gate electrode by diffusing impurities from boro-silicate glass (BSG) or

phospho-silicate glass (PSG) into polysilicon region above a gate dielectric.

Ex.1017, 2:42-54; *see also* Ex.1017, 2:6-66, Ex.1017, 3:30-66. Appel explains that “[t]he dopant can be diffused from these doped glass films into adjacent films of polysilicon [gate electrode] without having to worry about implant damage or implant straggle.” Ex.1017, 2:52-54. It would have been obvious to a POSITA to apply the diffused polysilicon gate electrode teachings of Appel because these details are directly applicable to successfully implementing the gate electrode of Matsunaga’s MOS transistor. Implementing Matsunaga’s MOS transistor gate electrode per Appel’s teachings would have been recognized as a suitable option, and therefore obvious to a POSITA.

148. Additionally, a POSITA would have been motivated to apply Appel’s teachings, when implementing the gate electrode of Matsunaga’s MOS transistor, because it is a more desirable alternative to ion implantation of impurities into a polysilicon gate electrode. Ex.1017, 2:52-54 (diffusion forms the gate electrode “without having to worry about implant damage or implant straggle.”).

149. The proposed combination is merely a simple substitution of one known element for another (e.g., substituting the gate of Matsunaga’s MOS transistor for a diffused polysilicon gate electrode, as Appel teaches) to obtain predictable results of forming a gate electrode for a functional MOS transistor.

c. **Reasonable Expectation of Success**

150. The results would have been predictable and there would have been a reasonable expectation of success in the combination given that it was conventional and well-known in the art how to form a gate electrode of polysilicon. *See* Ex.1008, 2:53-56 (“...polysilicon (gate)...”); Ex.1012, 436 (“...polysilicon transistor gates...”). Implementing Matsunaga’s semiconductor device to have a diffused polysilicon gate would have been a straightforward and simple matter of patterning polysilicon, doping, and annealing (as Appel teaches in detail), well within the level of skill in the art. Indeed, Appel references these processes as “Background of The Invention.” Ex.1017, 1:7-2:20.

3. **Claim 6**

a. **[6.0] *The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.***

151. Matsunaga in combination with Appel renders obvious this claim.

152. **First**, as analyzed at limitation [1.4.2], Matsunaga discloses an underlying gate electrode 14, which corresponds to the “*underlying conductive layer*.” Appel discloses how to form a gate electrode. In more detail, Appel discloses that a “**polysilicon gate layer...is doped by diffusing impurities into the polysilicon** from a doped silicate glass over the polysilicon gate layer.”

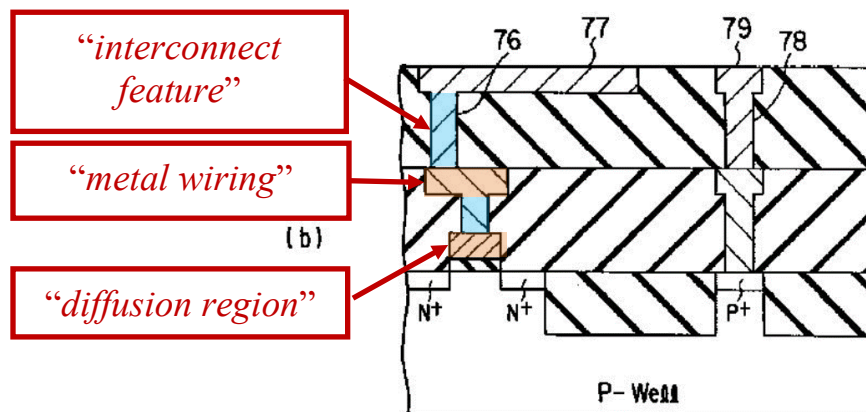
Ex.1017, 2:42-45. For example, “boro-silicate glass (BSG) and phospho-silicate glass (PSG)... can be used in accordance with the present invention, depending upon the impurity of interest.” Ex.1017, 2:45-54. **“The dopant can be diffused from these doped glass films into adjacent films of polysilicon [gate electrode]** without having to worry about implant damage or implant straggle.” Ex.1017, 2:52-54; *see also* Ex.1017, 2:6-66. Appel describes a process flow with BSG to form a “polysilicon gate portion p+.” *See* Ex.1017, 3:30-41, 4:13-65. Appel further explains that “process described above operates equally well for doping n + polysilicon from PSG.” Ex.1017, 3:65-66. Appel’s diffused polysilicon gate electrode corresponds to a “*diffusion region*,” as claimed.

153. It would have been obvious to a POSITA to implement Matsunaga’s gate electrode 14 as a polysilicon diffusion region, per Appel, because this is one suitable technique to implement gate electrodes. *See* Obviousness Combination Matsunaga and Appel.

154. Thus, Matsunaga in combination with Appel discloses that the gate electrode is implemented as a polysilicon diffusion region, which renders obvious that “*said underlying conductive layer comprises ... diffusion region*,” as claimed.

155. Second, the analysis in claim 1 focused on Matsunaga’s embodiment of Figures 14 (a) and (b). However, Matsunaga expands on that embodiment, in

Figures 15 (a) and (b), “which depicts a state wherein an interlayer insulating film 71 is formed on a lower portion structure that is formed through, for example, the process of FIG. 14, and a connecting hole 72 and an interconnection groove 73, for forming an interconnection of a dual damascene structure, are formed through an RIE process in the interlayer insulating film 71.” Ex.1005, [0058]. The further embodiment of Figure 15, which builds upon Figure 14, similarly has “the ability to weaken the electric field that acts on the gate insulating film 13, which can prevent charging damage.” Ex.1005, [0059].



Ex.1005, FIG. 15 (b) (annotated).

156. In the further embodiment of Figures 15 (a) and (b), functional interconnect 76, separately and together with functional interconnect 66, would correspond to the “interconnect feature,” while the metal line 67 and the gate electrode 14 as modified per Appel’s polysilicon diffusion region would correspond

to the “*underlying conductive layer...[that] comprises metal wiring and diffusion region.*”

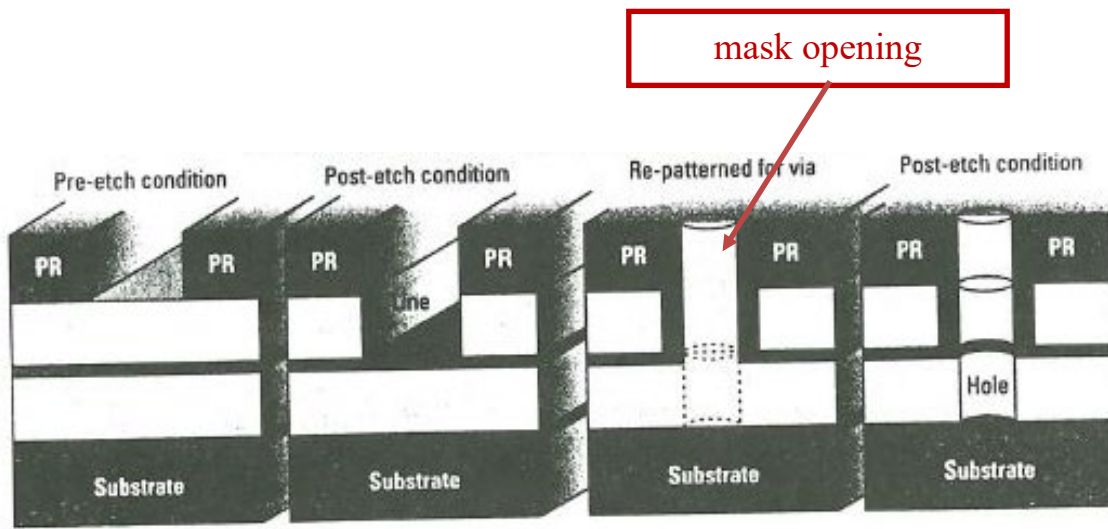
157. Thus, Matsunaga in combination with Appel discloses that the functional interconnect electrically connects to metal line and gate electrode implemented as a polysilicon diffusion region, which renders obvious that “*said underlying conductive layer comprises metal wiring and diffusion region,*” as claimed.

D. Ground 4: Claims 1 and 3-5 are Obvious over the combination of Matsunaga and Wolf

158. To the extent Patent Owner argues that Matsunaga alone is insufficient, the combination of Matsunaga and Wolf renders obvious Claims 1 and 3-5 as discussed below.

1. Summary of Wolf

159. The textbook titled “Silicon Processing for the VLSI Era,” by Wolf (“Wolf,” Ex.1004) teaches well-known dual-damascene processing using a mask comprising an opening shown below at FIG. 15-5. Ex.1004, 676-679.



Ex.1004, Fig. 15-5 (annotated).

2. Obviousness Combination Matsunaga and Wolf

a. Analogous Art

160. Like Matsunaga, Wolf is analogous art to the '584 patent, because it is in the same field of endeavor of manufacturing semiconductor devices, including using dual damascene processing. Ex.1001, 6:23-27, 7:12-13; Ex.1004, 674-677, Fig. 15-3; Ex.1005, [0055], [0058], [0063]. Accordingly, Wolf is analogous art to the '584 patent and a POSITA would have considered its teachings relevant when implementing Matsunaga's dual damascene teachings.

b. Combination Rationale

161. A POSITA would have been motivated to combine the teachings of Matsunaga and Wolf with a reasonable expectation of success.

162. Matsunaga seeks to form MOS transistors that have a “dual damascene structure.” Ex.1005, [0055], [0058], [0063]. Wolf provides implementation details regarding dual damascene methods suitable to form the dual damascene structure of Matsunaga’s MOS transistors. Ex.1004, 674-677, Fig. 15-3. It would have been obvious for a POSITA to consider and apply Wolf’s dual damascene technique, when implementing Matsunaga’s method of manufacturing MOS transistors that have dual damascene structure to achieve the results that Matsunaga describes; namely, to facilitate the manufacturing of a MOS transistor with a dual damascene structure.

163. The proposed combination is merely combining prior art elements (Wolf’s dual damascene technique with Matsunaga’s method for forming a dual damascene structure) according to known methods (Wolf provides significant details regarding dual damascene processing) to yield predictable results (facilitate the manufacturing of Matsunaga’s dual damascene structure).

c. Reasonable Expectation of Success

164. I note that the results would have been predictable and there would have been a reasonable expectation of success in the combination because Matsunaga and Wolf address the same technology, as analyzed above in the analogous art section. Also, a POSITA would have had a reasonable expectation of

success because the dual damascene teachings of Wolf are directly applicable to manufacture Matsunaga's dual damascene structure. Ex.1005, [0055], [0058]. Wolf's teachings would have been easily applied to Matsunaga because the proposed combination does not require any change to the dual damascene structure of Matsunaga. To the extent that any modification was needed to Matsunaga's method such that it includes Wolf's dual damascene technique, it would have been textbook knowledge and within the level of ordinary skill in the art. *See* Ex.1012, 307, 328.

165. The expectation of success is further evidenced by others that had used dual damascene processing to manufacture semiconductor devices. Ex.1010, 1:57-61("[A] dual damascene method is often used which forms in advance a wiring groove and a contact hole in an interlayer insulation film, and deposits a Cu layer by an electrolytic plating method or the like to fill the wiring groove and the contact hole as described above."); *see also* Ex.1016, [0070].

166. I note that the proposed combination of Matsunaga and Wolf relies on the teachings of the references—not on physical incorporation of the elements.

3. Claim 1

167. For the same reasons that I discussed above in Ground 1, Matsunaga renders obvious limitations [1.0]-[1.1.3] and [1.4.1]-[1.4.2] in Ground 4.

Furthermore, as discussed below, Matsunaga in combination with Wolf renders obvious limitations [1.2.1]-[1.3] and [1.5].

a. [1.0] *A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:*

168. As analyzed at Ground 1 limitation [1.0], Matsunaga discloses a method of preventing or reducing charging damage to integrated circuits during semiconductor manufacturing, which renders obvious “[a]method for reducing charging damage to integrated circuits during semiconductor manufacturing,” as recited in the preamble.

b. [1.1.1] *providing a semiconductor substrate comprising thereon a number of integrated circuit dies,*

169. As analyzed at Ground 1 limitation [1.1.1], Matsunaga discloses a semiconductor substrate (e.g., silicon wafer) that includes a number of microprocessor circuit dies, which renders obvious “providing a semiconductor substrate comprising thereon a number of integrated circuit dies,” as claimed.

c. [1.1.2] *said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*

170. As analyzed at Ground 1 limitation [1.1.2], Matsunaga discloses that each microprocessor circuit die is separated and surrounded by scribe lanes, which

renders obvious “*said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*” as claimed.

d. [1.1.3] *wherein said semiconductor substrate comprises thereon a dielectric layer;*

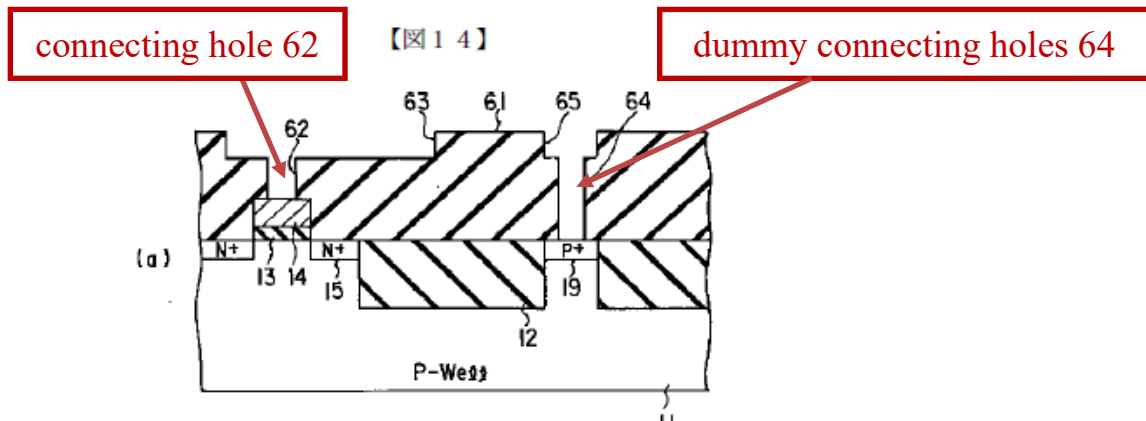
171. As analyzed at Ground 1 limitation [1.1.3], Matsunaga discloses that an interlayer insulating film is formed over the semiconductor substrate, which renders obvious that “*said semiconductor substrate comprises thereon a dielectric layer,*” as claimed.

e. [1.2.1] *forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,*

172. Matsunaga in combination with Wolf renders obvious this limitation.

173. First, as analyzed at Ground 1 limitation [1.2.1], Matsunaga’s MOS transistor has a “dual damascene structure” that includes a connecting hole 62 and dummy connecting hole 64, which respectively correspond to an “*interconnect*” and a “*non-interconnect.*”

174. Matsunaga’s Figure 14 (a), reproduced below, illustrates the resulting connecting hole 62 and dummy connecting hole 64:

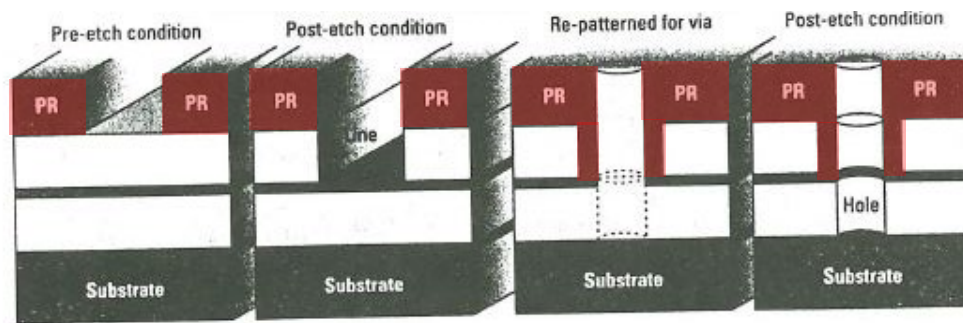


Ex.1005, FIG. 14 (a) (annotated).

175. While Matsunaga only briefly mentions the use of “resist” in its patterning process, such would have been well-known and conventional in the art. It would have been obvious to POSITA, considering Matsunaga’s MOS transistor to form a photoresist mask over interlayer insulating film 61, with the photoresist mask having an opening for connecting hole 62 and an opening for dummy connecting hole 64.

176. Wolf provides implementation details of processing techniques that were conventional/textbook and directly applicable when manufacturing Matsunaga’s MOS transistor of Figure 14(a), which has a “dual damascene structure.” Ex.1005, [0054]. Wolf discloses a “dual-damascene” sequence where a photoresist (PR) mask is used to etch a trench in an underlying interlayer dielectric. Ex.1004, 674-677, Fig. 15-3. Then, a second a photoresist (PR) mask is formed

with openings that are aligned with the trench that was etched previously. Ex.1004, 677. “The resist protects the other parts of the wafer surface (including the etched regions of the trenches) so that the via can be etched without further etching the dielectric in the trench[.]” Ex.1004, 677.

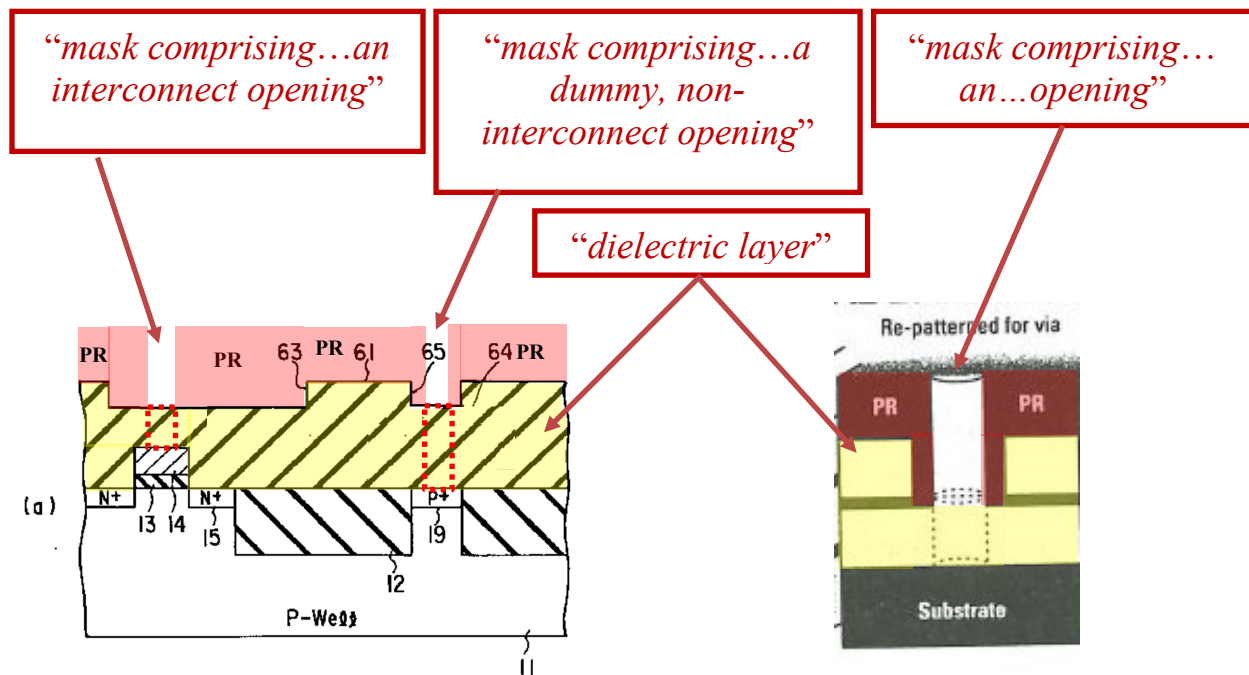


Ex. 1004, Fig. 15-5 (annotated).

177. It would have been obvious to use this process described in Wolf to create both Matsunaga’s interconnect openings and non-interconnect openings. As noted, Matsunaga discloses that connecting hole 62 and dummy connecting hole 64 are “formed at the same time through the RIE process.” Ex.1005, [0055]. Wolf provides a way to create these openings at the same time using the well-known dual damascene sequence. Specifically, it would have been obvious to a POSITA to form a photoresist (PR) mask over the interlayer insulating film 61, with the photoresist mask comprising an interconnect opening for connecting hole 62 and a dummy, non-interconnect opening for dummy connecting hole 64. Notably,

Matsunaga discloses using photoresist masks in the context of forming other interconnect structures. *See e.g.*, Ex.1005, [0003] (“...when patterning interconnections... [using] resist.”). Wolf’s processing techniques represent implementation details suitable for forming Matsunaga’s MOS transistor, including using a photoresist that protects other parts of the wafer surface during the etching process. *See* Obviousness Combination Matsunaga and Wolf.

178. Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have applied Wolf’s conventional and well known dual damascene techniques at the “re-patterned for via” step, to form Matsunaga’s MOS transistor with a dual damascene structure:



Ex.1005, FIG. 14 (a) (modified and annotated to show dual-damascene “re-patterned for via” step as applied to Matsunaga’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “re-patterned for via” annotated).

179. Thus, Matsunaga in combination with Wolf discloses a dual damascene process that includes forming over the interlayer insulating film a photoresist mask that comprises an interconnect opening and a dummy, non-interconnect opening, which renders obvious “*forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,*” as claimed.

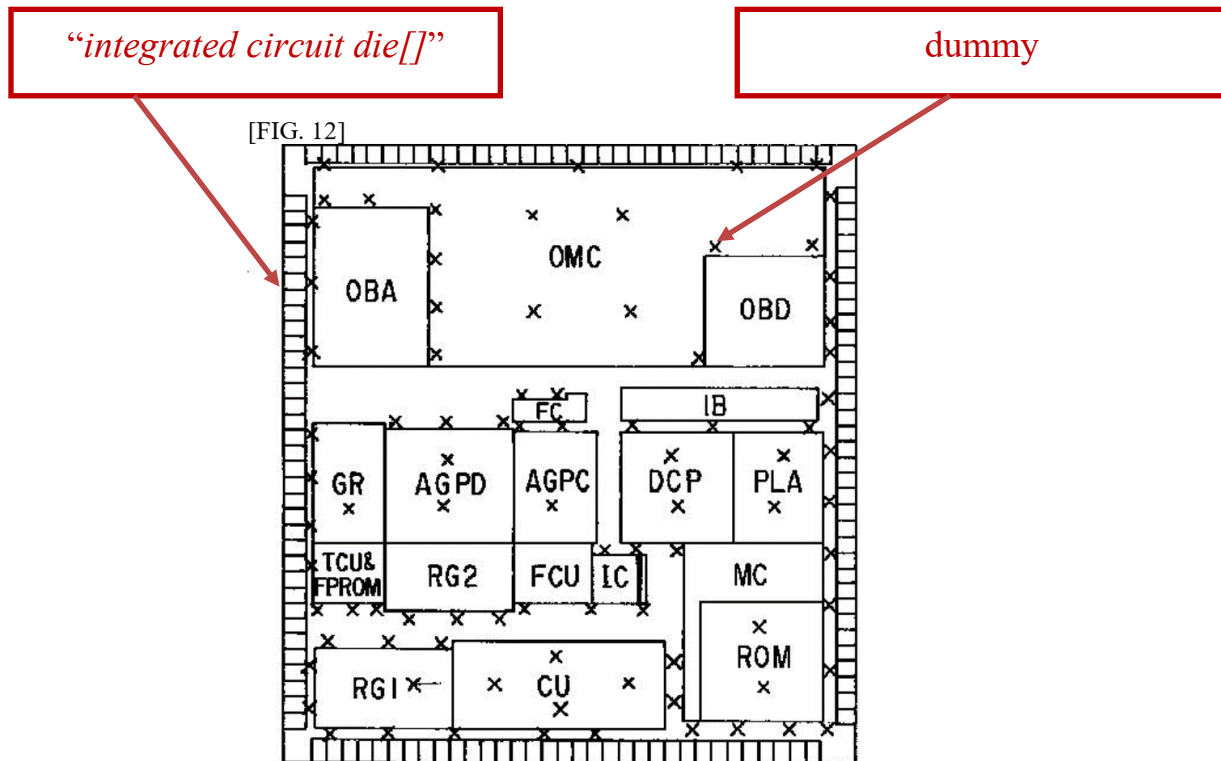
- f. [1.2.2] *wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;*

180. Matsunaga in combination with Wolf renders obvious this limitation.

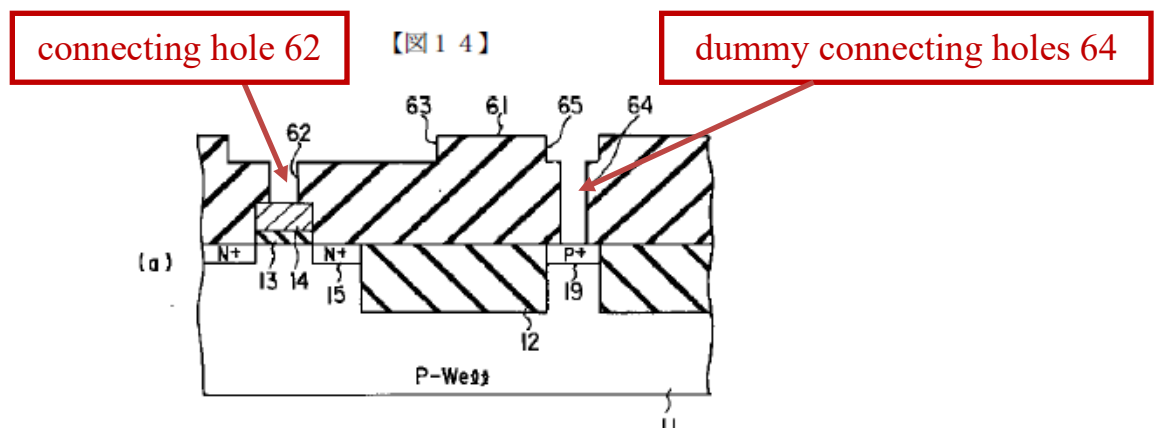
181. First, as analyzed at Ground 4 limitation [1.1.1], Matsunaga discloses microprocessor circuits (chips or dies), with each individual microprocessor circuit corresponding to “*each said integrated circuit die.*” Further, as analyzed at limitation [1.2.1], Matsunaga in combination with Wolf discloses that the photoresist mask has an interconnect opening and a dummy, non-interconnect opening, which correspond to “*said interconnect opening and said dummy, non-interconnect opening.*”

182. Second, Matsunaga in combination Wolf renders obvious that both openings “*are formed within each said integrated circuit die.*”

183. Consistent with the analysis at Ground 4 limitation [1.0], Matsunaga’s MOS transistor teachings apply when manufacturing the microprocessor circuit illustrated at Figure 12. Ex.1005, [0053], Fig. 12. In more detail, Matsunaga discloses that “a dummy interconnection is applied to a microprocessor circuit... arranged at the locations indicated by the ‘X’ marks.” Ex.1005, [0053]. As illustrated below at Figure 12, Matsunaga’s microprocessor circuit (chip or die) (“*said integrated circuit die*”) has a dummy interconnection within the die area.



Ex.1005, FIG. 12 (annotated).



Ex.1005, FIG. 14 (a) (annotated).

184. It would have been obvious to a POSITA for each microprocessor circuit (chip or die) illustrated at Matsunaga's Figure 12 that is manufactured on a

semiconductor substrate (e.g., silicon wafer), to include a MOS transistor illustrated at Figure 14. Ex.1015, 7 (describing that a chip's transistor count as of 2001 was "55,000,000."). In such instances, the microprocessor circuit (chip or die) of Figure 12 would be manufactured per the sequence analyzed at limitation [1.2.1], including forming a photoresist mask that has an interconnect opening (for connecting hole 62) and a dummy, non-interconnect opening (for dummy connecting hole 64). Moreover, it would have been obvious for the masking process to be also utilized when forming each microprocessor circuit (chip or die) on the silicon wafer, to facilitate scaling and cost benefits as analyzed at limitations [1.1.1]-[1.1.2].

185. Thus, Matsunaga in combination with Wolf discloses that the photoresist mask interconnect opening and dummy, non-interconnect opening, are both formed within each microprocessor circuit (chip or die), which renders obvious "*said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die*" as claimed.

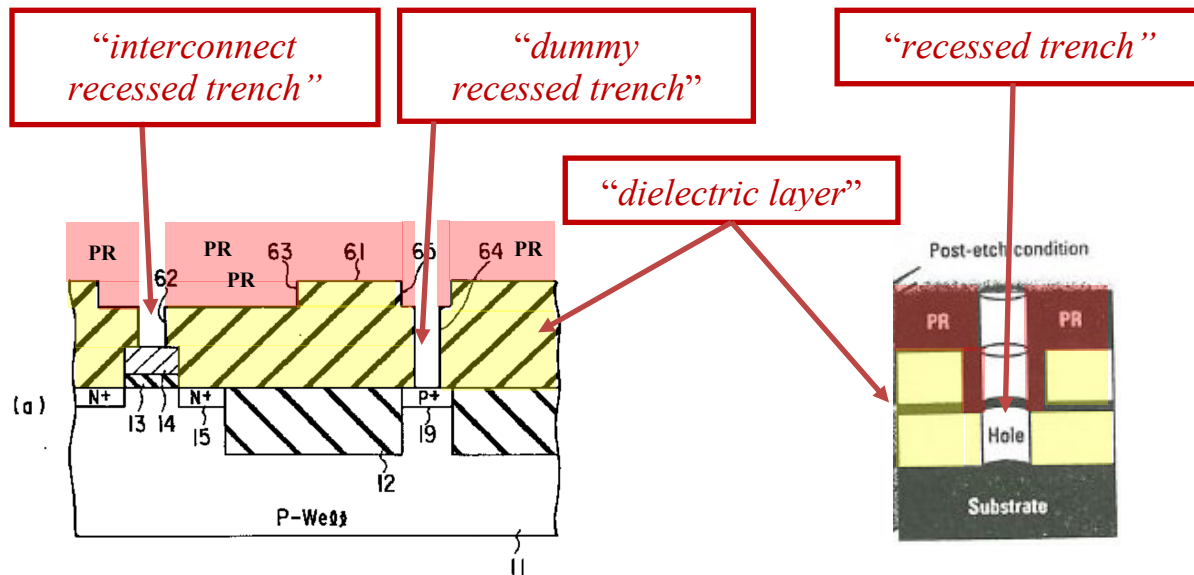
- g.** **[1.3] *performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and***

186. Matsunaga in combination with Wolf renders obvious this limitation.

187. First, as analyzed at Ground 4 limitation [1.2.1], Matsunaga in combination with Wolf discloses that a photoresist mask has an interconnect opening and a dummy, non-interconnect opening, which correspond to “*said interconnect opening and said dummy, non-interconnect openings of said mask.*”

188. Second, as analyzed at Ground 1 limitation [1.3], Matsunaga discloses performing a plasma REI process thereby simultaneously forming connecting hole 62 and dummy connecting holes 64 in the dielectric layer, which renders obvious “*performing a plasma etching process...thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer,*” as claimed.

189. Moreover, consistent with conventional manufacturing techniques, analyzed at Ground 4 limitation [1.2.1]-[1.2.2], Wolf teaches etching the interlayer dielectric layer using the openings of the photoresist mask. Ex.1004, 675-677, FIG. 15-5. Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have applied Wolf’s conventional techniques, at the “post-etch condition,” to form Matsunaga’s MOS transistor that includes connecting hole 62 (“*interconnect recessed trench*”) and a dummy connecting hole 64 (“*dummy recessed trench*”) in a dielectric layer (“*dielectric layer*”).



Ex.1005, FIG. 14 (a) (modified and annotated to show dual-damascene “post etch condition” as applied to Matsunaga’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “post etch condition” annotated).

190. Thus, Matsunaga in combination with Wolf discloses damascene processing that uses an RIE plasma etch process to simultaneously etch interlayer insulating film through the photoresist mask conductor openings and dummy conductor openings, thereby forming a connecting hole and a dummy connecting hole in the interlayer insulating film, which renders obvious *“performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer,”* as claimed.

- h. [1.4.1] *filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,***

191. As analyzed at Ground 1 limitation [1.4.1], Matsunaga discloses filling the connecting hole and the dummy connecting hole with metal to form a functional interconnecting portion and a dummy interconnecting portion, which renders obvious “*filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,*” as claimed.

- i. [1.4.2] *wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;***

192. As analyzed at Ground 1 limitation [1.4.1], Matsunaga discloses that the functional interconnecting portion is electrically connected to underlying gate electrode and that the dummy interconnecting portion is grounded to the substrate, which renders obvious “*said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate,*” as claimed.

- j. [1.5] *wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.*

193. Matsunaga in combination with Wolf renders obvious this limitation.

194. **First**, as analyzed at Ground 4 limitation [1.2.1], Matsunaga in combination with Wolf discloses a dual damascene process that uses a photoresist mask with a dummy opening, which corresponds to the “*dummy, non-interconnect opening*.” Further, as analyzed at limitation [1.3], the dummy opening in the photoresist mask is used in a RIE plasma process, which corresponds to the “*plasma etching process*.”

195. **Second**, as analyzed at Ground 1 limitation [1.5], Matsunaga discloses that because the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed simultaneously in the RIE process, the “*dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies*.”

196. Thus, Matsunaga in combination with Wolf renders obvious that the photoresist mask dummy openings and dummy connecting holes increases an in-die shunt path current flow during the RIE plasma process, thereby preventing charge

damage to MOS transistors of the microprocessor circuit dies, which renders obvious that “*said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies,*” as claimed.

4. Claim 3

k. [3.0] *The method according to claim 1 wherein said mask comprises photoresist.*

197. As analyzed at Ground 4 limitation [1.2.1], a photoresist mask is used in a dual damascene process, which renders obvious that “*said mask comprises photoresist,*” as claimed. Ex.1004, 674-677, Fig. 15-3 (disclosing “dual-damascene” sequence where a photoresist (PR) mask is used).

5. Claim 4

a. [4.0] *The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.*

198. As analyzed at Ground 4 limitations [1.2.1]-[1.3], the connecting hole is formed in a dual damascene process, which renders obvious that “*said interconnect recessed trench is a damascene opening,*” as claimed. Ex.1004, 674-677, Fig. 15-3 (disclosing “dual-damascene” opening).

6. Claim 5

- a. [5.0] *The method according to claim 1 wherein said interconnect recessed trench is a contact hole.***

199. As analyzed at Ground 4 limitations [1.3] and [1.4.1]-[1.4.2], the dual damascene structure includes a connecting hole, which renders obvious that “*said interconnect recessed trench is a contact hole,*” as claimed.

E. Ground 5: Claim 2 is Obvious over the combination of Matsunaga, Wolf, and Jaso

1. Claim 2

- a. [2.0] *The method according to claim 1 wherein an exposed surface area of said interconnect and dummy, non-interconnect openings is higher than 5% of a die area of each said integrated circuit die.***

200. As analyzed at Ground 4 claim 1 and Ground 2 claim 2, the combination of Matsunaga, Wolf, and Jaso renders obvious Claim 2.

F. Ground 6: Claim 6 is Obvious over the combination of Matsunaga, Wolf, and Appel

1. Claim 6

- a. [6.0] *The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.***

201. As analyzed at Ground 4 claim 1 and Ground 3 claim 6, the combination of Matsunaga, Wolf, and Appel renders obvious Claim 6.

G. Ground 7: Claims 1 and 3-6 are Obvious over the combination of Eriguchi, Quirk, and Wolf

202. The combination of Eriguchi, Quirk, and Wolf renders obvious Claims 1 and 3-5 as discussed below.

1. Summary of Eriguchi

203. U.S. Publication No. 2005/0006707 to Eriguchi *et al.* (Ex.1007, “Eriguchi”) generally pertains to semiconductor manufacturing. Ex.1007, [0009]. Like the ’584 patent, Eriguchi recognizes that in prior art “process for forming conductors of such a semiconductor device, plasma processing including plasma CVD or plasma etching,” “plasma charging damage” occurs. Ex.1007, [0003]-[0005]. Eriguchi explains that due to plasma charging damage, “the device characteristics are deteriorated, so that the semiconductor device is defective.” Ex.1007, [0006].

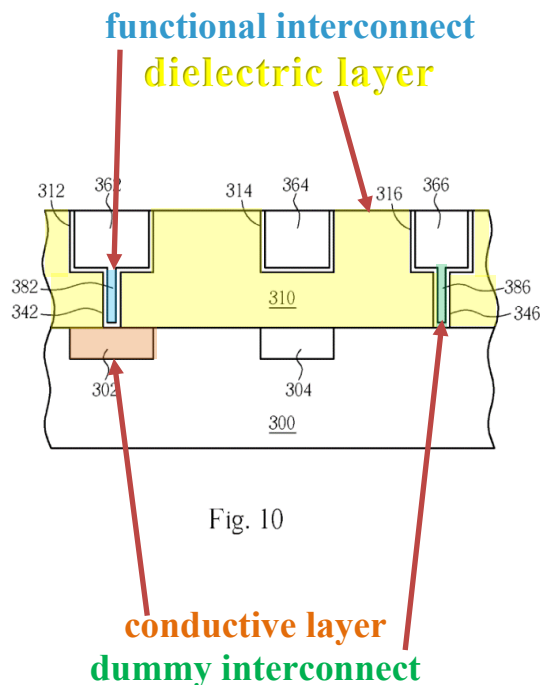
204. To “solve the above-described problem,” Eriguchi discloses “a semiconductor device that can suppress plasma charging damage in a plasma process and a method for manufacturing the same.” Ex.1007, [0037]. For example, in the context of Embodiment 1 of Figures 1 and 2, Eriguchi discloses “a method for manufacturing the semiconductor device” “in which **the occurrence of plasma**

charging damage is suppressed.” Ex.1007, [0075]-[0087]; *see also* Ex.1007, [0088]-[0095].

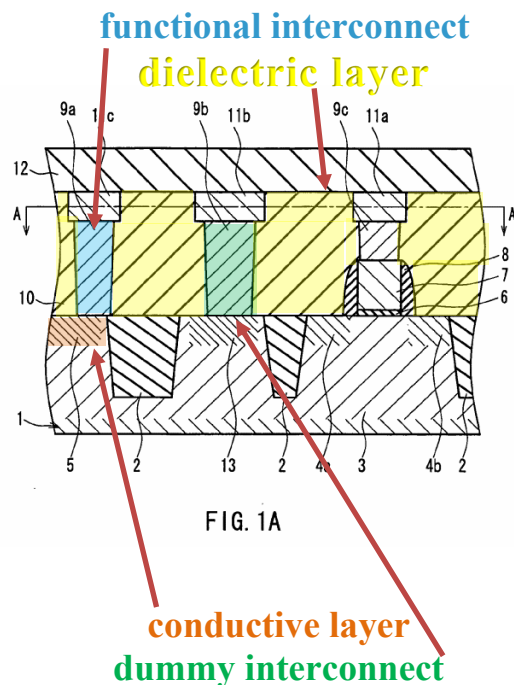
205. Eriguchi discloses that its method is applicable to MOS transistors with “a dual damascene structure.” Ex.1007, [0078], [0148]. Eriguchi’s MOS transistor includes functional conductors electrically connected to the gate electrode 7 and functional conductors electrically connected to source and drain region 5. Ex.1007, [0081]. Additionally, Eriguchi’s MOS transistor includes a “dummy conductor... and does not contribute to the function of the semiconductor device.” Ex.1007, [0082]; *see also* Ex.1007, [0040]-[0041].

206. Eriguchi’s semiconductor device has the same basic arrangement as the ’584 patent’s semiconductor device, namely: **(1)** a semiconductor substrate (Ex.1001, 6:28-30; Ex.1007, [0080]); **(2)** a dielectric layer (Ex.1001, 6:31-33; Ex.1007, [0080]); **(3)** a functional interconnect electrically connected to a conductive layer (Ex.1001, 7:3-11; Ex.1007, [0080]-[0081]); and **(4)** a dummy interconnect, which is not used in circuit operation, that is grounded to the substrate (Ex.1001, 7:3-11; Ex.1007, [0081], [0084]).

207. These elements are shown in a side-by-side comparison of the ’584 patent’s Figure 10 and Eriguchi’s Figure 1A:



Ex.1001, Fig. 10 (annotated).



Ex.1007, Fig. 1A (annotated).

208. Additionally, like the '584 patent, Eriguchi's method is applicable to forming "semiconductor integrated circuits." Ex.1007, [0002]. Thus, Eriguchi's method, which utilizes a dual damascene process like the '584 patent, forms a semiconductor device that is substantially similar to the device of the '584 patent.

2. Summary of Quirk

209. The textbook titled "Semiconductor Manufacturing Technology," by Quirk et al ("Quirk," Ex.1012) teaches well-known techniques for manufacturing devices such as ICs. Ex.1012, 1, 4-7, 436. In this context, Quirk discloses how to form a number of identical ICs on a silicon wafer. As illustrated below at Figures

1.3 and 1.6, the silicon wafer includes identical ICs (known as dies, chips, and microchips) that are separated by scribe lines.

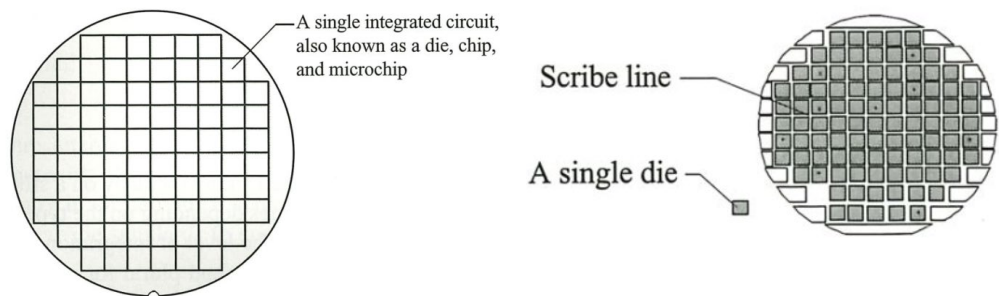


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3.

Ex.1012, FIG. 1.6 (partial).

210. According to Quirk, by implementing the manufacturing techniques, “[t]he cost of fabricating ICs drops dramatically....due to benefits from the economies of scale (more chips are produced from the same effort). Ex.1012, 6. Quirk further discloses that dual damascene processing for such ICs was well-known in the art and commonplace. Ex.1012, 326.

3. Obviousness Combination Eriguchi and Quirk

211. A POSITA would have been motivated to combine the teachings of Eriguchi and Quirk, as discussed below.

a. Analogous Art

212. Eriguchi and Quirk are analogous art to the '584 patent, because they are in the same field of endeavor of manufacturing semiconductor devices implemented as integrated circuits. Ex.1001, 3:36-54; Ex.1007, [0002], [0087]; Ex.1012, 1, 4-9. As such, a POSITA considering Eriguchi's method would have also considered Quirk, which provides additional teachings applicable to Eriguchi.

b. Combination Rationale

213. A POSITA would have been motivated to combine the teachings of Eriguchi and Quirk to produce predictable and beneficial results as discussed below.

214. Eriguchi teaches forming a MOS transistor for integrated circuits. *See* Ex.1007, [0002], [0087]. It was a well-known semiconductor manufacturing technique to form identical integrated circuits on the same silicon wafer to achieve scaling and to obtain related benefits, including cost reductions. Ex.1012, 6 ("Tens or hundreds of identical chips are fabricated simultaneously on a silicon wafer."), 8 ("The fabrication of microchips from wafers is the second stage, referred to as wafer fabrication....The completed wafers have a full complement of integrated circuits."); Ex.1015, 72 ("The polished starting wafers come into fabrication with blank surfaces and exit with the surface covered with hundreds of completed

chips.”). It was also conventional to use scribe lanes that surround and separate different integrated circuit dies on a semiconductor substrate. Ex.1004, 348-349 (“...unpatterned field areas, scribe lines, and wafer edges.”).

215. Quirk provides implementation details directly relevant when manufacturing Eriguchi’s integrated circuits. Quirk describes a well-known silicon wafer manufacturing technique that includes forming a plurality of integrated circuit dies on a silicon wafer, with each die separated and surrounded by scribe lines. Ex.1012, 6-7, 548, FIGS. 1.3, 1.6. Quirk explains that the scribe lines are used to slice the silicon wafer into individual integrated circuit dies. Ex.1012, 9. A POSITA would have understood that after individual integrated circuit dies are manufactured on a silicon wafer, it is necessary to separate them to be used as an electronic component.

216. It would have been obvious to a POSITA, in view of Quirk, to manufacture a plurality of integrated circuit dies on the same wafer substrate with Eriguchi’s method, to obtain the benefits of scaling and reducing cost. Ex.1012, 6 (“The **cost of fabricating ICs drops dramatically** if there are more chips on a wafer due to benefits from the **economies of scale** (more chips are produced from the same effort).”). Because the integrated circuits are implemented as a distinct die separated by scribe lanes, they can be cut from the wafer along the scribe lanes.

Ex.1008, 2:7-15 (“[T]he regions between die, which are ultimately sacrificed during wafer cutting into individual ICs.”); Ex.1014, 101 (“Scribe lines, saw lines, streets, and avenues. These areas are small avenues of space between the chips used to separate the chips from each other.”); Ex.1012, 9 (“[T]he front of the wafer is sliced along the scribe lines with a diamond tip saw blade to separate the die from each wafer.”), Figs. 1.3, 1.6; Ex.1015, 72 (“Scribe lines, saw lines, streets, and avenues. These areas are spaces between the chips that allow separation of the chip from the wafer.”).

217. The proposed combination is merely applying a known technique to a known device or method (e.g., Quirk’s technique of forming a number of integrated circuit dies on a wafer substrate that are separated and surrounded by scribe lanes, with Eriguchi’s method and integrated circuit) ready for improvement (e.g., scaling, reducing cost, providing an area to cut the dies from the wafer) to yield predictable results of forming individual integrated circuit chips.

218. These reasons, separately and together, would have motivated a POSITA to combine the teachings of Quirk with Eriguchi.

c. Reasonable Expectation of Success

219. The results would have been predictable and there would have been a reasonable expectation of success in the combination because Eriguchi and Quirk

address the same technology, as analyzed above in the analogous art section.

Modifying Eriguchi's method and integrated circuit to be implemented according to Quirk's conventional teachings would have been well within the skill in the art as detailed in various textbooks. *See* Ex.1004, 348-349; Ex.1012, *generally*, Fig. 1.3; Ex.1014, 101; Ex.1015, 72; Ex.1018, ¶¶99-143.

220. Lastly, I note that the proposed combinations rely on the teachings of the references—not on physical incorporation of the elements.

4. Obviousness Combination Eriguchi and Wolf

221. Eriguchi teaches that its method is applicable to MOS transistors that are formed by techniques including a dual damascene process. Ex.1007, [0011], [0078]-[0082], [0148]. Wolf provides implementation details regarding such dual damascene methods, thereby allowing for the manufacturing of Eriguchi's MOS transistors. Ex.1004, 674-677, Fig. 15-3. Accordingly, the proposed combination is simply applying the teachings of a textbook reference (Wolf) to another reference (Eriguchi) that is ready for and expressly calls for those teachings, with a reasonable expectation of success. Ex.1003, ¶242. For this and for the same reasons discussed above in Ground 4, regarding the combination of Wolf and Matsunaga, it would have been obvious to apply Wolf's fundamental semiconductor manufacturing details (which represent common background knowledge to a

POSITA and that are omitted from many references), when manufacturing Eriguchi's semiconductor device.

5. Claim 1

- a. [1.0] *A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:***

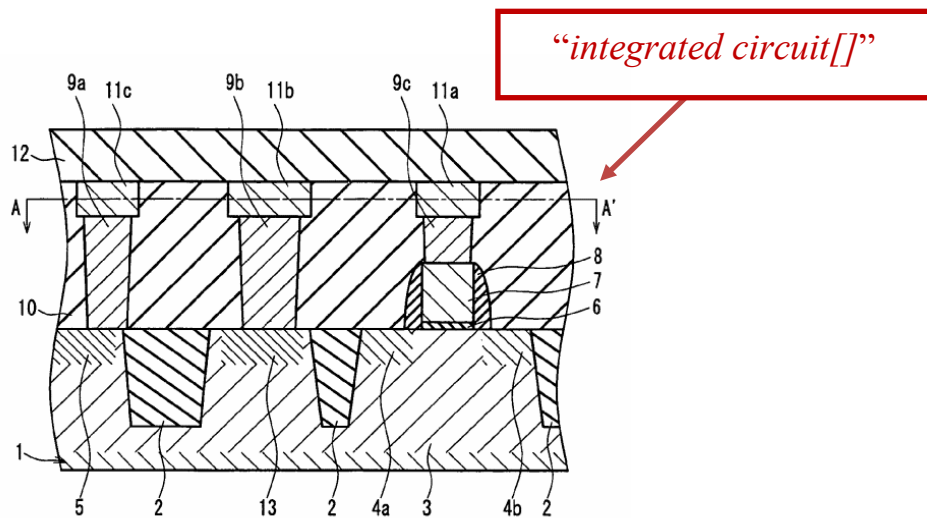
222. To the extent limiting, Eriguchi alone and in combination with Quirk renders obvious the preamble.

223. First, Eriguchi teaches a “*method for reducing charging damage...during semiconductor manufacturing.*” Eriguchi recognizes that in the prior art “process for forming conductors of such a semiconductor device, plasma processing including plasma CVD or plasma etching,” causes “plasma charging damage.” Ex.1007, [0003]-[0005]. Eriguchi explains that due to plasma charging damage, “the device characteristics are deteriorated, so that the semiconductor device is defective.” Ex.1007, [0006].

224. To “solve the above-described problem,” Eriguchi discloses “a semiconductor device that can suppress plasma charging damage in a plasma process and a method for manufacturing the same.” Ex.1007, [0037]. In the context of Embodiment 1 of Figures 1 and 2, Eriguchi discloses “**a method for manufacturing the semiconductor device**” “**in which the occurrence of plasma**

charging damage is suppressed.” Ex.1007, [0075]-[0087]; *see also* Ex.1007, [0088]-[0095].

225. Second, Eriguchi’s method is applicable to “*integrated circuits*” because it is used to manufacture a “semiconductor device constituted by **semiconductor integrated circuits**” that includes “**an n-channel MOS transistor.**” Ex.1007, [0002], [0078]. Eriguchi’s Figure 1A is reproduced below, illustrating an MOS transistor:

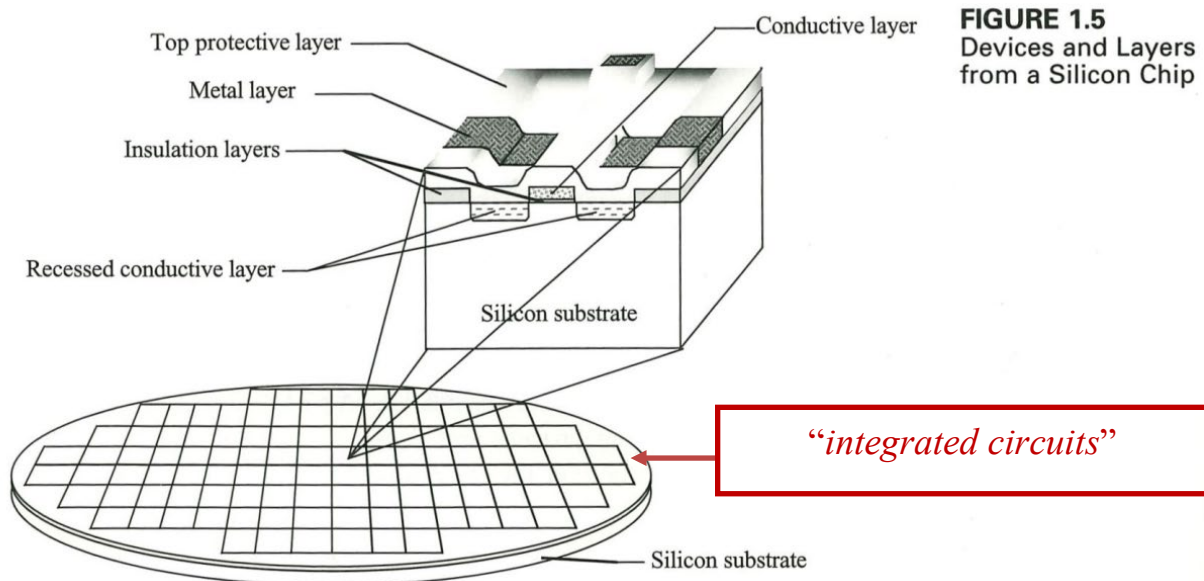


Ex.1007, FIG. 1A (annotated).

226. Notably, the ’584 patent’s exemplary integrated circuit similarly corresponds to a “MOS transistor.” Ex.1001, 4:52-5:11; *see also* Ex.1001, 6:11-15 (“[T]he above exemplary embodiments reveal the present invention method of

reducing charging damage to integrated circuits during LDD implant process of high-voltage MOS devices.”).

227. Third, to the extent argued that Eriguchi’s teachings are insufficient to renders obvious that the method is applied to “*integrated circuits*,” the further combination with Quirk renders such obvious. Quirk discloses forming a plurality of identical integrated circuit “**ICs**” “die” “chips” on the same silicon wafer. Ex.1012, 6-8. Quirk’s Figure 1.5 is reproduced below, illustrating a plurality of integrated circuit dies on a wafer substrate:



Ex.1012, FIG. 1.5 (annotated).

228. Consistent with conventional well-known textbook techniques, it would have been obvious to a POSITA to manufacture a plurality of Eriguchi's integrated circuits on the same silicon wafer/substrate to obtain the benefits of scaling and reduce cost. In the proposed combination of Eriguchi and Quirk, a plurality of integrated circuits on the same silicon substrate correspond to "*integrated circuits*" as claimed. *See* Ex.1012, 6, 8; Ex.1015, 72; Ex.1018, ¶¶122-143; Obviousness Combination Eriguchi and Quirk.

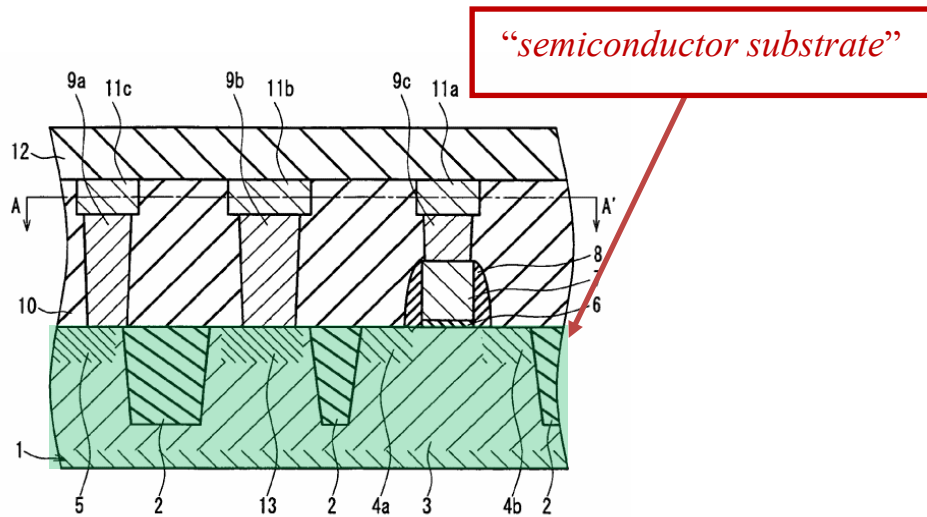
229. Thus, Eriguchi alone and in combination with Quirk discloses a method of suppressing plasma charging damage to integrated circuits during semiconductor manufacturing, which renders obvious "[a]method for reducing charging damage to integrated circuits during semiconductor manufacturing," as recited in the preamble.

b. [1.1.1] *providing a semiconductor substrate comprising thereon a number of integrated circuit dies,*

230. Eriguchi in combination with Quirk renders obvious this limitation.

231. First, Eriguchi discloses "*providing a semiconductor substrate.*" For example, in the context of Figure1A (reproduced below), Eriguchi teaches that "the semiconductor device of Embodiment 1 includes an n-type silicon substrate 1" and

that the “an n-channel MOS transistor is formed with a p-well 3 formed in the internal portion of the n-type silicon substrate 1.” Ex.1007, [0077]-[0078];



Ex.1007, FIG. 1A (annotated).

232. A POSITA would have understood that Eriguchi’s “silicon substrate” is a semiconductor. Ex.1012, 4 (“Nowadays, greater than 85% of all microchips are made from silicon semiconductor material.”). The semiconductor substrate in the ’584 patent is also silicon. Ex.1001, 7:19-22 (“...semiconductor substrate 400 such as a silicon substrate...”). Accordingly, Eriguchi’s silicon substrate teaches a “*semiconductor substrate*,” as claimed.

233. Second, consistent with the analysis at the preamble [1.0], Eriguchi and Quirk disclose integrated circuits that include MOS transistors, which renders obvious “*integrated circuits*.” Further, Quirk’s Figures 1.3 and 1.6 reproduced

below, illustrates a plurality of circuit dies (“*number of integrated circuit dies*”) on a wafer substrate (“*semiconductor substrate*”). Ex.1012, 6 (“**The chip is also referred to as a die.**”), 8 (“The fabrication of **microchips...integrated circuits.**”).

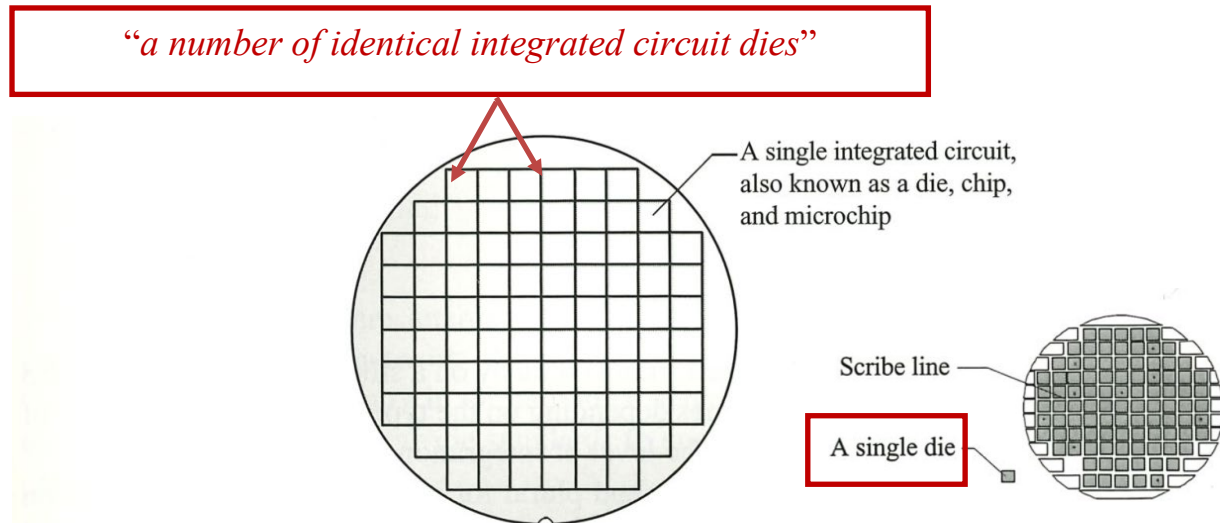


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3 (annotated).

Ex.1012, FIG. 1.6 (partial, annotated).

234. It would have been obvious to a POSITA to manufacture a plurality of integrated circuit dies (each die including at least a MOS transistor) on the same semiconductor substrate (e.g., wafer substrate), per the combination of Eriguchi and Quirk, to obtain the benefits of scaling and reducing cost. Ex.1012, 6, 8; Ex.1015, 72; Ex.1018, ¶¶122-143. Because the integrated circuits are each a separate die, they can be separated along the scribe lanes as taught by Quirk. Ex.1008, 2:7-15, 3:63-67; Obviousness Combination Eriguchi and Quirk.

235. Thus, Eriguchi in combination with Quirk discloses a silicon substrate (e.g., a wafer substrate) that includes a plurality of integrated circuit dies (each die including a MOS transistor), which renders obvious “*providing a semiconductor substrate comprising thereon a number of integrated circuit dies,*” as claimed.

c. [1.1.2] *said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*

236. Eriguchi in combination with Quirk renders obvious this limitation.

237. First, as analyzed at limitation [1.1.1] Eriguchi in combination with Quirk discloses that a silicon substrate (e.g., wafer substrate) includes a plurality of integrated circuit dies, which correspond to the “*integrated circuit dies.*”

238. Second, it would have been obvious to a POSITA, in implementing the combination of Eriguchi and Quirk, for the integrated circuit dies to be “*separated from each other by scribe lanes surrounding each said integrated circuit die.*” As shown below in Quirk’s Figures 1.3 and 1.6, each integrated circuit “die, chip, and microchip” is surrounded and separated by “**scribe lines,**” which would have been understood by a POSITA to correspond to a “*scribe lanes.*”

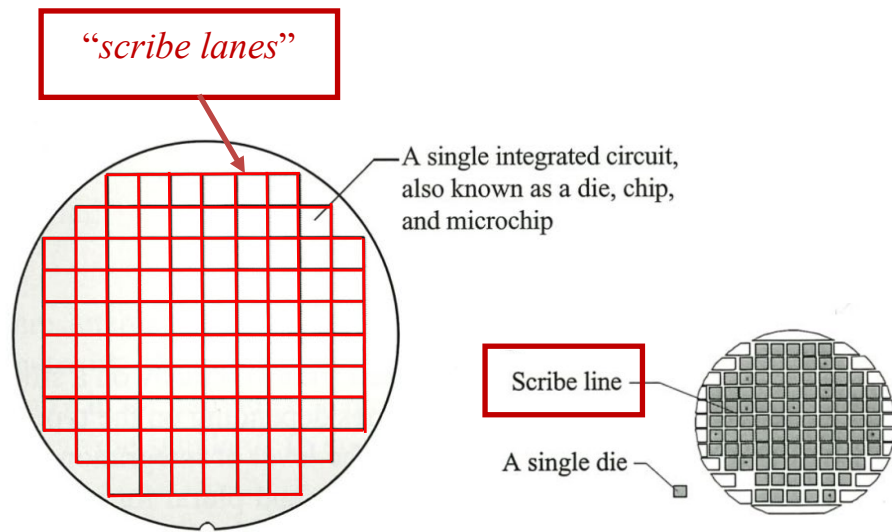


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3 (annotated).

Ex.1012, FIG. 1.6 (partial, annotated).

239. Accordingly, it would have been obvious to a POSITA for each of Eriguchi's integrated circuit (chip or die) to be separated from each other by scribe lanes that surround each integrated circuit (chip or die). The scribe lanes would beneficially serve to isolate different integrated circuit dies from each other and would also serve as the area for cutting each integrated circuit die from the wafer. *See* Ex.1004, 348-349; Ex.1008, 2:7-15, 3:63-66; Ex.1012, 9, 549, 575, Figure 20.5; Ex.1014, 101; Ex.1015, 72. Additionally, the scribe lanes enable the use of "scribe line monitors" for testing purposes. Ex.1012, 548-549; *see also* Obviousness Combination Eriguchi and Quirk.

240. Thus, Eriguchi in combination with Quirk discloses that each integrated circuit die is separated and surrounded by scribe lanes, which renders obvious “*said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,*” as claimed.

d. [1.1.3] *wherein said semiconductor substrate comprises thereon a dielectric layer;*

241. Eriguchi in combination with Quirk renders obvious this limitation.

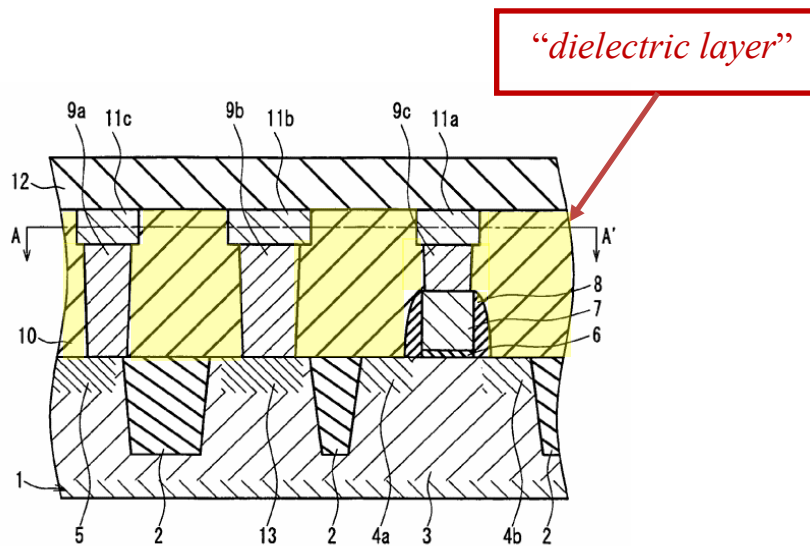
242. **First**, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses a semiconductor substrate (e.g., wafer substrate), which corresponds to the “*semiconductor substrate.*”

243. **Second**, Eriguchi discloses “*a dielectric layer.*” In the context of Figure 1A, discloses that “an underlying interlayer insulating film 10...[is formed] on the silicon substrate 1” and that the “underlying interlayer insulating film 10...[comprises] silicon oxide films or silicon nitride films.” Ex.1007, [0080]. A POSITA would have understood that silicon oxide and silicon nitride are dielectrics. Ex.1014, 381 (“CVD is the favored method of depositing films that will function in the device or circuit as insulators or dielectrics. The two films in widespread use are silicon dioxide and silicon nitride.”), 382 (“...deposited silicon oxide layers are used as interdielectric layers...”). Additionally, a POSITA would

have understood that an electrical insulator is a dielectric, as these terms are used in the art. Ex.1014, 6(“...a dielectric (electrical insulator).”), 141 (“When dielectrics are used in electrical circuits or devices they are referred to as insulators.”).

Accordingly, Eriguchi’s underlying interlayer insulating film 10 corresponds to the claimed “*dielectric layer*.”

244. As illustrated below at Figure 1A, Eriguchi’s interlayer insulating film 10 is formed on the semiconductor substrate 1 and serves to insulate various conducting features from each other:



Ex.1007, FIG. 1A (annotated).

245. Thus, Eriguchi in combination with Quirk discloses forming a dielectric interlayer insulating film (e.g., silicon oxide or silicon nitride) on a silicon

substrate (e.g., wafer substrate), which renders obvious that “*said semiconductor substrate comprises thereon a dielectric layer,*” as claimed.

- e. [1.2.1] *forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,*

246. Eriguchi in combination with Wolf renders obvious this limitation.

247. First, Eriguchi discloses that its method is applicable to MOS transistors with “a **dual damascene** structure.” Ex.1007, [0078], [0148]. Eriguchi’s “conductors 11*a* to 11*c* are... **simultaneously formed by the damascene method and embedded in the underlying interlayer insulating film 10.**” Ex.1007, [0081].

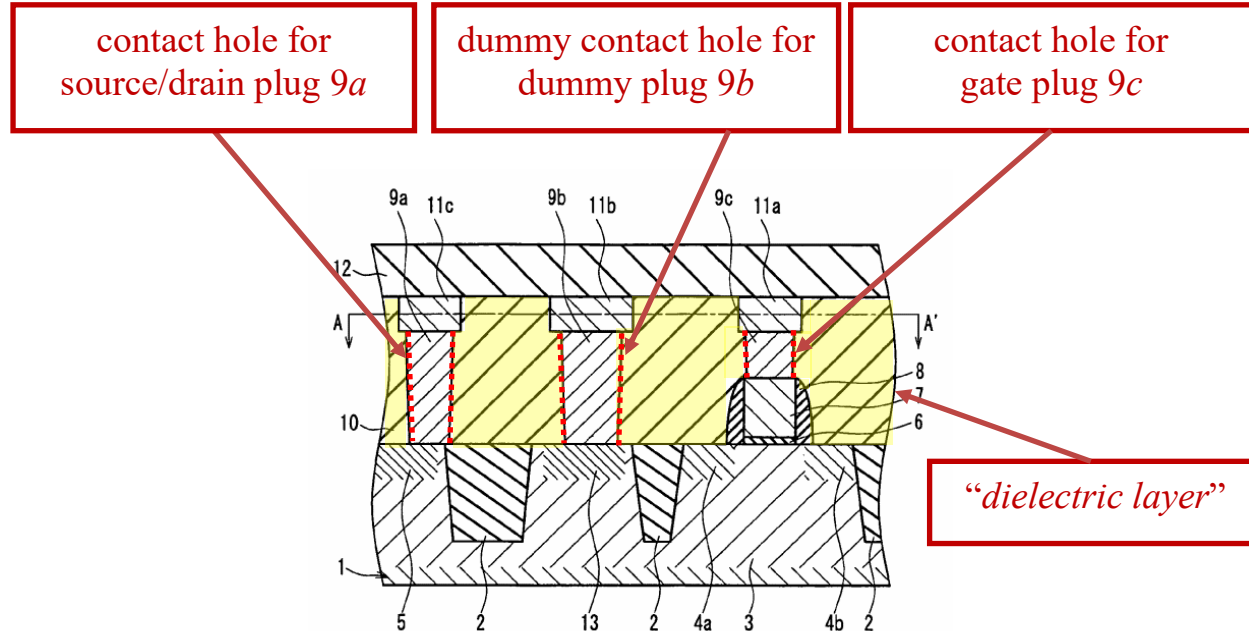
Eriguchi’s conductors 11*a* and 11*c* are functional, since “conductor 11*a* is a conductor for gate electrode connection that is connected to the gate electrode 7 via a W (tungsten) plug 9*c*” and “conductor 11*c* is a conductor for source and drain connection that is connected to the n⁺ region 5 via a W (tungsten) plug 9*a*.”

Ex.1007, [0081]. Additionally, Eriguchi’s “conductor 11*b* is a **dummy conductor... and does not contribute to the function of the semiconductor device.**” Ex.1007, [0082]; *see also* Ex.1007, [0040]-[0041].

248. Eriguchi further explains that the dual damascene method includes forming “contact holes” in the underlying interlayer insulating film 10 for plugs 9*a* to 9*c*. Ex.1007, [0086] (“Also in Embodiment 1, the W plugs 9*a* to 9*c* are formed

by filling contact holes formed in the underlying interlayer insulating film 10 with tungsten, as the W plugs.”), [0090] (“Then, in the underlying interlayer insulating film 10, **a contact hole** that exposes the n⁺ region 5 at the bottom face, **a contact hole** that exposes the active region 13 at the bottom face, and **a contact hole** that exposes the gate electrode 7 at the bottom face are formed. Furthermore, **these contact holes are filled with tungsten to form the W plugs 9a to 9c.**”).

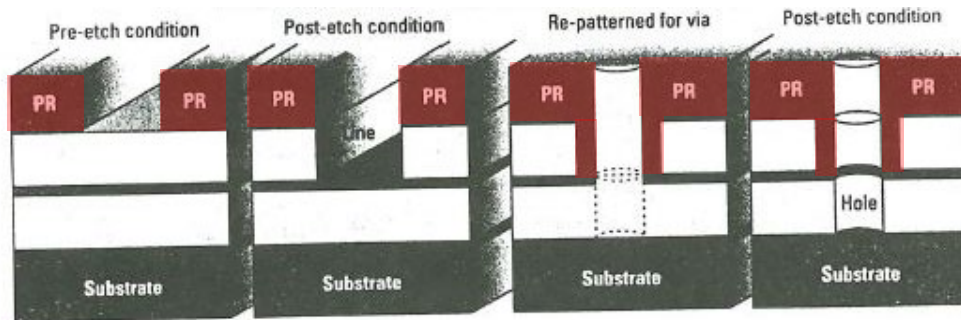
249. Figure 1A is reproduced below, illustrating the resulting “**dual damascene** structure” with the contact holes with functional plugs 9a and 9c and dummy plug 9b:



Ex.1007, FIG. 1A (annotated).

250. While Eriguchi omits the patterning process for forming the dual damascene structure, such would have been well-known and conventional in the art. It would have been obvious to POSITA to form a photoresist mask over interlayer insulating film 10, with the photoresist mask having an opening to form contact holes for functional plugs 9a and 9c and an opening to form a dummy contact hole for dummy plug 9b.

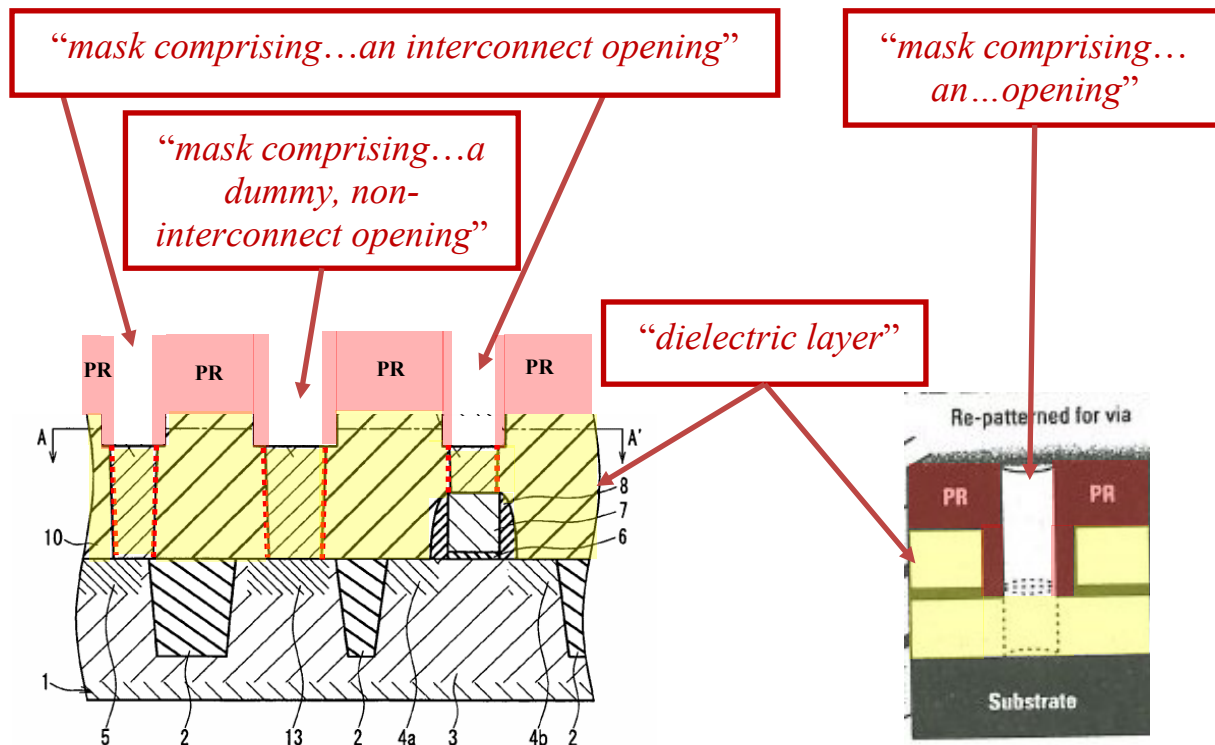
251. For example, Wolf teaches processing techniques that were known in the art and directly applicable when manufacturing Eriguchi's MOS transistor, which has "a dual damascene structure." Ex.1007, [0078]; Ex.1004, 674-676, Fig. 15-3. In more detail, Wolf discloses details regarding how to implement a "dual-damascene" technique where a photoresist (PR) mask is used to etch a trench in an underlying interlayer dielectric with an embedded etch-stop layer. Ex.1004, 677. Then, a second a photoresist (PR) mask is formed with openings that are aligned with the trench that was etched previously. Ex.1004, 677. "The resist protects the other parts of the wafer surface (including the etched regions of the trenches) so that the via can be etched without further etching the dielectric in the trench." Ex.1004, 677.



Ex. 1004, Fig. 15-5 (annotated).

252. It would have been obvious to a POSITA, when manufacturing Eriguchi's MOS transistor having "a dual damascene structure," to follow or adapt Wolf's dual damascene teachings to form the contact holes for functional plugs 9a and 9c and dummy plug 9b (which are formed "simultaneously by the damascene method", Ex.1007, [0040], [0091]) to use a dual damascene sequence per Wolf. Such a combination would involve creating Eriguchi's contact holes by forming a photoresist (PR) mask over the interlayer insulating film 10, with the photoresist mask comprising an interconnect opening for all three contact holes. Indeed, Eriguchi discloses using a mask having mask data in the context of forming a multilayer interconnect wiring structure comprising conductors, dummy conductors, and an interlayer insulating film. *See e.g.*, Ex.1007, [0145] ("...mask data for forming the conductor...").

253. Provided below is a modified Figure 1A of Eriguchi, illustrating how a POSITA would have applied conventional and well-known dual damascene techniques (i.e., trench-first dual-damascene), at the “re-patterned for via” step, to form Eriguchi’s MOS transistor with a dual damascene structure:



Ex.1007, FIG. 1A (modified and annotated to show dual-damascene “re-patterned for via” step as applied to Eriguchi’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “re-patterned for via” annotated).

254. Thus, Eriguchi in combination with Wolf discloses a dual damascene process that includes forming over the interlayer insulating film a photoresist mask that comprises an interconnect opening (for contact holes to form functional plugs

9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), which renders obvious “*forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,*” as claimed.

f. [1.2.2] *wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;*

255. Eriguchi in combination with Quirk and Wolf renders obvious this limitation.

256. First, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses integrated circuit dies, with an individual integrated circuit die (including a MOS transistor) corresponding to “*said integrated circuit die.*” Further, as analyzed at Ground 7 limitation [1.2.1], Eriguchi in combination with Wolf discloses that the photoresist mask has an interconnect opening (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), which correspond to “*said interconnect opening and said dummy, non-interconnect opening.*”

257. Second, Eriguchi in combination with Quirk and Wolf renders obvious that both mask openings “*are formed within each said integrated circuit die.*”

Specifically, it would have been obvious to a POSITA for each integrated circuit die, represented by the combination of Eriguchi and Quirk, to include a MOS transistor illustrated at Eriguchi's Figure 1A. *See* Ex.1015, 7 (describing that a chip's transistor count as of 2001 was "55,000,000."); Ex.1018, ¶¶122-143. In such instances, Eriguchi's MOS transistor would be manufactured per Wolf's sequence analyzed at Ground 7 limitation [1.2.1], including forming a photoresist mask that has interconnect openings (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b). Moreover, it would have been obvious for the masking process to be also utilized when forming each integrated circuit die on the silicon wafer, to facilitate scaling and cost benefits as analyzed at Ground 7 limitations [1.1]-[1.1.2].

258. Thus, Eriguchi in combination with Quirk and Wolf discloses that the photoresist mask interconnect opening (for contact holes to form functional plugs 9a and 9c) and dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), are both formed within each integrated circuit die, which renders obvious "*said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die*" as claimed.

- g. ***[1.3] performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and***

259. Eriguchi in combination with Wolf renders obvious this limitation.

260. First, as analyzed at limitation [1.2.1], Eriguchi in combination with Wolf discloses that a photoresist mask has an interconnect opening (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), which correspond “*said interconnect opening and said dummy, non-interconnect openings of said mask.*”

261. Second, during prosecution of the '584 patent, Applicant contended that the plasma etching step requires “concurrently” etching of the “dummy, non-interconnect structures” and “the interconnect structures.” Ex.1002, 31-32. The claims of the '584 patent, however, do not require this “concurrently” etching step. Nevertheless, to the extent that this is a claim requirement, Eriguchi teaches it.

262. Eriguchi discloses that the “dummy conductor insulated from the gate electrode and the active region by the first insulating layer is formed in a position adjacent to the dummy conductor simultaneously with the conductor for a gate electrode.” Ex.1007, [0070]. In the claims, Eriguchi recites that “the first dummy conductor and the first conductor are formed simultaneously by a damascene

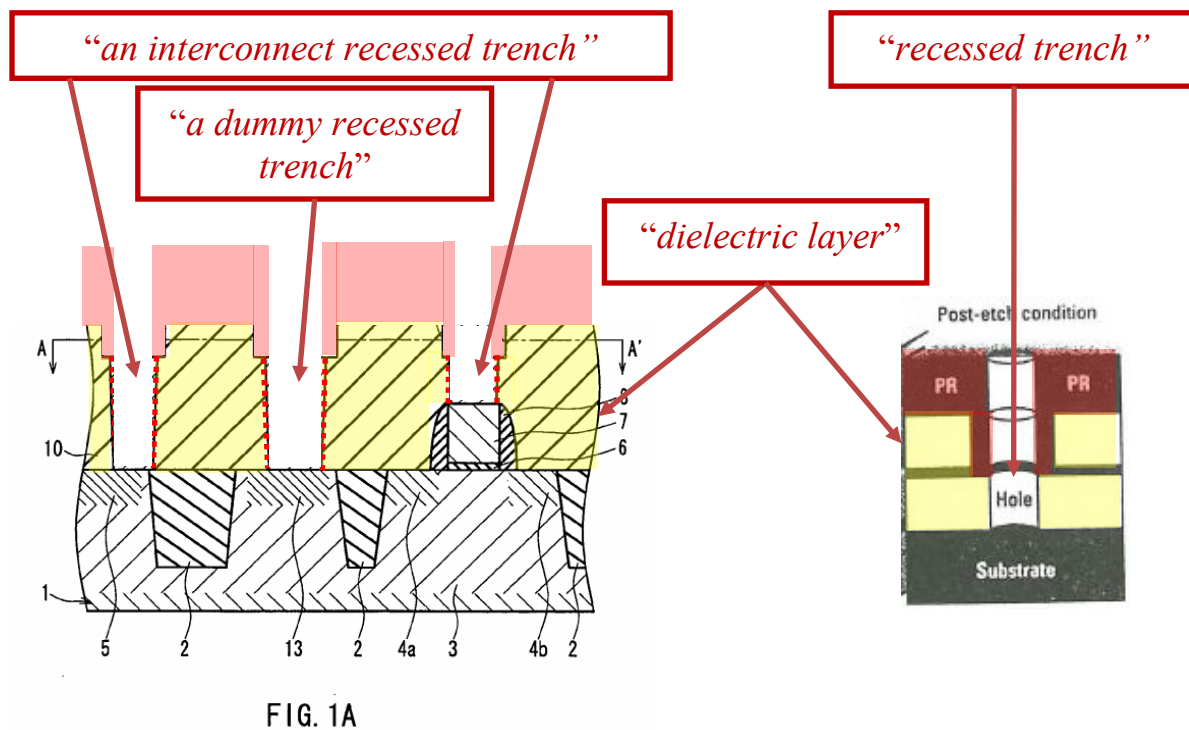
method and embedded in the lowermost insulating layer” and that “the second conductor and the second dummy conductor that are provided in a same insulating layer are formed simultaneously by a damascene method and embedded in the insulating layer in which these conductors are provided.” Ex.1007, claim 21.

Eriguchi also discloses that “a process for forming conductors of such a semiconductor device, plasma processing including plasma CVD or **plasma etching** has been increasingly utilized.” Ex.1007, [0003]; *see also* Ex.1007, [0149] (“...the conductors can be formed by **etching**.”). It would have been obvious to a POSITA that simultaneously forming the MOS transistor functional conductors and dummy conductor includes performing plasma etching.

263. Moreover, consistent with conventional manufacturing techniques, analyzed at limitation [1.2.1], Wolf teaches that it was known in the art to etch the interlayer dielectric layer using the openings of the photoresist mask. Ex.1004, 677 (“The resist protects the other parts of the wafer surface (including the **etched** regions of the trenches) so that the vias can be etched without further etching the dielectric in the trenches.”); *see also* Ex.1004, 675 (“Vias are defined by **PR #2** and then etched, using PR #2 to protect other regions of the IMD from etching.”).

264. Provided below is a modified Figure 1A of Eriguchi, illustrating how a POSITA would have applied Wolf’s conventional and well known techniques, at

the “post-etch condition,” to form Eriguchi’s MOS transistor that includes contact holes (“*interconnect recessed trench*”) for functional plugs and a dummy contact hole (“*dummy recessed trench*”) for dummy plug in dielectric layer 10 (“*dielectric layer*”).



Ex.1007, FIG. 1A (modified and annotated to show dual-damascene “post etch condition” as applied to Eriguchi’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “post etch condition” annotated).

265. Thus, Eriguchi in combination with Wolf discloses damascene processing that uses a plasma process to simultaneously etch interlayer insulating film through the photoresist mask conductor openings and dummy conductor

openings, thereby forming contact holes for functional plugs and a dummy contact hole for dummy plug in the interlayer insulating film, which renders obvious “performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer,” as claimed.

- h. [1.4.1] *filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,*

266. Eriguchi renders obvious this limitation.

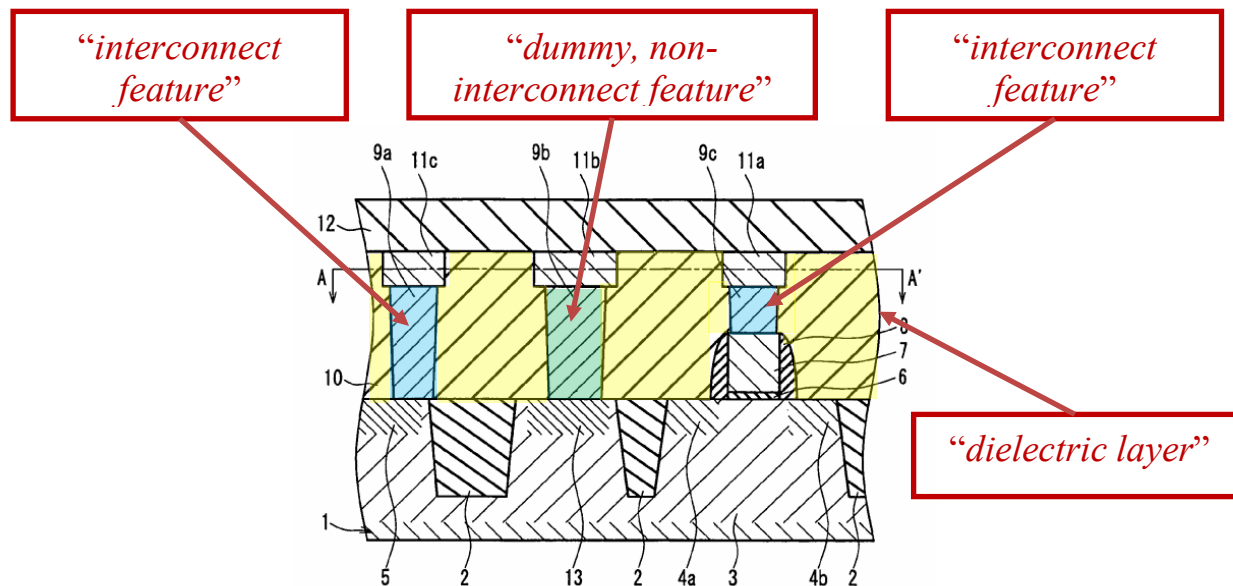
267. First, as analyzed at limitations [1.3], Eriguchi renders obvious forming contact holes (for functional plugs 9a and 9c) each of which corresponds to “said interconnect recessed trench” and forming a dummy contact hole (for dummy plug 9b) which corresponds to “said dummy recessed trench.”

268. Second, Eriguchi discloses that the holes are “fill[ed]” with “conductive materials to form an interconnect feature and a dummy, non-interconnect feature.” For example, in the context of Figures 1A and 2, Eriguchi explains that “**these contact holes are filled with tungsten to form the W plugs 9a to 9c.**” Ex.1007, [0090]; *see also* Ex.1007, claim 22 (“...the first dummy

conductor, the first conductor, the second dummy conductor and the second conductor are formed of a same **metal material.**”) A POSITA would have understood that filling the contact holes discloses “*filling*” and that tungsten (a metal material) plugs in the contact and dummy contact holes correspond to “*conductive materials.*”

269. Eriguchi’s dummy plug 9*b* is “*non-interconnect*” as that term is used in the ’584 patent since it “**does not contribute to the function of the semiconductor device**” and grounded to the substrate. Ex.1007, [0082]; limitation [1.4.2] (*non-interconnect feature is...grounded to said semiconductor substrate*”).

270. As illustrated below at Figure 1A, reproduced below, after the metal deposition process, the MOS transistor’s contact hole has a buried functional plugs 9*a* and 9*c* and the dummy contact hole has a dummy plug 9*b*:



Ex.1007, FIG. 1A (annotated).

271. Thus, Eriguchi discloses filling the contact holes with metal to form a functional plugs 9a and 9c and a dummy, nonfunctional plug 9b, which renders obvious *“filling said interconnect recessed trench and said dummy recessed trench with conductive materials to form an interconnect feature and a dummy, non-interconnect feature,”* as claimed.

- i. [1.4.2] *wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;*

272. Eriguchi renders obvious this limitation.

273. First, as analyzed at limitation [1.4.1], Eriguchi discloses a functional plugs 9a and 9c, which separately and together correspond to *“said interconnect*

feature,” and a dummy nonfunctional plug 9b, which corresponds to “*said dummy, non-interconnect feature.*”

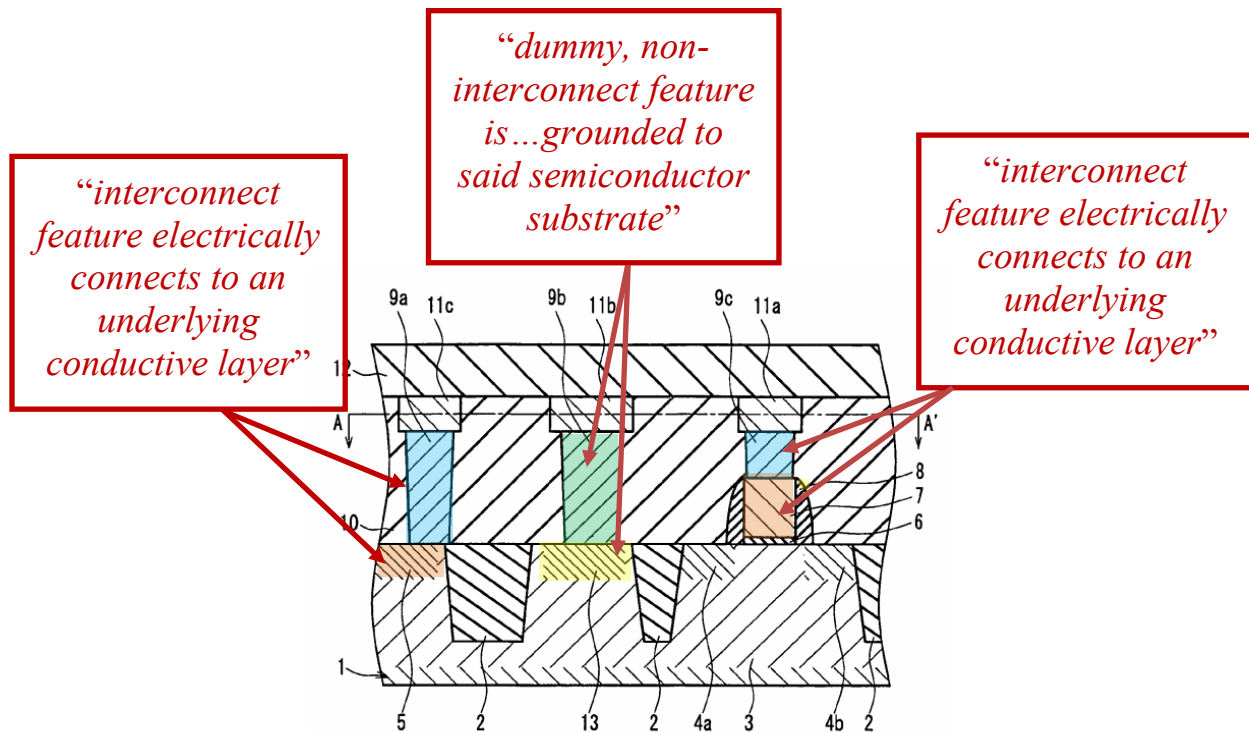
274. Second, as already noted above, in Eriguchi’s Figure 1A, “**the gate electrode 7 [is connected] via a W (tungsten) plug 9c**” and the “**source and drain...n+ region 5 [is connected] via a W (tungsten) plug 9a.**” Ex.1007, [0081].

Additionally, Eriguchi discloses that “dummy conductor... does not contribute to the function of the semiconductor device” and is “connected to...**active region 13 via the W plug 9b.**” Ex.1007, [0082], [0084]; *see also* Ex.1007, [0040]-[0041].

Eriguchi further explains that “active region (n+ region) 13...does not serve as either a source region or a drain region.” Ex.1007, [0085]. A POSITA would have understood that both gate electrode 7 and source/drain region 5 correspond to a “*conductive layer*” because these layers are used in circuit operation to switch the MOS transistor. Also, a POSITA would have understood that n+ region 13 is a n-type doped region that serves to “*ground[]*” to the substrate 1 since n+ region 13 is in the substrate 1.

275. As illustrated at Figure 1A, reproduced below, Eriguchi’s functional plug 9a is electrically connected to underlying source/drain region 5, functional plug 9c is electrically connected to underlying gate electrode 7, and dummy

nonfunctional plug 9b is grounded to the substrate by being connected to the n⁺ region 13 in the substrate:



Ex.1007, FIG. 1A (annotated).

276. Thus, Eriguchi discloses that functional plugs 9a and 9c are electrically connected to underlying conductive layers and that the dummy nonfunctional plug 9b is grounded to the substrate via the active region 13, which renders obvious “said interconnect feature electrically connects to an underlying conductive layer,

while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate,” as claimed.

- j. **[1.5] *wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.***

277. Eriguchi in combination with Quirk renders obvious this limitation.

278. First, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses a silicon substrate 1 implemented as a wafer that includes a number of integrated circuit dies (each die including a MOS transistor), which renders obvious “*said integrated circuit dies.*” Further, as analyzed at Ground 7 limitation [1.2.1], Eriguchi in combination with Wolf renders obvious using a photoresist mask with a dummy opening (for dummy nonfunctional plug 9b), which corresponds to the “*dummy, non-interconnect opening.*” Furthermore, as analyzed at Ground 7 limitation [1.3], Eriguchi in combination with Wolf renders obvious that the dummy opening in the photoresist mask is used in a plasma etching process, which corresponds to the “*plasma etching process.*”

279. Second, Eriguchi recognizes that due to plasma processing charging damage, “device characteristics are deteriorated, so that the semiconductor device is defective.” Ex.1007, [0006]. To address this concern, Eriguchi seeks to “**suppress**

plasma charging damage in a plasma process,” including during “plasma etching.” Ex.1007, [0003]-[0004], [0037]. Specifically, Eriguchi’s method “**in which the occurrence of plasma charging damage is suppressed**” includes a process that “**simultaneously**” forms functional and dummy conductors. Ex.1007, [0070], 0075]-[0087], claim 21; *see also* Ex.1007, [0088]-[0095]. Thus, “the deterioration of the device characteristics due to breakdown of the gate insulating film 6 can be suppressed.” Ex.1007, [0094].

280. A POSITA would have understood that because the process simultaneously forms the functional and dummy conductors, during the plasma etching process (see limitation [1.3]) the dummy contact hole provides a shunt electrical path that enables the current to flow to an alternative point, i.e., to the substrate 1 via the n⁺ region 13. Ex.1008, 1:66-2:6; *see also* Ex.1005, [0019] (“... prevent charging damage in the plasma processes, such as RIE, or the like, when processing the connecting holes or interconnection grooves, making it possible to prevent damage to the gate insulating films.”). Because Eriguchi’s dummy contact hole (for dummy nonfunctional plug 9*b*) as defined by the mask dummy opening, supplies electric charges to the substrate 1 via the n⁺ region 13 during the plasma etching process, Eriguchi’s renders obvious that the dummy, non-interconnect

opening “*increases an in-die shunt path current flow during said plasma etching process.*”

281. Moreover, because, as analyzed above, the MOS transistors are within the integrated circuit die, suppressing charge damage to the MOS transistor, e.g., gate insulating film 6, “*thereby reduc[es] charge damage to said integrated circuit dies,*” as claimed.

282. Thus, Eriguchi in combination with Quirk discloses that the photoresist mask dummy openings and dummy contact hole (for dummy nonfunctional plug 9b) increases an in-die shunt path current flow during the plasma etching process, thereby preventing charge damage to MOS transistors of the integrated circuit dies, which renders obvious that “*said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies,*” as claimed.

6. Claim 3

a. [3.0] *The method according to claim 1 wherein said mask comprises photoresist.*

283. As analyzed at limitation [1.2.1], the prior art combination uses a photoresist mask, which renders obvious that “*said mask comprises photoresist,*” as claimed.

7. Claim 4

- a. [4.0] *The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.***

284. As analyzed at limitations [1.2.1]-[1.3], Eriguchi's dual damascene structure includes contact holes for functional plugs 9a and 9c that are formed in a dual damascene process, which renders obvious that "*said interconnect recessed trench is a damascene opening,*" as claimed.

8. Claim 5

- a. [5.0] *The method according to claim 1 wherein said interconnect recessed trench is a contact hole.***

285. As analyzed at [1.3] and [1.4.1]-[1.4.2], Eriguchi's interconnect recessed trench is a contact hole for a functional plug, which renders obvious that "*said interconnect recessed trench is a contact hole,*" as claimed.

9. Claim 6

- a. [6.0] *The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.***

286. Eriguchi renders obvious this claim.

287. The analysis in claim 1 focused on Eriguchi's embodiment of Figure 1A. Additionally, Eriguchi's discloses a further embodiment, in Figure 10A, where a functional conductor 127a is formed over a conducting line 123 and an active

region 105 in the substrate 101. Ex.1007, [0138]-[0141]. The further embodiment of Figure 10A, similarly has the ability to reduce “the total electrical stress applied to the gate insulating film 106.” Ex.1007, [0144].

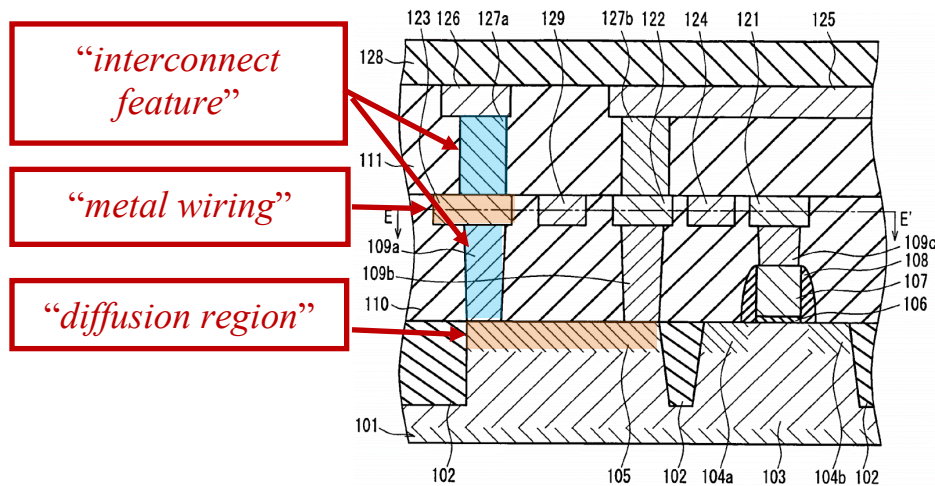


FIG 10A

Ex.1007, FIG. 10A (annotated).

288. A POSITA would have understood that active region 105 is formed by ion implantation of a dopant and annealing that causes the dopant to “diffuse” to proper location. In the further embodiment of Figure 10A, functional conductor 127a, separately and together with functional conductor 109a, would correspond to the “*interconnect feature*,” while the metal line 123 and the active region 105 (a diffusion region, Ex.1007, [0117]), would correspond to the “*underlying conductive layer...[that] comprises metal wiring and diffusion region.*”

289. It would have been obvious to a POSITA to combine Eriguchi's embodiment of Figure 1A with the teachings of Figure 10A, when implementing integrated circuit dies (see analysis at limitation [1.1.1]), so that the charging damage can be suppressed even if an electric field is applied in the reverse direction. Ex.1007, [0032], [0130], [0144]-[0145].

290. Thus, Eriguchi renders obvious that "*said underlying conductive layer comprises metal wiring and diffusion region,*" as claimed.

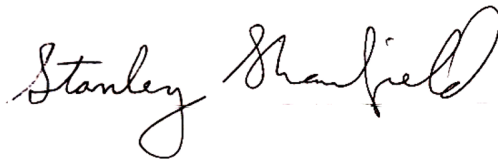
VI. SECONDARY CONSIDERATIONS

291. At this stage of these proceedings, it is my understanding that Petitioner has no burden to identify and rebut secondary considerations. Rather, it is my understanding that Patent Owner must first present a prima facie case for such consideration, which Petitioner should then have the chance to rebut. That said, I have considered evidence of secondary considerations that I am aware of at this time, and I am currently unaware of any evidence of secondary considerations that would support a finding of non-obviousness.

VII. DECLARATION

292. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: September 18, 2025

A handwritten signature in cursive script that reads "Stanley Shanfield". The signature is written in black ink and is positioned above a horizontal line.

Stanley Shanfield, Ph.D.