



Certification of Accuracy of Translation

Sun IP Project # 24-1521

Name: Dr. Warren Smith

Address: 27 Sandy Brook Dr., Durham, NH

Telephone: 603-868-2845

I, Dr. Warren Smith, hereby declare that I am a professional translator, with 40 years of professional experience, and am knowledgeable and well acquainted with the Japanese language and the English language.

The document (002-JP1999-0074523 -Matsunaga (Toshiba) 1999_ENGLISH) in the English language attached hereto is to the best of my ability, knowledge, and expertise, the correct English translation of the original document written in the Japanese language.

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A handwritten signature in black ink, appearing to read "Warren Smith", is written over a horizontal line.

<Dr. Warren Smith>

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(33) Country of Priority Claim	Japan (JP)	CITY, KANAGAWA PREFECTURE
		(72) Inventor
		MATSUNAGA, NORIAKI
		% Toshiba Yokohama Office
		8 Shin-Sugita-cho, Isogo-ku, Yokohama City,
		Kanagawa Prefecture
		(74) Agent
		Patent attorney SUZUE, TAKEHIKO (AND 6 OTHER)

(54) [TITLE OF THE INVENTION]

Semiconductor Device and Manufacturing Method
Thereof

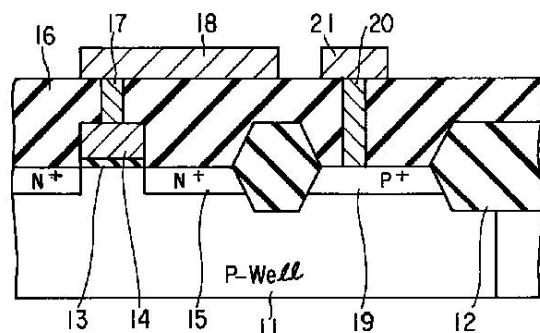
(57) [ABSTRACT]

[PROBLEM]

To provide an interconnecting structure able to prevent charging damage in a plasma process such as RIE, or the like.

[MEANS FOR RESOLUTION]

A semiconductor device comprising a semiconductor component that has an MIS structure, and a functional interconnection that is connected to a gate of said semiconductor component, used in circuit operation, wherein: dummy interconnections 20 and 21, connected to a semiconductor substrate and not used in circuit operation are provided in the vicinity of the functional interconnections.



11 P Well 12素子分離絶縁膜 13ゲート絶縁膜 14ゲート
15, 19 不純物拡散層 16層間絶縁膜 17層間接続機能配線部
18層上機能配線部 20層間接続タミー配線部 21層上タミー配線部

- 11: P Well
- 12: Insulating Film for Element Isolation
- 13: Gate Insulating Film
- 14: Gate
- 15, 19: Dopant Diffusion Layers
- 16: Interlayer Insulating Film
- 17: Interlayer Connecting Functional Interconnecting Portion
- 18: On-Layer Functional Interconnecting Portion
- 19: P+ Dopant Diffusion Layer
- 20: Interlayer Connecting Dummy Interconnecting Portion
- 21: On-Layer Dummy Interconnecting Portion

[PATENT CLAIMS]

[CLAIM 1]

A semiconductor device comprising:

a semiconductor component having an MIS structure, formed on a primary surface side of a semiconductor substrate;

an interlayer insulating film of at least one layer;

a functional interconnection that is made from a first functional interconnecting portion that is formed within a connecting hole in the interlayer insulating film and a second functional interconnecting portion that is formed on the interlayer insulating film, and is used in circuit operation, connected to a gate of the semiconductor component; and

a dummy interconnection that is provided in a region that is separated from the functional interconnection, and is not used in circuit operation, connected to the semiconductor substrate.

[CLAIM 2]

A semiconductor device set forth in claim 1, wherein:

a dummy interconnection is provided in a vicinity of a functional interconnection.

[CLAIM 3]

A semiconductor device set forth in claim 1, wherein:

at least one intermediate interconnection is provided between the functional interconnection and a dummy interconnection, where a dummy interconnection and a functional interconnection are each provided in a vicinity of said at least one intermediate interconnection.

[CLAIM 4]

A semiconductor device set forth in any of claim 1 through 3, comprising:

a first dummy interconnecting portion that is formed in a connecting hole of the interlayer insulating film of at least one layer, and a second dummy interconnecting portion that is formed on said interlayer insulating film of at least one layer.

[CLAIM 5]

A semiconductor device set forth in any of claim 1 through 3, wherein:

a dummy interconnection comprises only a first dummy interconnecting portion that is formed in a connecting hole in the interlayer insulating film.

[CLAIM 6]

A semiconductor device set forth in any of claim 1 through 3, wherein:

a dummy interconnection comprises a plurality of first dummy interconnecting portions that are formed within respective connecting holes in a plurality of interlayer insulating films, and at least one second dummy interconnecting portion that is formed over an interlayer insulating film other than a topmost layer interlayer insulating film.

[CLAIM 7]

A semiconductor device comprising:

a semiconductor component having an MIS structure that is formed on the primary surface side of a semiconductor substrate;

an interlayer insulating film of at least one layer;

a functional interconnection made from a first functional interconnecting portion that is formed within a connecting

hole of the interlayer insulating film and a second functional interconnecting portion that is buried in an interconnection groove of the interlayer insulating film, said functional interconnection used in circuit operation, connected to a gate of the semiconductor component; and

a dummy interconnection that is provided in a region that is a dummy, separate from the functional interconnection, and is not used in circuit operation, connected to the semiconductor substrate.

[CLAIM 8]

A semiconductor device set forth in claim 7, wherein:

a first dummy interconnecting portion that is formed in a dummy connecting hole of the interlayer insulating film of at least one layer, and a second dummy interconnecting portion that is buried in a dummy interconnection groove of said interlayer insulating film of at least one layer.

[CLAIM 9]

A semiconductor device set forth in claim 4 or 6, wherein:

short edges of an interconnection pattern for the second functional interconnecting portion and an interconnection pattern of the second dummy interconnecting portion face each other, or a short edge of one faces a long edge of the other.

[CLAIM 10]

A method for manufacturing a semiconductor device including:

a step for forming an electrically conductive film over a lower portion structure that has a semiconductor component that has an MIS structure that is formed on the primary surface side of a semiconductor substrate, an interlayer insulating film of at least one layer, and a portion of a functional interconnection that is connected to a gate of the semiconductor component through the interlayer insulating film of at least one layer and is used in circuit operation, and a dummy interconnection that is connected to the semiconductor substrate through the interlayer insulating film of at least one layer and is not used in circuit operation; and

a step for forming an upper portion functional interconnecting portion that is connected to the lower portion of functional interconnecting portion, that serves as a portion of the functional interconnection, and for forming an upper portion dummy interconnecting portion that is connected to the lower portion dummy interconnecting portion, as a portion of the dummy interconnection, through selectively removing the electrically conductive film through etching using a plasma.

[CLAIM 11]

A semiconductor device manufacturing method, including:

a step for forming an electrically conductive film over a lower portion structure that has a semiconductor component that has an MIS structure that is formed on the primary surface side of a semiconductor substrate, an interlayer insulating film of at least one layer, and a portion of a functional interconnection that is connected to a gate of the semiconductor component through the interlayer insulating film of at least one layer and is used in circuit operation, and a at least a portion of dummy interconnection that is connected to the semiconductor substrate through the interlayer insulating film of at least

one layer and is not used in circuit operation; and a step for forming only an upper portion functional interconnecting portion that is connected to the lower portion of functional interconnecting portion, that serves as a portion of the functional interconnection through selectively removing the electrically conductive film through etching using a plasma. [CLAIM 12]

A manufacturing method for a semiconductor device, including:

a step for forming an interlayer insulating film on the primary surface side of a semiconductor substrate on which is formed a semiconductor component that has an MIS structure;

a step for forming, in the interlayer insulating film, a connecting hole and an interconnection groove for forming a functional interconnection that is connected to a gate of the semiconductor component used in circuit operation, and for forming a dummy connecting hole and a dummy interconnection groove for forming a dummy interconnection that is connected to the semiconductor substrate and not used in circuit operation in the interlayer insulating film through etching using a plasma; and

a step for forming the functional interconnection in the connecting hole and the interconnection groove and also for forming the dummy interconnection in the dummy connecting hole and the dummy interconnection groove.

[DETAILED EXPLANATION OF THE INVENTION]

[0001]

[FIELD OF TECHNOLOGY OF THE PRESENT INVENTION]

The present invention relates to a semiconductor device and a manufacturing method thereof, and, in particular, to a semiconductor device, with the manufacturing method thereof, involving an interconnection structure for reducing charging damage.

[0002]

[PRIOR ART]

In manufacturing of semiconductor devices, charging damage that often occurs due to plasma, such as in RIE, has become a problem. While there are several causes that produce charging damage, one of them is a mechanism wherein electrostatic charge is produced in gate insulating films due to interconnections, contacts, vias, and the like, which are connected to gate electrodes, receiving electrical charges from a plasma, resulting in strong electrical fields, acting on the gate insulating films due to the increase in the gate electropotential, causing an FN electric current to flow, causing damage to the gate insulating film.

[0003]

FIG. 13 is a diagram for explaining the damaging mechanism when patterning interconnections, such as of Al, or the like, using RIE. 51 is an interlayer insulating film that is formed on a silicon substrate (not shown), 52 is a metal film for use by an interconnection using Al, or the like, and 53 is resist.

[0004]

FIG. 13 (a) depicts a stage part way through etching, where the metal film 52 for the interconnection is a continuous film and the gate of an MOS transistor (not shown) is connected to the substrate through the metal film 52 so that there will be no charging damage to the gate portion.

[0005]

FIG. 13 (b) shows the stage wherein etching has progressed further. Given the characteristics of RIE, etching progresses faster in regions wherein the patterns are sparse, when compared regions wherein they are dense, and thus island-shaped patterns are formed, depending on the density of the interconnection patterns, even at a stage that is part way through etching. In this case, despite no charging damage occurring if the pattern of the island-shaped metal film is connected to the substrate, if not connected to the substrate electric charge accumulates in the gate insulating films of the MOS transistors. Consequently, the gate electropotential is increased by the electric charges that have accumulated, causing strong electric field stresses to act on the gate insulating film.

[0006]

FIG. 13 (c) depicts the stage wherein the etching has progressed further, causing complete separation of the pattern of the metal film 52. In this stage, electric charges are received from the side wall parts of the separated pattern of the metal film 52, causing the strong electric field stress to act on the gate insulating film through increasing the gate electropotential.

[0007]

While in the example described above the explanation was for charging damage while processing interconnections through RIR, or the like, the problem also occurs when forming connecting holes or interconnection grooves using RIE, or the like, when manufacturing buried interconnection structures. That is, a potential difference is produced between the gate and the substrate of the MOS transistor through accumulation of electric charge when forming connecting holes and interconnection grooves in the interlayer insulating film through RIE, or the like, causing strong electric field stresses to act on the gate insulating film.

[0008]

[PROBLEM SOLVED BY THE PRESENT INVENTION]

As described above, conventionally charging damage occurs in the MIS structure in a plasma process, such as RIE, during interconnection processing, causing damage to the gate insulating film. Moreover, even in a buried interconnection structure, charging damage occurs in an MIS structure in plasma processes, such as RIE, or the like, when processing connecting holes or interconnection grooves, causing damage to the gate insulating film.

[0009]

The object of the present invention is to provide a semiconductor device, and manufacturing method thereof, enabling an interconnection structure that is able to prevent charging damage by a plasma process such as RIE, or the like.

[0010]

[MEANS FOR SOLVING THE PROBLEM]

A semiconductor device according to the present invention comprises a semiconductor component having an MIS structure, formed on a primary surface side of a semiconductor substrate; an interlayer insulating film of at least one layer; a functional interconnection that is made from a first functional interconnecting portion that is formed within a connecting hole in the interlayer insulating film and a second functional interconnecting portion that is formed on the interlayer insulating film, and is used in

circuit operation, connected to a gate of the semiconductor component; and a dummy interconnection that is provided in a region that is separated from the functional interconnection, and is not used in circuit operation, connected to the semiconductor substrate (defined as "configuration A").

[0011]

In configuration A, preferably the dummy interconnections are provided in a vicinity of the functional interconnections (defined as "configuration B"). Moreover, in configuration A, preferably at least one intermediate interconnection is provided between the functional interconnection and a dummy interconnection, where a dummy interconnection and a functional interconnection are each provided in a vicinity of said at least one intermediate interconnection (defined as "configuration C").

[0012]

In this way, most of the time in a plasma process, such as RIE, or the like, when processing an interconnection, it is possible to maintain the same electropotential for the electropotential of the gate and the electropotential of the semiconductor substrate (a well, or the like) through forming the dummy interconnections. Consequently, this makes it possible to prevent charging damage in the plasma processing, such as RIE, or the like, during interconnection processing, making it possible to prevent damage to the gate insulating film. In particular, it is possible to connect the functional interconnection and the dummy interconnection, with a higher probability, up until immediately prior to the end of RIE, through, in particular, configurations B and C.

[0013]

More specific structures of configuration A and C are as follows. A first dummy interconnecting portion is formed in a connecting hole of the interlayer insulating film of at least one layer, and a second dummy interconnecting portion is formed on said interlayer insulating film of at least one layer (defined as "configuration D").

[0014]

A dummy interconnection comprises only a first dummy interconnecting portion that is formed in a connecting hole in the interlayer insulating film (defined as "configuration E"). A dummy interconnection comprises a plurality of first dummy interconnecting portions that are formed within respective connecting holes in a plurality of interlayer insulating films, and at least one second dummy interconnecting portion that is formed over an interlayer insulating film other than a topmost layer interlayer insulating film (defined as "configuration F").

[0015]

The dummy configuration is terminated through the first dummy interconnecting portion, without the provision of a second dummy interconnecting portion over the interlayer insulating film of the topmost layer (or over the interlayer insulating film of the single layer if the interlayer insulating film is a single layer) in configuration E or F. Because there is no second dummy interconnecting portion, not only is the likelihood that shorting will occur in the first functional interconnection of the topmost layer reduced, but there is also the effect of reducing the capacitance between interconnections. In this case, making the first dummy interconnecting portion and the second functional

interconnecting portion of mutually differing materials, makes it possible to cause the first dummy interconnecting portion to remain in the connecting hole, without being etched, through selectively etching the second functional interconnecting portion in respect to the first dummy interconnecting portion.

[0016]

Note that the spacing between the functional interconnection and the dummy interconnection, the spacing between the functional interconnection and the intermediate interconnection, or the spacing between the dummy interconnection and the intermediate interconnection preferably, at at least some locations, is a distance of no greater than 5 times the design rule for the minimum distance between interconnections, or a distance no less than 1 μm .

[0017]

Moreover, a semiconductor device according to the present invention comprises: a semiconductor component having an MIS structure that is formed on the primary surface side of a semiconductor substrate; an interlayer insulating film of at least one layer; a functional interconnection made from a first functional interconnecting portion that is formed within a connecting hole of the interlayer insulating film and a second functional interconnecting portion that is buried in an interconnection groove of the interlayer insulating film, said functional interconnection used in circuit operation, connected to a gate of the semiconductor component; and a dummy interconnection that is provided in a region that is a dummy, separate from the functional interconnection, and is not used in circuit operation, connected to the semiconductor substrate (defined as "configuration G").

[0018]

More specific structures of configuration G are as follows. The dummy interconnection comprises a first dummy interconnecting portion that is formed in a dummy connecting hole of the interlayer insulating film of at least one layer, and a second dummy interconnecting portion that is buried in a dummy interconnection groove of said interlayer insulating film of at least one layer (defined as "configuration H").

[0019]

Given the configurations set forth above, the regions that will become dummies, wherein the dummy interconnections will ultimately be formed (dummy connecting holes and dummy interconnection grooves) will be formed simultaneously in a plasma process, such as RIE, or the like, when processing the connecting holes and the interconnection grooves. Because of this, in the plasma process the electric charges are supplied to not only the gates but also through the dummy regions to the semiconductor substrate (wells, or the like), which can reduce the potential difference between the electropotential of the gates and the electropotential of the semiconductor substrate. The result is the ability to prevent charging damage in the plasma processes, such as RIE, or the like, when processing the connecting holes or interconnection grooves, making it possible to prevent damage to the gate insulating films.

[0020]

In configurations A through H, set forth above, the methods for connecting the dummy interconnections to the semiconductor structure may be as described below. The dummy interconnection is connected to a substrate region of the same conductivity type, or of the opposite conductivity type (which may be a well region or a non-well region), as the dopant diffusion layer through a dopant diffusion layer (a P⁺ diffusion layer or N⁺ diffusion layer) that is provided in the semiconductor substrate, that is, the dummy interconnection is connected to the substrate through a forward or reverse diode. Note that even if connected in the opposite direction, normally the charge will be to more than several dozen volts, enabling the electric charge to escape into the substrate through a reverse breakdown current.

[0021]

The dummy interconnection is connected to a substrate region (which may be a well region or a non-well region) through a dopant diffusion layer (a P⁺ diffusion layer or N⁺ diffusion layer) that structures a source or drain of a semiconductor component. The footprint can be reduced through connecting the dummy interconnection to the source or drain region in this way.

[0022]

The method for connecting the dummy interconnection to the semiconductor substrate in the configurations A through F, set forth above, may also be as follows. The dummy interconnections provided is connected to a substrate region (which may be a well region or a non-well region), that is either the same as, or separate from, a substrate region in which is formed a semiconductor component that has a gate connection to a functional interconnection. Connecting to a substrate region that is separate can increase the degrees of freedom of the interconnection.

[0023]

In configurations G and H, set forth above, the method for connecting the dummy interconnection to the semiconductor substrate may further be as follows. The dummy interconnection is connected to a substrate region that is the same as a substrate region (which may be either a well region or a non-well region) in which is formed a semiconductor component that is gate-connected to a functional interconnection. Connecting to the same substrate region can effectively reduce the potential difference between the electropotential of the gate and the electropotential of the semiconductor substrate.

[0024]

In configurations D and F, set forth above, if short edges of the interconnecting pattern of the second functional interconnecting portion and the interconnecting pattern of the second dummy interconnecting portion face each other, or if, of the interconnecting pattern of the second functional interconnecting portion and the interconnecting pattern of the second dummy interconnecting portion, a short edge of one faces a long edge of the other, this can reduce the capacitance between interconnections between the second functional interconnecting portion and the second dummy interconnecting portion.

[0025]

In configurations A through F set forth above, if, when there is a region wherein there is a plurality of basic cells

that are configured with the semiconductor device including the semiconductor component, a dummy interconnection is provided for each individual basic cell or for each of a plurality of basic cells, then a basic pattern that includes the dummy interconnection can be used repeatedly, enabling a substantial reduction in time and effort for the circuit design.

[0026]

A method for manufacturing a semiconductor device according to the present invention includes: a step for forming an electrically conductive film over a lower portion structure that has a semiconductor component that has an MIS structure that is formed on the primary surface side of a semiconductor substrate, an interlayer insulating film of at least one layer, and a portion of a functional interconnection that is connected to a gate of the semiconductor component through the interlayer insulating film of at least one layer and is used in circuit operation, and a dummy interconnection that is connected to the semiconductor substrate through the interlayer insulating film of at least one layer and is not used in circuit operation; and a step for forming an upper portion functional interconnecting portion that is connected to the lower portion of functional interconnecting portion, that serves as a portion of the functional interconnection, and for forming an upper portion dummy interconnecting portion that is connected to the lower portion dummy interconnecting portion, as a portion of the dummy interconnection, through selectively removing the electrically conductive film through etching using a plasma.

[0027]

This is a manufacturing method that corresponds in general to Configuration D, set forth above, providing the same effects in operation as the effects in operation already described above. This is a manufacturing method that corresponds in general to Configuration D, set forth above, providing the same effects in operation as the effects in operation already described above. Moreover a method for manufacturing a semiconductor device according to the present invention comprises: a step for forming an electrically conductive film over a lower portion structure that has a semiconductor component that has an MIS structure that is formed on the primary surface side of a semiconductor substrate, an interlayer insulating film of at least one layer, and a portion of a functional interconnection that is connected to a gate of the semiconductor component through the interlayer insulating film of at least one layer and is used in circuit operation, and a at least a portion of dummy interconnection that is connected to the semiconductor substrate through the interlayer insulating film of at least one layer and is not used in circuit operation; and a step for forming only an upper portion functional interconnecting portion that is connected to the lower portion of functional interconnecting portion, that serves as a portion of the functional interconnection through selectively removing the electrically conductive film through etching using a plasma. This is a manufacturing method that corresponds in general to Configuration E or F, set forth above, providing the same effects in operation as the effects in operation already described above.

[0028]

Moreover a method for manufacturing a semiconductor device according to the present invention comprises: a step for forming an interlayer insulating film on the primary surface side of a semiconductor substrate on which is formed a semiconductor component that has an MIS structure; a step for forming, in the interlayer insulating film, a connecting hole and an interconnection groove for forming a functional interconnection that is connected to a gate of the semiconductor component used in circuit operation, and for forming a dummy connecting hole and a dummy interconnection groove for forming a dummy interconnection that is connected to the semiconductor substrate and not used in circuit operation in the interlayer insulating film through etching using a plasma; and a step for forming the functional interconnection in the connecting hole and the interconnection groove and also for forming the dummy interconnection in the dummy connecting hole and the dummy interconnection groove. This is a manufacturing method that corresponds in general to Configuration H, set forth above, providing the same effects in operation as the effects in operation already described above.

[0029]

[EMBODIMENTS OF THE INVENTION]

Ideal embodiments according to the present invention will be explained below in reference to the drawings. FIG. 1 depicts a first embodiment according to the present invention. 11 is a P well that is formed in a silicon substrate; 12 is a component isolating insulating film; 13 is a gate insulating film; 14 is a gate; 15 is a dopant diffusion layer that is used for sources and drains; and 16 is an interlayer insulating film. A functional interconnection that is used in actual circuit operation is connected to the gate 14, where this functional interconnection is structured from an interconnecting portion 17 that is formed within a connecting hole of the interlayer insulating film 16 (hereinafter termed an interlayer connecting functional interconnecting portion) and an interconnecting portion 18 that is formed on the interlayer insulating film (hereinafter termed an on-layer functional interconnecting portion). A dummy interconnection that is not used in actual circuit operation (that is isolated electrically from the functional interconnection, and the like) is connected to the dopant diffusion layer 19, where this dummy interconnection is structured from an interconnecting portion 20 that is formed within a connecting hole of the interlayer insulating film 16 (hereinafter termed an interlayer connecting dummy interconnecting portion) and an interconnecting portion 21 (hereinafter termed the on-layer dummy interconnecting portion) that is formed on the interlayer insulating film. The on-layer functional interconnecting portion 18 and the on-layer dummy interconnecting portion 21 are disposed so as to be in mutual proximity in at least some location (preferably in proximity at a distance that is no more than five times the design rule for the minimum distance between interconnections or a distance no more than 1 μm).

[0030]

While the on-layer functional interconnecting portion 18 is obtained through processing using RIE after film formation of an interconnection film on the interlayer insulating film 16, in this RIE process a pattern for the on-

layer dummy interconnecting portion 21 is formed in the vicinity of the pattern for the on-layer functional interconnecting portion 18. The formation of this on-layer dummy interconnecting portion 21 in the vicinity of the on-layer functional interconnecting portion 18 makes it possible to maintain the electropotential of the gate 16 of the MOS transistor and the electropotential of the P well 11 at conductive electropotentials throughout nearly the entirety of the RIE process. The result is the ability to prevent charging damage to the gate oxide film 13, through not applying the strong electric field.

[0031]

Note that the length of the on-layer dummy interconnecting portion 21 being as short as possible is preferred from the perspective of circuit operation through the ability to reduce the capacitance between interconnections that is formed between the on-layer dummy interconnecting portion 21 and the on-layer functional interconnecting portion 18. If the increase in the capacitance between interconnections is not a substantial problem in terms of circuit operation, then having a long length for the on-layer dummy interconnecting portion 21 is preferred from the perspective of preventing charging damage.

[0032]

FIG. 2 depicts a second embodiment according to the present invention. Identical numbers are applied to structural elements that are substantially identical or corresponding to those of the first embodiment, depicted in FIG. 1, and detailed explanations thereof are omitted (with the same true for the other embodiments as well).

[0033]

While in the first embodiment, shown in FIG. 1, the dummy interconnection was structured from an interlayer connecting dummy interconnecting portion 20 and an on-layer dummy interconnecting portion 21, in the present embodiment the dummy interconnection is structured from the interlayer connecting dummy interconnecting portion 20 alone, given that the on-layer dummy interconnecting portion 21, depicted in FIG. 1, is not provided. The on-layer functional interconnecting portion 18 and the interlayer connecting dummy interconnecting portion 20 are provided in mutual proximity in at least some location. The omission of the on-layer dummy interconnecting portion 21 can reduce shorting of the on-layer functional interconnecting portion 18 and can reduce the capacitance between interconnections.

[0034]

Although the on-layer functional interconnecting portion 18 is obtained through processing using RIE after film formation of the interconnection metal on the interlayer insulating film 16, only the pattern of the on-layer functional interconnecting portion 18 is formed in the RIE process. Unlike the first embodiment, no on-layer dummy interconnecting portion 21 is formed, but rather the interconnection metal remains on the interlayer insulating film 16 until the RIE process is complete, and thus, as with the first embodiment, the electropotential of the gate 16 of the MOS transistor and the electropotential of the P well 11 can maintain conduction electropotentials during nearly the entirety of the RIE process. Consequently, as with the first embodiment, it is possible to prevent the charging damage,

through not applying a strong electric field to the gate oxide film 13.

[0035]

Note that the interlayer connecting dummy interconnecting portion 20 and the on-layer functional interconnecting portion 18 being structured from mutually differing materials (for example, with tungsten for the interlayer connecting dummy interconnecting portion 20 and aluminum for the on-layer functional interconnecting portion 18) makes it possible to etch the on-layer functional interconnecting portion 18, with respect to the interlayer connecting dummy interconnecting portion 20, so as to leave the interlayer connecting dummy interconnecting portion 20 in the connecting hole, rather than etching it.

[0036]

FIG. 3 depicts a third embodiment according to the present invention. The present embodiment is that wherein the present invention is applied to a multilayer interconnection structure. That is, an interlayer insulating film 31 is formed on the top layer side of the interlayer insulating film 16, the functional interconnection is structured from an interlayer connecting functional interconnecting portion 17, an on-layer functional interconnecting portion 18, an interlayer connecting functional interconnecting portion 32, and an on-layer functional interconnecting portion 33, and the dummy interconnection is structured from an interlayer connecting dummy interconnecting portion 20, an on-layer dummy interconnecting portion 21, an interlayer connecting dummy interconnecting portion 34, and an on-layer dummy interconnecting portion 35.

[0037]

In the example depicted in FIG. 3, the on-layer functional interconnecting portion 18 and on-layer dummy interconnecting portion 21 are disposed so as to be mutually adjacent in at least some location, and also the on-layer functional interconnecting portion 33 and on-layer dummy interconnecting portion 35 are disposed so as to be mutually adjacent in at least some location. The result is the ability to prevent charging damage in both the RIE process for forming an on-layer functional interconnecting portion 18 and the RIE process for forming the on-layer functional interconnecting portion 33.

[0038]

FIG. 4 depicts a fourth embodiment according to the present invention. As with the third embodiment, set forth above, the present embodiment applies the present invention to a multilayer interconnection structure. In the present embodiment, the interlayer insulating film 31 of the topmost layer is not provided with the on-layer dummy interconnecting portion 35 that is depicted in FIG. 3. The on-layer functional interconnecting portion 33 and the interlayer connecting dummy interconnecting portion 34 are disposed so as to be mutually adjacent in at least some location. In this way, the omission of the on-layer dummy interconnecting portion 35 is able to reduce shorting of the on-layer functional interconnecting portion 33 and also to reduce capacitance between interconnections, the same as in the second embodiment, depicted in FIG. 2.

[0039]

FIG. 5 depicts a fifth embodiment according to the present invention. In the first embodiment, and like, the

dummy interconnection is connected to the P well through a P⁺ dopant diffusion layer, where the dopant diffusion layer and the well are of an identical conductivity type. In the present embodiment, however, the dummy interconnection is connected through the N⁺ dopant diffusion layer 19b to the P well 11, where the dopant diffusion layer and the well are of opposite conductivity type. Consequently, the dummy interconnection is connected to the P well 11 through a diode, but even with such a connection it is possible to achieve the same effect as in the first embodiment, and the like. The diode may be of a forward connection or a reverse connection, depending on the polarity of charging during RIE. Note that even if a reverse connection, normally the charging during RIE is to no less than several tens of volts, and thus the electric charge can escape into the P well 11 through a reverse breakdown current.

[0040]

FIG. 6 depicts a sixth embodiment according to the present invention. While in the first embodiment, and the like, the dummy interconnection was connected to the well through a dopant diffusion layer wherein the source and drain of the MOS transistor are provided separately, in the present embodiment the dummy interconnection is connected to the P well 11 through a dopant diffusion layer 15 that structures the source or the drain of a MOS transistor. In this way, the connection of the dummy interconnection to the dopant diffusion layer that structures the source or drain is able to reduce the footprint.

[0041]

FIG. 7 depicts a seventh embodiment according to the present invention. While in the first embodiment, and the like, the dummy interconnection was connected to the same well as the well in which is formed a MOS transistor that has functional interconnections 17 and 18 connected to the gate thereof, in the present embodiment the dummy interconnection is connected to a different well. In the example depicted in FIG. 7, the dummy interconnections 20 and 21 are connected to an N well 11a through the N⁺ dopant diffusion layer 19a. Note that while in this example the well (P well 11) wherein is formed the MOS transistor to which the functional interconnections 17 and 18 are connected and the well (N well 11a) to which the dummy interconnections 20 and 21 are connected are of different conductivity types, they may, of course, be of the same conductivity type instead.

[0042]

FIG. 8 depicts an eighth embodiment according to the present invention. While in the first embodiment, and the like, the dummy interconnection was disposed in the vicinity of the functional interconnection, in the present embodiment at least one intermediate interconnection 22 is disposed between the dummy interconnection and the functional interconnection, where the dummy interconnection and the functional interconnection are each disposed near the intermediate interconnection 22. If there is a plurality of intermediate interconnections, then mutually adjacent intermediate interconnections are disposed so as to be near to each other. Here the intermediate interconnections may be, for example, those that are used in actual circuit operation (for example, those that are connected to components that are used in circuit

operation), or those that are not used in actual circuit operation (for example, those that are electrically isolated from components, or the like).
[0043]

As with the first embodiment, and the like, the on-layer functional interconnecting portion 18 was obtained through processing using RIE after film formation of the interconnection metal on the interlayer insulating film 16, but the patterns for the on-layer dummy interconnecting portion 21 and the intermediate interconnection 22 are formed in the RIE process. In this way, the dummy interconnection and the functional interconnection are connected through the intermediate interconnection 22, even when an intermediate interconnection 22 is formed between the dummy interconnection and the functional interconnection, making it possible to maintain, at conductive electropotentials, the electropotential of the gate 14 of the MOS transistor and the electropotential of the well 11 throughout nearly all of the RIE process. The result is the ability to prevent charging damage, through not having a strong electric field act on the gate oxide film 13.
[0044]

Note that while in the first through eighth embodiments, described above, the explanations were for cases wherein the wells wherein the MOS transistors having the functional interconnections connected to the gates thereof were formed were P wells, they may of course be N wells instead. Moreover, while in the first through eighth embodiment set forth above the dopant diffusion layers to which the MOS transistors and dummy interconnections were connected were formed in well regions of the semiconductor substrates, they may instead be regions of the semiconductor substrates wherein wells are not formed (non-well regions). Moreover, the respective structures explained in the first through eighth embodiments set forth above may, of course, be combined with each other.
[0045]

The planar positional relationships between the functional interconnection and the dummy interconnection, described in the first through eighth embodiments, set forth above, and, in particular, the planar layout relationships between the on-layer functional interconnecting portion 18 (33) and the on-layer dummy interconnecting portion 21 (35), will be explained next in reference to FIG. 9 and FIG. 10.
[0046]

FIG. 9 (A) is that wherein the on-layer functional interconnecting portion 18 (33) and the on-layer dummy interconnecting portion 21 (35) are in parallel, and the length of the on-layer dummy interconnecting portion 21 (35) is shortened. Having the length of the on-layer dummy interconnecting portion 21 (35) be shortened in this way enables a reduction in the capacitance between the interconnections formed by the on-layer dummy interconnecting portion 21 (35) and the on-layer functional interconnecting portion 18 (33).
[0047]

FIG. 9 (B) is that wherein the on-layer functional interconnecting portion 18 (33) and the on-layer dummy interconnecting portion 21 (35) are parallel and the length of the on-layer dummy interconnecting portion 21 (35) is lengthened. The lengthening of the on-layer dummy

interconnecting portion 21 (35) in this way enables a higher probability that the functional interconnection and the dummy interconnection will be connected up until immediately prior to the completion of RIE.
[0048]

FIG. 9 (C) is that wherein respective short edges of the on-layer functional interconnecting portion 18 (33) and the on-layer dummy interconnecting portion 21 (35) are facing each other, enabling a reduction in the capacitance between interconnections formed by the on-layer dummy interconnecting portion 21 (35) and the on-layer functional interconnecting portion 18 (33).
[0049]

FIG. 9 (D) is that wherein, of the on-layer functional interconnecting portion 18 (33) and the on-layer dummy interconnecting portion 21 (35), the short edge of one faces the long edge of the other, enabling a reduction in the capacitance between interconnections formed by the on-layer dummy interconnecting portion 21 (35) and the on-layer functional interconnecting portion 18 (33).
[0050]

FIG. 10 is a structural example of a case wherein an intermediate interconnection is provided between the on-layer functional interconnection portion 18 (33) and the on-layer dummy interconnecting portion 21 (35). In this example, an intermediate interconnection 22a that is used in actual circuit operation (for example, that which is connected to a component that is used in circuit operation), and an intermediate interconnection 22b that is not used in actual circuit operation (for example, that which is electrically isolated from components, or the like), are provided.
[0051]

An example of application of a dummy interconnection (the location of application, and the like) will be explained next. The location of application of the dummy interconnection may be, for example, in the vicinity of an interconnection that is connected to the input of a CMOS inverter, the vicinity of a word line for an SRAM, the vicinity of a data line for a multiplier, or the like. Disposal in the vicinity of a clock signal line, word line, address bus line, or the like, wherein the interconnection is long (the antenna ratio is high), or in the vicinity of an interconnection that is prone to a potential difference occurring between the gate and the substrate and a plasma process, such as RIE, or the like, is particularly effective.
[0052]

FIG. 11 is that wherein a dummy interconnection is disposed within a basic cell of an SRAM, where an SRAM array is structured using repetitions of the basic cell. That is, an SRAM array is structured through configuring a basic cell through arranging a dummy interconnection DM in the vicinity of a word line WL (FIG. 11 (A)), and arranging these in repetitions (FIG. 11 (B)). If, when structuring a circuit through repeating basic cells in this way, the dummy interconnections are provided for each individual basic cell or each plurality of basic cells, this can greatly reduce the time and effort required for circuit design.
[0053]

FIG. 12 is an example of a case wherein a dummy interconnection is applied to a microprocessor circuit. In the figure, dummy interconnections are arranged at the

locations indicated by the "X" marks, and dummy interconnections are provided between adjacent circuit blocks instead of within each circuit. The use of such a structure enables formation of dummy interconnections even when it is not possible to secure space for the provision of dummy interconnections within the circuit block.

[0054]

A ninth embodiment according to the present invention will be explained next in reference to FIG. 14. In the present embodiment the present invention is applied to a buried interconnection structure. Note that those structural elements that are substantially identical or corresponding to those in the first embodiment, depicted in FIG. 1, are assigned identical numbers, and detailed explanations thereof will be omitted (both here and below).

[0055]

FIG. 14 (A) is that which depicts a state wherein an interlayer insulating film 61 is formed over a substrate whereon MOS transistors, or the like, are formed, and a connecting hole 62 and interconnection groove 63 for forming an interconnection, in the so-called dual damascene structure, to the interlayer insulating film 61 are formed through an RIE process, but in this case dummy connecting holes 64 and dummy interconnection grooves 65 are also formed at the same time through the RIE process.

[0056]

Because conventionally electric charges accumulate only on the gate 14 when the surface of the gate 14 is exposed through an RIE process, there is a problem in that a large potential difference is produced between the gate 14 and the substrate (the P well 11) so that a strong electric field stress acts on the gate insulating film 13. In the present embodiment, the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed simultaneously in the RIE process, and thus not only are electric charges supplied to the gate, but also to the P⁺ dopant diffusion layer 19 that is formed in the substrate, which can reduce the potential difference between the electropotential of the gate and the electropotential of the substrate. Consequently, the electric field that acts on the gate insulating film 13 is weakened, making it possible to prevent charging damage.

[0057]

After the RIE process has been completed, metal for a prescribed interconnection is deposited over the entire surface, to bury the metal for the interconnection through RIE or CMP. In this way, as depicted in FIG. 14 (b), not only are an interconnecting portion 66 that is buried in the connecting hole 62 (hereinafter termed an in-hole functional interconnecting portion) and an interconnecting portion 67 that is buried in the interconnection groove 63 (hereinafter termed an in-groove functional interconnecting portion) formed, but an interconnecting portion 68 that is buried in the dummy connecting hole 64 (hereinafter termed an in-hole dummy interconnecting portion) and an interconnecting portion 69 that is buried in the dummy interconnection groove 65 (hereinafter termed an in-groove dummy interconnecting portion) are formed as well.

[0058]

A tenth embodiment according to the present invention will be explained next in reference to FIG. 15. In the present embodiment, the present invention is applied to a multilayer interconnection of a buried interconnection structure. FIG. 15 (a) is that which depicts a state wherein an interlayer insulating film 71 is formed on a lower portion structure that is formed through, for example, the process of FIG. 14, and a connecting hole 72 and an interconnection groove 73, for forming an interconnection of a dual damascene structure, are formed through an RIE process in the interlayer insulating film 71. In this case, the dummy connecting hole 74 and the dummy interconnection groove 75 are also formed at the same time through the RIE process, described above.

[0059]

Conventionally, electric charge accumulates on only the gate 14 through the lower portion interconnection (the in-hole functional interconnecting portion 66 and the in-groove functional interconnecting portion 67) when the lower portion interconnection surface (the surface of the in-groove functional interconnecting portion 67) are exposed in the RIE process. Consequently, there is a problem in that a large potential difference is produced between the gate 14 and the substrate (the P well 11), so that a large electric field stress acts on the gate insulating film 13. In the present embodiment the dummy connecting holes 74 and the dummy interconnection groove 75 are also formed at the same time in the RIE process, so that the electric charge is supplied also to the P⁺ dopant diffusion layer 19 that is formed in the substrate, through the lower portion interconnection (the in-hole dummy interconnecting portion 68 and the in-groove dummy interconnecting portion 69), which can reduce the potential difference between the electropotential of the gate and the electropotential of the substrate. The result is the ability to weaken the electric field that acts on the gate insulating film 13, which can prevent charging damage.

[0060]

After completion of the RIE process, a prescribed metal for interconnection is deposited over the entire surface, burying the metal for interconnection through RIE or CMP. In this way, as depicted in FIG. 14 (b), not only are an in-hole functional interconnecting portion 76, which is buried in the connecting hole 72, and an in-groove functional interconnecting portion 77, which is buried in the interconnection groove 73, formed, but an in-hole dummy interconnecting portion 78, which is buried in the dummy connecting hole 74, and an in-groove dummy interconnecting portion 79, which is buried in the dummy interconnection groove 75, are formed as well.

[0061]

An 11th embodiment according to the present invention will be explained next in reference to FIG. 16. The present embodiment is also similar to the tenth embodiment in that the present invention is applied to a multilayer interconnection of a buried interconnection structure.

[0062]

In the present embodiment, as depicted in FIG. 16, a plurality of dummy interconnecting regions are provided in a single well. Preferably there is a balance between the electric charge received by the gate and the electric charge received by the well during RIE for a single well, in order

to reduce the charging damage on the gate insulating film. However, there are cases wherein the number of connecting holes in a gate is large, so that the electric charge received by the gate will be quite different from the electric charge received from the well. Given this, within a given well 11 the total area of the connecting holes in the gate 14 is made as equal as possible to the total area of the dummy connecting holes in the well (on the P⁺ diffusion layer 19). For example, if the area of each connecting hole in the gate 14 is equal to the area of a dummy connecting hole in the P⁺ dopant diffusion layer 19, the numbers for each should be identical.

[0063]

Note that in the ninth through 11th embodiments, described above (the examples wherein the present invention is applied to buried interconnection structures), the explanations were for interconnection of dual damascene structures; however, application may also be to interconnections of single damascene structures.

[0064]

Moreover, while in the ninth through 11th embodiments, examples were given wherein an NMOS transistor is manufactured in a P well, corresponding to the first embodiment, and the like, depicted in FIG. 1, where dummy interconnections are connected to the P⁺ diffusion layer, a structure may be employed as depicted in FIG. 5 and FIG. 6.

[0065]

Unlike the first through eighth embodiments, in the ninth through 11th embodiments, set forth above, there is no need to necessarily provide the dummy interconnection near to the functional interconnection, but when RIE is used when embedding the interconnection metal, a problem arises with charging damage when processing the interconnection, the same as in the first through eighth embodiments. Consequently, structures such as depicted in FIG. 9 and FIG. 10, for example, may be employed also for the planar positional relationships between the functional interconnections and the dummy interconnections.

[0066]

While various embodiments have been described above, the present invention is not limited to these embodiments, but rather various modifications may be applied within a range that does not deviate from the spirit and intent thereof.

[0067]

[EFFECTS OF THE INVENTION]

The present invention makes it possible to reduce the potential difference between the electropotential of a gate and the electropotential of a semiconductor substrate in a plasma process such as RIE, or the like. Consequently, this makes it possible to prevent damage to the gate insulating film, through preventing charging damage in the plasma process, such as RIE, or the like.

[BRIEF DESCRIPTIONS OF THE DRAWINGS]

FIG. 1 is a diagram depicting a cross-sectional structure of a first embodiment according to the present invention.

FIG. 2 is a diagram depicting a cross-sectional structure of a second embodiment according to the present invention.

FIG. 3 is a diagram depicting a cross-sectional structure of a third embodiment according to the present invention.

FIG. 4 is a diagram depicting a cross-sectional structure of a fourth embodiment according to the present invention.

FIG. 5 is a diagram depicting a cross-sectional structure of a fifth embodiment according to the present invention.

FIG. 6 is a diagram depicting a cross-sectional structure of a sixth embodiment according to the present invention.

FIG. 7 is a diagram depicting a cross-sectional structure of a seventh embodiment according to the present invention.

FIG. 8 is a diagram depicting a cross-sectional structure of an eighth embodiment according to the present invention.

FIG. 9 is a diagram depicting the planar positional relationships between the functional interconnections and the dummy interconnections depicted in the first through seventh embodiments.

FIG. 10 is a diagram depicting the planar positional relationships between the functional interconnections, the intermediate interconnections, and the dummy interconnections depicted in the eighth embodiment.

FIG. 11 depicts a structural example when a dummy interconnection is applied to an SRAM circuit.

FIG. 12 depicts a structural example when a dummy interconnection is applied to an microprocessor circuit.

FIG. 13 is a diagram for explaining problems with the prior art.

FIG. 14 is a diagram depicting a cross-sectional structure of manufacturing processes of a ninth embodiment according to the present invention.

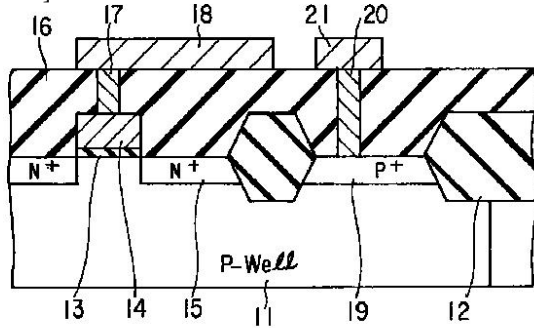
FIG. 15 is a diagram depicting a cross-sectional structure of manufacturing processes of a 10th embodiment according to the present invention.

FIG. 16 is a diagram depicting a cross-sectional structure of a 11th embodiment according to the present invention.

[EXPLANATIONS OF REFERENCE SYMBOLS]

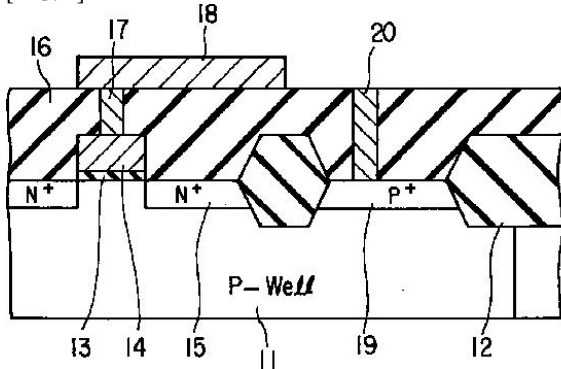
- 11: P Well (Semiconductor Substrate)
- 11a: N Well (Semiconductor Substrate)
- 12: Insulating Film for Element Isolation
- 13: Gate Insulating Film
- 14: Gate
- 15: Source, Drain (Dopant Diffusion Layer)
- 16, 31, 61, 71: Interlayer Insulating Film
- 17, 32: Interlayer Connecting Functional Interconnecting Portion (First Functional Interconnecting Portion)
- 18, 33: On-Layer Functional Interconnecting Portion (Second Functional Interconnecting Portion)
- 19: P⁺ Dopant Diffusion Layer
- 19a, 19b: N⁺ Dopant Diffusion Layer
- 20, 34: Interlayer Connecting Dummy Interconnecting Portion (First Dummy Interconnecting Portion)
- 21, 35: On-Layer Dummy Interconnecting Portion (Second Dummy Interconnecting Portion)
- 22a, 22b: Intermediate Interconnections
- 62, 72: Connecting Holes
- 63, 73: Interconnection Grooves
- 64, 74: Dummy Connecting Holes
- 65, 75: Dummy Interconnection Grooves
- 66, 76: In-hole Functional Interconnecting Portions (First Functional Interconnecting Portions)
- 67, 77: In-groove Functional Interconnecting Portions (Second Functional Interconnecting Portions)
- 68, 78: In-hole Dummy Interconnecting Portions (First Dummy Interconnecting Portions)
- 69, 79: In-groove Dummy Interconnecting Portions (Second Dummy Interconnecting Portions)

[FIG. 1]

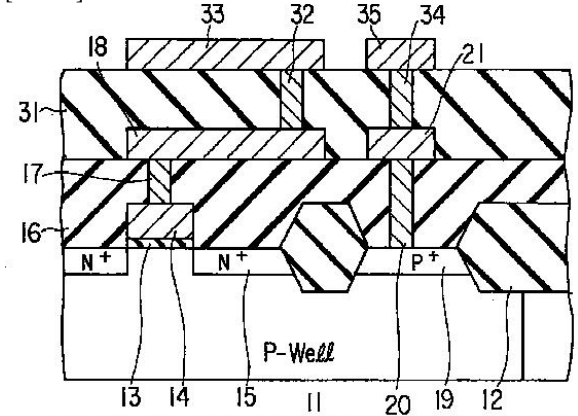


- 11 P Well 12 素子分離絶縁膜 13 ゲート絶縁膜 14 ゲート
15, 19 不純物拡散層 16 層間絶縁膜 17 層間接続機能配線部
18 層上機能配線部 20 層間接続ダミー配線部 21 層上ダミー配線部
11: P Well
12: Insulating Film for Element Isolation
13: Gate Insulating Film
14: Gate
15, 19: Dopant Diffusion Layers
16: Interlayer Insulating Film
17: Interlayer Connecting Functional Interconnecting Portion
18: On-Layer Functional Interconnecting Portion
20: Interlayer Connecting Dummy Interconnecting Portion
21: On-Layer Dummy Interconnecting Portion

[FIG. 2]

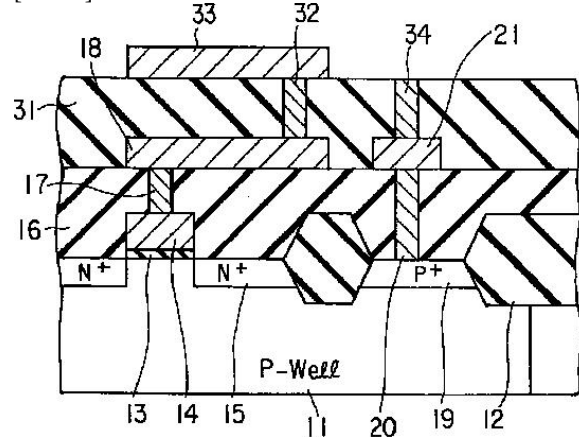


[FIG. 3]

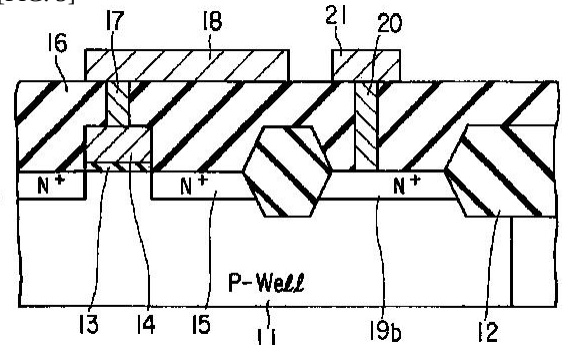


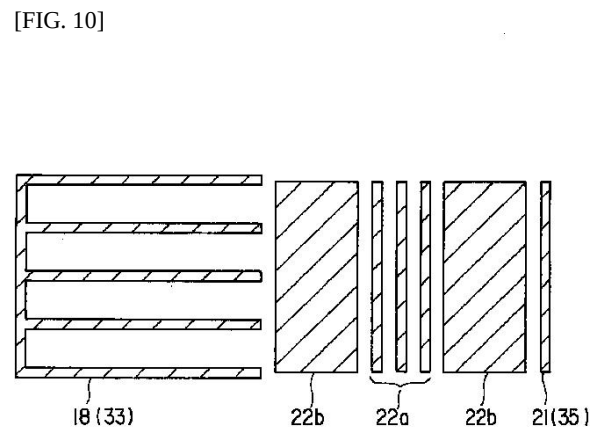
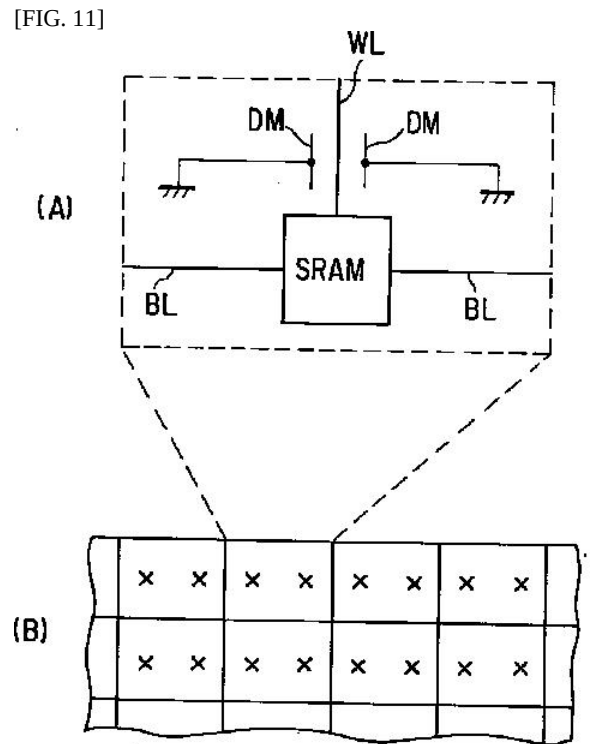
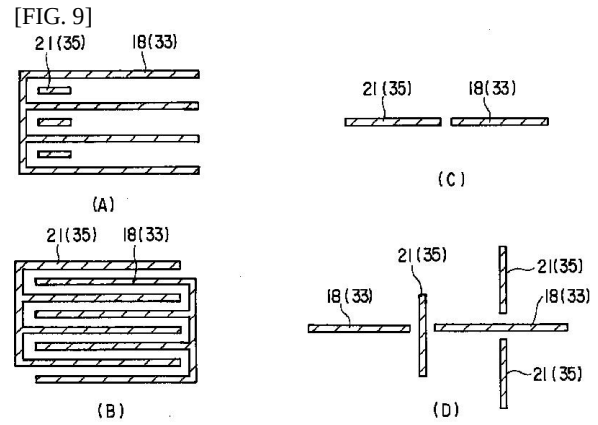
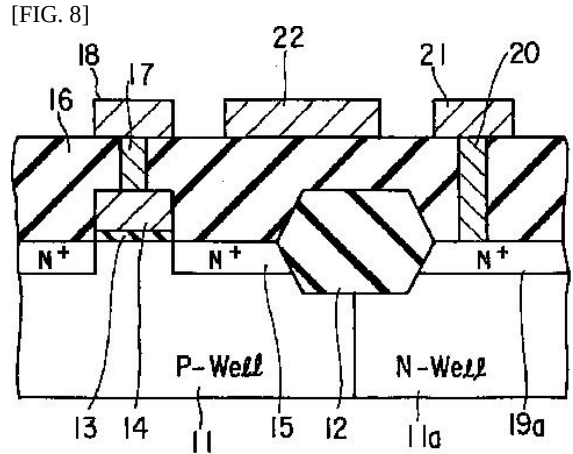
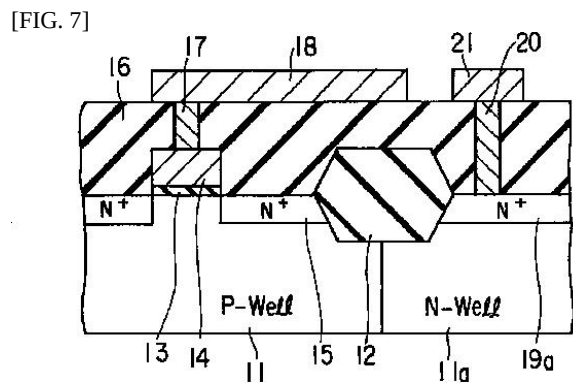
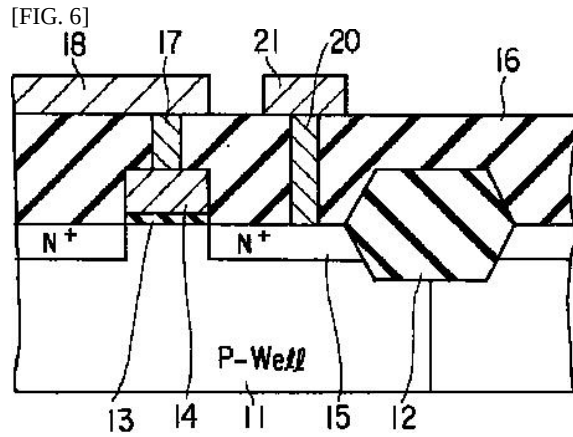
- 31 層間絶縁膜 32 層間接続機能配線部 33 層上機能配線部
34 層間接続ダミー配線部 35 層上ダミー配線部
31: Interlayer Insulating Film
32: Interlayer Connecting Functional Interconnecting Portion
33: On-Layer Functional Interconnecting Portion
34: Interlayer Connecting Dummy Interconnecting Portion
35: On-Layer Dummy Interconnecting Portion

[FIG. 4]

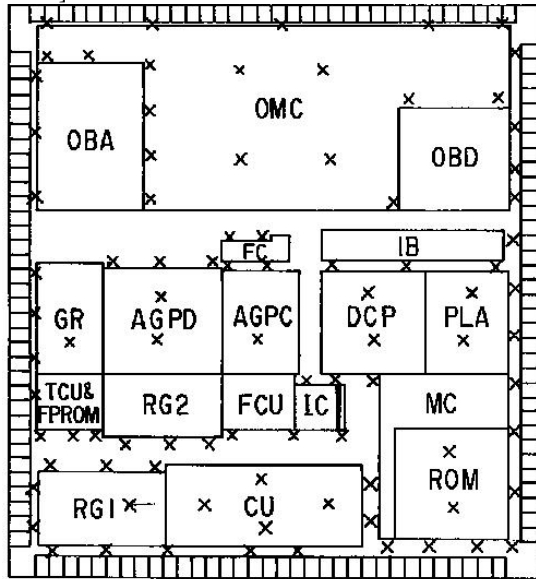


[FIG. 5]

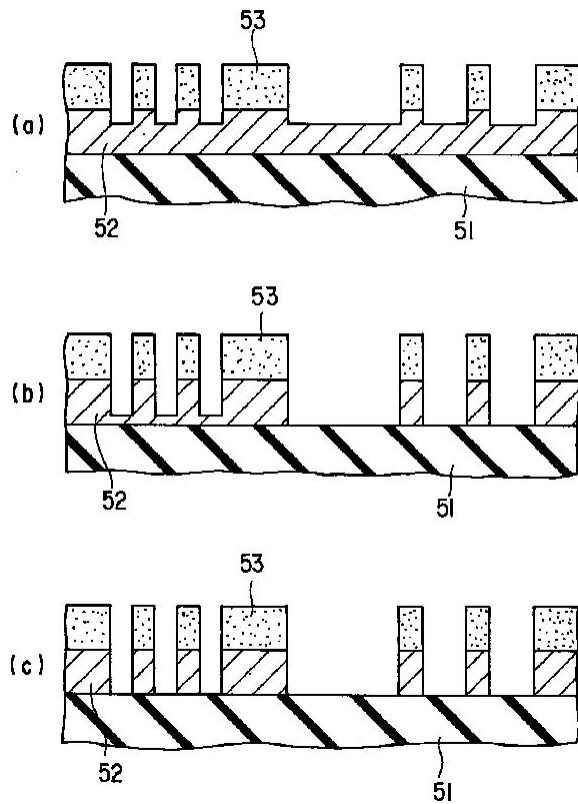




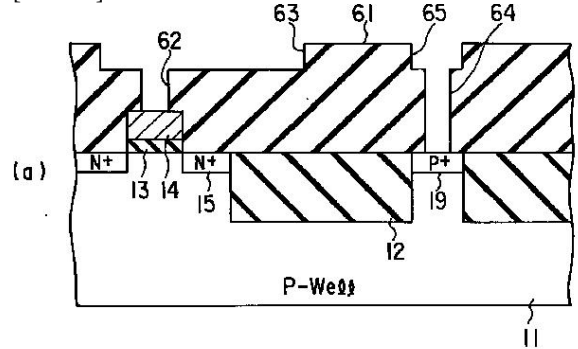
[FIG. 12]



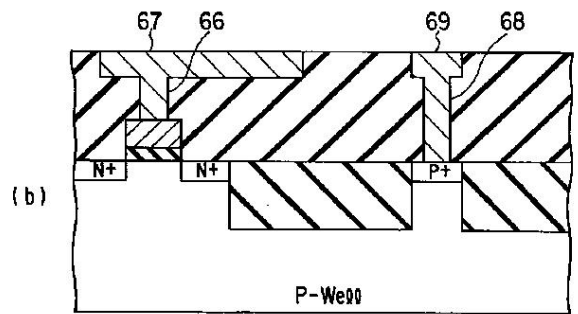
[FIG. 13]



[FIG. 14]



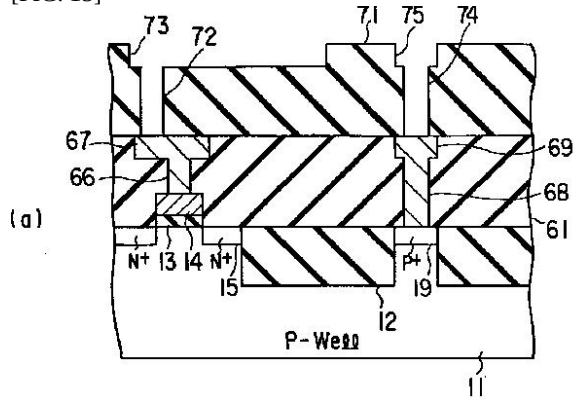
61層間絶縁膜 62接続孔 63配線溝
64ダミー接続孔 65ダミー配線溝



66孔内機能配線部 67溝内機能配線部
68孔内ダミー配線部 69溝内ダミー配線部

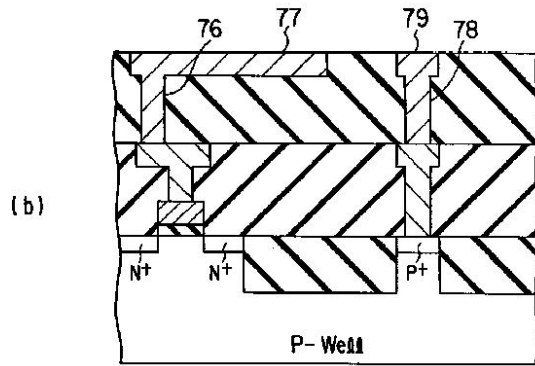
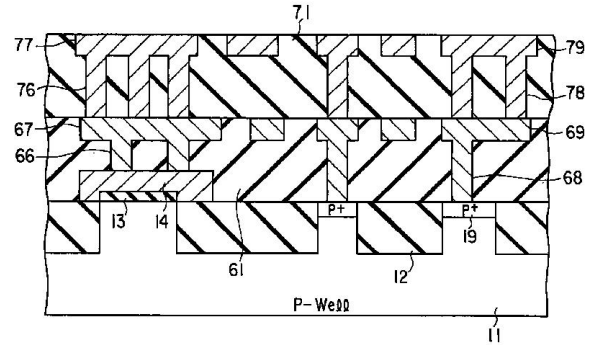
61: Interlayer Insulating Film
62: Connecting Holes
63: Interconnection Grooves
64: Dummy Connecting Holes
65: Dummy Interconnection Grooves
66: In-hole Functional Interconnecting
67: In-groove Functional Interconnecting Portions
68: In-hole Dummy Interconnecting Portions
69: In-groove Dummy Interconnecting Portions

[FIG. 15]



71層間絶縁膜 72接続孔 73配線溝
74ダミー接続孔 75ダミー配線溝

[FIG. 16]



76孔内機能配線部 77溝内機能配線部
78孔内ダミー配線部 79溝内ダミー配線部

- 71: Interlayer Insulating Film
- 72: Connecting Holes
- 73: Interconnection Grooves
- 74: Dummy Connecting Holes
- 75: Dummy Interconnection Grooves
- 76: In-hole Functional Interconnecting
- 77: In-groove Functional Interconnecting Portions
- 78: In-hole Dummy Interconnecting Portions
- 79: In-groove Dummy Interconnecting Portions