

Chemical Mechanical Polishing in Silicon Processing

Volume Editors

Shin Hwa Li

Robert O. Miller



SEMICONDUCTORS AND SEMIMETALS VOLUME 63

Treatise Editors: Robert K. Willardson and Eicke R. Weber

Semiconductors and Semimetals

A Treatise

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Contents

PREFACE	xi
LIST OF CONTRIBUTORS	xiii

Chapter 1 Introduction 1

Frank B. Kaufman

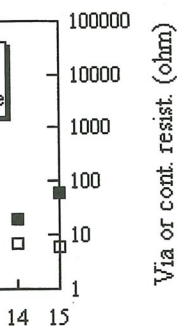
I. CMP: A UNIQUE AND EVOLVING SEMICONDUCTOR FABRICATION TECHNOLOGY—PAST, PRESENT, AND FUTURE	1
1. <i>The History and Development of CMP as a Unique Semiconductor Fabrication Technology</i>	2
2. <i>CMP: The Current State of the Art</i>	3
3. <i>The Evolution of CMP Technology into the New Millenium</i>	3

Chapter 2 Equipment 5

Thomas Bibby and Karey Holland

I. INTRODUCTION	5
II. CMP EQUIPMENT DESIGN EVOLUTION	8
1. <i>Throughput Improvement</i>	9
2. <i>First-Generation Polishers</i>	10
3. <i>Second-Generation Polishers</i>	11
4. <i>Third-Generation CMP Equipment</i>	13
III. CARRIERS	16
1. <i>Gimbale Carriers</i>	20
2. <i>Floating Carriers—The Use of Hydrostatic Pressure</i>	21
3. <i>Linear Polisher and Pressure Control</i>	23
IV. PLATENS	24
1. <i>Temperature Control</i>	24
2. <i>Orbital Polisher and Direct Slurry Delivery</i>	25
V. PAD CONDITIONING	25
VI. CMP EQUIPMENT INTEGRATION	30
1. <i>Post-CMP Cleaning</i>	30
2. <i>Integrated Metrology</i>	35
3. <i>Slurry Reprocessing</i>	37

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2. OXIDE EROSION

Global oxide erosion can be caused by two factors: the unintentional erosion due to poor selectivity between metal (for W, TiN, and Ti) and oxide CMP and the intentional erosion due to the additional step of oxide buffing for the purpose of eliminating defects (primarily scratches) generated by the W CMP process. Nowadays, we rarely see that the erosion is caused by poor selectivity. Usually, as long as the selectivity between W and oxide is greater than 10, its impact on oxide erosion is insignificant. This is easily accomplished, since most W slurries are acidic and oxide must be polished in a basic slurry. The global oxide erosion observed currently is most likely the result of oxide buffing process. Although global oxide erosion is not detrimental to integrated circuit production, it is troublesome for (1) ILD thickness control and (2) defectivity monitoring, because oxide erosion may cause surface color variation, which impairs defectivity visibility.

Local oxide erosion is associated with dishing in damascene process, as discussed in the following.

3. POLISH RATE AND UNIFORMITY

Instability in polish rate and nonuniformity in W CMP are also daily problems, as they are in oxide CMP. They are attributable to the quantity of consumables, tool maintenance, and the like; however, their impact on products is not as direct as in oxide CMP, because the W CMP process is self-limited by the metal-oxide selectivity (selectivity of tungsten to oxide greater than 10 is required). The polish time in W CMP is intentionally set up longer than necessary to overpolish by 25%. As a result, even if the polish rate is unstable, as long as the W, TiN, and Ti layers can be polished completely, there is no concern with overpolishing. However, if the polish rate is too low, 25% overpolish is not enough, and metal residuals may stay on the surface, eventually causing short circuits.

The nonuniformity problem in W CMP is also not detrimental. Again, as long as the W CMP can stop at oxide film, it does not matter if the metal at some areas is removed sooner or later.

VI. Other Problems

Some problems that are not classifiable into the preceding categories are considered in this section. These problems may occur occasionally, or they may appear only for certain applications.

1. MISSING ALIGNMENT MARK

A planarized surface is advantageous for photolithography in that the exposure of a pattern from a mask to the photoresist on a wafer can be better focused and less blurred; that is, little depth of focus latitude is required. On the other hand, it also has the disadvantage that, if the surface is too flat, the pattern underneath the planarized film cannot be aligned with the current mask. Two common examples of this problem are alignments after W CMP and STI CMP processes. The case of W CMP is illustrated in Fig. 23. On the left side of the figure are W plugs, and on the right side is a photolithographic alignment mark. Since the plug size is usually less than $1\text{ }\mu\text{m}$ in diameter, the plug can be completely filled by W. However, the alignment mark has a width of 5 to $10\text{ }\mu\text{m}$, so that after the W deposition, its trench is not filled. On the alignment mark, the surface is intentionally left nonplanarized, so that after the metal deposition, at photolithography, the photostepper can discern the alignment mark due to the nonplanarity. Several things can happen to make this fail. If the W deposited thickness is large enough, then after W CMP, the surface at the alignment can be planarized. Then, after the metal deposition, since the metal film is opaque, the alignment mark is too obscure to be seen by the stepper. Even if nonplanarity remains but the step abruptness has been reduced, after the metal deposition, the alignment mark image can be lost in the noise

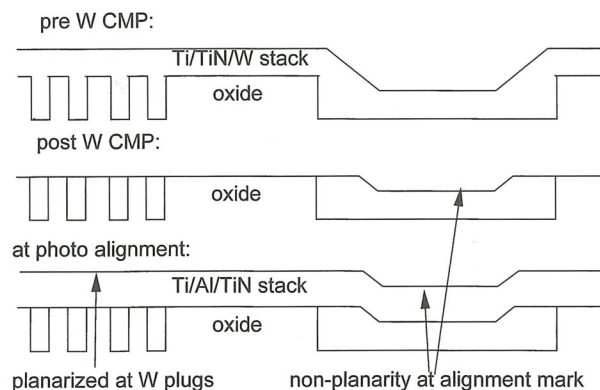


FIG. 23. Illustration of the nonplanarity at the photoalignment mark required for photolithography. This nonplanarity can be lost if the W deposited thickness prior to W CMP is too large or if nonplanarity exists but is insufficient due to the step abruptness having been smeared out. For the former, the surface at the alignment mark will be planarized after CMP; for the latter, after metal deposition, the image of the alignment mark can be obscured by noise due to the grainy metal surface.

generated by the grainy metal surface, and the alignment will fail the subsequent overlay inspection.

The same is true for the STI process, because after the CMP and the nitride strip, polysilicon is deposited. Polysilicon is also an opaque material, and if the nonplanarity is not present or reduced, the stepper cannot locate the alignment mark to align the polysilicon pattern to the STI pattern.

2. DISHING

Basically, dishing is defined as the percentage of the maximum recess to the nominal depth of the filling material in a plug (zero-dimensional feature), in a trench (one-dimensional feature), or in a well (two-dimensional feature). The severity of dishing is dependent on the material and the size of the structure. For the STI process, the material in a trench (or a well) is oxide, which is refractory, and dishing is hardly a problem even though the area of the trench or well is several hundreds of microns square. Similarly, for the W CMP with the plug application, since the size of the plug is small (less than $1\text{ }\mu\text{m}$), there is also no dishing problem. For W CMP in a damascene application, however, dishing is significant [25]. Figure 24 shows

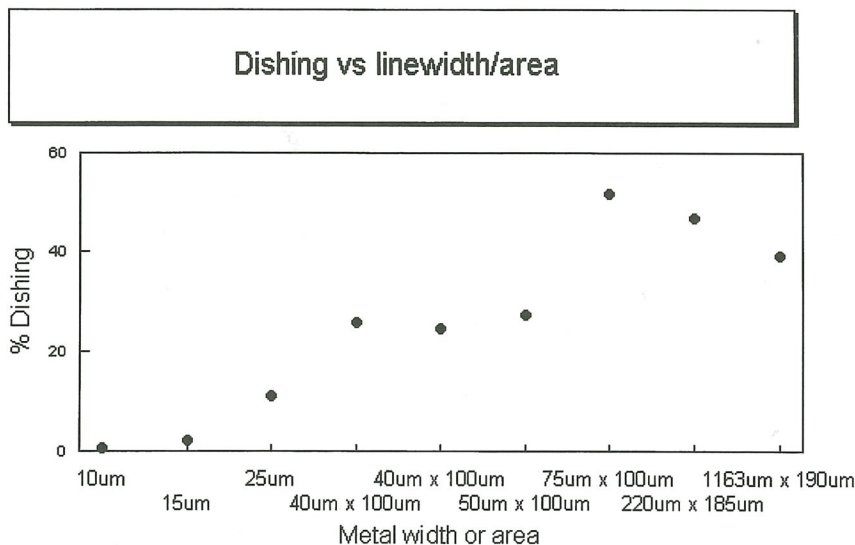


FIG. 24. Metal linewidth and area dependence of dishing for W CMP. Note: the x axis is not continuous, but represents various pattern features.

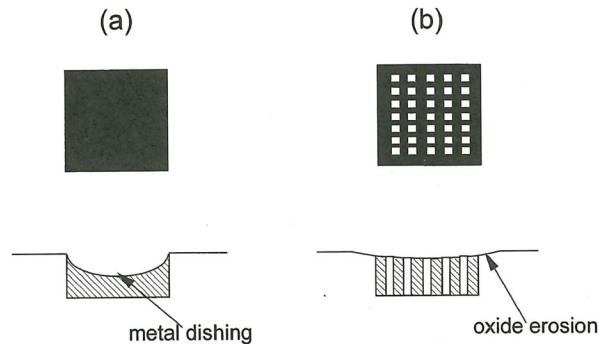


FIG. 25. Probe pad structure (a) without and (b) with oxide studs in the two-dimensional wells. The latter can be used to reduce dishing. However, local oxide erosion may be still a problem.

a metal linewidth or area dependence of the dishing. As we can see, as the size increases, more dishing is present. For two-dimensional features, we observe that amount of dishing is inversely related to perimeter; for instance, the dishing of a square-shaped pad is worse than that of a rectangle-shaped pad if their areas are the same. To reduce dishing, several things can be done. First, the down force of W CMP can be reduced. This will reduce the polish rate also, but higher platen speed can be used to compensate the rate loss. Second, a harder polish pad can be used rather than a soft pad. A harder pad works better, because it provides a better conformity, so that the pad will not push into the metal regions. When a harder pad (IC1000-type, for example) is used, however, more pad conditioning is required.

Dishing can be also reduced by adding oxide studs in the two-dimensional wells (see Fig. 25). Since the two-dimensional well structures are usually probe pads for electrical measurements, the addition of oxide studs will not affect the pad function as long as the test probe can still touch metal materials. Although this method can reduce dishing, local oxide erosion may still exist. The mechanism of local oxide erosion due to dishing is still unclear at this point of time [26].

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