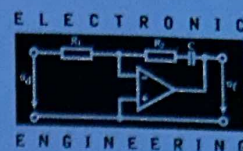


THE #1 BOOK IN THE INDUSTRY —
COMPLETELY REVISED AND UPDATED



Microchip Fabrication

Fifth Edition

- ✓ NEW! 300-mm wafer processing
- ✓ NEW! Nanotechnology processes
- ✓ NEW! Flip-chip and bump packaging processes
- ✓ NEW! Green processing
- ✓ NEW! Next Generation Lithography (NGL)

Peter Van Zant

NOYCE PATENT U.S. PATENT No. 2,981,877

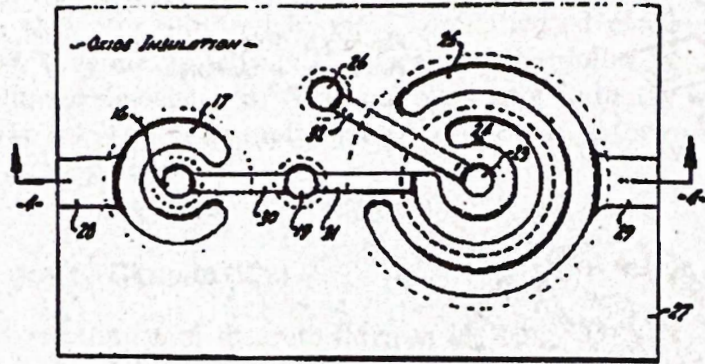
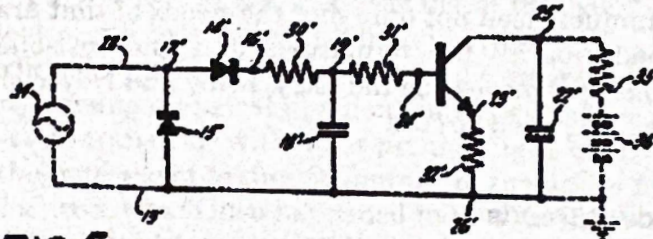

FIG-3

FIG-4

FIG-5

INVENTOR
ROBERT N. NOYCE
BY *Levinson & Kalla*
ATTORNEYS

Figure 1.7 Noyce IC patent. (Courtesy of Semiconductor Reliability News, June 2003.)

called the *feature size* and is usually expressed in microns or nanometers. A micron is 1/1,000,000 of a meter or about 1/100 the diameter of a human hair. A nanometer is 1/1,000,000,000 of a meter. A more specific tracker of semiconductor devices is *gate width*. Transistors are composed of three parts, one of which acts to allow the passage of cur-

rent. In today's technology, the most popular transistor is the metal-oxide-semiconductor (MOS) structure. The controlling part is called the *gate*. Smaller gate widths drive the industry by producing smaller and faster transistors and more dense circuits. Currently, the industry is driving to the 90-nm gate width, with projections in the *International Technology Roadmap* for semiconductors projecting 22 nm size in 2016.³

In 1965, Gordon Moore, a founder of Intel, noted that the number of transistors on a chip were doubling every 18 months. He published the observation, which was immediately dubbed *Moore's law*. Industry observers have used this law to predict the future density of chips. Over the years, it has proven very accurate and now drives technical advances (Fig. 1.8). It is the basis of the *International Technology Roadmap for Semiconductors*, developed by the Semiconductor Industry Association.

Circuit density is tracked by the *integration level*, which is the number of components in a circuit. Integration levels (Fig. 1.9) range from small scale integration (SSI) to ultra large scale integration (ULSI). ULSI chips are sometimes referred to as very very large scale integration (VVL SI). The popular press calls these newest products *megachips*.

Year	Transistor count
1978	29,000
1982	275,000
1985	1,200,000
1991	3,100,000
1993	7,500,000
1997	9,500,000
2001	55,000,000

Figure 1.8 Source: Intel Corporation.

Level	Abbreviation	# Components per Chip
Small Scale Integration	SSI	2 - 50
Medium Scale Integration	MSI	50 - 5000
Large Scale Integration	LSI	5000 - 100,000
Very Large Scale Integration	VLSI	Over 100,000 - 1,000,000
Ultra Large Scale Integration	ULSI	> 1,000,000

Figure 1.9 IC integration table.

Library of Congress Cataloging-in-Publication Data

Van Zant, Peter.

Microchip fabrication / Peter Van Zant.—5th ed.

p. cm.

Includes index.

ISBN 0-07-143241-8

1. Semiconductors—Design and construction. 2. Integrated circuits—Design and construction. I. Title.

TK7871.85.V36 2004

621.3815'2—dc22

2004040287

Copyright © 2004, 2000, 1997, 1984 by The McGraw-Hill Companies, Inc. All rights reserved. Printed in the United States of America. Except as permitted under the United States Copyright Act of 1976, no part of this publication may be reproduced or distributed in any form or by any means, or stored in a data base or retrieval system, without the prior written permission of the publisher.

3 4 5 6 7 8 9 10 IBT/IBT 1 9 8 7 6 5 4 3 2 1

ISBN 0-07-143241-8

The sponsoring editor for this book was Stephen S. Chapman and the production supervisor was Pamela Pelton. It was set in Century Schoolbook by J. K. Eckert & Company, Inc.

Printed and bound by IBT Global.

McGraw-Hill books are available at special quantity discounts to use as premiums and sales promotions, or for use in corporate training programs. For more information, please write to the Director of Special Sales, McGraw-Hill Professional, Two Penn Plaza, New York, NY 10121-2298. Or contact your local bookstore.

This book is printed on recycles, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

Information contained in this work has been obtained by The McGraw-Hill Companies, Inc. ("McGraw-Hill") from sources believed to be reliable. However, neither McGraw-Hill nor its authors guarantee the accuracy or completeness of any information published herein and neither McGraw-Hill nor its authors shall be responsible for any errors, omissions, or damages arising out of use of this information. This work is published with the understanding that McGraw-Hill and its authors are supplying information but are not attempting to render engineering or other professional services. If such services are required, the assistance of an appropriate professional should be sought.

Goal of Wafer Fabrication

The four stages of microchip manufacturing are materials preparation, crystal growth and wafer preparation, wafer fabrication, and packaging. The first two stages have been explored in Chapter 3. In this chapter, the fundamentals of stage 3, wafer fabrication, are explained.

Wafer fabrication is the manufacturing processes used to create the semiconductor devices in and on the wafer surface. The polished starting wafers come into fabrication with blank surfaces and exit with the surface covered with hundreds of completed chips (Fig. 4.1).

Wafer Terminology

A completed wafer is illustrated in Fig. 4.2. The regions of a wafer surface are:

1. Chip, die, device, circuit, microchip, or bar. All of these terms are used to identify the microchip patterns covering the majority of the wafer surface.
2. Scribe lines, saw lines, streets, and avenues. These areas are spaces between the chips that allow separation of the chip from the wafer. Generally, the scribe lines are blank, but some companies place alignment targets, or electrical test structures (see photomasking) in them.
3. Engineering die, test die. These chips are different from the regular device or circuit die. They contain special devices and circuit elements that allow electrical testing during the fabrication processing for process and quality control.
4. Edge chips. The edges of the wafer contain partial chip patterns that are wasted space. Larger chips on the same diameter wafer

Circuit/devices formed in
and on wafer surface.
Individual chips electronically
tested (wafer sort)

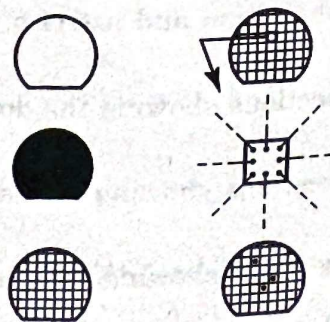


Figure 4.1 Wafer fabrication and wafer sort.