

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.,
Petitioner

IPR2025-01444
U.S. Patent No. 7,547,584

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

TABLE OF CONTENTS

PETITIONER’S EXHIBIT LIST	5
I. INTRODUCTION	6
II. GROUNDS FOR STANDING.....	8
III. NOTE.....	8
IV. SUMMARY OF THE ’584 PATENT	8
V. PROSECUTION HISTORY	9
VI. EFFECTIVE PRIORITY DATE OF THE ’584 PATENT	10
VII. LEVEL OF ORDINARY SKILL IN THE ART.....	11
VIII. CLAIM CONSTRUCTION	11
IX. RELIEF REQUESTED	12
X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE....	12
A. Challenged Claims	12
B. Statutory Grounds for Challenges	12
C. Ground 1: Claims 1 and 3-5 are Obvious over Matsunaga.....	14
1. Summary of Matsunaga	14
2. Claim 1	16
3. Claim 3	36
4. Claim 4.....	37
5. Claim 5	37
D. Ground 2: Claim 2 is Obvious over Matsunaga and Jaso	37

1.	Summary of Jaso	37
2.	Obviousness Combination Matsunaga and Jaso	38
3.	Claim 2	41
E.	Ground 3: Claim 6 is Obvious over Matsunaga and Appel	43
1.	Summary of Appel	43
2.	Obviousness Combination Matsunaga and Appel	43
3.	Claim 6	45
F.	Ground 4: Claims 1 and 3-5 are Obvious over Matsunaga and Wolf	48
1.	Summary of Wolf	48
2.	Obviousness Combination Matsunaga and Wolf	48
6.	Claim 1	50
3.	Claim 3	59
4.	Claim 4	59
5.	Claim 5	59
G.	Ground 5: Claim 2 is Obvious over Matsunaga, Wolf, and Jaso	60
H.	Ground 6: Claim 6 is Obvious over Matsunaga, Wolf, and Appel	60
I.	Ground 7: Claims 1 and 3-6 are Obvious over Eriguchi, Quirk, and Wolf	60
1.	Summary of Eriguchi	60
2.	Summary of Quirk	62
3.	Obviousness Combination Eriguchi and Quirk	62

4.	Obviousness Combination Eriguchi and Wolf	65
5.	Claim 1	66
6.	Claim 3	87
7.	Claim 4	87
8.	Claim 5	88
9.	Claim 6	88
XI.	CONCLUSION.....	90
XII.	MANDATORY NOTICES	91
A.	Real party-in-interest.....	91
B.	Related matters	91
C.	Lead and back-up counsel and service information.....	91
	Certificate of Word Count	92
	Certificate of Service	93

PETITIONER’S EXHIBIT LIST

Ex.1001	U.S. 7,547,584
Ex.1002	Prosecution History of U.S. 7,547,584
Ex.1003	Declaration of Stanley Shanfield, Ph.D. under 37 C.F.R. § 1.68
Ex.1004	Wolf S., Silicon processing for the VLSI Era, Volume 4 – Deep Submicron Process Technology (2002)
Ex.1005	Certified English Translation of JP Publication JPH1174523A to Matsunaga (“Matsunaga”)
Ex.1006	JP Publication JPH1174523A to Matsunaga (“Matsunaga”)
Ex.1007	U.S. Patent Publication No. 2005/0006707 to Eriguchi <i>et al.</i> (“Eriguchi”)
Ex.1008	U.S. Patent No. 5,998,282
Ex.1009	U.S. Patent No. 6,093,631 to Jaso <i>et al.</i> (“Jaso”)
Ex.1010	U.S. Patent No. 7,241,676
Ex.1011	U.S. Patent Publication No. 2010/0108652A1
Ex.1012	Quirk M. and Serda J., Semiconductor Manufacturing Technology (2001)
Ex.1013	Li S.H. and Miller R.O., Chemical Mechanical Polishing in Silicon Processing (2000)
Ex.1014	Van Zant, Microchip Fabrication, 3rd Ed. (1997)
Ex.1015	Van Zant, Microchip Fabrication, 5th Ed. (2004)
Ex.1016	U.S. Patent Publication No. 2005/0233564A1
Ex.1017	U.S. Patent No. 5,605,861 (“Appel”)
Ex.1018	Declaration of Ingrid Hsieh-Yee, Ph.D. under 37 C.F.R. § 1.68

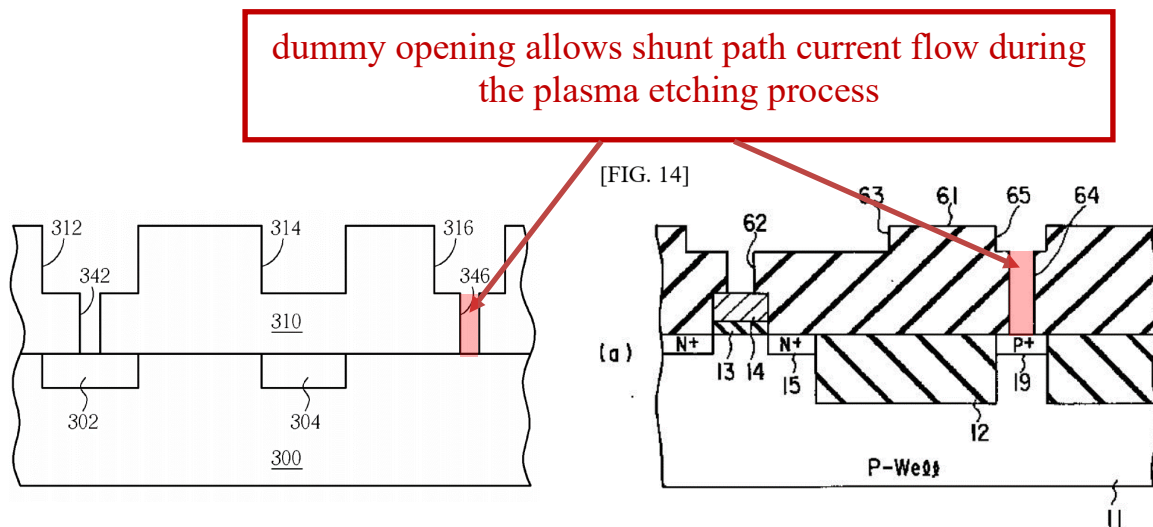
I. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311, 314(a), and 37 C.F.R. § 42.100, Taiwan Semiconductor Manufacturing Company Ltd. (“Petitioner”) respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. §103(a) claims 1-6 (hereinafter, the “Challenged Claims”) of U.S. 7,547,584 (the “’584 patent,” Ex.1001).

The ’584 patent describes manufacturing processing for integrated circuits including MOS transistors. Ex.1001, 4:12-15, 7:12-13. The only feature that the ’584 patent purports to add concerns processing to prevent stray current from damaging internal structures during fabrication. Since stray current is likely to travel through device regions, the ’584 patent proposes to make an alternative shunt pathway for the stray current to flow. This alternative pathway is a “dummy” non-interconnect opening. By providing an alternative shunt path for the stray current to flow, this dummy opening reduces charge damage to the integrated circuit during fabrication (and specifically, during plasma processing, a fabrication step which generates potentially harmful stray currents). Ex.1001, 4:35-39.

The inventors of the ’584 patent, however, were not the first to consider or use a dummy non-interconnect opening during plasma processing for the purpose of providing a shunt path that reduces charge damage. The cited primary reference Matsunaga, for example, teaches manufacturing processing that uses dummy

openings when forming a MOS transistor. Ex.1005, [0019], [0054]-[0058]. And just like the '584 patent's shunt path, illustrated below in a side-by-side comparison, Matsunaga's "electric charges...[are supplied] through the dummy regions to the semiconductor substrate...to prevent charging damage in the plasma processes." Ex.1005, [0019].



'584 patent (Ex.1001), FIG. 9.

Matsunaga (Ex.1005), FIG. 14(a).

Therefore, this Petition presents a reasonable likelihood that at least one claim of the '584 patent is unpatentable. Indeed, given the substantially overlapping disclosure in the prior art, this Petition presents an even stronger compelling-merits challenge that is a higher standard than the reasonable likelihood required for the institution of an IPR. *OpenSky Industries, LLC v. VLSI Technology, LLC*, IPR2021-01064, Paper 102 at 49 (P.T.A.B. Oct. 4, 2022) (precedential).

II. GROUNDS FOR STANDING

Petitioner certifies that the '584 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. NOTE

Petitioner cites to exhibits' original page numbers. Emphasis in quoted material has been added. Claim terms are presented in "*italics*."

IV. SUMMARY OF THE '584 PATENT

The '584 patent relates to processing of integrated circuits, including a MOS transistor. Ex.1001, 6:11-15, Abstract. The '584 patent's Figures 7-10 disclose processing for "reducing charging damage to integrated circuits during plasma etching utilized in a dual damascene process." Ex.1001, 6:24-27. A damascene process is one in which etches are made into a layer. A "dual damascene" process is one in which etches are made into a layer, and then additional etches are made over or into the first set of etches. This is illustrated in the '584 Patent, Figures 7-10 below, with the elements 312, 314, and 316 corresponding to a first set of etches and 332, 336, 342, and 346 corresponding to a second set of etches. Ex.1003, ¶¶36-39.

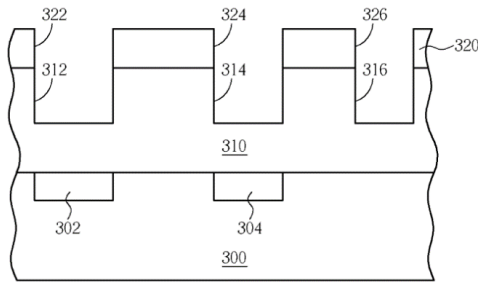


Fig. 7

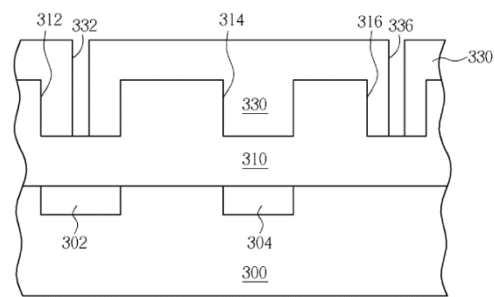


Fig. 8

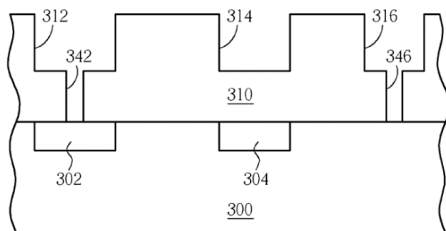


Fig. 9

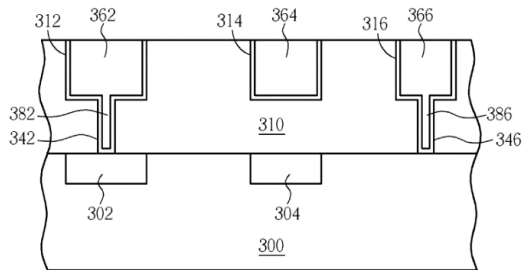


Fig. 10

Ex.1001, Figs. 7-10.

Dr. Shanfield also provides a “Technology Background” section, where he explains that “since the 1990’s dual damascene techniques were used for semiconductor manufacturing” and that this process “draws its name from the ancient art of metal inlaying.” Ex.1003, ¶¶26-35.

V. PROSECUTION HISTORY

During prosecution, the Applicant amended independent claim 1 to recite an interconnect opening and a dummy, non-interconnect opening:

1. (Currently amended) A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:

providing a semiconductor substrate comprising thereon a number of integrated circuit dies, said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die, wherein said semiconductor substrate comprises thereon a dielectric layer;

forming a mask over said dielectric layer, said mask comprising ~~a first opening defining an interconnection pattern~~ an interconnect opening and a ~~second opening defining a dummy, non-interconnect pattern opening~~, wherein said ~~first and second openings~~ interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;

performing a plasma etching process to etch said dielectric layer through said ~~first interconnect opening~~ and ~~second~~ said dummy, non-interconnect openings of said mask, thereby forming an ~~interconnection~~ interconnect recessed ~~feature~~ trench and a ~~recessed-dummy feature~~ dummy recessed trench in said dielectric layer; and

filling said ~~interconnection-recessed feature~~ interconnect recessed trench and said ~~recessed-dummy feature~~ dummy recessed trench with conductive materials to form an ~~interconnection~~ interconnect feature and a dummy, non-interconnect feature, wherein said ~~interconnection feature~~ interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;

wherein second opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

Ex.1002, 47-61. In a subsequent response, the Applicant argued that the prior art does not teach forming dummy non-interconnect structures “concurrently” with the interconnect structures to reduce charge damage during a plasma etching. Ex.1002, 28-46. The Office subsequently issued a Notice of Allowance, allowing claims 1-6. Ex.1002, 17-20; Ex.1003, ¶¶41-42.

VI. EFFECTIVE PRIORITY DATE OF THE '584 PATENT

The '584 patent was filed on November 16, 2006, and claims priority, as a continuation-in-part (“CIP”), to U.S. Patent No. 7,176,051 (“the '051 Patent”),

which was filed May 27, 2005. *See* Ex.1001. Determining whether the '584 patent is entitled to the earlier priority date of the '051 patent is unnecessary in this proceeding since all cited and relied-upon prior art predates May 27, 2005.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in The Art (“POSITA”) in May 2005 would have had a working knowledge of the semiconductor fabrication art that is pertinent to the '584 patent. A POSITA would have had a master’s degree in electrical engineering, physics, chemistry, materials science, or related fields, and three years of work experience in semiconductor manufacturing, including photolithography processing transistors. Additional graduate education could substitute for work experience, and additional work experience/training could substitute for formal education. Ex.1003, ¶¶23-25.

VIII. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. § 42.100(b). Petitioner submits that, for the purposes of this proceeding and the grounds presented herein, no claim term requires express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); Ex.1003, ¶¶43-44; Ex.1018, ¶¶73-98.

IX. RELIEF REQUESTED

Petitioner asks that the Board institute a trial for IPR and cancel the Challenged Claims in view of the analysis below.

X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenged Claims

Petitioner challenges claims 1-6, which are all claims of the '584 patent.

B. Statutory Grounds for Challenges

Grounds	Challenged Claims	35 U.S.C. §	References
1	1, 3-5	103	Matsunaga
2	2	103	Matsunaga, Jaso
3	6	103	Matsunaga, Appel
4	1, 3-5	103	Matsunaga, Wolf
5	2	103	Matsunaga, Wolf, Jaso
6	6	103	Matsunaga, Wolf, Appel
7	1, 3-6	103	Eriguchi, Quirk, Wolf

- The textbook titled “Silicon Processing for the VLSI Era,” by Wolf (“**Wolf**,” Ex.1004) was published in 2002. Dr. Hsieh-Yee provides evidence that Wolf was publicly available more than one year before the '584 patent's earliest claimed priority date. Ex.1018, ¶¶20-49.
- Japan Patent Publication No. 11-74523A to Matsunaga (Ex. 1005, Ex.1006,

“**Matsunaga**”) was published on March 16, 1999.

- U.S. Publication No. 2005/0006707 to Eriguchi *et al.* (Ex.1007, “**Eriguchi**”) was filed on June 2, 2004, and published on January 13, 2005.
- U.S. Patent No. 6,093,631 to Jaso *et al.* (Ex.1009, “**Jaso**”) was filed on January 15, 1998, and issued on July 25, 2000.
- The textbook titled “Semiconductor Manufacturing Technology,” by Quirk *et al.* (“**Quirk**,” Ex.1012) was published in 2001. Dr. Hsieh-Yee provides evidence that Quirk was publicly available more than one year before the ’584 patent’s earliest claimed priority date. Ex.1018, ¶¶50-72.
- U.S. Patent No. 5,605,861 to Appel (Ex.1017, “**Appel**”) was filed on May 5, 1995, and issued on February 25, 1997.

Wolf and Quirk are prior art under at least Pre-AIA 35 U.S.C. § 102(b).

Matsunaga, Jaso, and Appel are prior art under at least Pre-AIA 35 U.S.C.

§§ 102(a) and 102(b). Eriguchi is prior art at least under at least Pre-AIA 35 U.S.C.

§§ 102(a) and 102(e).¹

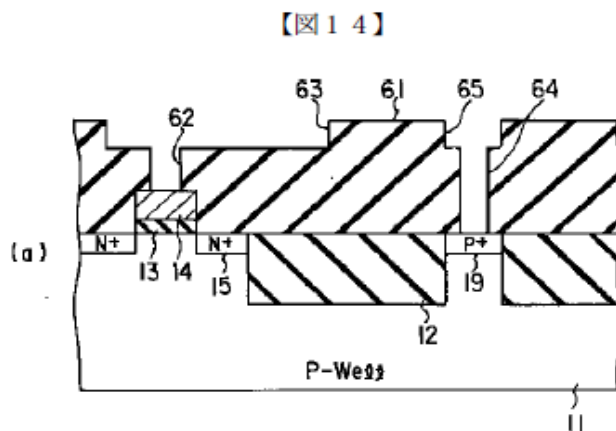
¹ Petitioner’s § 103 obviousness grounds rely on the teachings of the references and not on a physical incorporation. *See In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012); Ex.1003, ¶¶45-49.

Petitioner also cites additional prior art as evidence of the background knowledge of a POSITA. *See Yeda Research v. Mylan Pharm. Inc.*, 906 F.3d 1031, 1041-1042 (Fed. Cir. 2018) (affirming the use of “supporting evidence relied upon to support the challenge”); 37 C.F.R. § 42.104(b); *see also K/S HIMPP v. Hear-Wear Techs., LLC*, 751 F.3d 1362, 1365-66 (Fed. Cir. 2014).

C. Ground 1: Claims 1 and 3-5 are Obvious over Matsunaga

1. Summary of Matsunaga

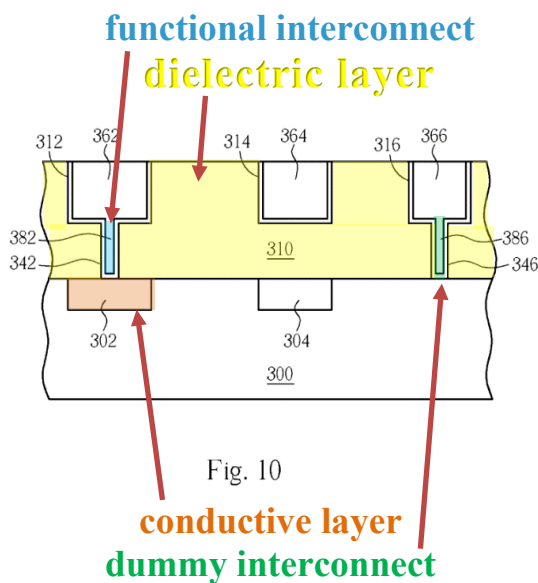
Like the '584 patent, Matsunaga discloses a method for forming integrated circuits (e.g., microprocessor circuits) comprising MOS transistors. Ex.1005, [0028]-[0029], [0055], [0058], Figs. 1, 12, 14-15. Matsunaga's Figure 14 (a) below illustrates that connecting hole 62 and dummy connecting hole 64 are “formed... simultaneously.” Ex.1005, [0019]- [0029], [0055]-[0056]; Ex.1003, ¶¶50-56.



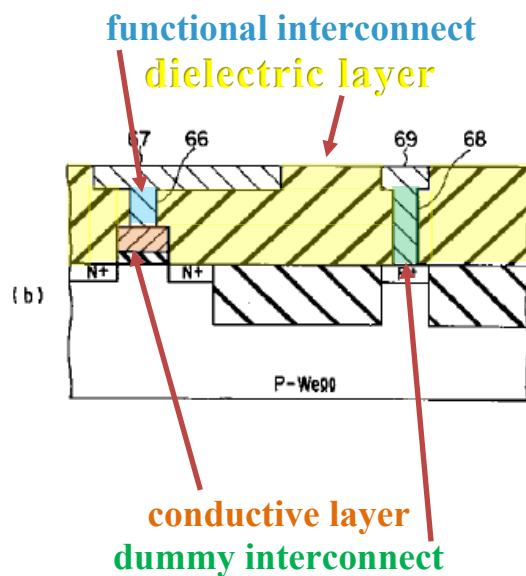
In the above figure, the dummy connecting hole 64 provides alternative path for current discharge during an RIE plasma etching, “making it possible to prevent

charging damage.” Ex.1005, [0009], [0055]-[0056]; *see also* Ex.1005, [0019]; Ex.1003, ¶51.

As shown below in a side-by-side comparison, the '584 patent's Figure 10 and Matsunaga's Figure 14 (b) have the same basic arrangement, namely: **(1)** a semiconductor substrate (Ex.1001, 6:28-30; Ex.1005, [0029]); **(2)** a dielectric layer (Ex.1001, 6:31-33; Ex.1005, [0055]); **(3)** a functional interconnect electrically connected to a conductive layer (Ex.1001, 7:3-11; Ex.1005, [0057]); and **(4)** a dummy interconnect, which is not used in circuit operation, that is grounded to the substrate (Ex.1001, 7:3-11; Ex.1005, [0029], [0057]). Ex.1003, ¶¶52-54.



Ex.1001, Fig. 10 (annotated).



Ex.1005, Fig. 14 (b) (annotated).

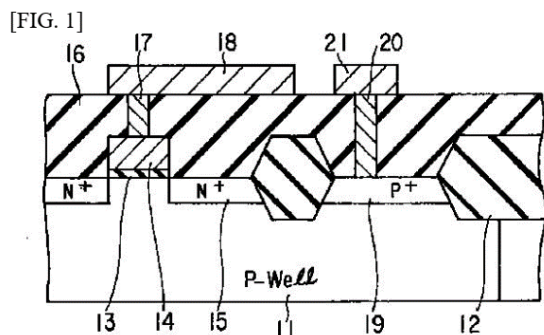
2. Claim 1

[1.0] A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising

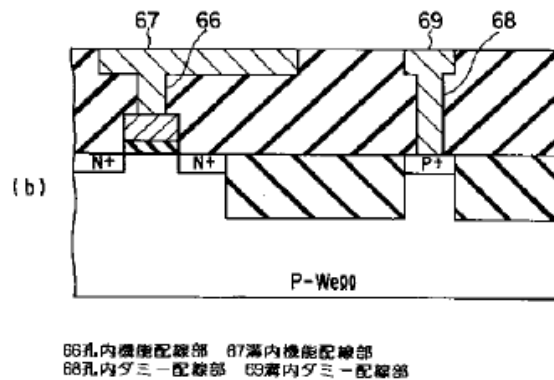
First, Matsunaga teaches a “method for reducing charging damage...during semiconductor manufacturing.” Matsunaga discloses a “manufacturing method...that is able to prevent charging damage by a plasma process.”

Ex.1005, [0009]; *see also* Ex.1005, [0019]; Ex.1003, ¶¶57-58.

Second, Matsunaga manufactures “integrated circuits” such as “MOS transistors,” illustrated at Figures 1 and 14 reproduced below. Ex.1005, [0055]; Ex.1003, ¶59.

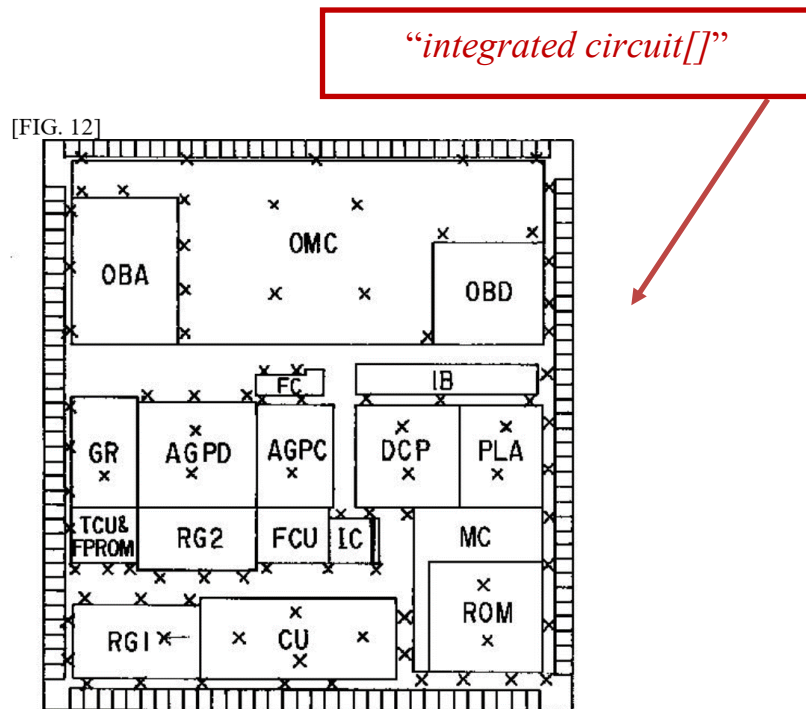


Ex.1005, FIG. 1.



Ex.1005, FIGS. 14 (b).

Additionally, Matsunaga in the context of Figure 12 discloses “a microprocessor circuit” that includes MOS transistors. Ex.1005, [0053]; Ex.1003, ¶60.



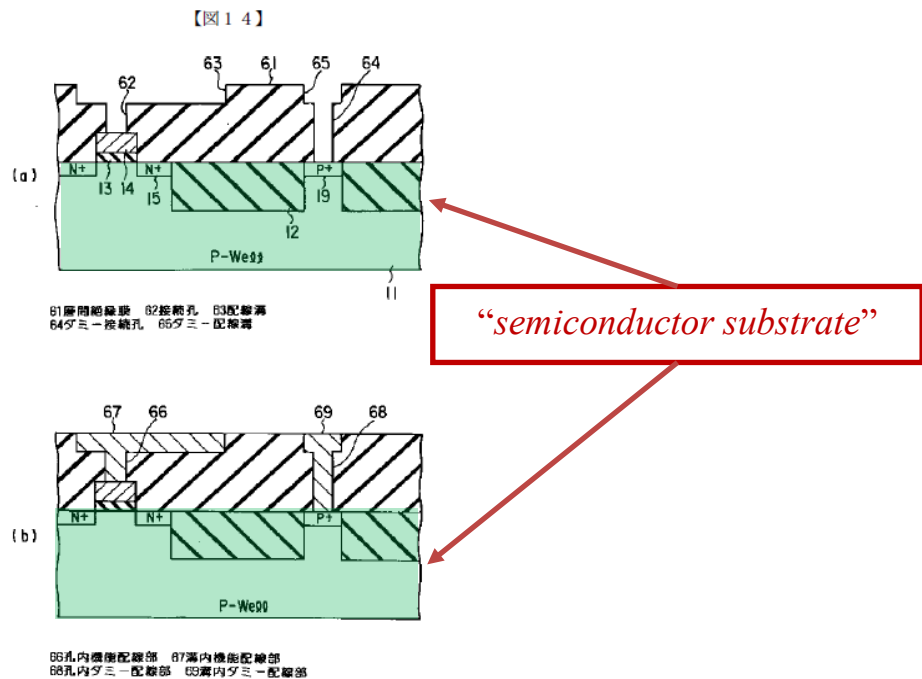
Ex.1005, FIG. 12 (annotated).

A POSITA would have understood that the illustrated microprocessor circuit includes one or more MOS transistors disclosed in the context of other figures.

Ex.1003, ¶61. Matsunaga’s circuit is “formed on a primary surface side of a semiconductor substrate.” Ex.1005, [0028]. It would have been obvious to a POSITA that Matsunaga’s microprocessor circuit is formed on a semiconductor substrate that includes a plurality of other identical microprocessor circuits, in line with conventional and well-known silicon wafer manufacturing processing techniques. Ex.1012, 6, Figure 1.5. Ex.1003, ¶63. A plurality of Matsunaga’s microprocessor circuits on a semiconductor substrate corresponds to the claimed “integrated circuits.” Ex.1003, ¶¶62-64.

[1.1.1] providing a semiconductor substrate comprising thereon a number of integrated circuit dies,

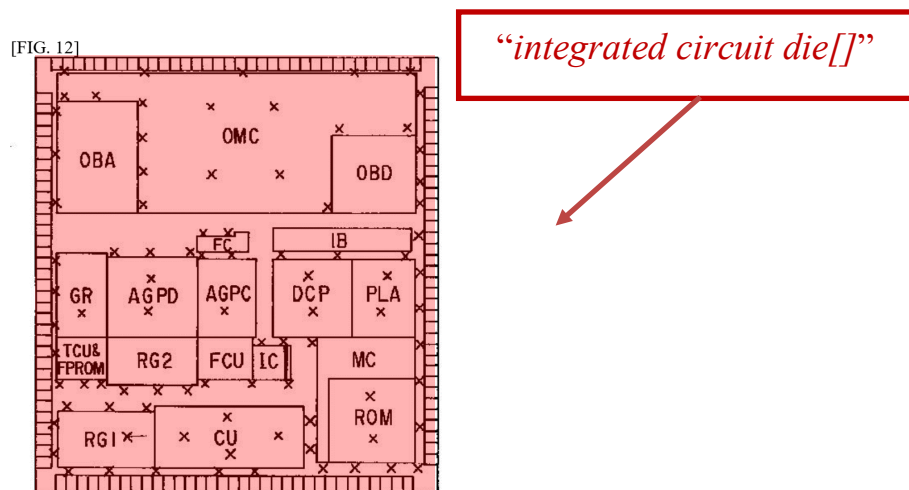
First, Matsunaga discloses “providing a semiconductor substrate” by teaching that its device is “formed on a primary surface side of a semiconductor substrate” and that the device illustrated at Figure 1 “is formed in a silicon substrate.” Ex.1005, [0028]-[0029], Claim 1 (“...semiconductor substrate...”). A POSITA would have understood that Matsunaga’s “silicon substrate” is a “semiconductor substrate.” Ex.1012, 4. In Matsunaga’s Figure 14 (reproduced below), “structural elements that are substantially identical or corresponding to those in the first embodiment, depicted in FIG. 1, are assigned identical numbers, and detailed explanations thereof will be omitted.” Ex.1005, [0054].



Ex.1005, FIGS. 14 (a) (b) (annotated).

Accordingly, the device illustrated at Figures 14(a), (b), which has a silicon substrate, is a “*semiconductor substrate*” as claimed. Ex.1003, ¶¶65-68.

Second, consistent with the analysis at [1.0], it would have been obvious for Matsunaga’s semiconductor substrate to have “*thereon a number of integrated circuit dies.*” A POSITA would have understood that the “microprocessor circuit” (“*integrated circuit*”) illustrated at Figure 12, reproduced below, corresponds to a “chip” or “die.” Ex.1005, [0053]; Ex.1012, 6 (“**The chip is also referred to as a die.**”), 8 (“The fabrication of **microchips...integrated circuits.**”); Ex.1003, ¶69.



Ex.1005, FIG. 12 (annotated).

It would have been obvious to a POSITA that Matsunaga’s semiconductor substrate accommodates a plurality of microprocessor circuits (which are chips or dies), in which case it would be obvious for Matsunaga’s semiconductor substrate to contain multiples of such dies. *See, In reHarza*, 274 F.2d 669, 124 USPQ 378

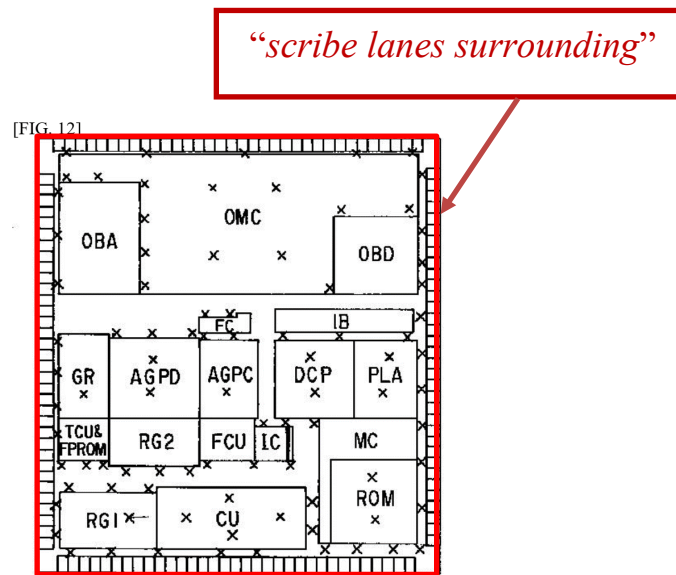
(CCPA 1960) (holding that mere duplication of parts has no patentable significance unless a new and unexpected result is produce); Ex.1003, ¶¶70-71.

Thus, Matsunaga renders obvious that the semiconductor substrate comprises “*a number of integrated circuit dies.*”

[1.1.2] said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,

First, as analyzed at [1.1.1] Matsunaga renders obvious a plurality of microprocessor circuit dies (“*integrated circuit dies*”). Ex.1003, ¶¶72-73.

Second, it would have been obvious for the microprocessor circuit dies to be “*separated from each other by scribe lanes surrounding each*” microprocessor circuit die. As shown below at Figure 12, Matsunaga’s microprocessor circuit die has a straight cutline on the perimeter, which would have been understood by a POSITA to correspond to “*scribe lanes surrounding [] said integrated circuit die.*” See Ex.1004, 348-349; Ex.1008, 2:7-15, 3:63-66; Ex.1012, 9, 549, 575, Figures 1.3, 1.6, 20.5; Ex.1014, 101; Ex.1015, 72; Ex.1018, ¶¶99-143; Ex.1003, ¶74.



Ex.1005, FIG. 12 (annotated).

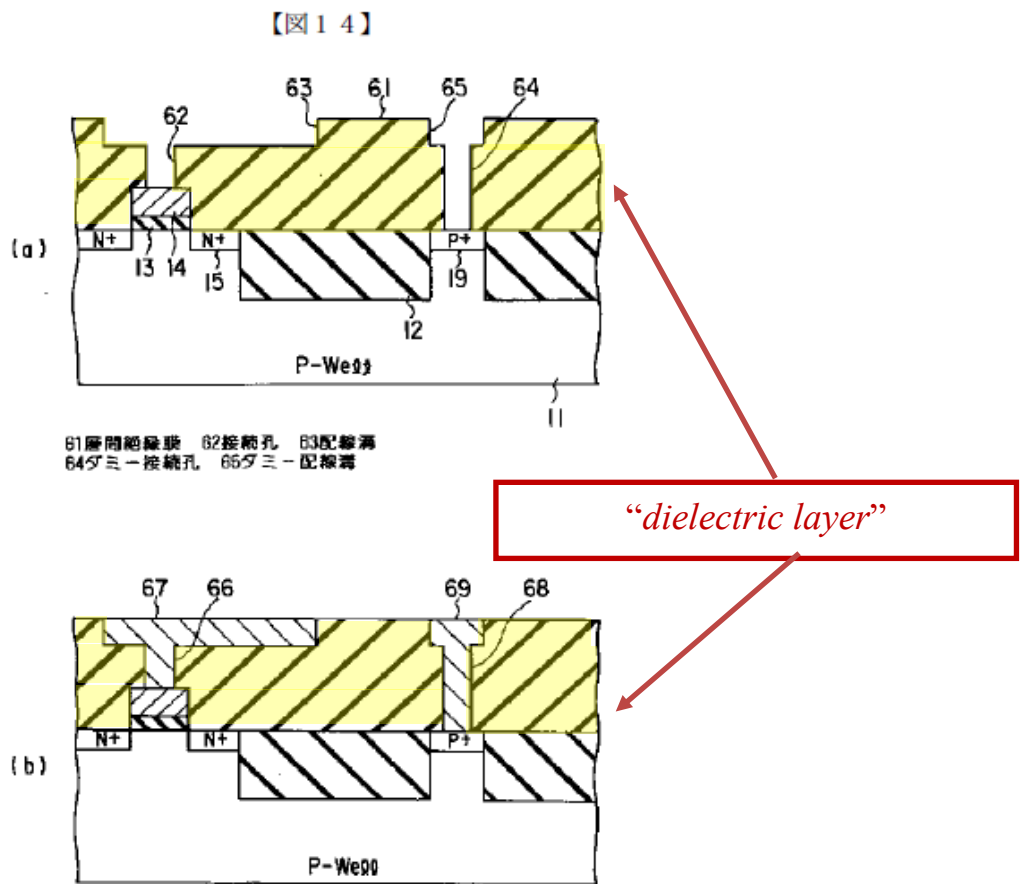
The '584 patent itself admits that the inventors did not conceive of using scribe lanes to separate integrated circuit dies from each other. Ex.1001, 1:59-2:1; Ex.1008, FIG. 3; Ex.1003, ¶75.

Furthermore, consistent with the analysis at limitations [1.0]-[1.1.1], it would have been obvious to a POSITA for a plurality of Matsunaga's microprocessor circuit chips or dies to be manufactured on a semiconductor substrate in accordance with well-known techniques, which would include using scribe lanes to surround and separate each microprocessor circuit chip or die so that they may later be cut out. Ex.1003, ¶¶76-78.

[1.1.3] wherein said semiconductor substrate comprises thereon a dielectric layer;

First, as analyzed at [1.1.1], Matsunaga discloses a semiconductor substrate (“said semiconductor substrate”). Ex.1003, ¶¶79-80.

Second, Matsunaga discloses that the semiconductor substrate comprises “a dielectric layer” by teaching that “an interlayer insulating film 61 is formed over a substrate whereon MOS transistors, or the like, are formed,” as illustrated below at Figure 14. Ex.1005, [0055]; Ex.1003, ¶81.



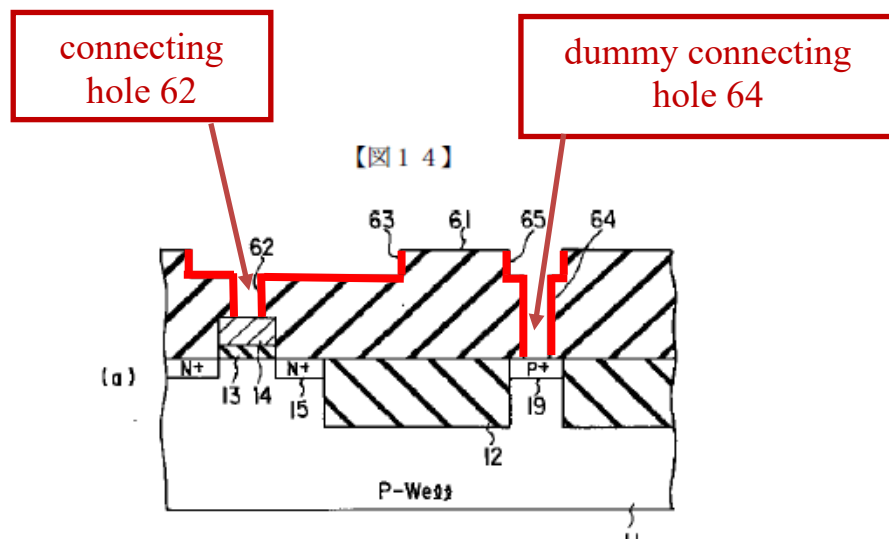
Matsunaga, FIGS. 14 (a) (b) (annotated).

It would have been understood that Matsunaga's interlayer insulator film 61 is a dielectric layer (e.g., silicon oxide or silicon nitride) as these terms are used interchangeably in semiconductor devices. *See e.g.*, Ex.1007, [0118] (“...**interlayer insulating film...[may be] silicon oxide films or silicon nitride films.**”); Ex.1009, 6:67 (“...**a silicon dioxide as the dielectric...**”); Ex.1014, 6, 141 (“**When dielectrics are used in electrical circuits or devices they are referred to as insulators.**”); *see also* Ex.1004, 639; Ex.1012, 696, Fig. 15-21; Ex.1010, 1:49-55; Ex.1018, ¶¶99-121; Ex.1003, ¶¶82-83.

[1.2.1] forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,

First, as analyzed at [1.1.3], Matsunaga discloses an interlayer insulating film 61 (“*dielectric layer*”). Matsunaga further discloses that “a connecting hole 62 and interconnection groove 63” are formed in the interlayer insulating film 61 “in the so-called dual damascene structure” and that “dummy connecting holes 64 and dummy interconnection grooves 65 are also formed at the same time.” Ex.1005, [0055]. Ex.1003, ¶¶84-85.

Matsunaga's Figure 14 (a), reproduced below, illustrates that its MOS transistor with a “dual damascene structure” (outlined in red) includes connecting hole 62 and dummy connecting hole 64. Ex.1003, ¶86.

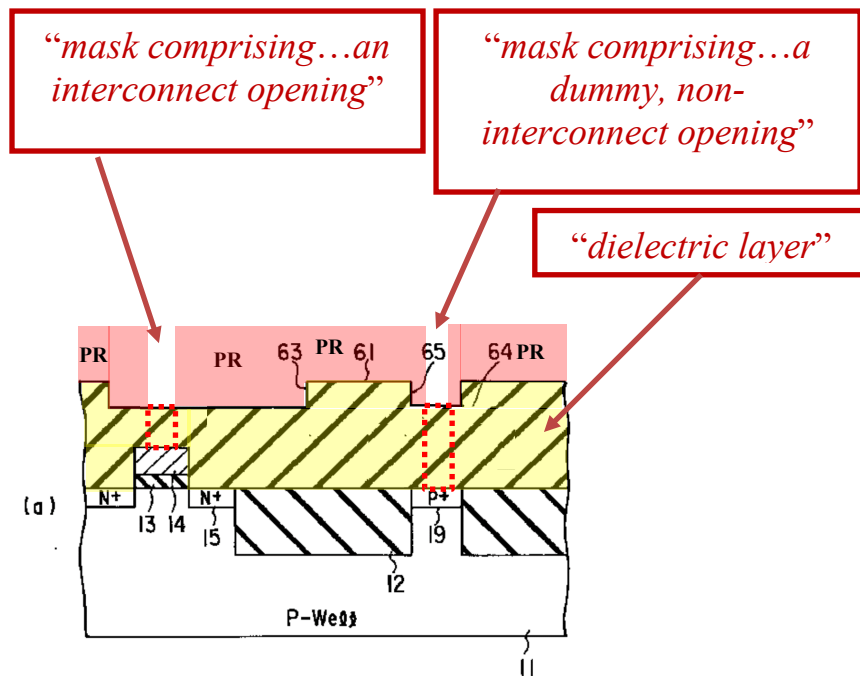


Ex.1005, FIG. 14 (a) (annotated).

Second, Matsunaga renders obvious “*forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening.*” Matsunaga discloses, relative to Figure 14, that its connecting hole 62 (*interconnect opening*) and dummy connecting hole 64 (*dummy, non-interconnect opening*) are “formed at the same time through the RIE process.” Ex.1005, [0055]. The result of this step is a “dual damascene structure.” *Id.* Matsunaga further discloses, relative to Figure 13, that RIE etching is performed using a “resist” to provide the desired pattern. *See e.g.*, Ex.1005, [0003]. Matsunaga accordingly discloses and renders obvious that when RIE etching is used to create the dual damascene structure of Figure 14, it uses resist masks as shown in the process of Figure 13. Ex.1003 ¶87. Further underscoring the obviousness of this process, it was well-known that patterning for a “dual

damascene structure” includes utilizing photoresist masks with corresponding openings. Ex.1004, 674-677, Fig. 15-3. Accordingly, it would have been obvious to a POSITA, considering Matsunaga’s MOS transistor with a “dual damascene structure,” to use a photoresist mask over interlayer insulating film 61, with the photoresist mask having an opening for etching connecting hole 62 and an opening for etching dummy connecting hole 64. Ex.1003, ¶88.

Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have implemented photoresist techniques (either as disclosed relative to Matsunaga Fig. 13 or from the standard practice of a POSITA) to form connecting hole 62 and dummy connecting hole 64. Ex.1003, ¶¶89-90.



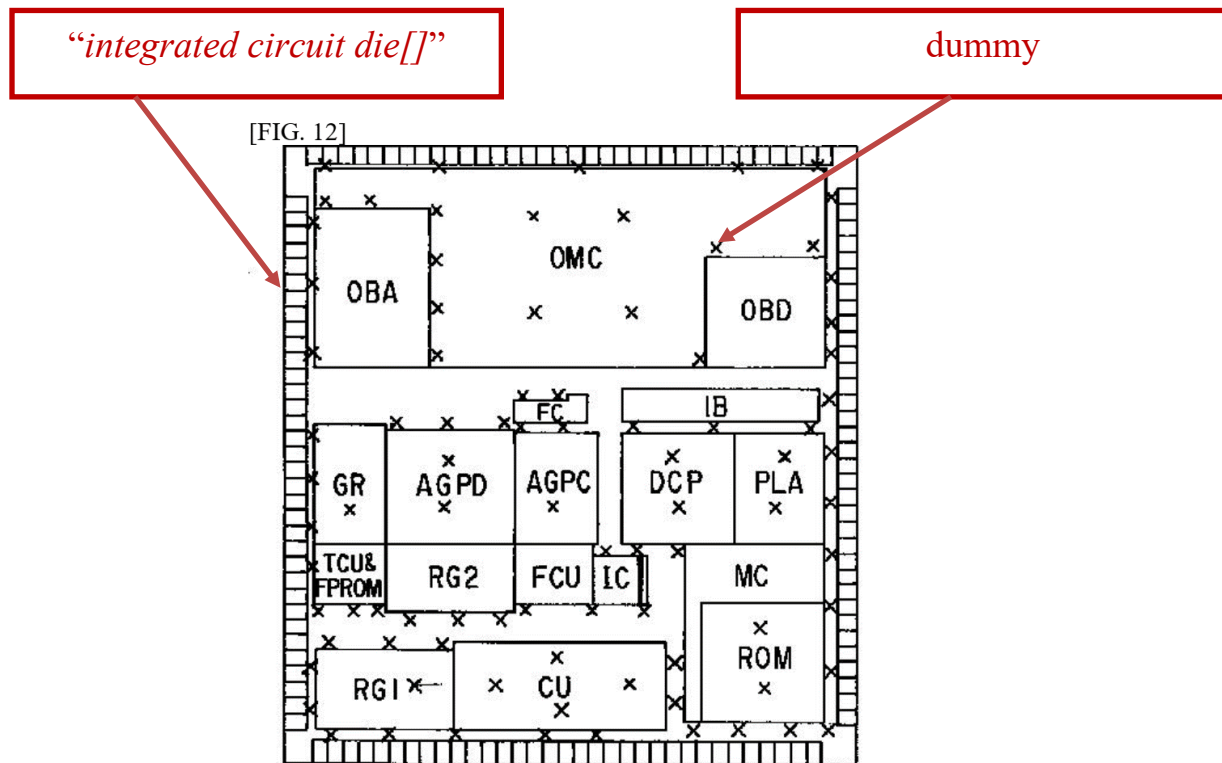
Ex.1005, FIG. 14 (a) (modified and annotated to show photoresist to form Matsunaga’s MOS transistor with a dual damascene structure).

[1.2.2] wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;

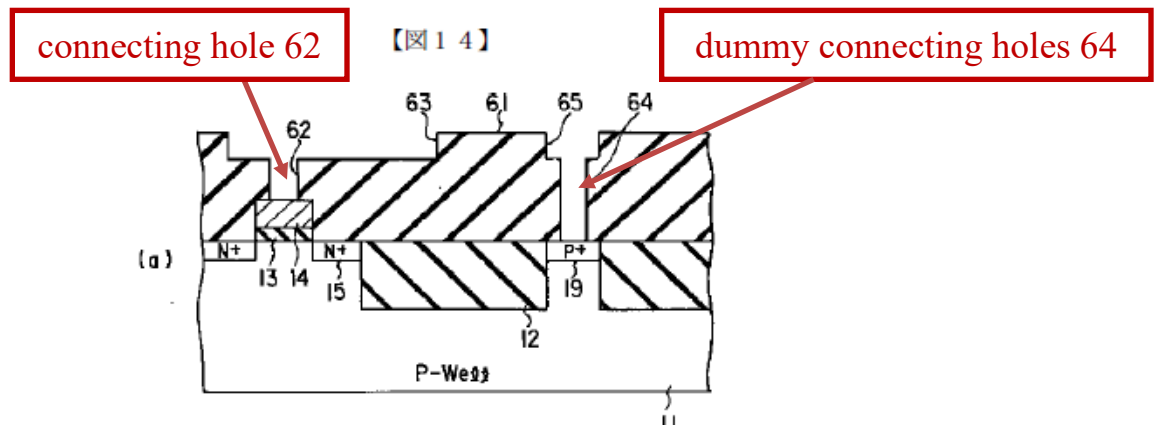
First, as analyzed at [1.1.1], Matsunaga renders obvious individual microprocessor circuits (chips or dies) (“*each said integrated circuit die*”). Further, as analyzed at [1.2.1], Matsunaga renders obvious that forming the MOS transistor includes using a photoresist mask with an interconnect opening and a dummy, non-interconnect opening (“*said interconnect opening and said dummy, non-interconnect opening*”). Ex.1003, ¶¶91-92.

Second, Matsunaga renders obvious that both openings “*are formed within each said integrated circuit die.*” Ex.1003, ¶93.

Consistent with the analysis in the preamble [1.0], Matsunaga’s MOS transistor teachings apply when manufacturing the microprocessor circuit illustrated at Figure 12. Ex.1005, [0053], Fig. 12. In more detail, Matsunaga discloses that “a dummy interconnection is applied to a microprocessor circuit... arranged at the locations indicated by the ‘X’ marks.” Ex.1005, [0053]. As illustrated below at Figure 12, Matsunaga’s microprocessor circuit (chip or die) (“*said integrated circuit die*”) has a dummy interconnection within the die area. Ex.1003, ¶94.



Ex.1005, FIG. 12 (annotated).



Ex.1005, FIG. 14 (a) (annotated).

It would have been obvious to a POSITA for each microprocessor circuit (chip or die) illustrated at Matsunaga's Figure 12 to include a MOS transistor illustrated at Figure 14. Ex.1015, 7 (describing that a chip's transistor count as of

2001 was “55,000,000.”); Ex.1018, ¶¶122-143. In such instances, the microprocessor circuit (chip or die) of Figure 12 would be manufactured according to the sequence analyzed at [1.2.1], including forming a photoresist mask that has an interconnect opening (for connecting hole 62) and a dummy, non-interconnect opening (for dummy connecting hole 64), which are thus included “within [] said integrated circuit die.” Moreover, it would have been obvious for the masking process to be also utilized when forming each microprocessor circuit (chip or die) on a semiconductor substrate as analyzed at [1.1.1]-[1.1.2]; Ex.1003, ¶¶95-96.

[1.3] performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and

First, as analyzed at [1.1.3], [1.2.1], Matsunaga renders obvious that over a dielectric layer (“*said dielectric layer*”) is a photoresist mask with an interconnect opening and a dummy, non-interconnect opening (“*said interconnect opening and said dummy, non-interconnect openings of said mask*”). Ex.1003, ¶¶97-98.

Second, during prosecution of the ’584 patent, Applicant contended that the plasma etching step requires “concurrently” etching of the “dummy, non-interconnect structures” and the “the interconnect structures.” Ex.1002, 31-32. The claims of the ’584 patent, however, do not require this “concurrently” etching step

Nevertheless, to the extent that “concurrently” etching is a claim requirement, Matsunaga discloses or renders it obvious. Ex.1003, ¶99.

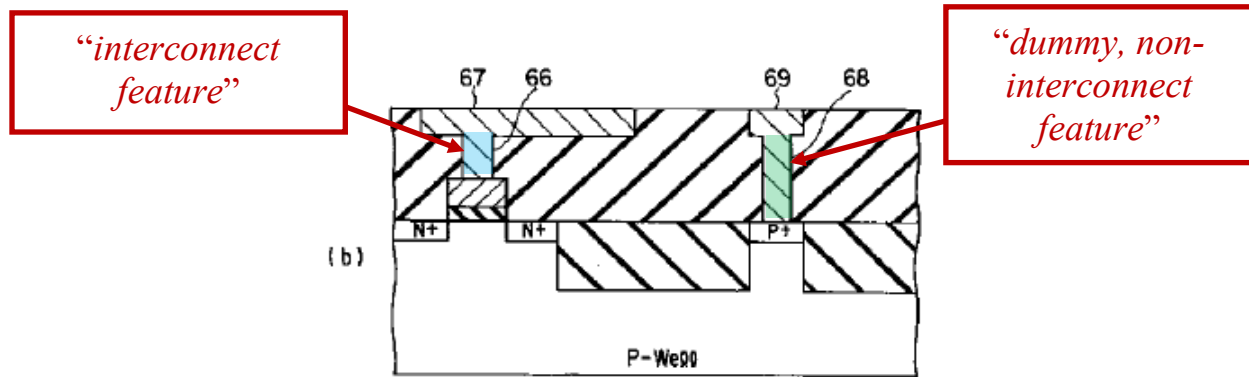
Matsunaga discloses “*performing a plasma etching process...thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer.*” Matsunaga describes using “**a plasma process such as RIE**” to etch the “interlayer insulating film 61,” thereby forming the “connecting hole 62” and the “dummy connecting holes 64” “**at the same time through the RIE plasma process.**” Ex.1005, [0009], [0030], [0055]-[0056]; Ex.1003, ¶100.

Moreover, consistent with the discussion at [1.2.1], it would have been obvious that to form Matsunaga’s “dual damascene structure,” etching is performed using the openings of the photoresist mask. Ex.1004, 675-677, FIG. 15-5. Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how Matsunaga’s RIE plasma process (“*a plasma etching process*”) etches through the mask openings to form connecting hole 62 (“*interconnect recessed trench*”) and dummy connecting hole 64 (“*dummy recessed trench*”) in the dielectric layer (“*dielectric layer*”). Ex.1003, ¶¶101-102.

**62 (hereinafter termed an in-hole functional interconnecting portion) and ...
an interconnecting portion 68 [] is buried in the dummy connecting hole 64
(hereinafter termed an in-hole dummy interconnecting portion).**” Ex.1005,
[0057]; Ex.1003, ¶105.

A POSITA would have understood that depositing metal over the entire surface results in “*filling*” any open holes with “*conductive materials*” to form the functional interconnecting portion 66 and the dummy interconnecting portion 68. Matsunaga’s dummy interconnecting portion 68 is “*non-interconnect*” as that term is used in the ’584 patent since it is “**not used in actual circuit operation**” and grounded to the substrate. Ex.1005, [0029]; [1.4.2] (“*non-interconnect feature is...grounded to said semiconductor substrate*”); Ex.1003, ¶106.

Matsunaga’s Figure 14(b), below, illustrates that the MOS transistor’s connecting hole 62 has a functional interconnecting portion 66 (“*interconnect feature*”) and the dummy connecting hole 64 has a dummy interconnecting portion 68 (“*dummy, non-interconnect feature*”). Ex.1003, ¶¶107-108.

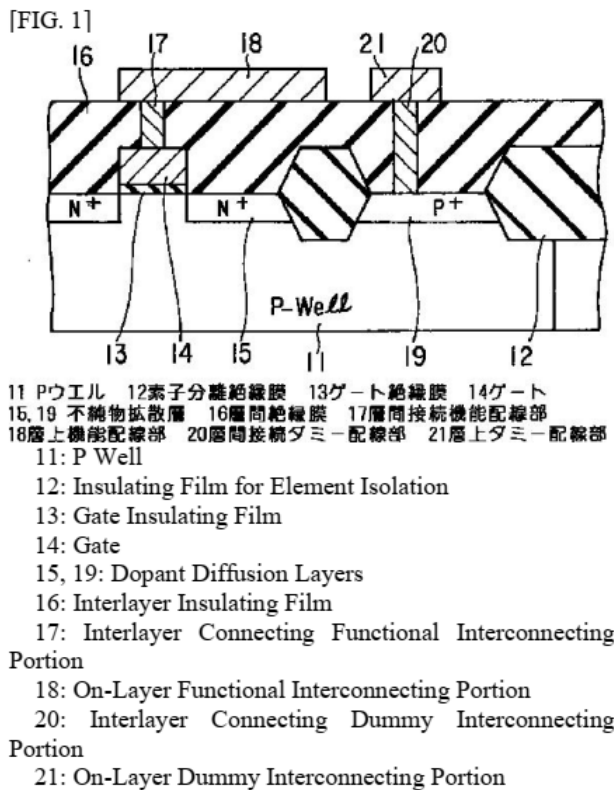


Ex.1005, FIG. 14 (b) (annotated).

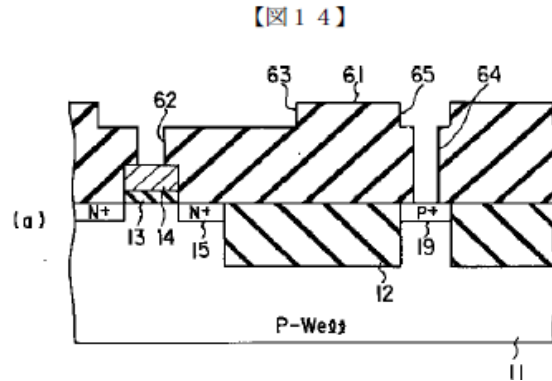
[1.4.2] wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;

First, as analyzed at [1.1.1], Matsunaga discloses a semiconductor substrate (“said semiconductor substrate”). And, as analyzed at [1.4.1], Matsunaga discloses a functional interconnecting portion (“said interconnect feature”) and a dummy interconnecting portion (“said dummy, non-interconnect feature”). Ex.1003, ¶¶109-110.

Second, as already noted above, in Matsunaga’s Figure 14, “structural elements that are substantially identical or corresponding to those in the first embodiment, depicted in FIG. 1, are assigned identical numbers, and detailed explanations thereof will be omitted.” Ex.1005, [0054]; Ex.1003, ¶111.



Ex.1005, Fig. 1.



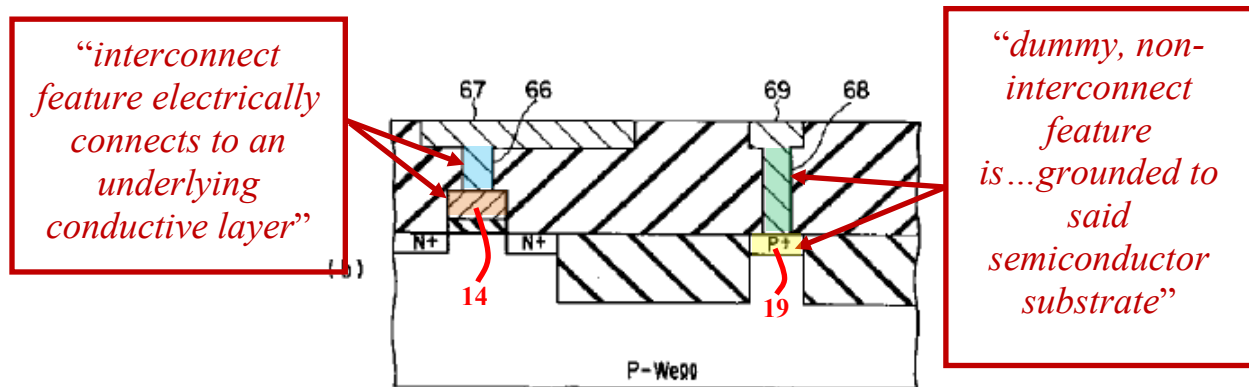
Ex.1005, Fig. 14 (a).

Matsunaga explains that the “functional interconnection 11 is used in actual circuit operation is connected to the gate 14” and that the “dummy interconnection that is not used in actual circuit operation...[and] is connected to the dopant diffusion layer 19 [in the substrate].” Ex.1005, [0029]; see also Ex.1005, Claim 1 (“a dummy interconnection... not used in circuit operation, [is] connected to the semiconductor substrate.”); Ex.1003, ¶112.

A POSITA would have understood that in Figure 14, gate 14 is a “*conductive layer*” because it is used in circuit operation to switch the MOS transistor. Also, a POSITA would have understood that connecting the dummy

interconnect to the dopant diffusion layer 19 is to “ground[]” it to the substrate because the dopant diffusion layer 19 serves to electrically connect the dummy interconnect to the substrate. Ex.1003, ¶113.

As illustrated at Figure 14 (b), reproduced below, Matsunaga’s functional interconnecting portion 66 is electrically connected to underlying gate electrode 14 (“underlying conductive layer”) and dummy interconnecting portion 68 is connected to the semiconductor substrate via P+ dopant diffusion layer 19 (“grounded to said semiconductor substrate”). Ex.1003, ¶¶114-115.



Ex.1005, FIG. 14 (b) (annotated).

[1.5] wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

First, as analyzed at [1.2.1], Matsunaga renders obvious using a photoresist mask with a dummy opening (“dummy, non-interconnect opening”). Further, as

analyzed at [1.3], the dummy opening in the photoresist mask is used in a RIE plasma process (“*plasma etching process*”). Ex.1003, ¶¶116-117.

Second, Matsunaga discloses that because “the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed simultaneously in the RIE process,” the “**electric charges supplied to the gate**” are also supplied “**to the P+ dopant diffusion layer 19 that is formed in the substrate**,” which can reduce the potential difference between the electropotential of the gate and the electropotential of the substrate.” Ex.1005, [0056]; *see also* Ex.1005, [0019], [0029]. A POSITA would have understood this passage as stating that the dummy opening provides another pathway for current to travel, thus (1) increasing the current through the “*shunt path*” (i.e., the path that does not go through the integrated circuits); and (2) decreasing the voltage at the gate, thereby decreasing the current flow at the integrated circuits (such as the gate). Ex.1008, 1:66 - 2:6. That is, the shunt path increases the current flow through the dummy connection while decreasing the current flow through the device connection. As such, Matsunaga’s disclosure that the dummy connecting hole 64 (which is defined by the mask dummy opening) supplies electric charges to the P+ dopant diffusion layer 19 during the RIE plasma process discloses “*increas[ing] an in-die shunt path current flow during said plasma etching process.*” Ex.1003, ¶118.

As noted above, Matsunaga teaches that, as a result of the dummy opening, the electrical potential at the gate is reduced. Ex.1005, [0056]; *see also* Ex.1005, [0019], [0029]. A POSITA would have understood that by reducing the electrical potential of the gate, the possibility for damage to the integrated circuit is reduced because less energy is being supplied to the gate of a MOS transistor during the RIE process. Ex.1003, ¶119. Matsunaga further explains that as a consequence of supplying electric charges to the P+ dopant diffusion layer 19 during the RIE plasma process, “the **electric field that acts on the gate insulating film 13 is weakened, making it possible to prevent charging damage.**” Ex.1005, [0056]; *see also* Ex.1005, [0019]. Because Matsunaga’s MOS transistors are within each microprocessor circuit die, preventing charge damage to the MOS transistor, e.g., gate insulating film, “*thereby reduc[es] charge damage to said integrated circuit dies.*” Ex.1003, ¶¶119-120.

3. Claim 3

[3.0] The method according to claim 1 wherein said mask comprises photoresist.

As analyzed at [1.2.1], in Matsunaga’s method, it would have been obvious to use a photoresist as the mask to make Matsunaga’s dual-damascene structure. Ex.1003, ¶121.

4. Claim 4

[4.0] The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.

As analyzed at [1.2.1]-[1.3], the connecting hole 62 (“*said interconnect recessed trench*”) is a damascene opening. Ex.1004, 674-677, Fig. 15-3 (disclosing “dual-damascene” opening); Ex.1003, ¶122.

5. Claim 5

[5.0] The method according to claim 1 wherein said interconnect recessed trench is a contact hole.

As analyzed at [1.3] and [1.4.1]-[1.4.2], Matsunaga’s connecting hole 62 (“*interconnect recessed trench*”) provides a contact to the gate 14 and thus is “*a contact hole.*” (“[T]he connecting hole 62 (hereinafter termed an in-hole functional interconnecting portion)” that facilitates “connect[ion] to gate 14”); Ex.1003, ¶123.

D. Ground 2: Claim 2 is Obvious over Matsunaga and Jaso

1. Summary of Jaso

Jaso concerns tools and mechanisms for improving the use of metals in a semiconductor device. Ex.1009, 2:7-10; Ex.1003, ¶¶124-125. One of these steps is called chemical mechanical polishing (“CMP”) and is used to planarize a surface after material is deposited. Jaso recognizes that problems may occur when attempting to planarize a surface that includes both metal and non-metal layers (such as in a dual-damascene process for inlaying metal layers in a die).

According to Jaso, “problems such as dishing occur causing a non-planar surface,”

which results in “significant overpolish...erosion of dielectric...increased sheet resistance,” among other “problems at later steps in the fabrication process.”

Ex.1009, 2:7-27. To address these problems, Jaso uses dummy metal pattern to “provid[e] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:2-5. Jaso defines a “pattern factor for a particular area or region...as the area covered by the metal divided by the total area of the particular area or region” and states that typically “the pattern factor is 50%.” Ex.1009, 3:5-13. In another example, Jaso discloses that “a method is provided to set a predetermined high pattern factor design limit of say 60-90%, preferably 70–80%” and as low as 20-50%.” Ex.1009, 3:38-47; *see also* Ex.1009, 7:24-8:18. In other words, Jaso discloses that, when inlaying metal into a microchip, one should ensure that between 20-90% of a surface is metallic, to ensure that the CMP process results in a planar surface with minimal dishing (i.e., areas where the surface is not sufficiently flat due to the undesirable removal of softer non-metallic material). Ex.1003, ¶126.

2. Obviousness Combination Matsunaga and Jaso

A POSITA would have been motivated to combine the teachings of Matsunaga and Jaso, as discussed below. Ex.1003, ¶127.

a) **Analogous Art**

Jaso, like Matsunaga, is in the same field of endeavor as the '584 patent, pertaining to semiconductor manufacturing. Ex.1001, 1:15-18, 7:12-13; Ex.1005, [0055]; Ex.1009, 2:45-50. As such, a POSITA considering Matsunaga's semiconductor manufacturing method, would have also considered Jaso, which provides additional teachings applicable to Matsunaga. Ex.1003, ¶128.

b) **Combination Rationale**

A POSITA would have been motivated to combine the teachings of Jaso with Matsunaga to produce predictable results as discussed below. Ex.1003, ¶129.

Matsunaga teaches a process to make MOS devices that utilizes CMP. *See* Ex.1005, [0055]-[0057], FIG. 14 (b). Jaso teaches that one potential problem with CMP is that it may cause “dishing” and other problems (e.g., over polishing, erosion of dielectrics, increased sheet resistance, etc.). Ex.1009, 2:7-27. To address the noted problems, Jaso teaches that it is important to “provid[e] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:3-5. Specifically, Jaso teaches that interconnect openings and dummy openings should be patterned such that the area of those openings covered by metal divided by the total area has a high pattern factor design limit of 60-90% and low pattern factor design limit of 20-50%. Ex.1009, 3:10-47; Ex.1009, 7:20-8:18; Ex.1003, ¶130.

It would have been obvious to a POSITA to apply the teachings of Jaso to ensure that sufficient metal surfaces are present in the dummy and interconnect areas (i.e., 20-90% coverage). By applying Jaso's teachings, Matsunaga's CMP step would avoid undesirable **"dishing effect and other non-planarization"** problems (e.g., **"overpolish,"** **"erosion of dielectric,"** **"increased sheet resistance,"** etc.). Ex.1009, 2:7-27; 3:29-31; Ex.1003, ¶131.

The proposed combination is merely applying a known technique to a known device or method (e.g., Jaso's technique of controlling the interconnect openings and dummy openings pattern to have a low pattern factor design limit of 20%, with Matsunaga's method and semiconductor device) ready for improvement (e.g., reduce dishing effects, over polishing, erosion of dielectrics, and increased sheet resistance, etc.) to yield predictable results. Ex.1003, ¶¶132-133.

c) Reasonable Expectation of Success

The results would have been predictable and there would have been a reasonable expectation of success in the combination given that both Jaso and Matsunaga relate to semiconductor processing. Modifying Matsunaga's method and semiconductor device to have a low pattern factor design limit of 20% would have been a straightforward and simple matter of utilizing a computer algorithm to generate dummy patterns that meet the desired metallization lower limit. *See* Ex.1009, 3:65-4:2; Ex.1007, [0106]. The reasonable expectation of success is also

supported by others that had implemented similar pattern densities. *See* Ex.1016, [0035]; Ex.1003, ¶134.

3. Claim 2

[2.0] The method according to claim 1 wherein an exposed surface area of said interconnect and dummy, non-interconnect openings is higher than 5% of a die area of each said integrated circuit die.

First, as analyzed at [1.2.1], Matsunaga renders obvious forming over the interlayer insulating film a photoresist mask that comprises an “*interconnect opening*” (for connecting hole) and a “*dummy, non-interconnect opening*” (for dummy connecting hole). Ex.1003, ¶¶135-136.

Second, Jaso discloses a device that has interconnect openings 15 (a-d) and dummy openings 20. Ex.1009, 5:66-6:9, Figs. 11A-11D. Jaso utilizes dummy patterns to “provid[e] a uniform distribution of damascene metal line circuitry across each integrated circuit chip.” Ex.1009, 3:3-5. Jaso explains that a “pattern factor for a particular area or region may be defined as the **area covered by the metal divided by the total area** of the particular area or region” and states that typically “**the pattern factor is 50%.**” Ex.1009, 3:5-10. Jaso teaches that the area covered by metal in figure 11D is the same as the area of the interconnect openings 15 (a-d) and dummy openings 20 in figure 11B. Ex.1009, Figs. 11B, 11D. In another example, Jaso sets a “**high pattern factor design limit of say 60-90%,**

preferably 70–80%” and a **“low pattern factor design limit [of] ...20-50%.”**

Ex.1009, 3:38-47; Ex.1009, 7:20-8:18; Ex.1003, ¶137.

It would have been obvious to a POSITA to form patterns, per Jaso’s examples, such that a photoresist mask is patterned to have an exposed surface area of the interconnect openings and the dummy openings to be higher than 20% of the integrated circuit chip or die area. Ex.1009, 3:3-5 (“...uniform distribution of damascene metal line circuitry across each integrated circuit chip.”); Ex.1003, ¶138.

It would have been obvious to a POSITA to apply Jaso’s teachings to Matsunaga and provide a uniform distribution of metal line circuitry across each integrated circuit microprocessor to beneficially “overcome the dishing effect and other non-planarization” related problems, such as erosion of dielectrics, over polishing areas, increased sheet resistance, etc. Ex.1009, 2:11-32, 3:29-31; Obviousness Combination Matsunaga and Jaso; Ex.1003, ¶139.

In implementing the combination, a POSITA would have found it obvious for Matsunaga’s photoresist mask to be patterned to have an exposed surface area of the interconnect opening (for connecting hole) and the dummy, non-interconnect opening (for dummy connecting hole), to be higher than 20% of the area of each microprocessor circuit (chip or die), so that Matsunaga’s CMP step will avoid the

undesirable dishing and other effects described in the combination rationale section above. Ex.1003, ¶¶140-141.

E. Ground 3: Claim 6 is Obvious over Matsunaga and Appel

1. Summary of Appel

Appel generally pertains to semiconductor manufacturing. Ex.1017, Title, Abstract. Appel teaches forming a MOS transistor gate electrode by diffusing impurities in polysilicon gate. Ex.1017, 2:6-3:66, 4:13-55; Ex.1003, ¶¶142-143.

2. Obviousness Combination Matsunaga and Appel

A POSITA would have been motivated to combine the teachings of Appel with Matsunaga, as discussed below. Ex.1003, ¶144.

a. Analogous Art

Appel, like Matsunaga, is in the same field of endeavor as the '584 patent, pertaining to methods of semiconductor manufacturing, including MOS transistors. Ex.1001, 1:15-18, 4:52-54; Ex.1005, [0055]; Ex.1017, Title, Abstract. As such, a POSITA considering Matsunaga's method, which includes forming a MOS transistor, would have also considered Appel, which provides additional teachings applicable to Matsunaga's MOS transistor. Ex.1003, ¶145.

b. Combination Rationale

A POSITA would have been motivated to combine the teachings of Appel with Matsunaga to produce predictable results as discussed below. Ex.1003, ¶146.

Matsunaga teaches that its device includes a “MOS transistors” with a “gate 14.” *See* Ex.1005, [0055]-[0056], FIGS. 1, 14. However, since MOS transistors were well-known in the art, Matsunaga provides limited detail regarding the formation of gate electrode 14. Appel provides this well-known technique and teaches the implementation details. In particular, Appel teaches forming a MOS transistor gate electrode by diffusing impurities from boro-silicate glass (BSG) or phospho-silicate glass (PSG) into polysilicon region above a gate dielectric. Ex.1017, 2:42-54; *see also* Ex.1017, 2:6-66, 3:31-66. Appel explains that “[t]he dopant can be diffused from these doped glass films into adjacent films of polysilicon [gate electrode] without having to worry about implant damage or implant straggle.” Ex.1017, 2:52-54. It would have been obvious to a POSITA to apply the diffused polysilicon gate electrode teachings of Appel because these details are directly applicable to successfully implementing the gate electrode of Matsunaga’s MOS transistor. Implementing Matsunaga’s MOS transistor gate electrode per Appel’s teachings would have been recognized as a suitable option, and therefore obvious to a POSITA. Ex.1003, ¶147.

Additionally, a POSITA would have been motivated to apply Appel’s teachings, when implementing the gate electrode of Matsunaga’s MOS transistor, because Matsunaga provides limited detail to form its gate electrode as it was well known at the time. Ex.1003, ¶148. The proposed combination is merely a simple

application of a known technique (forming a gate electrode by diffusion) to obtain predictable results of forming a gate electrode for a functional MOS transistor.

Ex.1003, ¶149.

c. Reasonable Expectation of Success

The results would have been predictable and there would have been a reasonable expectation of success in the combination given that it was conventional and well-known in the art how to form a gate electrode of polysilicon. *See* Ex.1008, 2:53-56; Ex.1012, 436. Implementing Matsunaga’s semiconductor device to have a diffused polysilicon gate would have been a straightforward and simple matter of patterning polysilicon, doping, and annealing (as Appel teaches in detail), well within the level of skill in the art. Indeed, Appel references these processes as “Background of The Invention.” Ex.1017, 1:7-2:20; Ex.1003, ¶150.

3. Claim 6

[6.0] The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.

First, as analyzed at [1.4.2], Matsunaga discloses an underlying gate electrode 14 (“*underlying conductive layer*”).

Appel discloses how to form a gate electrode by teaching that a “**polysilicon gate layer...is doped by diffusing impurities into the polysilicon** from a doped silicate glass over the polysilicon gate layer.” Ex.1017, 2:42-45. For example,

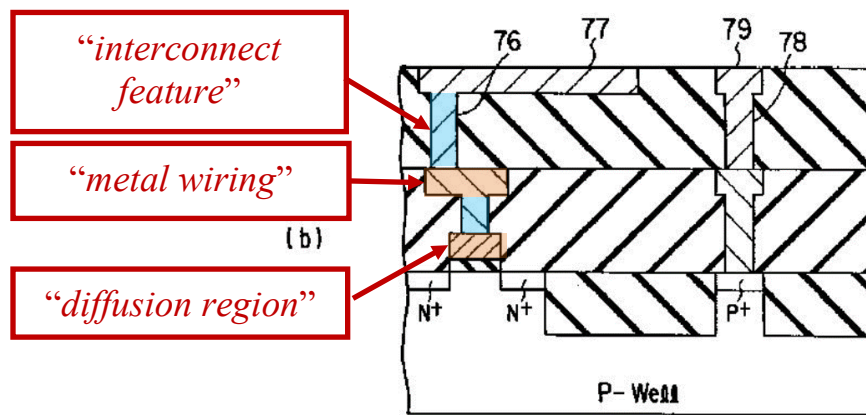
“boro-silicate glass (BSG) and phospho-silicate glass (PSG)... can be used in accordance with the present invention, depending upon the impurity of interest.” Ex.1017, 2:45-54. “**The dopant can be diffused from these doped glass films into adjacent films of polysilicon [gate electrode]** without having to worry about implant damage or implant straggle.” Ex.1017, 2:52-54; *see also* Ex.1017, 2:6-66. Appel describes a process flow with BSG to form a “polysilicon gate portion p+.” *See* Ex.1017, 3:30-41, 4:13-65. Appel further explains that “process described above operates equally well for doping n + polysilicon from PSG.” Ex.1017, 3:65-66. Appel’s diffused polysilicon gate electrode corresponds to a “*diffusion region*.” Ex.1003, ¶¶151-152.

It would have been obvious to a POSITA to implement Matsunaga’s gate electrode 14 as a polysilicon diffusion region, per Appel, because this is one suitable technique to implement gate electrodes. *See* Reasons to Combine Matsunaga and Appel. Ex.1003, ¶153.

Thus, Matsunaga in combination with Appel discloses that the gate electrode is implemented as a polysilicon diffusion region, which renders obvious that “*said underlying conductive layer comprises ... diffusion region*.” Ex.1003, ¶154.

Second, the analysis in claim 1 focused on Matsunaga’s embodiment of Figures 14 (a) and (b). However, Matsunaga expands on that embodiment, in Figures 15 (a) and (b), “which depicts a state wherein an interlayer insulating film

71 is formed on a lower portion structure that is formed through, for example, the process of FIG. 14, and a connecting hole 72 and an interconnection groove 73, for forming an interconnection of a dual damascene structure, are formed through an RIE process in the interlayer insulating film 71.” Ex.1005, [0058]. The further embodiment of Figure 15, which builds upon Figure 14, similarly has “the ability to weaken the electric field that acts on the gate insulating film 13, which can prevent charging damage.” Ex.1005, [0059]; Ex.1003, ¶155.



Ex.1005, FIG. 15 (b) (annotated).

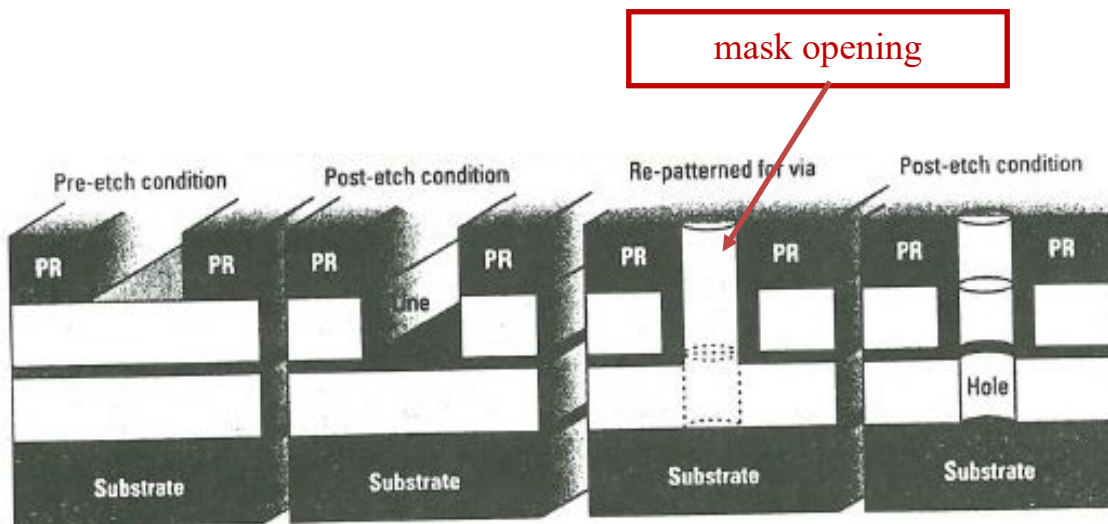
In the further embodiment of Figures 15 (a) and (b), functional interconnect 76, separately and together with functional interconnect 66, would correspond to the “*interconnect feature*,” while the metal line 67 and the gate electrode 14 as modified per Appel’s polysilicon diffusion region would correspond to the “*underlying conductive layer...[that] comprises metal wiring and diffusion region*.” Ex.1003, ¶¶156-157.

F. Ground 4: Claims 1 and 3-5 are Obvious over Matsunaga and Wolf

To the extent Patent Owner argues that Matsunaga alone is insufficient, the combination of Matsunaga and Wolf renders obvious Claims 1 and 3-5 as discussed below. Ex.1003, ¶158.

1. Summary of Wolf

Wolf teaches well-known dual-damascene processing using a mask comprising an opening shown below at FIG. 15-5. Ex.1004, 676-679; Ex.1003, ¶159.



Ex.1004, Fig. 15-5 (annotated).

2. Obviousness Combination Matsunaga and Wolf

a. Analogous Art

Wolf is analogous art to the '584 patent, because it is in the same field of endeavor of manufacturing semiconductor devices, including using dual

damascene processing. Ex.1001, 6:23-27, 7:12-13; Ex.1004, 674-677, Fig. 15-3.

Accordingly, a POSITA would have considered Wolf's teachings relevant.

Ex.1003, ¶160.

b. Combination Rationale

A POSITA would have been motivated to combine the teachings of Matsunaga and Wolf with a reasonable expectation of success. Ex.1003, ¶161.

Matsunaga seeks to form MOS transistors that have a "dual damascene structure." Ex.1005, [0055], [0058], [0063]. Wolf provides implementation details regarding dual damascene methods suitable to form the dual damascene structure of Matsunaga's MOS transistors. Ex.1004, 674-677, Fig. 15-3. It would have been obvious for a POSITA to consider and apply Wolf's dual damascene technique, when implementing Matsunaga's method of manufacturing MOS transistors that have dual damascene structure to achieve the results that Matsunaga describes; namely, to facilitate the manufacturing of a MOS transistor with a dual damascene structure. Ex.1003, ¶162.

The proposed combination is merely combining prior art elements (Wolf's textbook dual damascene technique with Matsunaga's method for forming a dual damascene structure) according to known methods (Wolf provides significant details regarding dual damascene processing) to yield predictable results (facilitate the manufacturing of Matsunaga's dual damascene structure). Ex.1003, ¶163.

c. Reasonable Expectation of Success

The results would have been predictable and there would have been a reasonable expectation of success in the combination because Matsunaga and Wolf address the same technology. And Wolf's teachings would have been easily applied to Matsunaga because the proposed combination does not require any change to the dual damascene structure of Matsunaga. Ex.1005, [0055], [0058]. To the extent that any modification was needed to Matsunaga's method such that it includes Wolf's dual damascene technique, it would have been textbook knowledge and within the level of ordinary skill in the art. Ex.1012, 307, 328. The expectation of success is further evidenced by others that had used dual damascene processing. Ex.1010, 1:57-61; Ex.1016, [0070]; Ex.1003, ¶¶164-166.

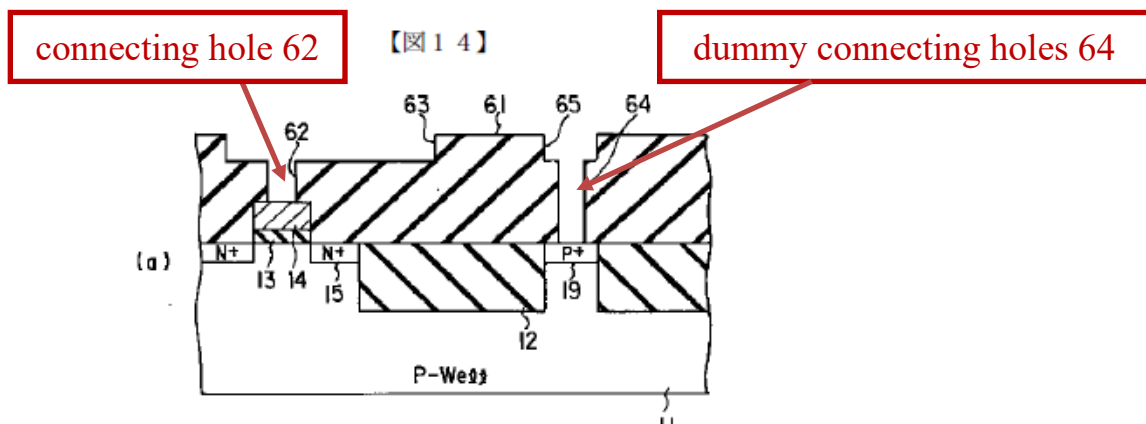
6. Claim 1

For the same reasons discussed above in Ground 1, Matsunaga renders obvious limitations [1.0]-[1.1.3] and [1.4.1]-[1.4.2] in Ground 4. Furthermore, as discussed below, Matsunaga in combination with Wolf renders obvious limitations [1.2.1]-[1.3] and [1.5]. Ex.1003, ¶¶167-171, 191-192.

[1.2.1] forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,

To the extent argued that in Ground 1 Matsunaga alone does not render obvious “forming a mask...comprising an interconnect opening and a dummy, non-interconnect opening,” the further combination with Wolf renders it obvious.

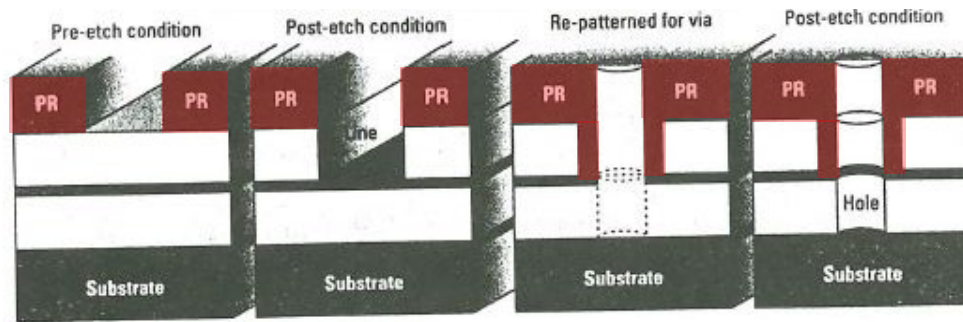
As noted in Ground 1 limitation [1.2.1], Matsunaga’s MOS transistor has a “dual damascene structure” that includes a connecting hole 62 (“interconnect”) and dummy connecting hole 64 (“non-interconnect”). Ex.1003, ¶¶172-174.



Ex.1005, FIG. 14 (a) (annotated).

While Matsunaga mentions the use of a “resist” in its patterning process, Wolf provides implementation details of processing techniques that were conventional/textbook and directly applicable to Matsunaga’s MOS transistor of Figure 14(a), which has a “dual damascene structure.” Ex.1005, [0054]. Wolf discloses a “dual-damascene” technique where a photoresist (PR) mask is used to

etch a trench in an underlying interlayer dielectric. Ex.1004, 674-677, Fig. 15-3; Ex.1003, ¶¶175-176.

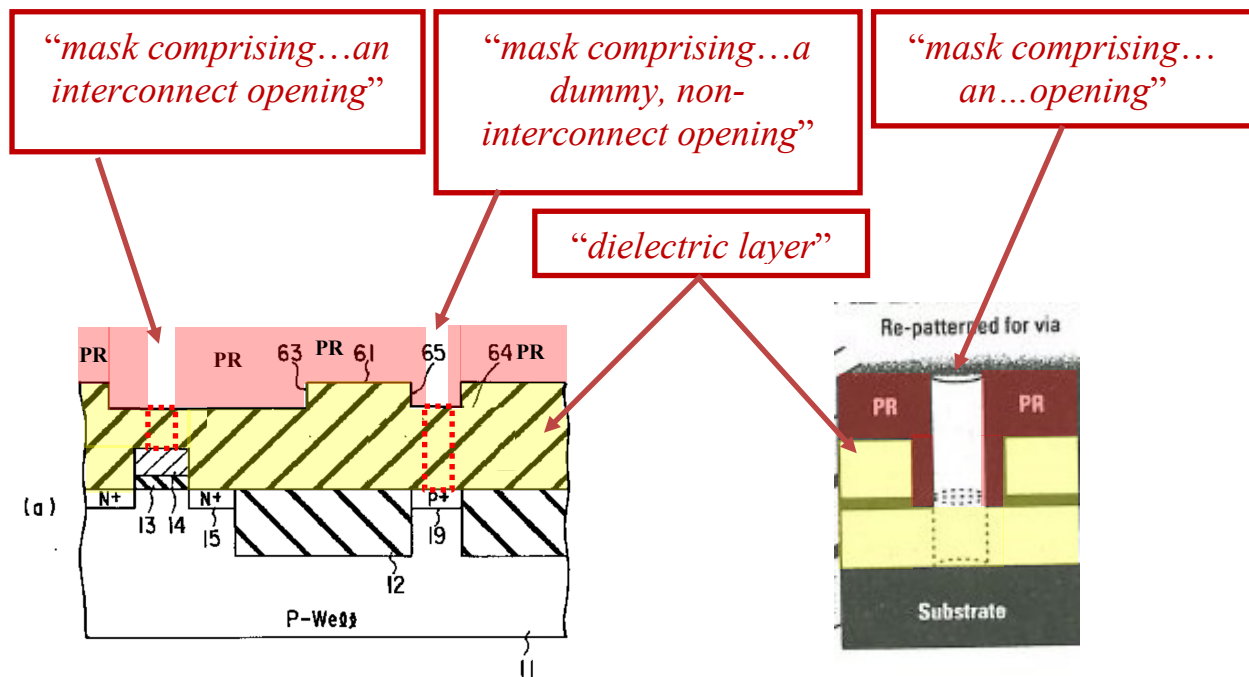


Ex. 1004, Fig. 15-5 (annotated).

It would have been obvious to use Wolf's process to create both Matsunaga's interconnect openings and non-interconnect openings. As noted, Matsunaga discloses that connecting hole 62 and dummy connecting hole 64 are "formed at the same time through the RIE process." Ex.1005, [0055]. Wolf provides a way to create these openings at the same time using the well-known dual damascene sequence. Specifically, it would have been obvious to a POSITA to form a photoresist (PR) mask over the interlayer insulating film 61, with the photoresist mask comprising an interconnect opening for connecting hole 62 and a dummy, non-interconnect opening for dummy connecting hole 64. Wolf's processing techniques represent implementation details suitable for forming Matsunaga's MOS transistor, including using a photoresist that protects other parts

of the wafer surface during the etching process. *See* Obviousness Combination Matsunaga and Wolf; Ex.1003, ¶177.

Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have applied Wolf's conventional and well-known dual damascene techniques at the “re-patterned for via” step. Ex.1003, ¶¶178-179.



Ex.1005, FIG. 14 (a) (modified and annotated to show dual-damascene “re-patterned for via” step as applied to Matsunaga’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “re-patterned for via” annotated).

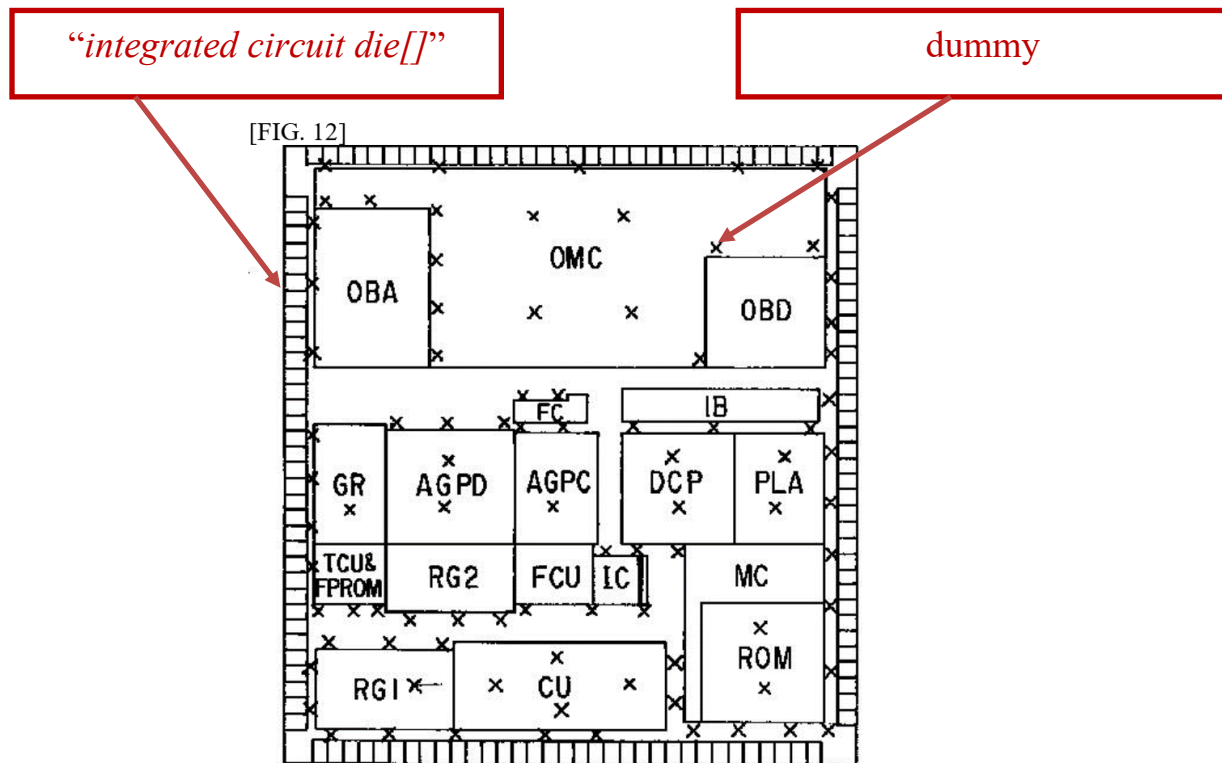
[1.2.2] wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;

First, as analyzed at Ground 1 limitation [1.1.1], Matsunaga renders obvious microprocessor circuits (chips or dies) (“*each said integrated circuit die*”). Further,

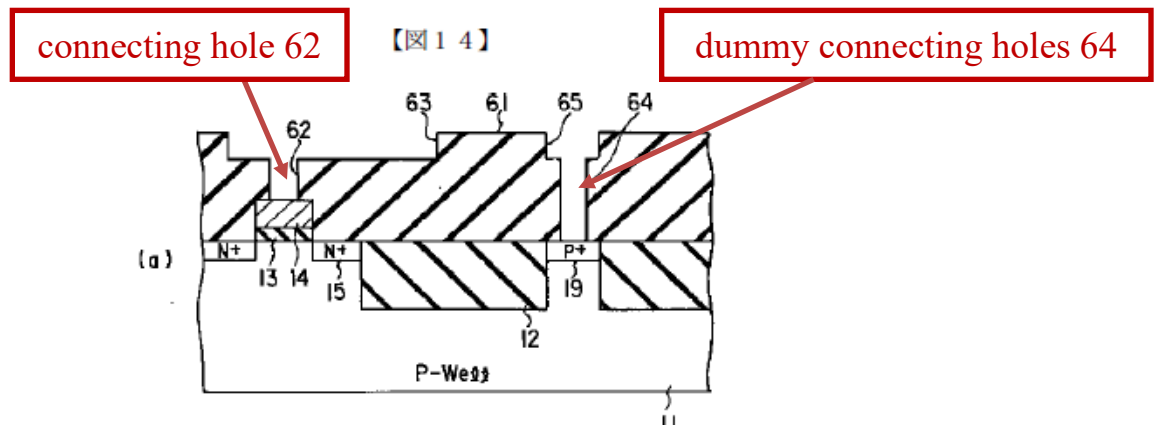
as analyzed at Ground 4 limitation [1.2.1], Matsunaga in combination with Wolf discloses that the photoresist mask has an interconnect opening and a dummy, non-interconnect opening (“*said interconnect opening and said dummy, non-interconnect opening*”). Ex.1003, ¶¶180-181.

Second, Matsunaga in combination with Wolf renders obvious that both openings “*are formed within each said integrated circuit die.*” Ex.1003, ¶182.

Consistent with Ground 1 limitation [1.0], Matsunaga’s MOS transistor teachings apply when manufacturing the microprocessor circuit illustrated at Figure 12. Ex.1005, [0053], Fig. 12. According to Matsunaga, “a dummy interconnection is applied to a microprocessor circuit... arranged at the locations indicated by the ‘X’ marks.” Ex.1005, [0053]. As illustrated below at Figure 12, Matsunaga’s microprocessor circuit (chip or die) (“*said integrated circuit die*”) has a dummy interconnection within the die area. Ex.1003, ¶183.



Ex.1005, FIG. 12 (annotated).



Ex.1005, FIG. 14 (a) (annotated).

It would have been obvious to a POSITA for each microprocessor circuit (chip or die) illustrated at Matsunaga's Figure 12 that is manufactured on a semiconductor substate, to include a MOS transistor illustrated at Figure 14.

Ex.1015, 7 (describing that a chip's transistor count as of 2001 was "55,000,000."); Ex.1018, ¶¶122-143. In such instances, the microprocessor circuit (chip or die) of Figure 12 would be manufactured according to the sequence analyzed at Ground 4, limitation [1.2.1], including forming a photoresist mask that has an interconnect opening (for connecting hole 62) and a dummy, non-interconnect opening (for dummy connecting hole 64). Moreover, it would have been obvious for the masking process (per the combination with Wolf) to be also utilized when forming each microprocessor circuit (chip or die) on the semiconductor substate, to facilitate scaling and cost benefits as analyzed at Ground 1 limitations [1.1.1]-[1.1.2]; Ex.1003, ¶¶184-185.

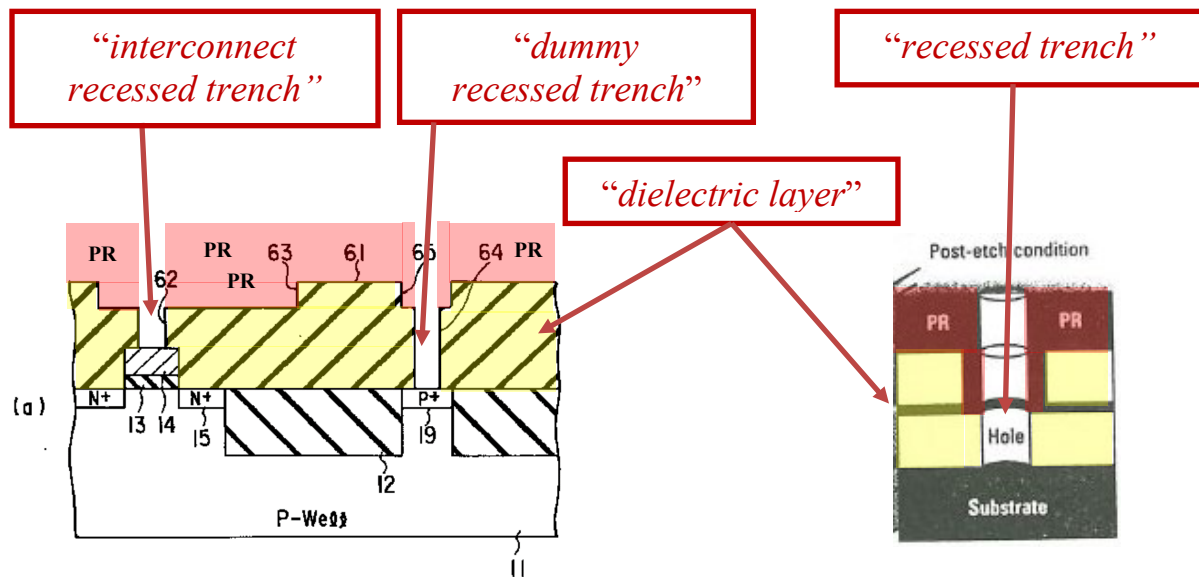
[1.3] performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and

First, as analyzed at Ground 4 limitation [1.2.1], Matsunaga in combination with Wolf discloses that over a dielectric layer is a photoresist mask with an interconnect opening and a dummy, non-interconnect opening ("*said interconnect opening and said dummy, non-interconnect openings of said mask*"). Ex.1003, ¶¶186-187.

Second, as analyzed at Ground 1 limitation [1.3], Matsunaga discloses performing a plasma REI process thereby simultaneously forming connecting hole

62 and dummy connecting holes 64 in the dielectric layer (“*performing a plasma etching process...thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer*”). Ex.1003, ¶188.

Moreover, as analyzed at Ground 4 limitation [1.2.1]-[1.2.2], Wolf teaches etching the interlayer dielectric layer using the openings of the photoresist mask. Ex.1004, 675-677, FIG. 15-5. Provided below is a modified Figure 14 (a) of Matsunaga, illustrating how a POSITA would have applied Wolf’s conventional techniques, at the “post-etch condition,” such that Matsunaga’s RIE plasma process (“*a plasma etching process*”) etches through the mask openings to form connecting hole 62 (“*interconnect recessed trench*”) and dummy connecting hole 64 (“*dummy recessed trench*”) in the dielectric layer (“*dielectric layer*”). Ex.1003, ¶¶189-190.



Ex.1005, FIG. 14 (a) (modified and annotated to show dual-damascene “post etch condition” as applied to Matsunaga’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “post etch condition” annotated).

[1.5] wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

First, as analyzed at Ground 4 limitation [1.2.1], Matsunaga in combination with Wolf discloses using a photoresist mask with a dummy opening (“dummy, non-interconnect opening.” Further, as analyzed at Ground 4 limitation [1.3], the dummy opening in the photoresist mask is used in a RIE plasma process (“plasma etching process”). Ex.1003, ¶¶193-194.

Second, as analyzed at Ground 1 limitation [1.5], Matsunaga discloses that because the dummy connecting holes 64 and the dummy interconnection grooves 65 are also formed simultaneously in the RIE process, the “dummy, non-

interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.” Ex.1003, ¶¶195-196.

3. Claim 3

[3.0] The method according to claim 1 wherein said mask comprises photoresist.

As analyzed at Ground 4 limitation [1.2.1], in Matsunaga’s method, the prior art uses a photoresist as a mask. Ex.1004, 674-677, Fig. 15-3 (disclosing “dual-damascene” sequence where a photoresist (PR) mask is used); Ex.1003, ¶197.

4. Claim 4

[4.0] The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.

As analyzed at Ground 4 limitations [1.2.1]-[1.3], the connecting hole is formed in a dual damascene process, which renders obvious that “*said interconnect recessed trench is a damascene opening,*” as claimed. Ex.1004, 674-677, Fig. 15-3 (disclosing “dual-damascene” opening). Ex.1003, ¶198.

5. Claim 5

[5.0] The method according to claim 1 wherein said interconnect recessed trench is a contact hole.

As analyzed at Ground 4 limitations [1.3] and [1.4.1]-[1.4.2], the dual damascene structure includes a connecting hole, which renders obvious that “*said interconnect recessed trench is a contact hole,*” as claimed. Ex.1003, ¶199.

G. Ground 5: Claim 2 is Obvious over Matsunaga, Wolf, and Jaso

See Ground 4 claim 1 and Ground 2 claim 2. Ex.1003, ¶200.

H. Ground 6: Claim 6 is Obvious over Matsunaga, Wolf, and Appel

See Ground 4 claim 1 and Ground 3 claim 6. Ex.1003, ¶201.

I. Ground 7: Claims 1 and 3-6 are Obvious over Eriguchi, Quirk, and Wolf

1. Summary of Eriguchi

Like the '584 patent, Eriguchi recognizes that in prior art “process for forming conductors of such a semiconductor device, plasma processing including plasma CVD or plasma etching,” “plasma charging damage” deteriorates “device characteristics.” Ex.1007, [0003]-[0009]; Ex.1003, ¶¶202-203.

To “solve the above-described problem,” Eriguchi discloses “a semiconductor device that can suppress plasma charging damage in a plasma process and a method for manufacturing the same.” Ex.1007, [0037]. In more detail, Eriguchi discloses a method for manufacturing a “semiconductor device constituted by semiconductor integrated circuits” “in which **the occurrence of plasma charging damage is suppressed.**” Ex.1007, [0002], [0075]-[0087]; *see also* Ex.1007, [0088]-[0095]; Ex.1003, ¶225. Eriguchi’s method is applicable to MOS transistors with functional and dummy conductors electrically connected to the gate electrode 7 and functional conductors electrically connected to source and drain region 5. Ex.1007, [0040]-[0041], [0078]-[0082], [0148]; Ex.1003, ¶204.

Eriguchi's device has the same basic arrangement as the '584 patent's device, namely: **(1)** a semiconductor substrate (Ex.1001, 6:28-30; Ex.1007, [0080]); **(2)** a dielectric layer (Ex.1001, 6:31-33; Ex.1007, [0080]); **(3)** a functional interconnect electrically connected to a conductive layer (Ex.1001, 7:3-11; Ex.1007, [0080]-[0081]); and **(4)** a dummy interconnect, which is not used in circuit operation, that is grounded to the substrate (Ex.1001, 7:3-11; Ex.1007, [0081], [0084]); Ex.1003, ¶¶205-206.

These elements are shown in a side-by-side comparison of the '584 patent's Figure 10 and Eriguchi's Figure 1A. Ex.1003, ¶¶207-208.

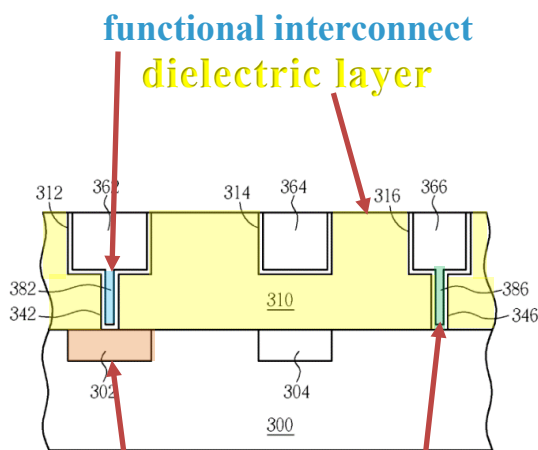


Fig. 10

functional interconnect
dielectric layer

conductive layer
dummy interconnect

Ex.1001, Fig. 10 (annotated).

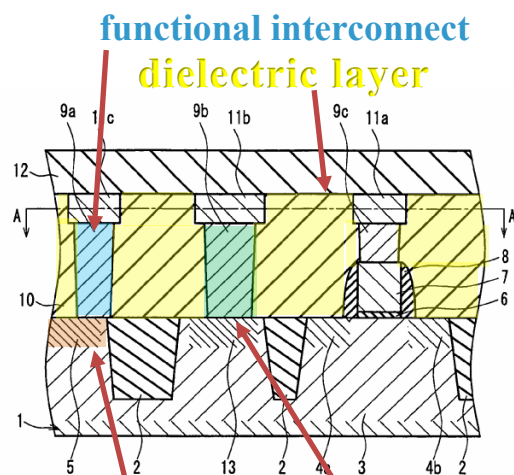


FIG. 1A

functional interconnect
dielectric layer

conductive layer
dummy interconnect

Ex.1007, Fig. 1A (annotated).

2. Summary of Quirk

Quirk teaches well-known techniques for manufacturing integrated circuits (“ICs”). Ex.1012, 1, 4-7, 436. As illustrated below at Figures 1.3 and 1.6, Quirk’s silicon wafers include identical ICs (known as dies, chips, and microchips) that are separated by scribe lines. Ex.1003, ¶¶209-210.

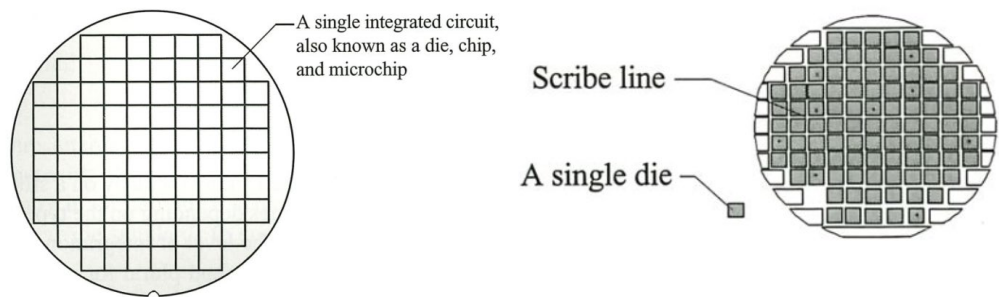


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3.

Ex.1012, FIG. 1.6 (partial).

3. Obviousness Combination Eriguchi and Quirk

d. Analogous Art

Eriguchi and Quirk are analogous art to the '584 patent, because they are in the same field of endeavor of manufacturing semiconductor devices implemented as integrated circuits. Ex.1001, 3:36-54; Ex.1007, [0002], [0087]; Ex.1012, 1, 4-9. As such, a POSITA considering Eriguchi’s method would have also considered Quirk, which provides additional teachings applicable to Eriguchi. Ex.1003, ¶¶211-212.

e. **Combination Rationale**

A POSITA would have been motivated to combine the teachings of Eriguchi and Quirk to produce predictable and beneficial results as discussed below.

Ex.1003, ¶213.

Eriguchi teaches forming a semiconductor device, e.g., MOS transistor, for integrated circuits. *See* Ex.1007, [0002], [0087]. It was a well-known semiconductor manufacturing technique to form identical integrated circuits on the same silicon wafer to achieve scaling and to obtain related benefits, including cost reductions. Ex.1012, 6, 8; Ex.1015, 72; Ex.1018, ¶¶122-143. It was also conventional to use scribe lanes that surround and separate different integrated circuit dies on a semiconductor substrate. Ex.1004, 348-349; Ex.1003, ¶214.

Quirk provides implementation details directly relevant when manufacturing Eriguchi's integrated circuits. Quirk describes a well-known silicon wafer manufacturing technique that includes forming a plurality of integrated circuit dies on a silicon wafer, with each die separated and surrounded by scribe lines.

Ex.1012, 6-7, 548, FIGS. 1.3, 1.6. Quirk explains that the scribe lines are used to slice the silicon wafer into individual integrated circuit dies. Ex.1012, 9. A

POSITA would have understood that after individual integrated circuit dies are manufactured on a silicon wafer, it is necessary to separate them to be used as an electronic component. Ex.1003, ¶215.

It would have been obvious to a POSITA, in view of Quirk, to manufacture a plurality of integrated circuit dies on the same wafer substrate with Eriguchi's method, to obtain the benefits of scaling and reducing cost. Ex.1012, 6. Because the integrated circuits are implemented as a distinct die separated by scribe lanes, they can be cut from the wafer along the scribe lanes. Ex.1008, 2:7-15; Ex.1014, 101; Ex.1012, 9, FIGS. 1.3, 1.6; Ex.1015, 72; Ex.1018, ¶¶99-143; Ex.1003, ¶216.

The proposed combination is merely applying a known technique to a known device or method (e.g., Quirk's technique of forming a number of integrated circuit dies on a wafer substrate that are separated and surrounded by scribe lanes, with Eriguchi's method and integrated circuit) ready for improvement (e.g., scaling, reducing cost, providing an area to cut the dies from the wafer) to yield predictable results of forming individual integrated circuit chips. Ex.1003, ¶217.

These reasons, separately and together, would have motivated a POSITA to combine the teachings of Quirk with Eriguchi. Ex.1003, ¶218.

f. Reasonable Expectation of Success

The results would have been predictable and there would have been a reasonable expectation of success in the combination because Eriguchi and Quirk address the same technology, as analyzed above in the analogous art section. Modifying Eriguchi's method and integrated circuit to be implemented according

to Quirk's conventional teachings would have been well within the skill in the art as detailed in various textbooks. *See* Ex.1004, 348-349; Ex.1012, *generally*, Fig. 1.3; Ex.1014, 101; Ex.1015, 72; Ex.1018, ¶¶99-143; Ex.1003, ¶¶219.

4. Obviousness Combination Eriguchi and Wolf

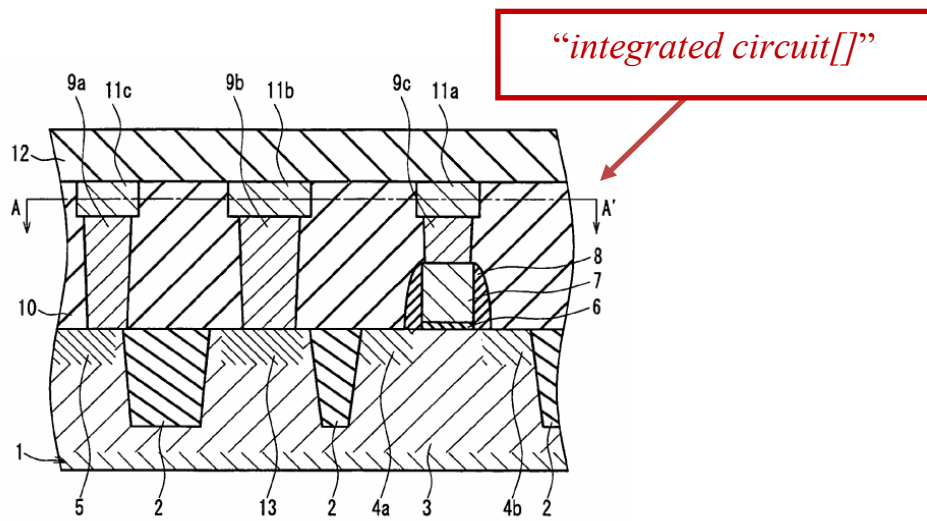
Eriguchi teaches that its method is applicable to MOS transistors that are formed by techniques including a dual damascene process. Ex.1007, [0011], [0078]-[0082], [0148]. Wolf provides implementation details regarding such dual damascene methods, thereby allowing for the manufacturing of Eriguchi's MOS transistors. Ex.1004, 674-677, Fig. 15-3. Accordingly, the proposed combination is simply applying the teachings of a textbook reference (Wolf) to another reference (Eriguchi) that is ready for and expressly calls for those teachings, with a reasonable expectation of success. Ex.1003, ¶242. For this and for the same reasons discussed above in Ground 4, regarding the combination of Wolf and Matsunaga, it would have been obvious to apply Wolf's fundamental semiconductor manufacturing details (which represent common background knowledge to a POSITA and that are omitted from many references), when manufacturing Eriguchi's semiconductor device. Ex.1003, ¶221.

5. Claim 1

[1.0] A method for reducing charging damage to integrated circuits during semiconductor manufacturing, comprising:

First, Eriguchi teaches a “*method for reducing charging damage...during semiconductor manufacturing.*” Eriguchi seeks to solve problems of “plasma charging damage by disclosing “**a semiconductor device that can suppress plasma charging damage in a plasma process and a method for manufacturing the same.**” Ex.1007, [0003]-[0006], [0037]. In the context of Embodiment 1 of Figures 1 and 2, Eriguchi discloses “**a method for manufacturing the semiconductor device**” “**in which the occurrence of plasma charging damage is suppressed.**” Ex.1007, [0075]-[0087]; *see also* Ex.1007, [0088]-[0095]; Ex.1003, ¶¶222-224.

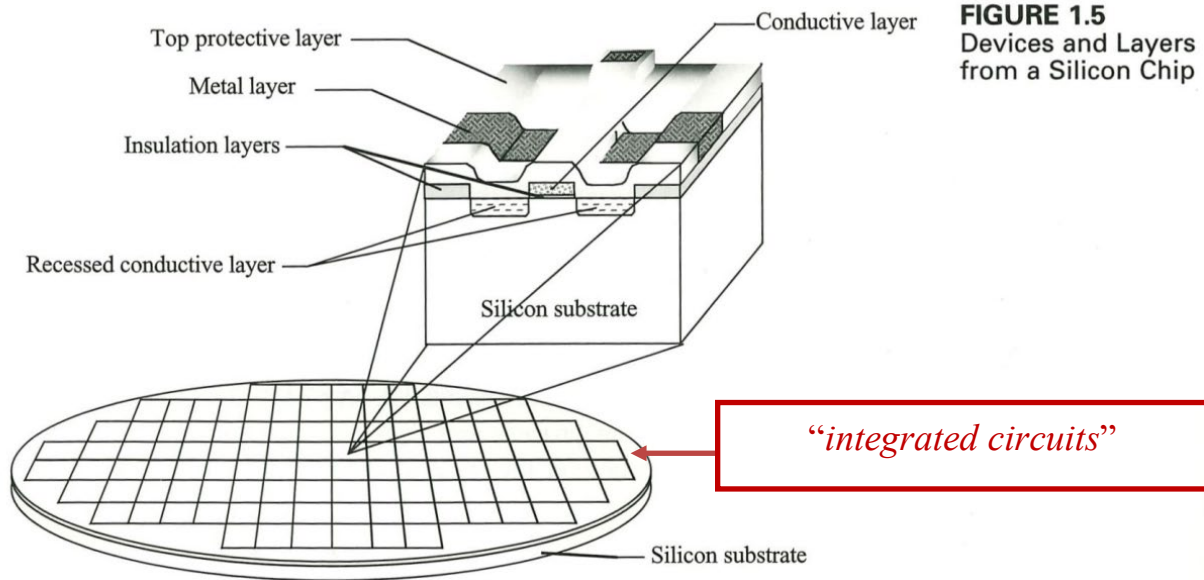
Second, Eriguchi’s method is applicable to “*integrated circuits*” because it is used to manufacture a “semiconductor device constituted by **semiconductor integrated circuits**” that includes “**an n-channel MOS transistor.**” Ex.1007, [0002], [0078]. Eriguchi’s Figure 1A is reproduced below, illustrating an MOS transistor; Ex.1003, ¶¶225-226.



Ex.1007, FIG. 1A (annotated).

Third, to the extent argued that Eriguchi’s teachings are insufficient to render obvious that the method is applied to “*integrated circuits*,” the further combination with Quirk renders such obvious. Quirk discloses forming a plurality of identical integrated circuit “ICs” “die” “chips” on the same silicon wafer.

Ex.1012, 6-8; Ex.1003, ¶¶227-228.

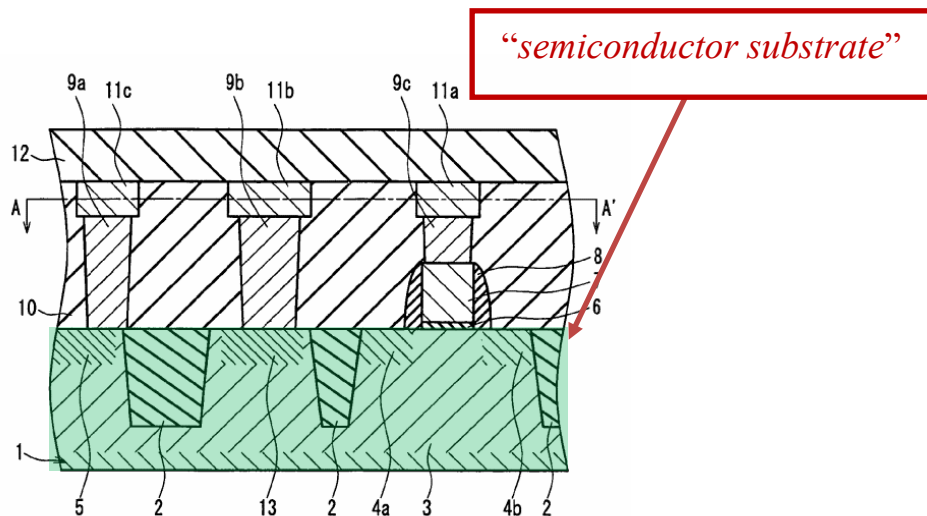


Ex.1012, FIG. 1.5 (annotated).

In view of Quirk, it would have been obvious to a POSITA to manufacture a plurality of Eriguchi’s integrated circuits on the same silicon wafer/substrate to obtain the benefits of scaling and reduce cost. In the proposed combination of Eriguchi and Quirk, a plurality of integrated circuits on the same silicon substrate correspond to “*integrated circuits*” as claimed. *See* Ex.1012, 6, 8; Ex.1015, 72; Ex.1018, ¶¶122-143; Obviousness Combination Eriguchi and Quirk; Ex.1003, ¶¶228-229.

[1.1.1] providing a semiconductor substrate comprising thereon a number of integrated circuit dies,

First, Eriguchi discloses “providing a semiconductor substrate” by teaching that the device illustrated at Figure 1A (reproduced below) “includes an n-type silicon substrate 1.” Ex.1007, [0077]-[0078]; Ex.1003, ¶¶230-231.



Ex.1007, FIG. 1A (annotated).

A POSITA would have understood that silicon is semiconductor and Eriguchi’s “silicon substrate” is thus a semiconductor substrate. Ex.1012, 4. Accordingly, Eriguchi’s silicon substrate teaches a “*semiconductor substrate.*” Ex.1003, ¶232.

Second, consistent with the analysis at the preamble [1.0], Eriguchi and Quirk disclose integrated circuits that include MOS transistors, which renders obvious “*integrated circuits.*” Further, Quirk’s Figures 1.3 and 1.6, reproduced below, illustrates a plurality of circuit dies (“*number of integrated circuit dies*”) on

a wafer substrate (“*semiconductor substrate*”). Ex.1012, 6 (“**The chip is also referred to as a die.**”), 8 (“The fabrication of **microchips...integrated circuits.**”); Ex.1003, ¶233.

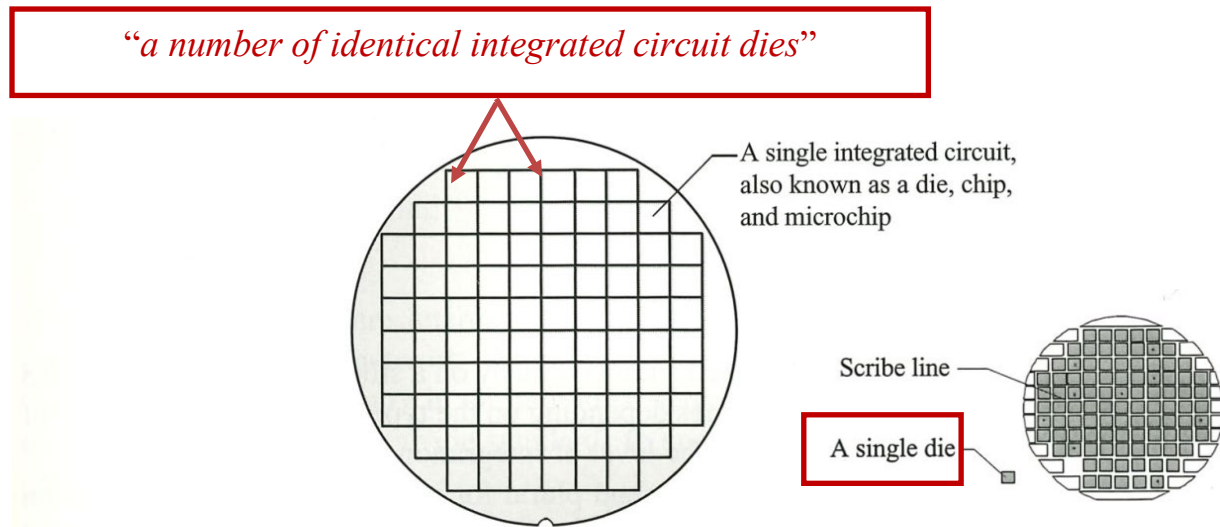


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3 (annotated). Ex.1012, FIG. 1.6 (partial, annotated).

It would have been obvious to a POSITA to manufacture a plurality of integrated circuit dies (each die including at least a MOS transistor) on the same semiconductor substrate (e.g., wafer substrate), per the combination of Eriguchi and Quirk, to obtain the benefits of scaling and reducing cost. Ex.1012, 6, 8; Ex.1015, 72; Ex.1018, ¶¶122-143. Because the integrated circuits are each a separate die, they can be separated along the scribe lanes as taught by Quirk. Ex.1008, 2:7-15, 3:63-67; Obviousness Combination Eriguchi and Quirk; Ex.1003, ¶¶234-235.

[1.1.2] said integrated circuit dies being separated from each other by scribe lanes surrounding each said integrated circuit die,

First, as analyzed at Ground 7 limitation [1.1.1] Eriguchi in combination with Quirk discloses that a semiconductor substrate (e.g., wafer substrate) includes a plurality of integrated circuit dies (“*integrated circuit dies*”). Ex.1003, ¶¶236-237.

Second, it would have been obvious to a POSITA, in implementing the combination of Eriguchi and Quirk, for the integrated circuit dies to be “*separated from each other by scribe lanes surrounding each said integrated circuit die.*” As shown below in Quirk’s Figures 1.3 and 1.6, each integrated circuit “die, chip, and microchip” is surrounded and separated by “**scribe lines**,” which would have been understood by a POSITA to correspond to a “*scribe lanes.*” Ex.1003, ¶238.

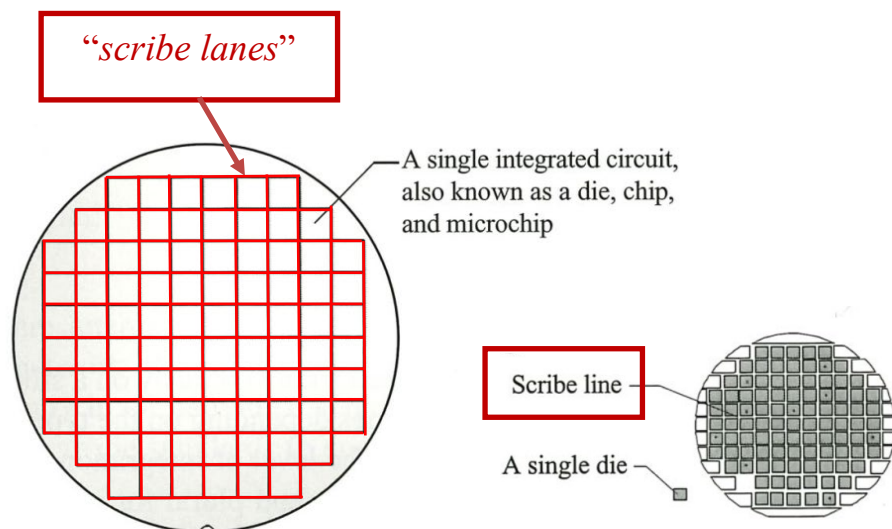


FIGURE 1.3 Top View of Wafer with Chips

Ex.1012, FIG. 1.3 (annotated).

Ex.1012, FIG. 1.6 (partial, annotated).

Accordingly, it would have been obvious to a POSITA for each of Eriguchi's integrated circuit (chip or die) to be separated from each other by scribe lanes that surround each integrated circuit (chip or die). The scribe lanes would beneficially serve to isolate different integrated circuit dies from each other and would also serve as the area for cutting each integrated circuit die from the wafer. See Ex.1004, 348-349; Ex.1008, 2:7-15, 3:63-66; Ex.1012, 9, 549, 575, Figure 20.5; Ex.1014, 101; Ex.1015, 72. Additionally, the scribe lanes enable the use of "scribe line monitors" for testing purposes. Ex.1012, 548-549; *see also* Obviousness Combination Eriguchi and Quirk; Ex.1003, ¶¶239-240.

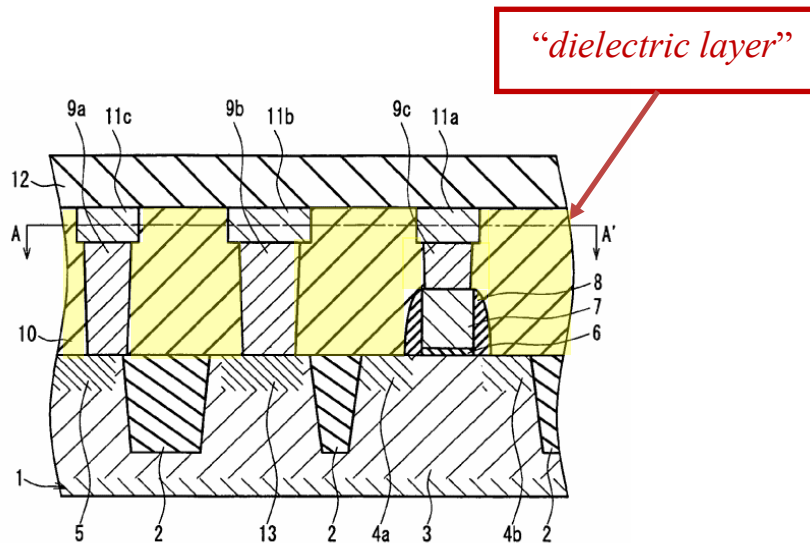
[1.1.3] wherein said semiconductor substrate comprises thereon a dielectric layer;

First, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses a semiconductor substrate (e.g., wafer substrate) ("*semiconductor substrate*"). Ex.1003, ¶¶241-242.

Second, Eriguchi discloses "*a dielectric layer*" by teaching that "an underlying interlayer insulating film 10...[is formed] on the silicon substrate 1" and that the "underlying interlayer insulating film 10...[comprises] silicon oxide films or silicon nitride films." Ex.1007, [0080]. A POSITA would have understood that silicon oxide and silicon nitride are dielectrics. Ex.1014, 381-382. Additionally, a POSITA would have understood that an electrical insulator film is

a dielectric. Ex.1014, 6, 141; Ex.1018, ¶¶99-121. Accordingly, Eriguchi's underlying interlayer insulating film 10 corresponds to the claimed "*dielectric layer*." Ex.1003, ¶243.

As illustrated below at Figure 1A, Eriguchi's interlayer insulating film 10 is formed on the semiconductor substrate 1 and serves to insulate various conducting features from each other. Ex.1003, ¶¶243-244.



Ex.1007, FIG. 1A (annotated).

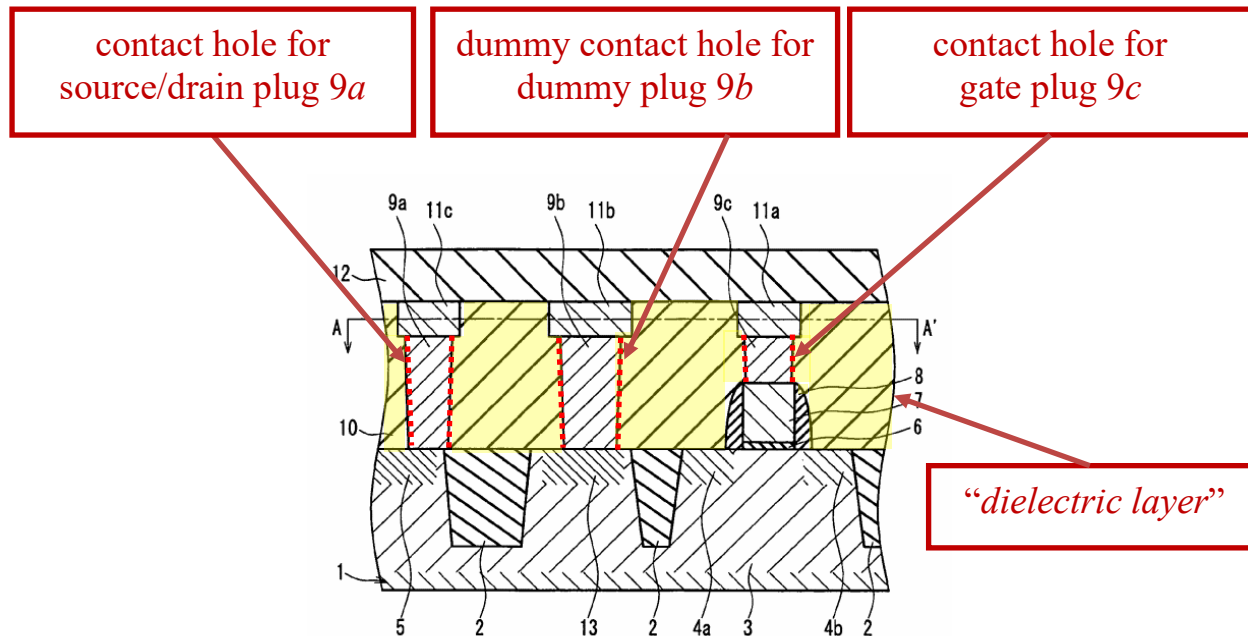
[1.2.1] forming a mask over said dielectric layer, said mask comprising an interconnect opening and a dummy, non-interconnect opening,

First, Eriguchi discloses that its method is applicable to MOS transistors.

Ex.1007, [0078], [0148]. Eriguchi's "conductors 11a to 11c are... simultaneously formed by the damascene method and embedded in the underlying interlayer insulating film 10." Ex.1007, [0081]. Eriguchi's conductors 11a and 11c are

functional, since “conductor 11*a* is a conductor for gate electrode connection that is connected to the gate electrode 7 via a W (tungsten) plug 9*c*” and “conductor 11*c* is a conductor for source and drain connection that is connected to the n⁺ region 5 via a W (tungsten) plug 9*a*.” Ex.1007, [0081]. Additionally, Eriguchi’s “conductor 11*b* is a **dummy conductor... and does not contribute to the function of the semiconductor device.**” Ex.1007, [0082]; *see also* Ex.1007, [0040]-[0041]. Eriguchi further explains that “**contact holes** [are] formed in the underlying interlayer insulating film 10” and “**filled with tungsten to form the W plugs 9*a* to 9*c*.**” Ex.1007, [0086], [0090]; Ex.1003, ¶¶246-248.

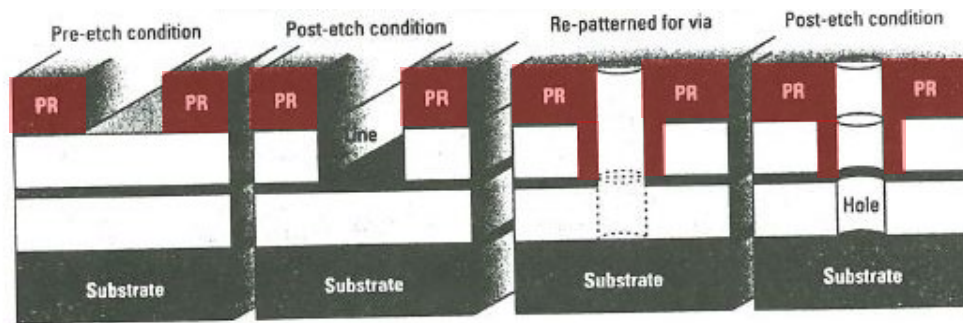
Figure 1A is reproduced below, illustrating the resulting MOS transistor with contact holes for functional plugs 9*a* and 9*c* and dummy plug 9*b*. Ex.1003, ¶249.



Ex.1007, FIG. 1A (annotated).

While Eriguchi omits the patterning process for forming the MOS transistor or the contact holes of Figure 1A, such would have been well-known and conventional in the art. Ex.1003, ¶250.

For example, Wolf teaches processing techniques that were known in the art and directly applicable when manufacturing Eriguchi’s MOS transistor, which has “a dual damascene structure.” Ex.1007, [0078]; Ex.1004, 674-676, Fig. 15-3. Wolf discloses a “dual-damascene” technique where a photoresist (PR) mask is used to etch a trench in an underlying interlayer dielectric. Ex.1004, 674-677, Fig. 15-3; Ex.1003, ¶251.



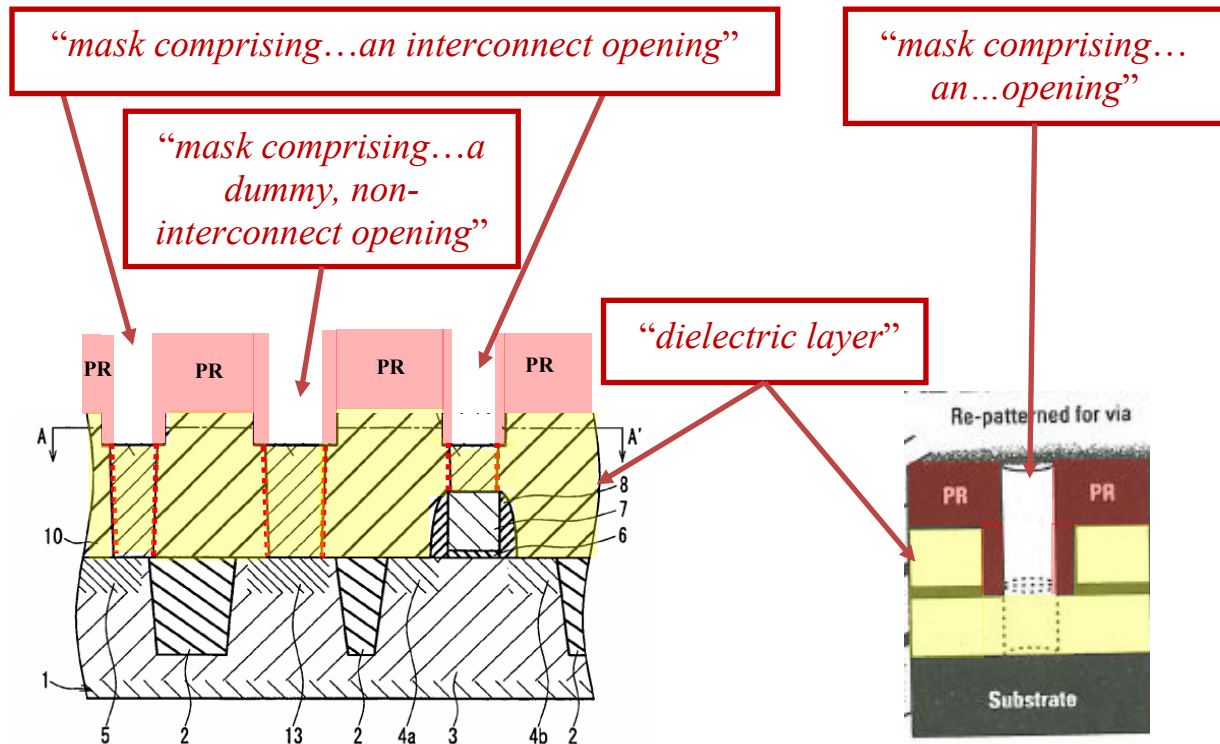
Ex. 1004, Fig. 15-5 (annotated).

It would have been obvious to a POSITA, when manufacturing Eriguchi's MOS transistor having "a dual damascene structure," to follow or adapt Wolf's dual damascene teachings to form the contact holes for functional plugs 9a and 9c and dummy plug 9b (which are formed "simultaneously by the damascene method", Ex.1007, [0040], [0091]) to use a dual damascene sequence per Wolf. Such a combination would involve creating Eriguchi's contact holes by forming a photoresist (PR) mask over the interlayer insulating film 10, with the photoresist mask comprising an interconnect opening for the non-dummy contact hole and a dummy, non-interconnect opening for the dummy contact hole. Indeed, Eriguchi discloses using a mask having mask data in the context of forming a multilayer interconnect wiring structure comprising conductors, dummy conductors, and an interlayer insulating film. *See e.g.*, Ex.1007, [0145]; Ex.1003, ¶252.

Provided below is a modified Figure 1A of Eriguchi, illustrating how a POSITA would have applied Wolf's textbook, conventional, and well-known

techniques at the “re-patterned for via” step, to form Eriguchi’s MOS transistor.

Ex.1003, ¶¶253-254.



Ex.1007, FIG. 1A (modified and annotated to show dual-damascene “re-patterned for via” step as applied to Eriguchi’s MOS transistor).

Ex.1005, FIG. 15-5 (partial “re-patterned for via” annotated).

[1.2.2] wherein said interconnect opening and said dummy, non-interconnect opening both are formed within each said integrated circuit die;

First, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses integrated circuit dies, with an individual integrated circuit die (including a MOS transistor) corresponding to “said integrated circuit die.”

Further, as analyzed at Ground 7 limitation [1.2.1], Eriguchi in combination with

Wolf discloses that the photoresist mask has interconnect openings (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), which correspond to “*said interconnect opening and said dummy, non-interconnect opening.*” Ex.1003, ¶¶255-256.

Second, Eriguchi in combination with Quirk and Wolf renders obvious that the mask openings “*are formed within each said integrated circuit die.*” Specifically, it would have been obvious to a POSITA for each integrated circuit die, represented by the combination of Eriguchi and Quirk, to include a MOS transistor illustrated at Eriguchi’s Figure 1A. *See* Ex.1015, 7 (describing that a chip’s transistor count as of 2001 was “55,000,000.”); Ex.1018, ¶¶122-143. In such instances, Eriguchi’s MOS transistor would be manufactured per Wolf’s sequence analyzed at Ground 7 limitation [1.2.1], including forming a photoresist mask that has interconnect openings (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b). Moreover, it would have been obvious for the masking process to be also utilized when forming each integrated circuit die on the silicon wafer, to facilitate scaling and cost benefits as analyzed at Ground 7 limitations [1.1]-[1.1.2]. Ex.1003, ¶¶257-258.

[1.3] performing a plasma etching process to etch said dielectric layer through said interconnect opening and said dummy, non-interconnect openings of said mask, thereby forming an interconnect recessed trench and a dummy recessed trench in said dielectric layer; and

First, as analyzed at Ground 7 limitation [1.2.1], Eriguchi in combination with Wolf discloses that a photoresist mask has at least one interconnect opening (for contact holes to form functional plugs 9a and 9c) and a dummy, non-interconnect opening (for dummy contact hole to form dummy plug 9b), which correspond “*said interconnect opening and said dummy, non-interconnect openings of said mask.*” Ex.1003, ¶¶259-260.

Second, during prosecution of the ’584 patent, Applicant contended that the plasma etching step requires “concurrently” etching of the “dummy, non-interconnect structures” and “the interconnect structures.” Ex.1002, 31-32. The claims of the ’584 patent, however, do not require this “concurrently” etching step. Nevertheless, to the extent that this is a claim requirement, Eriguchi teaches it. Ex.1003, ¶261.

Eriguchi discloses that the “dummy conductor insulated from the gate electrode and the active region by the first insulating layer is **formed** in a position adjacent to the dummy conductor **simultaneously** with the conductor for a gate electrode.” Ex.1007, [0070]. In the claims, Eriguchi recites that “**the first dummy conductor and the first conductor are formed simultaneously by a damascene**

method and embedded in the lowermost insulating layer” and that “the second conductor and the second dummy conductor that are provided in a same insulating layer are formed simultaneously by a damascene method and embedded in the insulating layer in which these conductors are provided.” Ex.1007, claim 21.

Eriguchi also discloses that “a process for forming conductors of such a semiconductor device, plasma processing including plasma CVD or **plasma etching** has been increasingly utilized.” Ex.1007, [0003]; *see also* Ex.1007, [0149]. It would have been obvious to a POSITA that simultaneously forming the MOS transistor functional conductors and dummy conductor includes performing plasma etching. Ex.1003, ¶262.

Moreover, consistent with conventional manufacturing techniques, analyzed at [1.2.1], Wolf teaches that it was known in the art to etch the interlayer dielectric layer using the openings of the photoresist (“PR”) mask. Ex.1004, 675, 677; Ex.1003, ¶263.

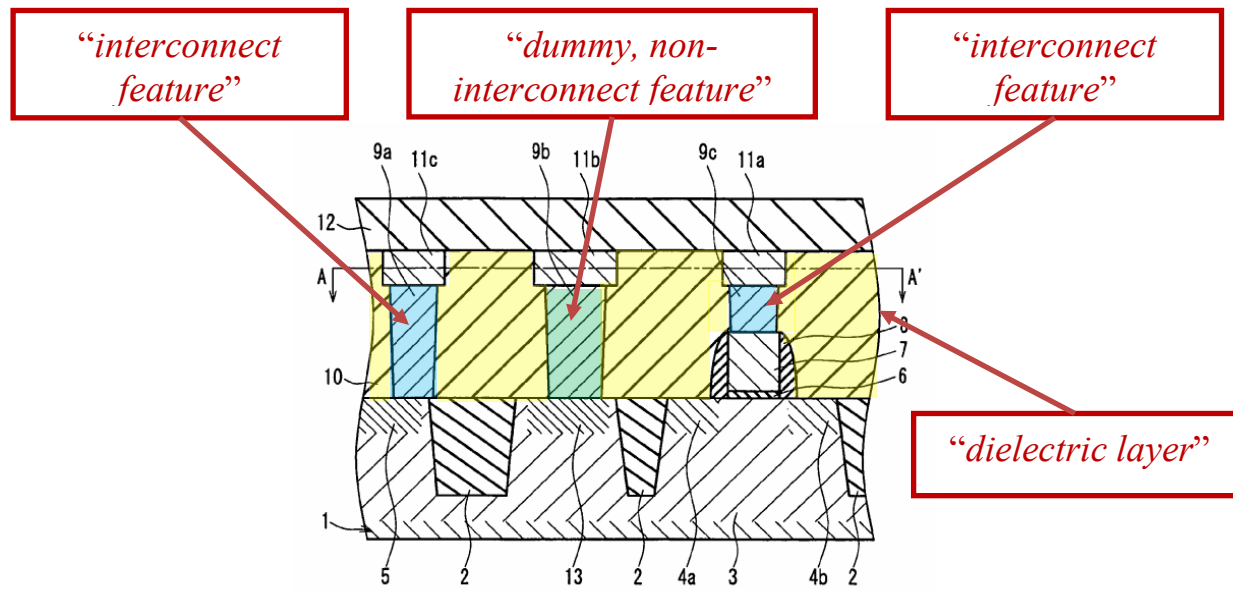
Provided below is a modified Figure 1A of Eriguchi, illustrating how a POSITA would have applied Wolf’s conventional and well known techniques, at the “post-etch condition,” to form Eriguchi’s MOS transistor that includes contact holes (“*interconnect recessed trench*”) for functional plugs and a dummy contact hole (“*dummy recessed trench*”) for dummy plug in dielectric layer 10 (“*dielectric layer*”). Ex.1003, ¶¶264-265.

Second, Eriguchi discloses that the holes are “*fill[ed]*” with “*conductive materials to form an interconnect feature and a dummy, non-interconnect feature.*”

For example, in the context of Figures 1A and 2, Eriguchi explains that “**these contact holes are filled with tungsten to form the W plugs 9a to 9c.**” Ex.1007, [0090]. A POSITA would have understood that filling the contact holes discloses “*filling*” and that tungsten (a metal material) plugs in the contact and dummy contact holes correspond to “*conductive materials.*” Ex.1003, ¶268.

Eriguchi’s dummy plug 9b is “*non-interconnect*” as that term is used in the ’584 patent since it “**does not contribute to the function of the semiconductor device**” and grounded to the substrate. Ex.1007, [0082]; [1.4.2] (*non-interconnect feature is...grounded to said semiconductor substrate*). Ex.1003, ¶269.

As illustrated below at Figure 1A, reproduced below, after the metal deposition process, the MOS transistor’s contact holes have the functional plugs 9a and 9c and the dummy contact hole has a dummy plug 9b. Ex.1003, ¶¶270-271.



Ex.1007, FIG. 1A (annotated).

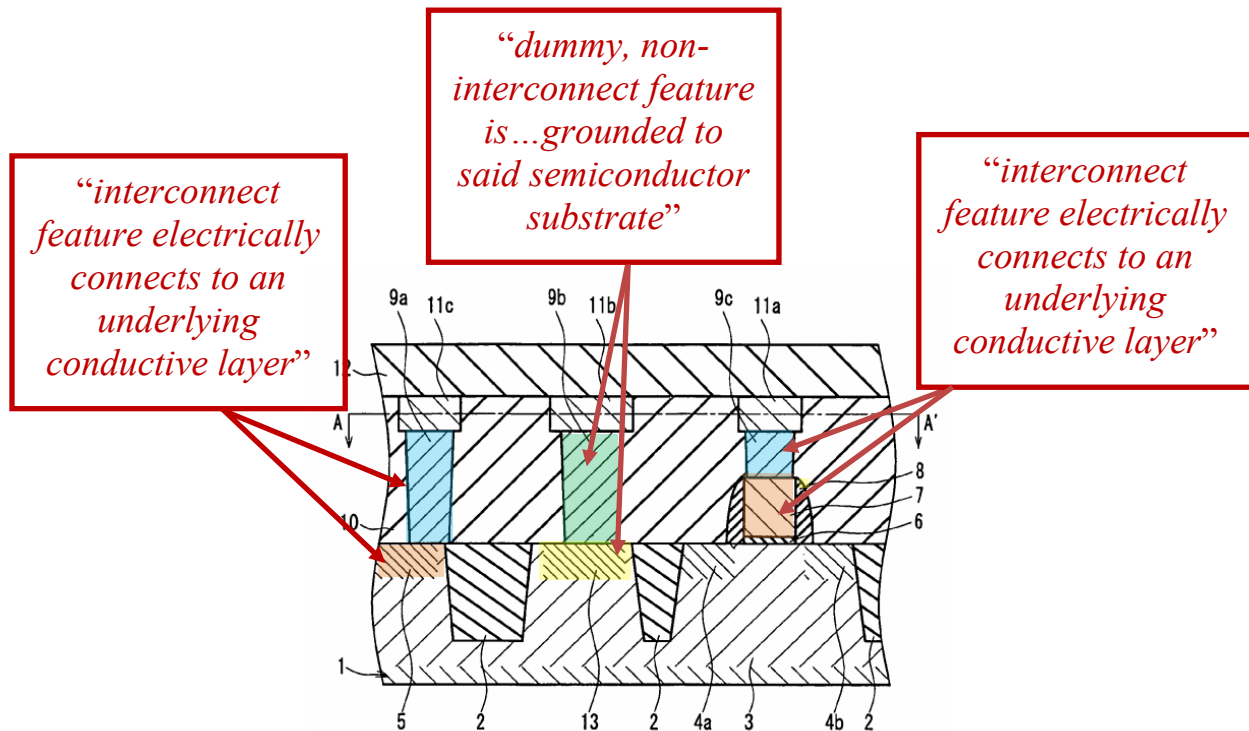
[1.4.2] wherein said interconnect feature electrically connects to an underlying conductive layer, while said dummy, non-interconnect feature is floating or grounded to said semiconductor substrate;

First, as analyzed at Ground 7 limitation [1.4.1], Eriguchi discloses functional plugs 9a and 9c, which separately and together correspond to “said interconnect feature,” and a dummy nonfunctional plug 9b, which corresponds to “said dummy, non-interconnect feature.” Ex.1003, ¶¶272-273.

Second, as already noted above, in Eriguchi’s Figure 1A, “the gate electrode 7 [is connected] via a W (tungsten) plug 9c” and the “source and drain...n+ region 5 [is connected] via a W (tungsten) plug 9a.” Ex.1007, [0081]. Additionally, Eriguchi discloses that “dummy conductor... does not contribute to the function of the semiconductor device” and is “connected

to...active region 13 via the W plug 9b.” Ex.1007, [0082], [0084]; *see also* Ex.1007, [0040]-[0041]. Eriguchi further explains that “active region (n+ region) 13...does not serve as either a source region or a drain region.” Ex.1007, [0085]. A POSITA would have understood that both gate electrode 7 and source/drain region 5 correspond to a “*conductive layer*” because these layers are used in circuit operation to switch the MOS transistor. Also, a POSITA would have understood that n+ region 13 is a n-type doped region that is provided to reduce contact resistance between the dummy conductor 9b and the substrate 1 and thus serves to “*ground[]*” to the substrate 1 since n+ region 13 is in the substrate 1. Ex.1003, ¶274.

As illustrated at Figure 1A, reproduced below, Eriguchi’s functional plug 9a is electrically connected to underlying source/drain region 5, functional plug 9c is electrically connected to underlying gate electrode 7, and dummy nonfunctional plug 9b is grounded to the substrate by being connected to the n+ region 13 in the substrate. Ex.1003, ¶¶275-276.



Ex.1007, FIG. 1A (annotated).

[1.5] wherein said dummy, non-interconnect opening increases an in-die shunt path current flow during said plasma etching process, thereby reducing charge damage to said integrated circuit dies.

First, as analyzed at Ground 7 limitation [1.1.1], Eriguchi in combination with Quirk discloses a silicon substrate 1 implemented as a wafer that includes a number of integrated circuit dies (each die including a MOS transistor), which renders obvious “*said integrated circuit dies.*” Further, as analyzed at Ground 7 limitation [1.2.1], Eriguchi in combination with Wolf renders obvious using a photoresist mask with a dummy opening (for dummy nonfunctional plug 9b), which corresponds to the “*dummy, non-interconnect opening.*” Furthermore, as

analyzed at Ground 7 limitation [1.3], Eriguchi in combination with Wolf renders obvious that the dummy opening in the photoresist mask is used in a plasma etching process, which corresponds to the “*plasma etching process*.” Ex.1003, ¶¶277-278.

Second, Eriguchi recognizes that due to plasma processing charging damage, “device characteristics are deteriorated, so that the semiconductor device is defective.” Ex.1007, [0006]. To address this concern, Eriguchi seeks to “**suppress plasma charging damage in a plasma process,**” including during “**plasma etching**.” Ex.1007, [0003]-[0004], [0037]. Specifically, Eriguchi’s method “**in which the occurrence of plasma charging damage is suppressed**” includes a process that “**simultaneously**” forms functional and dummy conductors. Ex.1007, [0070], [0075]-[0087], claim 21; *see also* Ex.1007, [0088]-[0095]. Thus, “the deterioration of the device characteristics due to breakdown of the gate insulating film 6 can be suppressed.” Ex.1007, [0094]; Ex.1003, ¶279.

A POSITA would have understood that because the process simultaneously forms the functional and dummy conductors, during the plasma etching process (see [1.3]) the dummy contact hole provides a shunt electrical path that enables the current to flow to an alternative point, i.e., to the substrate 1 via the n+ region 13. Ex.1008, 1:66-2:6; *see also* Ex.1005, [0019] (“... prevent charging damage in the plasma processes, such as RIE...when processing the connecting holes or

interconnection grooves, making it possible to prevent damage to the gate insulating films.”). Because Eriguchi’s dummy contact hole (for dummy nonfunctional plug 9b) as defined by the mask dummy opening, supplies electric charges to the substrate 1 via the n⁺ region 13 during the plasma etching process, Eriguchi’s renders obvious that the dummy, non-interconnect opening “*increases an in-die shunt path current flow during said plasma etching process.*” Ex.1003, ¶280.

Moreover, because, as analyzed above, the MOS transistors are within the integrated circuit die, suppressing charge damage to the MOS transistor, e.g., gate insulating film 6, “*thereby reduc[es] charge damage to said integrated circuit dies.*” Ex.1003, ¶¶281-282.

6. Claim 3

[3.0] The method according to claim 1 wherein said mask comprises photoresist.

As analyzed at Ground 7 limitation [1.2.1], in Eriguchi’s method the prior art combination uses a photoresist as a mask. Ex.1003, ¶283.

7. Claim 4

[4.0] The method according to claim 1 wherein said interconnect recessed trench is a damascene opening.

As analyzed at Ground 7 limitations [1.2.1]-[1.3], the prior art contact holes for functional plugs 9a and 9c are formed in a dual damascene process and thus are “a damascene opening.” Ex.1003, ¶284.

8. Claim 5

[5.0] The method according to claim 1 wherein said interconnect recessed trench is a contact hole.

As analyzed at Ground 7 limitations [1.3] and [1.4.1]-[1.4.2], the prior art interconnect recessed trench provides a contact to the gate (or source/drain) and thus is a contact hole. Ex.1003, ¶285.

9. Claim 6

[6.0] The method according to claim 1 wherein said underlying conductive layer comprises metal wiring and diffusion region.

The analysis in claim 1 focused on Eriguchi's embodiment of Figure 1A. Additionally, Eriguchi's discloses a further embodiment, in Figure 10A, where a functional conductor 127a is formed over a conducting line 123 and an active region 105 in the substrate 101. Ex.1007, [0138]-[0141]. The embodiment of Figure 10A, similarly has the ability to reduce "the total electrical stress applied to the gate insulating film 106." Ex.1007, [0144]; Ex.1003, ¶¶286-287.

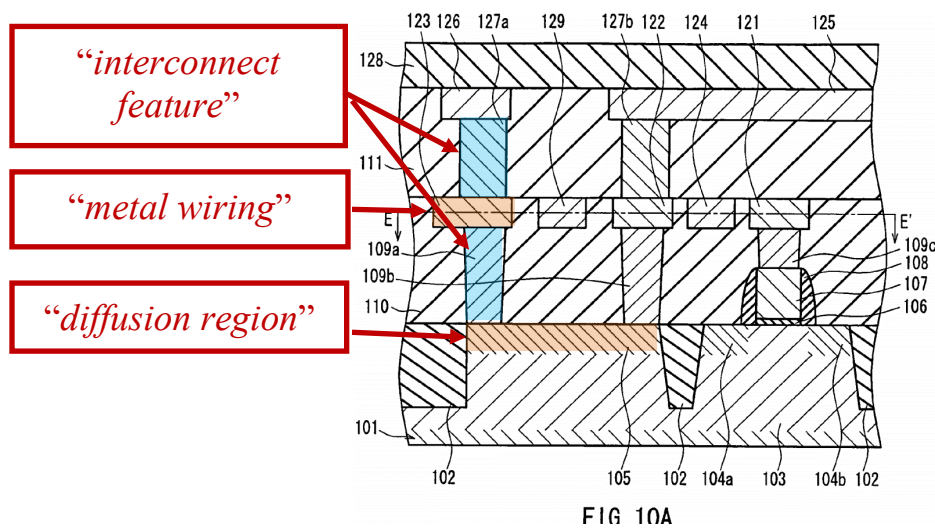


FIG 10A
Ex.1007, FIG. 10A (annotated).

Eriguchi discloses that the “active region 105 ... [is] formed by ion implantation of, for example, boron (B) ions.” Ex.1007, [0125]. A POSITA would have understood that active region 105 formed by ion implantation of a dopant needs to be heated in an annealing that causes the dopant to “diffuse” to proper location and thus a “diffusion region.” In the further embodiment of Figure 10A, functional conductor 127a, separately and together with functional conductor 109a, would correspond to the “*interconnect feature*,” while the metal line 123 and the active region 105 (a diffusion region, Ex.1007, [0117]), would correspond to the “*underlying conductive layer...[that] comprises metal wiring and diffusion region*.” Ex.1003, ¶288.

It would have been obvious to a POSITA to combine Eriguchi’s embodiment of Figure 1A with the teachings of Figure 10A, when implementing

integrated circuit dies (see analysis at Ground 7 limitation [1.1.1]), so that the charging damage can be suppressed even if an electric field is applied in the reverse direction. Ex.1007, [0032], [0130], [0144]-[0145]; Ex.1003, ¶¶289-290.

XI. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

Respectfully submitted,

Dated: September 19, 2025
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XII. MANDATORY NOTICES

A. Real party-in-interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that the real party-in-interest is Taiwan Semiconductor Manufacturing Company Ltd.

B. Related matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the '584 patent is not involved in any other matters.

C. Lead and back-up counsel and service information

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Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above.

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,054. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: September 19, 2025

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CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service September 19, 2025

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 7,547,584;
Petitioner's Power of Attorney;
Petitioner's Exhibit List;
Exhibits 1001-1018.

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