

Docket No.: 085393-0824

**REQUEST FORM FOR CONTINUATION
APPLICATION UNDER 35 USC 111(a)**

Prior Application: International Application No. PCT/JP2010/007402

Art Unit:(Unassigned)

Examiner:(Unassigned)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Request for filing a continuation application, entitled **SEMICONDUCTOR
MEMORY DEVICE**, under 35 U.S.C. 111(a) of pending prior International Application No. **PCT/JP2010/007402**, filed on **December 21, 2010**, by the following named inventor(s):

INVENTOR	RESIDENCE	CITIZENSHIP	POST OFFICE ADDRESS
Reiji MOCHIDA	Osaka, Japan	Japanese	c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma- shi, Osaka Japan 571-8501
Takafumi MARUYAMA	Osaka, Japan	Japanese	c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma- shi, Osaka Japan 571-8501
Yukimasa HAMAMOTO	Kyoto, Japan	Japanese	c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma- shi, Osaka Japan 571-8501

☒ I hereby verify, to the best of my knowledge, that the enclosed copy of this prior application is a true copy of the above-identified prior application, including the oath or declaration as originally filed.

☐ Preliminary Amendment is enclosed.

☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.

☐ Cancel claims

☐ Applicant is entitled to claim Small Entity status.

The filing fee is calculated on the basis of the claims existing in the prior application as amended above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	21	-20	1	\$60.00	\$60.00
Independent Claims	2	-3	0	\$250.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$310.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$380.00
Patent Search Fee					\$620.00
Patent Examination Fee					\$250.00
Total of Above Calculations					\$1310.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1310.00

☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees including any extension of time fees or credit any overpayment to Deposit Account No. 500417.

1. ☐ Amend the specification by inserting before the first line the sentence:
2. ☒ Priority of Japanese Application No. 2010-052722 filed on March 10, 2010, in Japan and International Application No. PCT/JP2010/007402 filed December 21, 2010 designating the U.S. is claimed under 35 USC 119, 120 and/or 365.
3. ☒ The prior application is assigned of record to

Panasonic Corporation
Kadoma-shi, Osaka, Japan 571-8501

4. ☒ The power of attorney in the prior application is to:

Maeda Patent Office
Chuo-ku, Osaka 541-0053 JAPAN

5. ☒ Also enclosed:

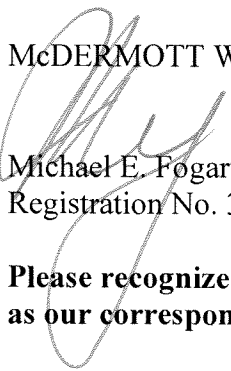
- **Executed Declaration and Power of Attorney**

- **Copy of Front page of Published International Application**
 - **Copy of PCT Request**
 - **Copy of PCT/IB/301**
 - **Copy of PCT/IB/304**
 - **Copy of PCT/IB/308**
 - **Copy of PCT/ISA/237**
 - **Copy of International Search Report**
6. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .
7. ☒ Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDERMOTT WILL & EMERY LLP
 600 13th Street, N.W.
 Washington, D.C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


 Michael E. Fogarty
 Registration No. 36,139

600 13th Street, N.W.
 Washington, DC 20005-3096
 Phone: 202.756.8000 MEF:mjb
 Facsimile: 202.756.8087
Date: August 22, 2012

**Please recognize our Customer No. 53080
 as our correspondence address.**

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE			
First Named Inventor/Applicant Name:	Reiji MOCHIDA			
Filer:	Michael E. Fogarty/Margaret Barham			
Attorney Docket Number:	085393-0824			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Claims in excess of 20	1202	1	60	60
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1310

Electronic Acknowledgement Receipt

EFS ID:	13562395
Application Number:	13591766
International Application Number:	
Confirmation Number:	2466
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Reiji MOCHIDA
Customer Number:	53080
Filer:	Michael E. Fogarty/Margaret Barham
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0824
Receipt Date:	22-AUG-2012
Filing Date:	
Time Stamp:	15:49:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1310
RAM confirmation Number	2270
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	P60241601_DEC_085393-0824.pdf	158930	no	3
			ac021e37932b6f19b0d27b977d997a2daf6bc842		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	P60241601_DRW_085393-0824.pdf	66771	no	5
			10981a6ea455f602edc138761ff4cc4295f84c90		
Warnings:					
Information:					
3	Transmittal Letter	P60241601_IDS_085393-0824.PDF	98667	no	5
			323e72f1c77aa53f805b0576cad8901ec2a7600		
Warnings:					
Information:					
4	Non Patent Literature	P60241601_ISR_085393-0824.pdf	148389	no	3
			383f606a3d5027b4b1084e9cdc55359559645fd1		
Warnings:					
Information:					
5	Miscellaneous Incoming Letter	P60241601_PCT_085393-0824.pdf	621058	no	14
			c640195d159e86dae6f91407919784d5b3eecca		
Warnings:					
Information:					
6	Foreign Reference	P60241601_REF_085393-0824.PDF	597655	no	18
			7c396d59b65743b42e71829cbefeb0dc69eed9b4		
Warnings:					
Information:					
7		P60241601_SPEC_CLAIMS_ABS T_085393-0824.pdf	905393	yes	25
			c8eed23832a2701aaab568696544cf42058fea5a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	16	
	Claims		17	24	
	Abstract		25	25	
SK hynix Ex. 1002, Page 7 of 145					

Warnings:					
Information:					
8	Transmittal of New Application	P60241601_TRN_085393-0824. PDF	62406 a62a84e9ace0af3aacee3a967dfd45d9ca3c1e2d	no	3
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	36399 e5a0a04f64ba5a1cd7d3ae7d8cc15f4b7de7efa8	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2695668		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Panasonic Ref: P602416-01

(* must be filled)

Japan Firm Name: MAEDA & PARTNERS

Application Serial No.

Japan Firm Ref: M10-512US1-YUS Firm Name: MWE

US Firm Ref: _____

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION(a) ☒ Original (b) ☐ Supplemental (c) ☐ Substitute (d) ☐ PCT (e) ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title of Invention:

SEMICONDUCTOR MEMORY DEVICE

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

1. For use when submitting this Declaration prior to U.S. application filing date

(f) ☒ the attached specification, or

2. For use when submitting this Declaration after U.S. application filing date

(g) ☐ the specification in the U.S. Application:Application No.
(if available)filed on:
(must be filled)

and with amendments (if applicable):

filed on

,or

3. For PCT-US national entry under 35 U.S.C. 371 (for use when filing this Declaration before and after the U.S. national entry date)

(h) ☐ the specification in the International Application:PCT
Application No.filed on:
(PCT filing date)

(Check here only for US national entry under 35 U.S.C. 371.)

and with amendments (if applicable):

filed on:

,

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

(Foreign Priority Information)

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2010-052722	March 10, 2010	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

(US Provisional Application Information)

APPLICATION NO.	U.S. PROVISIONAL APPLICATION FILING DATE

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Domestic Priority Information)

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED
PCT/JP2010/007402	December 21, 2010	Pending

☐ Additional U.S. or International application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with the U.S. Patent and Trademark Office Customer Number identified below to prosecute this application including divisions, continuations and reissues thereof in the United States and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Panasonic Corporation and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Power of Attorney given to practitioners associated with, and direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

INVENTOR (s)

Full Name of Sole or First Inventor	FIRST NAME Reiji	LAST NAME MOCHIDA	SIGNATURE <i>Reiji Mochida</i>	DATE OF SIGNATURE <i>July.12.2012</i>
Residence & Citizenship	CITY, STATE or COUNTRY Osaka, Japan			CITIZENSHIP JAPAN
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Full Name of Second Inventor	FIRST NAME Takafumi	LAST NAME MARUYAMA	SIGNATURE <i>Takafumi Maruyama</i>	DATE OF SIGNATURE <i>July.17.2012</i>
Residence & Citizenship	CITY, STATE or COUNTRY Osaka, Japan			CITIZENSHIP JAPAN
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Total of 3 pages are submitted.

INVENTOR (s)

Full Name of Third Inventor	FIRST NAME Yukimasa	LAST NAME HAMAMOTO	SIGNATURE <i>Yukimasa Hamamoto</i>	DATE OF SIGNATURE July 12, 2012
Residence & Citizenship	CITY, STATE or COUNTRY Kyoto, Japan			CITIZENSHIP JAPAN
Post office address	ADDRESS c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Full Name of Fourth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

Full Name of Fifth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

Full Name of Sixth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

Full Name of Seventh Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

Full Name of Eighth Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

☐ Check if additional paper(s) is/are attached.
Total of 3 pages are submitted.

FIG.3

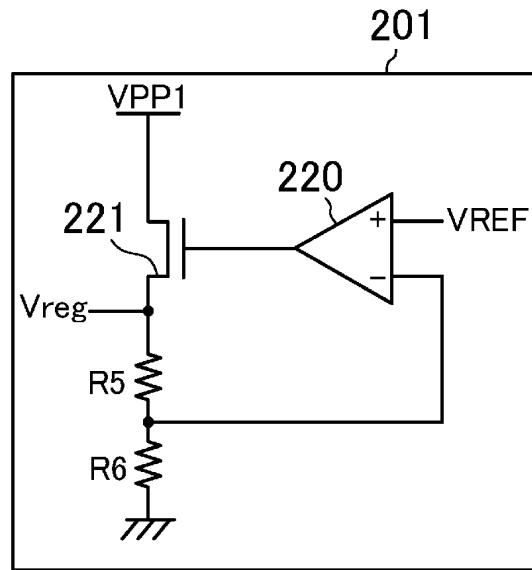


FIG.4

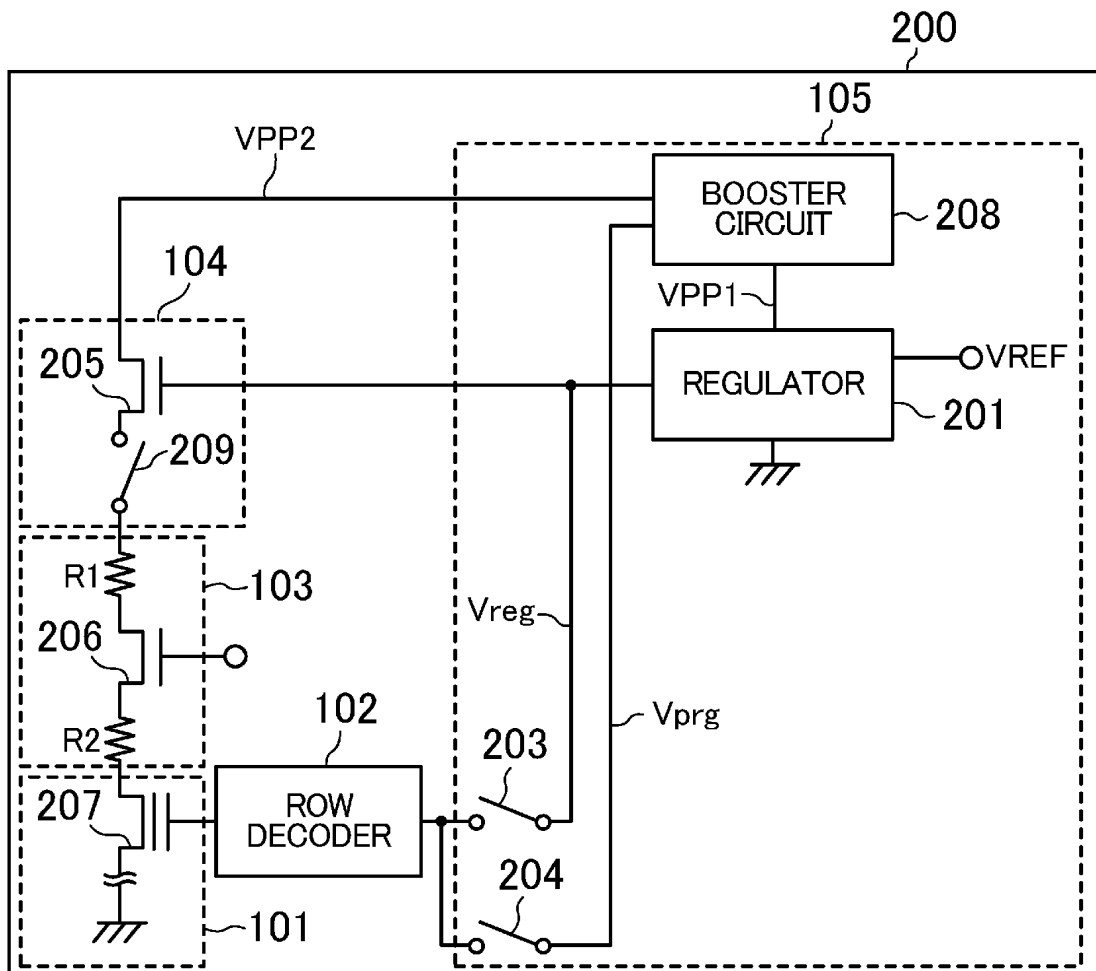


FIG.5

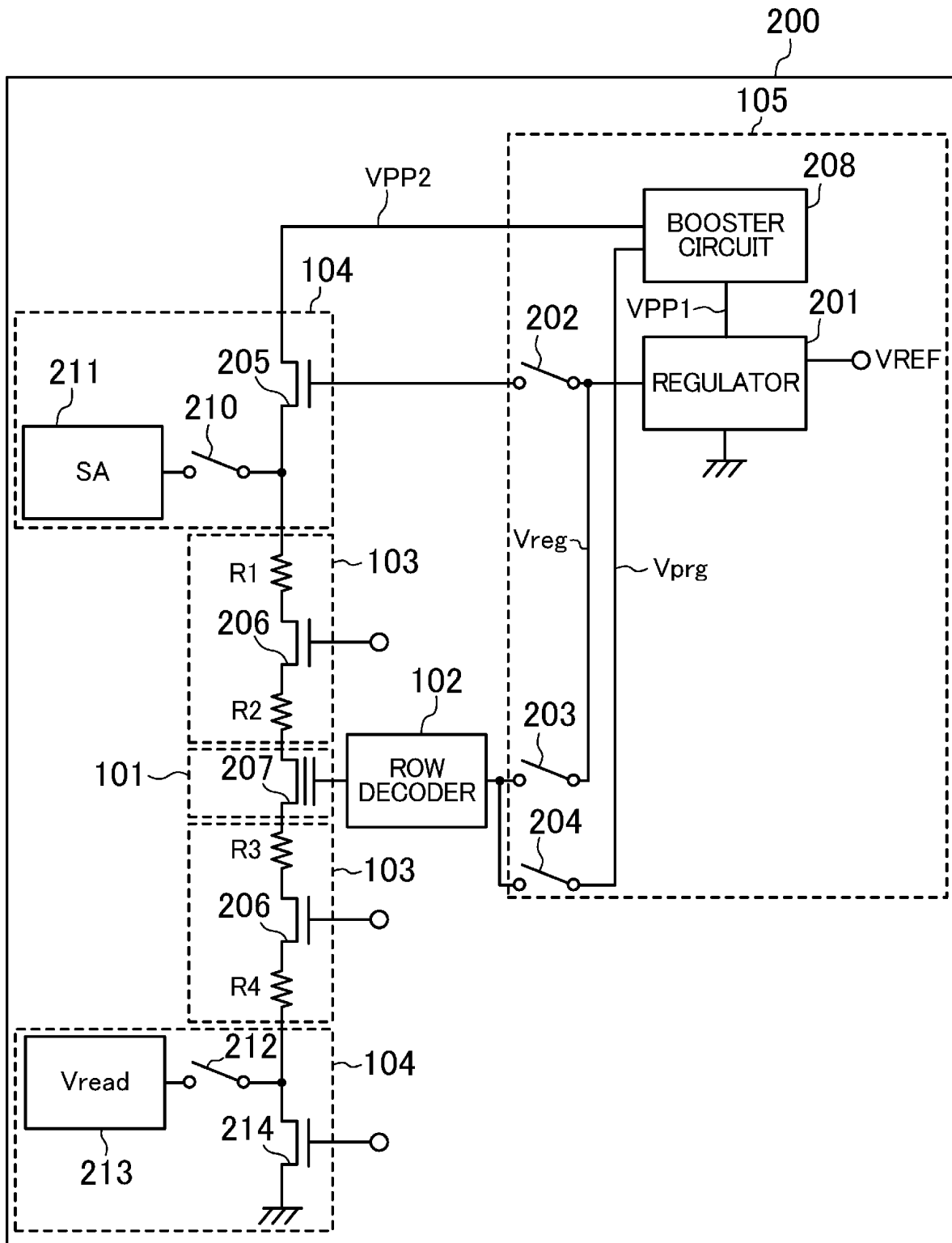
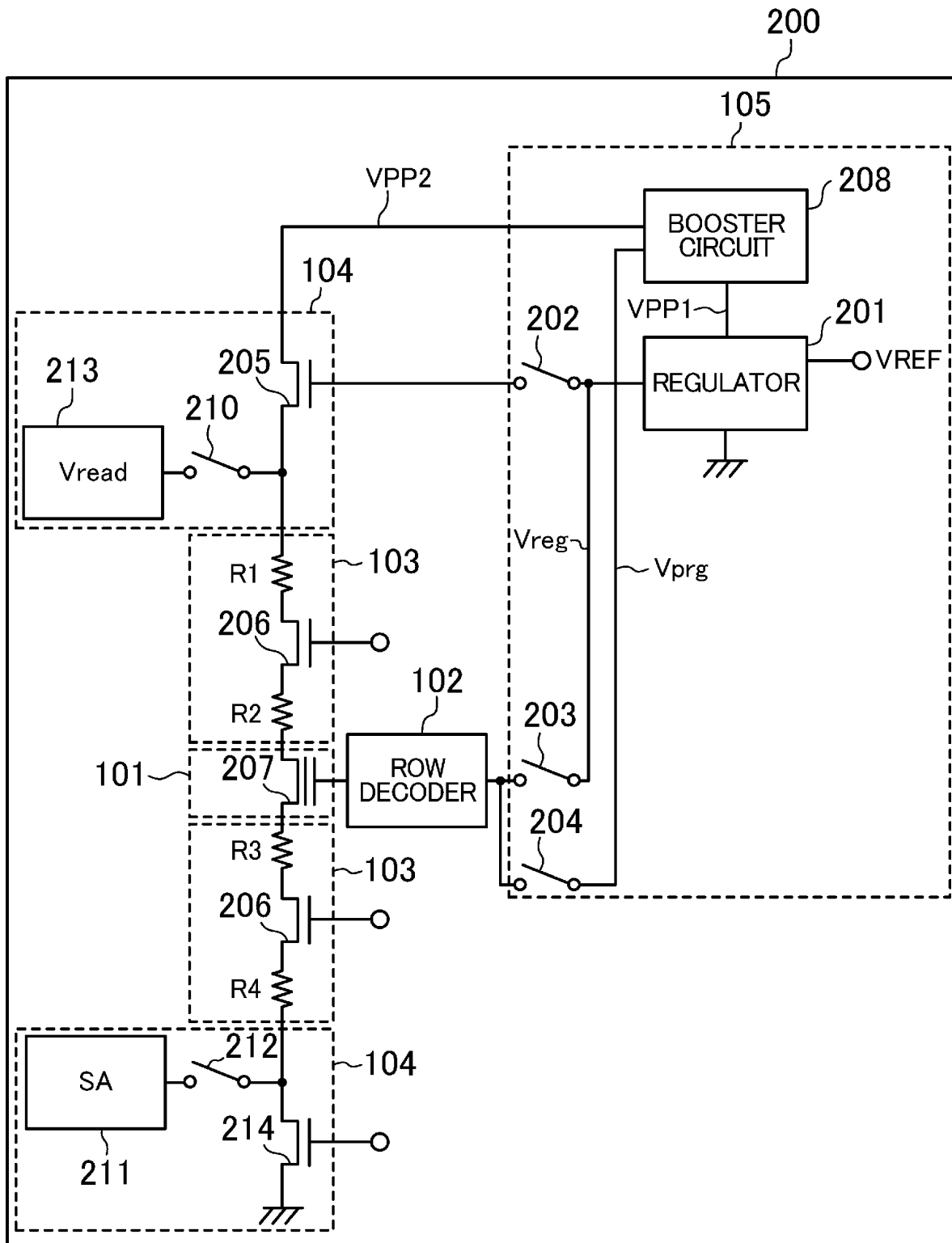
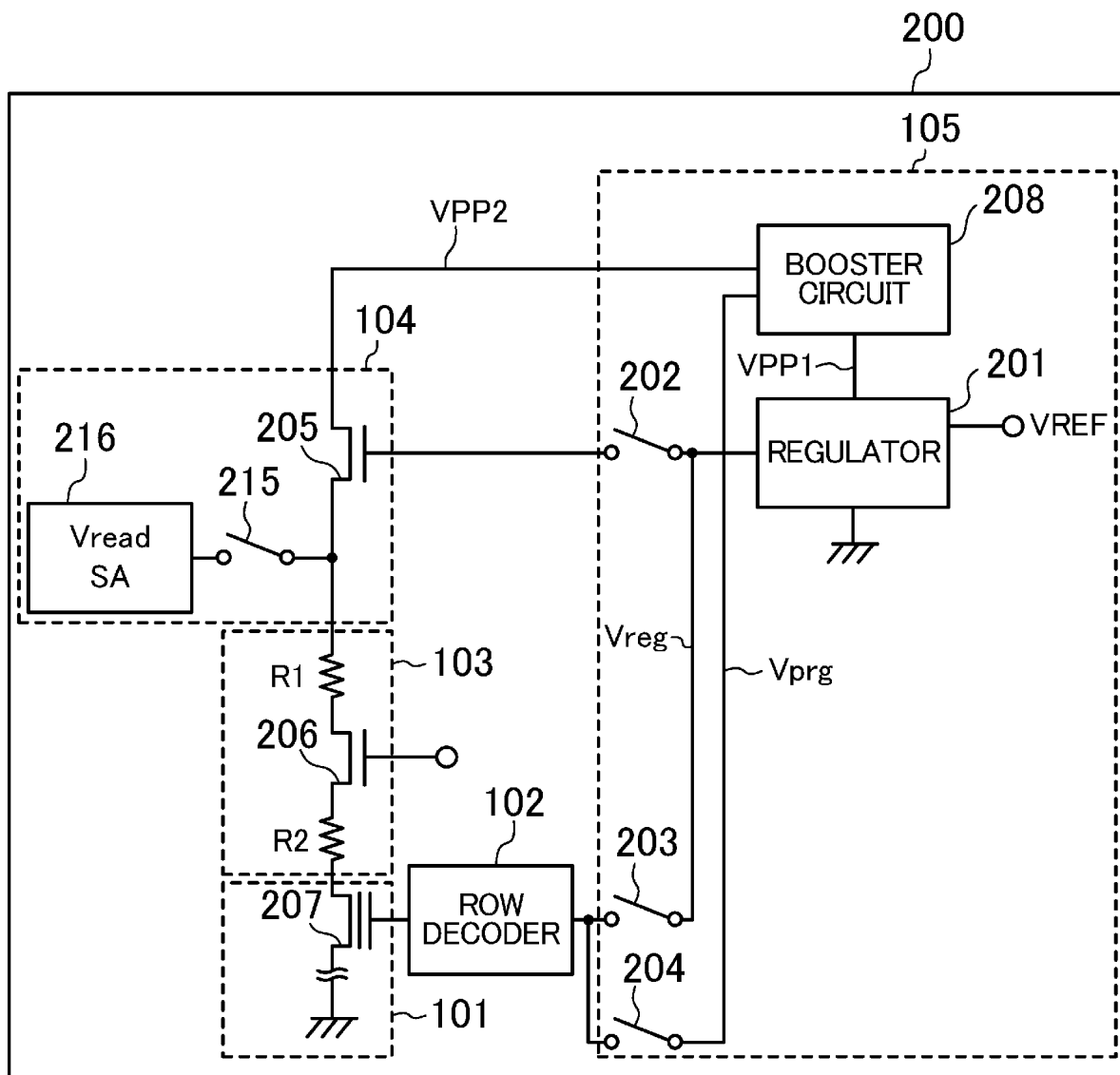


FIG.6





Docket No.: 085393-0824
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Reiji MOCHIDA et al.

Customer Number: 53080

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: August 22, 2012

Art Unit: N/A

For: SEMICONDUCTOR MEMORY DEVICE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A summary/abstract translation of the non-English language reference is enclosed.

Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

A concise explanation of relevance of the items listed on form PTO/SB/08 is (1) given and (2) in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references.

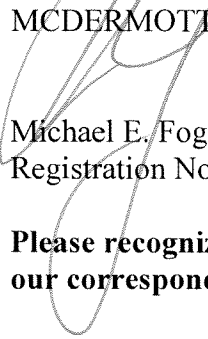
In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is “prior art” for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington DC, DC 20005-3096
Phone: (202) 756-8372 MEF:mjb
Facsimile: (202) 756-8087
Date: August 22, 2012

**Please recognize our Customer No. 53080 as
our correspondence address.**

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	Not Yet Assigned
Filing Date	August 22, 2012
First Named Inventor	Reiji MOCHIDA
Art Unit	N/A
Examiner Name	Not Yet Assigned
Attorney Docket Number	085393-0824

Sheet	1	of	2
-------	---	----	---

[illegible]

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	1-6
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	BA	JP-2008-217914-A	09-18-2008	Toshiba Corp	English abstract	

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	August 22, 2012
				First Named Inventor	Reiji MOCHIDA
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	085393-0824
Sheet	2	of	2		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	International Search Report issued in International Patent Application No. PCT/JP2010/007402 dated March 22, 2011	

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/007402

A. CLASSIFICATION OF SUBJECT MATTER

G11C16/06(2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C16/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2011
Kokai Jitsuyo Shinan Koho	1971-2011	Toroku Jitsuyo Shinan Koho	1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-217914 A (Toshiba Corp.), 18 September 2008 (18.09.2008), paragraphs [0049], [0050]; fig. 9 (Family: none)	1-21

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
09 March, 2011 (09.03.11)Date of mailing of the international search report
22 March, 2011 (22.03.11)Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

特許協力条約

PCT

国際調査報告

(法8条、法施行規則第40、41条)

[PCT18条、PCT規則43、44]



出願人又は代理人 M10-512CT1 の書類記号 P602416P0 -Y	今後の手続きについては、様式PCT/ISA/220 及び下記5を参照すること。	
国際出願番号 PCT/JP2010/007402	国際出願日 (日.月.年) 21.12.2010	優先日 (日.月.年) 10.03.2010
出願人 (氏名又は名称) パナソニック株式会社		

国際調査機関が作成したこの国際調査報告を法施行規則第41条 (PCT18条) の規定に従い出願人に送付する。
この写しは国際事務局にも送付される。

この国際調査報告は、全部で 2 ページである。

☐ この調査報告に引用された先行技術文献の写しも添付されている。

1. 国際調査報告の基礎

a. 言語に関し、この国際調査は以下のものに基づき行った。

☒ 出願時の言語による国際出願

☐ 出願時の言語から国際調査のための言語である _____ 語に翻訳された、
この国際出願の翻訳文 (PCT規則12.3(a) 及び23.1(b))

b. ☐ この国際調査報告は、PCT規則91の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した (PCT規則43.6の2(a))。

c. ☐ この国際出願は、ヌクレオチド又はアミノ酸配列を含んでいる (第I欄参照)。

2. ☐ 請求の範囲の一部の調査ができない (第II欄参照)。

3. ☐ 発明の単一性が欠如している (第III欄参照)。

4. 発明の名称は

☐ 出願人が提出したものを承認する。

☒ 次に示すように国際調査機関が作成した。

メモリセルのドレイン電圧用及びゲート電圧用のレギュレータを共有した
フラッシュメモリ

5. 要約は

☒ 出願人が提出したものを承認する。

☐ 第IV欄に示されているように、法施行規則第47条第1項 (PCT規則38.2) の規定により国際調査機関が作成した。出願人は、この国際調査報告の発送の日から1月以内にこの国際調査機関に意見を提出することができる。

6. 図面に関して

a. 要約書とともに公表される図は、

第 5 図とする。 ☒ 出願人が示したとおりである。

☐ 出願人は図を示さなかったもので、国際調査機関が選択した。

☐ 本図は発明の特徴を一層よく表しているもので、国際調査機関が選択した。

b. ☐ 要約とともに公表される図はない。

様式PCT/ISA/210 (第1ページ) (2009年7月) (改訂)

A. 発明の属する分野の分類 (国際特許分類 (IPC))

Int.Cl. G11C16/06(2006.01) i

B. 調査を行った分野

調査を行った最小限資料 (国際特許分類 (IPC))

Int.Cl. G11C16/06

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	1922-1996年
日本国公開実用新案公報	1971-2011年
日本国実用新案登録公報	1996-2011年
日本国登録実用新案公報	1994-2011年

国際調査で使用した電子データベース (データベースの名称、調査に使用した用語)

C. 関連すると認められる文献

引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号
A	JP 2008-217914 A (株式会社東芝) 2008.09.18, 段落【0049】、 【0050】、第9図 (ファミリーなし)	1-21

☐ C欄の続きにも文献が列挙されている。☐ パテントファミリーに関する別紙を参照。

* 引用文献のカテゴリー

「A」 特に関連のある文献ではなく、一般的技術水準を示すもの

「E」 国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの

「L」 優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献 (理由を付す)

「O」 口頭による開示、使用、展示等に言及する文献

「P」 国際出願日前で、かつ優先権の主張の基礎となる出願

の日の後に公表された文献

「T」 国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの

「X」 特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの

「Y」 特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの

「&」 同一パテントファミリー文献

国際調査を完了した日

09.03.2011

国際調査報告の発送日

22.03.2011

国際調査機関の名称及びあて先

日本国特許庁 (ISA/J P)

郵便番号 100-8915

東京都千代田区霞が関三丁目4番3号

特許庁審査官 (権限のある職員)

滝谷 亮一

5N

3135

電話番号 03-3581-1101 内線 3586

特許協力条約に基づく国際出願願書

紙面による写し (注意 電子データが原本となります)

0	受理官庁記入欄	
0-1	国際出願番号	
0-2	国際出願日	
0-3	(受付印)	
0-4	様式 PCT/RO/101 この特許協力条約に基づく国際出願願書は、	
0-4-1	右記によって作成された。	PCT-SAFE Version 3.51.041.217 MT/FOP 20090701/0.20.5.17
0-5	申立て 出願人は、この国際出願が特許協力条約に従って処理されることを請求する。	
0-6	出願人によって指定された受理官庁	日本国特許庁 (RO/JP)
0-7	出願人又は代理人の書類記号	P602416P0
I	発明の名称	半導体記憶装置
II	出願人	
II-1	この欄に記載した者は	出願人である (applicant only)
II-2	右の指定国についての出願人である。	米国を除く全ての指定国 (all designated States except US)
II-4ja	名称	パナソニック株式会社
II-4en	Name:	PANASONIC CORPORATION
II-5ja	あて名	5718501
II-5en	Address:	日本国 大阪府門真市大字門真 1 0 0 6 番地 1006, Oaza Kadoma, Kadoma-shi, Osaka 5718501 Japan
II-6	国籍(国名)	日本国 JP
II-7	住所(国名)	日本国 JP
II-8	電話番号	06-6908-1473
II-9	ファクシミリ番号	06-6909-0053
III-1	その他の出願人又は発明者	
III-1-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-1-2	右の指定国についての出願人である。	米国のみ (US only)
III-1-4ja	氏名(姓名)	持田礼司
III-1-4en	Name (LAST, First):	MOCHIDA, Reiji
III-1-5ja	あて名	
III-1-5en	Address:	
III-1-6	国籍(国名)	
III-1-7	住所(国名)	

特許協力条約に基づく国際出願願書

紙面による写し (注意 電子データが原本となります)

III-2	その他の出願人又は発明者	
III-2-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-2-2	右の指定国についての出願人である。	米国のみ (US only)
III-2-4ja	氏名(姓名)	圓山敬史
III-2-4en	Name (LAST, First):	MARUYAMA, Takafumi
III-2-5ja	あて名	
III-2-5en	Address:	
III-2-6	国籍(国名)	
III-2-7	住所(国名)	
III-3	その他の出願人又は発明者	
III-3-1	この欄に記載した者は	出願人及び発明者である (applicant and inventor)
III-3-2	右の指定国についての出願人である。	米国のみ (US only)
III-3-4ja	氏名(姓名)	濱本幸昌
III-3-4en	Name (LAST, First):	HAMAMOTO, Yukimasa
III-3-5ja	あて名	
III-3-5en	Address:	
III-3-6	国籍(国名)	
III-3-7	住所(国名)	
IV-1	代理人又は共通の代表者、通知のあて名 下記の者は国際機関において右記のごとく出願人のために行動する。	代理人 (agent)
IV-1-1ja	氏名(姓名)	前田弘
IV-1-1en	Name (LAST, First):	MAEDA, Hiroshi
IV-1-2ja	あて名	5410053 日本国 大阪府大阪市中央区本町2丁目5番7号 大阪丸紅ビル
IV-1-2en	Address:	Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome, Chuo-ku, Osaka-shi, Osaka 5410053 Japan
IV-1-3	電話番号	06-6125-2255
IV-1-4	ファクシミリ番号	06-6125-2288
IV-1-6	代理人登録番号	100077931
IV-2	その他の代理人	筆頭代理人と同じあて名を有する代理人 (additional agent(s) with the same address as first named agent)
IV-2-1ja	氏名	原田智雄(100117710); 井関勝守(100121728); 前田亮(100143409)
IV-2-1en	Names(s)	HARADA, Tomoo(100117710); ISEKI, Katsumori(100121728); MAEDA, Ryo(100143409)
V	国の指定	
V-1	この願書を用いてされた国際出願は、規則 4.9(a)に基づき、国際出願の時点で拘束さ れる全てのPCT締約国を指定し、取得しうる あらゆる種類の保護を求め、及び該当する 場合には広域と国内特許の両方を求める 国際出願となる。	

特許協力条約に基づく国際出願願書

紙面による写し(注意 電子データが原本となります)

VI-1	先の国内出願に基づく優先権主張		
VI-1-1	出願日	2010年 03月 10日 (10.03.2010)	
VI-1-2	出願番号	2010-052722	
VI-1-3	国名	日本国 JP	
VI-2	優先権証明書送付の請求 上記の先の出願のうち、右記の番号のものについては、出願書類の認証謄本を作成し国際事務局へ送付することを、受理官庁に対して請求している。	VI-1	
VI-3	引用による補充: 条約第11条(1)(iii)(d)若しくは(e)に規定する国際出願の要素の全部、又は規則20.5(a)に規定する明細書、請求の範囲若しくは図面の一部がこの国際出願には含まれていないが、受理官庁が条約第11条(1)(ii)に規定する要素の1つ以上を最初に受領した日において優先権を主張する先の出願にそれが完全に含まれている場合には、規則20.6に基づく確認の手続きを条件として、その要素又は部分を規則20.6の規定によりこの国際出願に引用して補充することを請求する。		
VII-1	特定された国際調査機関(ISA)	日本国特許庁 (ISA/JP)	
VIII	申立て	申立て数	
VIII-1	発明者の特定に関する申立て	-	
VIII-2	出願し及び特許を与えられる国際出願日における出願人の資格に関する申立て	-	
VIII-3	先の出願の優先権を主張する国際出願日における出願人の資格に関する申立て	-	
VIII-4	発明者である旨の申立て(米国を指定国とする場合)	-	
VIII-5	不利にならない開示又は新規性喪失の例外に関する申立て	-	
IX	照合欄	用紙の枚数	添付された電子データ
IX-1	願書(申立てを含む)	4	✓
IX-2	明細書	15	✓
IX-3	請求の範囲	8	✓
IX-4	要約	1	✓
IX-5	図面	5	✓
IX-7	合計	33	
	添付書類	添付	添付された電子データ
IX-8	手数料計算用紙	-	✓
IX-18	PCT-SAFE 電子出願	-	-
IX-20	要約とともに提示する図の番号	5	
IX-21	国際出願の使用言語名	日本語	
X-1	出願人、代理人又は代表者の記名押印	(PKCS7 デジタル署名)	
X-1-1	氏名(姓名)	前田弘	
X-1-2	署名者の氏名		
X-1-3	権限		

特許協力条約に基づく国際出願願書

紙面による写し(注意 電子データが原本となります)

受理官庁記入欄

10-1	国際出願として提出された書類 の実際の受理の日	
10-2	図面	
10-2-1	受理された	
10-2-2	不足図面がある	
10-3	国際出願として提出された書類 を補充する書類又は図面であつ てその後期間内に提出されたも のの実際の受理の日(訂正日)	
10-4	特許協力条約第11条(2)に基づ く必要な補充の期間内の受理の日	
10-5	出願人により特定された国際調査機関	ISA/JP
10-6	調査手数料未払いにつき、国際 調査機関に調査用写しを送付していない	

国際事務局記入欄

11-1	記録原本の受理の日	
------	-----------	--

From the INTERNATIONAL BUREAU

PCTNOTIFICATION OF RECEIPT OF
RECORD COPY

(PCT Rule 24.2(a))

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome,
Chuo-ku, Osaka-shi, Osaka
5410053
JAPON

JAN 16 2011

MAEDA PATENT OFFICE

Date of mailing (day/month/year) 31 January 2011 (31.01.2011)	IMPORTANT NOTIFICATION
Applicant's or agent's file reference P602416P0 M/0-512 CT1-Y	International application No. PCT/JP2010/007402

The applicant is hereby notified that the International Bureau has received the record copy of the international application as detailed below.

Name(s) of the applicant(s) and State(s) for which they are applicants:

PANASONIC CORPORATION (for all designated States except US)
MOCHIDA, Reiji et al (for US)

International filing date: 21 December 2010 (21.12.2010)

Priority date(s) claimed: 10 March 2010 (10.03.2010)

Date of receipt of the record copy by the International Bureau: 12 January 2011 (12.01.2011)

List of designated Offices:

AP: BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW

EA: AM, AZ, BY, KG, KZ, MD, RU, TJ, TM

EP: AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR

PA: BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

National: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

ATTENTION: The applicant should carefully check the data appearing in this Notification. In case of any discrepancy between these data and the indications in the international application, the applicant should immediately inform the International Bureau. In addition, the applicant's attention is drawn to:

- time limits for entry into the national phase (see www.wipo.int/pct/en/texts/time_limits.html and *PCT Applicant's Guide*, National Phase, especially Chapters 3 and 4)
- requirements regarding priority documents (if applicable) (see *PCT Applicant's Guide*, International Phase, paragraph 5.070)

A copy of this notification is being sent to the receiving Office and to the International Searching Authority.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Asakura Yo e-mail pt07.pct@wipo.int Telephone No. +41 22 338 74 07
Facsimile No. +41 22 338 90 90	

From the INTERNATIONAL BUREAU

PCTNOTIFICATION CONCERNING SUBMISSION,
OBTENTION OR TRANSMITTAL
OF PRIORITY DOCUMENT

(PCT Administrative Instructions, Section 411)

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome,
Chuo-ku, Osaka-shi, Osaka
5410053
JAPON

Date of mailing (day/month/year) 14 February 2011 (14.02.2011)			
Applicant's or agent's file reference P602416P0 M10-512 CT1 40	IMPORTANT NOTIFICATION		
International application No. PCT/JP2010/007402	International filing date (day/month/year) 21 December 2010 (21.12.2010)		
International publication date (day/month/year) Not yet published	Priority date (day/month/year) 10 March 2010 (10.03.2010)		
Applicant PANASONIC CORPORATION et al			

The applicant is hereby notified of the date of receipt (or of obtaining by the International Bureau) of the priority document(s) relating to all earlier application(s) whose priority is claimed. Unless otherwise indicated by the letters "NR", in the right-hand column or by an asterisk appearing next to the date of receipt, the priority document concerned was submitted or transmitted to or obtained by the International Bureau in compliance with Rule 17.1(a), (b) or (b-bis). This Form replaces any previously issued notification concerning submission, transmittal or obtaining of priority documents.

<u>Priority date</u>	<u>Priority application No.</u>	<u>Country or regional Office or PCT receiving Office</u>	<u>Date of receipt of priority document</u>
10 March 2010 (10.03.2010)	2010-052722	JP	09 February 2011 (09.02.2011)

The letters "NR" denote a priority document which, on the date of mailing of this Form, had not yet been received or obtained by the International Bureau in compliance with Rule 17.1(a), (b) or (b-bis). Where the applicant has failed to either submit, request to transmit or obtain and transmit the priority document within the applicable time limit under that Rule, the attention of the applicant is directed to Rule 17.1(c) which provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

An asterisk "*" next to a date of receipt, denotes a priority document submitted or transmitted to or obtained by the International Bureau but not in compliance with Rule 17.1(a), (b) or (b-bis) (the priority document was received after the time limit prescribed in Rule 17.1(a); the request to prepare and transmit the priority document was submitted to the receiving Office after the applicable time limit under Rule 17.1(b) or the request to the receiving Office or the International Bureau to obtain the priority document was made after the applicable time limit under Rule 17.1(b-bis)). Even though the priority document was not furnished in compliance with Rule 17.1(a), (b) or (b-bis), the International Bureau will nevertheless transmit a copy of the document to the designated Offices, for their consideration. In case such a copy is not accepted by the designated Office as the priority document, Rule 17.1(c) provides that no designated Office may disregard the priority claim concerned before giving the applicant an opportunity, upon entry into the national phase, to furnish the priority document within a time limit which is reasonable under the circumstances.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Gijsbertus Beijer e-mail pt07.pct@wipo.int Telephone No. +41 22 338 74 07
---	---

Facsimile No. +41 22 338 90 90

Form PCT/IB/304 (July 2010)

1/ERFT5DKSO

From the INTERNATIONAL BUREAU

PCT

SECOND AND SUPPLEMENTARY NOTICE
INFORMING THE APPLICANT OF THE
COMMUNICATION OF THE INTERNATIONAL
APPLICATION (TO DESIGNATED OFFICES
WHICH APPLY THE 30 MONTH TIME
LIMIT UNDER ARTICLE 22(1))

(PCT Rule 47.1(c))

To:

MAEDA, Hiroshi
Osaka-Marubeni Bldg., 5-7, Hommachi 2-chome,
Chuo-ku, Osaka-shi, Osaka
5410053
JAPON

Date of mailing (day/month/year) 12 July 2012 (12.07.2012)		
Applicant's or agent's file reference P602416P0		IMPORTANT NOTICE
International application No. PCT/JP2010/007402	International filing date (day/month/year) 21 December 2010 (21.12.2010)	Priority date (day/month/year) 10 March 2010 (10.03.2010)
Applicant PANASONIC CORPORATION et al		

- ATTENTION:** For any designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002 (30 months from the priority date), **does not apply**, please see Form PCT/IB/308(First Notice) issued previously.
- Notice is hereby given that the following designated Office(s), for which the time limit under Article 22(1), as in force from 1 April 2002, **does apply**, has/have requested that the communication of the international application, as provided for in Article 20, be effected under Rule 93bis.1. The International Bureau has effected that communication on the date indicated below:
15 September 2011 (15.09.2011)

AU, AZ, BY, CN, CO, DZ, EP, HU, KG, KP, KR, MD, MK, MY, MZ, NA, NG, PG, RU, SY, TM, US

In accordance with Rule 47.1(c-bis)(i), those Offices will accept the present notice as conclusive evidence that the communication of the international application has duly taken place on the date of mailing indicated above and no copy of the international application is required to be furnished by the applicant to the designated Office(s).

- The following designated Offices, for which the time limit under Article 22(1), as in force from 1 April 2002, **does apply**, have not requested, as at the time of mailing of the present notice, that the communication of the international application be effected under Rule 93bis.1 :

AE, AG, AL, AM, AO, AP, AT, BA, BB, BG, BH, BR, BW, BZ, CA, CH, CL, CR, CU, CZ, DE, DK, DM, DO, EA, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, ID, IL, IN, IS, JP, KE, KM, KN, KZ, LA, LC, LK, LR, LS, LT, LY, MA, ME, MG, MN, MW, MX, NI, NO, NZ, OA, OM, PE, PH, PL, PT, RO, RS, SC, SD, SE, SG, SK, SL, SM, ST, SV, TH, TJ, TN, TR, TT, UA, UZ, VC, VN, ZA, ZM, ZW

In accordance with Rule 47.1(c-bis)(ii), those Offices accept the present notice as conclusive evidence that the Contracting State for which that Office acts as a designated Office does not require the furnishing, under Article 22, by the applicant of a copy of the international application.

4. TIME LIMITS for entry into the national phase

For the designated or elected Office(s) listed above, the applicable time limit for entering the national phase will, **subject to what is said in the following paragraph**, be **30 MONTHS** from the priority date.

In practice, **time limits other than the 30-month time limit** will continue to apply, for various periods of time, in respect of certain of the designated or elected Office(s) listed above. For **regular updates on the applicable time limits** (30 or 31 months, or other time limit), Office by Office, refer to the *PCT Gazette*, the *PCT Newsletter* and the *PCT Applicant's Guide*, Volume II, National Chapters, all available from WIPO's Internet site, at <http://www.wipo.int/pct/en/index.html>.

It is the applicant's **sole responsibility** to monitor all these time limits.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Yukari Nakamura e-mail: pt07.pct@wipo.int
---	---

(19) 世界知的所有權機關
國際事務局

(43) 國際公開日
2011 年 9 月 15 日(15.09.2011)



(10) 国際公開番号

WO 2011/111144 A1

- (51) 国際特許分類:
G11C 16/06 (2006.01)

(21) 国際出願番号: PCT/JP2010/007402

(22) 国際出願日: 2010年12月21日(21.12.2010)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願 2010-052722 2010年3月10日(10.03.2010) JP

(71) 出願人(米国を除く全ての指定国について): パナソニック株式会社(PANASONIC CORPORATION) [JP/JP]; 〒5718501 大阪府門真市大字門真 1006番地 Osaka (JP).

(72) 発明者: および

(75) 発明者/出願人(米国についてのみ): 持田礼司(MOCHIDA, Reiji), 圓山敬史(MARUYAMA, Takafumi), 濱本幸昌(HAMAMOTO, Yukimasa).

(74) 代理人: 前田弘, 外(MAEDA, Hiroshi et al.); 〒5410053 大阪府大阪市中央区本町2丁目5番7号 大阪丸紅ビル Osaka (JP).

(81) 指定国(表示のない限り、全ての種類の国内保護が可能): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) 指定国(表示のない限り、全ての種類の広域保護が可能): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), ユーラシア(AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), ヨーロッパ(AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

添付公開書類:
— 国際調査報告(条約第21条(3))

(54) Title: FLASH MEMORY IN WHICH DRAIN VOLTAGE-USE AND GATE VOLTAGE-USE REGULATORS OF MEMORY CELL ARE SHARED

(54) 発明の名称: メモリセルのドレイン電圧用及びゲート電圧用のレギュレータを共有したフラッシュメモリ

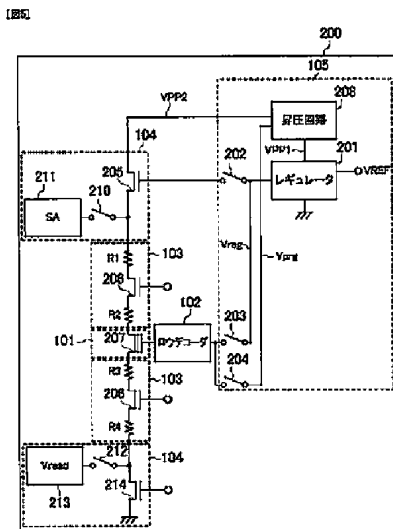


FIG. 8:
102 ROW DECODER
201 REGULATOR
208 BUFFERING CIRCUIT

(57) Abstract: In a semiconductor storage device, inputs of first and second switches (202 and 203) are connected to the output of a regulator (201), the output of the first switch (202) is connected to a path for supplying drain voltage to a memory cell (207) at a time of a first mode, and the output of the second switch (203) is connected to a path for supplying gate voltage to the memory cell (207) at a time of a second mode. Furthermore, a fourth switch (204) is provided parallel to the second switch (203). The output side of the fourth switch (204) is connected to the output side of the second switch (203) and supplies the gate voltage to the memory cell (207) at the time of the first mode. Therefore, the two regulators that are the drain voltage-use regulator of the memory cell and the gate voltage-use regulator of the memory cell are combined as one regulator.

(57) 要約: 半導体記憶装置において、レギュレータ201の出力に第1、第2のスイッチ202、203の入力を接続し、前記第1のスイッチ202の出力は第1のモード時にメモリセル207のドレイン電圧を供給するパスに接続し、前記第2のスイッチ203の出力は第2のモード時にメモリセル207のゲート電圧を供給するパスに接続される。また、前記第2のスイッチ203と並列に第4のスイッチ204が設けられる。この第4のスイッチ204の出力側は前記第2のスイッチ203の出力側と接続され、第1のモード時のメモリセル207のゲート電圧を供給する。従って、メモリセルのドレイン電圧用レギュレータと、メモリセルのゲート電圧用レギュレータとの2基のレギュレータを1個のレギュレータで兼用される。

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/007402

A. CLASSIFICATION OF SUBJECT MATTER

G11C16/06(2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C16/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2011
Kokai Jitsuyo Shinan Koho	1971-2011	Toroku Jitsuyo Shinan Koho	1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2008-217914 A (Toshiba Corp.), 18 September 2008 (18.09.2008), paragraphs [0049], [0050]; fig. 9 (Family: none)	1-21

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 March, 2011 (09.03.11)

Date of mailing of the international search report

22 March, 2011 (22.03.11)

Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

PCT

國際調查報告

(法 8 条、法施行規則第 40、41 条)

[PCT18 条、PCT 規則 43、44]



出願人又は代理人 M10-512CT1 の書類記号 P602416P0 -Y	今後の手続きについては、様式PCT/ISA/220 及び下記5を参照すること。	
国際出願番号 PCT/JP2010/007402	国際出願日 (日.月.年) 21.12.2010	優先日 (日.月.年) 10.03.2010
出願人(氏名又は名称) パナソニック株式会社		

国際調査機関が作成したこの国際調査報告を法施行規則第41条（PCT18条）の規定に従い出願人に送付する。
この写しは国際事務局にも送付される。

この国際調査報告は、全部で 2 ページである。

「この調査報告に引用された先行技術文献の写しも添付されている。

1. 国際調査報告の基礎

9. 言語に關し、この國際調査は以下のものに基づき行った。

☒ 出願時の言語による国際出願

☐ 出願時の言語から国際調査のための言語である _____ 語に翻訳された。
この国際出願の翻訳文（PCT規則12.3(a)及び23.1(b)）

b. ☐ この国際調査報告は、PCT規則91の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した（PCT規則43.6の2(a)）。

c. 「この国際出願は、ヌクレオチド又はアミノ酸配列を含んでいる（第Ⅰ欄参照）。

2. ☐ 請求の範囲の一部の調査ができない（第Ⅱ欄参照）。

3. ☐ 発明の単一性が欠如している（第Ⅲ欄参照）。

4. 発明の名称は ☐ 出願人が提出したものを承認する。

☒ 次に示すように国際調査機関が作成した。

メモリセルのドレイン電圧用及びゲート電圧用のレギュレータを共有したフラッシュメモリ

5. 要約は ☒ 出願人が提出したものを承認する。

□ 第IV欄に示されているように、法施行規則第47条第1項（PCT規則38.2）の規定により国際調査機関が作成した。出願人は、この国際調査報告の発送の日から1月以内にこの国際調査機関に意見を提出することができる。

6. 図面に関して

a. 要約書とともに公表される図は、

第 5 図とする。 ☒ 出願人が示したとおりである。

出願人は図を示さなかったため、国際調査機関が選択した。

「本図は発明の特徴を一層よく表しているので、国際調査機関が選択した。」

b. ☐ 要約とともに公表される図はない。

様式 PCT/ISA/210 (第1ページ) (2009年7月) (改訂)

A. 発明の属する分野の分類（国際特許分類（IPC））

Int.Cl. G11C16/06(2006.01)i

B. 調査を行った分野

調査を行った最小限資料（国際特許分類（IPC））

Int.Cl. G11C16/06

最小限資料以外の資料で調査を行った分野に含まれるもの

日本国実用新案公報	1922-1996年
日本国公開実用新案公報	1971-2011年
日本国実用新案登録公報	1996-2011年
日本国登録実用新案公報	1994-2011年

国際調査で使用した電子データベース（データベースの名称、調査に使用した用語）

C. 関連すると認められる文献

引用文献の カテゴリー*	引用文献名 及び一部の箇所が関連するときは、その関連する箇所の表示	関連する 請求項の番号
A	JP 2008-217914 A（株式会社東芝）2008.09.18, 段落【0049】、 【0050】、第9図（ファミリーなし）	1-21

☐ C欄の続きにも文献が列挙されている。☐ パテントファミリーに関する別紙を参照。

* 引用文献のカテゴリー

「A」特に関連のある文献ではなく、一般的技術水準を示すもの
「E」国際出願日前の出願または特許であるが、国際出願日以後に公表されたもの
「L」優先権主張に疑義を提起する文献又は他の文献の発行日若しくは他の特別な理由を確立するために引用する文献（理由を付す）
「O」口頭による開示、使用、展示等に言及する文献
「P」国際出願日前で、かつ優先権の主張の基礎となる出願

の日の後に公表された文献

「T」国際出願日又は優先日後に公表された文献であって出願と矛盾するものではなく、発明の原理又は理論の理解のために引用するもの
「X」特に関連のある文献であって、当該文献のみで発明の新規性又は進歩性がないと考えられるもの
「Y」特に関連のある文献であって、当該文献と他の1以上の文献との、当業者にとって自明である組合せによって進歩性がないと考えられるもの
「&」同一パテントファミリー文献

国際調査を完了した日

09.03.2011

国際調査報告の発送日

22.03.2011

国際調査機関の名称及びあて先

日本国特許庁（ISA/JP）

郵便番号100-8915

東京都千代田区霞が関三丁目4番3号

特許庁審査官（権限のある職員）

滝谷 亮一

電話番号 03-3581-1101 内線 3586

5N

3135

特許協力条約



発信人 日本国特許庁（国際調査機関）

代理人 前田弘 あて名 〒541-0053 日本国大阪府大阪市中央区本町2丁目5番7号 大 阪丸紅ビル	様
--	---

PCT
 国際調査機関の見解書
 (法施行規則第40条の2)
 [PCT規則43の2.1]

発送日
 (日.月.年) 22.03.2011

出願人又は代理人 の書類記号 P602416P0	今後の手続きについては、下記2を参照すること。
国際出願番号 PCT/J P 2010/007402	国際出願日 (日.月.年) 21.12.2010
優先日 (日.月.年) 10.03.2010	
国際特許分類 (IPC) IntCl. G11C16/06(2006.01)i	
出願人 (氏名又は名称) パナソニック株式会社	

1. この見解書は次の内容を含む。 ☒ 第I欄 見解の基礎 ☐ 第II欄 優先権 ☐ 第III欄 新規性、進歩性又は産業上の利用可能性についての見解の不作成 ☐ 第IV欄 発明の単一性の欠如 ☒ 第V欄 PCT規則43の2.1(a)(1)に規定する新規性、進歩性又は産業上の利用可能性についての見解、それを裏付けるための文献及び説明 ☐ 第VI欄 ある種の引用文献 ☐ 第VII欄 国際出願の不備 ☐ 第VIII欄 国際出願に対する意見
2. 今後の手続き 国際予備審査の請求がされた場合は、出願人がこの国際調査機関とは異なる国際予備審査機関を選択し、かつ、その国際予備審査機関がPCT規則66.1の2(b)の規定に基づいて国際調査機関の見解書を国際予備審査機関の見解書とみなさない旨を国際事務局に通知していた場合を除いて、この見解書は国際予備審査機関の最初の見解書とみなされる。 この見解書が上記のように国際予備審査機関の見解書とみなされる場合、様式PCT/ISA/220を送付した日から3月又は優先日から22月のうちいずれか遅く満了する期限が経過するまでに、出願人は国際予備審査機関に、適当な場合は補正書とともに、答弁書を提出することができる。 さらなる選択肢は、様式PCT/ISA/220を参照すること。
3. さらなる詳細は、様式PCT/ISA/220の備考を参照すること。

見解書を作成した日 09.03.2011	
名称及びあて先 日本国特許庁 (ISA/J P) 郵便番号100-8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官 (権限のある職員) 滝谷 亮一 電話番号 03-3581-1101 内線 3586
	5 N 3 1 3 5

様式PCT/ISA/237 (表紙) (2009年7月)

第 I 欄 見解の基礎

1. 言語に関し、この見解書は以下のものに基づき作成した。

☒ 出願時の言語による国際出願

☐ 出願時の言語から国際調査のための言語である _____ 語に翻訳された、この国際出願の翻訳文
(PCT規則12.3(a)及び23.1(b))

2. ☐ この見解書は、PCT規則 91 の規定により国際調査機関が認めた又は国際調査機関に通知された明らかな誤りの訂正を考慮して作成した (PCT規則 43 の 2.1(b))。

3. この国際出願で開示されたヌクレオチド又はアミノ酸配列に関して、提出された以下の配列表に基づき見解書を作成した。

a. 提出手段

☐ 紙形式

☐ 電子形式

b. 提出時期

☐ 出願時の国際出願に含まれていたもの

☐ この国際出願と共に電子形式により提出されたもの

☐ 出願後に、調査のために、この国際調査機関に提出されたもの

4. ☐ さらに、複数の版の配列表又は配列表の写しを提出した場合、出願後に提出した配列の写し若しくは追加して提出した配列の写しが、出願時に提出した配列と同一である旨又は出願時の開示を超える事項を含まない旨の陳述書の提出があった。

5. 補足意見：

第V欄 新規性、進歩性又は産業上の利用可能性についてのPCT規則43の2.1(a)(i)に定める見解、
それを裏付ける文献及び説明

1. 見解

新規性 (N)	請求項 請求項	1-21	有 無
進歩性 (IS)	請求項 請求項	1-21	有 無
産業上の利用可能性 (IA)	請求項 請求項	1-21	有 無

2. 文献及び説明

文献1 : JP 2008-217914 A (株式会社東芝) 2008.09.18, 段落【0049】、【0050】、第9図

請求の範囲1-21について

請求の範囲1-21に係る発明は、国際調査報告において引用されたいずれの文献にも記載されておらず、新規性・進歩性を有している。特に、レギュレータの出力を電圧印加トランジスタ及びメモリセルのゲートに選択的に印加する構成について、新規性・進歩性が認められる。

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2008-217914

(43)Date of publication of application : 18.09.2008

(51)Int.Cl. G11C 16/06 (2006.01)

(21)Application number : 2007-055056

(71)Applicant : TOSHIBA CORP

(22)Date of filing : 06.03.2007

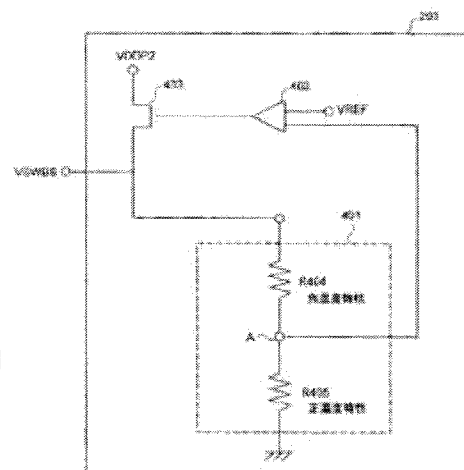
(72)Inventor : NAKAUCHI TAKAHIRO
AOKI MINORU
KONDO TOSHIYUKI
HARA NORIMASA
NARUGE KIYOMI

(54) NONVOLATILE SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a nonvolatile semiconductor memory device capable of reducing the deterioration amount of a tunnel oxide film and data erasure time.

SOLUTION: This nonvolatile semiconductor memory device 100 is provided with: a nonvolatile memory cell 201 having a charge storage part on a tunnel insulating film; and a voltage adjusting circuit 203 for adjusting a writing voltage on the basis of the composite resistance value of a composite resistance element 401 which serially connects a first resistance element R404 of negative temperature characteristics where a resistance value declines with a temperature increase and a second resistance element R405 of positive temperature characteristics where a resistance value increases with a temperature increase to supply it to the drain electrode of the nonvolatile memory cell.



(19) 日本国特許庁(JP)

(12) 公開特許公報(A)

(11) 特許出願公開番号

特開2008-217914

(P2008-217914A)

(43) 公開日 平成20年9月18日(2008.9.18)

(51) Int. Cl.

G 1 1 C 16/06 (2006.01)

F I

G 1 1 C 17/00 6 3 4 F

G 1 1 C 17/00 6 3 3 D

テーマコード (参考)

5 B 1 2 5

審査請求 未請求 請求項の数 5 O L (全 17 頁)

(21) 出願番号 特願2007-55056 (P2007-55056)

(22) 出願日 平成19年3月6日(2007.3.6)

(71) 出願人 000003078

株式会社東芝

東京都港区芝浦一丁目1番1号

(74) 代理人 110000408

特許業務法人高橋・林アンドパートナーズ

(72) 発明者 中内 孝浩

東京都港区芝浦一丁目1番1号 株式会社

東芝内

(72) 発明者 青木 実

東京都港区芝浦一丁目1番1号 株式会社

東芝内

(72) 発明者 近藤 敏行

東京都港区芝浦一丁目1番1号 株式会社

東芝内

最終頁に続く

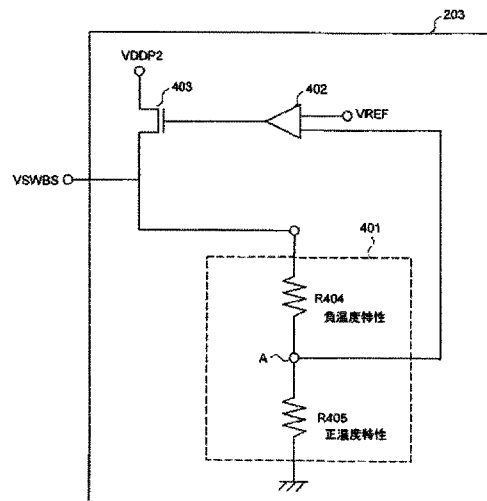
(54) 【発明の名称】 不揮発性半導体記憶装置

(57) 【要約】

【課題】 トンネル酸化膜の劣化量を減少させることができ、かつ、データ消去時間を減少させることができる不揮発性半導体記憶装置を提供すること。

【解決手段】 不揮発性半導体記憶装置100は、トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセル201と、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子R404と温度上昇に伴い抵抗値が増加する正の温度特性の第2の抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいて書き込み電圧を調整して不揮発性メモリセルのドレイン電極に供給する電圧調整回路203と、を備える。

【選択図】 図4



【特許請求の範囲】

【請求項 1】

トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセルと、
温度上昇に伴い抵抗値が減少する負の温度特性の第 1 の抵抗素子と温度上昇に伴い抵抗値が増加する正の温度特性の第 2 の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいて書き込み電圧を調整して前記不揮発性メモリセルのドレイン電極に供給する電圧調整回路と、
を備えることを特徴とする不揮発性半導体記憶装置。

【請求項 2】

前記電圧調整回路は、レギュレータ回路と電圧供給トランジスタとを有し、
前記レギュレータ回路は、
前記第 1 の抵抗素子と前記第 2 の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいて調整した調整電圧を前記電圧供給トランジスタのゲート電極に供給し、
前記電圧供給トランジスタは、
前記コントロールゲート電極に供給されるレギュレータ回路からの前記調整電圧に基づいてドレイン電極に供給される前記書き込み電圧を調整して前記不揮発性メモリセルの前記ドレイン電極に供給することを特徴とする請求項 1 記載の不揮発性半導体記憶装置。

【請求項 3】

前記レギュレータ回路は、
入力端子の 1 つに基準電圧が入力され、前記入力端子の他のものに前記合成抵抗素子における前記第 1 及び第 2 の抵抗素子のノードからの電圧が入力されるオペアンプと、
ドレイン電極に入力される電圧及びコントロールゲート電極に入力される前記オペアンプの出力電圧に基づいて前記電圧供給トランジスタのゲート電極に電圧を供給するトランジスタと、
を備えることを特徴とする請求項 2 記載の不揮発性半導体記憶装置。

【請求項 4】

トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセルと、
温度上昇に伴い抵抗値が減少する負の温度特性の第 1 の抵抗素子と温度上昇に伴い抵抗値が増加する正の温度特性の第 2 の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいてゲート電圧を調整して前記不揮発性メモリセルのゲート電極に供給する電圧調整回路と、
を備えることを特徴とする不揮発性半導体記憶装置。

【請求項 5】

前記電圧調整回路は、
前記第 1 の抵抗素子と前記第 2 の抵抗素子とを直列接続する前記合成抵抗素子の合成抵抗値に基づいて前記不揮発性メモリセルの前記ゲート電極の前記ゲート電圧を調整するレギュレータ回路を有し、
前記レギュレータ回路は、
入力端子の 1 つに基準電圧が入力され、前記入力端子の他のものに前記合成抵抗素子における前記第 1 及び第 2 の抵抗素子のノードからの電圧が入力されるオペアンプと、
ドレイン電極に入力される電圧及びコントロールゲート電極に入力される前記オペアンプの出力電圧に基づいて前記不揮発性メモリセルの前記ゲート電極に電圧を供給するトランジスタと、
を備えることを特徴とする請求項 4 記載の不揮発性半導体記憶装置。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、不揮発性半導体記憶装置に関し、特に H C I (Hot Carrier Injection: ホットキャリア注入) 方式を用いてデータの書き込みを行う不揮発性半導体記憶装置に関する。

【背景技術】

【0002】

HCI方式を用いる不揮発性半導体記憶装置において、メモリセルに対して、レギュレータ回路により調整された温度変化に対して一定電圧となるような書き込み(Program)電圧を供給するものがある。

【0003】

このような不揮発性半導体記憶装置においては、メモリセルの微細化が進み、ゲート長がシュリンク(Shrink)されると、ドレイン電圧が世代と共に変わらない場合には、ドレイン拡散層の電界は高くなり、メモリセルのフローティングゲート電極(電荷蓄積層)へ注入されるHCI量が増加する。この場合、書き込み(Program)特性は良くなるが、HCI量が大きくなるためトンネル酸化膜の劣化量が増加する。その結果、基板とコントロールゲート電極(制御電極)に高電圧を与えてトンネル消去する消去(Erase)方式によりデータ消去動作を行う場合、データの消去時間は増加する。すなわち、酸化膜の劣化はHCI量と相関があるため、書き込み特性が良い場合には、電子のトラップ量が増加するので消去時間の増加に繋がる。特に、この消去時間の増加は、書き込み及び消去回数が増加するに従って顕著に現れる。

【0004】

一方、HCI量を低下する方法として、書き込みが可能な限りにドレイン電圧を低下させる方法がある。しかし、この方法を用いた場合でも、書き込み時の温度領域、つまり、高温から低温のすべてを満足するようなHCI量にすることは難しい。具体的には、例えば85℃の高温時(HT)のHCI量は、酸化膜劣化を生じない程度のHCI量であるが、-40℃の低温時(LT)のHCI量は、高温時よりも増加する。

【0005】

また、温度検出回路を備えた不揮発性半導体記憶装置については、例えば下記特許文献1乃至特許文献3に記載がある。

【特許文献1】特開2002-184192号公報

【特許文献2】特開2002-215258号公報

【特許文献3】特開2006-65945号公報

【発明の開示】

【発明が解決しようとする課題】

【0006】

本発明は、トンネル酸化膜の劣化量を減少させることができ、かつ、データ消去時間を減少させることができる不揮発性半導体記憶装置を提供する。

【課題を解決するための手段】

【0007】

本発明の第1の態様は、不揮発性半導体記憶装置において、トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセルと、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子と温度上昇に伴い抵抗値が増加する正の温度特性の第2の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいて書き込み電圧を調整して不揮発性メモリセルのドレイン電極に供給する電圧調整回路と、を備える。

【0008】

本発明の第2の態様は、不揮発性半導体記憶装置において、トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセルと、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子と温度上昇に伴い抵抗値が増加する正の温度特性の第2の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいてゲート電圧を調整して不揮発性メモリセルのコントロールゲート電極に供給する電圧調整回路と、を備える。

【発明の効果】

【0009】

本発明の一実施形態によれば、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子と温度上昇に伴い抵抗値が増加する正の温度特性の第2の抵抗素子とを直列接続す

る合成抵抗素子の合成抵抗値に基づいて書き込み電圧を調整するため、トンネル酸化膜の劣化量を減少させることができ、かつ、データ消去時間を減少させることができる。

【発明を実施するための最良の形態】

【0010】

以下、本発明の実施の形態について、図面を参照して詳細に説明する。本実施の形態は、本発明をNOR型フラッシュメモリ装置（NOR型EEPROM）に適用した例を示すものである。なお、本発明は、これらの実施の形態に限定されるものではない。

【0011】

（実施の形態1）

図1は、本発明の実施の形態1に係るNOR型フラッシュメモリ装置（不揮発性半導体記憶装置）100の構成を示すブロック図である。図1に示すように、NOR型フラッシュメモリ装置100は、メモリセルアレイ101、電源回路102、主制御回路103、ロウデコーダ104、カラムデコーダ105、書込読出部106、電圧調整回路107、インターフェイス回路108及びデータレジスタ109を具備している。

【0012】

メモリセルアレイ101は、ビット線とワード線との交差部に配置される電氣的に書き換え可能な複数の（不揮発性）メモリセルを有している。これらのメモリセルは、行列状に配列されている。

【0013】

電源回路102は、主制御回路103、ロウデコーダ104、カラムデコーダ105、書込読出部106、電圧調整回路107、インターフェイス回路108及びデータレジスタ109に接続され、これらに電力を供給している。

【0014】

主制御回路103は、インターフェイス回路108からの制御信号に基づいて、電源回路102、ロウデコーダ104、カラムデコーダ105、書込読出部106及びデータレジスタ109を制御する。

【0015】

主制御回路103は、ロウデコーダ104及びカラムデコーダ105にメモリセルアレイ101のメモリセルに対するアクセス情報を与える。ロウデコーダ104及びカラムデコーダ105は、このアクセス情報及びデータに基づいて書込読出部106を制御してメモリセルに対してデータの読出、書込又は消去を行う。

【0016】

電圧調整回路107は、温度変化に応じてHCI量がほぼ一定になるように書き込み電圧を調整してメモリセルアレイ101のメモリセルへ供給する。

【0017】

インターフェイス回路108は、外部機器とデータ及び制御信号（メモリセルへのアクセス情報等）の送受信を行う。インターフェイス回路108は、外部機器からのデータ及び制御信号を受けて所定の処理をして主制御回路103及びデータレジスタ109に与える。

【0018】

図2は、本実施の形態1に係るNOR型フラッシュメモリ装置100の一部を示す回路図である。メモリセルアレイ101は、複数のメモリセル201及び複数のカラムゲートトランジスタ（Column Gate Transistor）202を具備している。メモリセルアレイ101は、抵抗R2（配線抵抗または制御トランジスタ（カラムゲートトランジスタ202及び電圧供給トランジスタ204）の寄生抵抗）を介して電圧調整回路107に接続されている。図2においては、1つのメモリセル201及びカラムゲートトランジスタ202のみが示されている。電圧調整回路107は、レギュレータ回路203及び複数の電圧供給トランジスタ204を具備している。レギュレータ回路203の出力端子（VSWBS）は、複数の電圧供給トランジスタ204のゲート電極にそれぞれ接続されている。電圧調整回路107は、レギュレータ回路203の合成抵抗素子の合成抵抗値に基づいて電圧供給

トランジスタ204に供給されるビット線からの書き込み電圧を調整して、カラムゲートトランジスタ202を介してメモリセル201のドレイン電極に供給する。

【0019】

メモリセル201のドレイン電極は、抵抗R1（配線抵抗または制御トランジスタ（カラムゲートトランジスタ202）の寄生抵抗）を介してカラムゲートトランジスタ202のソース電極に接続されている。メモリセル201のゲート電極にはワード線（WL）が電氣的に接続され、メモリセル201のソース電極は接地されている。

【0020】

具体的には、図3に示すように、メモリセル201は、実用的には、フローティングゲート電極（電荷蓄積部）301及びコントロール電極（制御電極）302を有する導電型電界効果トランジスタで構成される。フローティングゲート電極部301は、多結晶シリコン（ポリシリコン）で構成され、基板（sub）上にトンネル絶縁膜303を介在して配設されている。コントロールゲート電極302は、多結晶シリコン（ポリシリコン）とシリサイド層（例えばWSi₂）で構成され、フローティングゲート電極301上に絶縁膜304を介在して配設されている。ビット線は、電圧調整回路107を介してメモリセル201のドレイン領域（D）に接続されている。メモリセル201のソース領域（S）には、ソース線（基準電源Vss）が接続されている。メモリセル201のドレイン領域及びソース領域は拡散層で構成される。

【0021】

カラムゲートトランジスタ202のコントロールゲート電極には選択ゲート線が電氣的に接続され、カラムゲートトランジスタ202のソース電極は抵抗R1（配線抵抗または制御トランジスタの寄生抵抗）を介してメモリセル201のドレイン電極に接続されている。カラムゲートトランジスタ202のドレイン電極は、抵抗R2（配線抵抗または制御トランジスタのチャネル寄生抵抗）を介して電圧供給トランジスタのソース電極に接続されている。カラムゲートトランジスタ202は、コントロールゲート電極への印加電圧に基づいて、書き込み、読み出し及び消去電圧をメモリセル201のドレイン電極に供給する。

【0022】

レギュレータ回路203の2つの入力端子は、電源回路102とそれぞれ接続されている。レギュレータ回路203の入力端子の1つには電圧（VDDP2）が入力され、レギュレータ回路203の入力端子の他のものには基準電圧（VREF）が入力される。また、レギュレータ回路203の出力端子（VSWBS）は、電圧供給トランジスタ204のコントロールゲート電極に接続されている。また、レギュレータ回路203の一端は、接地されている。

【0023】

電圧供給トランジスタ204のドレイン電極はビット線（BL）に接続され、電圧供給トランジスタ204のゲート電極はレギュレータ回路203の出力端子（VSWBS）に接続されている。電圧供給トランジスタ204のソース電極は、抵抗R2（配線抵抗または制御トランジスタのチャネル寄生抵抗）を介してカラムゲートトランジスタ202のドレイン電極に接続されている。

【0024】

次に、レギュレータ回路203について、図4を用いて説明する。図4は、レギュレータ回路203を示す回路図である。レギュレータ回路203は、合成抵抗素子401、オペアンプ402及びトランジスタ403を具備している。レギュレータ回路203は、温度変化に応じてメモリセル201のフローティングゲート電極（電荷蓄積部）へのHCI量がほぼ一定になるように書き込み電圧を調整する。

【0025】

合成抵抗素子401は、第1の抵抗素子R404及び第2の抵抗素子R405を具備している。第1の抵抗素子R404と第2の抵抗素子R405とは直列に接続され合成抵抗素子401を構成している。合成抵抗素子401の一端は、レギュレータ回路203の出力

端子(VSWBS)を介して電圧供給トランジスタ204に接続され、合成抵抗素子401の他端は接地されている。

【0026】

具体的には、第1の抵抗素子R404の一端は、レギュレータ回路203の出力端子(VSWBS)を介して電圧供給トランジスタ204に接続され、かつ、トランジスタ403のソース電極に接続されている。第1の抵抗素子R404と第2の抵抗素子R405とは直列に接続されている。第2の抵抗素子R405の他端は、接地されている。第1の抵抗素子R404と第2の抵抗素子R405のノードAは、オペアンプ402の入力端子の1つに接続されている。

【0027】

合成抵抗素子401において、第1の抵抗素子R404は、温度上昇に伴い抵抗値が減少する負の温度特性を有している。第1の抵抗素子R404は、例えば、ポリシリコン抵抗素子(例えば、N型ポリシリコン抵抗素子)で構成される。一方、第2の抵抗素子R405は、温度上昇に伴い抵抗値が増加する正の温度特性を有している。例えば、拡散層抵抗素子(例えば、N型拡散層抵抗素子やP型拡散層抵抗素子)で構成される。

【0028】

オペアンプ402の入力端子の1つは、合成抵抗素子401における第1の抵抗素子R404と第2の抵抗素子R405のノードAと接続されている。オペアンプ402の入力端子の他のものは、電源回路102と接続されている。オペアンプ402の入力端子の1つには第1の抵抗素子R404と第2の抵抗素子R405のノードAからの出力電圧が入力され、オペアンプ402の入力端子の他のものには電源回路102からの基準電圧(VREF)が入力される。このオペアンプ402は、第1の抵抗素子R404と第2の抵抗素子R405のノードAからの出力電圧及び電源回路102からの基準電圧に基づいて、一定電圧をトランジスタ403のゲート電極に供給する。

【0029】

トランジスタ403のドレイン電極は電源回路102に接続され、電圧(VDDP2)を受ける。トランジスタ403のゲート電極はオペアンプ402の出力端子に接続され、トランジスタ403のソース電極はレギュレータ回路203の出力端子(VSWBS)に接続されている。このトランジスタ403は、ドレイン電極に入力される電圧(VDDP2)及びゲート電極に入力されるオペアンプ402の出力電圧によりON状態となり、電圧供給トランジスタ204のゲート電極及び合成抵抗素子401に電圧を供給する。

【0030】

次に、合成抵抗素子401の電流－電圧特性について、図5を用いて説明する。図5は、合成抵抗素子401のノードAにおける第1の抵抗素子R404及び第2の抵抗素子R405の電流－電圧特性を示す図である。この場合に、第1の抵抗素子R404はポリシリコン抵抗素子で構成され、かつ、第2の抵抗素子R405は拡散層抵抗素子で構成されている。

【0031】

図5に示す実線501はポリシリコン抵抗素子R404の低温時(LT)の電流－電圧特性を示し、実線502は拡散層抵抗素子R405の低温時の電流－電圧特性を示している。また、一点鎖線503はポリシリコン抵抗素子R404の高温時(HT)の電流－電圧特性を示し、一点鎖線504は拡散層抵抗素子R405の高温時の電流－電圧特性を示している。

【0032】

低温の場合、実線501に示すように、ポリシリコン抵抗素子R404は、温度上昇に伴い抵抗値が減少する負の温度特性を有しているため、印加される電圧が大きくなると電流は小さくなる。一方、実線502で示すように、拡散層抵抗素子R405は、温度上昇に伴い抵抗値が増加する正の温度特性を有しているため、印加される電圧が大きくなると電流は大きくなる。そして、ポリシリコン抵抗素子R404と拡散層抵抗素子R405が直列接続され合成抵抗素子401となることにより、合成抵抗素子401の合成抵抗値は互

いの抵抗素子の抵抗値の中間値となる。具体的には、ポリシリコン抵抗素子R404と拡散層抵抗素子R405のノードAにおける低温時の電流－電圧特性は、実線501及び502の動作点（交点）505で示される。

【0033】

また、高温の場合、一点鎖線503に示すように、ポリシリコン抵抗素子R404は、温度上昇に伴い抵抗値が減少する負の温度特性を有しているため、印加される電圧が大きくなると電流は小さくなる。一点鎖線504で示すように、拡散層抵抗素子R405は、温度上昇に伴い抵抗値が増加する正の温度特性を有しているため、印加される電圧が大きくなると電流は大きくなる。そして、ポリシリコン抵抗素子R404と拡散層抵抗素子R405とが直列に接続されて合成抵抗素子401となることにより、この合成抵抗素子401の合成抵抗値は互いの抵抗素子の抵抗値の中間値となる。具体的には、ポリシリコン抵抗素子R404と拡散層抵抗素子R405のノードAにおける低温時の電流－電圧特性は、一点鎖線503及び504の動作点（交点）506で示される。

【0034】

そして、レギュレータ回路203は、ポリシリコン抵抗素子R404と拡散層抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいて調整した調整電圧を、出力端子（VSWBS）に供給する。例えば、低温時には図5に示す交点505からの矢印で示す電圧（VSWBS_LT）が調整電圧となり、高温時には図5に示す交点506からの矢印で示す電圧（VSWBS_HT）が調整電圧となる。この調整電圧は、本実施の形態に係る先行技術であるレギュレータ回路から供給される一定電圧とは異なり、温度特性を有している。

【0035】

そして、カラムゲートトランジスタ202で選択されたメモリセル201のドレイン電極に供給される電圧（ドレイン電圧）は、図6に示すように、本実施の形態に係る先行技術と比較した場合、逆の温度－電圧特性を持つことになる。具体的には、図6（A）に示すように、本発明に係る先行技術のレギュレータ回路を用いた場合、メモリセルの低温時のドレイン電圧（Vd2_cell_LT）は、高温時のドレイン電圧（Vd__cell__HT）より大きい。一方、図6（B）に示すように、本実施の形態1に係るレギュレータ回路107を用いた場合、メモリセル201の低温時のドレイン電圧（Vd2_cell_LT）は、高温時のドレイン電圧（Vd__cell__HT）より小さい。

【0036】

その結果、図7の電流－電圧（Id－Vd）特性図に示すように、低温時のメモリセル201へのドレイン電圧を高温時とほぼ同じ電圧か、又はそれ以下の電圧とすることができるので、低温時の書き込み電流（Iprog_LT）を小さくすることができる。すなわち、低温時のHCI量は、温度変化があった場合でも、高温時のHCI量とほぼ一定となるので、トンネル酸化膜の劣化量を減少させることができる。

【0037】

次に、上述した構成を有するNOR型フラッシュメモリ装置100の書き込み動作について説明する。

【0038】

電圧供給トランジスタ204のドレイン電極に印加されるビット線からの書き込み電圧（VDDP）は、負の温度特性の第1の抵抗素子R404と正の温度特性の第2の抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいて調整された調整電圧が電圧供給トランジスタ204のコントロールゲート電極に印加されることにより調整される。この調整された書き込み電圧は、温度特性を有する書き込み電圧であり、高温時に比べて低温時の方が小さい。

【0039】

電圧供給トランジスタ204から出力される調整後の書き込み電圧は、抵抗R2（配線抵抗及び制御トランジスタのチャネル抵抗）を介してカラムゲートトランジスタ202のドレイン電極に入力される。カラムゲートトランジスタ202は、ゲート電極に供給される

電圧によりON状態となり、抵抗素子R1を介してメモリセル201のドレイン電極に調整後の書き込み電圧を供給する。

【0040】

そして、メモリセル201のドレイン電極に供給される調整後の書き込み電圧とワード線に供給されるゲート電圧(V_g)とにより、チャンネル領域とワード線との間に高電圧が発生し、チャンネル領域からトンネル絶縁膜を通してフローティングゲート電極(電荷蓄積部)にデータとしての電子が注入され、データが書き込まれる。

【0041】

このように、本実施の形態1に係る不揮発性半導体記憶装置100は、トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセル201と、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子R404と温度上昇に伴い抵抗値が増加する正の温度特性の第2の抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいてビット線からの書き込み電圧を調整して不揮発性メモリセル201のドレイン電極に供給する電圧調整回路107と、を備える。

【0042】

その結果、本実施の形態1によれば、温度変化があった場合でもメモリセルの電荷蓄積部に注入されるHCI量がほぼ一定となるように書き込み電圧が調整されてメモリセルのドレイン電極に供給されるので、トンネル酸化膜の劣化量を減少させることができ、かつ、データ消去時間を減少させることができる。

【0043】

また、本実施の形態1によれば、メモリセルのソース領域及びドレイン領域を構成する拡散層により第1の抵抗素子を構成することができるので、同一の製造工程において製造することができる。さらに、本実施の形態1によれば、メモリセルのフローティングゲート電極(電荷蓄積部)及びコントロールゲート電極を構成するポリシリコンにより第2の抵抗素子を構成することができるので、同一の製造工程において製造することができる。

【0044】

(実施の形態2)

上述の実施の形態1では、温度調整回路は、温度変化に応じて不揮発性メモリセルのドレイン電極へ供給される書き込み電圧を調整した。本発明の実施の形態2では、温度調整回路は、温度変化に応じて不揮発性メモリセルのコントロールゲート電極へ供給されるゲート電圧を調整する。

【0045】

図8は、本発明の実施の形態2に係るNOR型フラッシュメモリ装置(不揮発性半導体記憶装置)1000の構成を示すブロック図である。図8に示すNOR型フラッシュメモリ装置1000は、メモリセルアレイ101、電源回路102、主制御回路103、ロウデコーダ104、カラムデコーダ105、書込読出部106、インターフェイス回路108、データレジスタ109、電圧供給回路1001及び電圧調整回路1002を具備している。なお、図8に示すNOR型フラッシュメモリ装置1000において、図1のNOR型フラッシュメモリ装置100と同じ構成については同じ符号を付し、それらの説明を省略する。

【0046】

ロウデコーダ104は、主制御回路103からのアクセス情報に基づいて書込制御部106を制御してメモリセルに対してデータの読出又は消去を行う。また、ロウデコーダ104は、主制御回路103からのアクセス情報に基づいて、電圧調整回路1001にメモリセルのコントロールゲート電極へゲート電圧を供給する。

【0047】

電圧供給回路1001は、電源回路102からの電圧を受けて、温度変化に対して一定電圧となる書き込み電圧を生成して、メモリセルアレイ101のメモリセルへ供給する。

【0048】

電圧調整回路1002は、ロウデコーダ104からのゲート電圧を受けて、温度変化に応

じてH C I量がほぼ一定になるようにゲート電圧を調整して、メモリセルアレイ101のメモリセルへ供給する。

【0049】

図9は、本実施の形態2に係るNOR型フラッシュメモリ装置1000の一部を示す回路図である。図9に示すNOR型フラッシュメモリ装置1000において、図2に示すNOR型フラッシュメモリ装置100と同じ構成については同じ符号を付し、それらの説明を省略する。

【0050】

メモリセルアレイ101は、複数のメモリセル201及び複数のカラムゲートトランジスタ202を具備している。メモリセルアレイ101の一端は抵抗素子R2を介して電圧供給回路1001に接続され、メモリセルアレイ101の他端は電圧調整回路1002に接続されている。図9においては、1つのメモリセル201及びカラムゲートトランジスタ202のみが示されている。電圧供給回路1001は、レギュレータ回路1100及び複数の電圧供給トランジスタ204を具備している。レギュレータ回路1100の出力端子(VSWBS2)は、複数の電圧供給トランジスタ204のコントロールゲート電極にそれぞれ接続されている。図9においては、1つの電圧供給トランジスタ204のみが示されている。電圧調整回路1002は、例えば、レギュレータ回路1101により構成される。このレギュレータ回路1101の合成抵抗素子の合成抵抗値に基づいてロウデコーダ104から供給されるゲート電圧を調整して、メモリセル201のコントロールゲート電極に供給する。

【0051】

メモリセル201のドレイン電極は、抵抗R1(配線抵抗及び制御トランジスタ(カラムゲートトランジスタ202)のチャネル寄生抵抗)を介してカラムゲートトランジスタ202のソース電極に接続されている。メモリセル201のコントロールゲート電極は、レギュレータ回路1101の出力端子(VSWBS3)に接続され、メモリセル201のソース電極は接地されている。

【0052】

レギュレータ回路1100の入力端子は電源回路102と接続され、電圧(VDDP2)を受ける。また、レギュレータ回路1100の出力端子(VSWBS2)は電圧供給トランジスタ204のコントロールゲート電極に接続されている。また、レギュレータ回路1100の一端は、接地されている。

【0053】

電圧供給トランジスタ204のドレイン電極はビット線(BL)に接続され、電圧供給トランジスタ204のコントロールゲート電極はレギュレータ回路1100の出力端子(VSWBS2)に接続されている。電圧供給トランジスタ204のソース電極は、抵抗R2(配線抵抗及び制御トランジスタ(電圧供給トランジスタ204及びカラムゲートトランジスタ202)のチャネル寄生抵抗)を介してカラムゲートトランジスタ202のドレイン電極に接続されている。

【0054】

レギュレータ回路1101の2つの入力端子の1つはワード線を介してロウデコーダ104に接続され、レギュレータ回路1101の入力端子の他のものは電源回路102に接続されている。また、レギュレータ回路1101の出力端子(VSWBS3)は、メモリセル201のコントロールゲート電極に接続されている。また、レギュレータ回路1101の一端は、接地されている。レギュレータ回路1101の入力端子の1つには、ロウデコーダ104からのメモリセル201のコントロールゲート電極へのゲート電圧(Vg)が入力される。レギュレータ回路1101の入力端子の他のものには、電源回路102からの基準電圧(VREF)が入力される。

【0055】

次に、レギュレータ回路1101について、図10を用いて説明する。図10は、レギュレータ回路1101を示す回路図である。レギュレータ回路1101は、合成抵抗素子4

01、オペアンプ402及びトランジスタ403を具備している。レギュレータ回路1101は、温度変化に応じてメモリセル201のフローティングゲート電極（電荷蓄積部）へのHCl量がほぼ一定になるようにゲート電圧を調整する。なお、図10に示すレギュレータ回路1101において、図4に示すレギュレータ回路203と同じ構成については同じ符号を付し、それらの説明を省略する。

【0056】

合成抵抗素子401は、第1の抵抗素子R404及び第2の抵抗素子R405を具備している。第1の抵抗素子R404と第2の抵抗素子R405とは直列に接続され合成抵抗素子401を構成している。合成抵抗素子401の一端はレギュレータ回路1101の出力端子（VSWBS3）を介してメモリセル201のコントロールゲート電極に接続され、合成抵抗素子401の他端は接地されている。

【0057】

具体的には、第1の抵抗素子R404の一端は、レギュレータ回路1101の出力端子（VSWBS3）を介してメモリセル201のコントロールゲート電極に接続され、かつ、トランジスタ403のソース電極に接続されている。第1の抵抗素子R404と第2の抵抗素子R405とは直列に接続されている。第2の抵抗素子R405の他端は、接地されている。第1の抵抗素子R404と第2の抵抗素子R405のノードAは、オペアンプ402の入力端子の1つに接続されている。

【0058】

オペアンプ402の入力端子の1つは、合成抵抗素子401における第1の抵抗素子R404と第2の抵抗素子R405のノードAと接続されている。オペアンプ402の入力端子の他のものは、電源回路102と接続されている。オペアンプ402の入力端子の1つには第1の抵抗素子R404と第2の抵抗素子R405のノードAからの出力電圧が入力され、オペアンプ402の入力端子の他のものには電源回路102からの基準電圧（VREF）が入力される。このオペアンプ402は、第1の抵抗素子R404と第2の抵抗素子R405のノードAからの出力電圧及び電源回路102からの基準電圧に基づいて、一定電圧をトランジスタ403のコントロールゲート電極に供給する。

【0059】

トランジスタ403のドレイン電極はロウデコーダ104に接続され、ゲート電圧（Vg）を受ける。トランジスタ403のコントロールゲート電極はオペアンプ402の出力端子に接続され、トランジスタ1200のソース電極はレギュレータ回路1101の出力端子（VSWBS3）に接続されている。このトランジスタ403は、ドレイン電極に入力されるゲート電圧（Vg）及びコントロールゲート電極に入力されるオペアンプ402の出力電圧によりON状態となり、合成抵抗素子401に電圧を供給する。

【0060】

そして、レギュレータ回路1101は、第1の抵抗素子R404と第2の抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいて調整した調整電圧を、出力端子（VSWBS3）に供給する。例えば、低温時には図5に示す交点505からの矢印で示す電圧（VSWBS__HT）が調整電圧となり、低温時には図5に示す交点506からの矢印で示す電圧（VSWBS__LT）が調整電圧となる。この調整電圧は、本実施の形態に係る先行技術のレギュレータ回路から供給される一定電圧とは異なり、温度特性を有している。

【0061】

その結果、メモリセル201のコントロールゲート電極に供給される調整後のゲート電圧は、図11に示すように、本実施の形態に係る先行技術と比較した場合、逆の温度－電圧特性を持つことになる。具体的には、図11（A）に示すように、本実施の形態に係る先行技術のレギュレータ回路を用いた場合、メモリセルの低温時のゲート電圧（Vg2__cell__LT）は、高温時のゲート電圧（Vg__cell__HT）より大きい。一方、図11（B）に示すように、本実施の形態に係るレギュレータ回路1101を用いた場合、メモリセル201の低温時のゲート電圧（Vg2__cell__LT）は、高温時のゲート電圧（Vg__cell__HT）より小さい。

ト電圧 ($V_{g_cell_HT}$) より小さい。

【0062】

その結果、図12の電流－電圧 ($I_g - V_g$) 特性図に示すように、低温時のメモリセル201へのゲート電圧を高温時とほぼ同じ電圧か、又はそれ以下の電圧とすることができるので、低温時の書き込み電流 (I_{prog_LT}) を、従来と比べて小さくすることができる。すなわち、低温時のHCI量は、温度変化があった場合でも、高温時のHCI量とほぼ一定となるので、トンネル酸化膜の劣化量を減少させることができる。

【0063】

次に、上述した構成を有するNOR型フラッシュメモリ装置1000の書き込み動作について説明する。

【0064】

レギュレータ回路1100から出力される一定電圧により、電圧供給トランジスタ204はON状態となり、ドレイン電極に印加されるビット線からの書き込み電圧 (V_{DDP}) を、抵抗素子R1を介してカラムゲートトランジスタ202のドレイン電極に出力する。カラムゲートトランジスタ202は、コントロールゲート電極に供給される電圧によりON状態となり、抵抗素子R1を介してメモリセル201のドレイン電極に書き込み電圧を供給する。

【0065】

メモリセル201のコントロールゲート電極には、負の温度特性の第1の抵抗素子R404と正の温度特性の第2の抵抗素子R405とを直列接続する合成抵抗素子401の合成抵抗値に基づいて調整されたゲート電圧がレギュレータ回路1101から入力される。この調整後のゲート電圧は、温度特性を有するゲート電圧であり、高温時に比べて低温時の方が小さい電圧となる。

【0066】

そして、メモリセル201のドレイン電極に入力される書き込み電圧は、コントロールゲート電極に入力される調整後のゲート電圧により調整され、チャネル領域とワード線との間に高電圧が発生し、チャネル領域からトンネル絶縁膜を通してフローティングゲート電極（電荷蓄積部）にデータとしての電子が注入され、データが書き込まれる。

【0067】

このように、本実施の形態2に係る不揮発性半導体記憶装置は、トンネル絶縁膜上に電荷蓄積部を有する不揮発性メモリセルと、温度上昇に伴い抵抗値が減少する負の温度特性の第1の抵抗素子と温度上昇に伴い抵抗値が上昇する正の温度特性の第2の抵抗素子とを直列接続する合成抵抗素子の合成抵抗値に基づいてゲート電圧を調整して不揮発性メモリセルのコントロールゲート電極に供給する電圧調整回路と、を備える。

【0068】

その結果、本実施の形態2によれば、温度変化があった場合でもメモリセルの電荷蓄積部に注入されるHCI量がほぼ一定となるようにゲート電圧が調整されてメモリセルのコントロールゲート電極に供給されるので、トンネル酸化膜の劣化量を減少させることができ、かつ、データ消去時間を減少させることができる。

【0069】

また、本実施の形態2によれば、メモリセルのソース領域及びドレイン領域を構成する拡散層により第2の抵抗素子を構成することができるので、同一の製造工程において製造することができる。さらに、本実施の形態2によれば、メモリセルのフローティングゲート電極（電荷蓄積部）及びコントロールゲート電極を構成するポリシリコンにより第1の抵抗素子を構成することができるので、同一の製造工程において製造することができる。

【0070】

なお、本発明の実施の形態1及び2を組み合わせても良い。すなわち、メモリセルのドレイン電極及びコントロールゲート電極に、温度特性を有する書き込み電圧及びゲート電圧を供給しても良い。これにより、上記実施の形態1及び2で述べた効果に加えて、さらに高温時と低温時の書き込み特性をほぼ同じにすることが可能となる。

【0071】

また、本発明の実施の形態1及び2において、メモリセルがフローティングゲート電極（電荷蓄積電極）及びコントロールゲート電極を有する所謂フローティングゲート型EEPROMを例に説明したが、これに限定されるものではない。すなわち、本発明は、トンネル絶縁膜上に電荷蓄積部を有するものに適用可能であり、例えば、MNOS（Metal Nitride Oxide Semiconductor）型EEPROMでも適用可能である。

【図面の簡単な説明】

【0072】

【図1】本発明の実施の形態1に係る不揮発性半導体記憶装置の構成を示すブロック図である。

【図2】本実施の形態1に係る不揮発性半導体記憶装置の一部を示す回路図である。

【図3】本実施の形態1に係る不揮発性メモリセルを説明するための図である。

【図4】本実施の形態1に係るレギュレータ回路を示す回路図である。

【図5】本実施の形態1に係るレギュレータ回路の合成抵抗素子のノードAにおける第1の抵抗素子及び第2の抵抗素子の電流－電圧特性を示す図である。

【図6】本実施の形態1に係る不揮発性半導体記憶装置の電圧－温度特性を示す図である。

【図7】本実施の形態1に係る不揮発性半導体記憶装置の低温時の電流－電圧特性を示す図である。

【図8】本発明の実施の形態2に係る不揮発性半導体記憶装置の構成を示すブロック図である。

【図9】本実施の形態2に係る不揮発性半導体記憶装置の一部を示す回路図である。

【図10】本実施の形態2に係るレギュレータ回路を示す回路図である。

【図11】本実施の形態2に係る不揮発性半導体記憶装置の電圧－温度特性を示す図である。

【図12】本実施の形態2に係る不揮発性半導体記憶装置の低温時の電流－電圧特性を示す図である。

【符号の説明】

【0073】

100、800、1000、1500 NOR型フラッシュメモリ装置（不揮発性半導体記憶装置）

101 メモリセルアレイ

102 電源回路

103 主制御回路

104 ロウデコーダ

105 カラムデコーダ

106 書込読出部

107、1002 電圧調整回路

201 不揮発性メモリセル

202 カラムゲートトランジスタ

203、801、1101、1501 レギュレータ回路

204 電圧供給トランジスタ

301 フローティングゲート電極（電荷蓄積部）

302 コントロールゲート電極

303 トンネル絶縁膜

401、802 合成抵抗素子

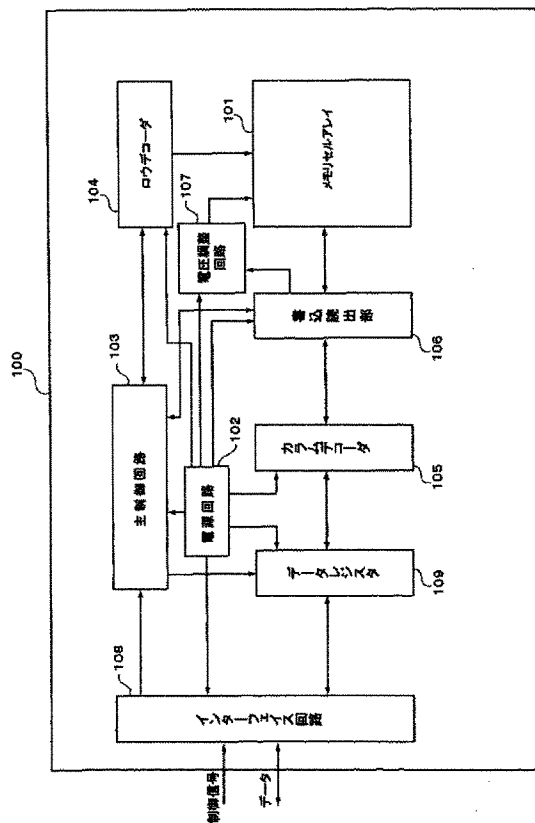
402 オペアンプ

403 トランジスタ

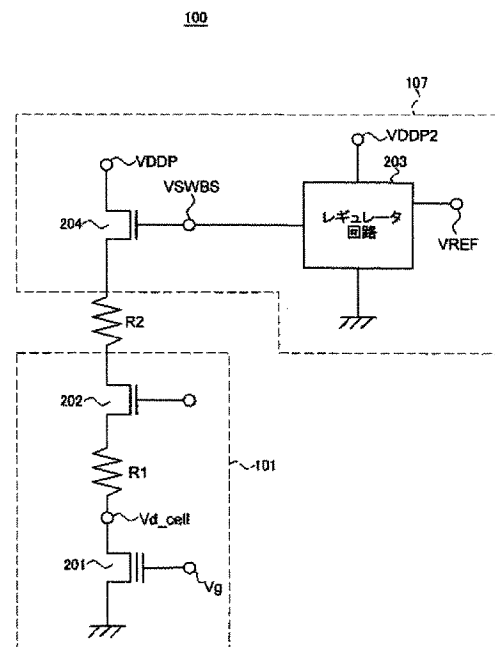
R404 第1の抵抗素子

R405 第2の抵抗素子
T803 トランジスタ

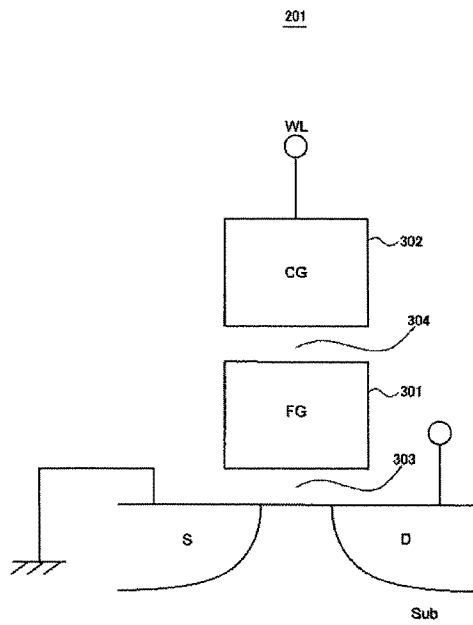
【図1】



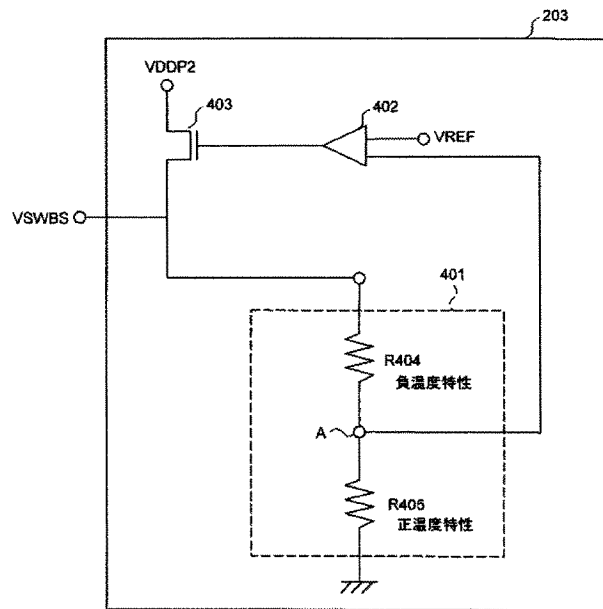
【図2】



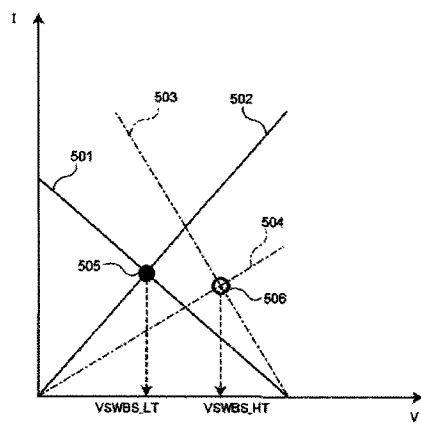
【図3】



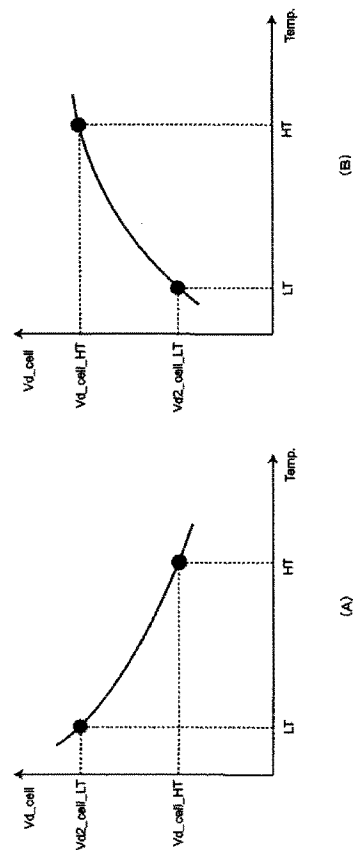
【図4】



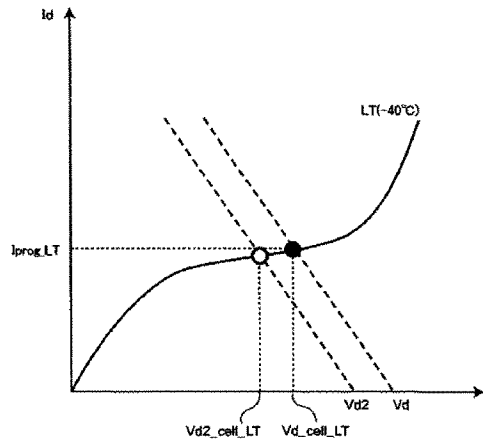
【図5】



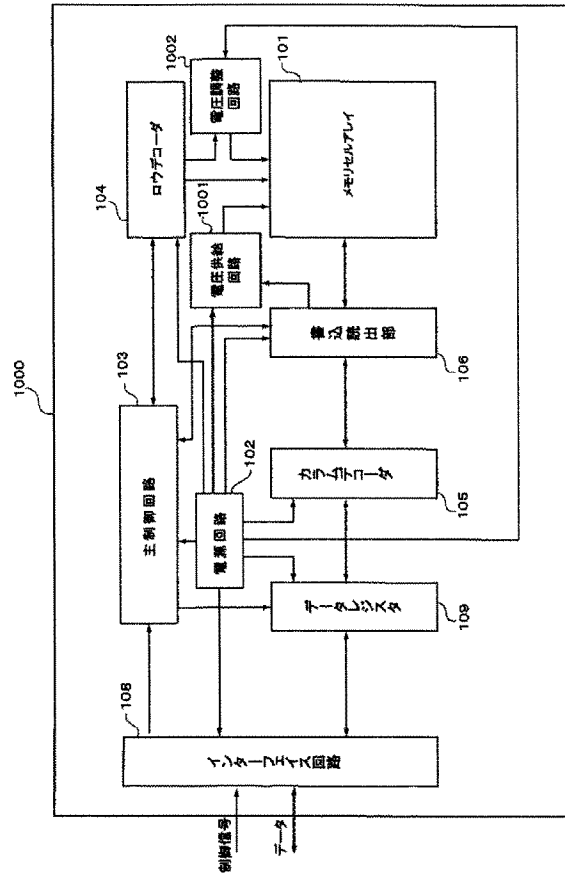
【図6】



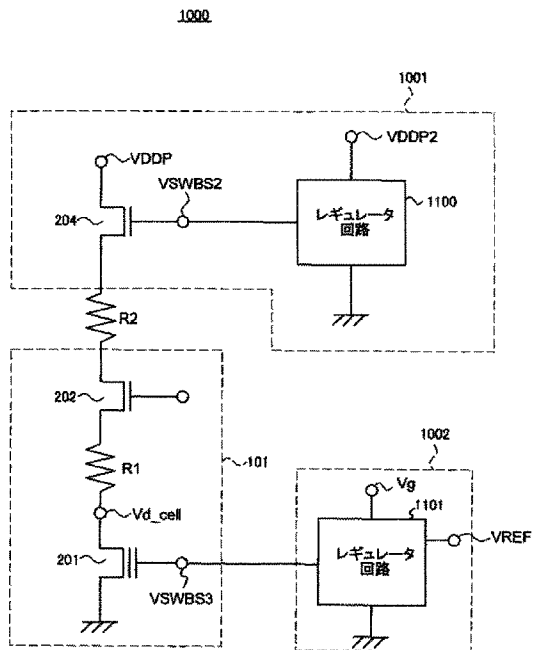
【図7】



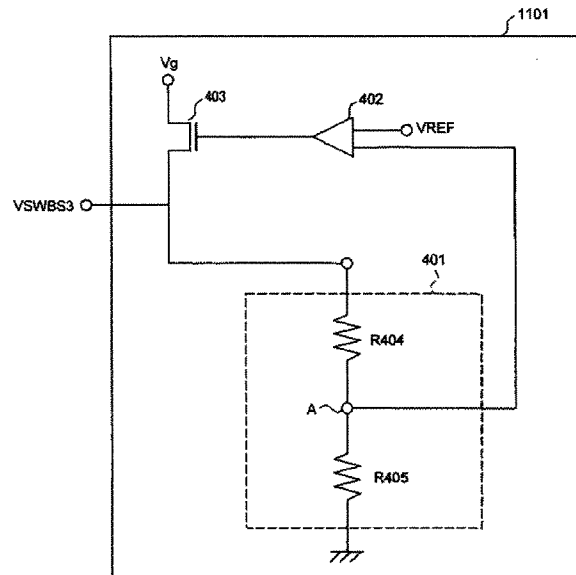
【図8】



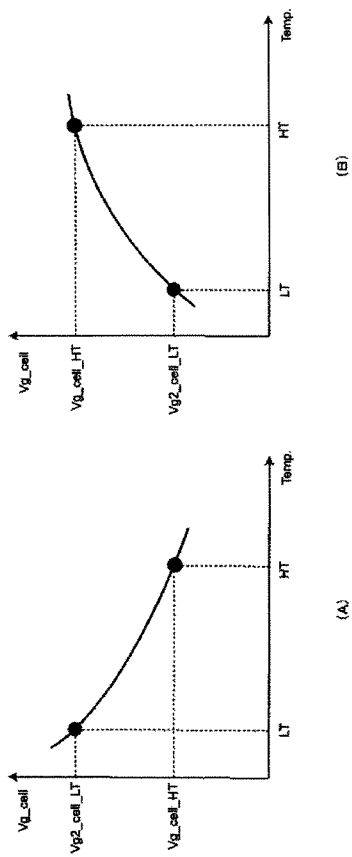
【図9】



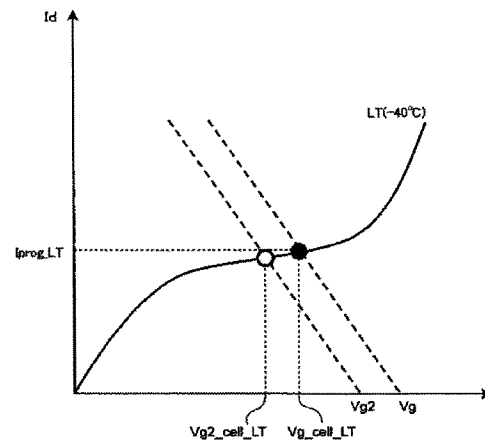
【図10】



【図 1 1】



【図 1 2】



フロントページの続き

(72)発明者 原 徳正

東京都港区芝浦一丁目1番1号 株式会社東芝内

(72)発明者 成毛 清実

東京都港区芝浦一丁目1番1号 株式会社東芝内

Fターム(参考) 5B125 BA02 CA13 CA27 EA01 EB02 EB04 EG02 EG08 EH08 EJ03

FA05

SEMICONDUCTOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This is a continuation of PCT International Application PCT/JP2010/007402 filed
5 on December 21, 2010, which claims priority to Japanese Patent Application No. 2010-
052722 filed on March 10, 2010. The disclosures of these applications including the
specifications, the drawings, and the claims are hereby incorporated by reference in their
entirety.

10 BACKGROUND

The present disclosure relates to semiconductor memory devices, and more
particularly to nonvolatile memory such as electrically erasable programmable read only
memory (EEPROM).

In EEPROM, the memory contents in memory cells can be erased and rewritten
15 using electric signals. In specific write operation, hot carrier injection (HCI) is used in some
cases. In such cases, the output of a first regulator is coupled to the gate of a memory cell,
and also the output of a second regulator is coupled to the gate of a voltage applying
transistor, so that the gate voltage of the memory cell is regulated while a voltage is applied
from the drain terminal of the voltage applying transistor to the drain terminal of the memory
20 cell. A technique like this is described in Japanese Patent Publication No. 2008-217914
(FIG. 9), for example.

SUMMARY

In the conventional circuit configuration described above, two regulators are
25 necessary, one for the drain voltage of the memory cell and the other for the gate voltage

thereof, because the required output voltage ranges and precisions for these voltages are different, and this poses a problem of increasing the circuit area.

To overcome the above problem, according to the present disclosure, the two regulators are combined, and when the voltage applied from the drain terminal of the voltage
5 applying transistor to the drain terminal of the memory cell is regulated by the regulator, the gate voltage of the memory cell is applied without intervention of a regulator.

Specifically, a first semiconductor memory device of the present disclosure is a semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, including the memory cell, one regulator, first and second
10 switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein an output of the regulator is coupled to inputs of the first and second switches, an output of the first switch is coupled to a gate of the voltage applying transistor, a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and an output of the second switch is coupled to a gate of the memory cell for
15 application of a voltage.

A second semiconductor memory device of the present disclosure is a semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, including the memory cell, one regulator, second and third
20 switches, and a voltage applying transistor, wherein an output of the regulator is coupled to an input of the second switch and a gate of the voltage applying transistor, a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell via the third switch, and an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

A third semiconductor memory device of the present disclosure is the first
25 semiconductor memory device, wherein an output of a fourth switch is coupled to the output

of the second switch, and a voltage different from the output of the regulator is applied to the gate of the memory cell.

A fourth semiconductor memory device of the present disclosure is the second semiconductor memory device, wherein an output of a fourth switch is coupled to the output
5 of the second switch, and a voltage different from the output of the regulator is applied to the gate of the memory cell.

A fifth semiconductor memory device of the present disclosure is the third semiconductor memory device, wherein, in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain
10 terminal of the memory cell and the voltage different from the output of the regulator to be applied to the gate of the memory cell, and in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

A sixth semiconductor memory device of the present disclosure is the fourth
15 semiconductor memory device, wherein, in a first operation mode, the third and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and the voltage different from the output of the regulator to be applied to the gate of the memory cell, and in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory
20 cell.

A seventh semiconductor memory device of the present disclosure is the first or third semiconductor memory device, further including fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit, wherein an input of the fifth switch is coupled between the drain terminal of the voltage applying transistor and the drain
25 terminal of the memory cell, and an input of the sense amplifier is coupled to an output of the

fifth switch, a source terminal of the memory cell is grounded via the grounding transistor, an output of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and an output of the voltage generator circuit is coupled to an input of the sixth switch.

5 An eighth semiconductor memory device of the present disclosure is the second or fourth semiconductor memory device, further including fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit, wherein an input of the fifth switch is coupled between the third switch and the drain terminal of the memory cell, and an input of the sense amplifier is coupled to an output of the fifth switch, a source terminal of the
10 memory cell is grounded via the grounding transistor, an output of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and an output of the voltage generator circuit is coupled to an input of the sixth switch.

 A ninth semiconductor memory device of the present disclosure is the first or third semiconductor memory device, further including fifth and sixth switches, a grounding
15 transistor, a sense amplifier, and a voltage generator circuit, wherein an output of the fifth switch is coupled between the drain terminal of the voltage applying transistor and the drain terminal of the memory cell, and an output of the voltage generator circuit is coupled to an input of the fifth switch, a source terminal of the memory cell is grounded via the grounding transistor, an input of the sixth switch is coupled between the source terminal of the memory
20 cell and the grounding transistor, and an input of the sense amplifier is coupled to an output of the sixth switch.

 A tenth semiconductor memory device of the present disclosure is the second or fourth semiconductor memory device, further including fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit, wherein an output of the fifth
25 switch is coupled between the third switch and the drain terminal of the memory cell, and an

output of the voltage generator circuit is coupled to an input of the fifth switch, a source terminal of the memory cell is grounded via the grounding transistor, an input of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and an input of the sense amplifier is coupled to an output of the sixth switch.

5 An eleventh semiconductor memory device of the present disclosure is the first or third semiconductor memory device, further including a fifth switch, a sense amplifier, and a voltage generator circuit, wherein an output of the fifth switch is coupled between the drain terminal of the voltage applying transistor and the drain terminal of the memory cell, and an output of the voltage generator circuit and an input of the sense amplifier are coupled to an
10 input of the fifth switch, and a source terminal of the memory cell is grounded.

 A twelfth semiconductor memory device of the present disclosure is the second or fourth semiconductor memory device, further including a fifth switch, a sense amplifier, and a voltage generator circuit, wherein an output of the fifth switch is coupled between the third
15 switch and the drain terminal of the memory cell, and an output of the voltage generator circuit and an input of the sense amplifier are coupled to an input of the fifth switch, and a source terminal of the memory cell is grounded.

 A thirteenth semiconductor memory device of the present disclosure is the seventh semiconductor memory device, wherein in a first operation mode, the first and fourth switches and the grounding transistor are turned on, allowing the output voltage of the
20 regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and a source of the memory cell to be grounded, and in a second operation mode, the second, fifth, and sixth switches are turned on, allowing the input of the sense amplifier to be coupled to the drain terminal of the memory cell, the output voltage of the regulator to be applied to the gate of the
25 memory cell, and the output voltage of the voltage generator circuit to be applied to the

source of the memory cell.

A fourteenth semiconductor memory device of the present disclosure is the eighth semiconductor memory device, wherein in a first operation mode, the third and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and a source of the memory cell to be grounded, and in a second operation mode, the second, fifth, and sixth switches are turned on, allowing the input of the sense amplifier to be coupled to the drain terminal of the memory cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the output voltage of the voltage generator circuit to be applied to the source of the memory cell.

A fifteenth semiconductor memory device of the present disclosure is the ninth semiconductor memory device, wherein in a first operation mode, the first and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and in a second operation mode, the second, fifth, and sixth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the input of the sense amplifier to be coupled to the source terminal of the memory cell.

A sixteenth semiconductor memory device of the present disclosure is the tenth semiconductor memory device, wherein in a first operation mode, the third and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the

output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and in a second operation mode, the second, fifth, and sixth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the input of the sense amplifier to be coupled to the source terminal of the memory cell.

A seventeenth semiconductor memory device of the present disclosure is the eleventh semiconductor memory device, wherein in a first operation mode, the first and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and in a second operation mode, the second and fifth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, as well as the input of the sense amplifier to be coupled to the drain terminal of the memory cell, and the output voltage of the regulator to be applied to the gate of the memory cell.

An eighteenth semiconductor memory device of the present disclosure is the twelfth semiconductor memory device, wherein in a first operation mode, the third and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and in a second operation mode, the second and fifth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, as well as the input of the sense amplifier to be coupled to the drain terminal of the memory cell, and the output voltage of the regulator to be applied to

the gate of the memory cell.

Preferably, the first operation mode represents write into the memory cell, and the second operation mode represents read of memory cell information.

Preferably, the voltage different from the output of the regulator is an output voltage
5 of a booster circuit.

Preferably, an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

As described above, according to the present disclosure, in the first mode (e.g., during write operation), while a voltage that has not been regulated is directly applied to the
10 gate of the memory cell, the output of the regulator is supplied to the gate of the voltage applying transistor, to control the voltage applied to the drain side of the memory cell with the output voltage of the regulator. In the second mode (e.g., during read operation), the output of the regulator is supplied to the gate of the memory cell, to control the gate voltage of the memory cell.

15 Therefore, since the gate voltage of the memory cell is a voltage applied without intervention of a regulator in the first mode, the regulator for application of the drain voltage of the memory cell used in the first mode and the regulator for the gate voltage of the memory cell used in the second mode can be combined as one regulator. Thus, a small-area semiconductor memory device can be provided.

20 As described above, according to the present disclosure, one regulator can serve as the regulator for the drain voltage of the memory cell used in the first mode and the regulator for the gate voltage of the memory cell used in the second mode, so that a small-area semiconductor memory device can be provided.

25 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a semiconductor memory device of the first embodiment of the present disclosure.

FIG. 2 is a circuit diagram showing a relevant part of the semiconductor memory device of the first embodiment.

5 FIG. 3 is a view showing a specific configuration of a regulator of the semiconductor device of the first embodiment.

FIG. 4 is a view showing a configuration of a relevant part of a semiconductor memory device of the second embodiment of the present disclosure.

FIG. 5 is a view showing a configuration of a relevant part of a semiconductor
10 memory device of the third embodiment of the present disclosure.

FIG. 6 is a view showing a configuration of a relevant part of a semiconductor memory device of the fourth embodiment of the present disclosure.

FIG. 7 is a view showing a configuration of a relevant part of a semiconductor memory device of the fifth embodiment of the present disclosure.

15

DETAILED DESCRIPTION

Embodiments of the present disclosure will be described hereinafter.

(First Embodiment)

FIG. 1 is a block diagram of a semiconductor memory device of the first
20 embodiment of the present disclosure. As shown in FIG. 1, the semiconductor memory device 100, which is a semiconductor memory device capable of erasing and writing memory contents in memory cells using electric signals, includes a memory cell array 101, a row decoder 102, a column decoder 103, a write/read circuit 104, and a power supply circuit 105.

The memory cell array 101 has a plurality of electrically rewritable memory cells
25 placed at intersections of bit lines and word lines. Such memory cells are arranged in a

matrix.

The power supply circuit 105 supplies voltages to the row decoder 102, the column decoder 103, and the write/read circuit 104.

The row decoder 102 applies a voltage supplied from the power supply circuit 105 to selected memory cells. The column decoder 103 applies a voltage supplied from the write/read circuit 104 to selected memory cells. The column decoder 103 also outputs information in memory cells to the write/read circuit 104 during read operation. The write/read circuit 104 outputs the voltage supplied from the power supply circuit 105 to the column decoder 103, and also has a function of determining the state of memory cells based on the memory cell information received from the column decoder 103 during read operation.

FIG. 2 is a circuit diagram showing part of the semiconductor memory device 100 of FIG. 1. Although a plurality of memory cells 207 are arranged in the memory cell array 101 and a plurality of selective transistors 206 are arranged in the column decoder 103, only part of them are shown in FIG. 2. R1 and R2 respectively denote a parasitic resistance between the memory cell 207 and the selective transistor 206 and a parasitic resistance between the selective transistor 206 and a voltage applying transistor 205 of the write/read circuit 104. The drain terminal of the voltage applying transistor 205 is coupled to an output voltage VPP2 of a booster circuit 208 of the power supply circuit 105, and the source terminal of the memory cell 207 is coupled to the ground potential via a switch (not shown).

In the power supply circuit 105, a regulator 201 is coupled to an output voltage VPP1 of the booster circuit 208, and the output of the regulator 201 is coupled to the inputs of a first switch 202 and a second switch 203. The output of the first switch 202 is coupled to the gate of the voltage applying transistor 205 that applies a voltage to the drain side of the memory cell 207. By regulating this gate voltage, the voltage applied to the drain side of the memory cell 207 can be controlled. Likewise, the output of the second switch 203 is

coupled to the gate of the memory cell 207 via the row decoder 102. By regulating this gate voltage, the voltage applied to the gate of the memory cell 207 can be controlled. Also, a voltage Vprg output from the booster circuit 208 can be applied to the gate of the memory cell 207 via a fourth switch 204 the output of which is coupled to the output of the second switch 203.

No limitation is posed on the magnitude relations among the output voltages VPP1, VPP2, and Vprg of the booster circuit 208, and appropriate voltages are set according to the characteristics of the memory cell 207. Alternatively, the output voltages VPP1, VPP2, and Vprg of the booster circuit 208 may be supplied from outside directly. Also, a plurality of booster circuits 208 may be provided.

Next, the operation in this embodiment will be described specifically. In the first mode, the fourth switch 204 is turned on, allowing the voltage Vprg to be applied to the gate of the memory cell 207 via the row decoder 102. Also, the first switch 202 is turned on and the second switch 203 is turned off, whereby an output voltage Vreg of the regulator 201 is coupled to the gate of the voltage applying transistor 205, and a voltage obtained by controlling the boosted voltage VPP2 with the output voltage Vreg of the regulator 201 is applied to the drain side of the memory cell 207 via the parasitic resistances R1 and R2 and the selective transistor 206.

In the second mode, the first switch 202 is turned off, the second switch 203 is turned on, and the fourth switch 204 is turned off, allowing the output voltage Vreg of the regulator 201 to be applied to the gate of the memory cell 207 via the row decoder 102.

The first mode represents write operation, and the second mode represents read operation.

FIG. 3 shows a specific configuration of the regulator 201. Referring to FIG. 3, a reference voltage VREF is applied to one of the input terminals of an operational amplifier

220, and resistance elements R5 and R6 are coupled to the other input terminal. The output of the operational amplifier 220 drives the gate of an output transistor 221, to allow output of the voltage Vreg.

(Second Embodiment)

5 Next, the second embodiment of the present disclosure will be described.

FIG. 4 is a circuit diagram showing the second embodiment. The configuration of the second embodiment is different from that of the first embodiment in that the output voltage Vreg of the regulator 201 is directly applied to the voltage applying transistor 205 and that the voltage on the drain side of the memory cell 207 is controlled with a third switch 209.

10 The other configuration is the same as that of the first embodiment.

The operation in this embodiment will be described specifically. In the first mode, the third switch 209 is turned on, the fourth switch 204 is turned on, and the second switch 203 is turned off, whereby the voltage Vprg is applied to the gate of the memory cell 207 via the row decoder 102, the output voltage Vreg of the regulator 201 is coupled to only the gate of the voltage applying transistor 205, and a voltage obtained by controlling the boosted voltage VPP2 with the output voltage Vreg of the regulator 201 is applied to the drain side of the memory cell 207 via the parasitic resistances R1 and R2 and the selective transistor 206.

15 In the second mode, the third switch 209 is turned off, the second switch 203 is turned on, and the fourth switch 204 is turned off, allowing the output voltage Vreg of the regulator 201 to be applied to the gate of the memory cell 207 via the row decoder 102.

The first mode represents write operation, and the second mode represents read operation.

(Third Embodiment)

FIG. 5 is a circuit diagram showing the third embodiment.

25 Although a plurality of memory cells 207 are arranged in the memory cell array 101

and a plurality of selective transistors 206 are arranged in the column decoder 103, only part of them are shown in FIG. 5. R1, R2, R3, and R4 denote parasitic resistances between the selective transistors 206 related to the memory cell 207. The drain side of the memory cell 207 is coupled to the write/read circuit 104 via the parasitic resistances R1 and R2 and the selective transistor 206. In the write/read circuit 104, whether to be applied with a voltage via the voltage applying transistor 205 or to be coupled to a sense amplifier 211 via a fifth switch 210 is selectable. Likewise, the source side of the memory cell 207 is coupled to the write/read circuit 104 via the parasitic resistances R3 and R4 and the selective transistor 206. In the write/read circuit 104, whether to be coupled to the ground potential via a grounding transistor 214 or to be applied with a voltage Vread generated by a voltage generator circuit 213 via a sixth switch 212 is selectable.

The output of the regulator 201 coupled to the output voltage VPP1 of the booster circuit 208 is coupled to the inputs of the first and second switches 202 and 203. The output of the first switch 202 is coupled to the gate of the voltage applying transistor 205 that applies a voltage to the drain side of the memory cell 207. By regulating this gate voltage, the voltage to be applied to the drain side of the memory cell 207 can be controlled. Likewise, the output of the second switch 203 is coupled to the gate of the memory cell 207 via the row decoder 102. By regulating this gate voltage, the voltage to be applied to the gate of the memory cell 207 can be controlled. Also, the voltage Vprg output from the booster circuit 208 can be applied to the gate of the memory cell 207 via the fourth switch 204 the output of which is coupled to the output of the second switch 203.

No limitation is posed on the magnitude relations among the output voltages VPP1, VPP2, and Vprg of the booster circuit 208. Appropriate voltage values are set for these voltages according to the characteristics of the memory cell 207. Alternatively, the output voltages VPP1, VPP2, and Vprg of the booster circuit 208 may be supplied from outside

directly. Also, a plurality of booster circuits 208 may be provided.

Next, the operation in this embodiment will be described specifically. In the first mode, the fourth switch 204 is turned on, the first switch 202 is turned on, the second switch 203 is turned off, the fifth switch 210 is turned off, the sixth switch 212 is turned off, and the grounding transistor 214 is turned on, allowing the voltage V_{prg} to be applied to the gate of the memory cell 207 via the row decoder 102. Also, the output voltage V_{reg} of the regulator 201 is applied to the gate of the voltage applying transistor 205, and a voltage obtained by controlling the boosted voltage V_{PP2} with the output voltage V_{reg} of the regulator 201 is applied to the drain side of the memory cell 207 via the parasitic resistances $R1$ and $R2$ and the selective transistor 206. The source side of the memory cell 207 is coupled to the ground potential.

In the second mode, the first switch 202 is turned off, the second switch 203 is turned on, the fourth switch 204 is turned off, the fifth switch 210 is turned on, the sixth switch 212 is turned on, and the grounding transistor 214 is turned off, allowing the output voltage V_{reg} of the regulator 201 to be applied to the gate of the memory cell 207 via the row decoder 102. Also, with the voltage applying transistor 205 being off, the drain side of the memory cell 207 is coupled to the sense amplifier 211 via the parasitic resistances $R1$ and $R2$ and the selective transistor 206. Moreover, the voltage V_{read} generated by the voltage generator circuit 213 is supplied to the source side of the memory cell 207 via the parasitic resistances $R3$ and $R4$ and the selective transistor 206.

The first mode represents write operation, and the second mode represents read operation.

(Fourth Embodiment)

FIG. 6 shows the fourth embodiment of the present disclosure.

The configuration of the fourth embodiment is different from that of the third

embodiment in that the voltage generator circuit 213 is coupled to the input of the fifth switch 210 and that the sense amplifier 211 is coupled to the input of the sixth switch 212. The other configuration is the same as that of the third embodiment.

This embodiment is advantageous for a device operated by switching bias
5 conditions for the memory cells 207 from one to another during read operation, such as storing two units of information in one memory cell 207.

Note that the third and fourth embodiments can also be implemented using the configuration of the second embodiment using the third switch 209.

(Fifth Embodiment)

10 FIG. 7 shows the fifth embodiment of the present disclosure.

Referring to FIG. 7, the output of a fifth switch 215 is coupled to the drain terminal of the voltage applying transistor 205, and the input of the fifth switch 215 is coupled to a circuit block 216 having a voltage generator circuit and a sense amplifier. The other configuration is the same as that of the first embodiment shown in FIG. 2.

15 The operation in this embodiment will be described specifically. In the first mode, the fourth switch 204 is turned on, the first switch 202 is turned on, the second switch 203 is turned off, and the fifth switch 215 is turned off, allowing the voltage V_{prg} to be applied to the gate of the memory cell 207 via the row decoder 102. Also, the output voltage V_{reg} of the regulator 201 is coupled to the gate of the voltage applying transistor 205, and a voltage
20 obtained by controlling the boosted voltage V_{PP2} with the output voltage V_{reg} of the regulator 201 is applied to the drain side of the memory cell 207 via the parasitic resistances $R1$ and $R2$ and the selective transistor 206.

In the second mode, the first switch 202 is turned off, the second switch 203 is turned on, the fourth switch 204 is turned off, and the fifth switch 215 is turned on, allowing
25 the output voltage V_{reg} of the regulator 201 to be applied to the gate of the memory cell 207

via the row decoder 102. Also, the voltage Vread generated by the voltage generator circuit in the circuit block 216 is supplied to the source side of the memory cell 207 via the parasitic resistances R1 and R2 and the selective transistor 206. The sense amplifier in the circuit block 216 determines the state of the memory cell 207 from a difference in the current
5 flowing at this time.

The first mode represents write operation, and the second mode represents read operation.

As described above, according to the present disclosure, one regulator can be used as both the regulator for the drain voltage of the memory cell used in the first mode and the
10 regulator for the gate voltage of the memory cell used in the second mode. Therefore, the present disclosure is useful as a small-area semiconductor memory device, and is applicable to microcomputers having such semiconductor memory devices.

CLAIMS

What is claimed is:

1. A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:
 - 5 the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein
 - an output of the regulator is coupled to inputs of the first and second switches,
 - an output of the first switch is coupled to a gate of the voltage applying transistor,
 - 10 a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and
 - an output of the second switch is coupled to a gate of the memory cell for application of a voltage.
- 15 2. A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:
 - the memory cell, one regulator, second and third switches, and a voltage applying transistor,
 - wherein
 - 20 an output of the regulator is coupled to an input of the second switch and a gate of the voltage applying transistor,
 - a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell via the third switch, and
 - an output of the second switch is coupled to a gate of the memory cell for
 - 25 application of a voltage.

3. The semiconductor memory device of claim 1, wherein
an output of a fourth switch is coupled to the output of the second switch, and
a voltage different from the output of the regulator is applied to the gate of the
5 memory cell.

4. The semiconductor memory device of claim 2, wherein
an output of a fourth switch is coupled to the output of the second switch, and
a voltage different from the output of the regulator is applied to the gate of the
10 memory cell.

5. The semiconductor memory device of claim 3, wherein
in a first operation mode, the first and fourth switches are turned on, allowing the
output voltage of the regulator to be applied to the drain terminal of the memory cell and the
15 voltage different from the output of the regulator to be applied to the gate of the memory cell,
and

in a second operation mode, the second switch is turned on, allowing the output
voltage of the regulator to be applied to the gate of the memory cell.

20 6. The semiconductor memory device of claim 4, wherein
in a first operation mode, the third and fourth switches are turned on, allowing the
output voltage of the regulator to be applied to the drain terminal of the memory cell and the
voltage different from the output of the regulator to be applied to the gate of the memory cell,
and

25 in a second operation mode, the second switch is turned on, allowing the output

voltage of the regulator to be applied to the gate of the memory cell.

7. The semiconductor memory device of claim 1, further comprising:

5 fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit,
wherein

an input of the fifth switch is coupled between the drain terminal of the voltage applying transistor and the drain terminal of the memory cell, and an input of the sense amplifier is coupled to an output of the fifth switch,

10 a source terminal of the memory cell is grounded via the grounding transistor,
an output of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and
an output of the voltage generator circuit is coupled to an input of the sixth switch.

15 8. The semiconductor memory device of claim 2, further comprising:

fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit,
wherein

20 an input of the fifth switch is coupled between the third switch and the drain terminal of the memory cell, and an input of the sense amplifier is coupled to an output of the fifth switch,

a source terminal of the memory cell is grounded via the grounding transistor,
an output of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and

25 an output of the voltage generator circuit is coupled to an input of the sixth switch.

9. The semiconductor memory device of claim 1, further comprising:

fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit,

5 wherein

an output of the fifth switch is coupled between the drain terminal of the voltage applying transistor and the drain terminal of the memory cell, and an output of the voltage generator circuit is coupled to an input of the fifth switch,

a source terminal of the memory cell is grounded via the grounding transistor,

10 an input of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and

an input of the sense amplifier is coupled to an output of the sixth switch.

10. The semiconductor memory device of claim 2, further comprising:

15 fifth and sixth switches, a grounding transistor, a sense amplifier, and a voltage generator circuit,

wherein

an output of the fifth switch is coupled between the third switch and the drain terminal of the memory cell, and an output of the voltage generator circuit is coupled to an input of the fifth switch,

a source terminal of the memory cell is grounded via the grounding transistor,

an input of the sixth switch is coupled between the source terminal of the memory cell and the grounding transistor, and

an input of the sense amplifier is coupled to an output of the sixth switch.

25

11. The semiconductor memory device of claim 1, further comprising:
a fifth switch, a sense amplifier, and a voltage generator circuit,
wherein

an output of the fifth switch is coupled between the drain terminal of the voltage
5 applying transistor and the drain terminal of the memory cell, and an output of the voltage
generator circuit and an input of the sense amplifier are coupled to an input of the fifth switch,
and
a source terminal of the memory cell is grounded.

10 12. The semiconductor memory device of claim 2, further comprising:
a fifth switch, a sense amplifier, and a voltage generator circuit,
wherein

an output of the fifth switch is coupled between the third switch and the drain
terminal of the memory cell, and an output of the voltage generator circuit and an input of the
15 sense amplifier are coupled to an input of the fifth switch, and
a source terminal of the memory cell is grounded.

13. The semiconductor memory device of claim 7, wherein
in a first operation mode, the first and fourth switches and the grounding transistor
20 are turned on, allowing the output voltage of the regulator to be applied to the drain terminal
of the memory cell, the voltage different from the output of the regulator to be applied to the
gate of the memory cell, and a source of the memory cell to be grounded, and

in a second operation mode, the second, fifth, and sixth switches are turned on,
allowing the input of the sense amplifier to be coupled to the drain terminal of the memory
25 cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the

output voltage of the voltage generator circuit to be applied to the source of the memory cell.

14. The semiconductor memory device of claim 8, wherein

in a first operation mode, the third and fourth switches and the grounding transistor
5 are turned on, allowing the output voltage of the regulator to be applied to the drain terminal
of the memory cell, the voltage different from the output of the regulator to be applied to the
gate of the memory cell, and a source of the memory cell to be grounded, and

in a second operation mode, the second, fifth, and sixth switches are turned on,
allowing the input of the sense amplifier to be coupled to the drain terminal of the memory
10 cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the
output voltage of the voltage generator circuit to be applied to the source of the memory cell.

15. The semiconductor memory device of claim 9, wherein

in a first operation mode, the first and fourth switches and the grounding transistor
15 are turned on, allowing the output voltage of the regulator to be applied to the drain terminal
of the memory cell, the voltage different from the output of the regulator to be applied to the
gate of the memory cell, and the source of the memory cell to be grounded, and

in a second operation mode, the second, fifth, and sixth switches are turned on,
allowing the output voltage of the voltage generator circuit to be applied to the drain terminal
20 of the memory cell, the output voltage of the regulator to be applied to the gate of the memory
cell, and the input of the sense amplifier to be coupled to the source terminal of the memory
cell.

16. The semiconductor memory device of claim 10, wherein

25 in a first operation mode, the third and fourth switches and the grounding transistor

are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and

in a second operation mode, the second, fifth, and sixth switches are turned on,
5 allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, the output voltage of the regulator to be applied to the gate of the memory cell, and the input of the sense amplifier to be coupled to the source terminal of the memory cell.

10 17. The semiconductor memory device of claim 11, wherein
in a first operation mode, the first and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the gate of the memory cell, and the source of the memory cell to be grounded, and

15 in a second operation mode, the second and fifth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, as well as the input of the sense amplifier to be coupled to the drain terminal of the memory cell, and the output voltage of the regulator to be applied to the gate of the memory cell.

20

18. The semiconductor memory device of claim 12, wherein
in a first operation mode, the third and fourth switches and the grounding transistor are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell, the voltage different from the output of the regulator to be applied to the
25 gate of the memory cell, and the source of the memory cell to be grounded, and

in a second operation mode, the second and fifth switches are turned on, allowing the output voltage of the voltage generator circuit to be applied to the drain terminal of the memory cell, as well as the input of the sense amplifier to be coupled to the drain terminal of the memory cell, and the output voltage of the regulator to be applied to the gate of the
5 memory cell.

19. The semiconductor memory device of claim 5, wherein
the first operation mode represents write into the memory cell, and the second
operation mode represents read of memory cell information.

10

20. The semiconductor memory device of claim 3, wherein
the voltage different from the output of the regulator is an output voltage of a
booster circuit.

15 21. The semiconductor memory device of claim 1, wherein
an output of a booster circuit is coupled to a source terminal of the voltage applying
transistor.

ABSTRACT

In a semiconductor memory device, the output of a regulator is coupled to the inputs of first and second switches, the output of the first switch is coupled to a path for supplying the drain voltage of a memory cell in the first mode, and the output of the second switch is coupled to a path for supplying the gate voltage of the memory cell in the second mode. A fourth switch is placed in parallel with the second switch: the output of the fourth switch is coupled to the output of the second switch, to supply the gate voltage of the memory cell in the first mode. Thus, one regulator is used as both the regulator for the drain voltage of the memory cell and the regulator for the gate voltage of the memory cell.

Electronic Acknowledgement Receipt

EFS ID:	13562395
Application Number:	13591766
International Application Number:	
Confirmation Number:	2466
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Reiji MOCHIDA
Customer Number:	53080
Filer:	Michael E. Fogarty/Margaret Barham
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0824
Receipt Date:	22-AUG-2012
Filing Date:	
Time Stamp:	15:49:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1310
RAM confirmation Number	2270
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	P60241601_DEC_085393-0824.pdf	158930	no	3
			ac021e37932b6f19b0d27b977d997a2daf6bc842		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	P60241601_DRW_085393-0824.pdf	66771	no	5
			10981a6ea455f602edc138761ff4cc4295f84c90		
Warnings:					
Information:					
3	Transmittal Letter	P60241601_IDS_085393-0824.PDF	98667	no	5
			323e72f1c77aa53f805b0576cad8901ec2a7600		
Warnings:					
Information:					
4	Non Patent Literature	P60241601_ISR_085393-0824.pdf	148389	no	3
			383f606a3d5027b4b1084e9cdc55359559645fd1		
Warnings:					
Information:					
5	Miscellaneous Incoming Letter	P60241601_PCT_085393-0824.pdf	621058	no	14
			c640195d159e86dae6f91407919784d5b3eecca		
Warnings:					
Information:					
6	Foreign Reference	P60241601_REF_085393-0824.PDF	597655	no	18
			7c396d59b65743b42e71829cbefeb0dc69eed9b4		
Warnings:					
Information:					
7		P60241601_SPEC_CLAIMS_ABS T_085393-0824.pdf	905393	yes	25
			c8eed23832a2701aaab568696544cf42058fea5a		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	16	
	Claims		17	24	
	Abstract		25	25	
SK hynix Ex. 1002, Page 83 of 145					

Warnings:					
Information:					
8	Transmittal of New Application	P60241601_TRN_085393-0824. PDF	62406 a62a84e9ace0af3aacee3a967dfd45d9ca3c1e2d	no	3
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	36399 e5a0a04f64ba5a1cd7d3ae7d8cc15f4b7de7efa8	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2695668		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/591,766				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250			
TOTAL CLAIMS (37 CFR 1.16(j))	21	minus 20 = * 1				x 60 =	60			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *				x 250 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
			TOTAL			TOTAL	1310			
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/591,766	08/22/2012	2827	1310	085393-0824	21	2

CONFIRMATION NO. 2466

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

FILING RECEIPT



Date Mailed: 09/06/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Reiji MOCHIDA, Osaka, JAPAN;
Takafumi Maruyama, Osaka, JAPAN;
Yukimasa Hamamoto, Kyoto, JAPAN;

Assignment For Published Patent Application

Panasonic Corporation, Osaka, JAPAN

Power of Attorney: The patent practitioners associated with Customer Number 53080

Domestic Priority data as claimed by applicant

This application is a CON of PCT/JP2010/007402 12/21/2010

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

JAPAN 2010-052722 03/10/2010

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/30/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/591,766**

Projected Publication Date: 12/13/2012

Non-Publication Request: No

Early Publication Request: No
Title

SEMICONDUCTOR MEMORY DEVICE

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日

Date of Application:

2010年 3月10日

出 願 番 号

Application Number:

特願2010-052722

パリ条約による外国への出願
に用いる優先権の主張の基礎
となる出願の国コードと出願
番号

The country code and number
of your priority application,
to be used for filing abroad
under the Paris Convention, is

J P 2010-052722

出 願 人

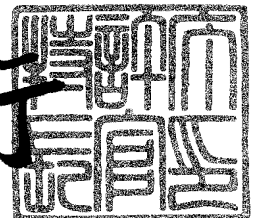
Applicant(s):

パナソニック株式会社

2012年 9月24日

特許庁長官
Commissioner,
Japan Patent Office

深野弘行



【書類名】	特許願
【整理番号】	2037610005
【あて先】	特許庁長官 殿
【国際特許分類】	G11C 16/06
【発明者】	
【住所又は居所】	大阪府門真市大字門真 1 0 0 6 番地 パナソニック株式会社内
【氏名】	持田 礼司
【発明者】	
【住所又は居所】	大阪府門真市大字門真 1 0 0 6 番地 パナソニック株式会社内
【氏名】	圓山 敬史
【発明者】	
【住所又は居所】	大阪府門真市大字門真 1 0 0 6 番地 パナソニック株式会社内
【氏名】	濱本 幸昌
【特許出願人】	
【識別番号】	000005821
【氏名又は名称】	パナソニック株式会社
【代理人】	
【識別番号】	100077931
【弁理士】	
【氏名又は名称】	前田 弘
【選任した代理人】	
【識別番号】	100110939
【弁理士】	
【氏名又は名称】	竹内 宏
【選任した代理人】	
【識別番号】	100110940
【弁理士】	
【氏名又は名称】	嶋田 高久
【選任した代理人】	
【識別番号】	100113262
【弁理士】	
【氏名又は名称】	竹内 祐二
【選任した代理人】	
【識別番号】	100115059
【弁理士】	
【氏名又は名称】	今江 克実
【選任した代理人】	
【識別番号】	100117581
【弁理士】	
【氏名又は名称】	二宮 克也
【選任した代理人】	
【識別番号】	100117710
【弁理士】	
【氏名又は名称】	原田 智雄
【電話番号】	06-6125-2255
【連絡先】	担当
【選任した代理人】	
【識別番号】	100121728
【弁理士】	
【氏名又は名称】	井関 勝守

【選任した代理人】
【識別番号】 100124671
【弁理士】
【氏名又は名称】 関 啓
【選任した代理人】
【識別番号】 100131060
【弁理士】
【氏名又は名称】 杉浦 靖也
【手数料の表示】
【予納台帳番号】 014409
【納付金額】 15,000円
【提出物件の目録】
【物件名】 明細書 1
【物件名】 特許請求の範囲 1
【物件名】 要約書 1
【物件名】 図面 1
【包括委任状番号】 0814523

【書類名】明細書

【発明の名称】半導体記憶装置

【技術分野】

【0001】

本発明は、半導体記憶装置に関し、特に、EEPROM (Electrically Erasable Programmable Read Only Memory) 等の不揮発性メモリに関する。

【背景技術】

【0002】

EEPROMでは、メモリセルの記憶内容を電気信号によって消去及び書き換えすることができる。具体的な書込みには、HCI (Hot Carrier Injection: ホットキャリア注入) を利用するものがある。その際、第1のレギュレータ出力をメモリセルのゲートに印加すると共に、第2のレギュレータ出力は電圧印加トランジスタのゲートに接続し、前記電圧印加トランジスタのドレイン端から前記メモリセルのドレイン端に電圧を印加しながら、メモリセルのゲート電圧を調整する。このような技術は、例えば、特許文献1に記載されている。

【先行技術文献】

【特許文献】

【0003】

【特許文献1】特開2008-217914号公報(第9図)

【発明の概要】

【発明が解決しようとする課題】

【0004】

しかしながら、前記従来の回路構成では、必要な出力電圧範囲や精度が異なるために、メモリセルのドレイン電圧用レギュレータと、メモリセルのゲート電圧用レギュレータとの2基のレギュレータが必要となり、回路面積が大きくなるという課題がある。

【課題を解決するための手段】

【0005】

前記課題を解決するために、本発明では、前記2基のレギュレータの兼用化を図ることとして、電圧印加トランジスタのドレイン端からメモリセルのドレイン端に印加する電圧をレギュレータで調整する際には、メモリセルのゲート電圧をレギュレータを介さずに電圧印加する構成を採用する。

【0006】

具体的に、請求項1記載の発明の半導体記憶装置は、メモリセルの記憶内容を電気信号によって消去及び書き込みすることができる半導体記憶装置であって、前記メモリセルと、1個のレギュレータと、第1及び第2のスイッチと、前記メモリセルに電圧を印加するための電圧印加トランジスタとを有し、前記レギュレータの出力は前記第1及び第2のスイッチの入力が接続され、前記第1のスイッチの出力は前記電圧印加トランジスタのゲートに接続され、前記電圧印加トランジスタのドレイン端から前記メモリセルのドレイン端に電圧を印加し、前記第2のスイッチの出力は前記メモリセルのゲートに接続されて電圧を印加することを特徴とする。

【0007】

請求項2記載の発明の半導体記憶装置は、メモリセルの記憶内容を電気信号によって消去及び書き込みすることができる半導体記憶装置であって、前記メモリセルと、1個のレギュレータと、第2及び第3のスイッチと、電圧印加トランジスタとを有し、前記レギュレータの出力は、前記第2のスイッチの入力と、前記電圧印加トランジスタのゲートとに接続され、前記電圧印加トランジスタのドレイン端から前記第3のスイッチを介して前記メモリセルのドレイン端に電圧を印加し、前記第2のスイッチの出力は前記メモリセルのゲートに接続されて電圧を印加することを特徴とする。

【0008】

請求項3記載の発明は、前記請求項1記載の半導体記憶装置であって、前記第2のスイ

ッチの出力に第4のスイッチの出力が接続され、前記レギュレータ出力とは異なる電圧を前記メモリセルのゲートに印加することを特徴とする。

【0009】

請求項4記載の発明は、前記請求項2記載の半導体記憶装置であって、前記第2のスイッチの出力に第4のスイッチの出力が接続され、前記レギュレータ出力とは異なる電圧を前記メモリセルのゲートに印加することを特徴とする。

【0010】

請求項5記載の発明は、前記請求項3記載の半導体記憶装置であって、第1の動作モードでは、前記第1及び第4のスイッチがオンし、前記メモリセルのドレイン端には前記レギュレータの出力電圧で調整された電圧が印加され、前記メモリセルのゲートには前記レギュレータの出力とは異なる電圧が印加され、第2の動作モードでは、前記第2のスイッチがオンし、前記メモリセルのゲートに前記レギュレータの出力電圧が印加されることを特徴とする。

【0011】

請求項6記載の発明は、前記請求項4記載の半導体記憶装置であって、第1の動作モードでは、前記第3及び第4のスイッチがオンし、前記メモリセルのドレイン端には前記レギュレータの出力電圧で調整された電圧が印加され、前記メモリセルのゲートには前記レギュレータの出力とは異なる電圧が印加され、第2の動作モードでは、前記第2のスイッチがオンし、前記メモリセルのゲートに前記レギュレータの出力電圧が印加されることを特徴とする。

【0012】

請求項7記載の発明は、前記請求項5又は6記載の半導体記憶装置であって、前記第1の動作モードはメモリセルへの書込み、前記第2の動作モードはメモリセル情報の読出しであることを特徴とする。

【0013】

以上により、請求項1～7記載の発明では、第1のモード時（例えば書き込み時）には、メモリセルのゲート電圧はレギュレートしない電圧を直接印加し、レギュレータの出力を電圧印加トランジスタのゲートに与えて、メモリセルのドレイン側に印加する電圧を前記レギュレータの出力電圧で制御する。一方、第2のモード（例えば読み出し時）には、前記レギュレータの出力をメモリセルのゲートに与えて、メモリセルのゲート電圧を制御する。

【0014】

従って、第1のモードにおけるメモリセルのゲート電圧はレギュレータを介さずに電圧印加されるので、第1のモードで使用するメモリセルのドレイン電圧印加レギュレータと、第2のモードで使用するメモリセルのゲート電圧レギュレータとを兼用化することができ、小面積な半導体記憶装置を提供できる。

【発明の効果】

【0015】

以上説明したように、本発明によれば、第1のモードで使用するメモリセルのドレイン電圧印加レギュレータと、第2のモードで使用するメモリセルのゲート電圧レギュレータとを兼用化して、小面積な半導体記憶装置を提供できる。

【図面の簡単な説明】

【0016】

【図1】 本発明の第1の実施形態に係る半導体記憶装置の構成を示すブロック図である。

【図2】 同半導体記憶装置の要部構成を示す回路図である。

【図3】 同半導体記憶装置に備えるレギュレータの具体的構成を示す図である。

【図4】 本発明の第2の実施形態の半導体記憶装置の要部構成を示す図である。

【図5】 本発明の第3の実施形態の半導体記憶装置の要部構成を示す図である。

【図6】 本発明の第4の実施形態の半導体記憶装置の要部構成を示す図である。

【図 7】 本発明の第 5 の実施形態の半導体記憶装置の要部構成を示す図である。
【発明を実施するための形態】

【0017】

以下、本発明の実施形態を説明する。

【0018】

(第 1 の実施形態)

図 1 は、本発明の第 1 の実施形態に係る半導体記憶装置の構成を示すブロック図である。同図に示すように、本半導体記憶装置 100 は、メモリセルの記憶内容を電気信号によって消去及び書き込みすることができる半導体記憶装置であって、内部に、メモリセルアレイ 101、ロウデコーダ 102、カラムデコーダ 103、書込み・読出し回路 104、電源回路 105 を具備している。

【0019】

前記メモリセルアレイ 101 は、ビット線とワード線との交差部に配置される電氣的に書換え可能な複数のメモリセルを有している。これらのメモリセルは行列状に配置されている。

【0020】

前記電源回路 105 は、前記ロウデコーダ 102、カラムデコーダ 103、書込み・読出し回路 104 に電圧を供給している。

【0021】

前記ロウデコーダ 102 は、電源回路 105 から供給された電圧を、選択されたメモリセルに印加する。また、カラムデコーダ 103 は、書込み・読出し回路 104 から供給された電圧を、選択されたメモリセルに印加する。更に、カラムデコーダ 103 は、読出し時にはメモリセルの情報を書込み・読出し回路 104 に出力する。書込み・読出し回路 104 は、電源回路 105 から供給された電圧をカラムデコーダ 103 に出力し、読出し時にはカラムデコーダ 103 から入力されたメモリセル情報からメモリセルの状態を判定する機能を有する。

【0022】

図 2 は、前記図 1 の半導体記憶装置 100 の一部を示す回路図である。メモリセルアレイ 101 には複数のメモリセル 207 が配置され、カラムデコーダ 103 には複数の選択トランジスタ 206 が配置されており、図 2 にはその一部を記載している。R1、R2 は、各々、メモリセル 207 と選択トランジスタ 206 との間の寄生抵抗、及び選択トランジスタ 206 と書込み・読出し回路 104 の電圧印加トランジスタ 205 との間の寄生抵抗を示している。前記電圧印加トランジスタ 205 のドレイン端には、電源回路 105 の昇圧回路 208 の出力電圧 VPP2 が接続されている。そして、メモリセル 207 のソース側はスイッチ（図示せず）を介して接地電位に接続されている。

【0023】

前記電源回路 105 において、昇圧電圧 208 の出力電圧 VPP1 を接続したレギュレータ 201 の出力には、第 1 のスイッチ 202 及び第 2 のスイッチ 203 の入力接続され、第 1 のスイッチ 202 の出力はメモリセル 207 のドレイン側に電圧を印加する電圧印加トランジスタ 205 のゲートに接続され、このゲート電圧をレギュレートすることにより、メモリセル 207 のドレイン側に印加する電圧を制御することが可能である。また、第 2 のスイッチ 203 の出力はロウデコーダ 102 を介してメモリセル 207 のゲートに接続され、このゲート電圧をレギュレートすることにより、メモリセル 207 のゲートに印加する電圧を制御することが可能である。更に、メモリセル 207 のゲートには、出力を前記第 2 のスイッチ 203 の出力に接続した第 4 のスイッチ 204 を介して昇圧回路 208 から出力された電圧 Vprg を印加することも可能である。

【0024】

尚、昇圧回路 208 の出力電圧 VPP1、VPP2、Vprg は、電圧の大小関係に制約はなく、メモリセル 207 の特性に応じて最適な電圧を設定する。更に、昇圧回路 208 の出力電圧 VPP1、VPP2、Vprg は外部から直接印加しても良い。また、昇圧

回路208は複数で構成しても良い。

【0025】

次に、本実施形態の動作について具体的に説明する。第1のモードにおいて、第4のスイッチ204はオンし、メモリセル207のゲートにはロウデコーダ102を介して電圧 V_{prg} が印加される。また、第1のスイッチ202をオン、第2のスイッチ203をオフとすることにより、レギュレータ201の出力電圧 V_{reg} は電圧印加トランジスタ205のゲートに接続され、昇圧電圧 V_{PP2} をレギュレータの出力電圧 V_{reg} で制御した電圧が、寄生抵抗 R_1 、 R_2 や選択トランジスタ206を介してメモリセル207のドレイン側に印加される。

【0026】

次に第2のモードにおいては、第1のスイッチ202をオフ、第2のスイッチ203をオン、第4のスイッチ204をオフとすることにより、メモリセル207のゲートには、ロウデコーダ102を介してレギュレータ201の出力電圧 V_{reg} が印加される。

【0027】

ここで、第1のモードは書込み動作を、第2のモードは読出し動作を示している。

【0028】

図3は、レギュレータ201の具体的構成の一例を示す。同図において、オペアンプ220の入力端子の一方には基準電圧 V_{REF} が印加され、その入力端子の他方には抵抗素子 R_5 と抵抗素子 R_6 とが接続されている。オペアンプ220の出力は出力トランジスタ221のゲートを駆動し、出力電圧 V_{reg} を出力する。

【0029】

(第2の実施形態)

次に、本発明の第2の実施形態を説明する。

【0030】

図4は、本発明の第2の実施形態を示す回路図である。前記第1の実施形態と異なる点は、レギュレータ201の出力電圧 V_{reg} を直接に電圧印加トランジスタ205に印加し、第3のスイッチ209によって、メモリセル207のドレイン側の電圧を制御する。その他の構成は第1の実施形態と同様である。

【0031】

次に、本実施形態の動作について具体的に説明する。第1のモードにおいて、第3のスイッチ209をオン、第4のスイッチ204をオン、第2のスイッチ203をオフとすることにより、メモリセル207のゲートにはロウデコーダ102を介して電圧 V_{prg} が印加され、レギュレータ201の出力電圧 V_{reg} は電圧印加トランジスタ205のゲートにのみ接続され、昇圧電圧 V_{PP2} をレギュレータ201の出力電圧 V_{reg} で制御した電圧が、寄生抵抗 R_1 、 R_2 や選択トランジスタ206を介してメモリセル207のドレイン側に印加される。

【0032】

次に、第2のモードにおいては、第3のスイッチ209をオフ、第2のスイッチ203をオン、第4のスイッチ204をオフとすることにより、メモリセル207のゲートにはロウデコーダ102を介してレギュレータ201の出力電圧 V_{reg} が印加される。

【0033】

ここで、第1のモードは書込み動作、第2のモードは読出し動作を示している。

【0034】

(第3の実施形態)

図5は、本発明の第3の実施形態を示す回路図である。

【0035】

同図において、メモリセルアレイ101には複数のメモリセル207が、カラムデコーダ103には複数の選択トランジスタ206が配置されており、図5にはその一部を記載している。 R_1 、 R_2 、 R_3 、 R_4 はメモリセル207に関わる選択トランジスタ206間の寄生抵抗を示している。メモリセル207のドレイン側はこの寄生抵抗 R_1 、 R_2 と

選択トランジスタ206を介して書込み・読出し回路104に接続される。そして、書込み・読出し回路104内で、電圧印加トランジスタ205を介して電圧を印加するか、スイッチ210を介してセンスアンプ211に接続するかを選択可能な構成となっている。更に、メモリセル207のソース側も寄生抵抗R3、R4と選択トランジスタ206とを介して、書込み・読出し回路104に接続される。そして、この書込み・読出し回路104内で、トランジスタ214を介して接地電位に接続するか、スイッチ212を介して電圧発生回路213で発生した電圧を印加するかを選択可能な構成となっている。

【0036】

昇圧電圧208の出力電圧VPP1を接続したレギュレータ201の出力には、第1及び第2のスイッチ202、203の入力が接続され、第1のスイッチ202の出力は、メモリセル207のドレイン側に電圧を印加する電圧印加トランジスタ205のゲートに接続され、このゲート電圧をレギュレートすることにより、メモリセル207のドレイン側に印加する電圧を制御することが可能である。また、第2のスイッチ203の出力はロウデコーダ102を介してメモリセル207のゲートに接続され、このゲート電圧をレギュレートすることにより、メモリセル207のゲートに印加する電圧を制御することが可能である。更に、メモリセル207のゲートには、出力を第2のスイッチ203の出力に接続した第4のスイッチ204を介して昇圧回路208から出力された電圧Vprgを印加することも可能である。

【0037】

尚、昇圧回路208の出力電圧VPP1、VPP2、Vprgは、電圧の大小関係に制約はなく、メモリセル207の特性に応じて最適な電圧を設定する。更に、昇圧回路208の出力電圧VPP1、VPP2、Vprgは外部から直接印加しても良い。また、昇圧回路208は複数で構成しても良い。

【0038】

次に、本実施形態の動作について具体的に説明する。第1のモードにおいて、第4のスイッチ204をオン、第1のスイッチ202をオン、第2のスイッチ203をオフ、スイッチ210をオフ、スイッチ212をオフ、トランジスタ214をオンとする。これにより、メモリセル207のゲートには、ロウデコーダ102を介して電圧Vprgが印加される。また、レギュレータ201の出力電圧Vregは電圧印加トランジスタ205のゲートに接続され、昇圧電圧VPP2をレギュレータ201の出力電圧Vregで制御した電圧が、寄生抵抗R1、R2や選択トランジスタ206を介してメモリセル207のドレイン側に印加される。更にメモリセル207のソース側は接地電位に接続される。

【0039】

次に、第2のモードにおいては、第1のスイッチ202をオフ、第2のスイッチ203をオン、第4のスイッチ204をオフ、スイッチ210をオン、スイッチ212をオン、トランジスタ214をオフとする。これにより、メモリセル207のゲートには、ロウデコーダ102を介してレギュレータ201の出力電圧Vregが印加される。また、電圧印加トランジスタ205はオフのため、メモリセル207のドレイン側は寄生抵抗R1、R2や選択トランジスタ206を介してセンスアンプ211に接続される。更に、メモリセル207のソース側は寄生抵抗R3、R4や選択トランジスタ206を介し、電圧発生回路213で発生した電圧が供給される。

【0040】

ここで、第1のモードは書込み動作、第2のモードは読出し動作を示している。

【0041】

(第4の実施形態)

図6は本発明の第4の実施形態を示す。

【0042】

本実施形態が前記第3の実施形態と異なる点は、スイッチ210の入力側に電圧発生回路213を接続し、スイッチ212の入力側にセンスアンプ211を接続した構成である。その他の構成は第3の実施形態と同様である。

【0043】

本実施形態は、1つのメモリセル207に2つの情報を記憶するなど、読出し動作時のメモリセル207へのバイアス条件を切り替えて動作させるデバイスに対して有効である。

【0044】

ここで、第1のモードは書込み動作、第2のモードは読出し動作を示している。

【0045】

尚、前記第3の実施形態及び第4の実施形態では、前記第2の実施形態の第3のスイッチ209を用いた構成でも可能である。

【0046】

(第5の実施形態)

図7は本発明の第5の実施形態を示す。

【0047】

同図においては、電圧印加トランジスタ205のドレイン端にスイッチ215の出力を接続し、電圧発生回路とセンスアンプを搭載した回路ブロック216をスイッチ215の入力に接続している。その他の構成は図2に示した第1の実施形態と同様である。

【0048】

次に、本実施形態の動作について具体的に説明する。第1のモードにおいて、第4のスイッチ204をオン、第1のスイッチ202をオン、第2のスイッチ203をオフ、スイッチ215をオフとする。これにより、メモリセル207のゲートには、ロウデコーダ102を介して電圧V_{prg}が印加される。また、レギュレータ201の出力電圧V_{reg}は電圧印加トランジスタ205のゲートに接続され、昇圧電圧V_{PP2}をレギュレータ201の出力電圧V_{reg}で制御した電圧が、寄生抵抗R₁、R₂や選択トランジスタ206を介してメモリセル207のドレイン側に印加される。

【0049】

次に、第2のモードにおいては、第1のスイッチ202をオフ、第2のスイッチ203をオン、第4のスイッチ204をオフ、スイッチ215をオンとすることにより、メモリセル207のゲートには、ロウデコーダ102を介してレギュレータ201の出力電圧V_{reg}が印加される。また、メモリセル207のソース側は寄生抵抗R₁、R₂や選択トランジスタ206を介して、回路ブロック216に搭載されている電圧発生回路で発生した電圧が供給され、この時に流れる電流の違いから、回路ブロック216内のセンスアンプでメモリセル207の状態を判定する。

【0050】

ここで、第1のモードは書込み動作、第2のモードは読出し動作を示している。

【産業上の利用可能性】

【0051】

以上説明したように、本発明は、第1のモードで使用するメモリセルのドレイン電圧レギュレータと、第2のモードで使用するメモリセルのゲート電圧レギュレータとを兼用できるので、小面積な半導体記憶装置として有用であり、これを搭載したマイコン等に適用できる。

【符号の説明】

【0052】

- 101 メモリセルアレイ
- 102 ロウデコーダ
- 103 カラムデコーダ
- 104 書込み・読出し回路
- 105 電源回路
- 201 レギュレータ
- 202 第1のスイッチ
- 203 第2のスイッチ

204	第4のスイッチ
209	第3のスイッチ
205	電圧印加トランジスタ
206	選択トランジスタ
207	メモリセル
208	昇圧回路
211	センスアンプ
213	電圧発生回路
220	オペアンプ
221	出力トランジスタ

【書類名】 特許請求の範囲

【請求項 1】

メモリセルの記憶内容を電気信号によって消去及び書き込みすることができる半導体記憶装置であって、

前記メモリセルと、1個のレギュレータと、第1及び第2のスイッチと、前記メモリセルに電圧を印加するための電圧印加トランジスタとを有し、

前記レギュレータの出力は前記第1及び第2のスイッチの入力が接続され、

前記第1のスイッチの出力は前記電圧印加トランジスタのゲートに接続され、

前記電圧印加トランジスタのドレイン端から前記メモリセルのドレイン端に電圧を印加し、

前記第2のスイッチの出力は前記メモリセルのゲートに接続されて電圧を印加することを特徴とする半導体記憶装置。

【請求項 2】

メモリセルの記憶内容を電気信号によって消去及び書き込みすることができる半導体記憶装置であって、

前記メモリセルと、1個のレギュレータと、第2及び第3のスイッチと、電圧印加トランジスタとを有し、

前記レギュレータの出力は、前記第2のスイッチの入力と、前記電圧印加トランジスタのゲートとに接続され、

前記電圧印加トランジスタのドレイン端から前記第3のスイッチを介して前記メモリセルのドレイン端に電圧を印加し、

前記第2のスイッチの出力は前記メモリセルのゲートに接続されて電圧を印加することを特徴とする半導体記憶装置。

【請求項 3】

前記請求項 1 記載の半導体記憶装置であって、

前記第2のスイッチの出力に第4のスイッチの出力が接続され、

前記レギュレータ出力とは異なる電圧を前記メモリセルのゲートに印加することを特徴とする半導体記憶装置。

【請求項 4】

前記請求項 2 記載の半導体記憶装置であって、

前記第2のスイッチの出力に第4のスイッチの出力が接続され、

前記レギュレータ出力とは異なる電圧を前記メモリセルのゲートに印加することを特徴とする半導体記憶装置。

【請求項 5】

前記請求項 3 記載の半導体記憶装置であって、

第1の動作モードでは、前記第1及び第4のスイッチがオンし、前記メモリセルのドレイン端には前記レギュレータの出力電圧で調整された電圧が印加され、前記メモリセルのゲートには前記レギュレータの出力とは異なる電圧が印加され、

第2の動作モードでは、前記第2のスイッチがオンし、前記メモリセルのゲートに前記レギュレータの出力電圧が印加される

ことを特徴とする半導体記憶装置。

【請求項 6】

前記請求項 4 記載の半導体記憶装置であって、

第1の動作モードでは、前記第3及び第4のスイッチがオンし、前記メモリセルのドレイン端には前記レギュレータの出力電圧で調整された電圧が印加され、前記メモリセルのゲートには前記レギュレータの出力とは異なる電圧が印加され、

第2の動作モードでは、前記第2のスイッチがオンし、前記メモリセルのゲートに前記レギュレータの出力電圧が印加される

ことを特徴とする半導体記憶装置。

【請求項 7】

前記請求項 5 又は 6 記載の半導体記憶装置であって、
前記第 1 の動作モードはメモリセルへの書込み、前記第 2 の動作モードはメモリセル情報
の読出しである
ことを特徴とする半導体記憶装置。

【書類名】 要約書

【要約】

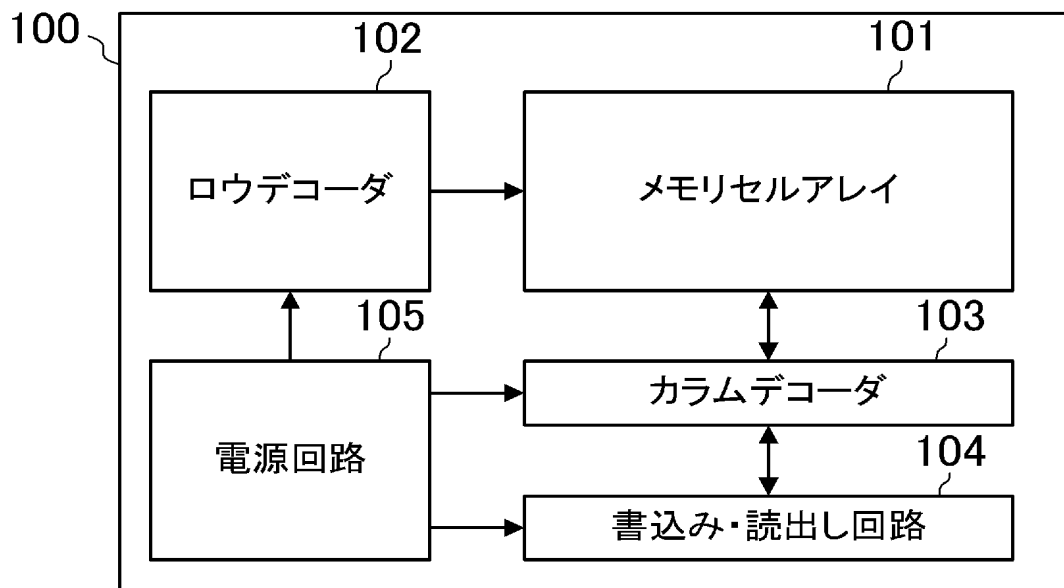
【課題】 メモリセルのドレイン電圧用レギュレータと、メモリセルのゲート電圧用レギュレータとの2基のレギュレータを1個のレギュレータで兼用する。

【解決手段】 レギュレータ201の出力に第1、第2のスイッチ202、203の入力を接続し、前記第1のスイッチ202の出力は第1のモード時にメモリセル207のドレイン電圧を供給するパスに接続し、前記第2のスイッチ203の出力は第2のモード時にメモリセル207のゲート電圧を供給するパスに接続される。また、前記第2のスイッチ203と並列に第4のスイッチ204が設けられる。この第4のスイッチ204の出力側は前記第2のスイッチ203の出力側と接続され、第1のモード時のメモリセル207のゲート電圧を供給する。

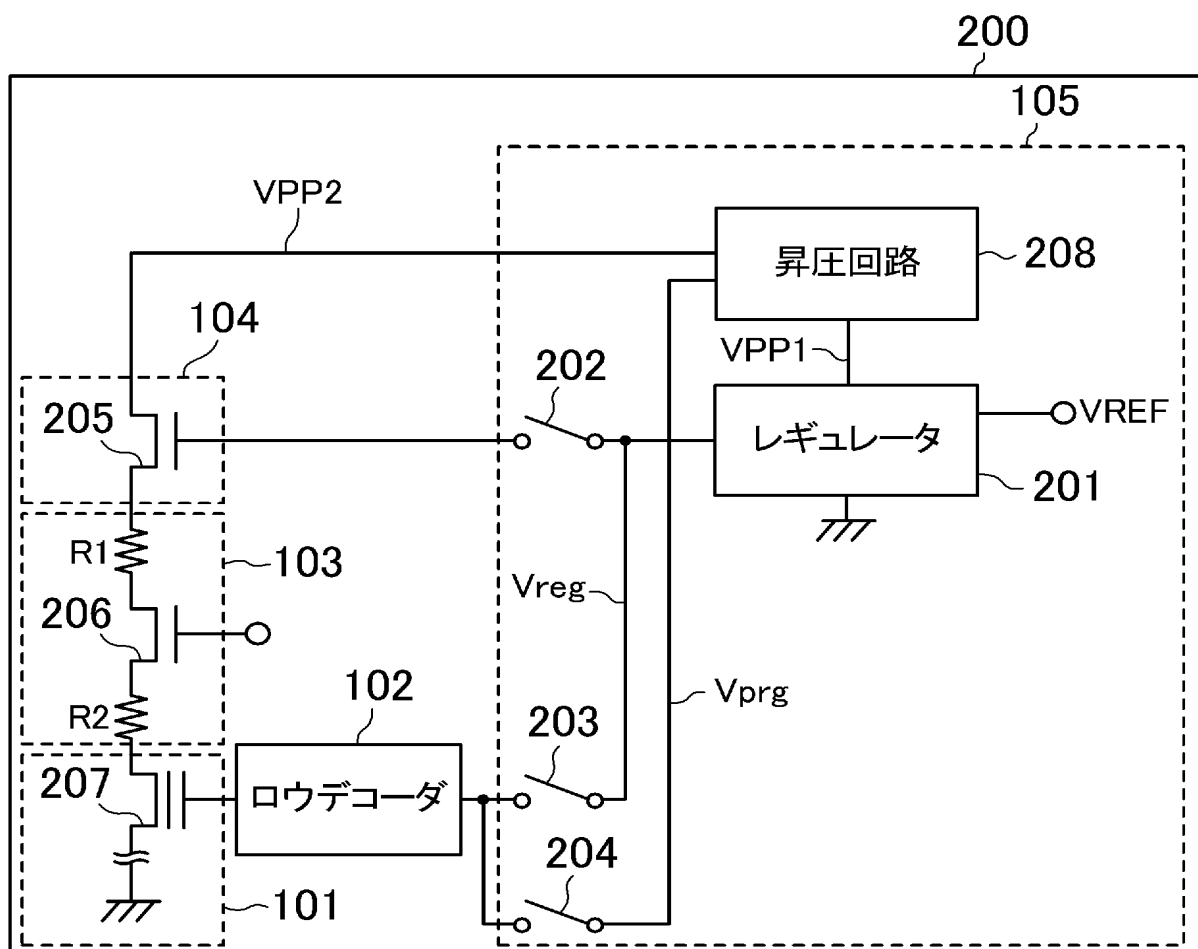
【選択図】 図5

【書類名】 図面

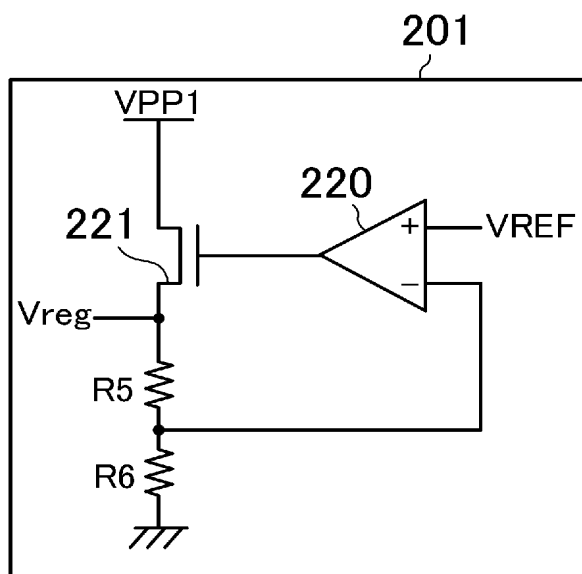
【図 1】



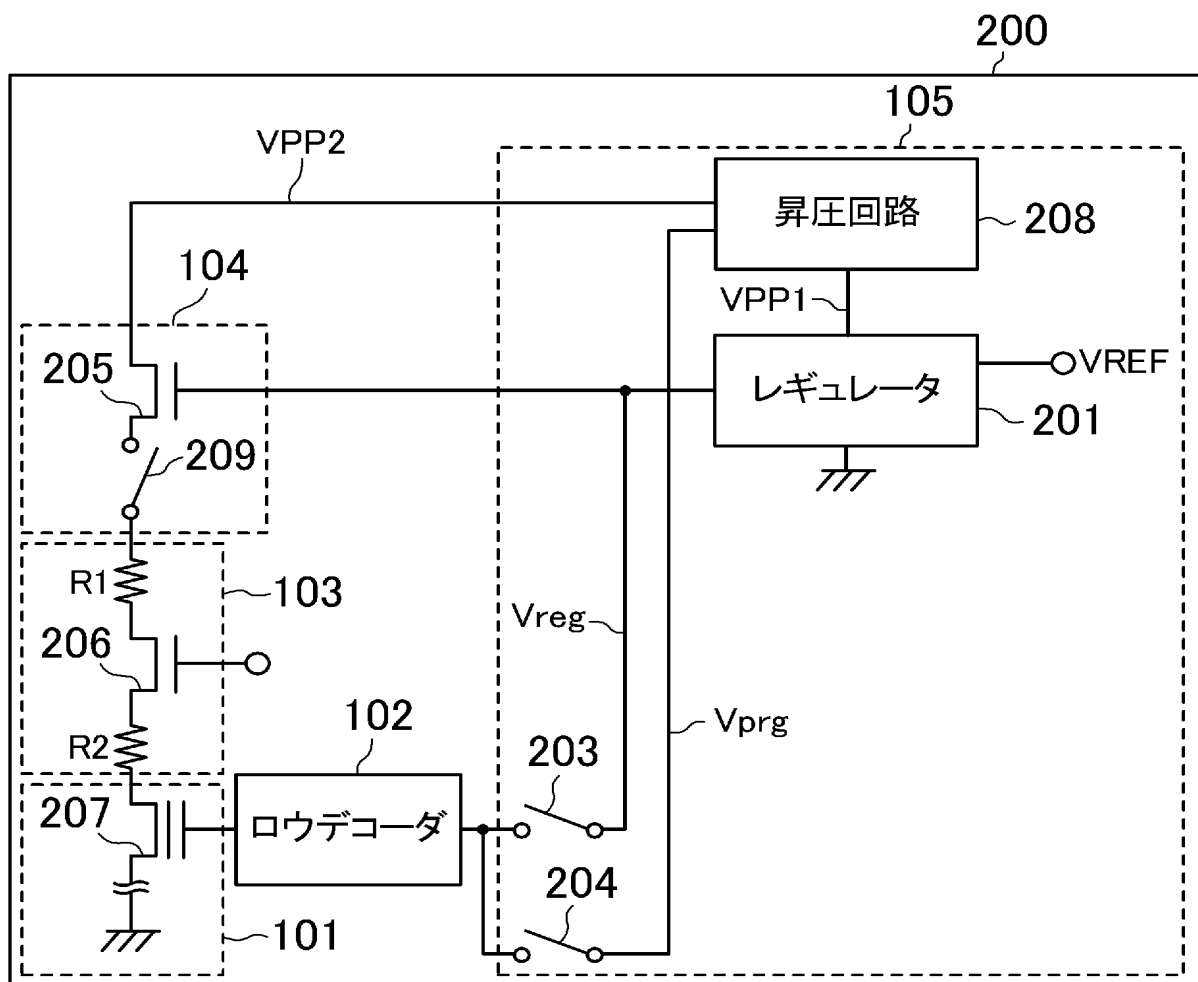
【図 2】



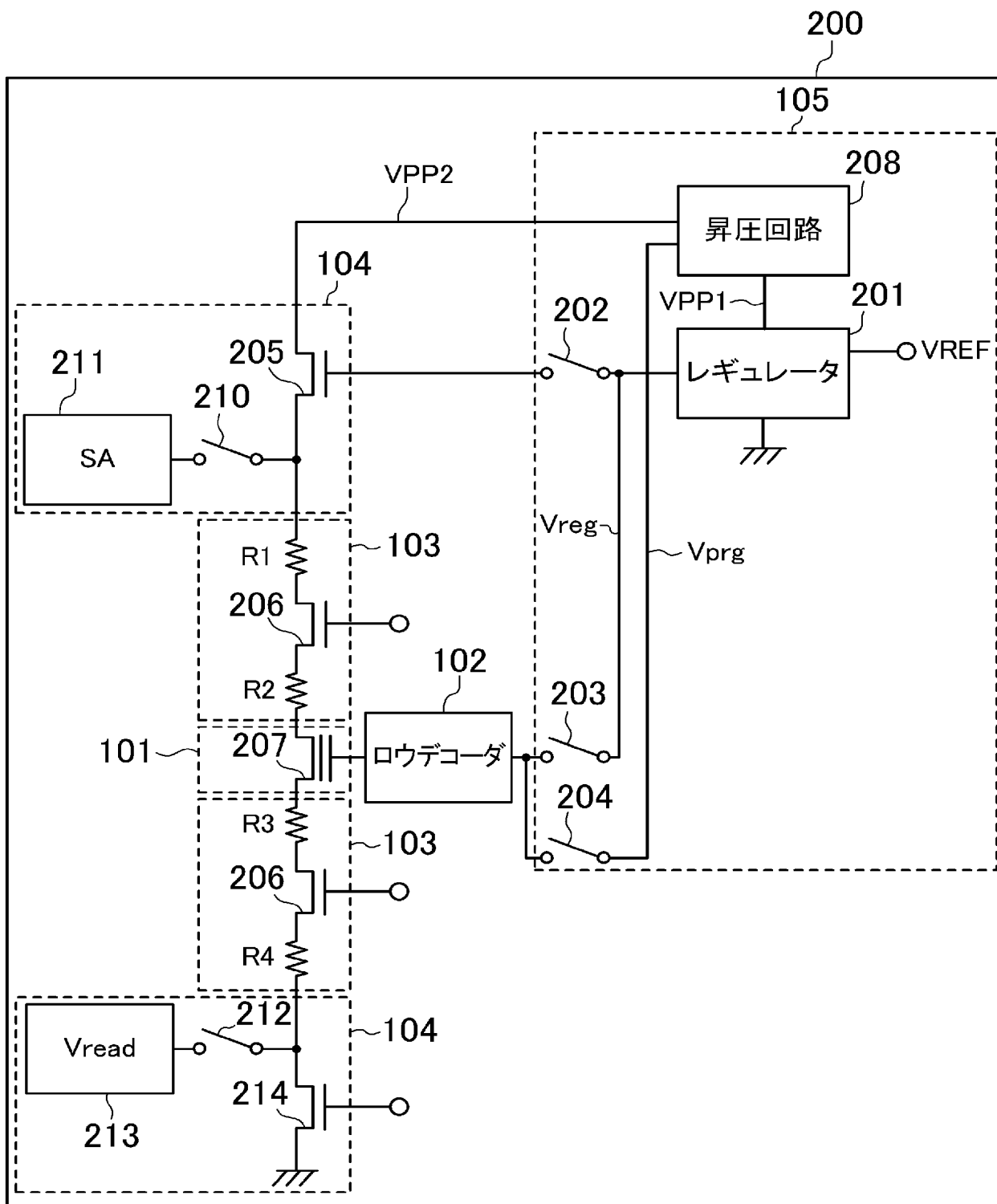
【図 3】



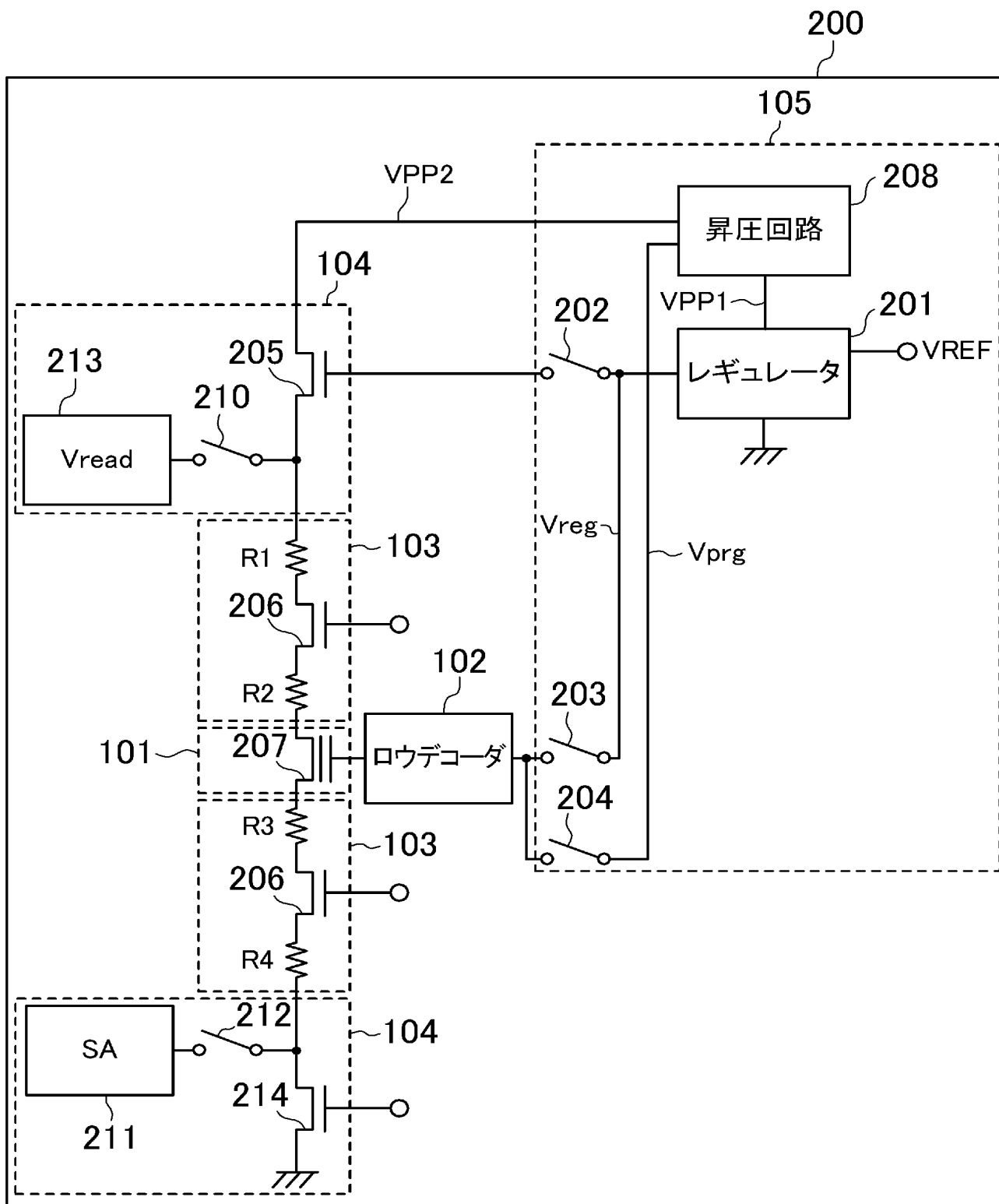
【図 4】



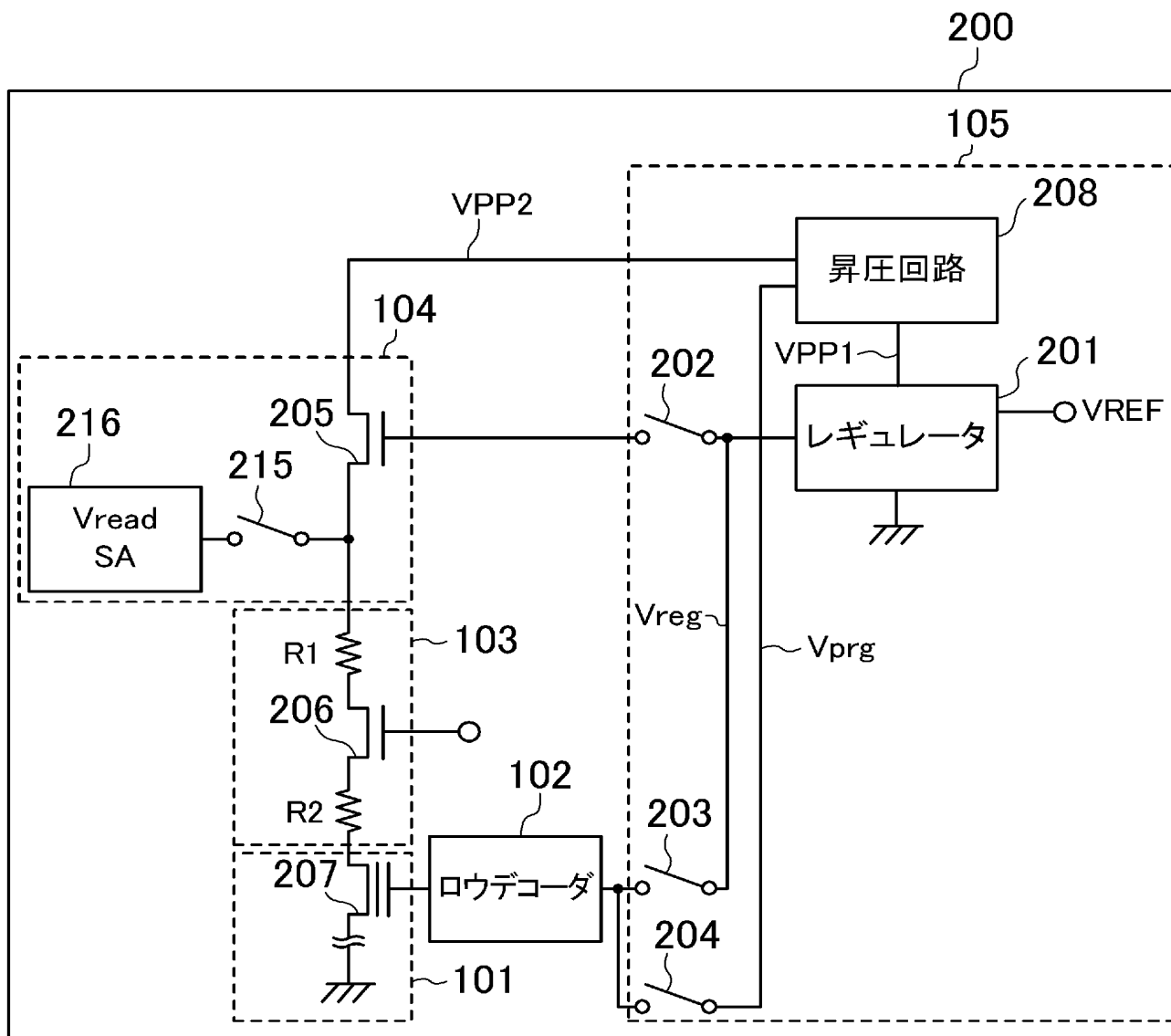
【図 5】



【図 6】



【图 7】



出願人履歴

0 0 0 0 0 5 8 2 1

20081001

名称変更

5 0 6 1 7 8 4 4 9

大阪府門真市大字門真 1 0 0 6 番地

パナソニック株式会社



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824

CONFIRMATION NO. 2466

PUBLICATION NOTICE



OC00000058142131

53080
MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Title:SEMICONDUCTOR MEMORY DEVICE

Publication No.US-2012-0314515-A1

Publication Date:12/13/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 09/17/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER

HOANG, HUAN

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 09/17/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/591,766

08/22/2012

Reiji MOCHIDA

085393-0824

2466

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	12/17/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

53080 7590 09/17/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824	2466

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	12/17/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-189090

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 1 _____ 2 _____ 3 _____
---	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted: ☐ Issue Fee ☐ Publication Fee (No small entity discount permitted) ☐ Advance Order - # of Copies _____	4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above) ☐ A check is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
---	--

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824	2466

53080 7590 09/17/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

EXAMINER

HOANG, HUAN

ART UNIT	PAPER NUMBER
----------	--------------

2827

DATE MAILED: 09/17/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/591,766	Applicant(s) MOCHIDA ET AL.	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-21. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| 1. ☒ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>08/22/1</u> | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/Huan Hoang/
Primary Examiner, Art Unit 2827

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Regarding claim 1: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation "wherein an output of the regulator is coupled to inputs of the first and second switches, an output of the first switch is coupled to a gate of the voltage applying transistor, a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and an output of the second switch is coupled to a gate of the memory cell for application of a voltage" in combination with the other limitations thereof as is recited in the claim. Claims 3, 5, 7, 9, 11, 13, 15, 17 and 19-21 depend on claim 1.

Regarding claim 2: The prior art made of record and considered pertinent to the applicant's disclosure does not teach the claimed limitation of "wherein an output of the regulator is coupled to an input of the second switch and a gate of the voltage applying transistor, a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell via the third switch, and an output of the second switch is coupled to a gate of the memory cell for application of a voltage" in combination with the other limitations thereof as is recited in the claim. Claims 4, 6, 8, 10, 12, 14, 16 and 18 depend on claim 2.

Therefore, the application is in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

Art Unit: 2827

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Huan Hoang/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 13/591,766		Applicant(s)/Patent Under Reexamination MOCHIDA ET AL.	
	Examiner HUAN HOANG		Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,428,170	09-2008	Lee, Doo-Sub	365/185.19
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	187015	(memory or stor\$4) and (cell or element) with regulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:25
S2	10579	(memory or stor\$4) and (cell or element) with regulat\$3 with (switch\$3 or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:26
S3	2125	S2 and (switch\$3 or transistor) with gate with (cell or element)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:26
S4	791	S3 and regulat\$3 with input\$3 with (switch\$3 or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:27
S5	791	S4 and (switch\$3 or transistor) with gate	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:28
S6	115	S5 and eras\$3 with (program\$4 or writ\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 15:29
S7	146	S5 and "365"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 16:18
S8	67	S7 not S6	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/08 16:18
S9	187015	(memory or stor\$4) and (cell or element) with regulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:12
S10	195396	(memory or stor\$4) and (cell or element) with (regulat\$3 or constant adj (voltage or potential))	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:13
S11	7054	S10 and (switch\$3 or transistor) with gate with (cell or element)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:17
S12	3218	S11 and (switch\$3 or transistor) with (output\$4 or input\$4) with gate with transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:19
S13	2747	S11 and (switch\$3 or transistor) with output\$4 with gate with transistor	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:19
S14	1777	S13 and drain with (cell or element)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:20
S15	587	S14 and eras\$3 and (writ\$3 or program\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:20
S16	378	S14 and eras\$3 and (writ\$3 or	US-PGPUB;	OR	ON	2013/09/09

		program\$4) and (boost\$3 or pump\$3)	USPAT; EPO; JPO; DERWENT			07:21
S17	318	S14 and eras\$3 and (writ\$3 or program\$4) and (boost\$3 or pump\$3) and amplifi\$7	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:22
S18	241	S17 and "365"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2013/09/09 07:24

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(memory and cell and regulator and switches and apply\$4 and transistor and input and output and drain and terminal and eras\$3 and writ\$3).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/09/09 08:43

9/ 9/ 2013 8:45:23 AM
C:\ Users\ hhoang1\ Documents\ EAST\ Workspaces\ 13519766.wsp

Search Notes 	Application/Control No. 13591766	Applicant(s)/Patent Under Reexamination MOCHIDA ET AL.
	Examiner HUAN HOANG	Art Unit 2827

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

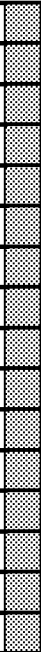
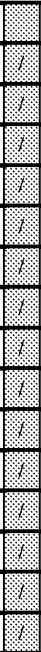
US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	189.09, 185.18	9/9/13	HH

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (text search)	9/9/13	HH
Inventor search	9/9/13	HH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	EAST (US-PGPUB, UPAD)	9/9/13	HH

	/HUAN HOANG/ Primary Examiner.Art Unit 2827
--	--

Issue Classification 	Application/Control No. 13591766	Applicant(s)/Patent Under Reexamination MOCHIDA ET AL.	
	Examiner HUAN HOANG	Art Unit 2827	

CPC			
Symbol		Type	Version
			

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version
						
						

NONE		Total Claims Allowed:	
(Assistant Examiner)		21	
(Date)			
/HUAN HOANG/ Primary Examiner.Art Unit 2827	09/09/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification 	Application/Control No. 13591766	Applicant(s)/Patent Under Reexamination MOCHIDA ET AL.
	Examiner HUAN HOANG	Art Unit 2827

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4		20												
	5		21												
	6														
	7														
	8														
	9														
	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE	Total Claims Allowed: 21	
(Assistant Examiner)	(Date)	
/HUAN HOANG/ Primary Examiner.Art Unit 2827	09/09/2013	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 2



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 2466

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/591,766	08/22/2012	365	2827	085393-0824		
RULE						
APPLICANTS Reiji MOCHIDA, Osaka, JAPAN; Takafumi Maruyama, Osaka, JAPAN; Yukimasa Hamamoto, Kyoto, JAPAN; ** CONTINUING DATA ***** This application is a CON of PCT/JP2010/007402 12/21/2010 ** FOREIGN APPLICATIONS ***** JAPAN 2010-052722 03/10/2010 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/30/2012						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /HUAN HOANG/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 5	TOTAL CLAIMS 21	INDEPENDENT CLAIMS 2
ADDRESS McDermott Will and Emery LLP The McDermott Building 500 North Capitol Street, N.W. WASHINGTON, DC 20001 UNITED STATES						
TITLE SEMICONDUCTOR MEMORY DEVICE						
FILING FEE RECEIVED 1310	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Docket No.: 085393-0824
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Reiji MOCHIDA et al.

Customer Number: 53080

Application No.: Not Yet Assigned

Confirmation No.: N/A

Filed: August 22, 2012

Art Unit: N/A

For: SEMICONDUCTOR MEMORY DEVICE

Examiner: Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement accompanies the new patent application submitted herewith.

A summary/abstract translation of the non-English language reference is enclosed.

Docket No.: 085393-0824

Applicant submits herewith copies of foreign patents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

A concise explanation of relevance of the items listed on form PTO/SB/08 is (1) given and (2) in the form of an English language copy of a Search Report from a foreign patent office, issued in a counterpart application, which refers to the relevant portions of the references.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists. In accordance with 37 CFR 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that any patent, publication or other information referred to therein is "prior art" for this invention unless specifically designated as such.

It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

Docket No.: 085393-0824

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington DC, DC 20005-3096
Phone: (202) 756-8372 MEF:mjb
Facsimile: (202) 756-8087
Date: August 22, 2012

**Please recognize our Customer No. 53080 as
our correspondence address.**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Examiner Signature	/Huan Hoang/	Date Considered	09/09/2013
--------------------	--------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language translation is attached.

PTO/SB/08b (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	Not Yet Assigned
				Filing Date	August 22, 2012
				First Named Inventor	Reiji MOCHIDA
				Art Unit	N/A
				Examiner Name	Not Yet Assigned
Sheet	2	of	2	Attorney Docket Number	085393-0824

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	CA	International Search Report issued in International Patent Application No. PCT/JP2010/007402 dated March 22, 2011		

Examiner Signature	/Huan Hoang/	Date Considered	09/09/2013
-----------------------	--------------	--------------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

53080 7590 09/17/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824	2466

TITLE OF INVENTION: SEMICONDUCTOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	12/17/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-189090

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 McDermott Will & Emery LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Panasonic Corporation

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 50-0417 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Michael E. Fogarty/

Date October 24, 2013

Typed or printed name Michael E. Fogarty

Registration No. 36,139

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	13591766			
Filing Date:	22-Aug-2012			
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE			
First Named Inventor/Applicant Name:	Reiji MOCHIDA			
Filer:	Michael E. Fogarty/Doris Barnes			
Attorney Docket Number:	085393-0824			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2080

Electronic Acknowledgement Receipt

EFS ID:	17222029
Application Number:	13591766
International Application Number:	
Confirmation Number:	2466
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Reiji MOCHIDA
Customer Number:	53080
Filer:	Michael E. Fogarty/Doris Barnes
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0824
Receipt Date:	24-OCT-2013
Filing Date:	22-AUG-2012
Time Stamp:	17:45:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 2080
RAM confirmation Number	4985
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P602416-01_FEE_085393-0824.pdf	111863 2472fba42938f36f22c2f1e8b947e4be8b8ea974	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32060 795f641d4fec455d926dbc1c4a99935e67114711	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			143923		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/591,766	11/26/2013	8593888	085393-0824	2466

53080 7590 11/06/2013
McDermott Will and Emery LLP
The McDermott Building
500 North Capitol Street, N.W.
WASHINGTON, DC 20001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Reiji MOCHIDA, Osaka, JAPAN;
Takafumi Maruyama, Osaka, JAPAN;
Yukimasa Hamamoto, Kyoto, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	8593888
	Issue Date	November 26, 2013
	First Named Inventor	Reiji MOCHIDA
	Title	SEMICONDUCTOR MEMORY DEVICE
	Attorney Docket No.	0870-04135 US

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

27197

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

Country

Telephone

State

Zip

Email

I am the:

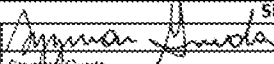
☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature		Date	December 26, 2024
Name	Reiji Mochida	Telephone	
Title and Company	Authorized Signatory, ADVANCED MEMORY TECHNOLOGIES LLC		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: ADVANCED MEMORY TECHNOLOGIES LLCApplication No./Patent No.: 8593888Filed/Issue Date: November 26, 2013Titled: SEMICONDUCTOR MEMORY DEVICEADVANCED MEMORY TECHNOLOGIES LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: the inventor(s) To: PANASONIC CORPORATION

The document was recorded in the United States Patent and Trademark Office at

Reel 029440, Frame 0826, or for which a copy thereof is attached.2. From: PANASONIC CORPORATION To: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD.

The document was recorded in the United States Patent and Trademark Office at

Reel 053570, Frame 0429, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SK hynix Ex. 1002, Page 139 of 145

STATEMENT UNDER 37 CFR 3.73(c)

3. From: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD. To: NUVOTON TECHNOLOGY CORPORATION JAPAN

The document was recorded in the United States Patent and Trademark Office at
Reel 066849, Frame 0802, or for which a copy thereof is attached.

4. From: NUVOTON TECHNOLOGY CORPORATION JAPAN To: ADVANCED MEMORY TECHNOLOGIES LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 067184, Frame 0869, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/

Signature

Szymon M. Gurda

Printed or Typed Name

December 30, 2024

Date

58451

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
13/591,766

RECEIPT DATE / TIME
12/30/2024 10:48:56 PM Z ET

ATTORNEY DOCKET #
085393-0824

Title of Invention

SEMICONDUCTOR MEMORY DEVICE

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 8593888

CONFIRMATION # 2466

FILED BY Yi Lu

PATENT CENTER # 68561272

FILING DATE 08/22/2012

CUSTOMER # 53080

FIRST NAMED
INVENTOR Reiji MOCHIDA

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA.pdf	2	Power of Attorney	1153 KB
aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	120 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA.pdf	4B5DA4D2DDFFBB53A9F5BC96247E952E48264BF3226708B73 82FE36CD9240A18D0740588DFD38B91ECEB0A5DC5059CF43 153794040A16F851C7A0ECF9812941B
aia0096.pdf	856F5EC97D6525388A7B9F8C7289F7829429BF80561FD32203 74A7CCB6DB317920AECF0BDE63BD9E886D1B4750ACEF717

D489C8A1E8C79FD02953B629657926D

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824

CONFIRMATION NO. 2466

POA ACCEPTANCE LETTER



OC000000082995359

27197
MICHAEL J. CHERSKOV
SZYMON M. GURDA
903 COMMERCE DR
SUITE 310
OAK BROOK, IL 60523

Date Mailed: 01/15/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/591,766	08/22/2012	Reiji MOCHIDA	085393-0824

CONFIRMATION NO. 2466

53080
Rimon PC - Panasonic Corporation
8300 Greensboro Dr.
Suite 500
McLean, VA 22102

POWER OF ATTORNEY NOTICE



OC000000082995305

Date Mailed: 01/15/2025

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/