

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC.,

Petitioner,

v.

ADVANCED MEMORY TECHNOLOGIES, LLC,

Patent Owner.

Case No. IPR2025-01449

U.S. Patent No. 8,593,888

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,593,888**

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EXHIBIT LIST

Ex.	Description
EX-1001	U.S. Patent No. 8,593,888 (“’888 Patent”)
EX-1002	Prosecution History for U.S. Pat. No. 8,593,888
EX-1003	Declaration of Sunil Khatri, Ph.D.
EX-1004	Curriculum Vitae of Dr. Sunil Khatri
EX-1005	U.S. Pat. No. 5,907,505 (“Tomita”)
EX-1006	U.S. Pat. No. 7,372,747 (“Nam”)
EX-1007	T. Nakayama et al., (Aug. 1989), <i>A 5-V-Only One-Transistor 256K EEPROM with Page-Mode Erase</i> , IEEE Journal of Solid-State Circuits, Vol. 24, No. 4 (“Nakayama”)
EX-1008	Japanese Pat. Appl. Pub. No. JP 2008-217914 (“Nakauchi”)
EX-1009	Certified Translation of Nakauchi
EX-1010	U.S. Pat. No. 8,116,132 (“Im”)
EX-1011	[reserved]
EX-1012	U.S. Patent Appl. Pub. No. 2006/0055452A1 (“Tanzawa”)
EX-1013	L. Guo, <i>Design And Implementation Of Digital Controllers For Buck And Boost Converters Using Linear And Nonlinear Control Methods</i> , Dissertation (2006), available at https://auetd.auburn.edu/bitstream/handle/10415/1323/GUO_LIPING_41.pdf (“Guo”)
EX-1014	Application Note 2031, <i>DC-DC Converter Tutorial</i> , Maxim Integrated (Nov. 29, 2001), available at https://www.analog.com/media/en/technical-documentation/tech-articles/dc-to-dc-buck-converter-tutorial--diagram--maxim-integrated.pdf (“Analog”)
EX-1015	U.S. Pat. App. Pub. No. 2004/0004851A1 (“Itoh”)

Petition for *Inter Partes* Review
U.S. Patent No. 8,593,888

EX-1016	Texas Instruments, LM2750 Low-Noise Switched-Capacitor Boost Regulator
EX-1017	U.S. Pat. No. 7,512,010 (“Cho”)
EX-1018	U.S. Pat. No. 6,842,383 (“Shor”)
EX-1019	U.S. Pat. Appl. Pub. No. 2005/0232013 (“Kawai”)
EX-1020	U.S. Pat. Appl. Pub. No. 2010/0332858 (“Trantham”)
EX-1021	U.S. Pat. Appl. Pub. No. 2010/0205348 (“Moshayedi”)
EX-1022	U.S. Pat. Appl. Pub. No. 2008/0158915 (“Williams”)
EX-1023	J. Alberkrack, <i>Theory and Applications of the MC34063 and $\mu A78S40$ Switching Regulator Control Circuits</i> , Motorola Semiconductor Application Note AN920 Rev. 2 (1989) (“Alberkrack”)

LIST OF CHALLENGED CLAIMS

Claim	Limitation
1[pre]	A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:
1[a]	the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein
1[b]	an output of the regulator is coupled to inputs of the first and second switches,
1[c]	an output of the first switch is coupled to a gate of the voltage applying transistor,
1[d]	a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and
1[e]	an output of the second switch is coupled to a gate of the memory cell for application of a voltage.
3[pre]	The semiconductor memory device of claim 1, wherein
3[a]	an output of a fourth switch is coupled to the output of the second switch, and
3[b]	a voltage different from the output of the regulator is applied to the gate of the memory cell.
5[pre]	The semiconductor memory device of claim 3, wherein
5[a][i]	in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and
5[a][ii]	the voltage different from the output of the regulator to be applied to the gate of the memory cell, and
5[b]	in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

Claim	Limitation
20[pre]	The semiconductor memory device of claim 3, wherein
20[a]	the voltage different from the output of the regulator is an output voltage of a booster circuit.
21[pre]	The semiconductor memory device of claim 1, wherein
21[a]	an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

I. RELIEF REQUESTED

Petitioner requests inter partes review of U.S. Patent No. 8,593,888 (the “’888 Patent”) and cancellation of claims 1, 3, 5, 20, and 21 under the following Grounds:

Ground	Basis	Reference(s)	Claims
1	§102	Tomita	1 and 21
2	§103	Tomita in view of Im	1, 3, 5, 20, and 21
3	§103	Tomita in view of Nam	1, 3, 5, and 21
4	§102	Nakayama	1, 3, 5, and 21

Each reference applied in this Petition predates March 10, 2010 (“Critical Date”), which is the earliest filed foreign application from which the ’888 Patent claims priority. Petitioner does not necessarily agree that the ’888 Patent is entitled to priority to this Critical Date.

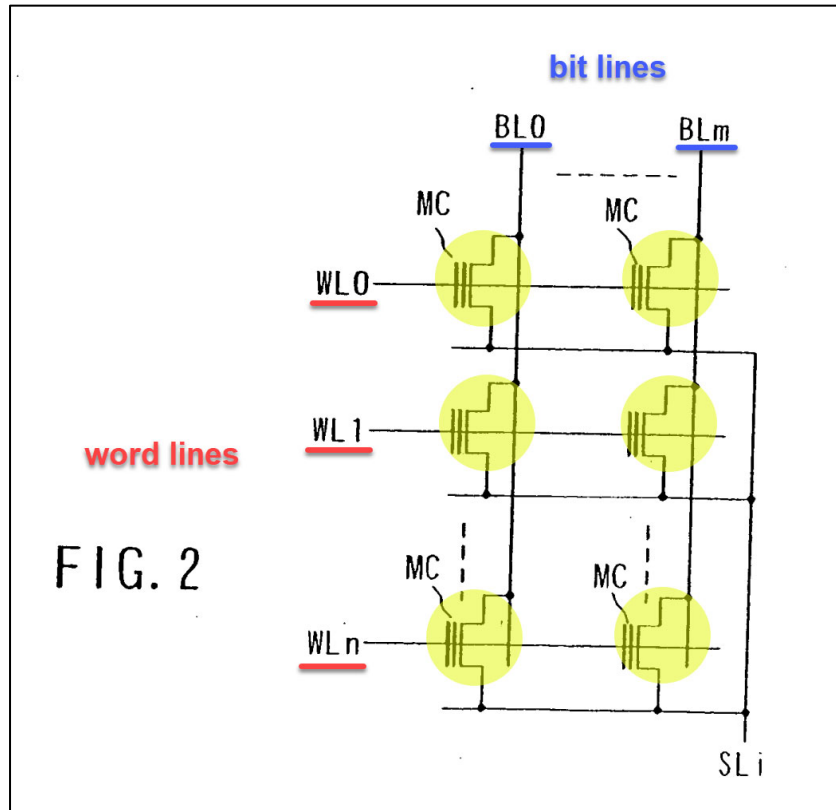
Reference	Date	Pre-AIA Section
Tomita	May 25, 1999 (issue date)	§§102(a), 102(b)
Im	January 5, 2009 (filing date)	§102(e)
Nam	May 13, 2008 (issue date)	§§102(a), 102(b)
Nakayama	Aug. 1989 (publication date)	§§102(a), 102(b)

II. TECHNOLOGY BACKGROUND

A. Memory Cells and Voltage Applying Transistor

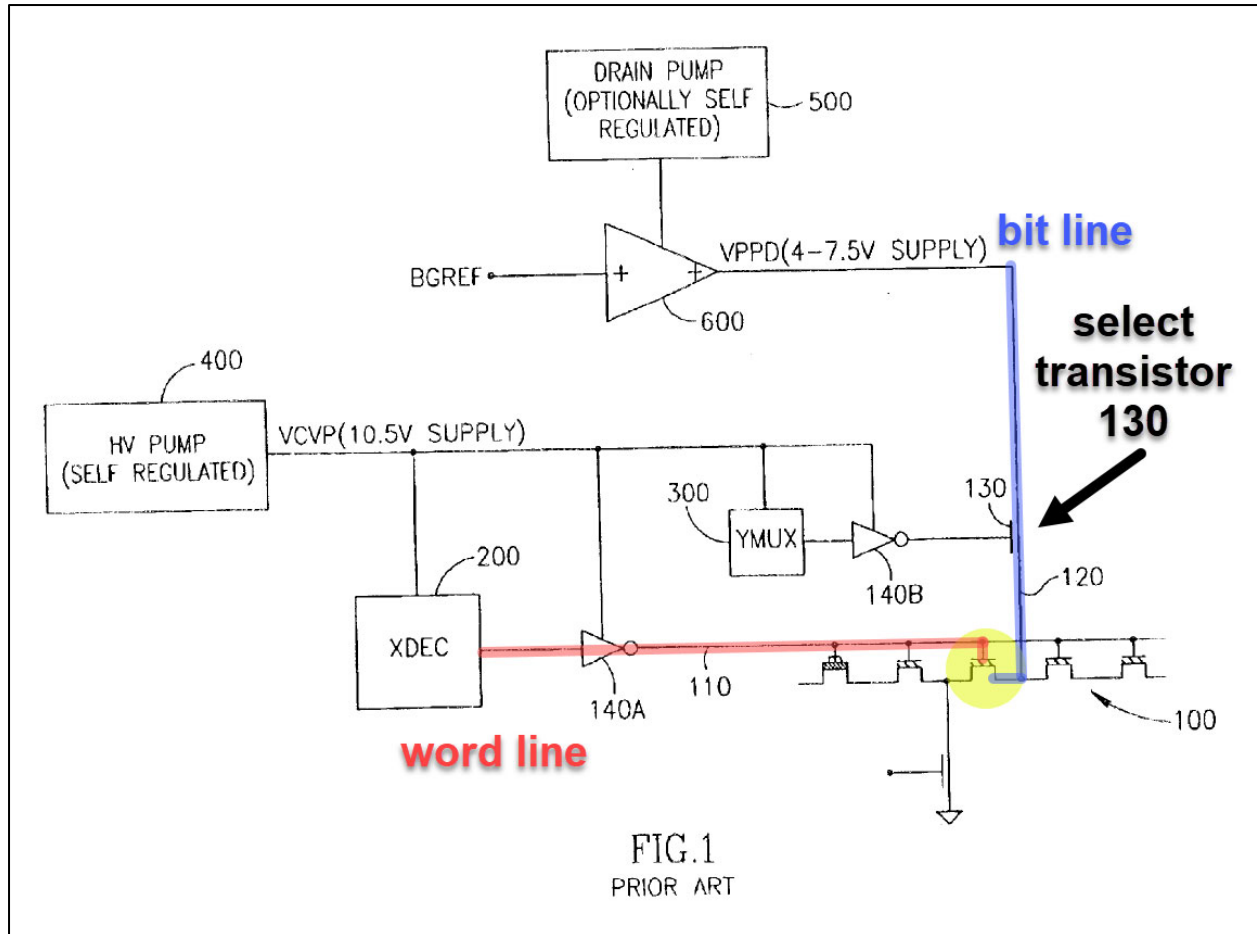
A memory cell (MC) can store data as either “0” or “1.” EX-1012, [0006]; EX-1003, ¶40. Memory cells are usually arranged in an array of rows and columns, with each memory cell situated at the intersection of a word line (WL) and a bit line (BL). EX-1012, [0007], Fig. 2; EX-1017, 4:48-52; EX-1018, 1:53-58; EX-1003, ¶40. As illustrated below, the **gate terminals** of memory cells MC (highlighted yellow) in the same row are all connected to one of the **word lines** WL0, WL1, ...

WLn, and the **drain terminals** of memory cells in the same column are all connected to one of the **bit lines** BL0, ... BLm. EX-1012, [0007], Fig. 2; EX-1018, 1:55-59; EX-1003, ¶40.¹

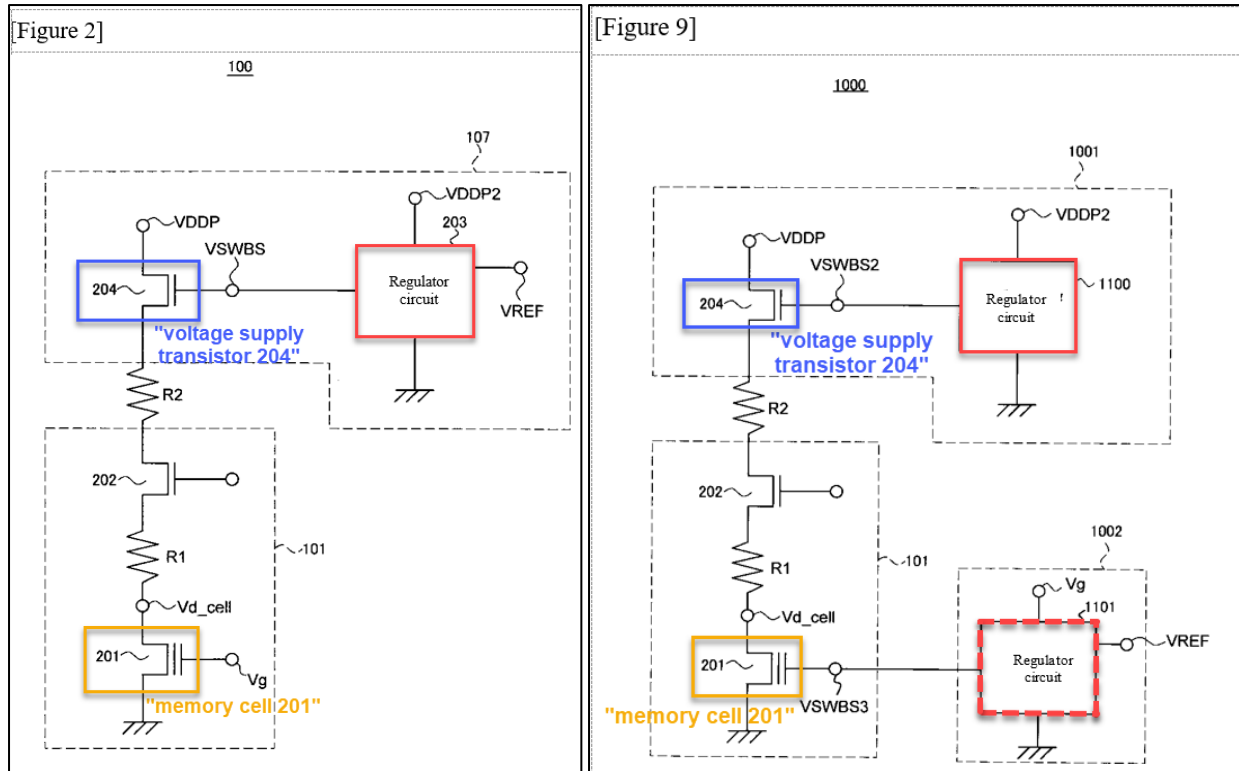


Memory operations such as read, write (program), or erase can be performed on a subset of the memory cells at a given time. EX-1003, ¶41. Specific subsets of memory cells from the array can be chosen for a given memory operation by addressing the respective word line and bit lines corresponding to the subset of cells. *Id.* The bit line may be controlled by a select transistor, connected in series with the source terminal of the memory cell(s). EX-1018, Fig. 1 (below), 2:7-14.

¹ All annotations are added unless indicated otherwise.



The '888 Patent acknowledges that memory devices with memory cells that can be “erased and rewritten” and voltage applying transistors were known in the art. EX-1001, 1:15-21 (background); EX-1003, ¶43. The '888 Patent specifically identified a prior art, Japanese Patent Publication No. 2008-217914 (“Nakauchi”). EX-1008, 1; EX-1009 (certified English translation of Nakauchi). Nakauchi discloses “a NOR-type flash memory device 100,” which includes “a plurality of **memory cells 201**,” “a plurality of **voltage supply transistors 204**,” and a “**regulator circuit 203**.” EX-1009, [0018], Fig. 2, Fig. 9.



B. Supply Voltages for A Memory Cell (Wordline Voltages)

Memory cells are controlled by different levels of **gate voltages**, depending on the memory operation required (*e.g.*, read, verify, write/program, erase). EX-1003, ¶46; EX-1018, 1:14-21; EX-1012, [0016]-[0017]. In general, a high voltage is required for programming or erasing data from the memory cell. EX-1017, 1:19-37. The voltage applied to the gate terminal of the memory cell is also known as the **word line voltage**. EX-1003, ¶46; EX-1018, 1:55-57. Additional voltages are applied to the drain or source terminal of the memory cell (bit line voltage) or to the select transistor. EX-1003, ¶46.

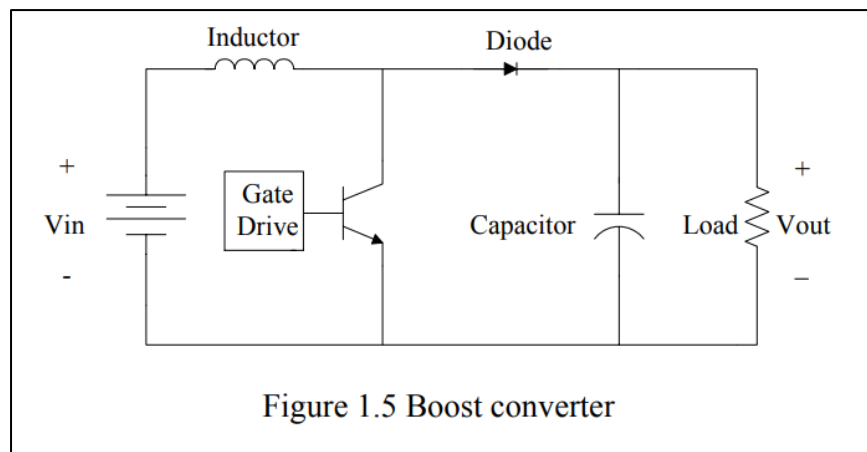
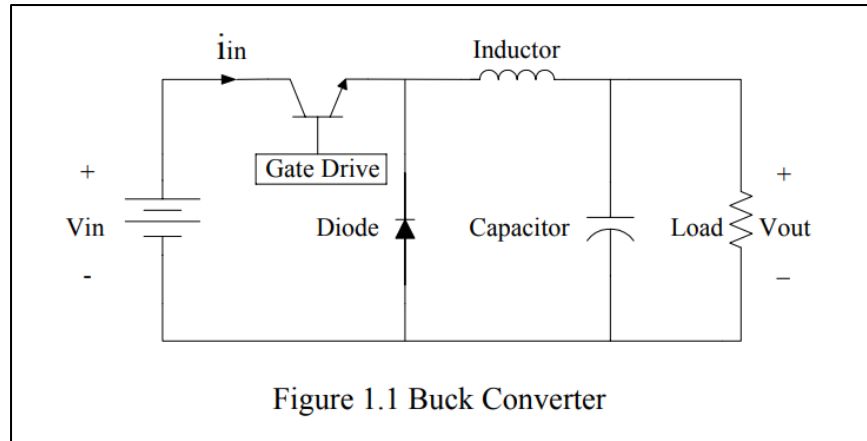
The voltage at the gate terminal of the memory cell is typically driven by a row decoder, which selects a particular row (*i.e.*, word line) based on a memory

address provided. EX-1003, ¶47; EX-1018, Fig. 1; EX-1012, Fig. 16, [0111]; EX-1017, Fig. 2, 4:45-48; EX-1009, Fig. 1. The foregoing general structure for powering various components of the memory cell array was ubiquitous before the Critical Date. EX-1003, ¶47.

C. Voltage Regulator

To supply different voltage levels during different memory operations (*e.g.*, write/program, erase, read, verify), memory devices include one or more DC-to-DC voltage regulators. EX-1003, ¶48. A voltage regulator receives an input voltage and “regulates” it to an output voltage of a desired level. *Id.*

There are different types of regulators. EX-1003, ¶49. For example, step-down or “buck” regulators output a reduced DC voltage compared to the input DC voltage, and step-up or “boost” regulators output a DC voltage higher than the input DC voltage. EX-1022, [0004]; EX-1020, [0029]; EX-1021, [0061]; EX-1023, 2. Exemplary buck converter and boost converter are illustrated below:



EX-1013, 2-5

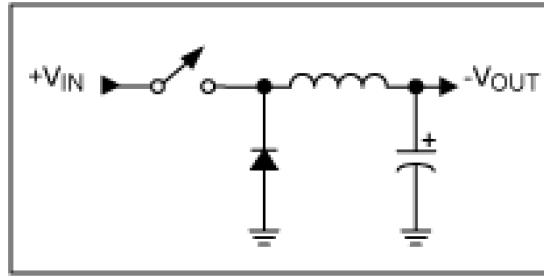


Figure 1. Buck converter topology.

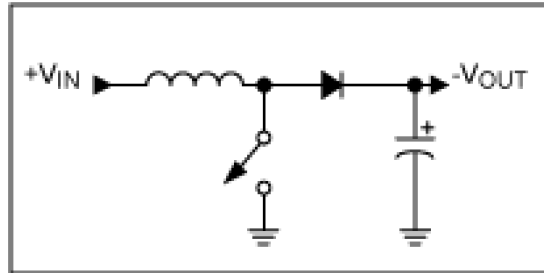


Figure 2. Simple boost converter.

EX-1014, Figs. 1-2

Despite the different voltage levels required by the word line, the bit line, and the select transistor, it is often desired, for efficiency, that the same regulator be used to supply various voltages to them all. EX-1018, 2:53-61 (seeking to “reduce the number of charge pumps required.”); EX-1003, ¶50.

A charge pump, which uses switches and capacitors to boost (or pump) an internal voltage, is a well-known type of a boost circuit. EX-1018, 2:16-22 (“High Voltage charge pump 400 may provide a regulated 10.5V” to the word line); EX-1017, 1:49-62 (“regulated voltage V_{reg_pump} has a stable waveform” and is obtained by “boosting a voltage up to the high voltage through the charge pumping operation”); EX-1003, ¶51. A charge pump is often used for its high efficiency. EX-

1022, [0068]-[0069]; EX-1016, §7.1; EX-1003, ¶51.

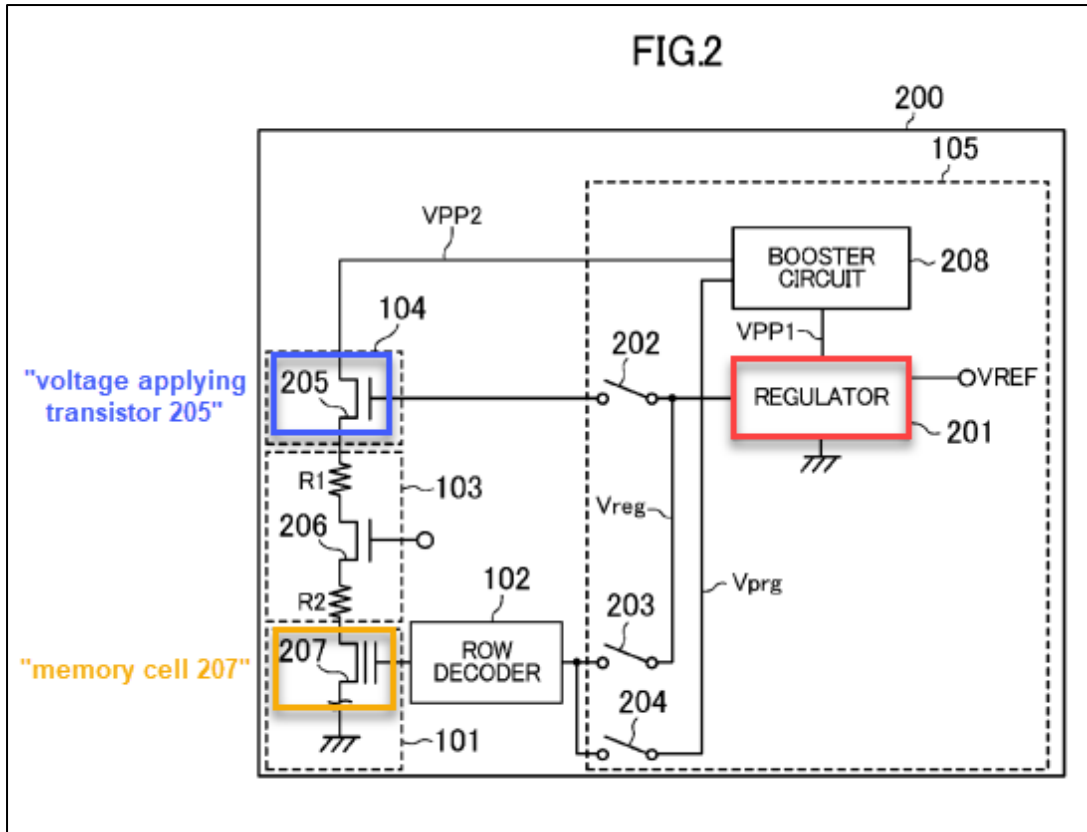
D. Switch Circuits

In memory devices, switch circuits are commonly used to select an appropriate voltage level to drive a particular row (*i.e.*, word line) or column (*i.e.*, bit line). EX-1003, ¶52-53. A switch circuit conventionally comprises one or more transistor switches, each of which is controlled by a voltage received at its gate such that, when the chosen transistor is turned “on,” it connects the electrical terminals of its drain and source. EX-1006, 4:23-36, Fig. 2; EX-1010, 6:29-36, Fig. 1; EX-1018, Fig. 2, 5:38-63.

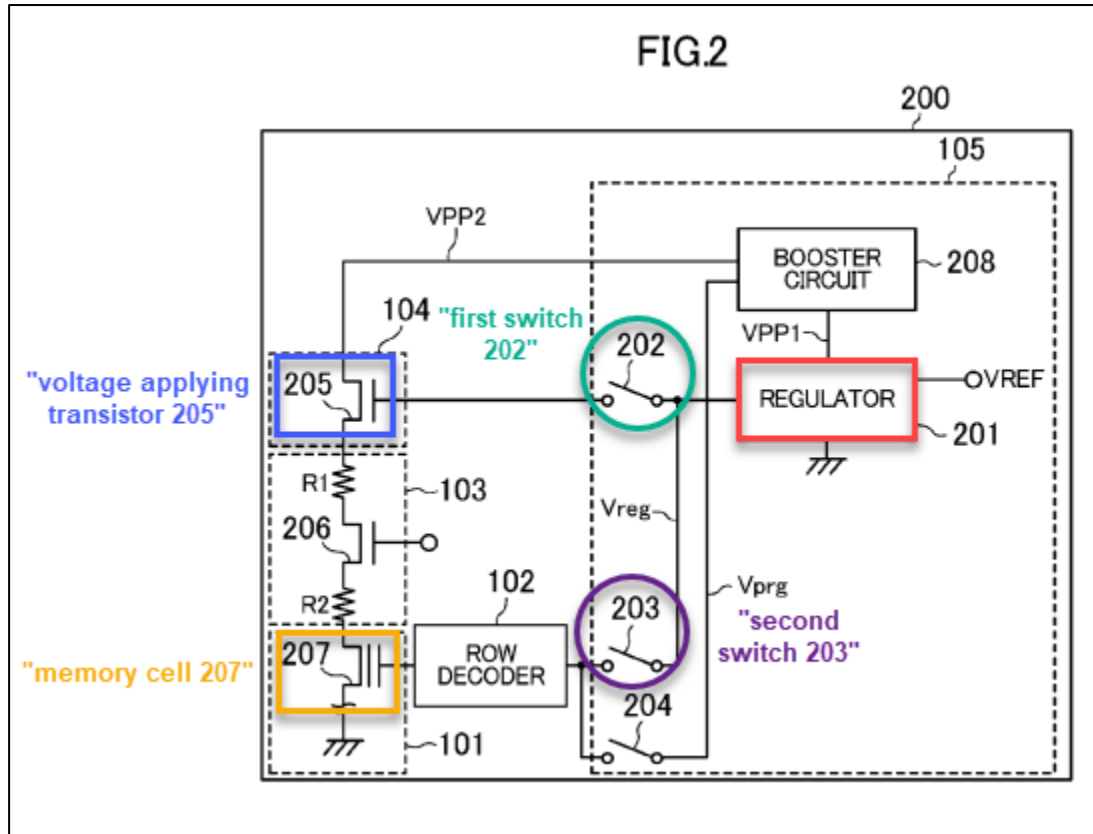
III. '888 PATENT

A. '888 Patent Specification (EX-1001)

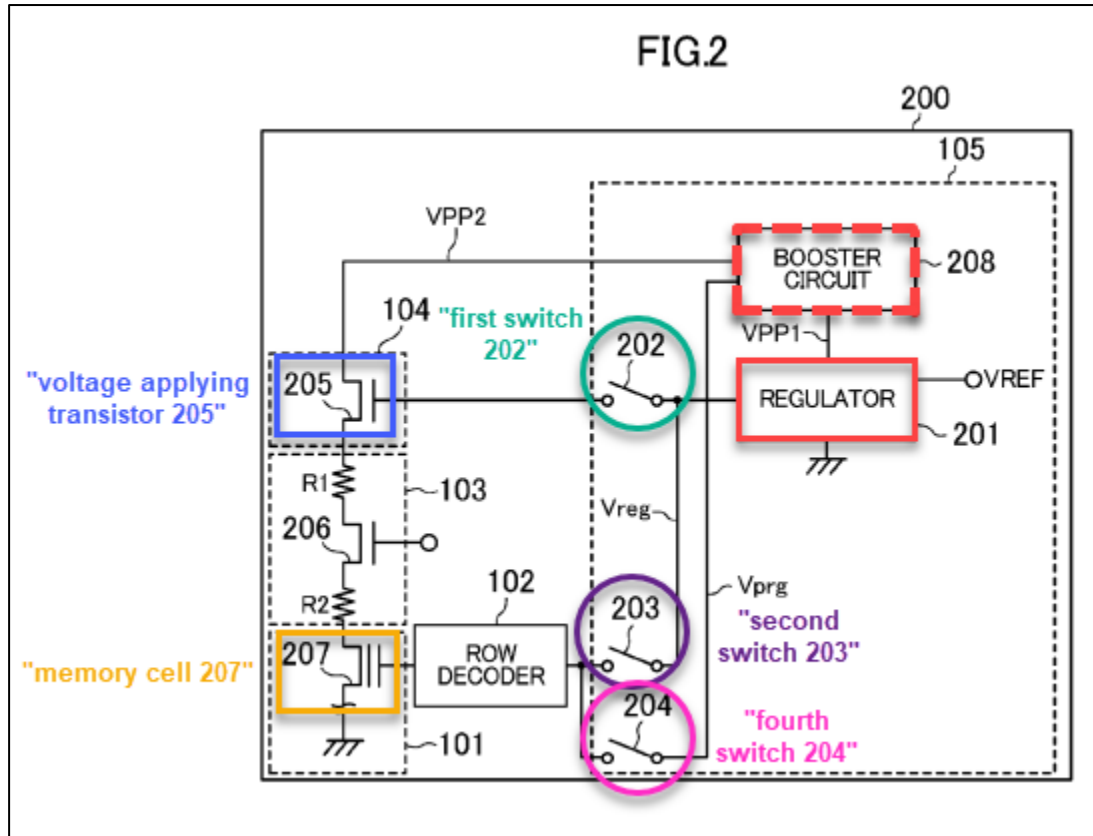
Building upon the foregoing disclosures in Figures 2 and 9 of Nakauchi, the '888 Patent proposes two minor adjustments. “A technique like this is described in Japanese Patent Publication No. 2008-217914 (FIG. 9)”, EX-1001, 1:28-30.



First, rather than using *two* regulators, the '888 Patent proposes using one regulator. EX-1001, 1:40-41. To supply the gate terminals of the **voltage applying transistor 205** and the **memory cell 207**, respectively, the '888 Patent describes using one “**regulator 201** [that] is coupled to the inputs of a **first switch 202** and a **second switch 203**” to supply *both* gate terminals. EX-1001, 6:19-21. “The output of the first switch 202 is coupled to the gate of the voltage applying transistor 205,” whereas “the output of the second switch 203 is coupled to the gate of the memory cell 207 via the row decoder 102.” *Id.*, 6:21-28.



Second, in addition to the first and second switches, the '888 Patent introduces a **fourth switch 204**, which is coupled to “the **booster circuit 208**” (shown in dotted red box below) and also coupled to the gate terminal of memory cell 207 via the row decoder 102. EX-1001, 6:30-34. The output ends of the second and fourth switches are tied together, as shown below, allowing either the output of the booster circuit 208 or the output of the regulator 201 to be supplied to the gate of memory cell 207.



Accordingly, one of ordinary skill in the art would have understood the alleged invention of the '888 Patent is the use of a *single regulator* and a booster circuit, along with the *first*, *second*, and *fourth* switches. EX-1003, ¶58.

B. Prosecution History (EX-1002)

The '888 Patent was allowed on the first office action. Regarding claims 1, 3, 5, 20, and 21 that are relevant to this petition, the Examiner cited claim limitations 1[b] through 1[d] as the stated reasons for allowance. EX-1002 at 127. These claim limitations generally recite the use of a regulator and the arrangement of switches between the regulator on the one hand, and the voltage applying transistor and memory cell on the other hand. EX-1003, ¶59.

IV. PERSON OF ORDINARY SKILL

A person of ordinary skill in the art at the time of the '888 Patent ("POSITA") would have at least a Bachelor of Science in electrical engineering, computer engineering, or similar fields with courses in integrated circuit design and at least two years of experience in the field of integrated circuit design for memories. More education can supplement for less experience, and vice versa. EX-1003, ¶¶60. Petitioner's expert, Dr. Khatri, exceeded this level by the priority date. *Id.* ¶¶4-20, 61.

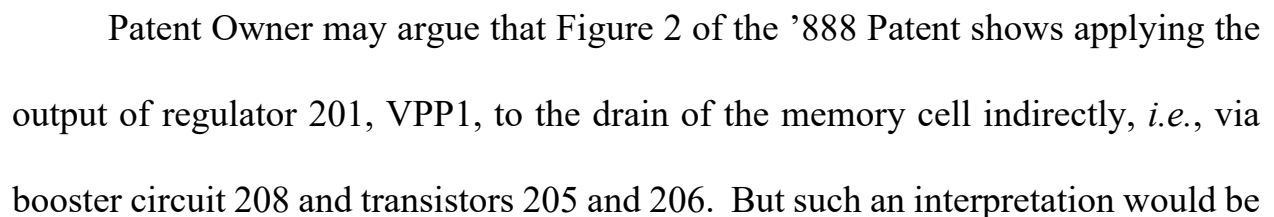
V. CLAIM CONSTRUCTION

Claim 5 of the '888 patent recites "in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the *drain terminal* of the *memory cell* and the voltage different from the output of the regulator to be applied to the gate of the memory cell." The term "the drain terminal of the memory cell" is an obvious drafting error and should be construed to mean "the *gate* of the *voltage applying transistor*." See *Novo Indus., L.P. v. Micro Molds Corp.*, 350 F.3d 1348, 1355 (Fed. Cir. 2003) (obvious errors in a claim can be corrected in construing the claim); *Amazon.com, Inc. v. Nokia Technologies Oy*, IPR2024-00921, Paper 11 at 11.

The claim language supports this interpretation. Claim 1, from which claim 5 depends, recites that "the regulator is coupled" to the "input[]" of the first ... switch,"

whose output is in turn “coupled to a *gate* of the *voltage applying transistor*.” As a result of this coupling, when the first switch is “turned on” in claim 5’s “first operation mode,” it allows the output voltage of the regulator to be applied to the *gate* of the *voltage applying transistor*. EX-1001, Fig. 2; EX-1003, ¶63. Neither claim 1 nor claim 5 provides any connection via which the regulator output in the first operation mode is applied to “the drain terminal of the memory cell,” let alone as a result of the first switch being “turned on,” as claim 5 recites.

The specification confirms this interpretation. Consistent with Petitioner’s construction and mirroring the remaining language of claim 5, the specification describes that, “in the first mode (*e.g.*, during write operation),” “the output of the regulator is supplied to the *gate* of the *voltage applying transistor*, to control the voltage applied to the drain side of the memory cell,” whereas in “the second mode (*e.g.*, during read operation)” the regulator output is “supplied to the gate of the *memory cell*.” EX-1001, 4:61-5:3, Fig. 2.



unsupported because the specification is plain that VPP1 is the output of booster circuit 208, not the output of regulator 201. EX-1001, 6:18-21. Further, if the applicant had intended to claim the booster circuit's voltage being applied to the drain of the memory cell (rather than the regulator's voltage being applied to the drain of the memory cell), claim 5 would have expressly stated so. EX-1003, ¶66. The '888 patent claims explicitly distinguish the output of a booster circuit ("**voltage different from** the output of the regulator") from the "output of a regulator." EX-1001, 9:35-36 ("an output of the regulator"), 9:61 ("a voltage different from the output of the regulator"), 13:5-7 ("the voltage different from the output of the regulator is an output voltage of a booster circuit"), 13:8-10 ("an output of a booster circuit is coupled to a source terminal of the voltage applying transistor"). Such a distinction would be rendered meaningless if the output of the booster circuit can also be considered an output of the regulator simply because the booster circuit is connected to the regulator. *See Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010) ("Claims must be interpreted with an eye toward giving effect to all terms in the claim.").

Accordingly, the Board should construe the first operation in claim 5 to require applying an output of the regulator to the "gate of the voltage applying transistor," not the "drain terminal of the memory cell." Should the Board agree, claim 5 (the only claim affected by this construction) is invalid as discussed in

Grounds 2 and 3. But even if the Board disagrees and finds no construction is needed for claim 5, it would still be invalid as discussed in Grounds 2 through 4.

No other express constructions are required to find the '888 Patent claims invalid. To the extent relevant, Petitioner addresses the plain meaning of certain terms in the analysis for the presented Grounds.

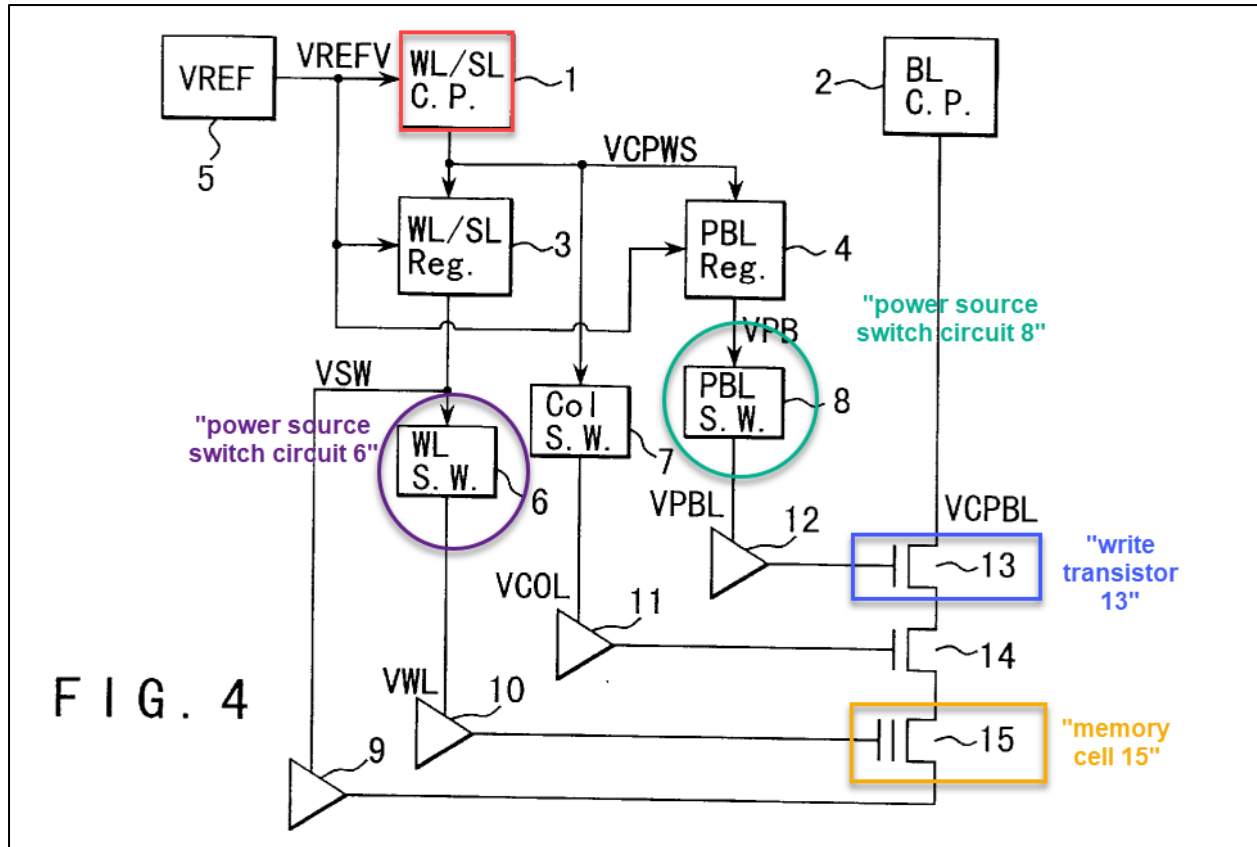
VI. GROUNDS

A. Ground 1: Tomita Anticipates Claims 1 and 21

1. Overview of Tomita (EX-1005)

Tomita is prior art under at least pre-AIA 35 U.S.C. §§102(a)-(b), having been patented on May 25, 1999, and thus before the Critical Date. Tomita was not considered by the Examiner during prosecution of the '888 Patent.

Tomita discloses “a power source circuit ... used for a non-volatile semiconductor memory.” EX-1005, 5:56-60. Ground 1 focuses on Tomita’s power source circuit shown in Figure 4:



Tomita Fig. 4

In the Figure 4 embodiment, Tomita's power source circuit includes **boost circuit WL/SL C.P. 1**, which receives a reference potential VREFV and provides an output potential VCPWS to stepdown circuits 3 and 4. EX-1005, 7:18-24. The stepdown circuit 3 supplies an output potential VSW to switch circuits **WL switch ("WL S.W.") 6**, while stepdown circuit 4 supplies an output potential VPB to **PBL switch ("PBL S.W.") 8**. *Id.*, 7:20-29, 7:46-53, 7:60-8:2. The output potential VCPWS of the boost circuit 1 is "directly used or is reduced" by the switches, depending on the intended operation (e.g., write, erase, verify, or read). *Id.*, 7:35-41, 7:54-59. The switches select from either the output of a stepdown circuit or an

external power source potential, VDD (not shown). *Id.*, 1:12-13, 1:50-52, 14:60-62.

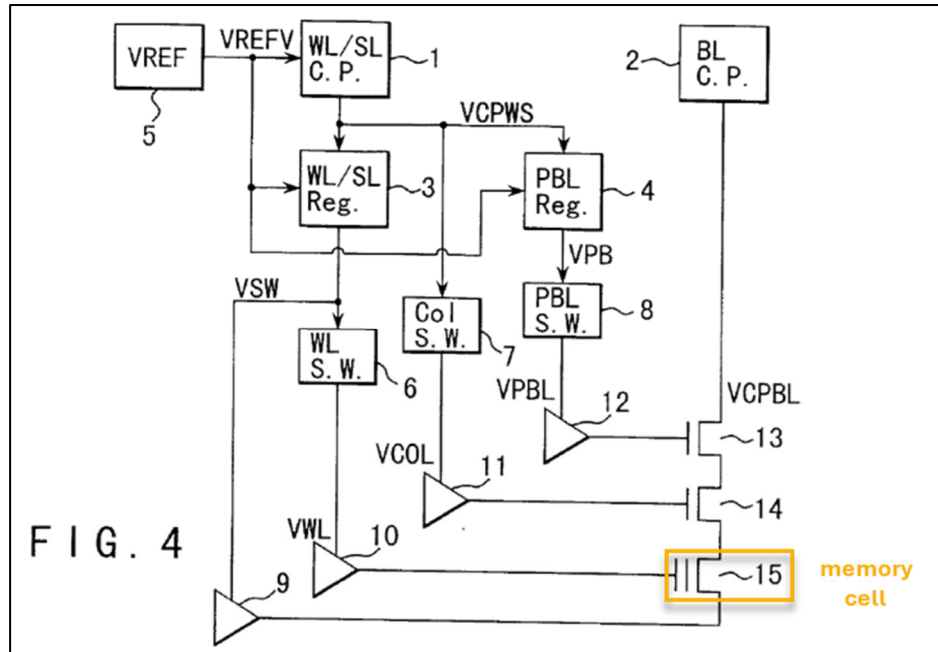
Switch circuit 6, for example, “selects and outputs” VSW or VDD depending on the state. *Id.* 8:12-21. The outputs of switches 6, 7, and 8 are coupled—via a row decoder 10, column decoder 11, and write transistor decoder 12—to a “**memory cell 15**,” a “column select transistor 14,” and a “**write transistor 13**,” respectively. *Id.*, 1:62-65, 2:20-22.

2. Analysis

(a) Claim 1

- (i) **1[pre]: A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:**

Tomita discloses 1[pre]. Tomita discloses a “non-volatile semiconductor memory” comprising a “power source circuit” that supplies potential for reading as well as “writing, erasing, and verifying data on the memory cell.” EX-1005, 5:56-60, 7:8-16, 7:30-34, 7:17-18.

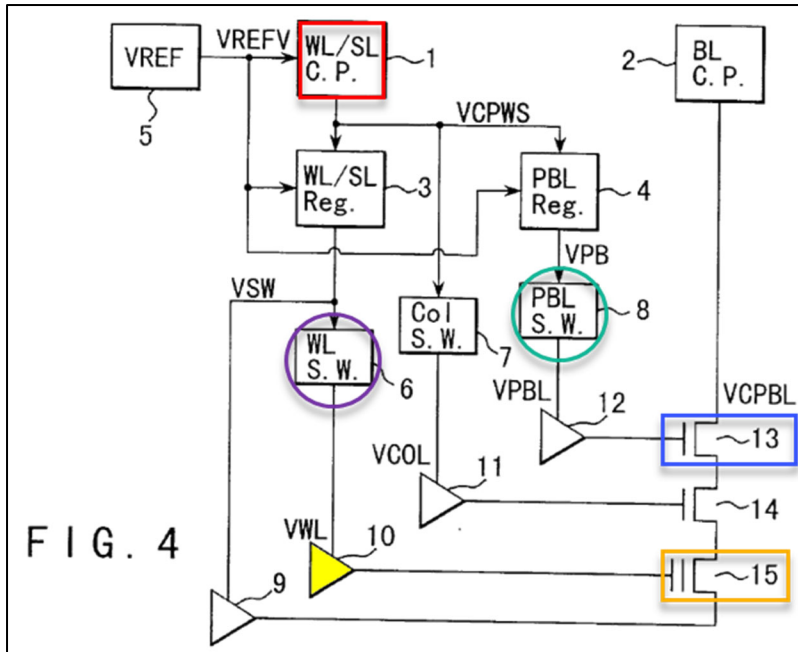


Tomita Fig. 4

Further, Tomita discloses that its invention relates to “flash memory, an EEPROM, or the like,” which is a memory device in which memory cells can be erased and rewritten. EX-1005, 1:5-7; EX-1001, 1:16-21; EX-1003, ¶75.

- (ii) 1[a]: the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein

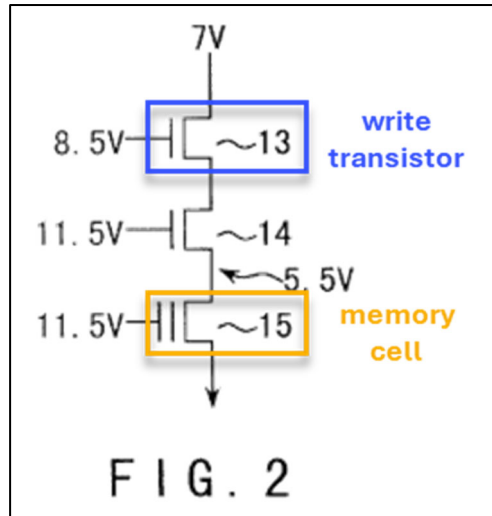
Tomita discloses 1[a]. Tomita discloses **memory cell 15**. EX-1005, 7:35-45. Tomita also discloses “one regulator” because it discloses a **boost circuit WL/SL C.P.1**, which receives the input voltage VREF and outputs a regulated voltage VCPWS. EX-1005, 7:20-24, 7:47-50; EX-1003, ¶76; §II.C, *supra*. For example, Tomita discloses that boost circuit 1 outputs 11.5V when writing, erasing, and verifying data, and outputs VDD when reading data. EX-1005, 7:30-34.



Tomita Fig. 4

Tomita’s switch circuits **PBL S.W. 8** and **WL S.W. 6** comprise “first and second switches,” respectively, because they are each a *switch* circuit that receives two inputs (e.g., VSW and VDD for switch circuit 6, and VPB and VDD for switch circuit 8) and “selects and outputs” either of the two inputs received. EX-1005, 8:12-22, 8:40-49; EX-1003, ¶77.

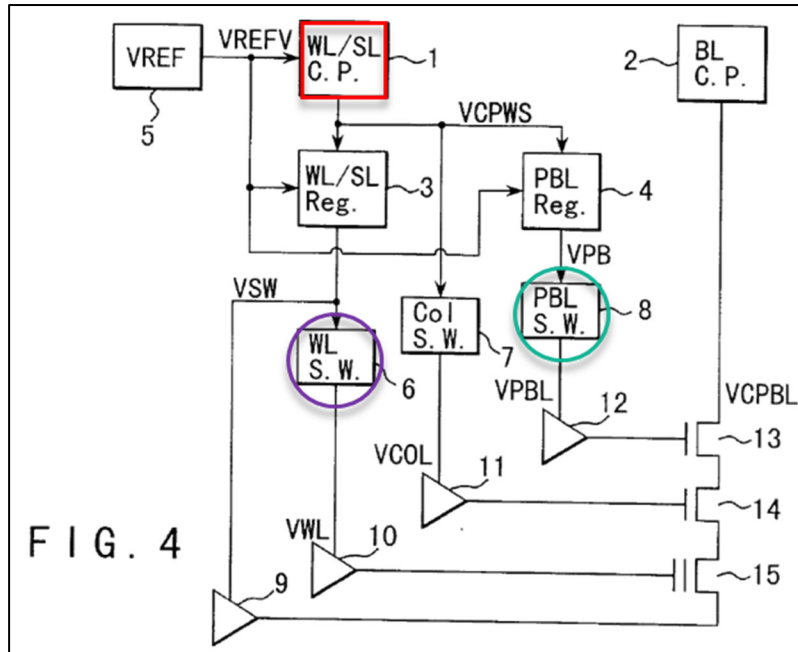
Lastly, Tomita discloses a “voltage applying transistor for applying a voltage to the memory cell 15” because it discloses **write transistor 13**, which “serves to control a drain voltage of the **[memory] cell 15.**” EX-1005, 6:52-53; EX-1003, ¶78. Tomita’s Figure 2 demonstrates a voltage being applied to the memory cell via write transistor 13. EX-1005, 6:49-50; Fig. 2.



Tomita Fig. 2

- (iii) 1[b]: an output of the regulator is coupled to inputs of the first and second switches,

Tomita discloses 1[b] because the output VCPWS of **boost circuit WL/SL C.P. 1** (the “regulator”) is coupled to inputs of **switch circuit 8** and **switch circuit 6**, which comprise the “first” switch and “second” switch, respectively. EX-1005, 7:20-24, 7:50-52, 7:63-65, Fig. 4.



Tomita Fig. 4

The presence of intervening components, namely stepdown circuits 3 and 4, does not undermine that the output VCPWS of the boost circuit 1 (the “regulator”) is “coupled” to inputs of the first and second switches. The plain ordinary meaning of the term “coupled” includes both direct and indirect connections. *See MEMS Tech. Berhad v. Int’l Trade Comm’n*, 447 F. App’x 142, 151-152 (Fed. Cir. 2011) (finding that “electrically coupled” ordinarily includes indirect modes of connection); *GSK Techs. Inc. v. Eaton Elec. Inc.*, No. 606CV358, 2008 WL 906713, at *5 (E.D. Tex. Apr. 1, 2008) (construing “electrically coupled” to mean “arranged so that electrical signals may be passed either directly, or indirectly via intervening circuitry, from one component to another.”); EX-1003, ¶80. Consistent with the ordinary meaning, the ‘888 Patent uses the term “coupled” to include a connection that has

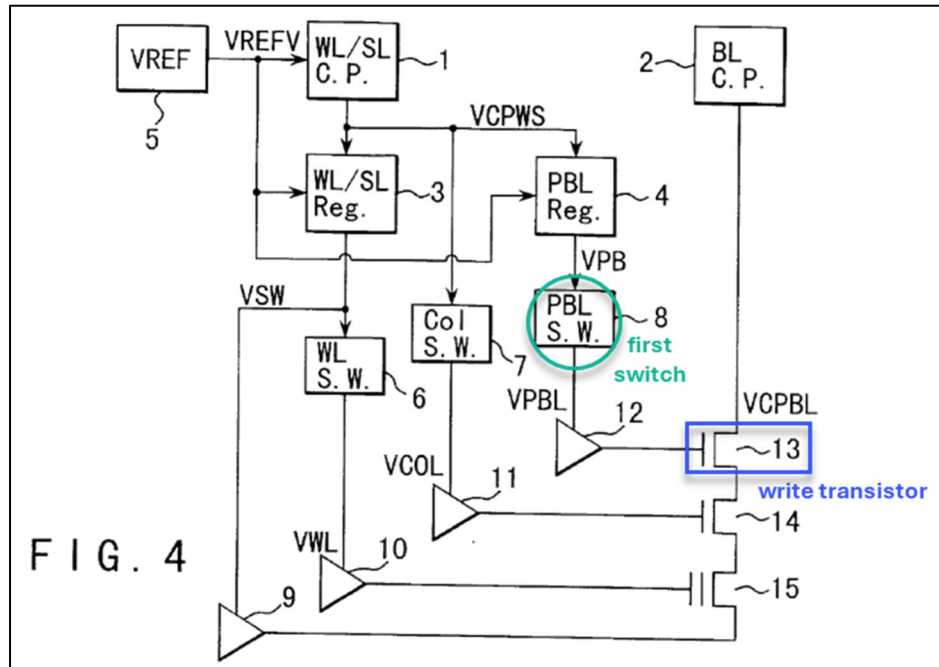
intervening components. *E.g.*, EX-1001, 6:26-28 (“[T]he output of the second switch 203 is coupled to the gate of the memory cell 207 via the row decoder 102.”); EX-1003, ¶80.

Even if the Board finds that *direct* coupling is required between the regulator output and the first and second switches, Tomita discloses 1[b]. Tomita discloses that the output VCPWS of the boost circuit 1 (the “regulator”) may be supplied “directly” for gates of transistor 13 and memory cell 15. EX-1005, 7:35-42. For example, stepdown circuit 3 passes the output of boost circuit 1 “directly” to row decoder 10 when writing and erasing data on the memory cell; and lowers the output before supplying it to row decoder 10 when verifying data after writing and erasing data on the memory cell. EX-1005, 7:54-59; EX-1003, ¶81. The outputs of stepdown circuits 3 and 4, VSW and VPB, respectively, are therefore each also an “output of the regulator,” and the outputs are directly coupled to the first and second switches. EX-1003, ¶81.

(iv) 1[c]: an output of the first switch is coupled to a gate of the voltage applying transistor,

Tomita discloses 1[c] because the output of **switch circuit 8**, which comprises the “first switch,” is coupled, via decoder 12, to a gate of **write transistor 13** (the “voltage applying transistor”). EX-1005, 8:41-50, 2:20-22. As discussed in Section VI.A.2(a)(iii), *supra*, the presence of an intervening component, decoder 12, does

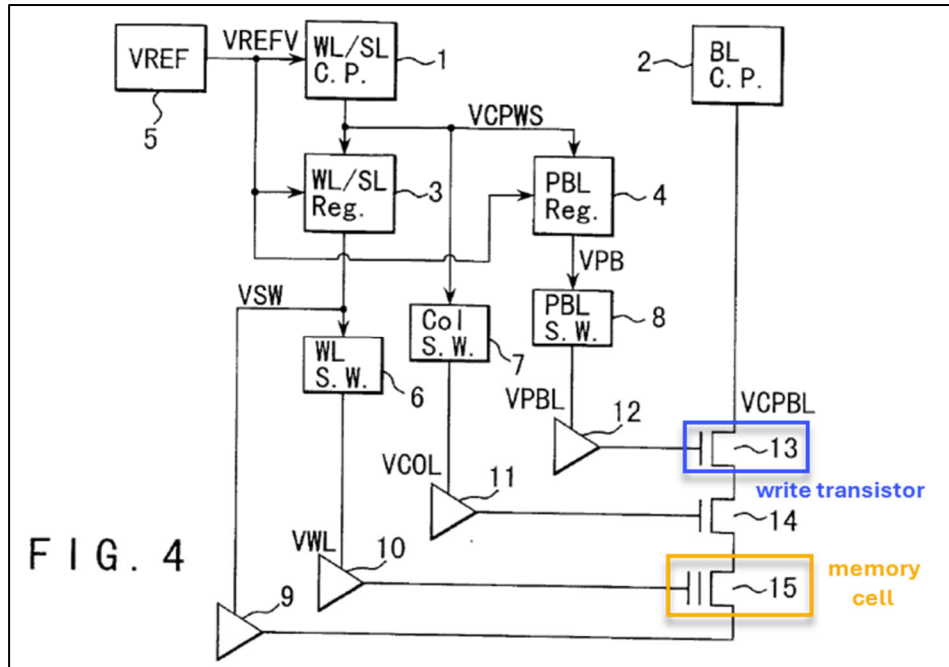
not undermine that the first switch is “coupled” as claimed under its plain and ordinary meaning.



Tomita Fig. 4

- (v) 1[d]: a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and

Tomita discloses 1[d] because **write transistor 13** (the “voltage applying transistor”) applies the voltage it receives from its drain terminal VCPBL to the drain terminal of **memory cell 15**. EX-1003, ¶83.



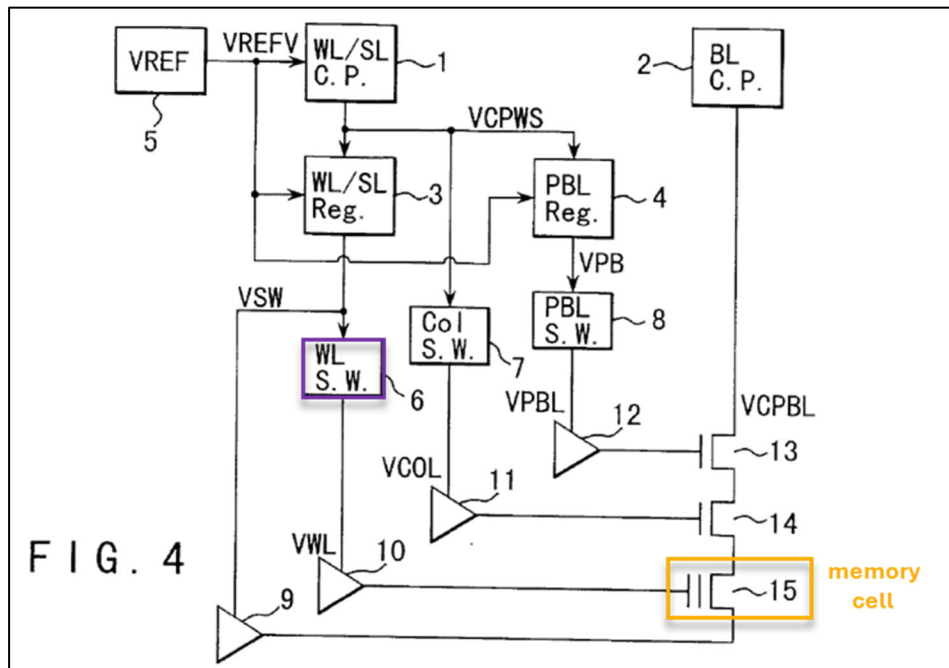
Tomita Fig. 4

Tomita discloses that “**write transistor 13** serves to control *a drain voltage* of the **[memory] cell 15**” (EX-1005, 6:51-52) and that the voltage is applied from a “drain terminal” of the write transistor to a “drain terminal” of the memory cell. *Id.*, 6:52-59 (“A *drain* of the write transistor 13 is applied with a voltage of, for example, 7V” and, “[a]s a result of this, a voltage of 5.5V is applied to a *drain* of the memory cell 15.”), Fig. 2.

- (vi) 1[e]: an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

Tomita discloses 1[e]. In Tomita, the output of **switch circuit 6**, which comprises the “second switch,” is coupled, via row decoder circuit 10, to a gate of **memory cell 15** for application of a voltage such as VSW. EX-1005, 8:11-21, 8:22-

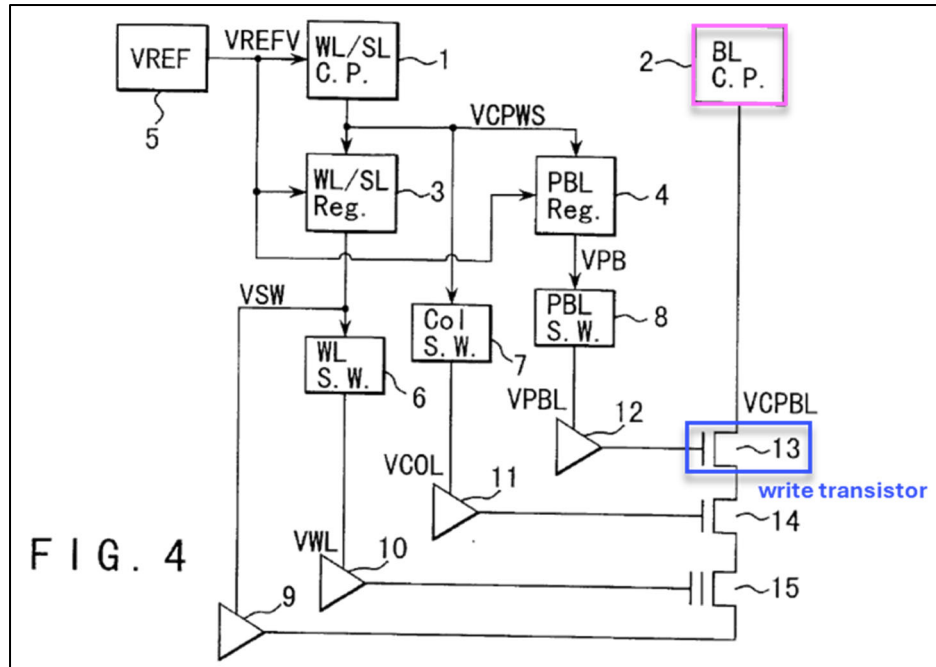
26, 1:40-42, Fig. 4. As discussed in Section VI.A.2(a)(iii), *supra*, the presence of an intervening component, decoder 10, does not undermine that the second switch is “coupled” as claimed under its plain and ordinary meaning.



Tomita Fig. 4

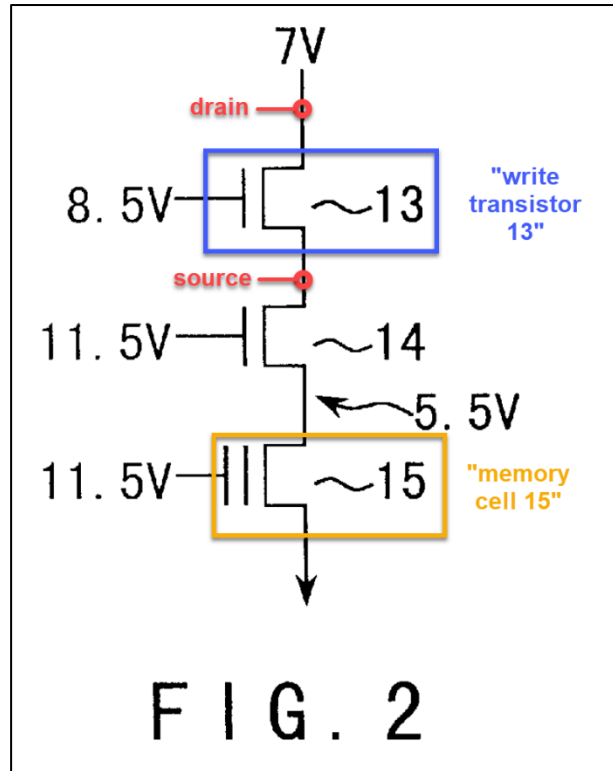
- (b) **Claim 21.** The semiconductor memory device of claim 1, wherein an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

Tomita discloses claim 21. Tomita discloses a **boost circuit BL C.P. 2** (the “booster circuit”), which “generates a high potential of, for example 7V, and supplies this potential to a drain of the [write] transistor 13.” EX-1005, 7:42-46.



Tomita Fig. 4

An output of the booster circuit, VCPBL, is “coupled a source terminal of the voltage applying transistor.” Tomita’s Figure 2, which shows “an example of a voltage applied when writing data into a memory cell 15,” demonstrates coupling of a 7V-output of the **boost circuit 2** to a source terminal of the **write transistor 13** (“the voltage applying transistor”). EX-1005, 6:49-50.



Tomita Fig. 2

Specifically, “[a] drain of the **write transistor 13** is applied with a voltage of, for example, 7V, and a gate of the **[write] transistor 13** is applied with a voltage of 8.5V.” *Id.*, 6:52-54. A POSITA would have understood that the 8.5V applied to the gate of Tomita’s write transistor 13 would have turned “on” the transistor, causing the 7V potential applied at its drain to be applied (with a small drop) to the source terminal, as shown above. EX-1003, ¶88. Indeed, Tomita makes clear that “[a]s a result of this, a voltage of 5.5V is applied to a drain of the memory cell 15.” EX-1005, 6:57-58. The drain terminal of memory cell 15 would receive a voltage of 5.5V if the write transistor 13 is turned “on” and there is a voltage potential applied at its source terminal. EX-1003, ¶88. Accordingly, Tomita discloses the “high

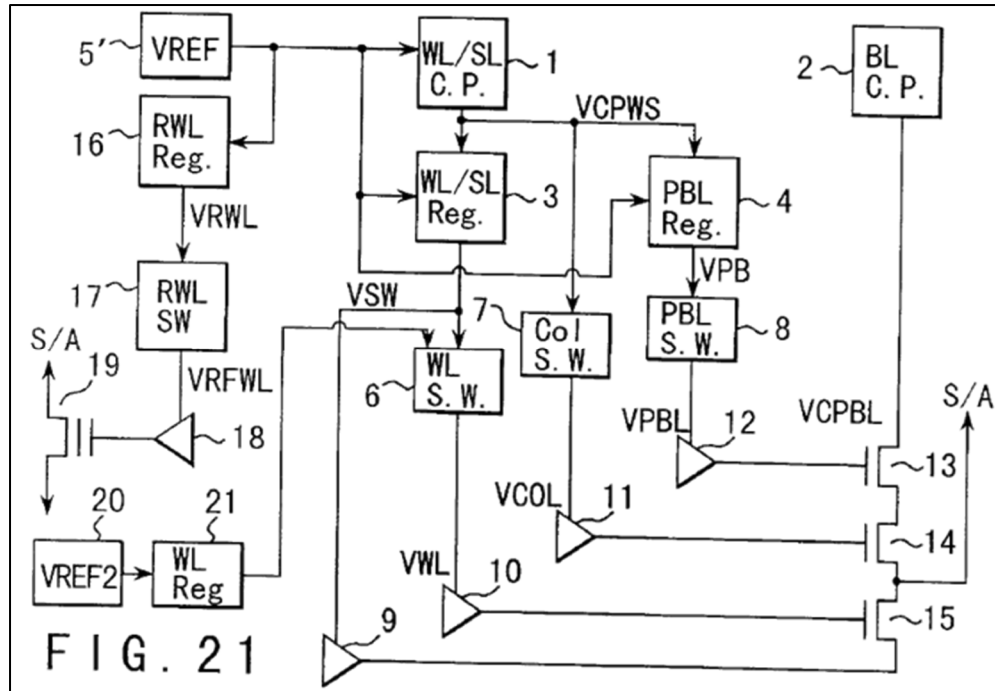
potential of, for example, 7V” (the “output of a booster circuit”) is “coupled to a source terminal” of write transistor 13 (“the voltage applying transistor”).

B. Ground 2: Tomita in View of Im Renders Claims 1, 3, 5, and 20-21 Obvious

1. Overview of Tomita’s Figure 21 Embodiment (EX-1005)

Ground 2 focuses on Tomita’s Figure 21 embodiment. To construct this embodiment, Tomita builds out the circuit shown in Figure 4 by adding a word line power source (elements 16 through 19) (EX-1005, 14:50-57, Fig. 16), low power consumption type reference potential generation circuit VREF2 20, and step down circuit 21. *Id.*, 16:53-59, Figs. 16, 21. Tomita also replaces a reference potential generation circuit VREF5 with VREF5’, the only difference being that VREF5’ operates only when required to reduce the power consumption. *Id.*, 15:61-67, 16:47-52.

Other components of Figure 21 and disclosures about them remain the same as in Figure 4, as described in §VI.A.1, *supra*, and are labeled identically as in Figure 4 and other figures. *Id.*, 16:53-56, 14:53-57.



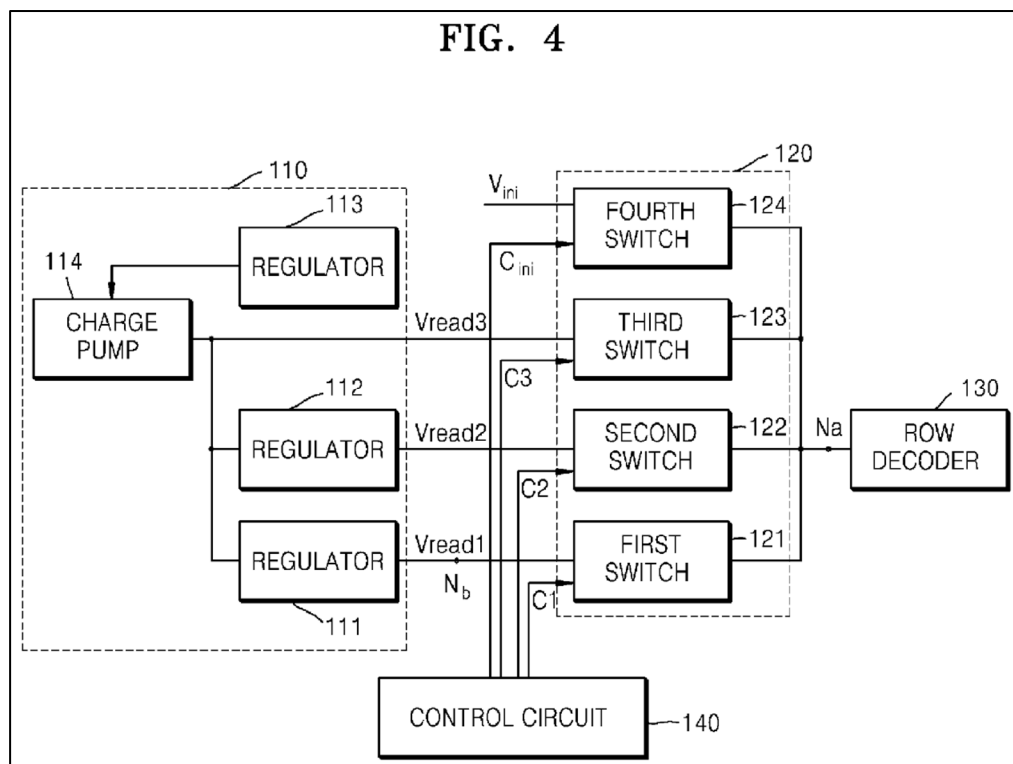
Tomita Fig. 21

Unlike in Figure 4, switch circuit 6 of Figure 21 receives three (rather than two) inputs, namely “output potentials of the stepdown circuits 3 and 21 and the power source potential VDD, and [it] selects and outputs one of the three potentials in accordance with the state of the cell.” *Id.*, 17:4-10. The addition of stepdown circuit 21 enables “independently separate[ing] the function of generating a word line potential when reading data, from the stepdown circuit 3.” *Id.*, 17:1-3. Applying relatively lower supply voltage, “no higher voltage than 5V ... to the word line” also improves the reliability of the cell. *Id.*, 17:11-14.

2. Overview of Im (EX-1010)

Im was filed on January 5, 2009, before the Critical Date, and is therefore prior art under pre-AIA 35 U.S.C. §102(e). EX-1010. Im was not considered by the Examiner during prosecution of the '888 Patent.

Im discloses wordline voltage generating unit 110 configured to provide multiple voltage levels (*e.g.*, Vread1 through Vread 3), which can selectively be applied to a memory cell via switch unit 120 and row decoder 130. *Id.*, 6:14-36, Fig. 4, 6:53-7:18.



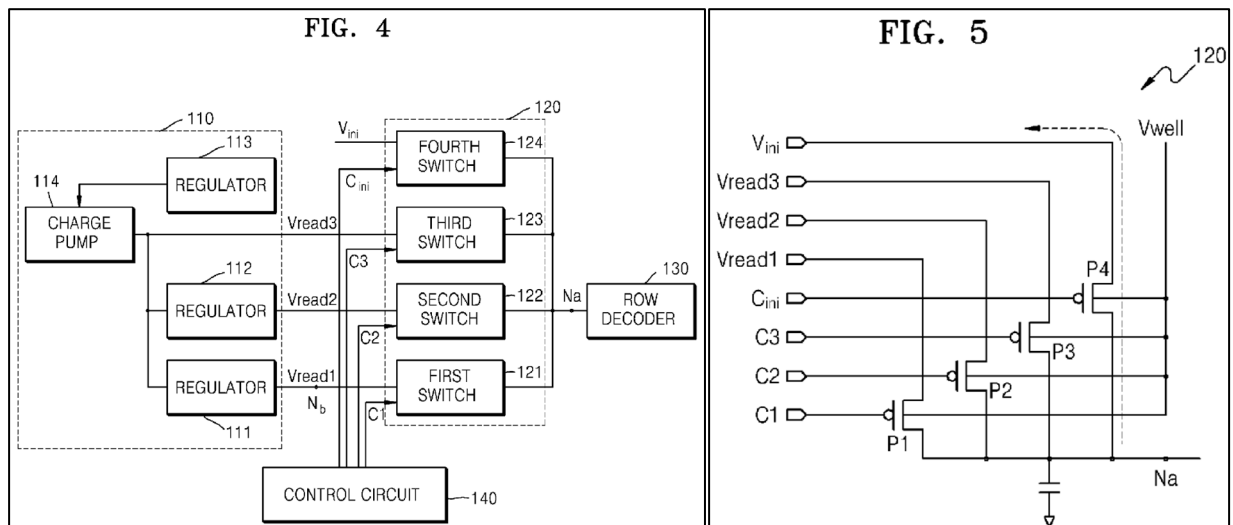
Im Fig. 4

3. Combining Tomita with Im

(a) Implementing Tomita's Switch Circuits in View of Im's Switching Unit

It would have been obvious to implement Tomita's switch circuits 6 and 8 using a plurality of transistor switches, like Im's switch unit 120. In Figure 21, Tomita discloses supplying different voltages (*e.g.*, VDD, VSW, and output of stepdown circuit 21) to the gate of memory cell 15. EX-1005, 17:4-10. The voltages applied for writing and erasing, for example, may be 11.5V and 0V, respectively. *Id.*, 6:49-50, 6:59-61, 6:64-7:7, Figs. 2-3.

Im discloses a conventional implementation of such a switch circuit. EX-1003, ¶96. Im's switch unit 120 includes multiple switches (including switches 121 through 123) "for switching the first through third wordline voltages." EX-1010, 6:29-36, Figs. 3-5. For example, when switch 121 (P1) is turned on, Vread1 will be applied to the memory cell. *Id.*, 6:53-59. When switch 122 (P2) is turned on, Vread2 will be applied as the wordline voltage to a memory cell. *Id.*, 6:60-64.



in the same field of endeavor, *i.e.*, power sources and voltages for “flash memory” designs (EX-1005, 1:5-13; EX-1010, 1:16-18), and disclose common structures for generating and supplying word line voltages, including (a) a **switch circuitry** that receives multiple inputs and selects one of them, such as Tomita’s switch circuits 6 and 8 and Im’s switch unit 120; (b) a **regulator** such as Tomita’s WL/SL C.P.1 and Im’s regulators 111 through 113 and charge pump 114; (c) a **row decoder** such as Tomita’s row decoder circuit 10 and Im’s row decoder 130; and (d) a **memory cell** such as Tomita’s memory cell 15 and Im’s memory cells M11 through M14 and M21 through M26. These are the exact same structures claimed or shown in the ’888 Patent. EX-1003, ¶98.

Im’s disclosures of wordline generation circuit supplement Tomita. EX-1003, ¶99. Tomita discloses that, by adding the stepdown circuit 21 and giving the switch circuit 6 an ability to choose from different potentials depending on the state of the cell (*e.g.*, write, erase, read, and verify), “the reliability of the cell can be improved.” EX-1005, 17:4-14. Im also seeks to improve a memory cell’s reliability, stating that “[a] stable read operation can be performed when the wordline voltages are maintained at uniform values.” EX-1010, 2:7-9. A POSITA looking to improve the stability of a memory device by utilizing different power sources as taught by Tomita would have looked to references like Im for implementation details of a switch circuit. EX-1003, ¶99.

A POSITA would have had a reasonable expectation of success in implementing Tomita's switch circuits 6 and 8 using a plurality of transistors, as disclosed in Im's switch unit 120. EX-1003, ¶100. Tomita already discloses having the switch circuits select from a plurality of different input potentials to supply to the gate terminal of the memory cell 15. EX-1005, 17:4-10, 8:41-51; EX-1003, ¶100. The combination of Tomita and Im would involve no more complexity than implementing Tomita's switch circuits 6 and 8 each with a switch unit 120 from Im's Figure 5, with transistors connected such as shown in Im's FIG. 5 to select between one of several signals, with each of Im's transistors driven by different gate voltages (e.g., C1 through C3) and allowing different voltages (e.g., Vread1 through Vread3) to be applied at the output of the switch, as shown in Im's switch unit 120. EX-1003, ¶100. Indeed, Im discloses that a switch circuit comprising multiple switches connected at a common node was a "conventional method" used for selecting and driving a word line voltage to a memory cell. EX-1010, 2:10-26, 2:30-39, Fig. 2A; §II.D, *supra*.

Implementing Tomita's switch circuits 6 and 8 with a switch unit 120 from Im's Figure 5 would require no other changes to Tomita's existing structure. EX-1003, ¶101. The output of the switch circuit 6 (after it was replaced by a switch unit 120 from Im), for example, would be applied to row decoder 10 and applied to the gate of memory cell 15, in much the same fashion as how the output of Im's switch

(b) Modifying Tomita's Read-Mode Potential Generation Circuit in View of Im

As discussed in Section VI.B.1, Tomita's Figure 21 adds low power consumption type reference potential generation circuit 20 (VREF 2) and stepdown circuit 21 to independently generate a word line potential when reading data. EX-1005, 16:53-59, 17:1-3.

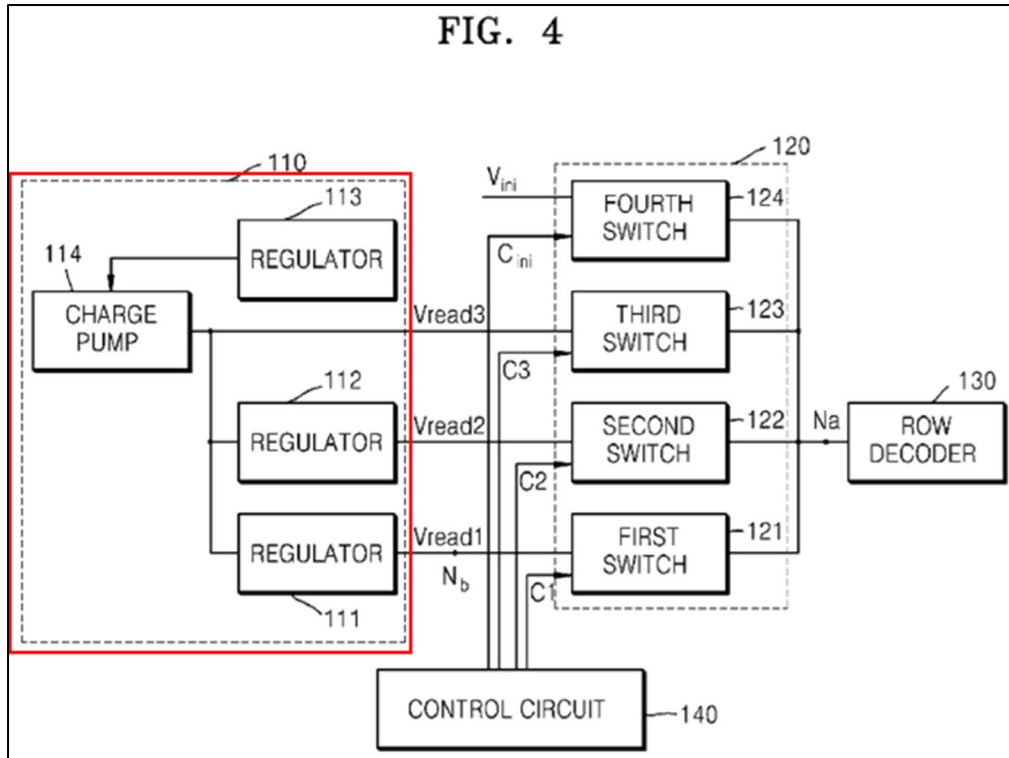


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power source VWL to be a certain level or a lower level.” EX-1005, 15:28-32.

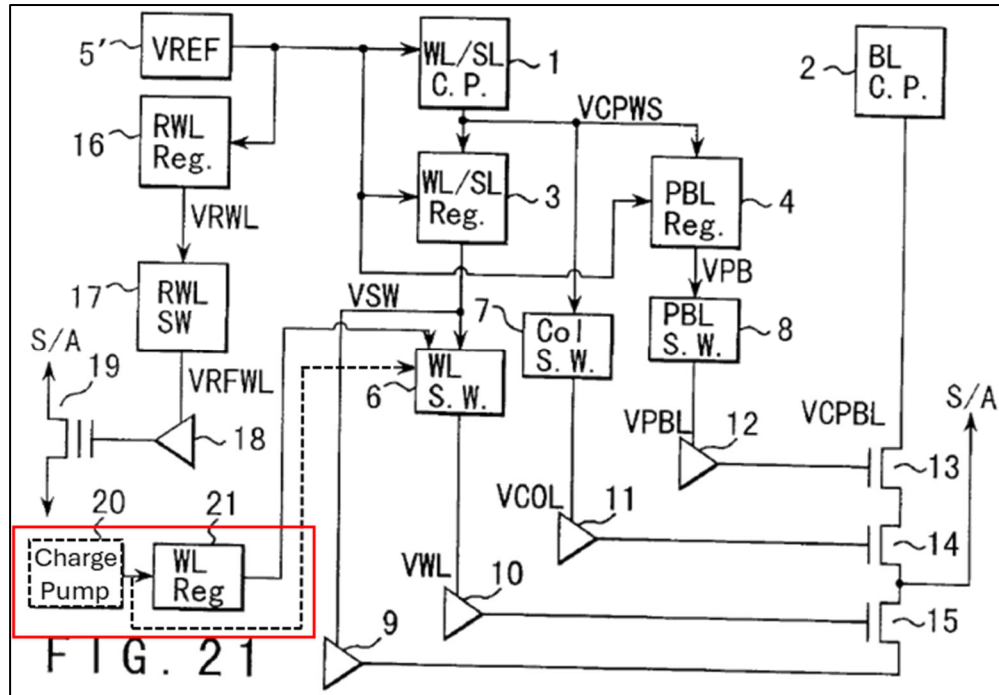
Additionally, Tomita discloses that “there is a case in which a word line power source for a reference cell is provided independently.” *Id.*, 14:40-50. Accordingly, Tomita discloses the need for additional voltages to be driven to the gates of memory cells. EX-1003, ¶104.

Additionally, Im expands on Tomita’s Figure 21 embodiment by disclosing that, to increase the capacity of a memory device, a plurality of wordline voltages can be utilized for reading data. EX-1010, 6:14-28, 1:64-2:9. Im’s Figure 4 illustrates **wordline voltage generating unit 110** generating three different voltages, Vread1, Vread2, and Vread3, and selectively supplying one of the read voltages, via switch unit 120, to row decoder 130. *Id.*, 6:14-28, Fig. 4. As shown in Im’s Figure 4, one of the wordline voltage options, Vread3, is a direct output of charge pump 114, while the other two wordline voltage options are outputs of regulators 111 and 112, which both receive the output of charge pump 114. EX-1003, ¶105.



Im Fig. 4

A POSITA would have found it obvious to modify Tomita's reference potential generation circuit 20 (VREF2) and stepdown circuit 21 such that the output of VREF2, implemented as a charge pump, can bypass stepdown circuit 21 and supplied directly to switch circuit 6, as disclosed in Im. EX-1003, ¶106. The proposed modification is illustrated below in dashed lines:



Modified Tomita Fig. 21

As an initial matter, Tomita states that stepdown circuit 21 “lowers and outputs the power source potential VDD (EX-1005, 16:66-67)” and ensures that “no higher voltage than 5V is applied to the word line.” EX-1005, 17:11-14. From this, a POSITA would understand that the VDD of the Tomita circuit is 5V and that VREF2 is a boost circuit that outputs a voltage higher than 5V. EX-1003, ¶107. A charge pump would have been an obvious choice of design for the boost circuit. *Id.* A charge pump is a well-known boost circuit (*see* §II.C, *supra*), and Tomita already discloses using charge-pump boost circuits—such as boost circuits 1 and 2 (*e.g.*, EX-1005, 7:20-24, 7:42-45, Fig. 4 (boost circuits 1 and 2), Figs. 5-7)—to eliminate the need for an external high voltage power source and save costs. *Id.*, 2:47-55. Moreover, Tomita discloses that VREF2 is a “low power consumption” type

reference potential generation circuit. *Id.*, 16:53-55. A POSITA would understand that a charge-pump based boost-circuit design, such as one based on switched capacitors, is well suited to be used as a “low power consumption type reference potential generation circuit.” EX-1015, Abstract (disclosing a “charge pump circuit” that produces a “voltage much higher than a supply voltage”), [0003]; EX-1016, 1, 9 (a switched capacitor voltage boosting operation used as a regulator, based on “switched capacitor[s]” or “flying capacitor[s]”).

A POSITA would have been motivated to modify the low power generation circuitry in view of Im such that the output of VREF2, implemented as a charge pump as explained above, can bypass the stepdown regulator 21. EX-1003, ¶108. As discussed above, Tomita and Im are in the same field of endeavor, *i.e.*, power sources and voltages for “flash memory” designs EX-1005, 1:5-7; EX-1010, 1:16-18; EX-1003, ¶108. Tomita and Im disclose similar motivations. EX-1003, ¶108. Tomita seeks to improve reliability of *read* operations by adding the stepdown circuit 21 and “separat[ing] the function of generating a word line potential when reading data.” EX-1005, 17:1-14. Tomita thus discloses the motivation for driving the gate of memory cells with a range of different voltages. EX-1005, 14:40-50, 15:28-32, 17:1-14; EX-1003, ¶108. Im furthers Tomita’s goal by disclosing a wordline voltage generation circuit that increases the speed and reliability of *read* operations. EX-1010, 6:46-52; EX-1003, ¶108.

Moreover, market forces demanded memory devices to have an increased storage capacity, which by the time of the Critical Date was commonly achieved with the use of a multi-level cell (MLC) method. EX-1010, 1:64-2:9; EX-1006, 1:59-2:8; EX-1003, ¶109. Unlike in the single-level cell (SLC) method, in the MLC method, one cell stores two or more bits, requiring using multiple voltage thresholds to perform memory operations on a cell. EX-1010, 1:66-2:9; EX-1006, 1:62-2:8; EX-1003, ¶109. To construct a high-capacity memory device based on Tomita's teaching, a POSITA would have utilized the MLC method and looked to references like Im for implementation details on multi-level wordline voltage generation. EX-1003, ¶109.

The modification would have provided a predictable benefit. EX-1003, ¶110. Allowing VREF2 to bypass stepdown circuit 21 and supply a boosted voltage directly to Tomita's switch circuit 6 would increase the range of voltage supplies available in a read operation. *Id.* Specifically, by directly receiving the output of VREF20, Tomita's switch circuit 6 can drive memory cell 15 with a relatively higher voltage not limited by stepdown circuit 21, in a low power consumption setting. *Id.* The wider range of read voltages would have improved device reliability and performance. *Id.*

A POSITA would have had a reasonable expectation in implementing VREF2 as a charge pump capable of bypassing stepdown circuit 21, as disclosed in Im. EX-

1003, ¶111. The only modification would be to connect the charge pump directly to a switch in switch circuit 6 (*e.g.*, transistor P3 in Im's switch unit 120). Im discloses precisely such an implementation: as shown in Im's Figure 4, switch unit 120 receives both the direct output of charge pump 114 (switch 123) and output voltages of regulators 111 and 112 (respectively fed through switches 121 and 122). EX-1010, 6:29-36, Fig. 4-5; EX-1003, ¶111. The proposed modification would simply extend the functionality of the charge pump VREF2 and stepdown circuit 21 and enhance the storage capacity of the memory while maintaining reliable operation. EX-1003, ¶111.

No other modification is needed for the rest of the Tomita's wordline path. EX-1003, ¶112. The output of the switch circuit 6, for example, would be applied to row decoder 10 and applied to the gate of memory cell 15, in much the same fashion as how the output of Im's switch unit 120 is supplied via row decoder 130 to memory cells. EX-1005, 7:35-41, 16:53-56, 14:53-57; EX-1010, 6:29-36; EX-1003, ¶112.

4. Analysis

(a) Claim 1

- (i) **1[pre]: A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:**

Tomita discloses 1[pre] as discussed in Ground 1. *See* §VI.A.2(a)(i), *supra*.

As discussed in Ground 1, Tomita discloses **memory cell 15**, **boost circuit WL/SL C.P.1**, and **write transistor 13**, which are the claimed “memory cell,” “one regulator,” and “voltage applying transistor,” respectively. EX-1005, 7:25-42, 6:49-53, Fig. 2; EX-1003, ¶114; §VI.A.2(a)(ii). The same description applies to Figure 21. *Id.*, 16:53-59, 14:51-57.



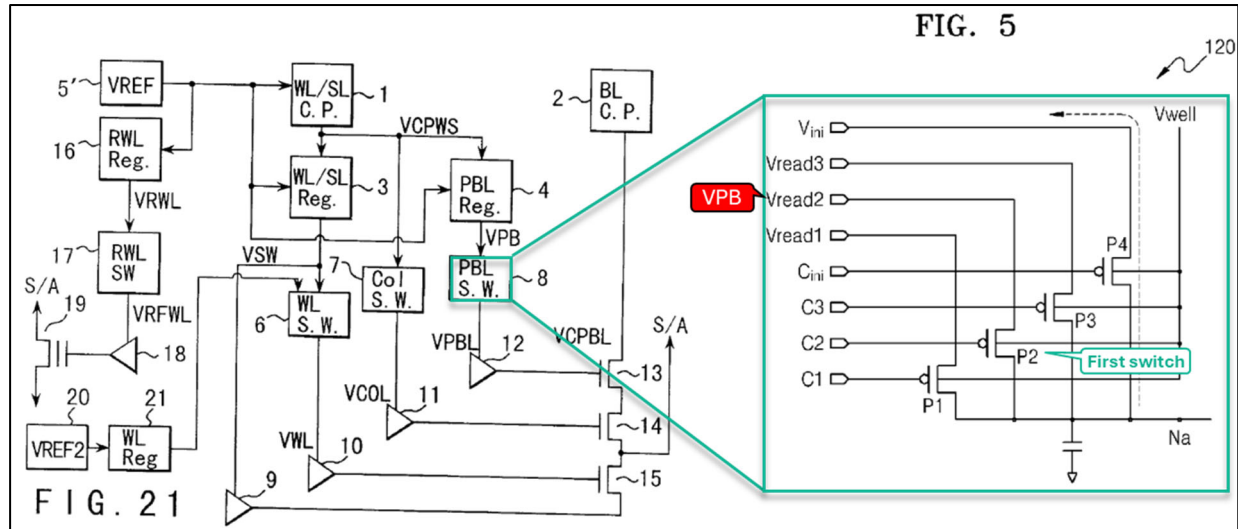
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In Tomita-Im, the output VCPWS of **boost circuit WL/SL C.P. 1** (the “regulator”) is coupled to inputs of the **first** and **second** switches in switch circuit 8 and switch circuit 6, respectively, as discussed in 1[a] above. EX-1005, 7:20-24, 7:50-52, 7:63-65; §VI.B.4(a)(ii), *supra*.

As discussed in Ground 1, the presence of intervening components, namely stepdown circuits 3 and 4, does not undermine that the output of the boost circuit 1 (the “regulator”) is “coupled” to inputs of the first and second switches. *See* §VI.A.2(a)(iii), *supra*. And even if the Board finds that *direct* coupling is required between the regulator output and the first and second switches, Tomita-Im would meet such a requirement because the output VCPWS of the boost circuit 1 (the “regulator”) may be supplied “directly” for gates of transistor 13 and memory cell 15. EX-1005, 7:47-50, 7:35-42, 7:54-59; VI.A.2(a)(iii), *supra*. The outputs of stepdown circuits 3 and 4, VSW and VPB, respectively, are therefore each also an “output of the regulator,” coupled to the first and second switches (*e.g.*, transistors P2 from Im’s Fig. 5, in switch circuits 8 and 6, respectively). EX-1003, ¶118.

(iv) 1[c]: an output of the first switch is coupled to a gate of the voltage applying transistor,

Tomita-Im renders 1[c] obvious because the output VPBL of the “**first switch**” (*e.g.*, transistor P2 in switch circuit 8, *see* §VI.B.4(a)(iii), *supra*) is coupled, via decoder 12, to a gate of **write transistor 13** (the “voltage applying transistor”). EX-1005, 8:41-50.



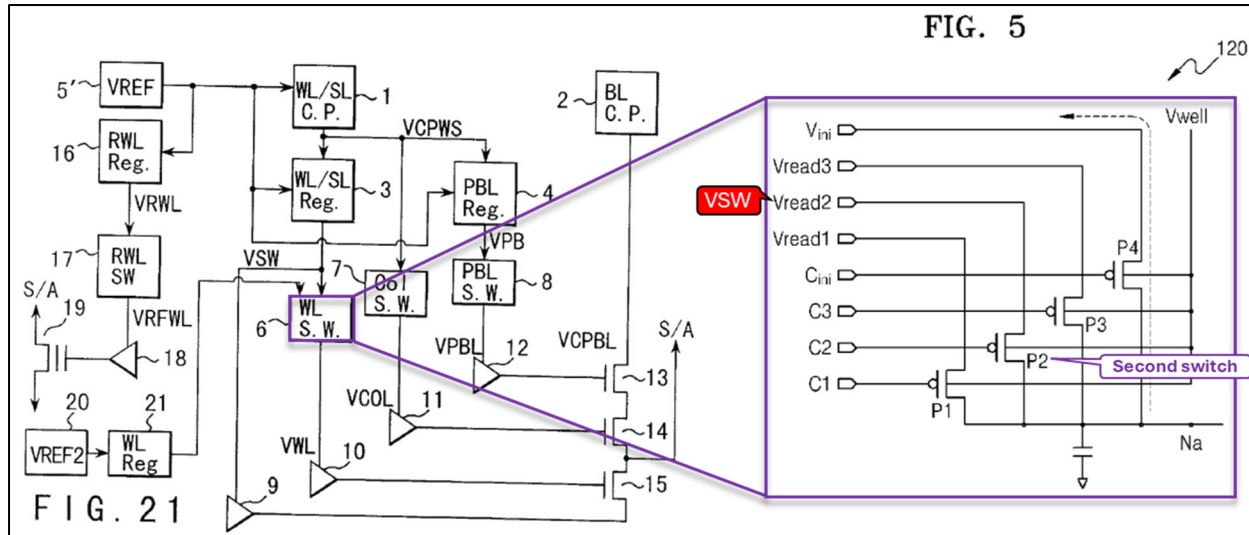
Tomita Fig. 21 (left) and Im Fig. 5 (right)

- (v) 1[d]: a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and

Tomita discloses 1[d] because, as discussed in Ground 1, **write transistor 13** (the “voltage applying transistor”) applies the voltage it receives from its drain terminal VCPBL to the drain terminal of **memory cell 15**. EX-1005, 6:51-59, Fig. 2; EX-1003, ¶120; §VI.A.2(a)(v), *supra*.

- (vi) 1[e]: an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

Tomita-Im renders 1[e] obvious because the output VWL of the “**second switch**” (e.g., P2 in switch circuit 6, see §VI.B.4(a)(iii), *supra*) is coupled, via row decoder circuit 10, to a gate of **memory cell 15** for application of a voltage. EX-1005, 8:11-26, 1:40-42.

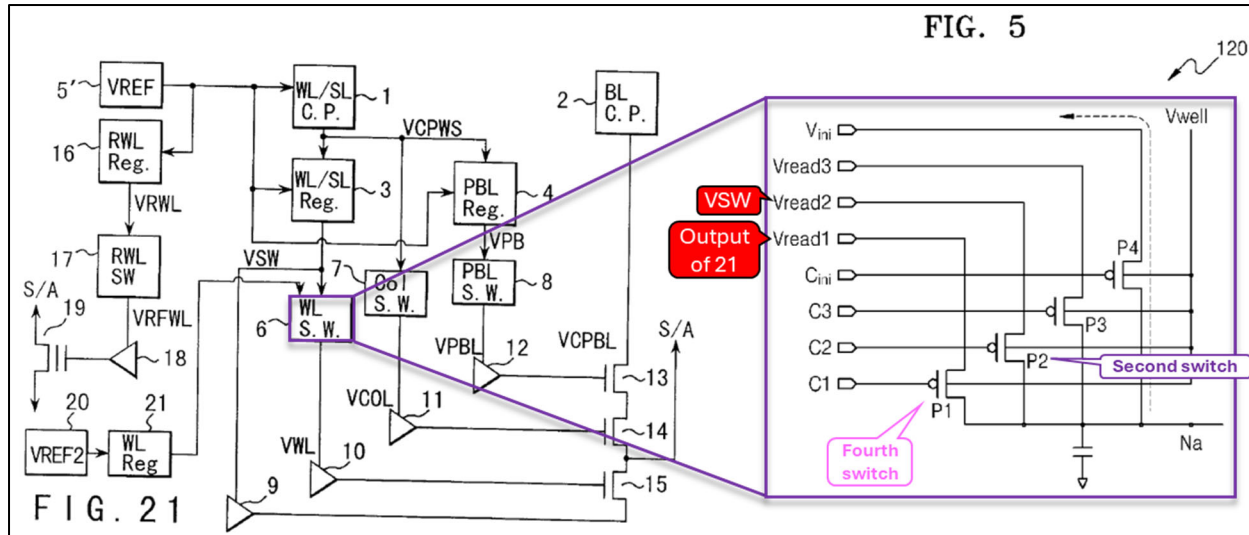


Tomita Fig. 21 (left) and Im Fig. 5 (right)

(b) Claim 3

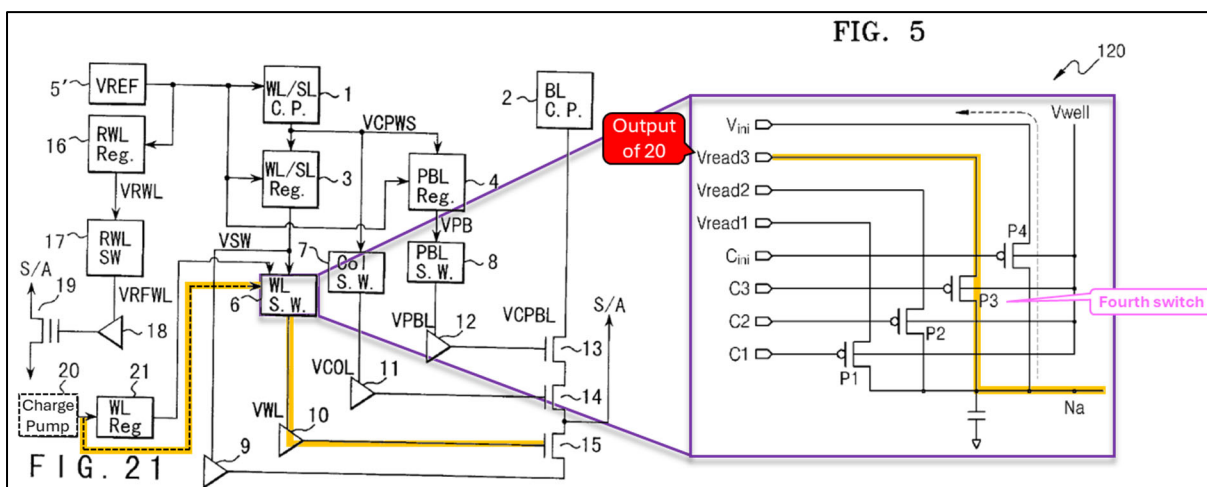
- (i) 3[a]: The semiconductor memory device of claim 1, wherein: an output of a fourth switch is coupled to the output of the second switch, and;

Tomita-Im renders 3[a] obvious. As discussed for 1[a] (*see* §VI.B.4(a)(ii), *supra*), Tomita-Im's switch circuit 6 includes transistors P2 and P1, which supply power sources VSW and the output of stepdown circuit 21, respectively, to memory cell 15. Transistor P1 in switch circuit 6 is a “**fourth switch**,” and its output is coupled to the output of transistor P2 (the “**second switch**”). EX-1003, ¶122; EX-1005, Fig. 21.



Tomita Fig. 21 (left) and Im Fig. 5 (right)

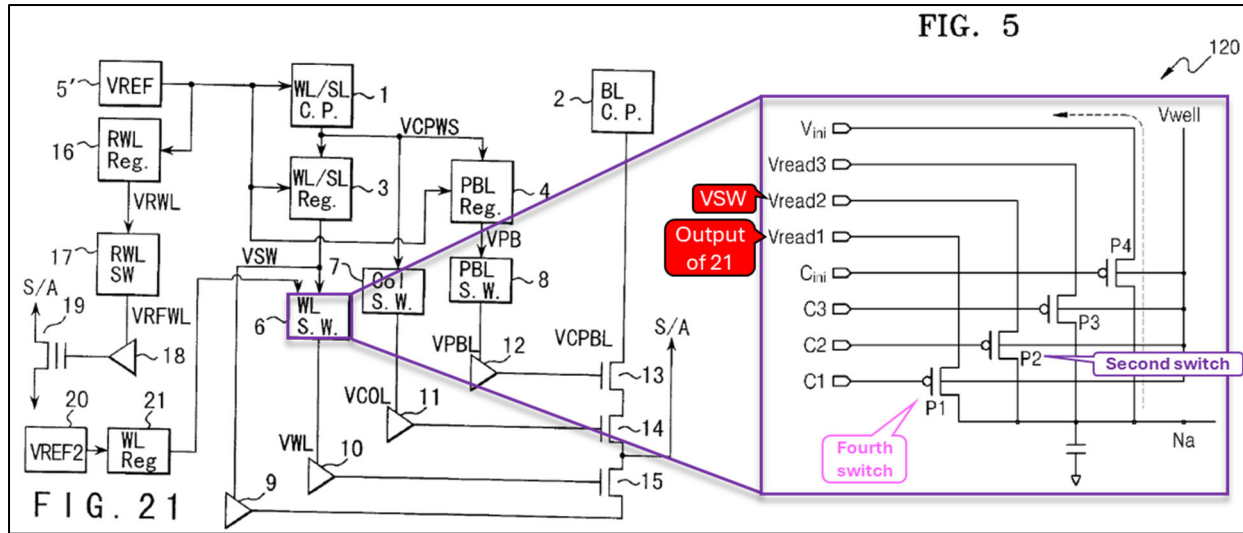
Alternatively, when Tomita is further modified, as discussed in Section VI.B.3(b), *supra*, such that VREF2 is implemented as a charge pump that can directly supply a potential to switch circuit 6, transistor P3 in switch circuit 6 is also a “**fourth switch**,” and its output is coupled to the output of transistor P2 (the “**second switch**”). EX-1003, ¶123; EX-1005, Fig. 21.



Modified Tomita Fig. 21 (left) and Im Fig. 5 (right)

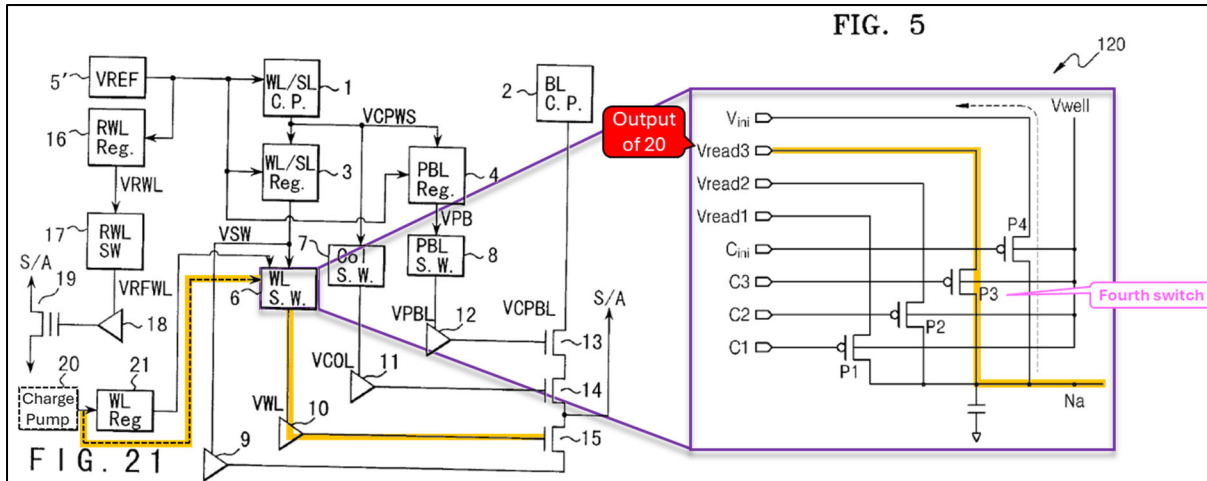
- (ii) **3[b]: a voltage different from the output of the regulator is applied to the gate of the memory cell.**

Tomita-Im renders 3[b] obvious. Tomita's switch circuit 6 is "supplied with output potentials of the stepdown circuits 3 and 21 and the power source potential VDD" and "selects and outputs one of the three potentials" based on the state of memory cell 15, such as write, read, erase, and verify. EX-1005, 17:4-10. The output of stepdown circuit 21, for example, is a "voltage different from the output of the regulator." EX-1003, ¶124. As discussed in 1[b] (§VI.B.4(a)(iii), *supra*), VCPWS and VSW are each "the output of the regulator." EX-1005, 7:47-50, 7:54-59; EX-1003, ¶124. Further, Tomita discloses that the Figure 21 embodiment "is arranged to as to independently separate the function of generating a word line potential when reading data, from the stepdown circuit 3" (EX-1005, 17:1-3), indicating that the voltage of the stepdown circuit 21 is "independently separate" from the other voltages produced for switch circuit 6 to drive the wordline of the memory cell. EX-1003, ¶124. Thus, the output of stepdown circuit 21 is "a voltage different from" the output of the regulator (e.g., VCPWS and VSW). When switch circuit 6 selects and outputs the output of stepdown circuit 21, it is "applied to the gate of the memory cell." EX-1005, Fig. 21; EX-1003, ¶124.



Tomita Fig. 21 (left) and Im Fig. 5 (right)

In addition, when Tomita is further modified, as discussed in Section VI.B.3(b), *supra*, such that VREF2 is implemented as a charge pump that can directly supply a potential to switch circuit 6, the output of charge pump 20 is also “a voltage different from” the output (VCPWS or VSW) of boost circuit 1 (“the regulator”). EX-1005, 7:54-59; EX-1003, ¶125. When switch circuit 6 selects and outputs the output of charge pump 20, it is “applied to the gate of the memory cell,” as illustrated below. EX-1005, Fig. 21; EX-1003, ¶125.



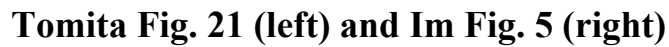
Modified Tomita Fig. 21 (left) and Im Fig. 5 (right)

(c) Claim 5.

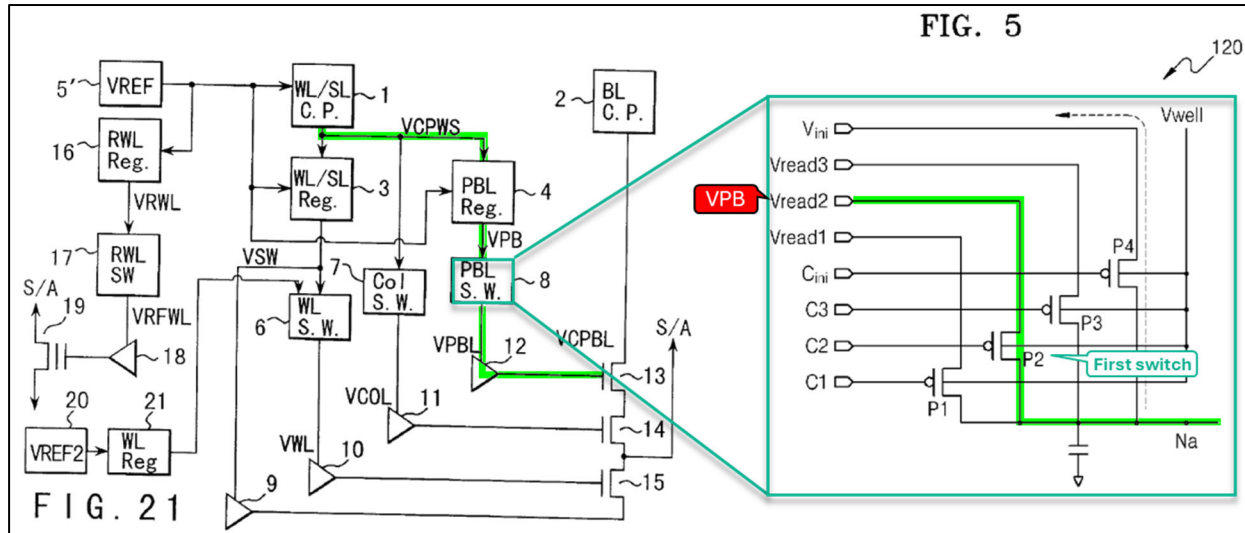
- (i) 5[a][i]:** The semiconductor memory device of claim 3, wherein: in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and;

Tomita-Im renders 5[a] obvious. *First*, Tomita-Im renders obvious that, “in a first operation mode, the first and fourth switches are turned on.” Tomita discloses different modes of operation for the power source circuit, such as a “writing,” “erasing,” “verifying,” and a “reading” mode. EX-1005, 7:30-34, 7:54-59. The reading mode, for example, is a “first operation mode.” EX-1003, ¶126. In the reading mode, Tomita discloses using low potential generation circuit 20 and stepdown circuit 21 to supply, via switch circuit 6, a voltage of 5V or less to the gate of memory cell 15. *Id.*, 17:1-3, 17:4-14, Fig. 21. Transistor P1 in switch circuit 6 (the “**fourth switch**”) is therefore turned on, allowing the 5V-potential to be applied

EX-1003, ¶126.



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Tomita Fig. 21 (left) and Im Fig. 5 (right)

Further, in the reading mode, Tomita-Im “allow[s] the output voltage of the regulator to be applied to the drain terminal of the memory cell.” As discussed in Section V, *supra*, this limitation should be corrected to recite that the output voltage of the regulator is to be applied to “the gate of the voltage applying transistor.” Under this construction, Tomita-Im meets this limitation because, when the **first switch P2** in switch circuit 8 (see §VI.B.4(a)(iii), *supra*) is on, it allows the output VCPWS, and by extension VPB, of **boost circuit 1** (the “regulator”) to be applied to the gate of **write transistor 13** (the “voltage applying transistor”) via decoder 12. EX-1003, ¶128. Application of the regulator’s output to the gate of the voltage applying transistor is illustrated in green traces above.

Even if the Board disagrees with Petitioner’s proposed construction, Tomita-Im would still render this limitation obvious. The specification of the ‘888 Patent

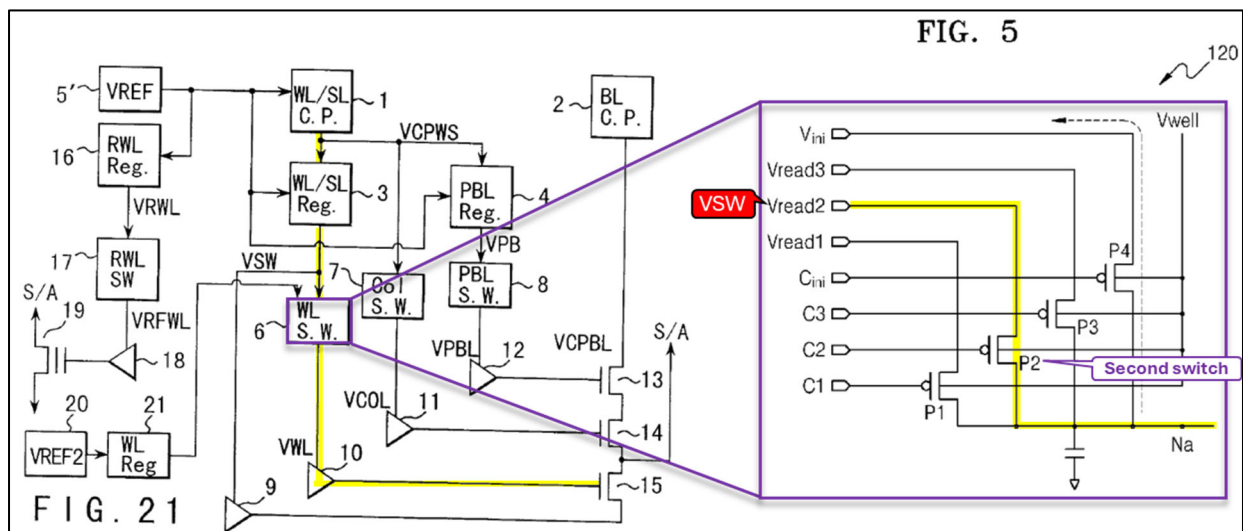
describes applying the output voltage of a regulator to the gate of a voltage applying transistor as a means to control a voltage applied to the drain terminal of a memory cell. EX-1001, 4:61-67, 6:45-53, 7:13-22, 8:6-18; EX-1003, ¶129. There is no other embodiment in the '888 patent that would support a claim requirement that the regulator output be supplied to the drain of the memory cell. EX-1003, ¶129. As such, if the Board finds that the embodiments in the specification support the claim language as drafted, because Tomita-Im discloses applying the regulator output (VCPWS and VPB) to the gate of transistor 13 and as a means to control the application of a voltage to the drain of memory cell 15, Tomita-Im would meet this limitation. *Id.*

(ii) 5[a][ii] the voltage different from the output of the regulator to be applied to the gate of the memory cell, and

Tomita-Im renders 5[a][ii] obvious because, as discussed for 3[b], the potential output by stepdown regulator 21, which is limited to 5V or less in the reading mode, is the “voltage different from the output of the regulator to be applied to the gate of the memory cell” (*i.e.*, memory cell 15). EX-1005, 17:1-3, 17:4-14, Fig. 21; EX-1003, ¶130; §VI.B.4(b)(ii), *supra*.

(iii) 5[b]: in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

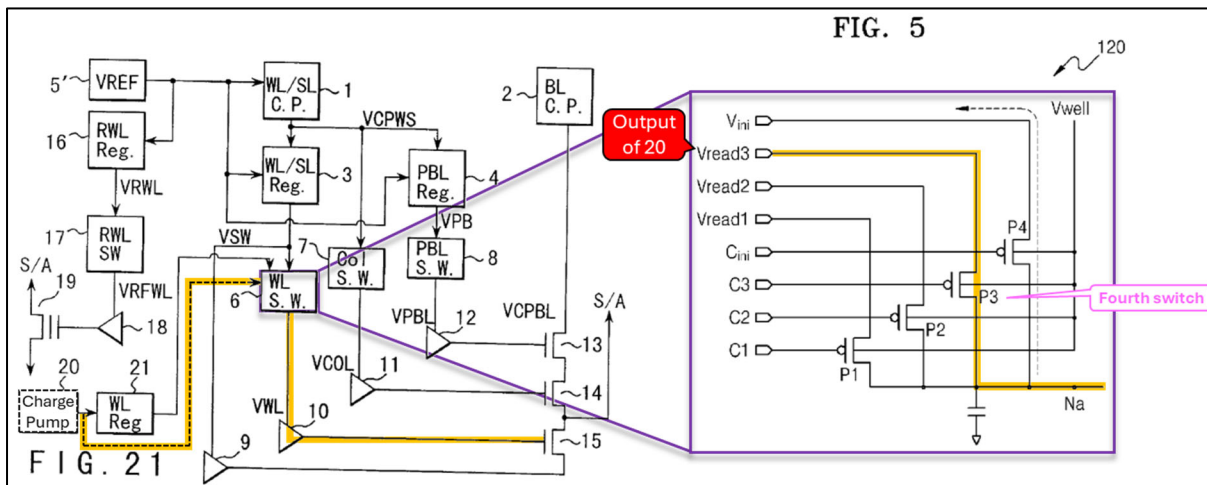
Tomita-Im renders 5[b] obvious. In the writing, erasing, and verify modes, transistor P2 in switch circuit 6 (the “**second switch**”) is turned on, allowing the output voltage VCPWS, and by extension VSW, of boost circuit 1 (the “regulator”) to be applied to the gate of memory cell 15, as illustrated with yellow highlights below. EX-1005, 7:30-34 (“The boost circuit 1 outputs a high potential of, for example, 11.5V when writing, erasing, and verifying data on the memory cell.”), 7:54-59 (“The stepdown circuit 3 “directly outputs an output potential VCPWS of the boost circuit 1 when writing and erasing data on the memory cell” and “lowers the potential VCPWS to, for example, 6V” “when verifying data.”); EX-1003, ¶131. Accordingly, the writing, erasing, and verifying mode are each a “second operation mode.” In each of these modes, the output voltage of the boost circuit 1 (the “regulator”) is applied to the gate of the memory cell, as seen in the highlight below.



Tomita Fig. 21 (left) and Im Fig. 5 (right)

(d) Claim 20. The semiconductor memory device of claim 3, wherein the voltage different from the output of the regulator is an output voltage of a booster circuit.

Tomita-Im renders claim 20 obvious. As discussed in 3[b], charge pump is a “booster circuit,” and therefore “the voltage different from the output of the regulator” is an “output voltage of a booster circuit.” EX-1005, 7:30-34, 42-45.



Modified Tomita Fig. 21 (left) and Im Fig. 5 (right)

(e) Claim 21. The semiconductor memory device of claim 1, wherein an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

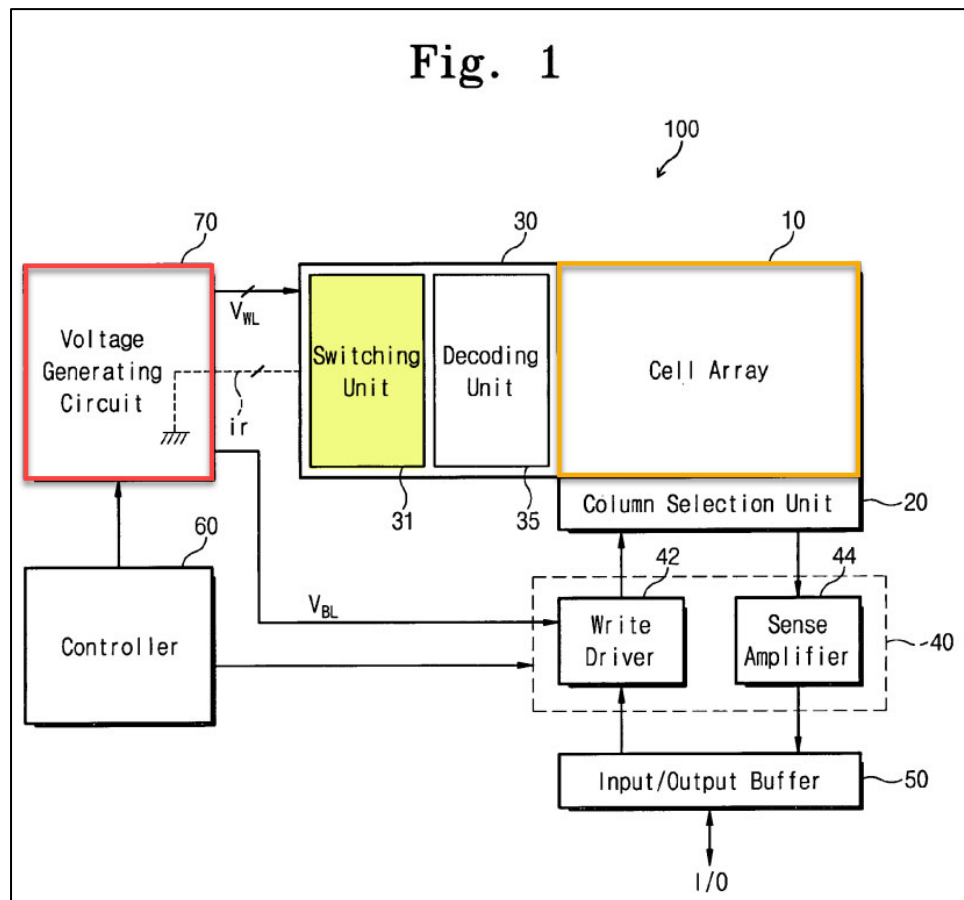
Tomita-Im renders claim 21 obvious because, as discussed in Ground 1 (§VI.A.2(b), *supra*), the output of **boost circuit BL C.P. 2** (the “booster circuit”) is “coupled a source terminal” of **write transistor 13** (“the voltage applying transistor”). EX-1005, 6:49-58, Figs. 2-4. 14:51-57, 16:53-59.

C. Ground 3: Tomita in View of Nam Renders Claims 1, 3, 5, and 21 Obvious

1. Overview of Nam (EX-1006)

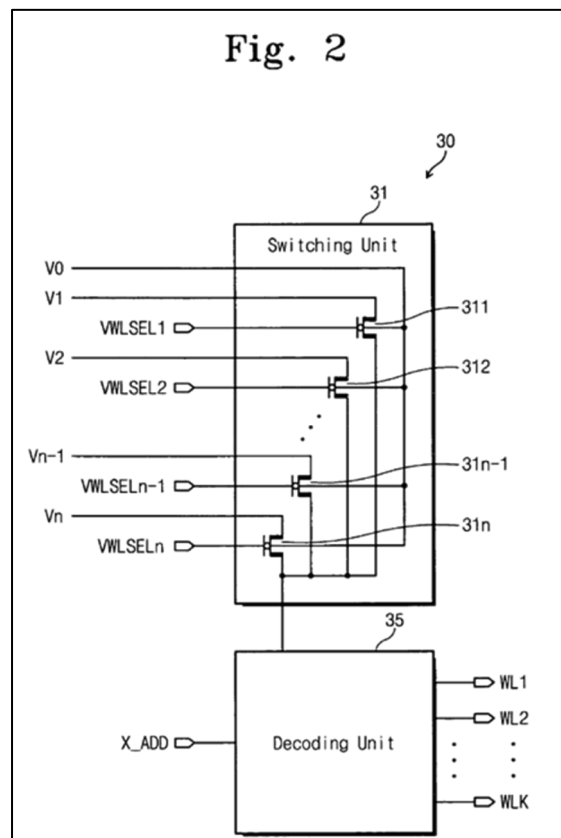
Nam is prior art under at least pre-AIA 35 U.S.C. §§102(a)-(b), having been patented on May 13, 2008, and thus before the Critical Date. Nam was not considered by the Examiner during prosecution of the '888 Patent.

Similar to Tomita, Nam discloses “[a] flash memory device and a voltage generating circuit for the same.” EX-1006, Abstract, Fig. 1.



Nam Fig. 1

According to Nam, “**memory cell array 10** includes a plurality of memory cells arranged at intersection regions where a plurality of rows, i.e., word lines, and a plurality of columns, i.e., bit lines, are intersected with each other.” EX-1006, 3:46-49. Further, “**voltage generating circuit 70** generates a plurality of constant voltages needed for the program, erase, and read-out operations of the memory cell” (*id.*, 3:49-52), and “switching unit 31 selects one constant voltage among the plurality of constant voltages generated by the voltage generating circuit 70.” *Id.*, 3:56-58. Figure 2 of Nam illustrates the row selection unit 30 of Figure 1, including switching unit 31.



Nam Fig. 2

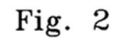
In Figure 2 of Nam, “[t]he MOS transistors 311, 312, 31n-1, and 31n **act as switches** so that they receive a plurality of constant voltages V0, V1, V2, ... , Vn-1, and Vn, respectively, and select to output one among the input constant voltages V0, V1, V2, ... Vn-1, and Vn.” EX-1006, 4:27-33.

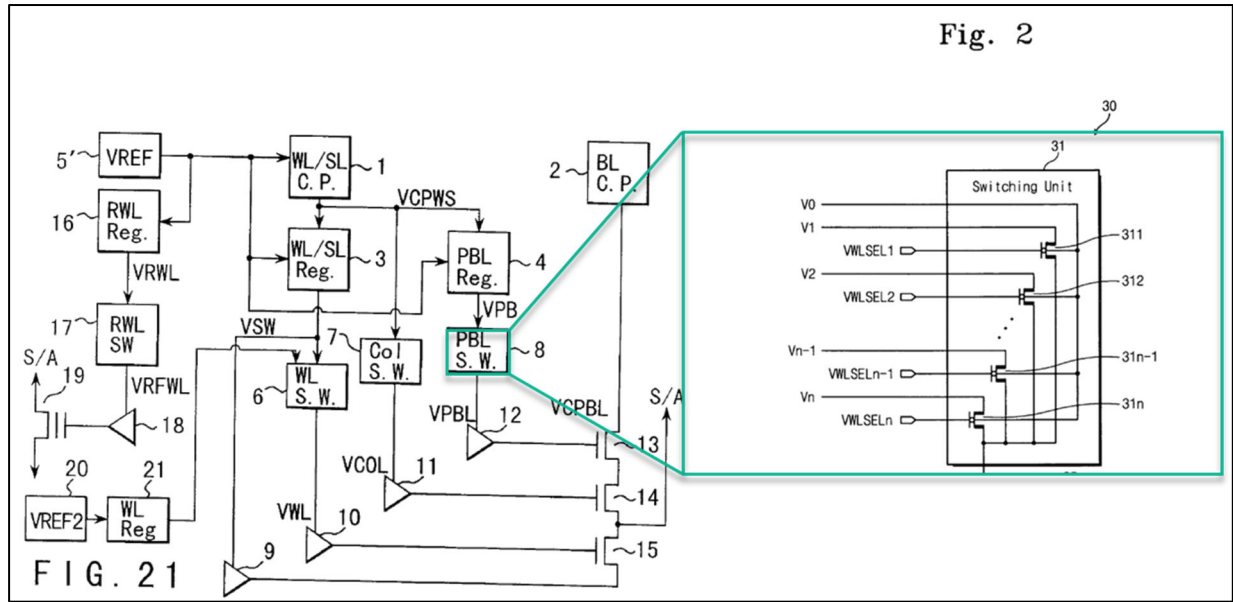
2. Implementing Tomita’s Switch Circuits in View of Nam’s Switching Unit

It would have been obvious to implement Tomita’s switch circuits 6 and 8 using a plurality of transistor switches, as Nam discloses in switching unit 31. Tomita discloses supplying different voltages (e.g., the “output potentials of the stepdown circuits 3 and 21 and the power source potential VDD”) to the gate of memory cell 15, for the operations of writing, reading, erasing and verifying. EX-1005, 17:4-10. The gate voltages applied to memory cell 15 for writing and erasing, for example, may be 11.5V and 0V, respectively. *Id.*, 6:49-50, 6:59-63, 6:64-7:7, Figs. 2-3.

Nam discloses a conventional implementation of such a switch circuit. EX-1003, ¶139. Like Tomita’s switch circuit 6 that “selects and outputs” “potentials in accordance with the state of the cell” (write, read erase or verify) (EX-1005, 17:4-10, 8:11-22), Nam discloses a switching unit 31 “select[ing] to output one among the input constant voltages V0, V1, V2, ... , Vn-1, and Vn.” EX-1006, 4:27-36. For example, when switch 312 is turned on, V2 will be applied to the gate of memory cells in cell array 10. EX-1006, Fig. 1; EX-1003, ¶139. When switch 31n is turned

A POSITA would have found it obvious to implement Tomita's word line **switch circuit 6** and **switch circuit 8** with a plurality of transistor switches (e.g., 311, 312, ... , 31n), as disclosed in Nam's Figure 2, as illustrated below. EX-1003, ¶140.





Tomita Fig. 21 (left); Nam Fig. 2 (right)

A POSITA would have been motivated to implement Tomita's switch circuits 6 and 8 using a plurality of transistor switches implemented in the manner described in Switching Unit 31 of Nam's Fig 2. EX-1003, ¶141. Both Nam and Tomita are directed to the field of voltage supply circuits for semiconductor memory devices, the same field of the '888 Patent. EX-1005, 1:5-7; EX-1006, 1:15-17; EX-1003, ¶141. Tomita and Nam disclose common structures for generating and supplying word line voltages, including (a) a **switch circuitry** that receives multiple inputs and selects one of them, such as Tomita's switch circuits 6 and 8 and Nam's switching unit 31; (b) a **regulator** such as Tomita's WL/SL C.P.1 and Nam's voltage generating circuit 70; (c) a **row decoder** such as Tomita's row decoder circuit 10 and Nam's row decoding unit 35; and (d) a **memory cell** such as Tomita's memory cell 15 and Nam's memory cell in cell array 10. These are the exact same structures

claimed or shown in the '888 Patent. EX-1003, ¶141.

Nam and Tomita disclose similar motivations. Tomita discloses that, by giving the switch circuit 6 an ability to choose from different potentials depending on the state of the cell (*e.g.*, write, erase, and read) while avoiding “an external high voltage power source,” “the reliability of the cell can be improved.” EX-1005, 2:34-35, 17:4-14, 8:41-51. Similarly, Nam discloses that reducing “[t]he fluctuation of voltages generated by the voltage generating circuit” and “more accurately and stably perform a program, an erase, and a read-out operation on the flash memory device.” EX-1006, 3:33-37. A POSITA looking to improve the stability of the different operations performed by a memory device by utilizing different power sources as taught by Tomita would have looked to references like Nam for implementation details of a switch circuit. EX-1003, ¶142.

A POSITA would have had a reasonable expectation in implementing Tomita’s switch circuits 6 and 8 using a plurality of transistors, configured as shown in Switching Unit 31 of Nam’s Fig. 2, to select between one of several input signals of the switch circuits 6 and 8 of Tomita. EX-1003, ¶143. Tomita already discloses having the switch circuits select from a plurality of different input potentials to supply to the gate terminal of the memory cell 15. EX-1005, 17:4-10, 8:41-51; EX-1003, ¶143. The combination would involve no more than implementing Tomita’s switch circuits 6 and 8 each with the circuit of Switching Unit 31 of Nam’s Figure

2, driven by different gate voltages (e.g., VWLSEL1 through VWLSELn) and allowing different drain voltages (e.g., V0 through Vn) to be applied at the output of the switch, as shown in Nam's switching unit 31. EX-1003, ¶143. The gate voltages would be driven by Nam's Decoding Unit 32 (Fig. 2), which correspond to decoder 10 of Tomita. *Id.* Indeed, a switch circuit comprising multiple switches connected at a common node was a "conventional method" used for selecting and driving one of several word line voltages to a memory cell. EX-1010, 2:10-39, 6:29-36, Fig. 2A; §II.D, *supra*.

Implementing Tomita's switch circuits 6 and 8 with the circuit of Switching Unit 31 of Nam's Fig. 2 would require no other changes to Tomita's existing structure. EX-1003, ¶144. The output of the switch circuit 6, for example, would be applied to row decoder 10 and applied to the gate of memory cell 15, in much the same fashion as how the output of Nam's switching unit 31 is supplied via decoding unit 35 to the cell array. EX-1005, 8:11-29, 1:30-42, , 16:53-56, 14:53-59; EX-1006, 3:33-51, Figs. 1-2, 21; EX-1003, ¶144.

3. Analysis

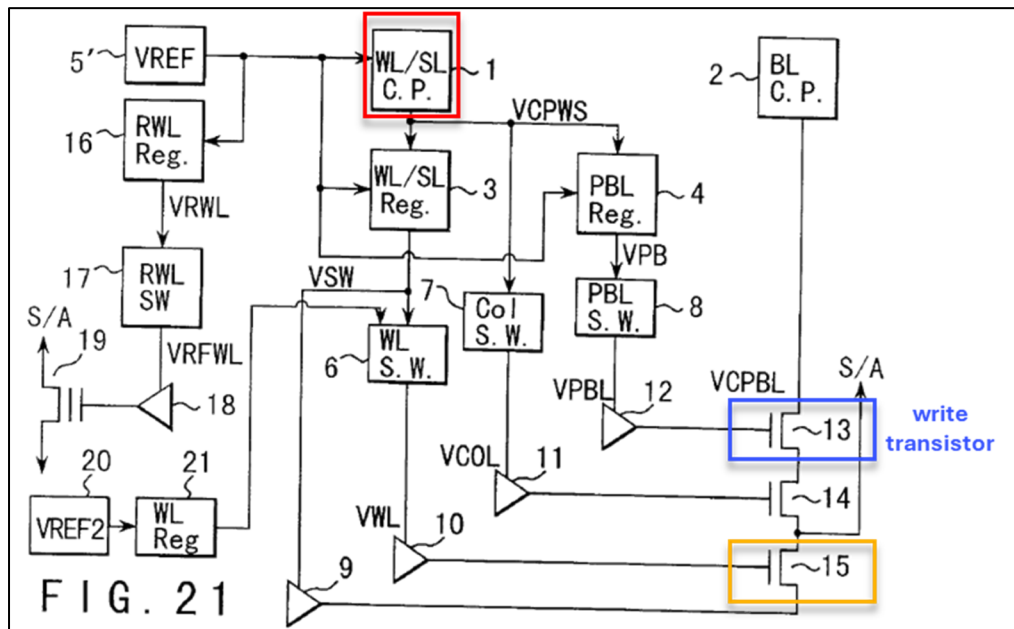
(a) Claim 1

- (i) **1[pre]: A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:**

Tomita discloses 1[pre] as discussed in Ground 1. *See* §VI.A.2(a)(i), *supra*.

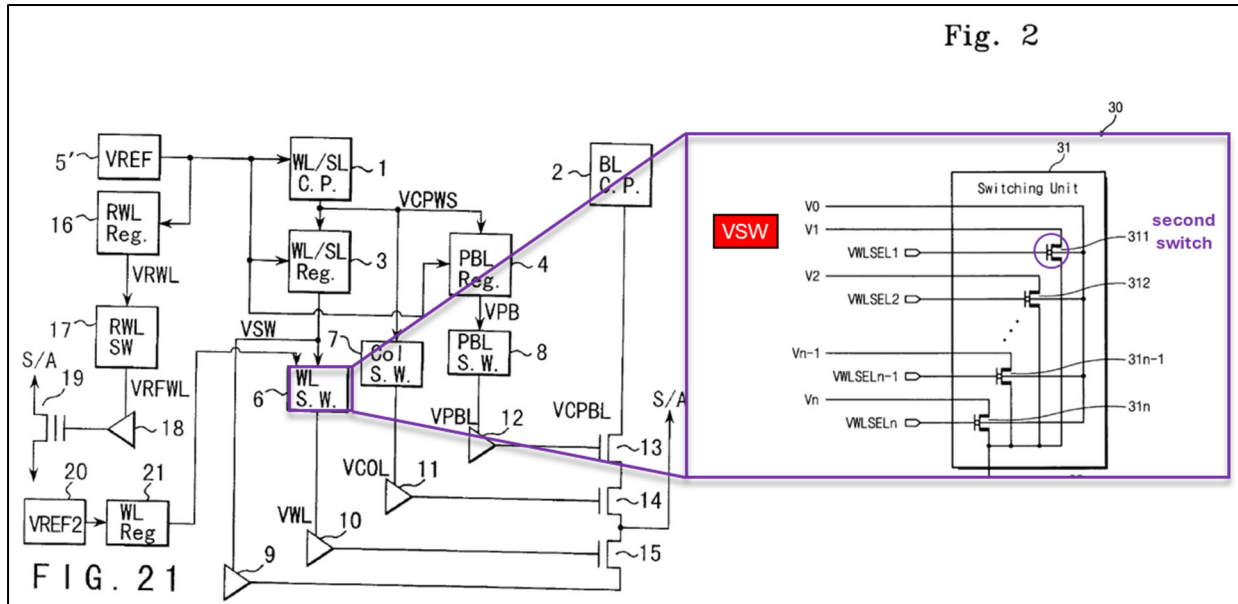
- (ii) 1[a]: the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein

As discussed in Ground 1, Tomita discloses **memory cell 15**, **boost circuit WL/SL C.P.1**, and **write transistor 13**, which are the claimed “memory cell,” “one regulator,” and “voltage applying transistor,” respectively. EX-1005, 7:25-42, 6:49-53, Fig. 2; EX-1003, ¶146. The same description applies to Figure 21. *Id.*, 16:53-59, 14:51-57.



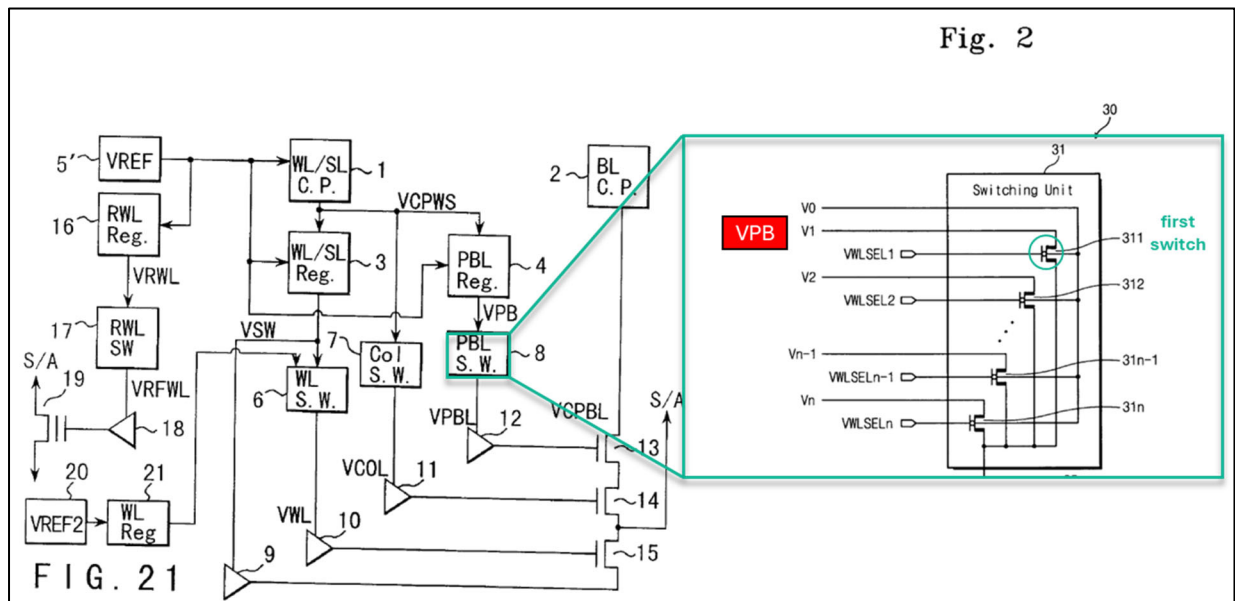
Tomita Fig. 21

In Tomita-Nam, switch circuits 6 and 8 each include a plurality of switches, corresponding to each of the inputs received. EX-1005, 17:4-10, 8:40-49. For example, in switch circuit 6, transistor 311, which may receive the regulator output VSW, is a “**second switch**.” EX-1003, ¶147.



Tomita Fig. 21 (left) and Nam Fig. 2 (right)

Switch circuit 8 would be similarly constructed, and transistor 311 in Tomita's switch circuit 8, which receives VPB, is a "**first switch**." EX-1003, ¶148.



Tomita Fig. 21 (left) and Nam Fig. 2 (right)

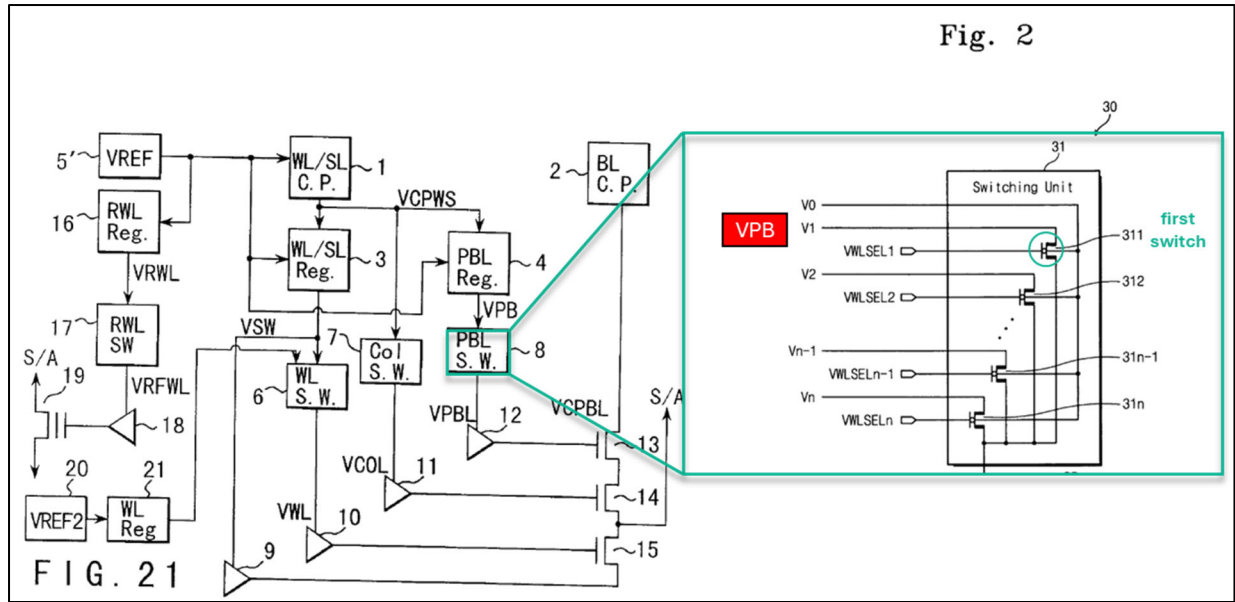
- (iii) 1[b]: an output of the regulator is coupled to inputs of the first and second switches,

In Tomita-Nam, the output VCPWS of **boost circuit WL/SL C.P. 1** (the “regulator”) is coupled to inputs of the **first** and **second** switches in switch circuit 8 and switch circuit 6, respectively, as discussed in 1[a] above. EX-1005, 7:20-24, 7:50-52, 7:63-65; §VI.B.4(a)(ii), *supra*.

As discussed in Ground 1, the presence of intervening components, namely stepdown circuits 3 and 4, does not undermine that the output of the boost circuit 1 (the “regulator”) is “coupled” to inputs of the first and second switches. *See* §VI.A.2(a)(iii), *supra*. And even if the Board finds that *direct* coupling is required between the regulator output and the first and second switches, Tomita-Nam would meet such a requirement because the output VCPWS of the boost circuit 1 (the “regulator”) may be supplied “directly” for gates of transistor 13 and memory cell 15. EX-1005, 7:35-42, 7:54-59; VI.A.2(a)(iii), *supra*. The outputs of stepdown circuits 3 and 4, VSW and VPB, respectively, are therefore each also an “output of the regulator,” coupled to the first and second switches (e.g., transistors 311 from Nam’s Figure 3 in switch circuits 8 and 6, respectively). EX-1003, ¶150.

(iv) 1[c]: an output of the first switch is coupled to a gate of the voltage applying transistor,

Tomita-Nam renders 1[c] obvious because the output VPBL of the “**first switch**” (e.g., transistor 311 in switch circuit 8, *see* §VI.C.3(a)(ii), *supra*) is coupled, via decoder 12, to a gate of **write transistor 13** (the “voltage applying transistor”). EX-1005, 8:41-50; EX-1003, ¶151.



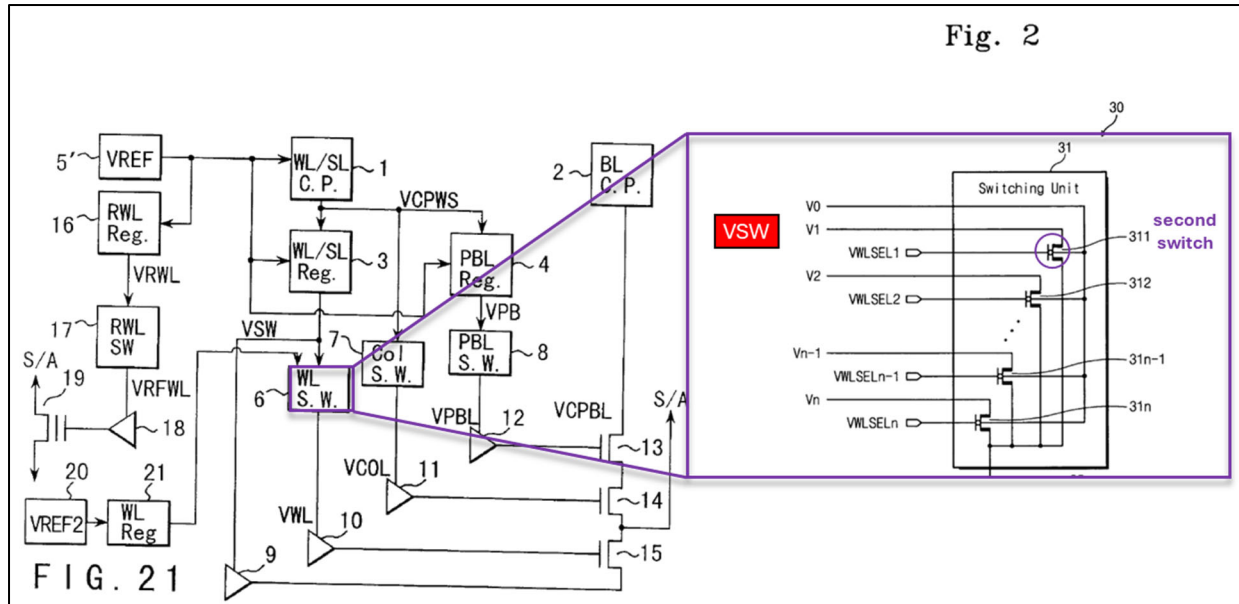
Tomita Fig. 21 (left) and Nam Fig. 2 (right)

- (v) 1[d]: a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and

Tomita discloses 1[d] because, as discussed in Ground 1, **write transistor 13** (the “voltage applying transistor”) applies the voltage it receives from its drain terminal VCPBL to the drain terminal of **memory cell 15**. EX-1003, ¶152; §VI.A.2(a)(v), *supra*.

- (vi) 1[e]: an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

Tomita-Nam renders 1[e] obvious because the output VWL of the “**second switch**” (e.g., transistor 311 in switch circuit 6, *see* §VI.C.3(a)(ii), *supra*) is coupled, via row decoder circuit 10, to a gate of **memory cell 15** for application of a voltage. EX-1005, 8:11-21; EX-1003, ¶153.

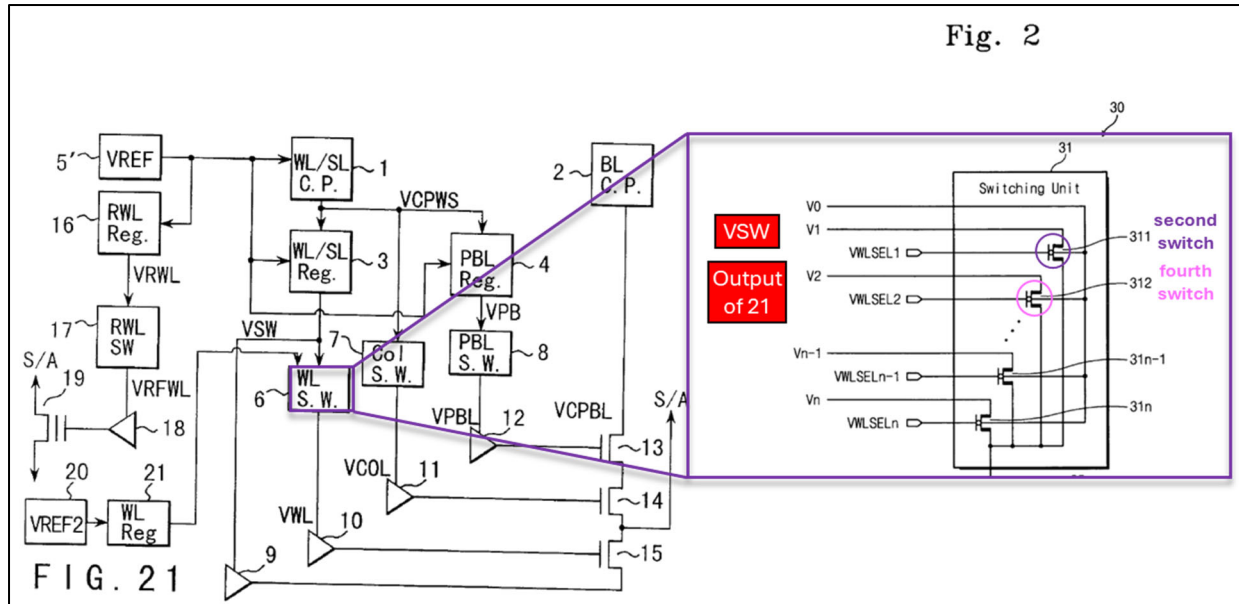


Tomita Fig. 21 (left) and Nam Fig. 2 (right)

(b) Claim 3

- (i) 3[a]: The semiconductor memory device of claim 1, wherein: an output of a fourth switch is coupled to the output of the second switch, and;

Tomita-Nam renders 3[a] obvious. As discussed for 1[a] (*see* §VI.C.3(a)(ii), *supra*), Tomita-Nam’s switch circuit 6 comprises transistors 311 and 312, which supply power sources VSW and the output of stepdown circuit 21, respectively, to memory cell 15. Transistor 312 in switch circuit 6 is a “**fourth switch**,” and its output is coupled to the output of transistor 311 (the “**second switch**”). EX-1003, ¶154; EX-1005, Fig. 21.

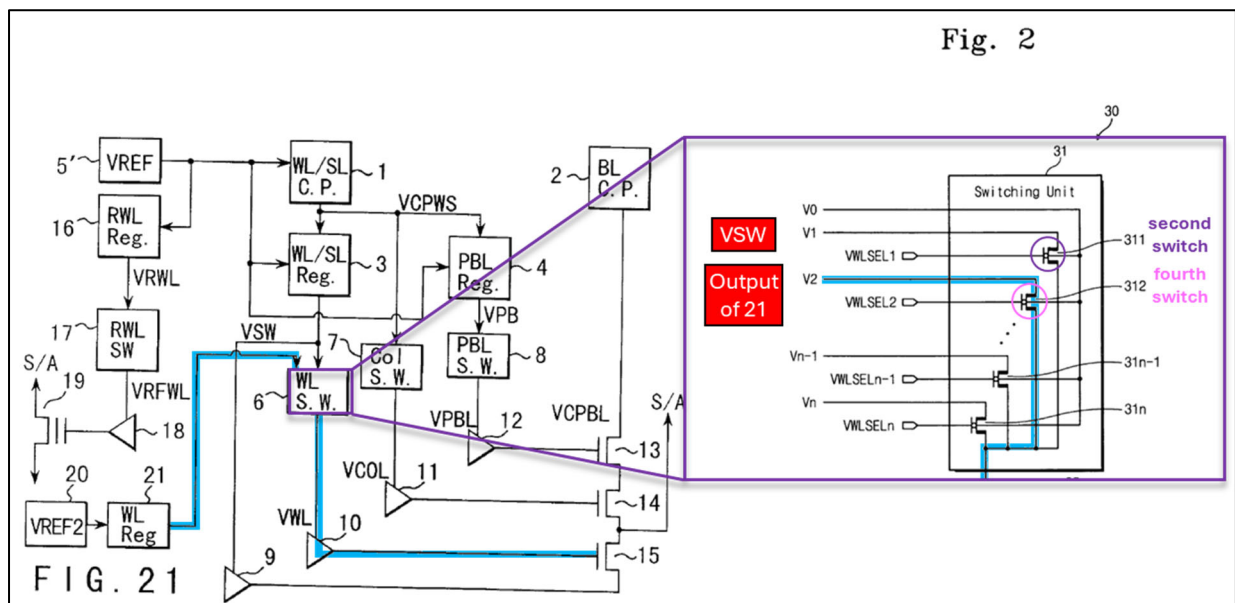


Tomita Fig. 21 (left) and Nam Fig. 2 (right)

- (ii) 3[b]: a voltage different from the output of the regulator is applied to the gate of the memory cell.

Tomita-Nam renders 3[b] obvious. Tomita's switch circuit 6 is "supplied with output potentials of the stepdown circuits 3 and 21 and the power source potential VDD" and "selects and outputs one of the three potentials" based on the state of memory cell 15, such as write, read, erase, and verify. EX-1005, 17:4-10. The output of stepdown circuit 21, for example, is a "voltage different from the output of the regulator." EX-1003, ¶155. As discussed in 1[b] (§VI.C.3(a)(iii), *supra*), VCPWS and VSW are each "the output of the regulator." EX-1005, 7:47-50, 7:54-59; EX-1003, ¶155. Further, Tomita discloses that the Figure 21 embodiment "is arranged to as to independently separate the function of generating a word line potential when reading data, from the stepdown circuit 3" (EX-1005, 17:1-3),

indicating that the voltage of the stepdown circuit 21 is “independently separate” from the other voltages produced for switch circuit 6 to drive the wordline of the memory cell. EX-1003, ¶155. Thus, the output of stepdown circuit 21 is “a voltage different from” the output of the regulator (e.g., VCPWS and VSW). When switch circuit 6 selects and outputs the output of stepdown circuit 21, it is “applied to the gate of the memory cell.” EX-1005, Fig. 21; EX-1003, ¶155.

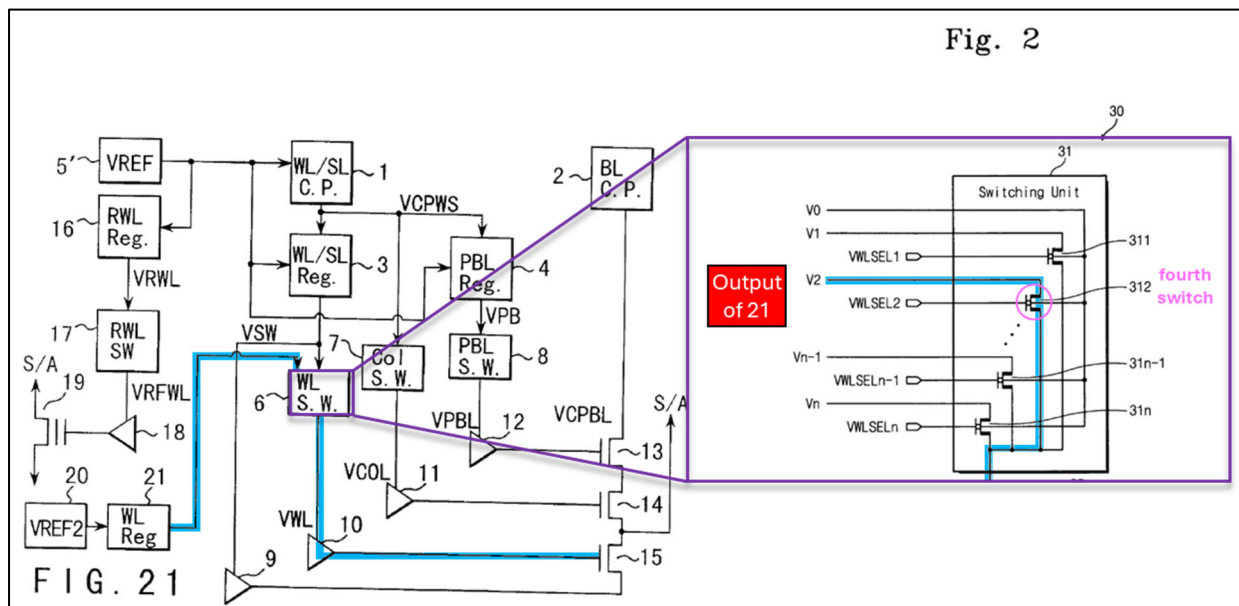


Tomita Fig. 21 (left) and Nam Fig. 2 (right)

(c) Claim 5.

- (i) 5[a][i]:** The semiconductor memory device of claim 3, wherein: in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and;

Tomita-Nam renders 5[a] obvious. *First*, Tomita-Nam discloses that, “in a first operation mode, the first and fourth switches are turned on.” Tomita discloses different modes of operation for the power source circuit, such as a “writing,” “erasing,” “verifying,” and a “reading” mode. EX-1005, 7:30-34, 7:54-59. The reading mode, for example, is a “first operation mode.” In the reading mode, Tomita discloses using low potential generation circuit 20 and stepdown circuit 21 to supply, via switch circuit 6, a voltage of 5V or less to the gate of memory cell 15. *Id.*, 17:1-3, 17:4-14, Fig. 21. Transistor 312 in switch circuit 6 (*i.e.*, the “**fourth switch**”) is therefore turned on, allowing the 5V-potential to be applied to the gate of the memory cell in the reading mode, as shown in blue traces below. EX-1003, ¶156.



Tomita Fig. 21 (left) and Nam Fig. 2 (right)

In the reading mode (a “first operation mode”), transistor 311 in switch circuit 8 (*i.e.*, the “**first switch**”) is also turned on so that cell bit current flows to the



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Application of the regulator's output to the gate of the voltage applying transistor is illustrated in green traces above.

Even if the Board disagrees with Petitioner's proposed construction, Tomita-Nam would still render this limitation obvious. The specification of the '888 Patent describes applying the output voltage of a regulator to the gate of a voltage applying transistor as a means to control a voltage applied to the drain terminal of a memory cell. EX-1001, 4:61-67, 6:45-53, 7:13-22, 8:6-18; EX-1003, ¶159. There is no other embodiment of the '888 patent that would support a claim requirement that the regulator output be supplied to the drain of the memory cell. EX-1003, ¶159. As such, if the Board finds that the embodiments in the specification support the claim language as drafted, because Tomita-Nam discloses applying the regulator output (VCPWS and VPB) to the gate of transistor 13 and as a means to control the application of a voltage to the drain of memory cell 15, Tomita-Nam would meet this limitation. *Id.*

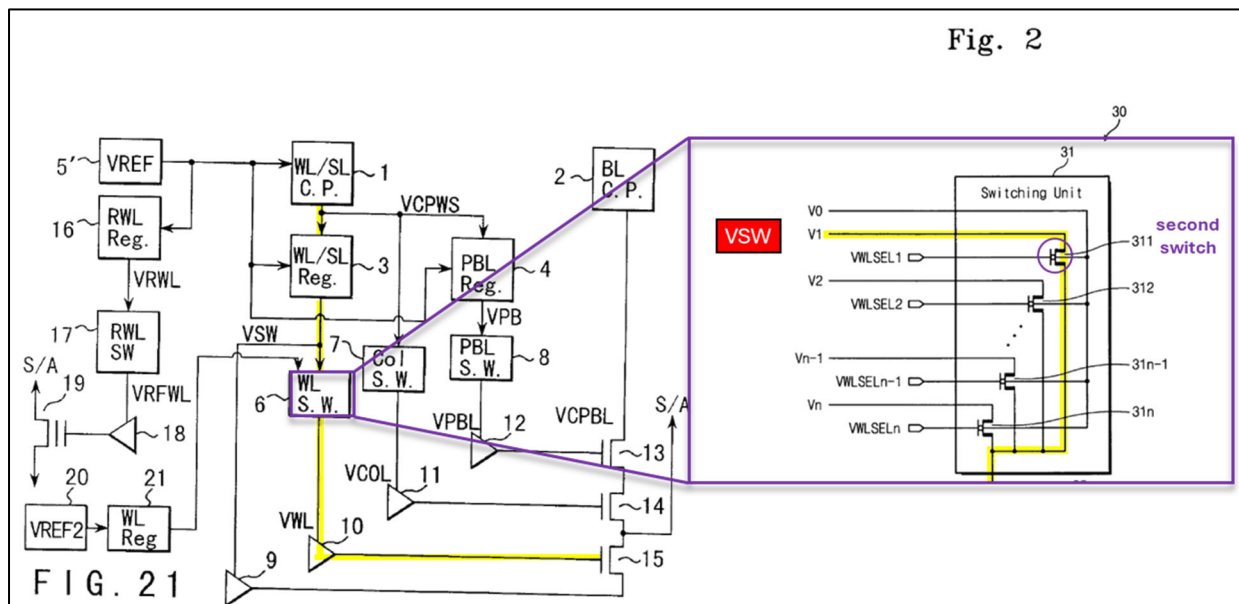
(ii) 5[a][iii] the voltage different from the output of the regulator to be applied to the gate of the memory cell, and

Tomita-Nam renders 5[a][iii] obvious because, as discussed for 3[b], the potential output by stepdown regulator 21, which is limited to 5V or less in the reading mode, is the “voltage different from the output of the regulator to be applied

to the gate of the memory cell” (*i.e.*, memory cell 15). EX-1005, 17:1-3, 17:4-14, Fig. 21; EX-1003, ¶160; §VI.C.3(b)(ii), *supra*.

- (iii) **5[b]: in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.**

Tomita-Nam renders 5[b] obvious. In the writing, erasing, and verify modes, transistor 311 in switch circuit 6 (the “**second switch**”) is turned on, allowing the output voltage VCPWS, and by extension VSW, of boost circuit 1 (the “regulator”) to be applied to the gate of memory cell 15, as illustrated with yellow highlights below. EX-1005, 7:30-34, 7:54-59; EX-1003, ¶161. Accordingly, the writing, erasing, and verifying mode are each a “second operation mode.” In each of these modes, the output voltage of the regulator WL/SP C.P. 1 is applied to the gate of the memory cell, as seen in the highlight below.



Tomita Fig. 21 (left) and Nam Fig. 2 (right)

- (d) Claim 21. The semiconductor memory device of claim 1, wherein an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.**

Tomita-Nam renders claim 21 obvious because, as discussed in Ground 1 (§VI.A.2(b), *supra*), the output of **boost circuit BL C.P. 2** (the “booster circuit”) is “coupled a source terminal” of **write transistor 13** (“the voltage applying transistor”). EX-1005, 6:49-58, Figs. 2-4. 14:51-57, 16:53-59.

D. Ground 4: Nakayama Anticipates Claims 1, 3, 5, and 20-21

1. Overview of Nakayama (EX-1007)

Nakayama is prior art under at least pre-AIA 35 U.S.C. §§102(a)-(b), having been published in August 1989, and thus before the Critical Date. Nakayama was not considered by the Examiner during prosecution of the ’888 Patent.

Nakayama is directed to a non-volatile memory device such as an EEPROM. EX-1007, Abstract. The memory cell in Nakayama’s EEPROM undergoes either an “erase operation” or a “program operation.” EX-1007, 911 (Section II.A). The high level block diagram of Nakayama’s EEPROM is shown in Figure 4, which includes various components such as a high voltage generator, a memory cell array, a row decoder, and a column latch. EX-1007, 912 (Fig. 4). The structure of each component is further shown in Figures 5 and 7. EX-1007, 913 (Sections III.A and III.B).

2. Analysis

(a) Claim 1

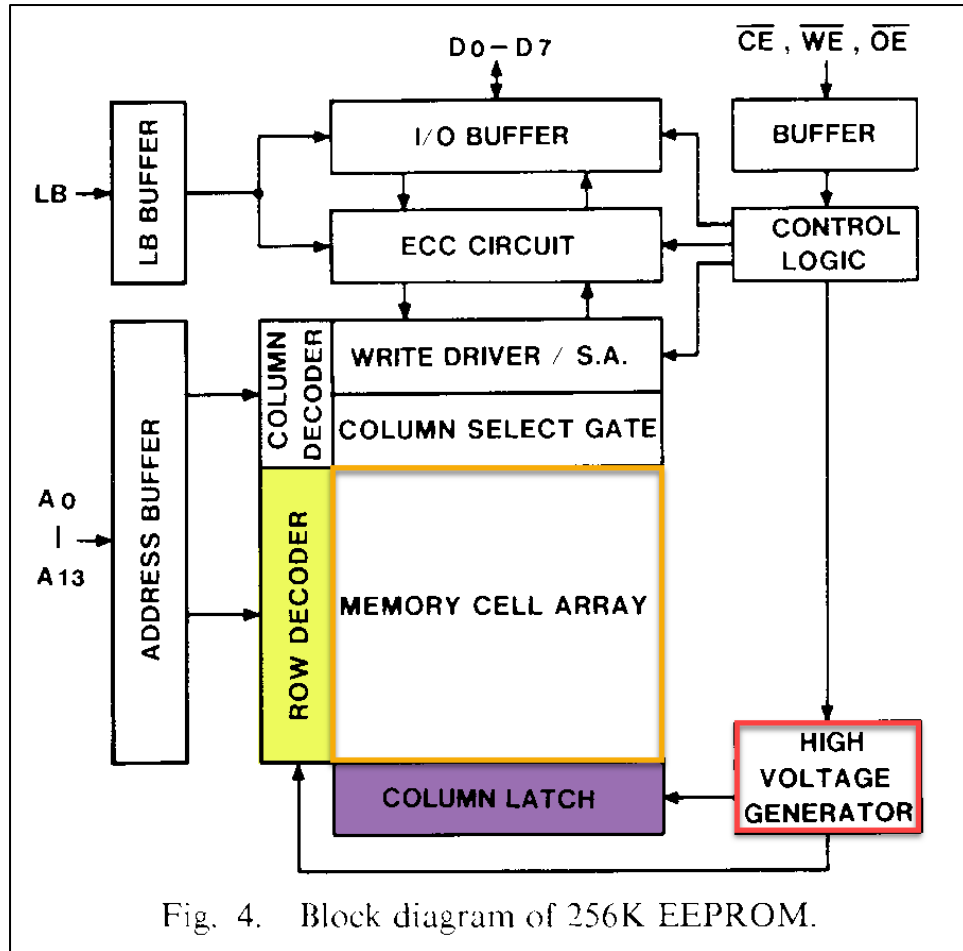
- (i) **1[pre]: A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:**

Nakayama discloses 1[pre] because Nakayama discloses a “256K EEPROM” in which a cell is erased and programmed by the F-N tunneling mechanism. EX-1007, 911 (Abstract), 915; EX-1001, 1:16-21; EX-1003, ¶¶165-167.

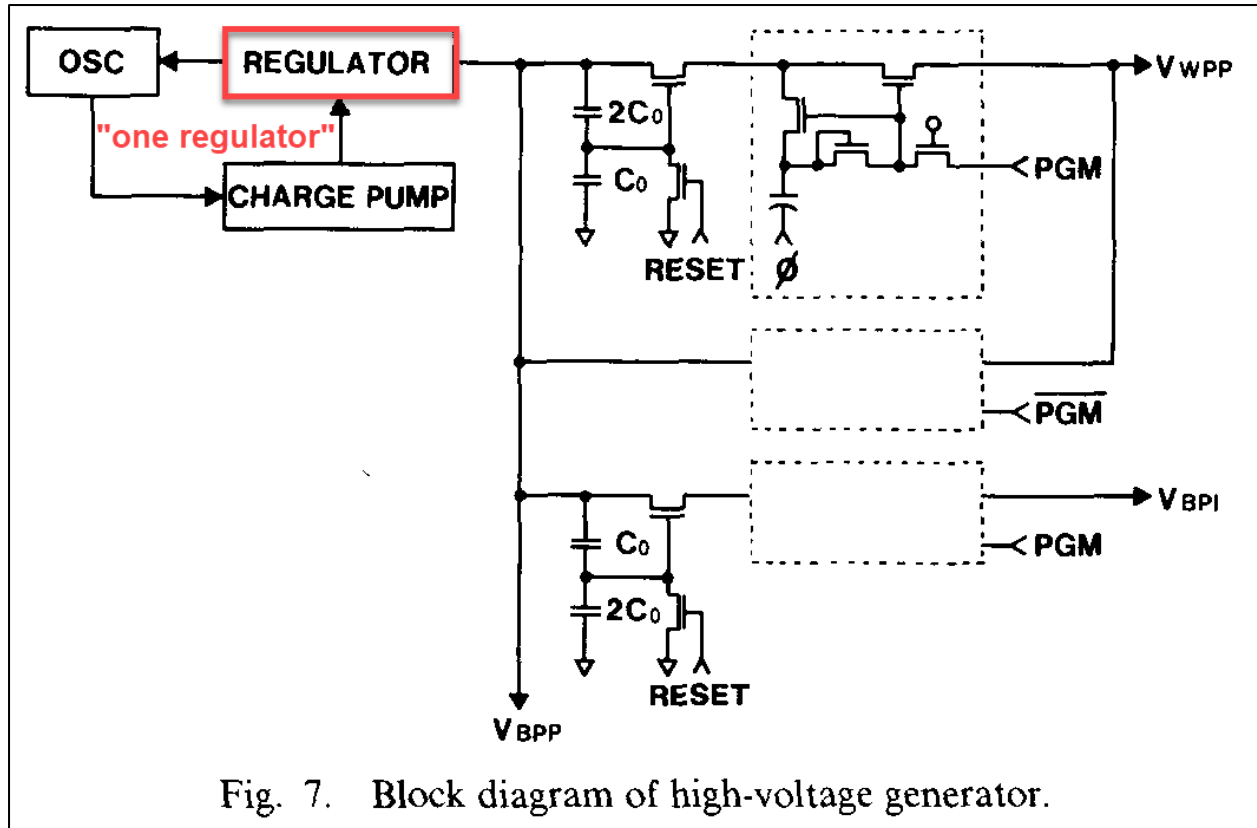
- (ii) **1[a]: the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein**

Nakayama discloses 1[a]. Nakayama shows a block diagram of the 256K EEPROM in Figure 4, reproduced below. Nakayama discloses a memory cell because Nakayama’s EEPROM includes, *inter alia*, a “**memory cell array** [that] consists of 16K words of 16 bits,” a column latch (purple), and a row decoder (yellow). EX-1007, 912 (§III); EX-1003, ¶¶168-169.

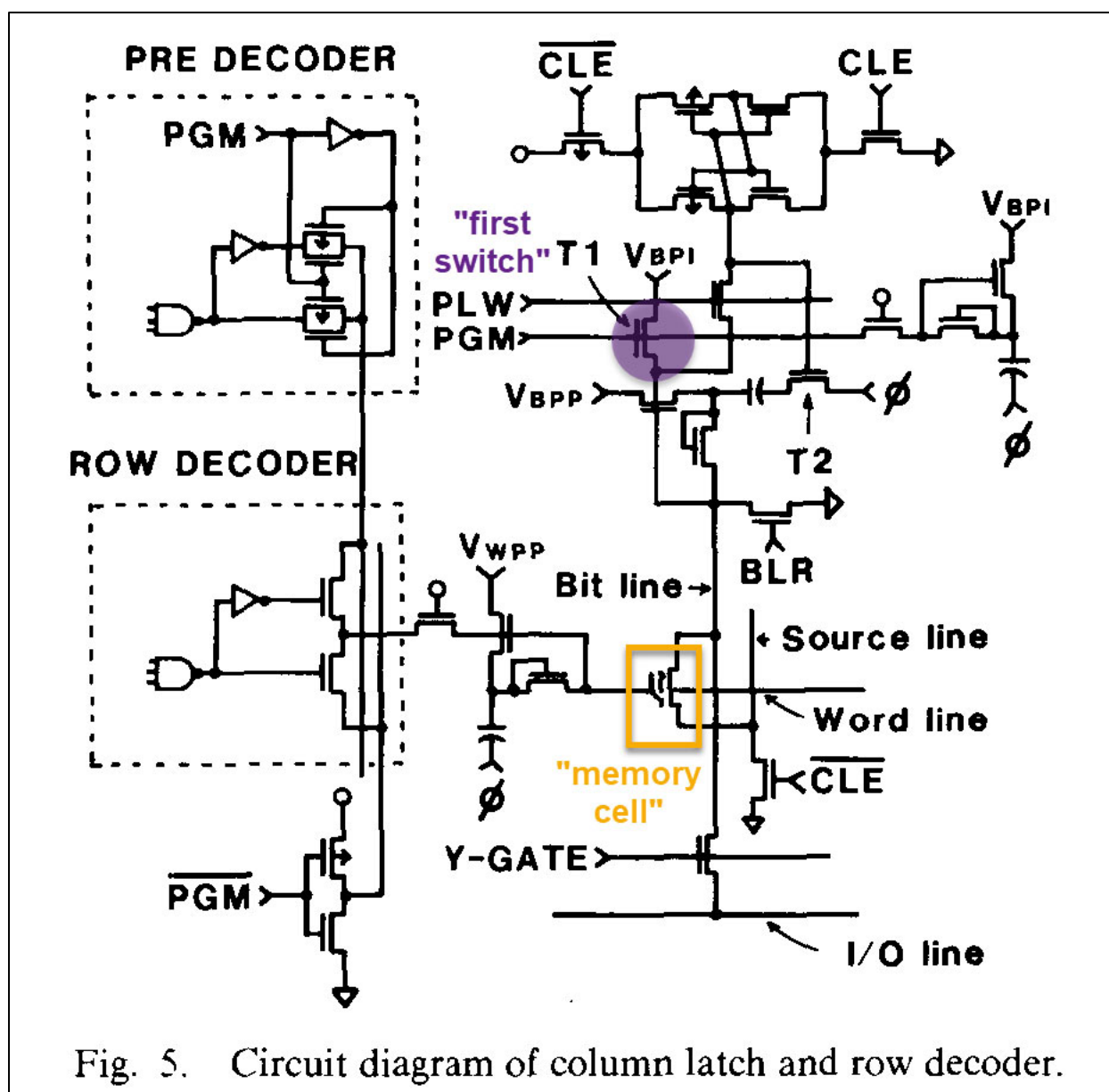
Nakayama’s EEPROM also discloses a “**high-voltage generator** which supplies V_{PP} and program-inhibiting voltages (V_{WPI} , V_{BPI}).” EX-1007, 912 (§III), Fig. 4; EX-1003, ¶170.



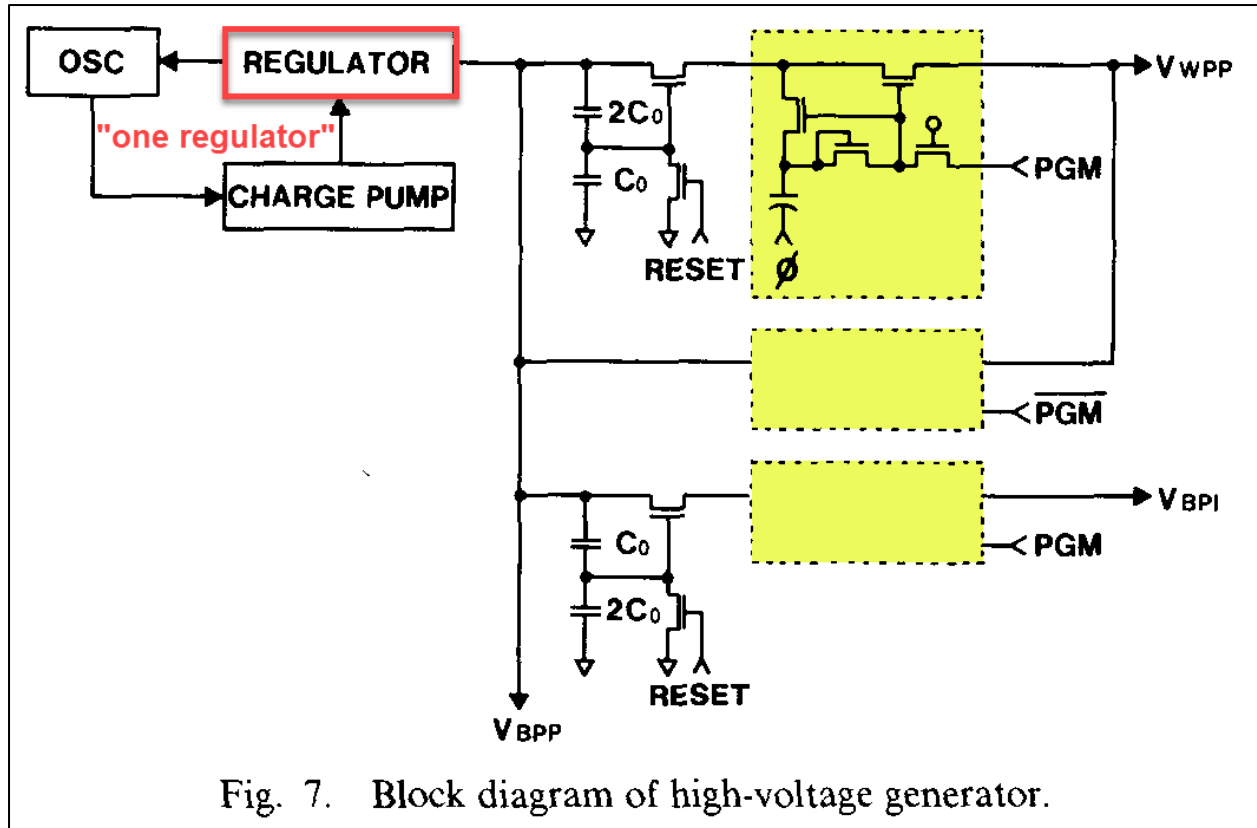
As shown in Nakayama's Figure 7 below, the high-voltage generator circuitry includes **one regulator**. EX-1007, 913 (§III.B); EX-1003, ¶171.



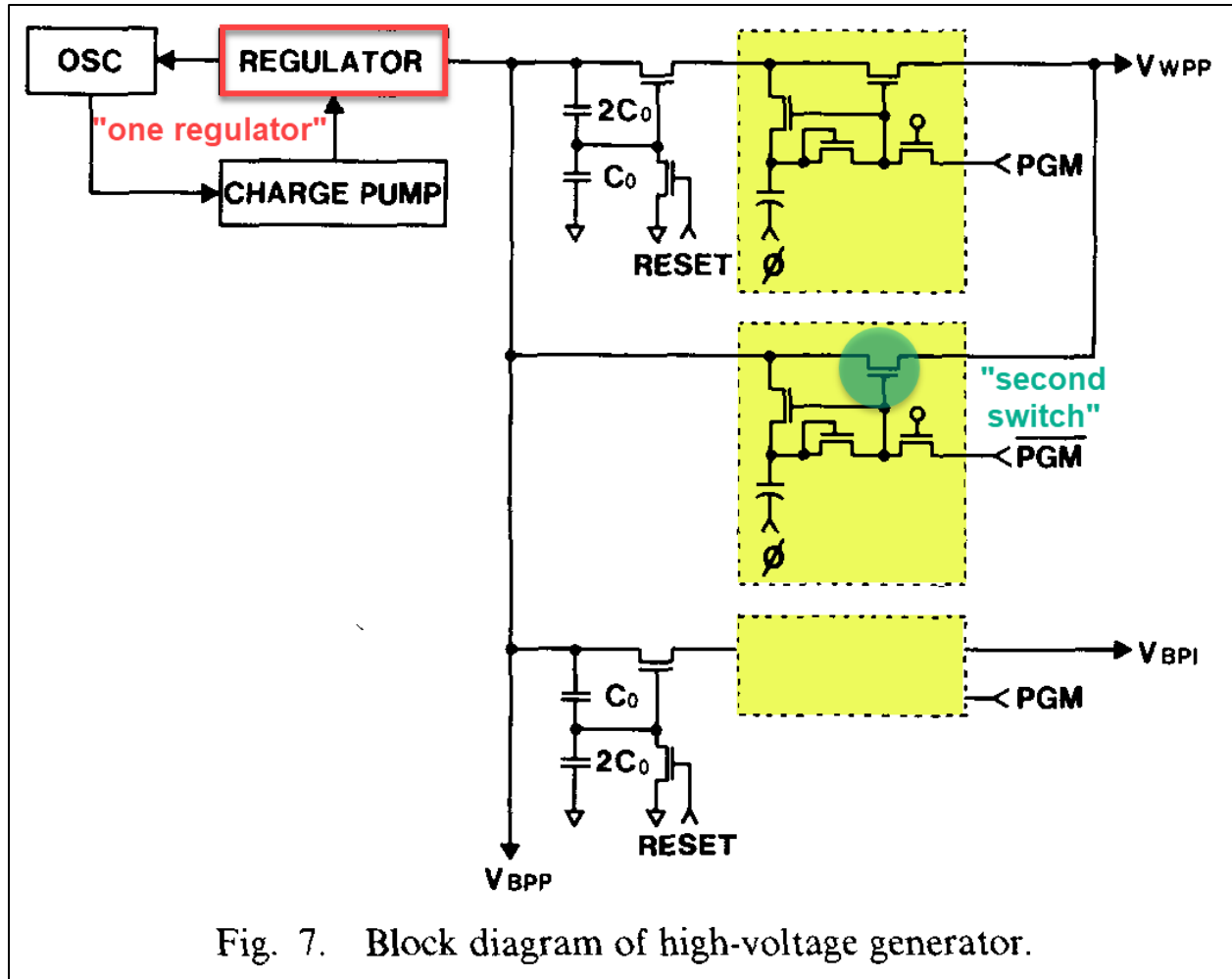
Nakayama's column latch and row decoder circuit (*i.e.*, Figure 5) and high-voltage regulator (*i.e.*, Figure 7) include transistors that act as **switches**. EX-1003, ¶171. For example, in Nakayama's Figure 5, the "**transistor T1**" is a "first switch" operating based on its gate voltage PGM. EX-1003, ¶172.



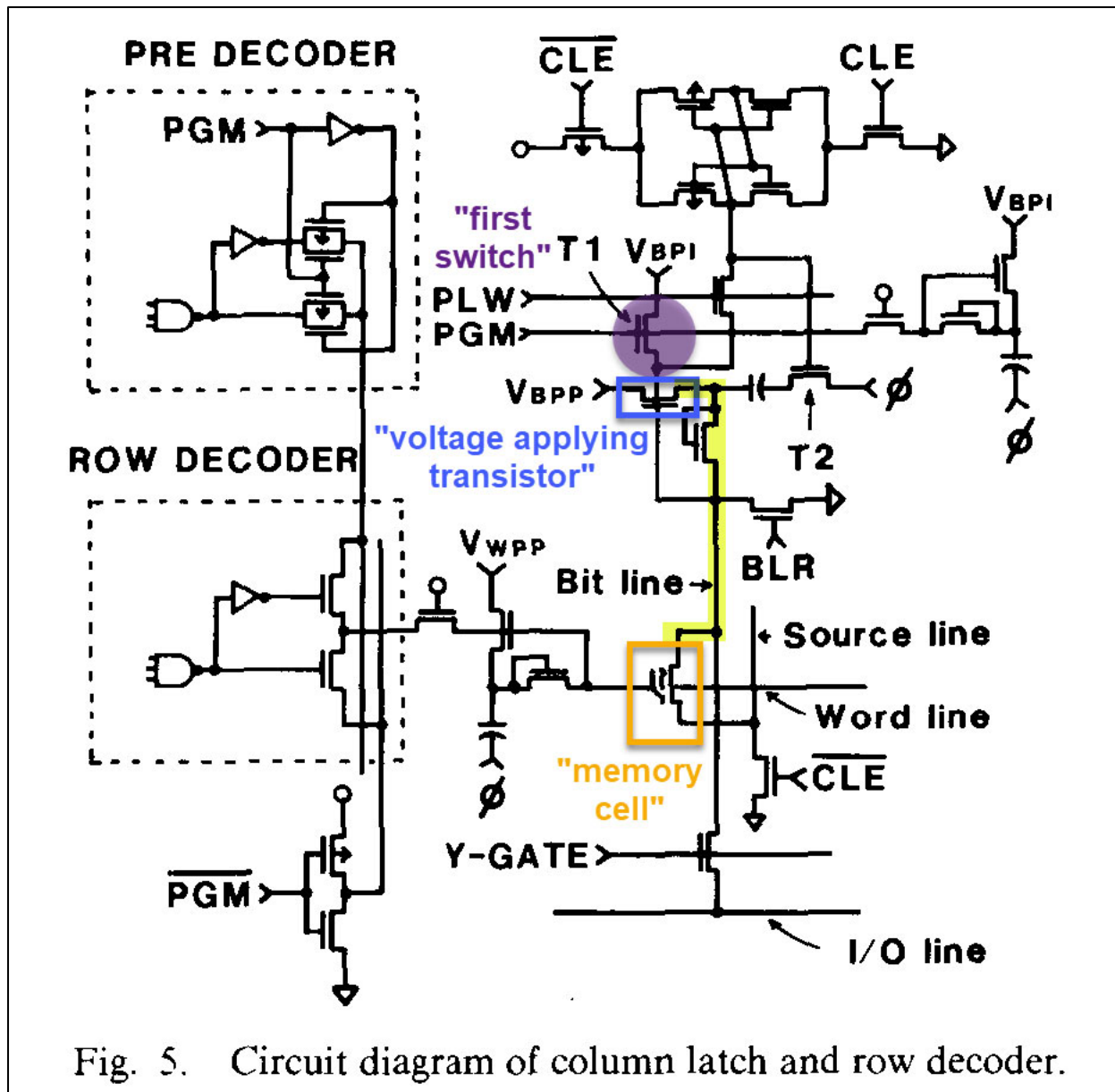
Further, Nakayama's high-voltage generator (Figure 7 below) includes three identical blocks, shown in dotted rectangles. The same circuit diagram shown in the first dotted rectangle is repeated in the second and third dotted rectangles. EX-1007, Fig. 7; EX-1003, ¶173.



In the expanded Figure 7 below, the second dotted rectangle is filled with the same circuitry found in the first dotted rectangle. EX-1003, ¶174. The expanded block diagram for the high-voltage generator includes a **transistor** shown in green, *i.e.*, the claimed “second switch.” *Id.*

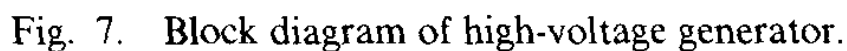


The column latch and memory cell array in Nakayama include a **transistor** shown in blue rectangle, which is a “voltage applying transistor” because, like the voltage applying transistor 205 of the '888 Patent, it applies a voltage to **the memory cell** by transferring the voltage via its channel. EX-1007, Fig. 5; EX-1003, ¶175; *see also*, EX-1001, Figure 2.



- (iii) 1[b]: an output of the regulator is coupled to inputs of the first and second switches,

Nakayama discloses 1[b]. One output of the **regulator** is coupled to the input of the green **transistor** (the “second switch”), as indicated by the yellow-highlighted line. EX-1007, Fig. 7; EX-1003, ¶176.



Further, Nakayama discloses the output of the **regulator** is coupled to the input of **transistor T1** (the “first switch”), via V_{BPI} , as shown in the yellow highlighted line in the two figures below. EX-1003, ¶177. Figure 7 shows that the output of the **regulator** is coupled to V_{BPI} , as shown in the yellow highlighted line:

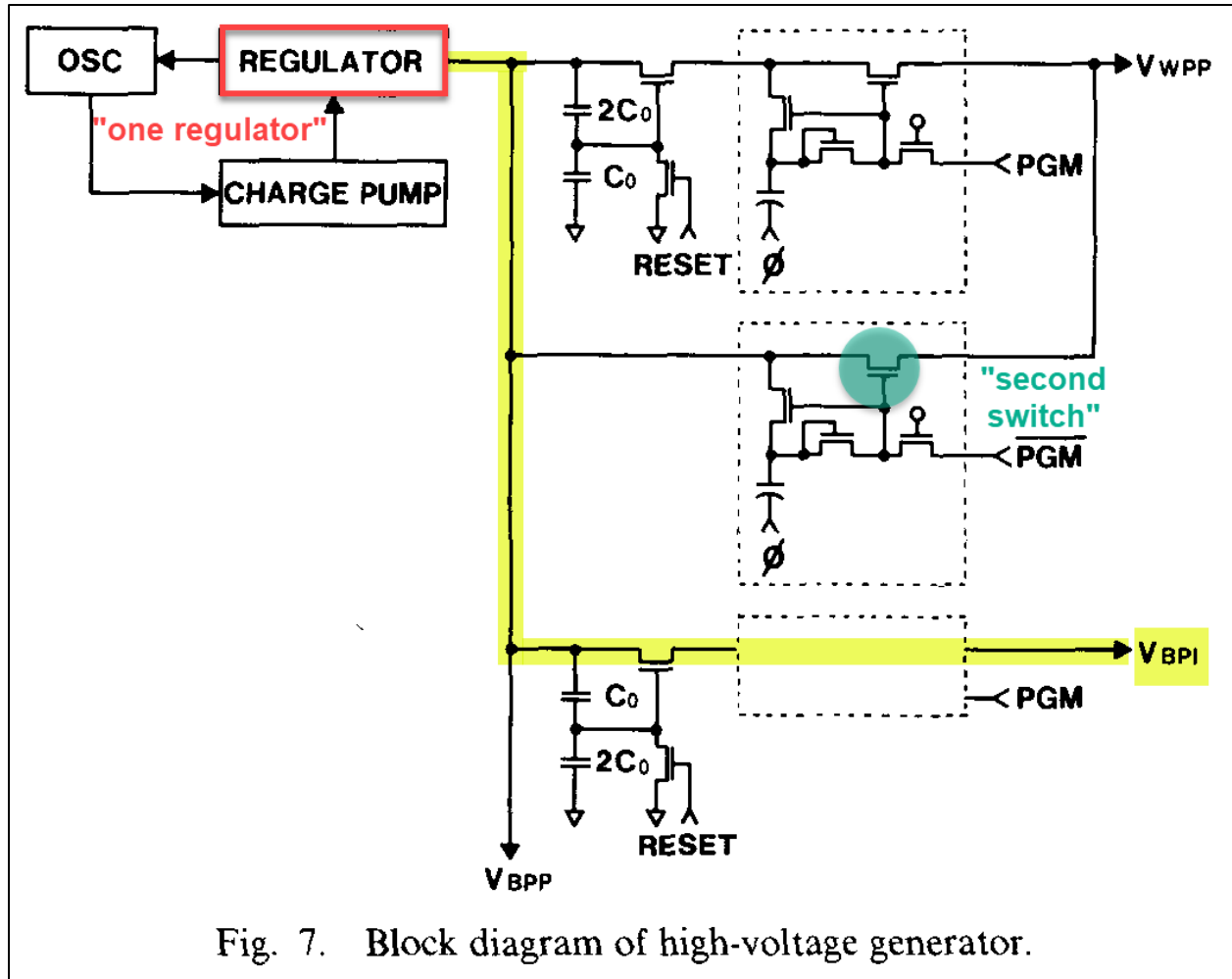
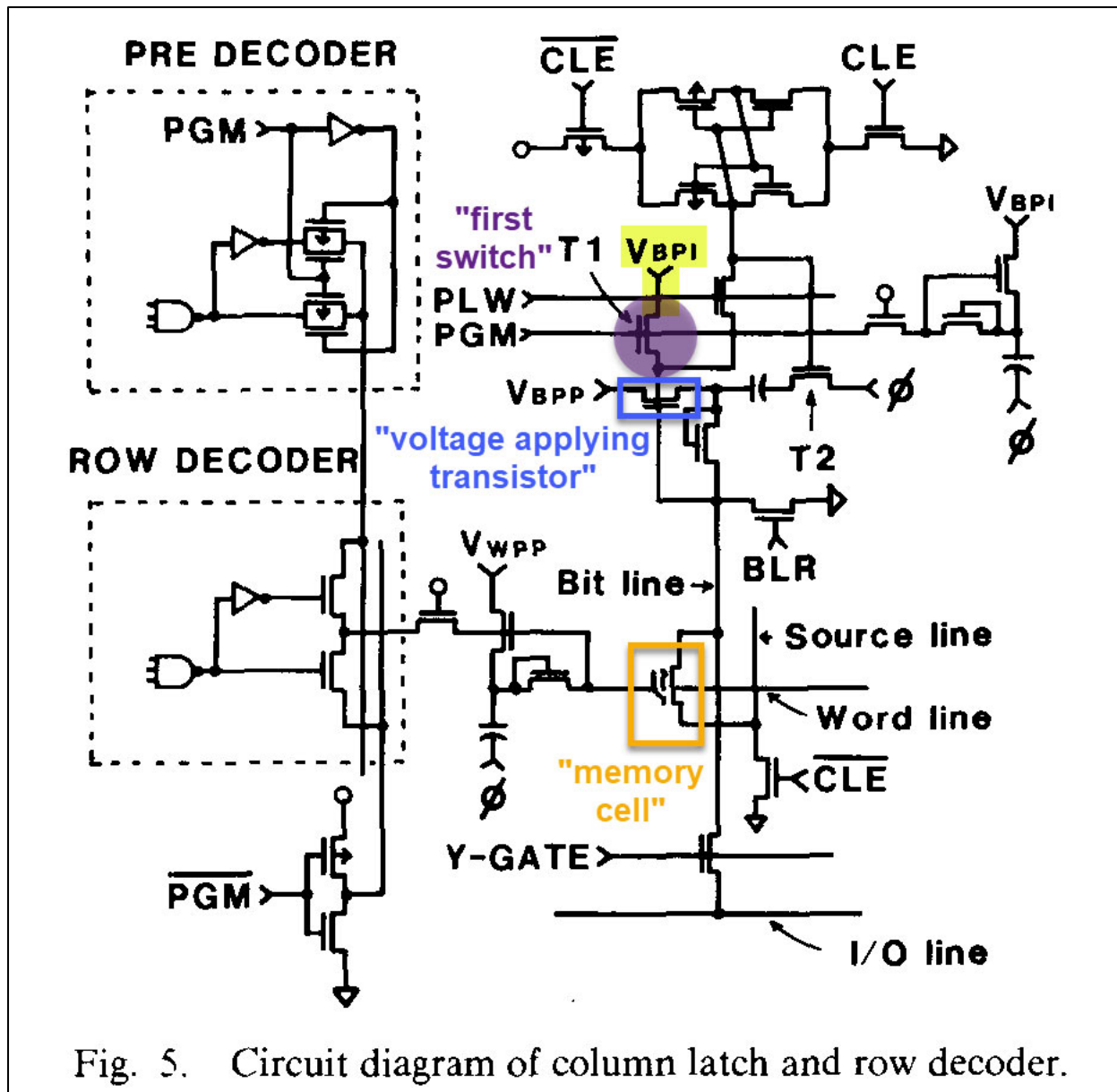


Figure 5 shows V_{BPI} is coupled to the first switch. EX-1003, ¶178.

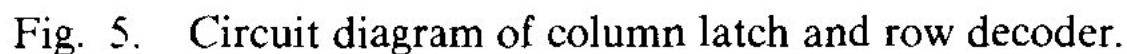


Accordingly, in Nakayama, the output of the regulator is coupled to the inputs of both the purple **transistor T1** in Figure 5 (“first switch”) and the green **transistor** in Figure 7 (“second switch”).

- (iv) **1[c]:** an output of the first switch is coupled to a gate of the voltage applying transistor,

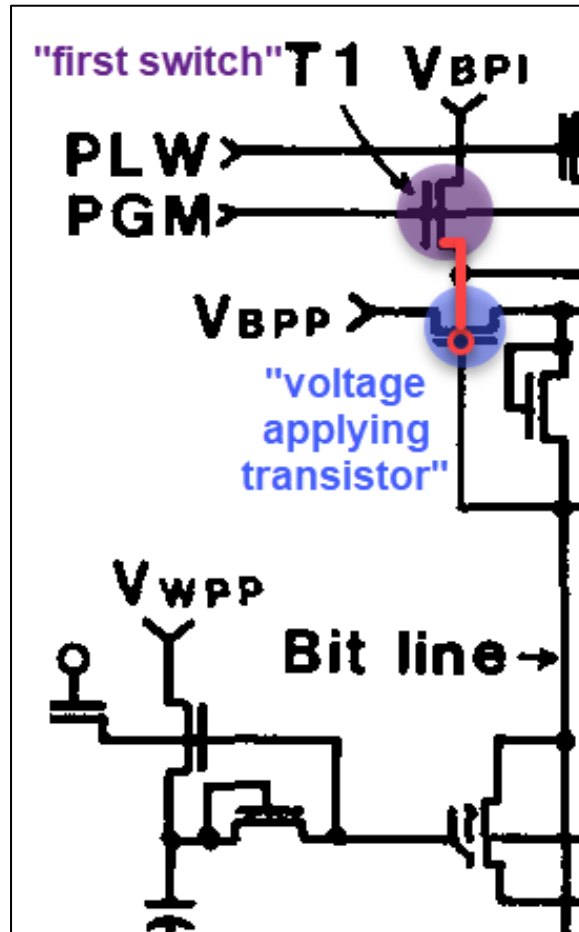
Nakayama discloses 1[c]. The output of **transistor T1** (“first switch”) is

1007, Fig. 5; EX-1003, ¶180.



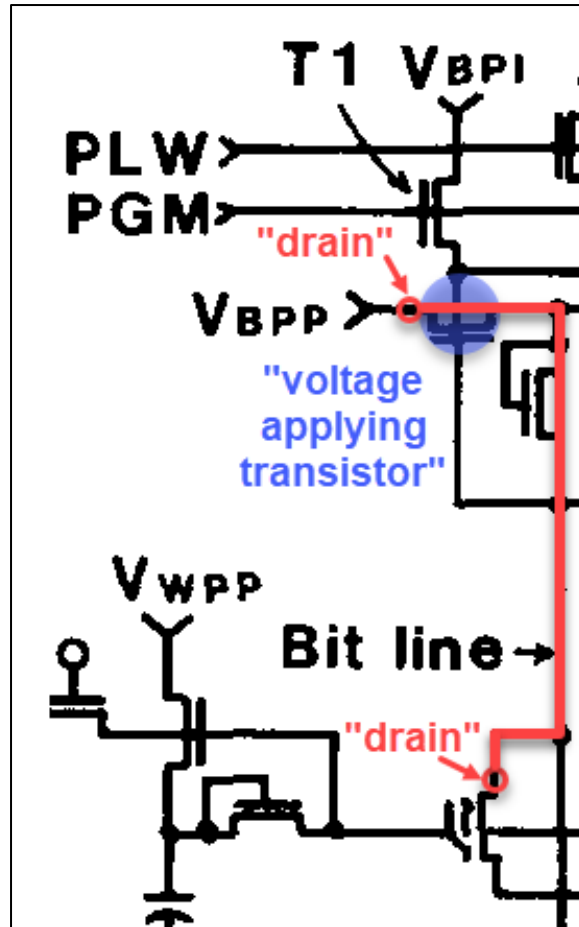
The portion of Figure 5 is magnified below to show its details. Specifically, the output of transistor T1 (the “first switch”), shown in the red line, is coupled to the gate terminal of the blue transistor (the “voltage applying transistor”). EX-1003,

¶181. Accordingly, Nakayama discloses an output of the first switch is coupled to a gate of the voltage applying transistor. *Id.*



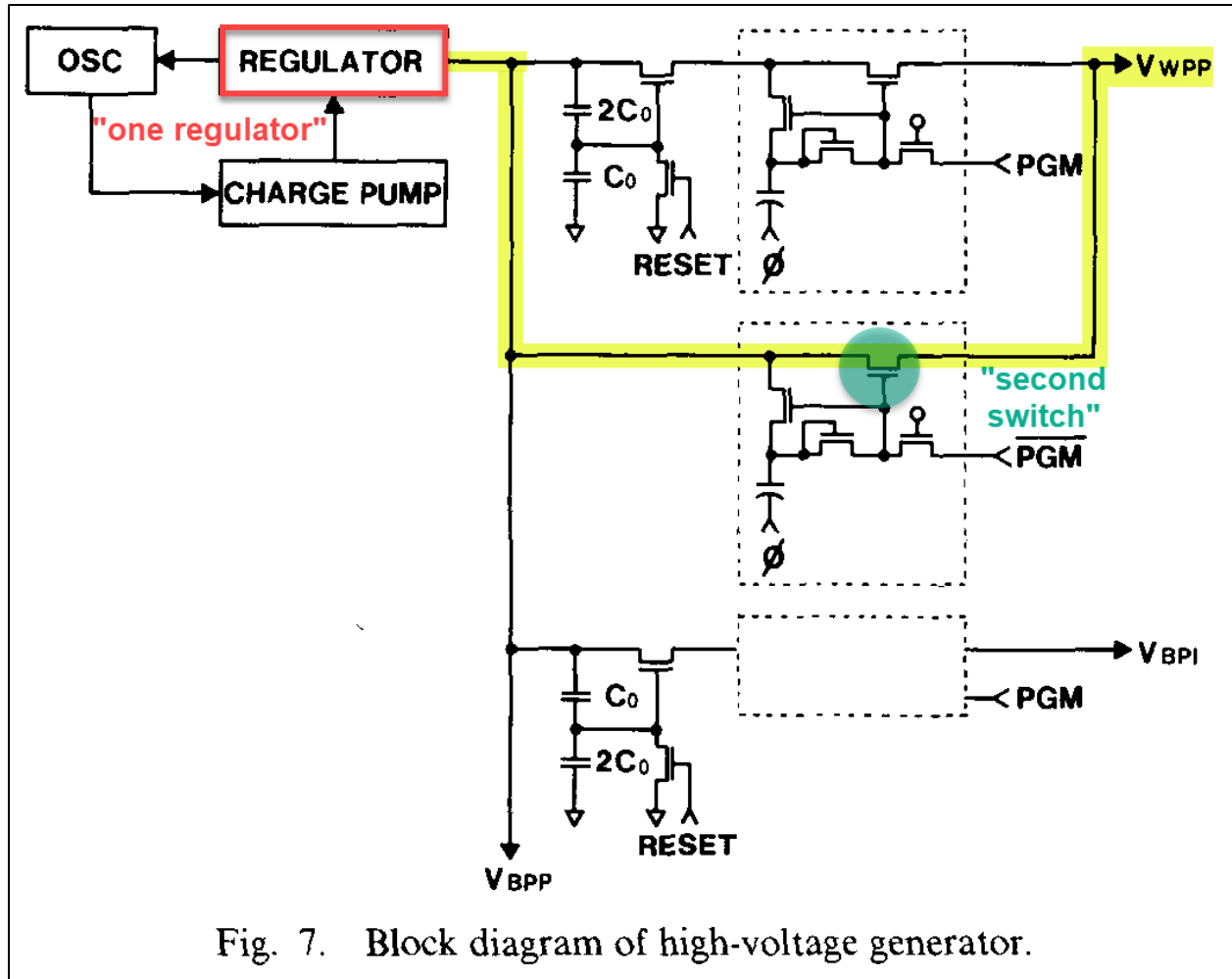
- (v) 1[d]: a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell, and

Nakayama discloses 1[d]. As shown in the red rectangle below, a voltage is applied from a drain terminal of the blue **transistor** ("voltage applying transistor") to a drain terminal of the memory cell. EX-1007, Fig. 5; EX-1003, ¶182.



- (vi) 1[e]: an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

Nakayama discloses 1[e]. An output of the green-highlighted **transistor** in Figure 7 (“second switch”) is V_{WPP} , as shown in the yellow-highlighted pathway below. EX-1007, Fig. 7; EX-1003, ¶184.



Further, the output of the second switch, V_{WPP} , is coupled to a gate of the memory cell. EX-1007, 913 (§III.B), Fig. 5. The word line voltage (V_{WPP}) is applied to the gate terminal of the memory cell via the channels of two transistors shown in yellow highlight. EX-1003, ¶185.

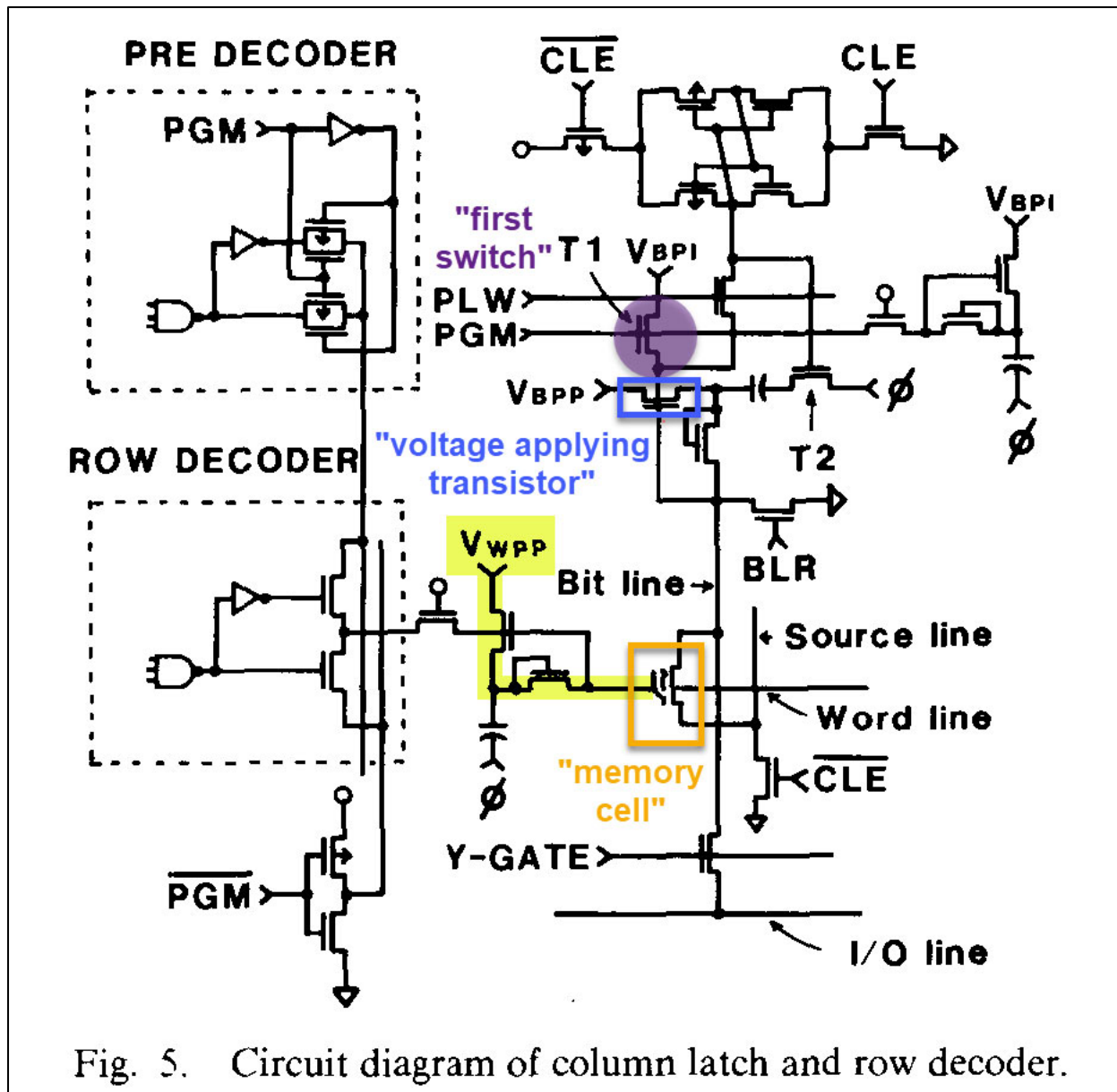


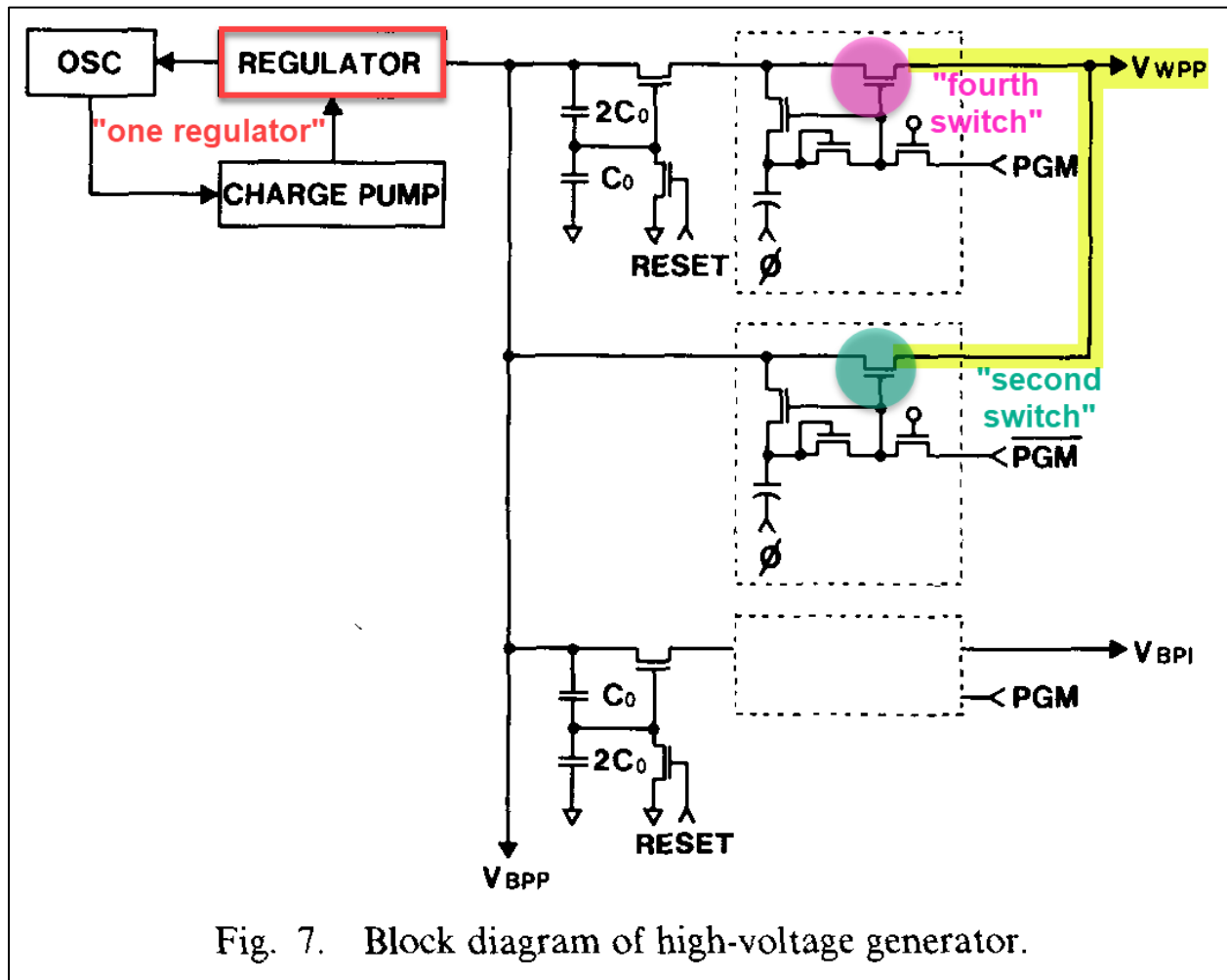
Fig. 5. Circuit diagram of column latch and row decoder.

(b) Claim 3

- (i) 3[a]: The semiconductor memory device of claim 1, wherein an output of a fourth switch is coupled to the output of the second switch, and;

As discussed above for 1[e], Nakayama discloses that the output of the green transistor ("the second switch") is V_{WPP} . Nakayama also discloses a magenta transistor ("a fourth switch") whose output is labeled V_{WPP} . EX-1007, Fig. 7; EX-

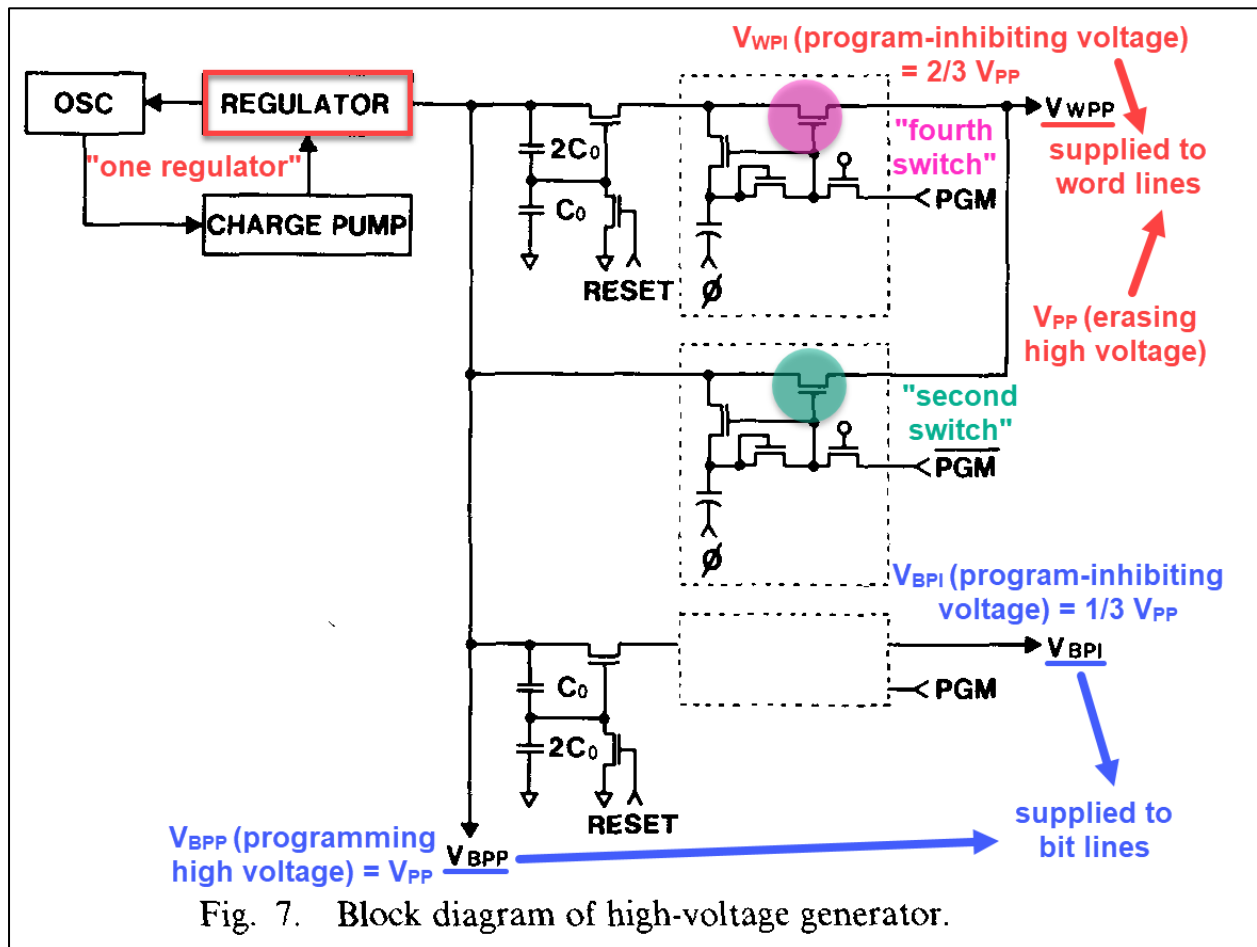
1003, ¶186. Accordingly, Nakayama discloses that the output of the fourth switch is coupled to the output of the second switch, as shown in the yellow-highlighted pathways below.



- (ii) 3[b]: a voltage different from the output of the regulator is applied to the gate of the memory cell.

Nakayama discloses that the output V_{PP} of the regulator in Figure 7 is used to derive the bit line supply voltages and word line supply voltages. EX-1007, 912 (Section III) (“[a] high-voltage generator which supplies V_{PP} ”); EX-1003, ¶187. As

Nakayama explains, “[a]ll high voltages, V_{BPP} , V_{WPP} , and V_{BPI} , are generated internally. V_{BPP} (programming high voltage, V_{PP}) and V_{BPI} (program-inhibiting voltage, $1/3 V_{PP}$) are applied to bit lines and V_{WPP} is applied to word lines. V_{WPP} has two different voltage levels that correspond to V_{PP} (erasing high voltage) and V_{WPI} (program-inhibiting voltage, $2/3 V_{PP}$).” EX-1007, 913 (Section III.B).



Nakayama’s PGM signal in Figure 7 is either active-high (“PGM”) or active-low (“ $\overline{\text{PGM}}$ ”). EX-1003, ¶188. In particular, when PGM is set to “L,” the green **transistor** is turned on, the erasing high voltage of V_{PP} is supplied to the word line

as V_{WPP} . *Id.* On the other hand, when PGM is set to “H,” the magenta transistor is turned on, the program-inhibiting voltage of $2/3 V_{PP}$ is supplied to the word line as V_{WPP} . *Id.* Nakayama illustrates this behavior in the signal diagram in Figure 6, which has been highlighted in like colors to show the switch that has been turned on. EX-1007, Fig. 6.

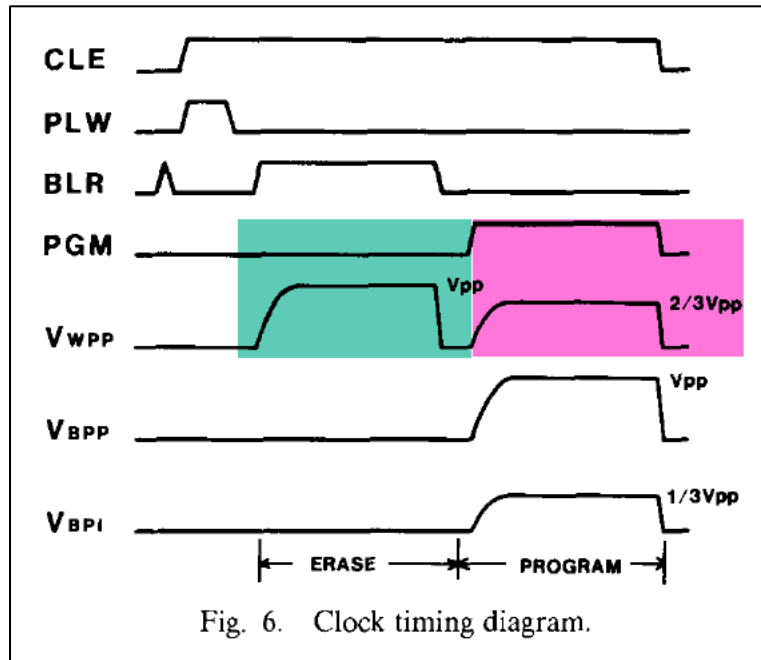
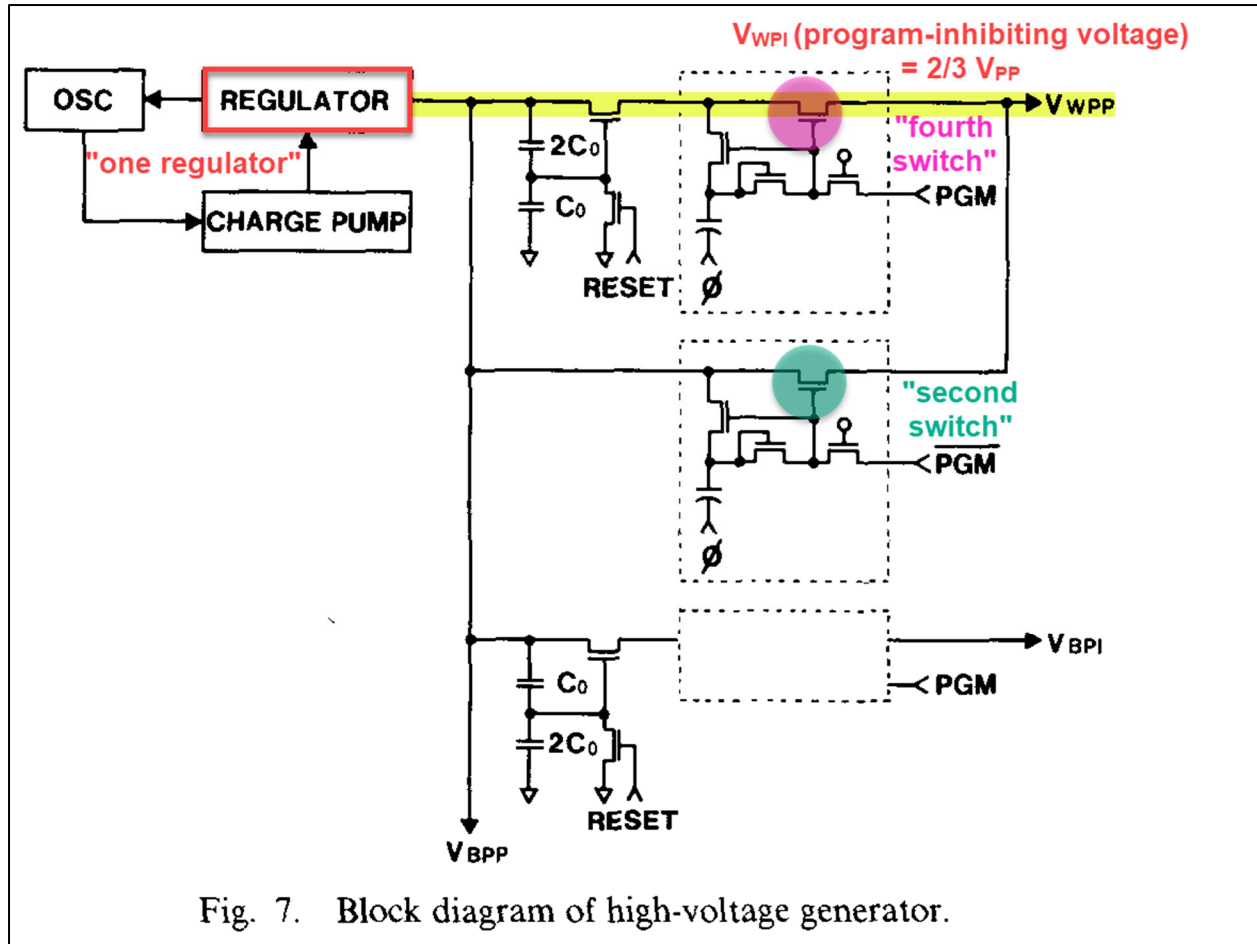
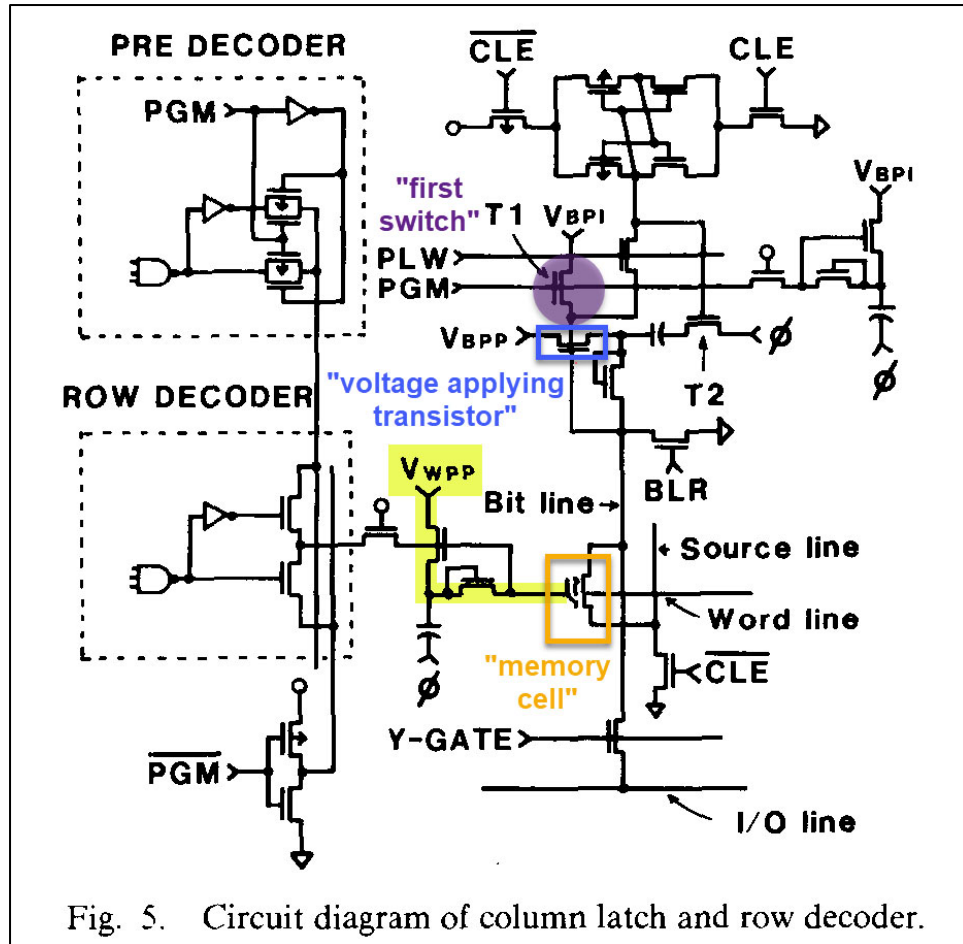


Fig. 6. Clock timing diagram.

As such, when the magenta transistor is turned on, the word line supply voltage ($2/3 V_{PP}$) is “a voltage different from the output of the regulator” (V_{PP}). EX-1003, ¶189. This voltage is applied to the gate of the memory cell as V_{WPP} , as shown by the yellow-highlighted pathway spanning Figures 7 and 5 below.



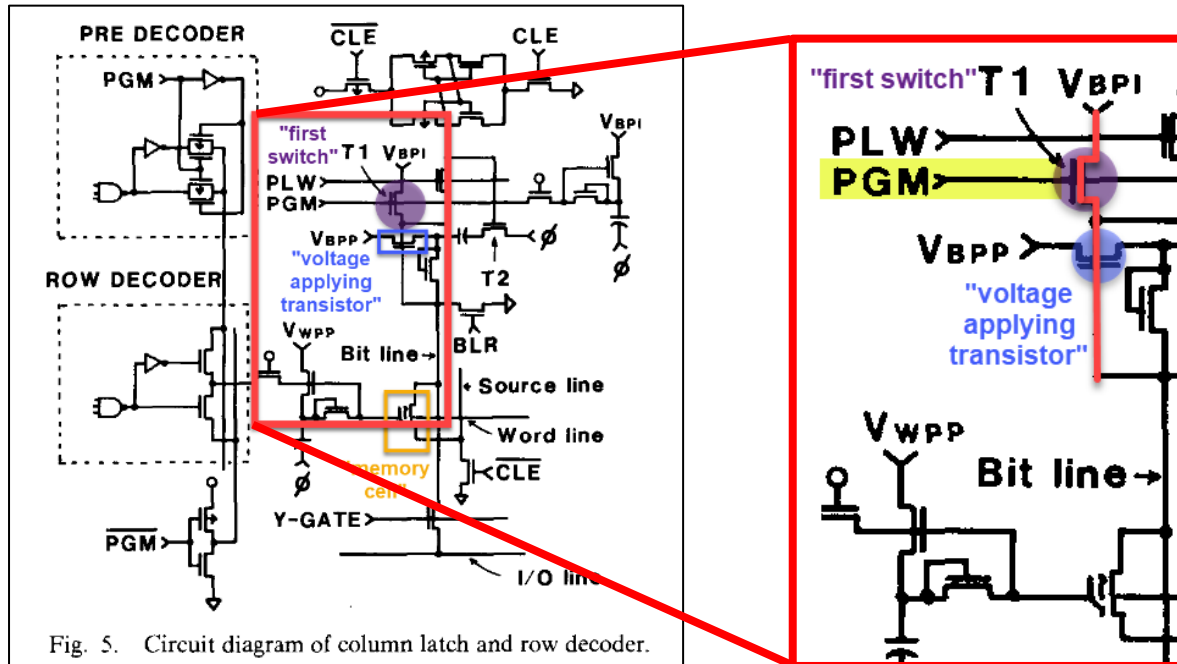


(c) Claim 5

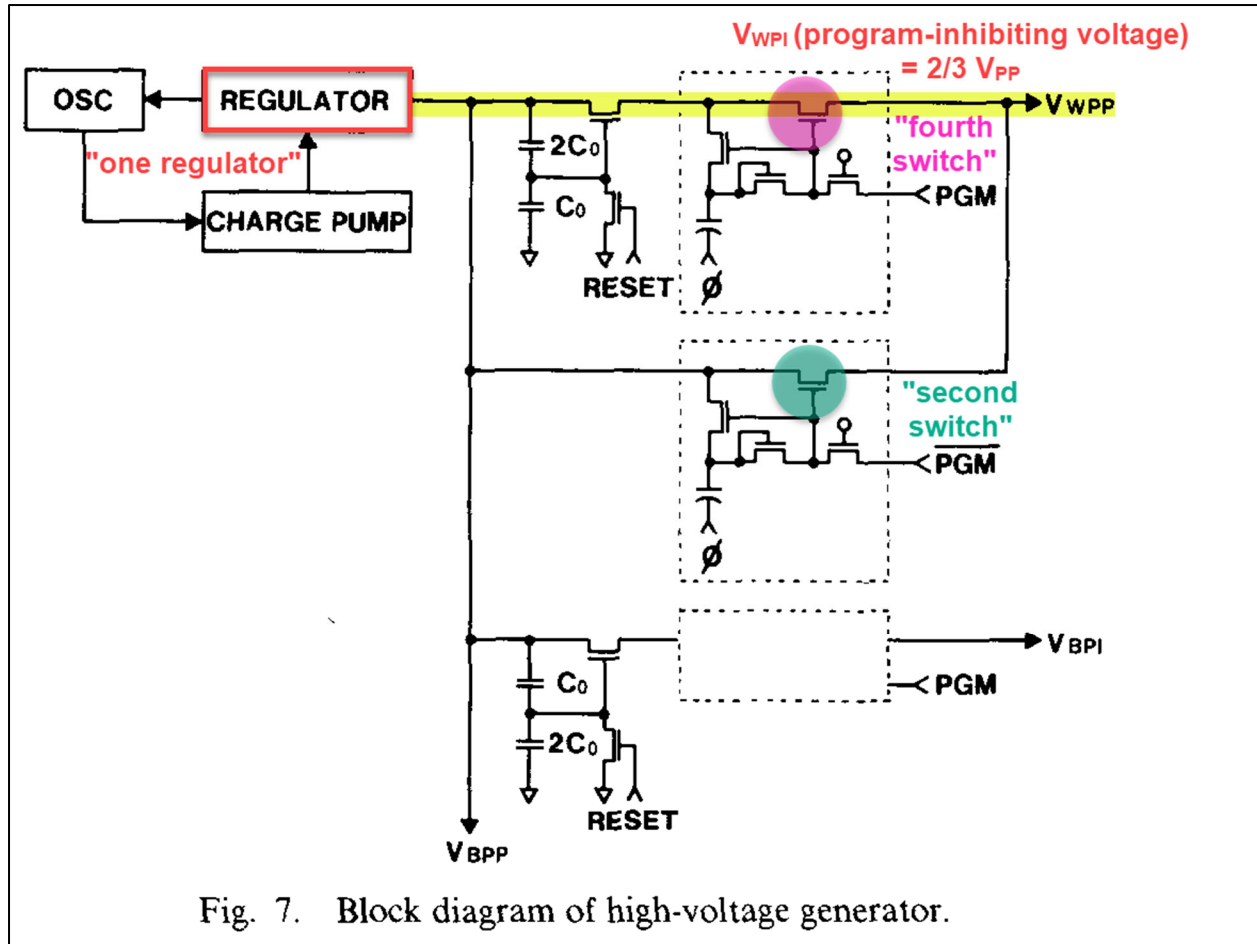
- (i) 5[a][i]: The semiconductor memory device of claim 3, wherein: in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and;

To the extent the Board disagrees with Petitioner's proposed claim construction of 5[a][i] (§V, *supra*), Nakayama discloses this limitation. Nakayama discloses a first operation mode when PGM is set to high ("H"). EX-1007, 913 (§III.A) ("In a **program operation**, as PGM is set to 'H,' all bit lines are precharged

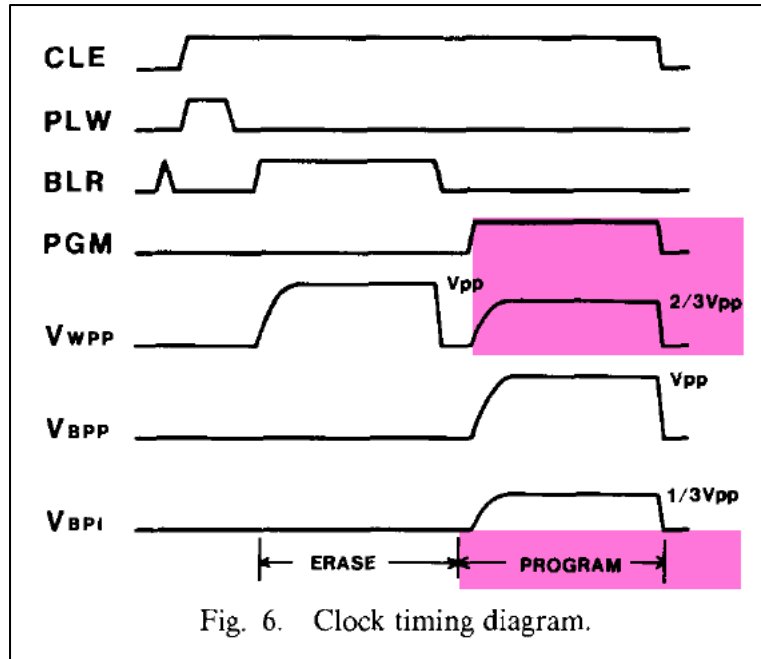
to V_{BPI} through a transistor T1”). In this “program operation” mode, **transistor T1** (*i.e.*, the “first switch”) is turned on. *Id.*; EX-1003, ¶190. As a result, the blue **transistor** (*i.e.*, the “voltage applying transistor”) is turned on. EX-1003, ¶__.



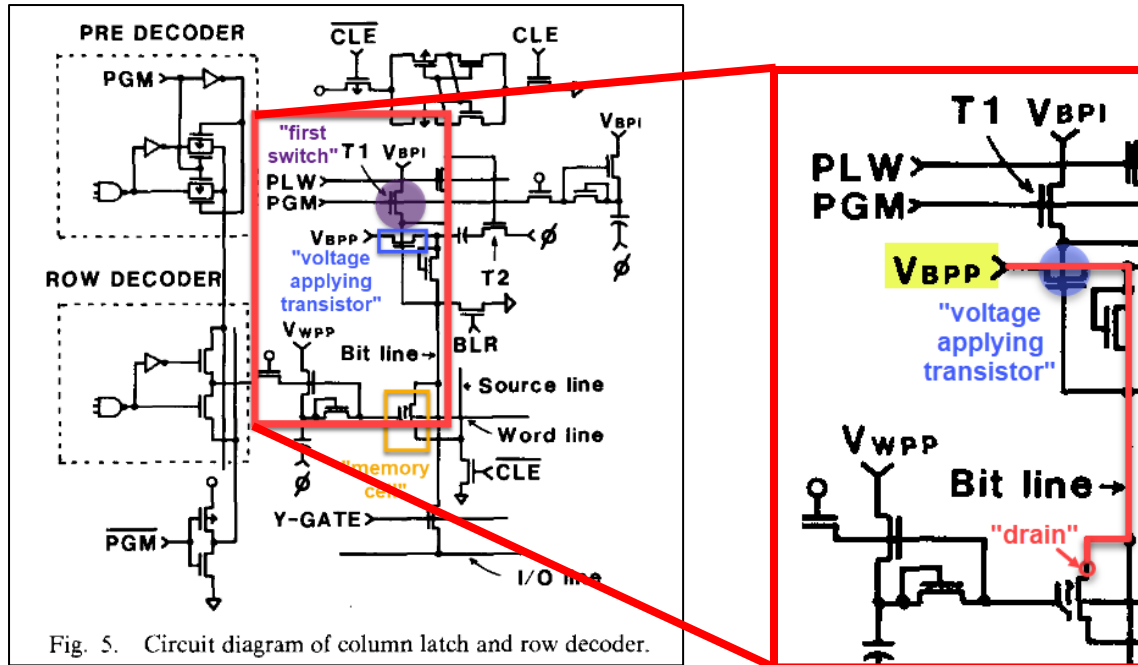
Likewise, in this “program operation” mode, the magenta **transistor** (the “fourth switch”) in Figure 7 is also turned on. EX-1007, Fig. 7; EX-1003, ¶191.



The signal diagram of Figure 6 shows the V_{WPP} supply voltage to the word line is set to V_{WPI} (at $2/3 V_{PP}$), which further supports that the magenta transistor is turned on in the program mode. EX-1007, Fig. 6; EX-1003, ¶192.



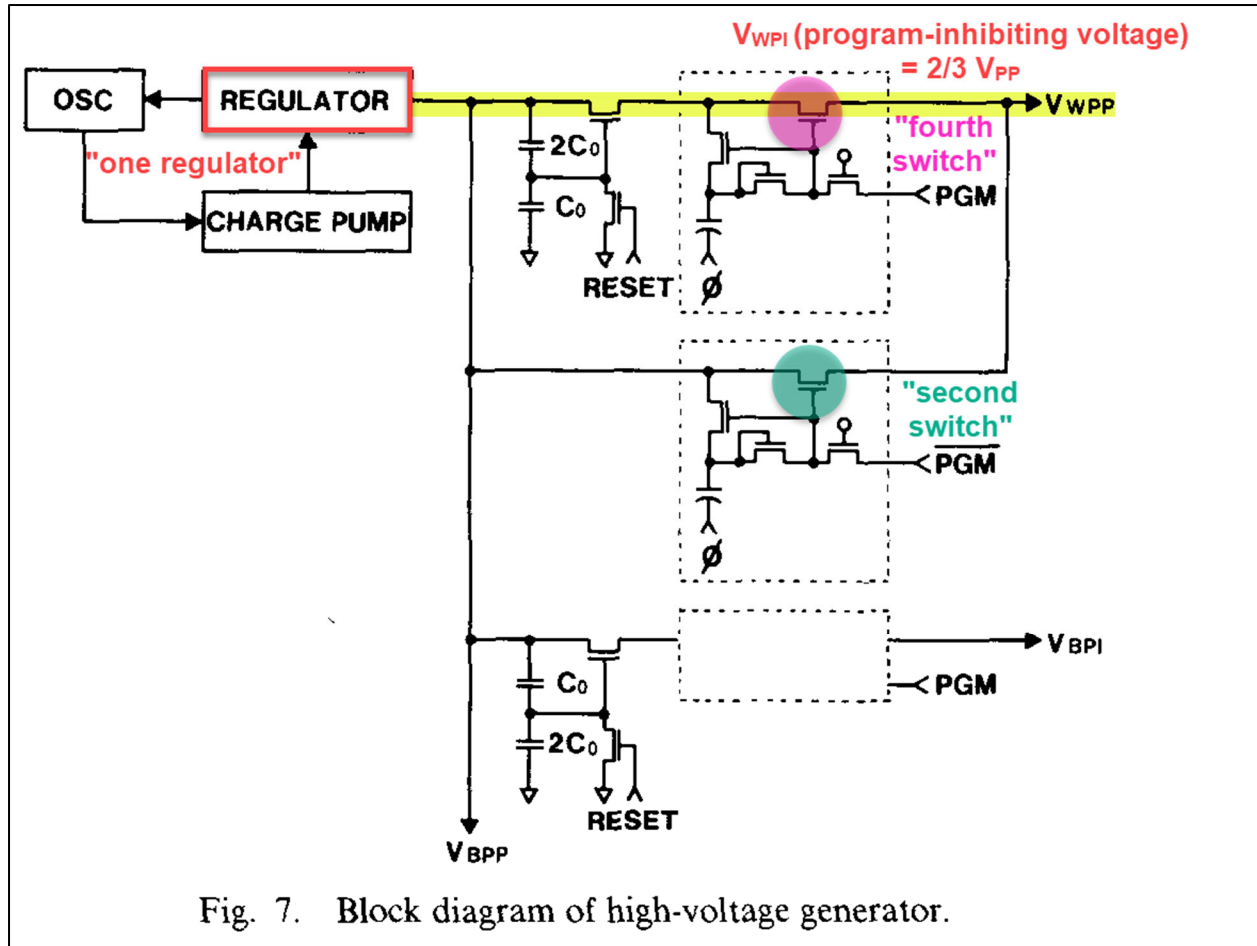
Because the blue **transistor** (the “voltage applying transistor”) is turned on by the V_{BPI} voltage applied through transistor T1, the voltage V_{BPP} , highlighted in yellow below, is applied to a drain terminal of the memory cell. As Nakayama discloses, the voltage V_{BPP} is the “programming high voltage, V_{PP} ,” that is, the output of the voltage regulator itself. EX-1007, Fig. 5; EX-1003, ¶193.



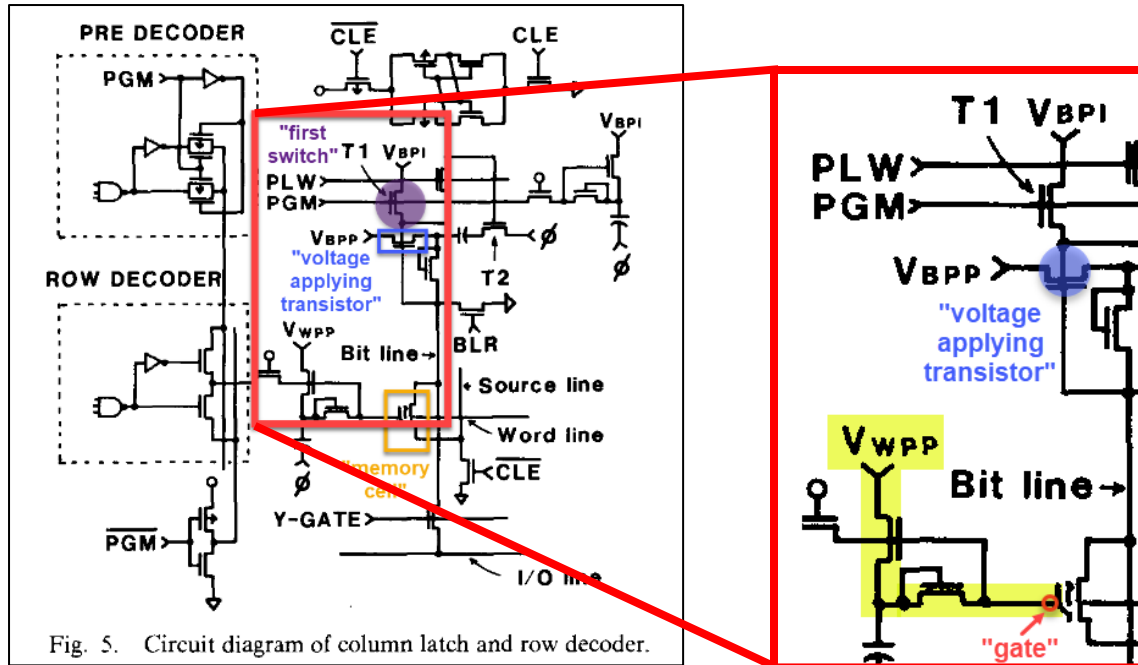
In sum, Nakayama discloses that, when the EEPROM is in a “program mode” (a “first operation mode”), the purple **transistor T1** (the “first switch”) and the magenta **transistor** (the “fourth switch”) are turned on, allowing the “output voltage of the regulator” to be applied to the drain terminal of the memory cell. Accordingly, to the extent the Board disagrees with Petitioner’s proposed claim construction of 5[a][i] (§V, *supra*), Nakayama discloses this limitation.

- (ii) **5[a][ii]: the voltage different from the output of the regulator to be applied to the gate of the memory cell, and**

Nakayama discloses 5[a][ii]. As discussed in 5[a][i] above, when the magenta transistor (“the fourth switch”) is turned on, it causes the word line supply voltage V_{WPP} to be set to V_{WPI} , which is at $2/3 V_{PP}$. EX-1007, Fig. 7; EX-1003, ¶195.



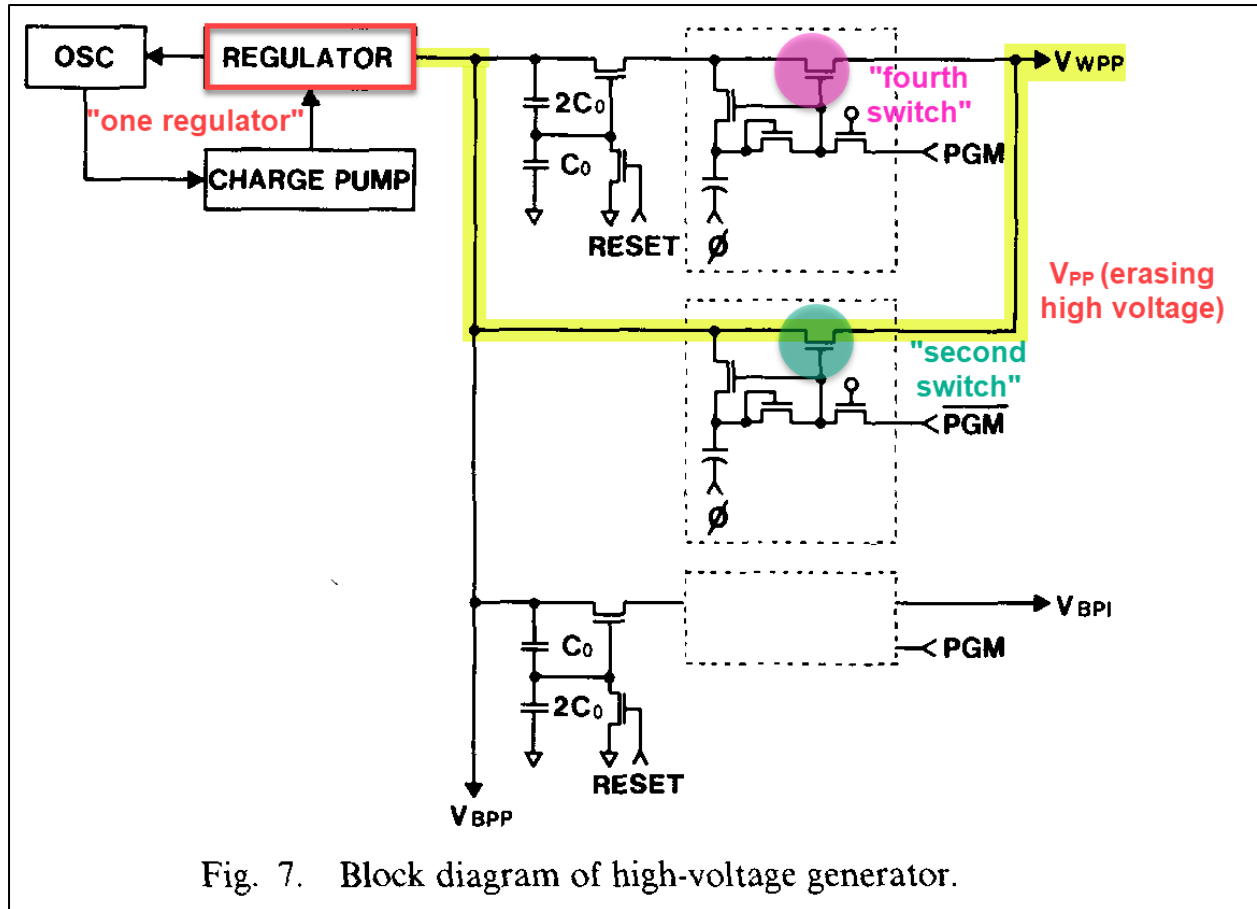
Continuing to trace V_{WPP} , as shown in Figure 5 of Nakayama, V_{WPP} is applied to the gate of the memory cell. EX-1007, Fig. 5; EX-1003, ¶196. Accordingly, Nakayama discloses the voltage ($2/3 V_{PP}$), different from the output of the regulator (V_{PP}), to be applied to the gate of the memory cell in a program operation.



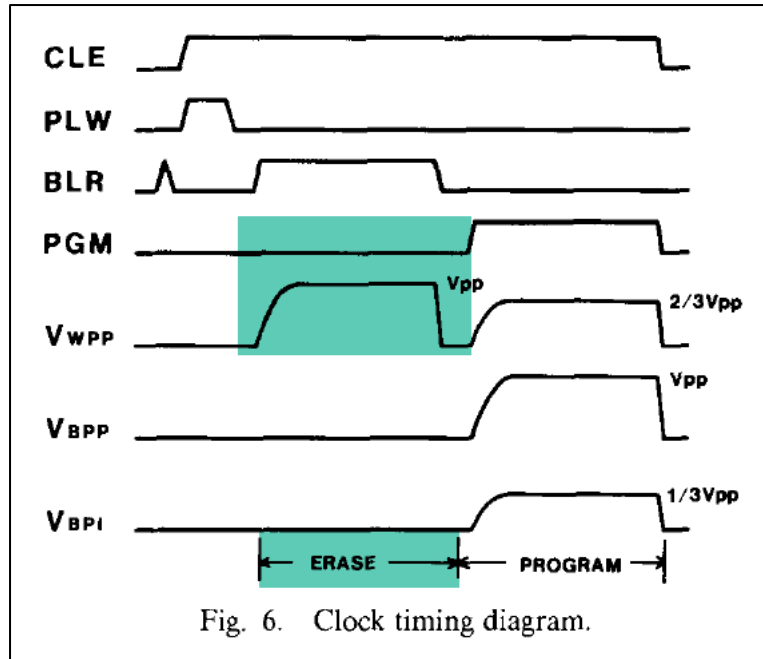
- (iii) **5[b]:** in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

Nakayama discloses an “erase operation,” which is a “second operation mode.”

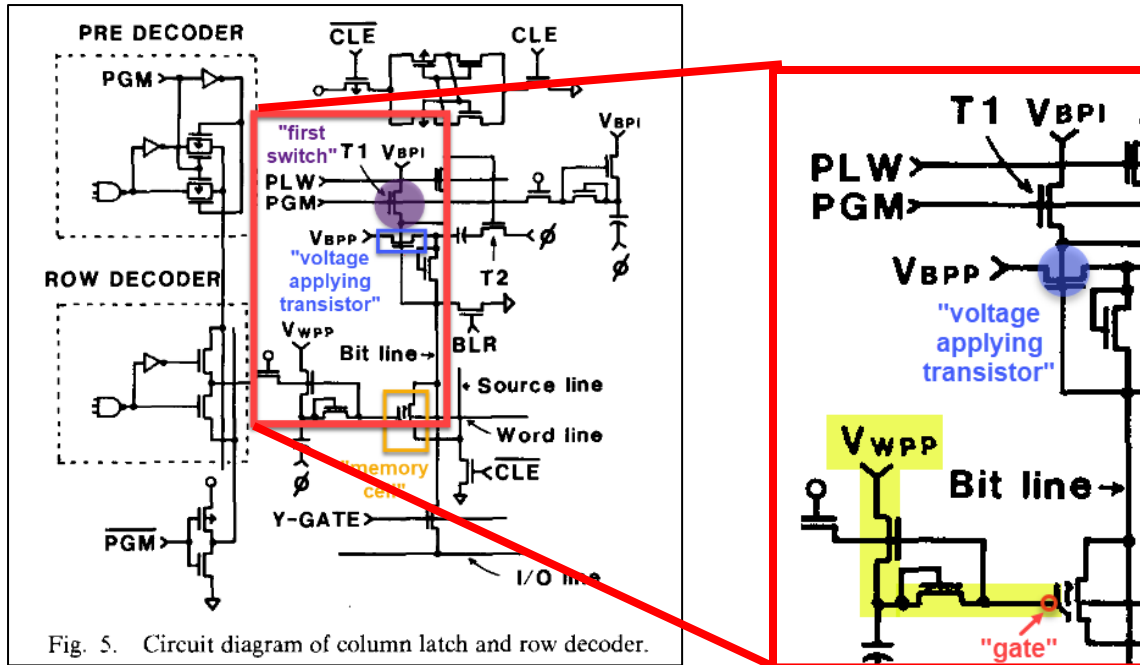
EX-1007, 913 (§III.A). In this “erase operation” mode, because PGM is set to ‘L,’ the green-highlighted **transistor** (the “second switch”) is turned on (and the “fourth switch” is turned off). EX-1003, ¶197.



The signal diagram of Figure 6 shows that, when PGM is set to “L,” the V_{WPP} supply voltage to the word line is set to V_{PP} , which further supports that the green transistor (the “second switch”) is turned on. EX-1003, ¶198. Figure 6 also demonstrates that the “erase mode” is in effect when PGM is set to “L,” as shown below.

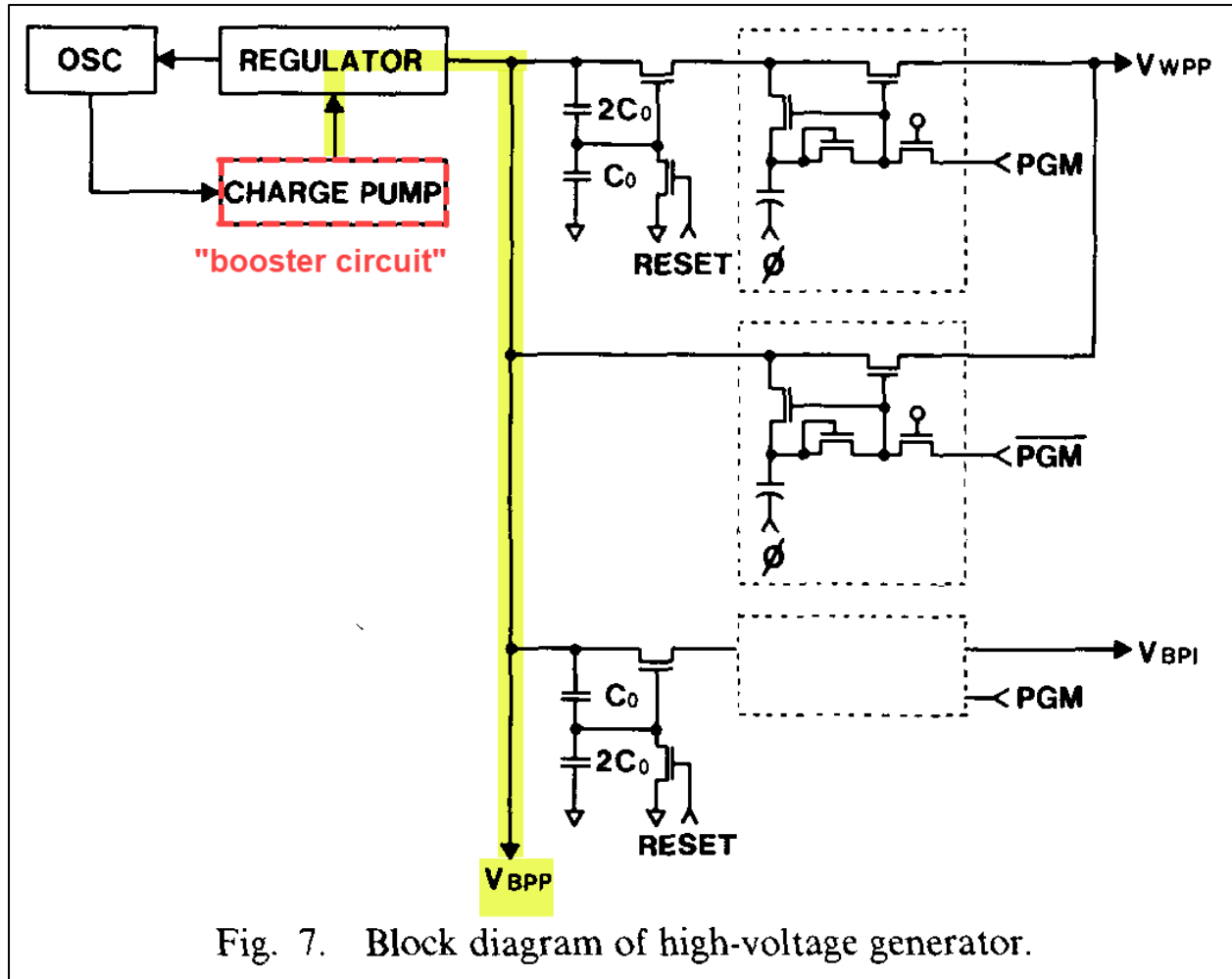


Again, tracing V_{WPP} in this “erase mode,” as shown in Figure 5 of Nakayama, the voltage level V_{PP} is applied to the gate of the memory cell. EX-1003, ¶199. Accordingly, Nakayama discloses that, in a second operation mode (“erase operation,” with PGM = “L”), the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell. *Id.*

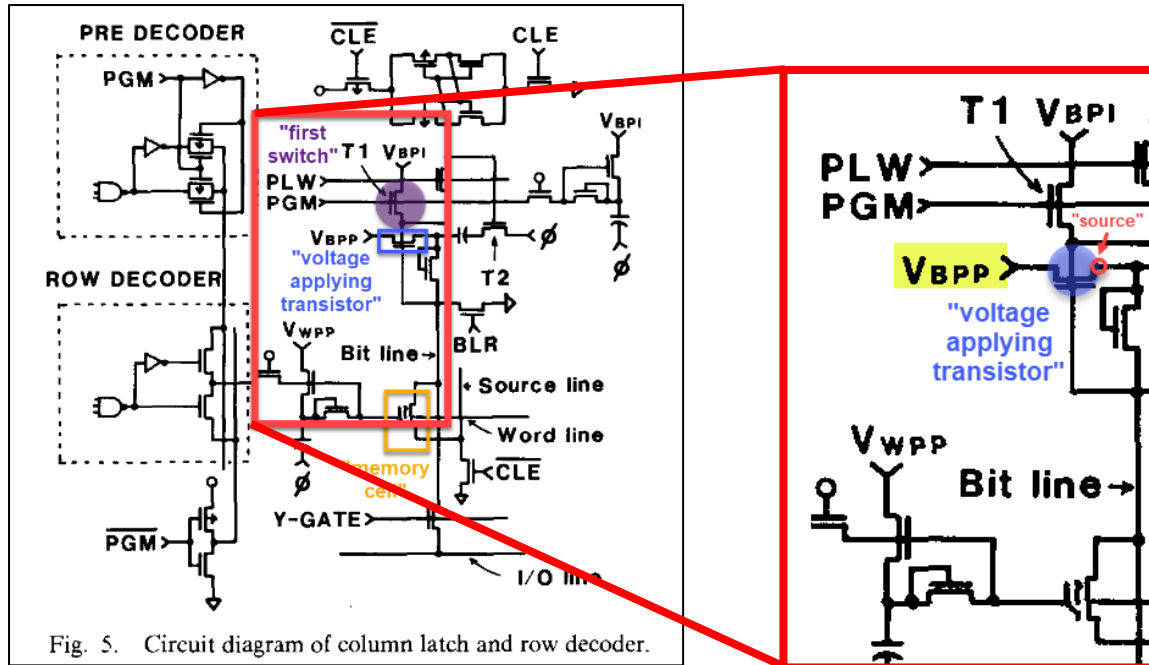


- (d) **Claim 21.** The semiconductor memory device of claim 1, wherein an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

Nakayama discloses 21[a]. Nakayama discloses in Figure 7 that V_{BPP} is coupled to an output of the charge pump circuit ("booster circuit"), as shown below in dotted red rectangle. EX-1007, Fig. 7; §II.C, *supra*; EX-1003, ¶200.



V_{BPP} , in turn, is coupled to a source terminal of the blue **transistor** (“voltage applying transistor”), as shown below. EX-1003, ¶201. Therefore, the output of the booster circuit (the “CHARGE PUMP” of Fig. 7 of Nakayama) is coupled to the source terminal of the voltage applying transistor.



VII. MANDATORY NOTICES AND FEES

A. Real Party-In-Interest

The real party-in-interest for Petitioner is SK hynix, Inc.

B. Related Matters

The '888 Patent was asserted against Petitioner in *Advanced Memory Technologies, LLC v. SK hynix Inc.*, Case No. 2:24-cv-01078-JRG (E.D. Tex., filed August 21, 2024).

C. Counsel and Service Information

Electronic service may be made on the email addresses identified below and in the accompanying Power of Attorney.

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D. Payment of Fees

The Office is authorized to charge the fee required for this Petition (and any additional fees) to Deposit Account No. 50-5708.

E. Requirements for Inter Partes Review

Petitioner certifies that the '888 Patent is available for *inter partes* review, that Petitioner is not barred or estopped, and that 35 U.S.C. §§315(a)-(b) is inapplicable.

VIII. CONCLUSION

For the reasons above, *inter partes* review is requested.

Date: August 22, 2025

Respectfully submitted,

By: /s/ James M. Glass

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Counsel for Petitioner

CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 C.F.R. § 42.24, the undersigned hereby certifies that the word count for the foregoing Petition for *inter partes* review (excluding the table of contents, table of authorities, mandatory notices, certificate of service or word count, and appendix of exhibits or claim listing) totals 13,050 words, which is within the word limit allowed under 37 C.F.R. § 42.24(a)(i).

Date: August 22, 2025

/s/ James M. Glass

James Glass (Reg. No. 46729)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e), 42.105(a), the undersigned hereby certifies that a copy of this Petition and its respective exhibits were served via FedEx on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for the '888 Patent:

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Szymon M. Gurda
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OAK BROOK, IL 60523
UNITED STATES

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