Exhibit D-OB: Omnibus Obviousness Chart

The following chart demonstrates that asserted claims 1, 3, 5, 20, and 21 of U.S. Patent No. 8,593,888 (the '888 patent") are obvious in view of the references discussed in Exhibits D-1 – D-X3 alone, or in combination with one or more of the following references (collectively the "Omnibus References"), consistent with the obviousness combinations and rationale set forth in the cover pleading hereto:

- Nakauchi
- Tomita
- Nam
- Lin
- Lo Giudice
- Nakayama
- Seiko
- XPM
- Micron
- Shor
- Im
- Cho
- Yamauchi
- Tanzawa-452
- Tanzawa-945
- Tanzawa-724
- Hirabayashi
- Kawai
- Barnett
- O
- Nierle
- Shibata
- De Vita
- Barnett-2007
- Barnett-2008
- Banba
- Daga

As set out below, each limitation was well known in the art and would have been obvious to a person of ordinary skill in the art as it was part of the general knowledge of one of ordinary skill in the art, as shown by the teachings of at least one of the prior art references set forth above. A person of ordinary skill in the art would have been motivated to combine any of these references with at least one or more of the foregoing prior art references for at least the reasons set forth in the cover document of SK hynix's invalidity contentions and/or as further set out in Exhibits D-1 – D-X3.

This chart incorporates by reference—for each respective claim and claim limitation of the '888 patent—the exemplary prior art disclosures identified in SK hynix's charts Exhibits D-1 through D-X3. Those disclosures are each incorporated into this chart in this Exhibit D-OB as if fully set forth, but which for brevity are not repeated verbatim below. This chart therefore sets out the additional disclosures from the remaining references described above which, together with such other references incorporated or noted in this chart, render obvious each and every claim limitation of the '888 patent, to the extent such limitation(s) are not anticipated.

The analysis in this chart is based on the apparent claim constructions and interpretations that AMT has advanced to allege infringement of the asserted claims of the '888 patent, as set forth in AMT's infringement contentions served April 2, 2025. Nothing in this chart should be interpreted as SK hynix conceding that AMT's apparent claim constructions and interpretations are correct or supported by intrinsic or extrinsic evidence.

The analysis in this chart is preliminary, and SK hynix's investigation into the invalidity of the asserted claims of the '888 patent is ongoing. SK hynix reserves the right to provide additional theories under which the cited prior art anticipates or renders obvious the asserted claims of the '888 patent, including in response to the receipt of third party discovery currently ongoing and to be produced in this litigation. The citations to specific disclosure of the prior art references in this chart are exemplary, and SK hynix reserves the right to rely on additional disclosures to the same references. SK hynix also reserves the right to offer expert testimony and opinions explaining how a person of skill in the art would understand the disclosures of the cited prior art references.

Exemplary Disclosures
1[a] A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal, comprising:
To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious a semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal. *See, e.g.*: Banba at 2:66-3:5: Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate. Banba at 4:24-34: According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating

a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

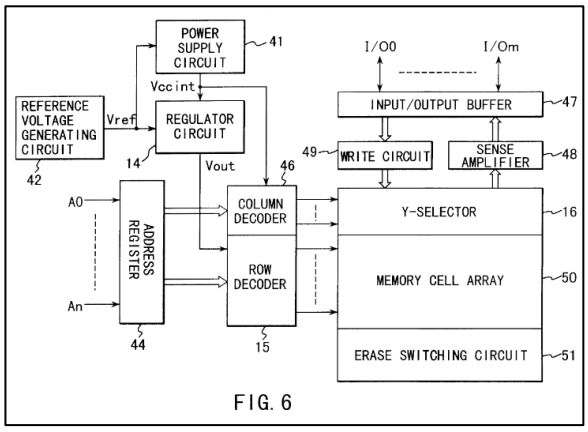


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50

by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

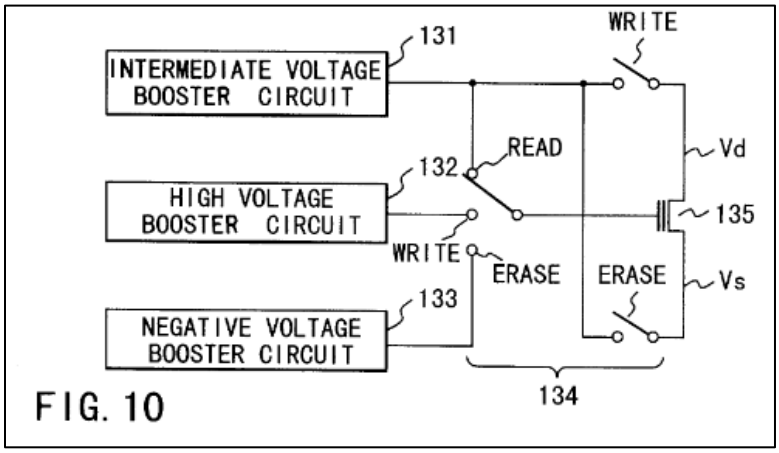


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is

distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

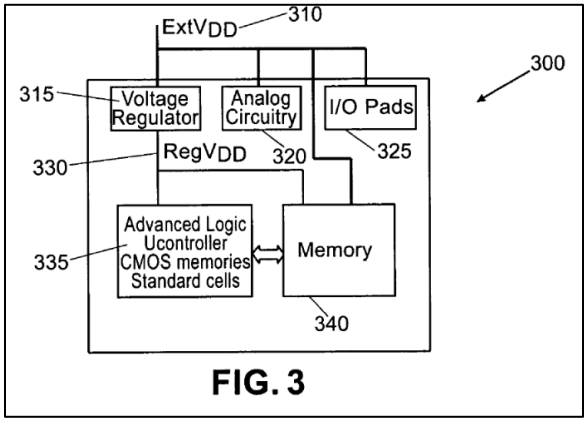


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

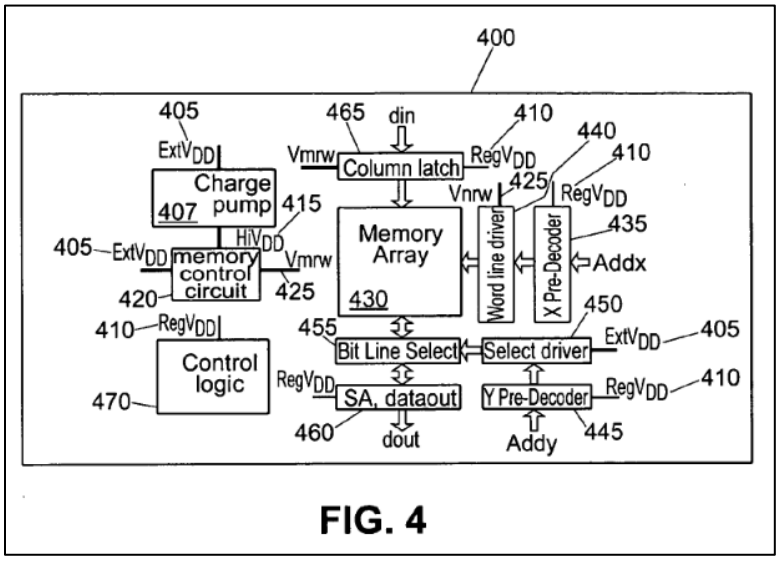


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory

control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

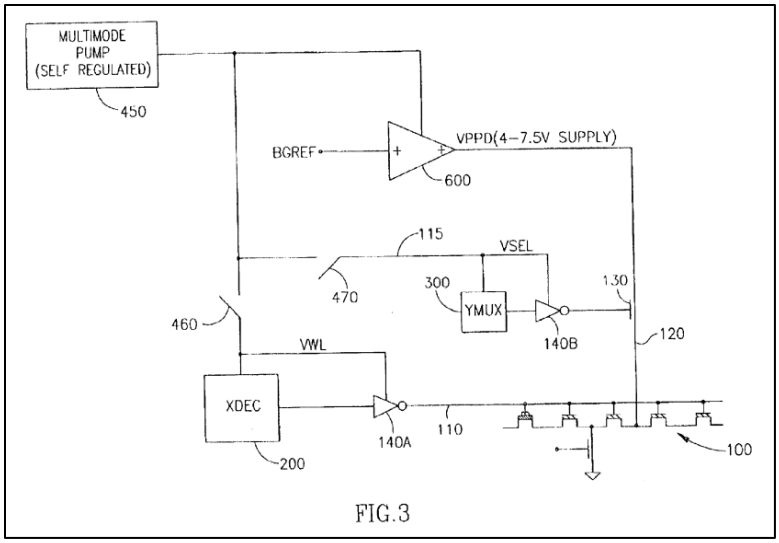


FIG.3

Shor at 2:42-61:

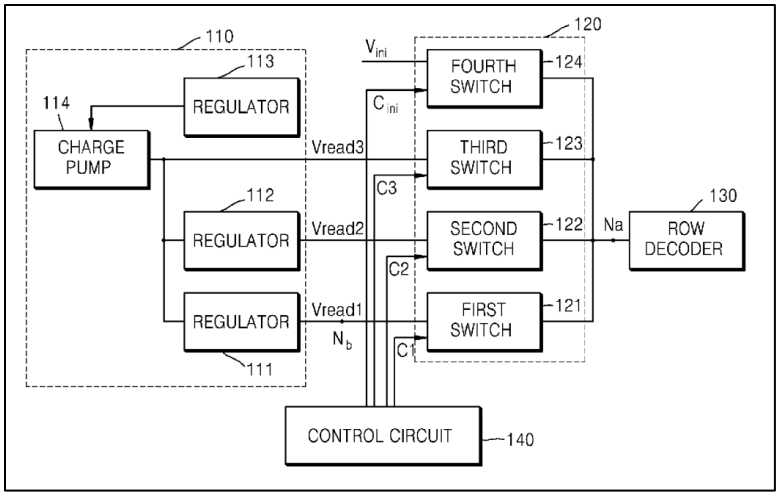
As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled “Efficient Charge Pump with Constant Boosted Output Voltage” by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively

low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

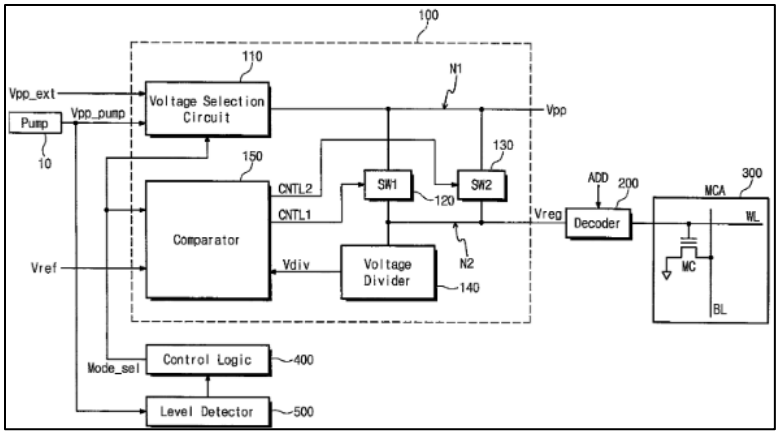
Cho at 2:24-64:

Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit, the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and

a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

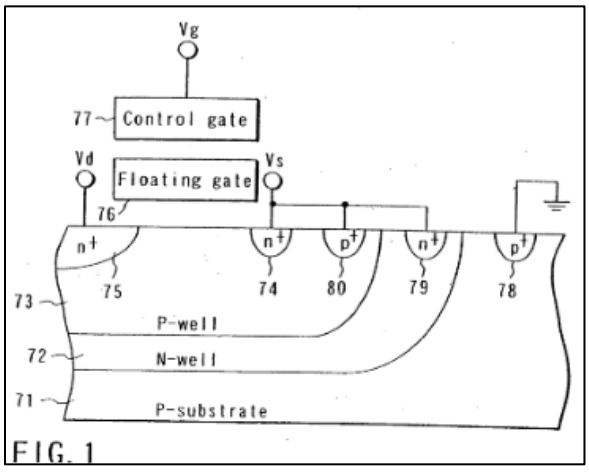


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

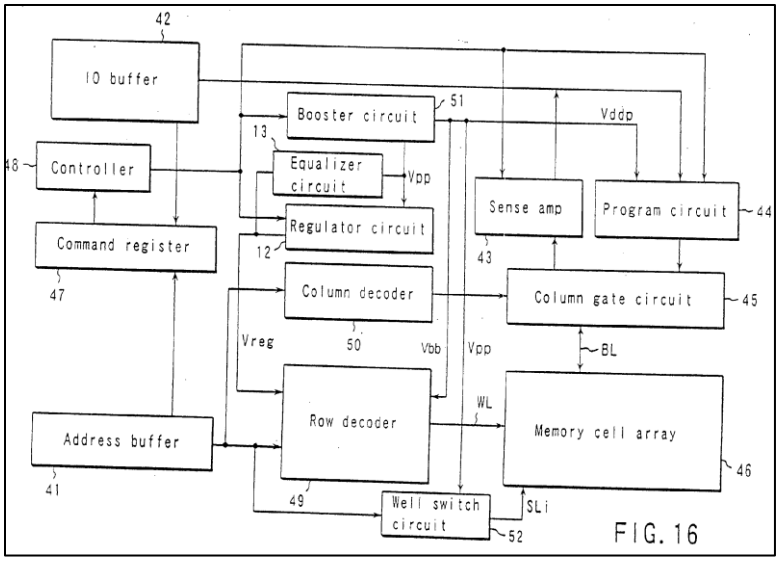


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1,

Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

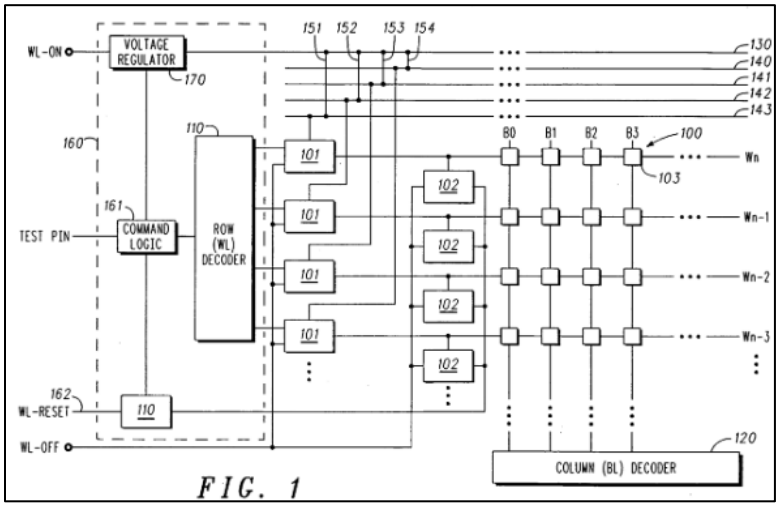


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

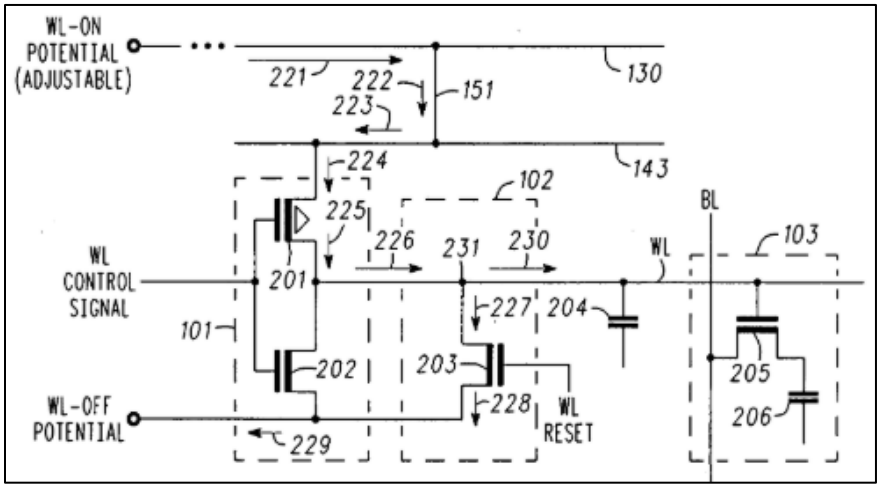


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

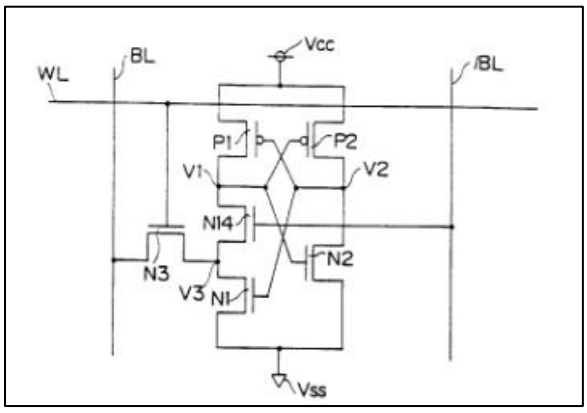
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is

controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the

columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

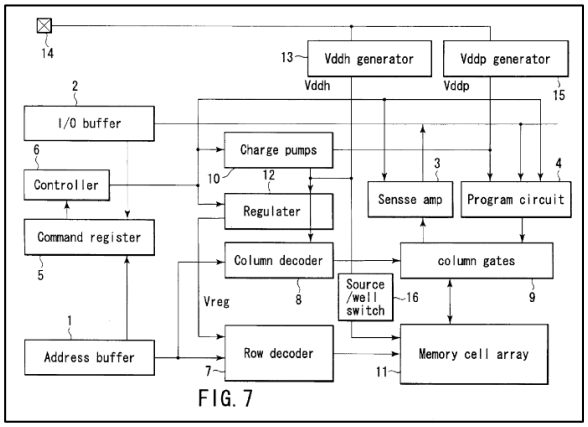


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

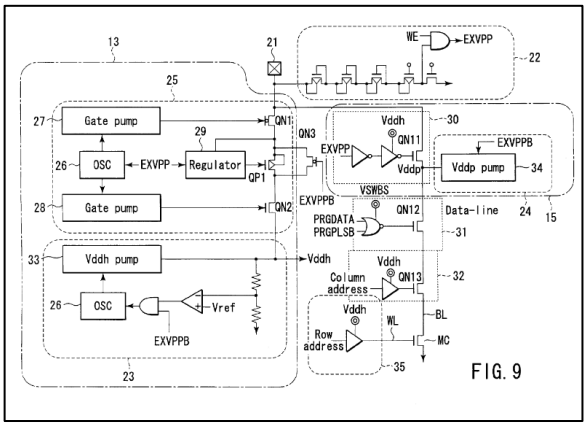
FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.



Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

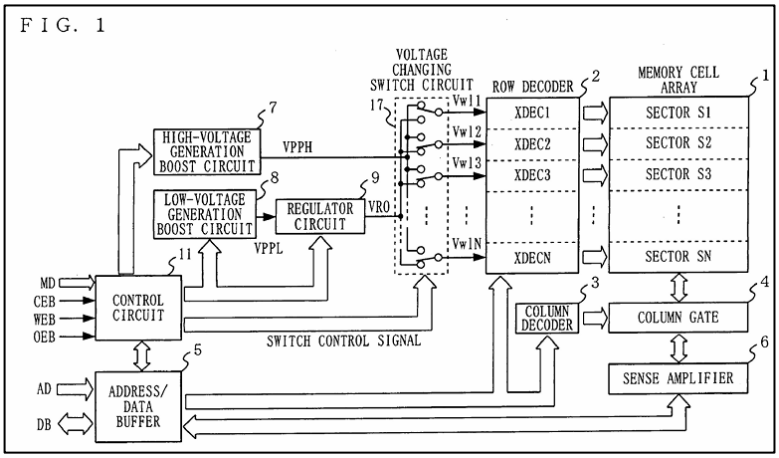
Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17

comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.

FIG. 1



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

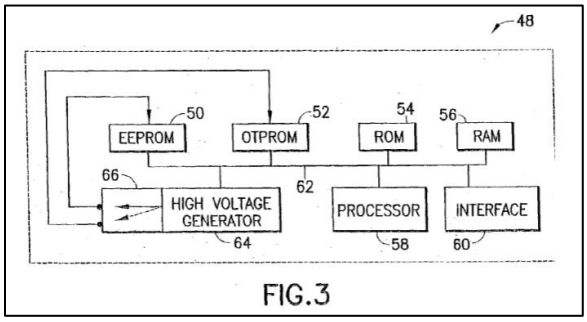


FIG.3

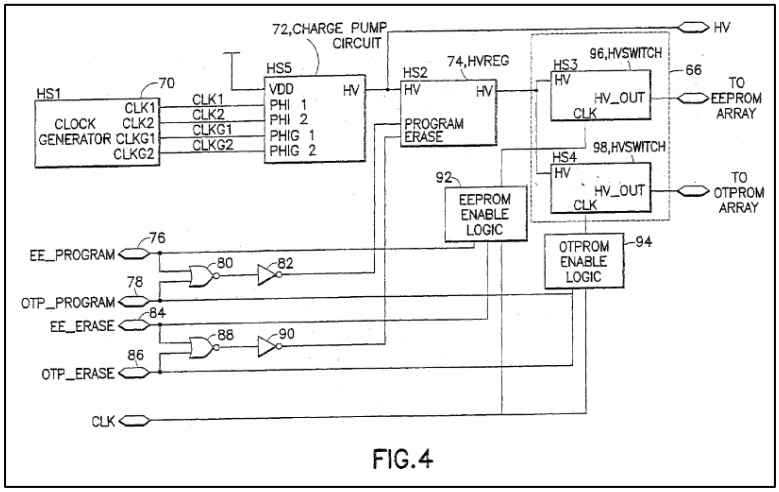


FIG.4

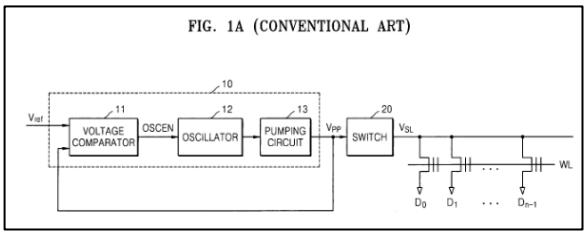
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

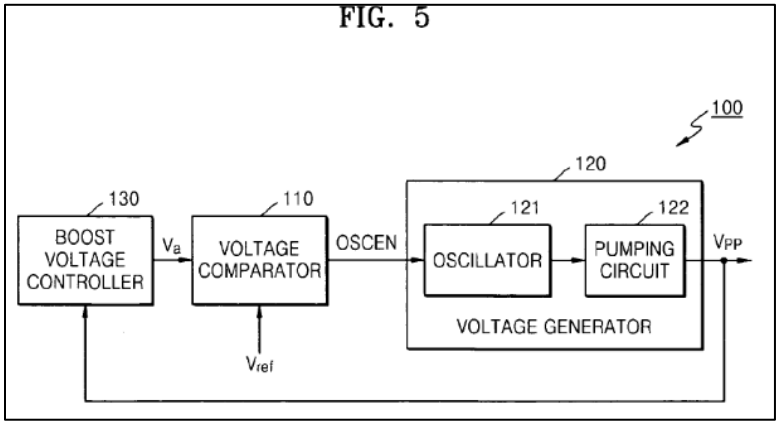
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

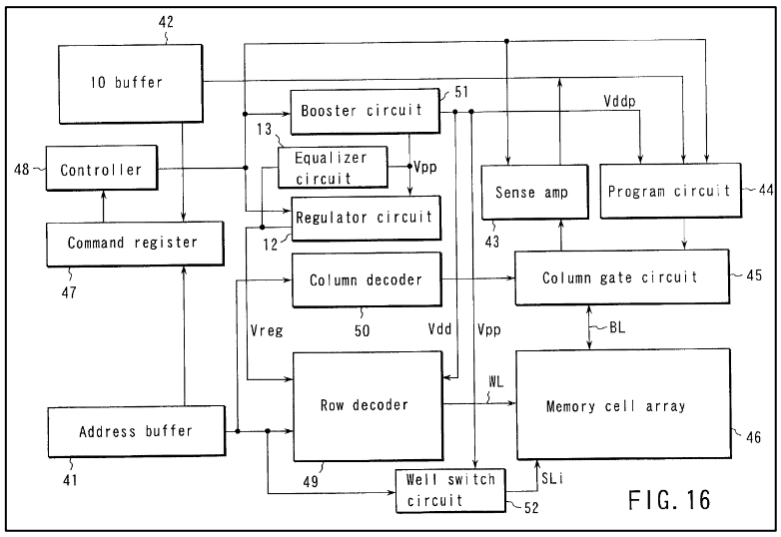
The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.



Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

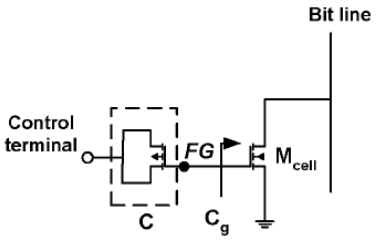


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

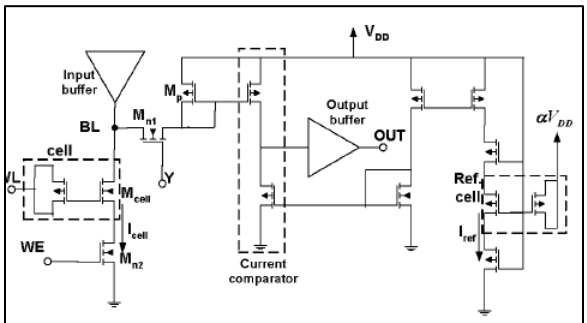


Figure 3. Current mode Sense Amplifier.

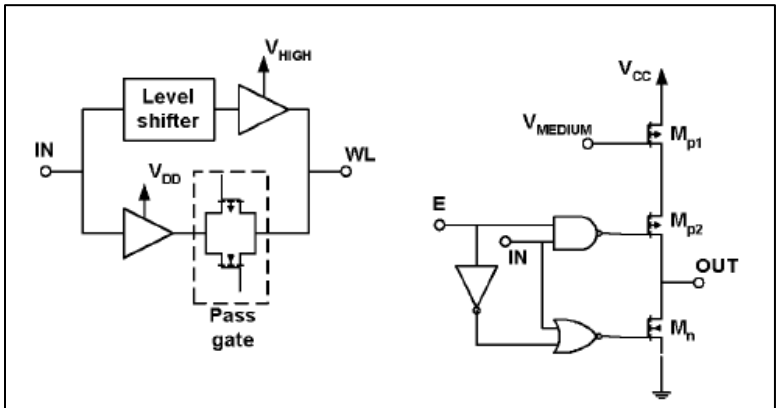


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

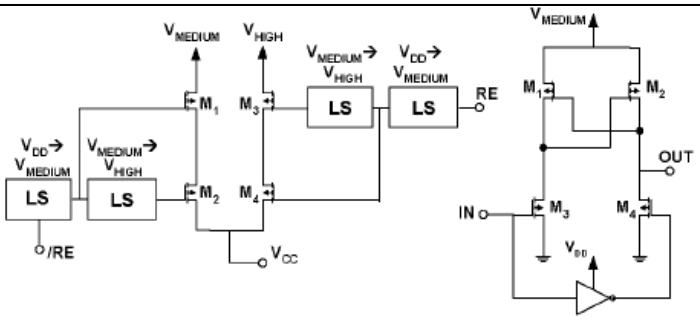


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

1[b] the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell, wherein

The Omnibus References disclose and/or render obvious the memory cell, one regulator, first and second switches, and a voltage applying transistor for applying a voltage to the memory cell.

See, e.g.:

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for

regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

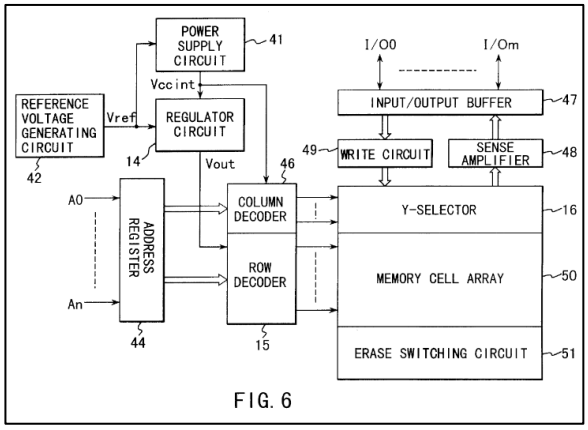


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

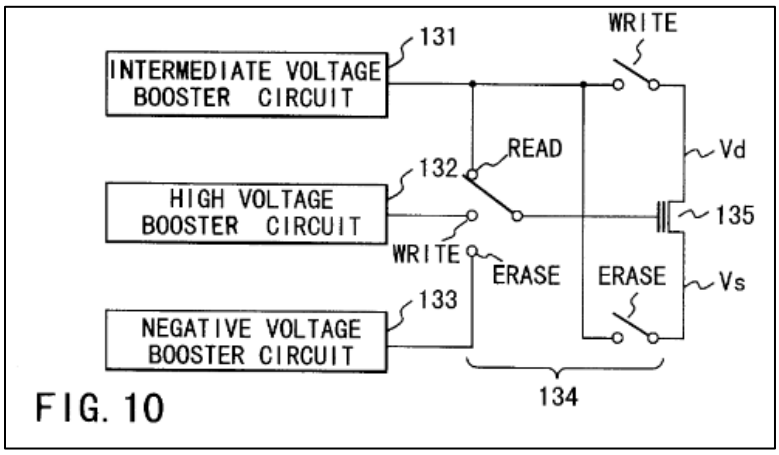


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

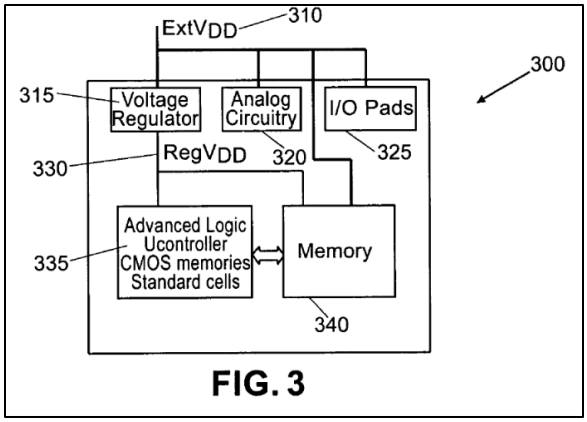


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

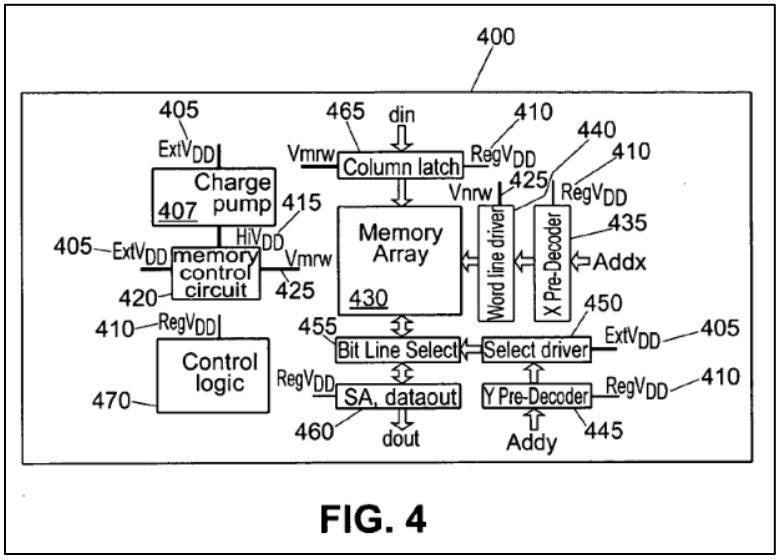


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

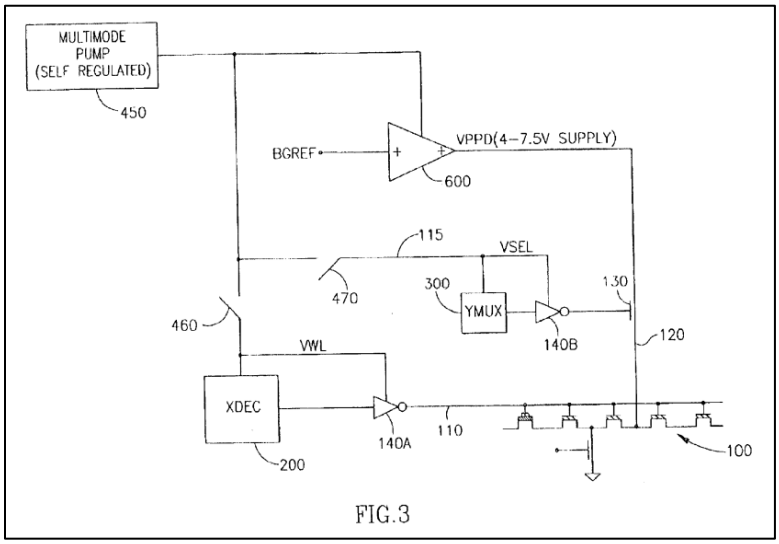


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

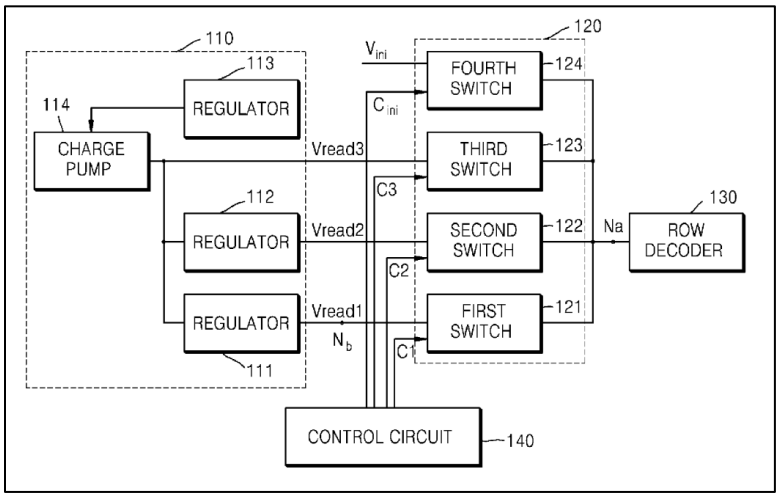
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

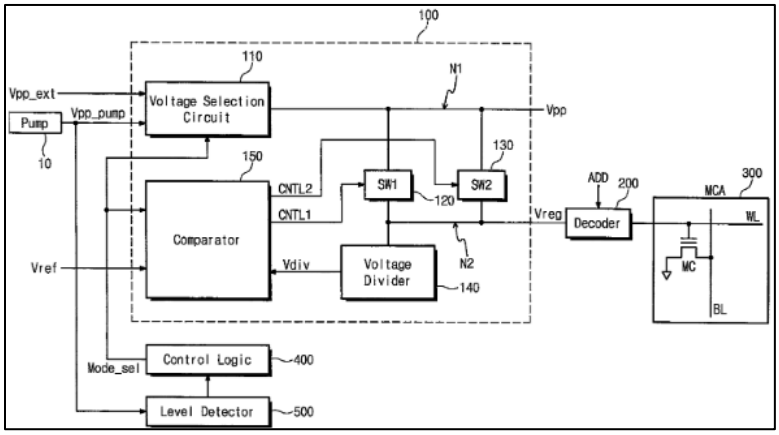
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

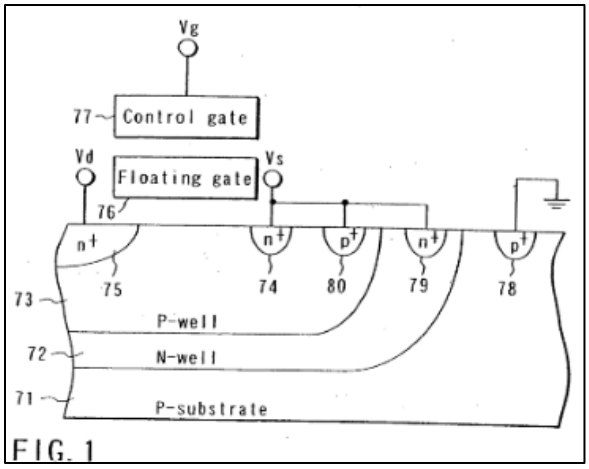


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

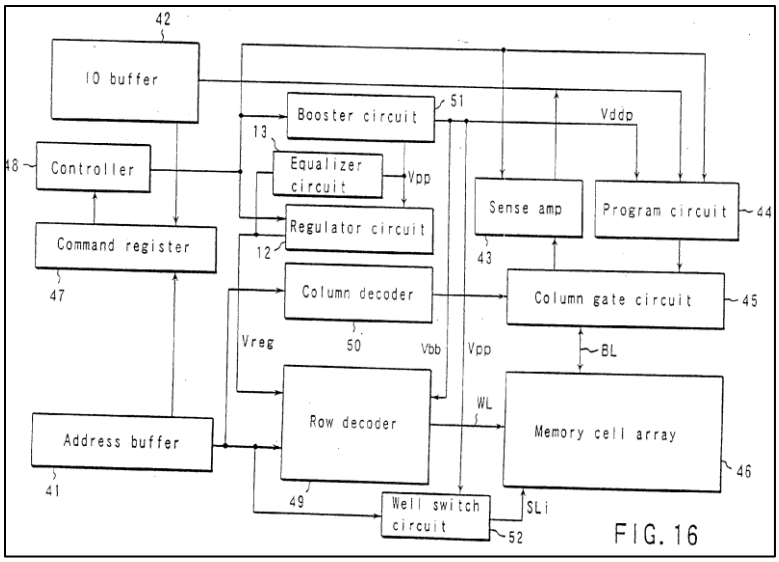


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

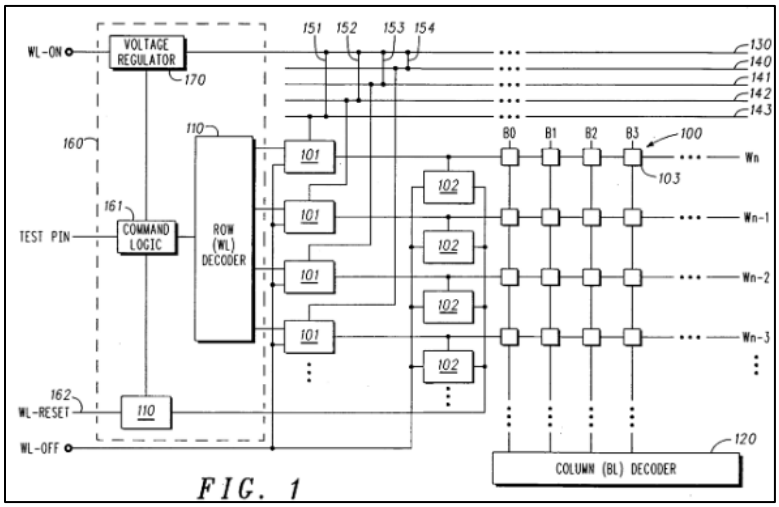


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

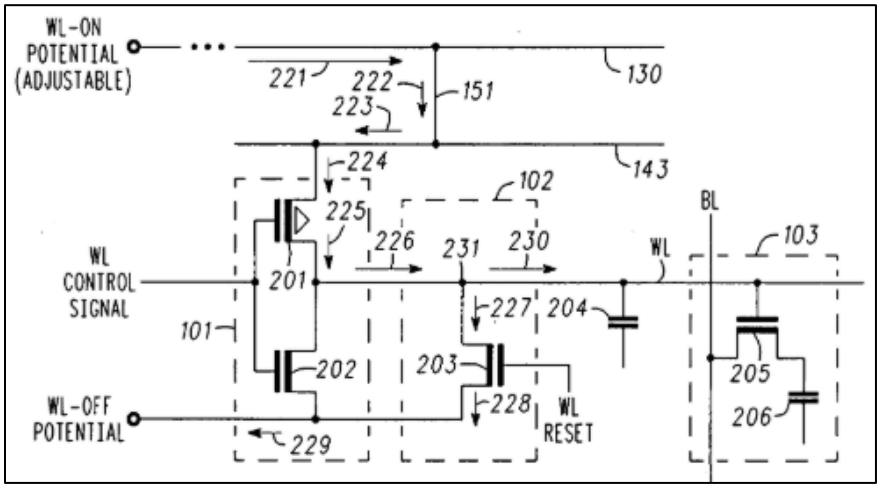


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

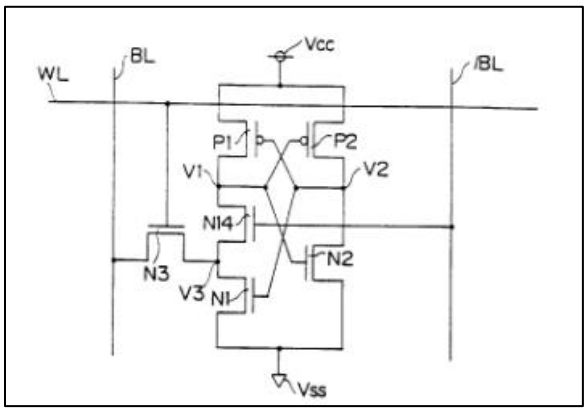
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

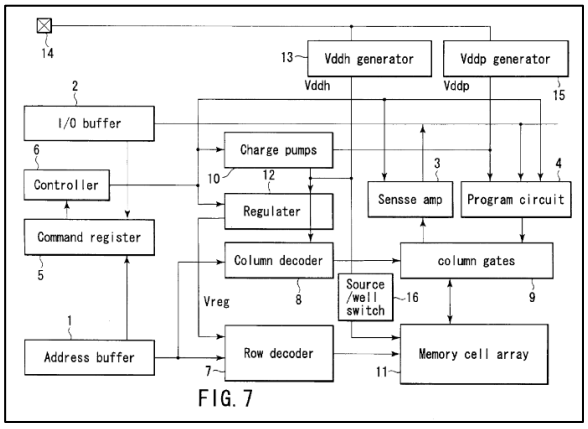


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

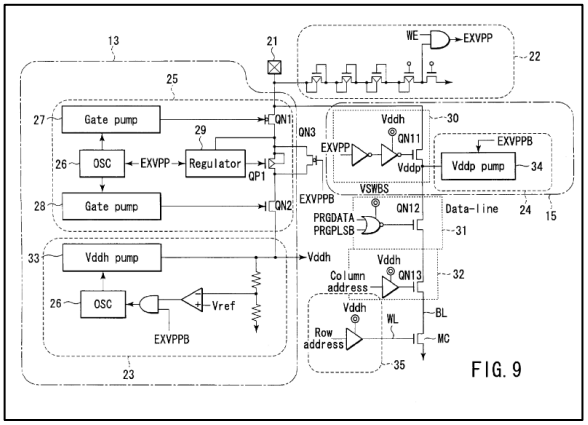


FIG. 9

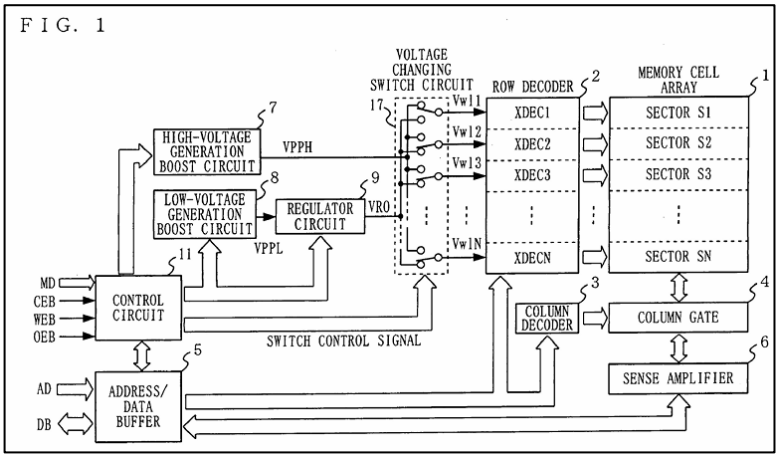
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

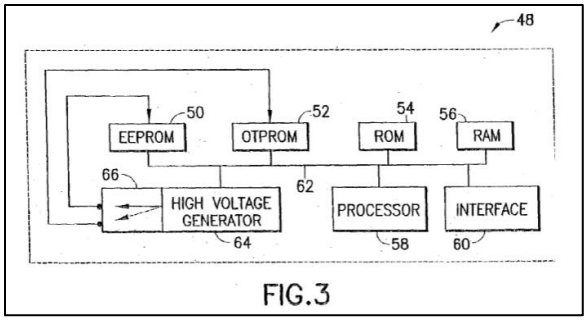


FIG.3

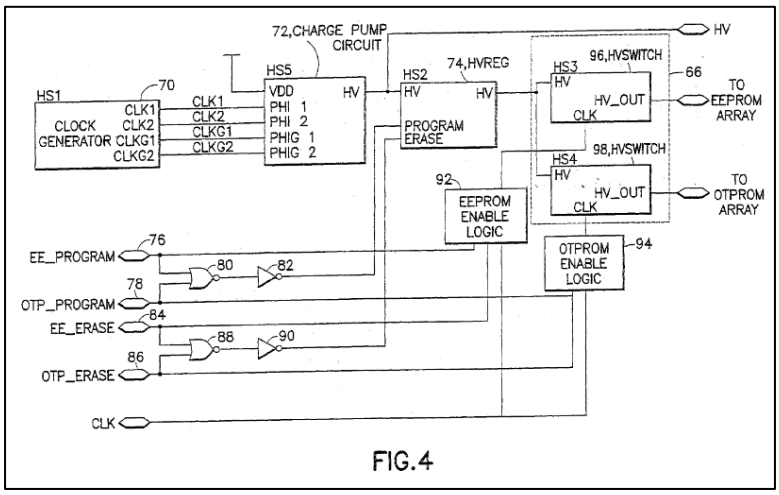


FIG.4

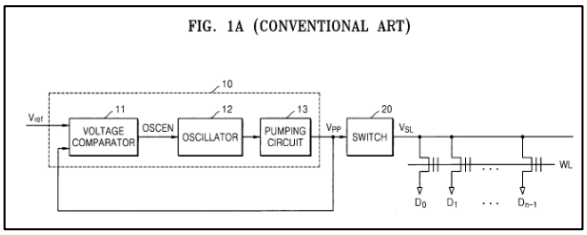
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

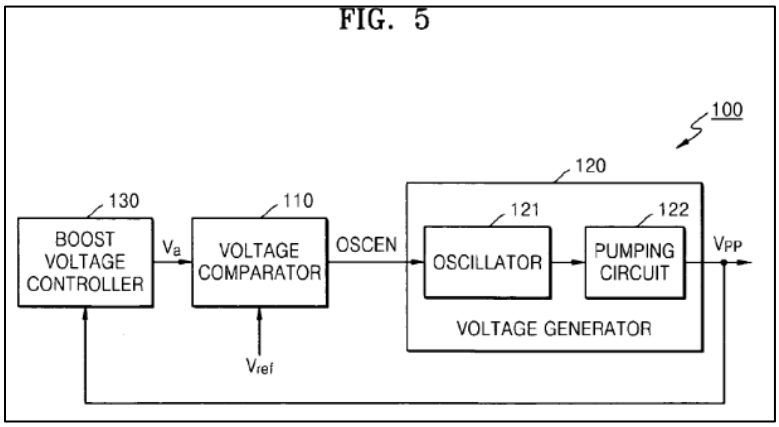
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

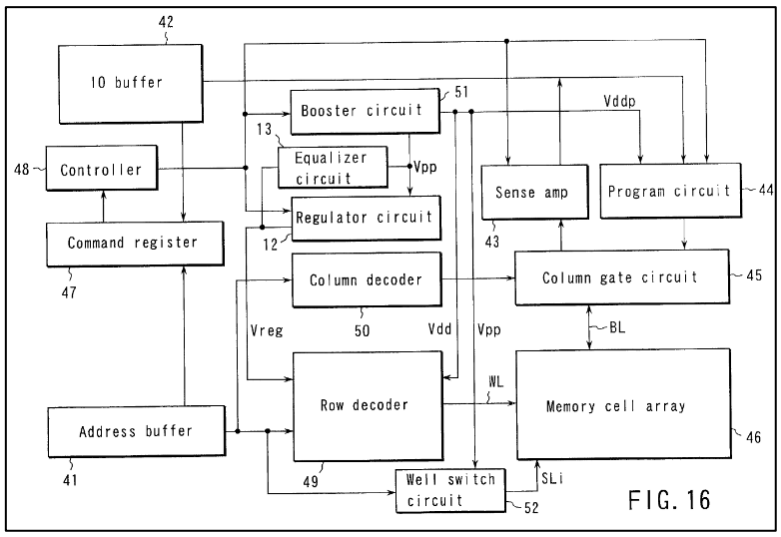


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

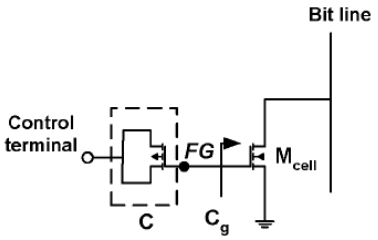


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

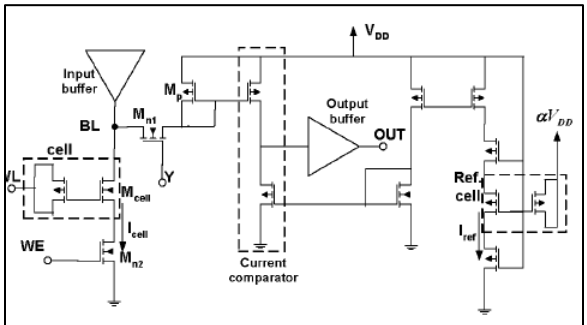


Figure 3. Current mode Sense Amplifier.

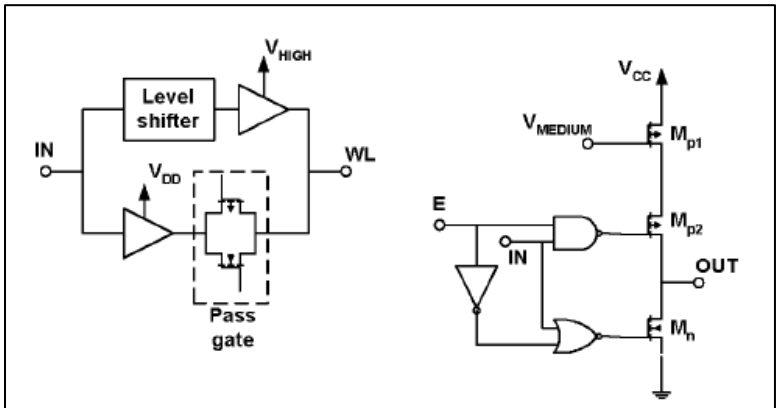


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

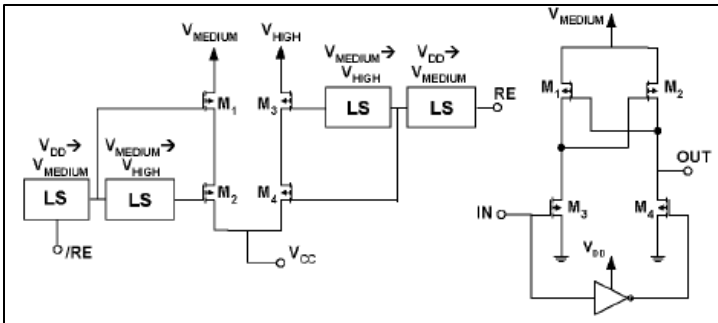


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

1[c] an output of the regulator is coupled to inputs of the first and second switches,

The Omnibus References disclose and/or render obvious an output of the regulator is coupled to inputs of the first and second switches.

See, e.g.:

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a

regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

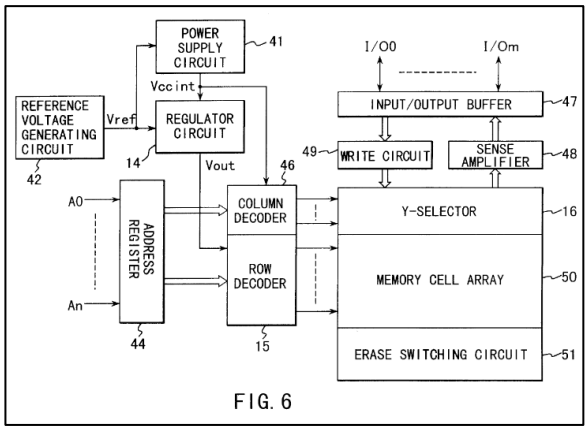


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

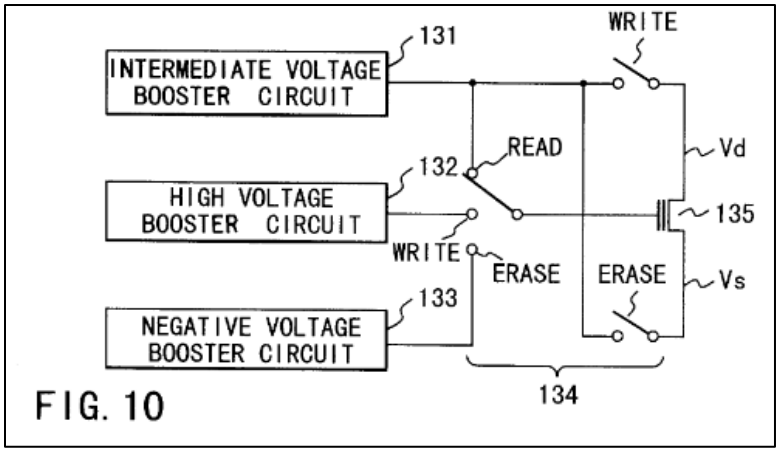


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

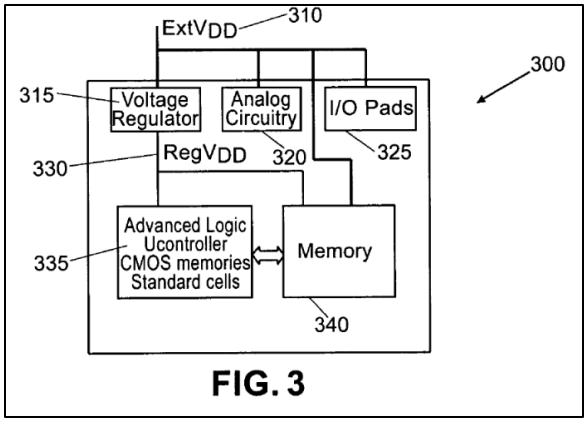


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

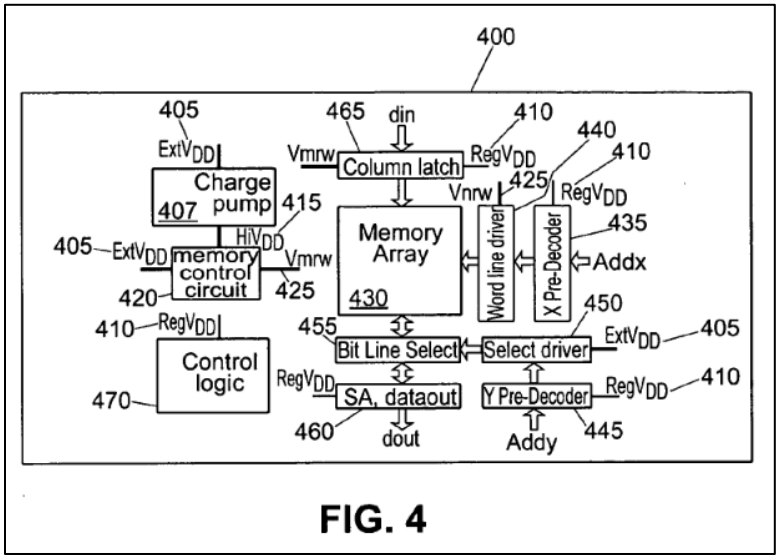


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

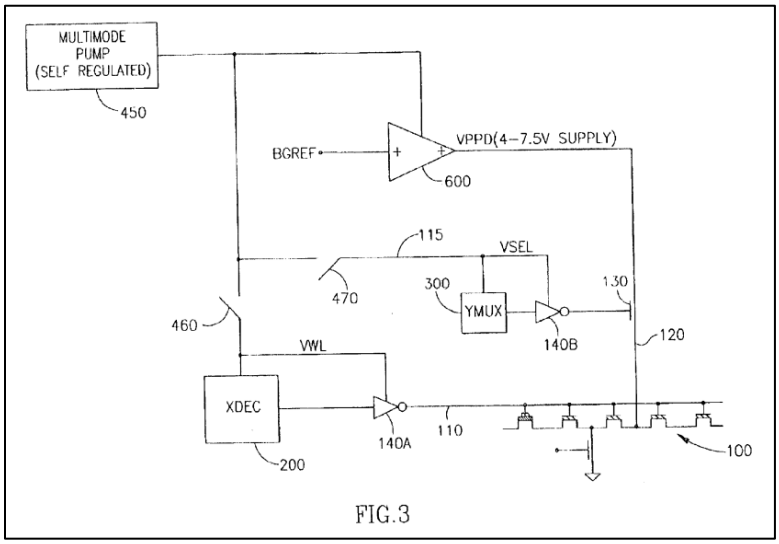


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

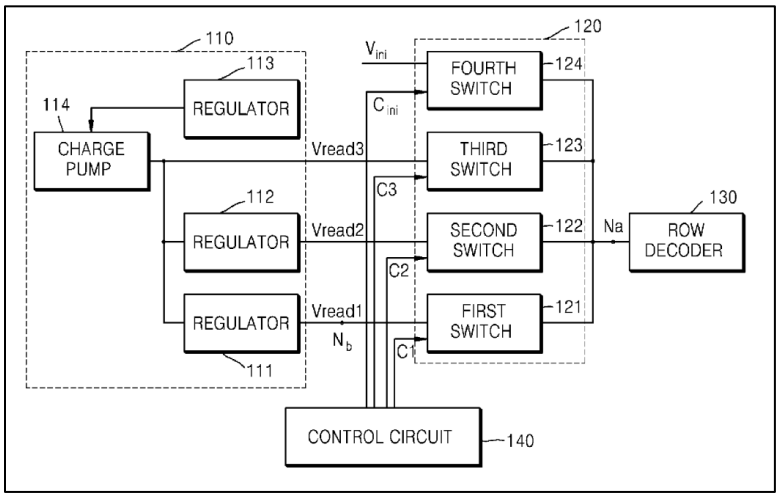
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

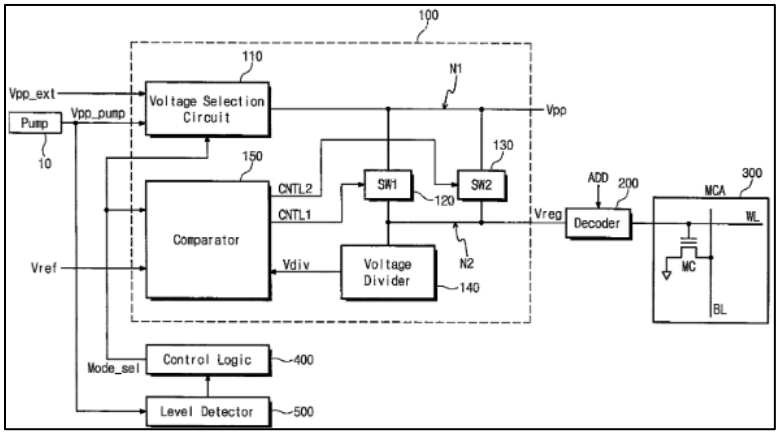
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

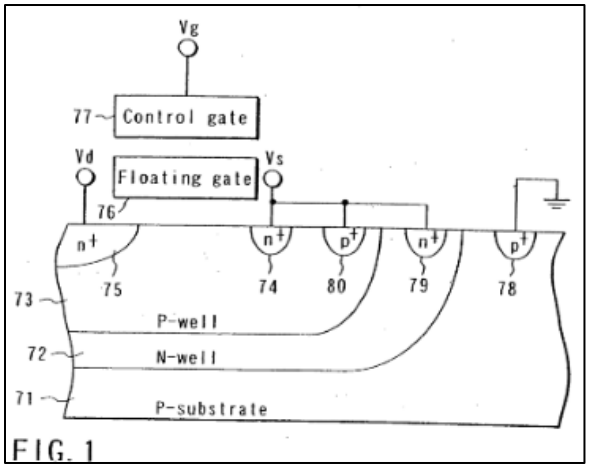


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

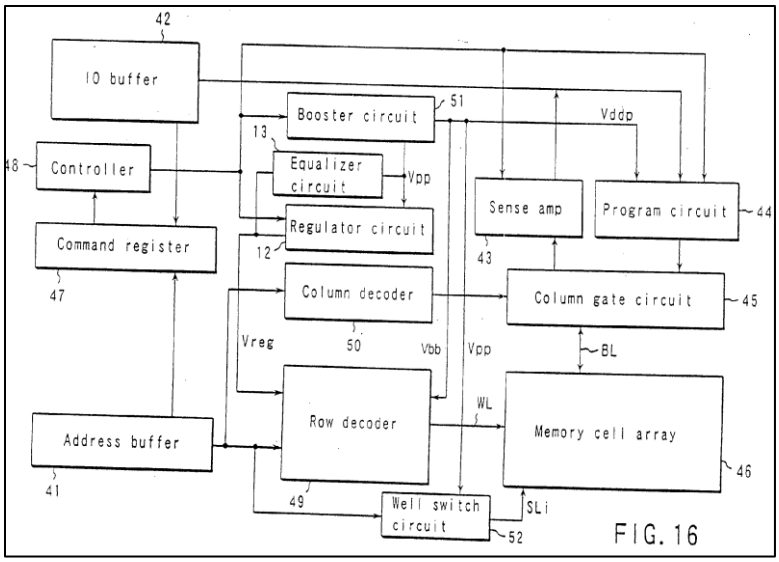


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

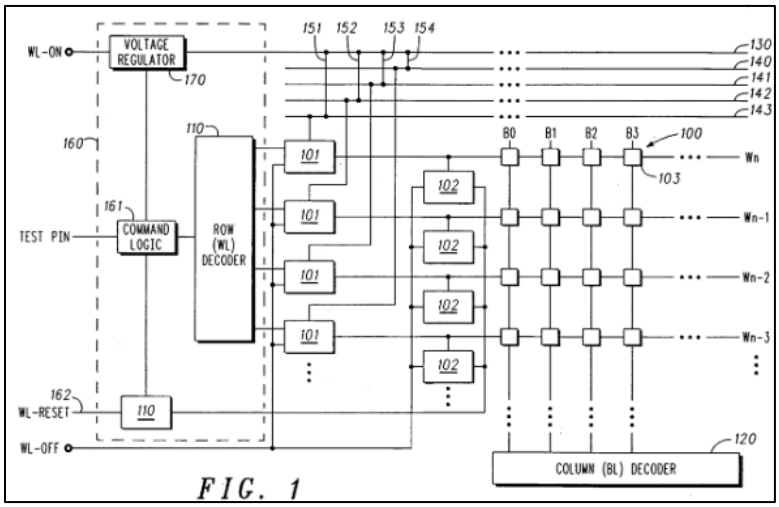


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

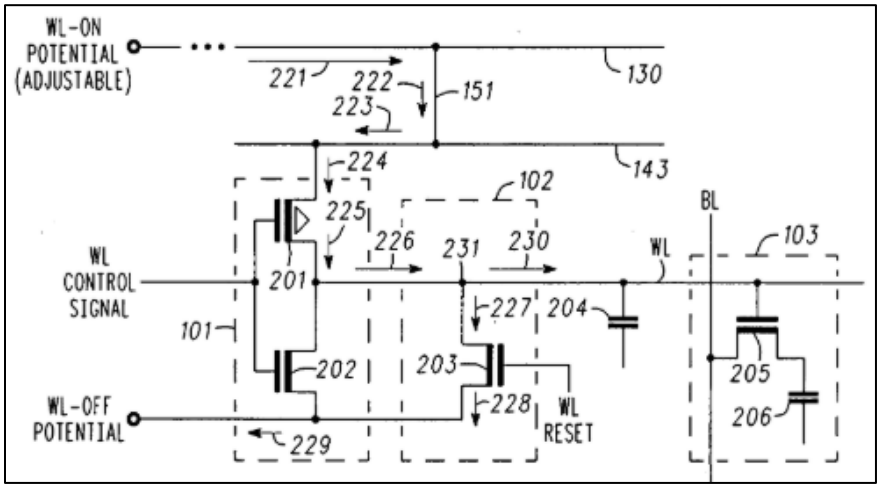


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

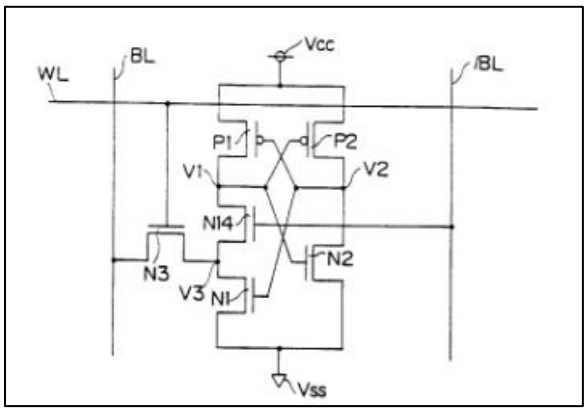
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

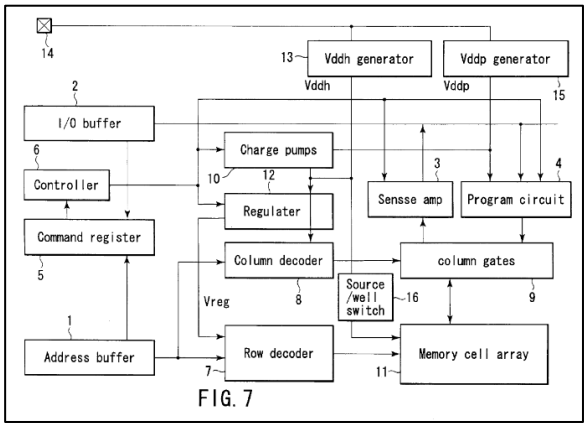


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

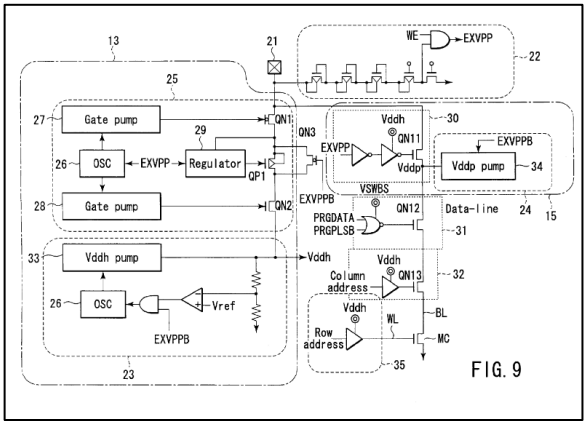


FIG. 9

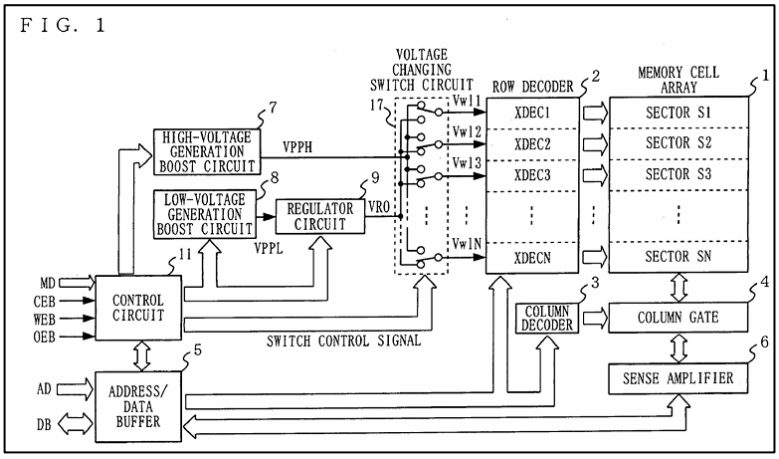
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

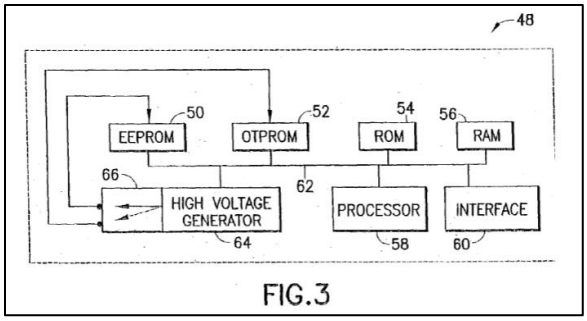


FIG.3

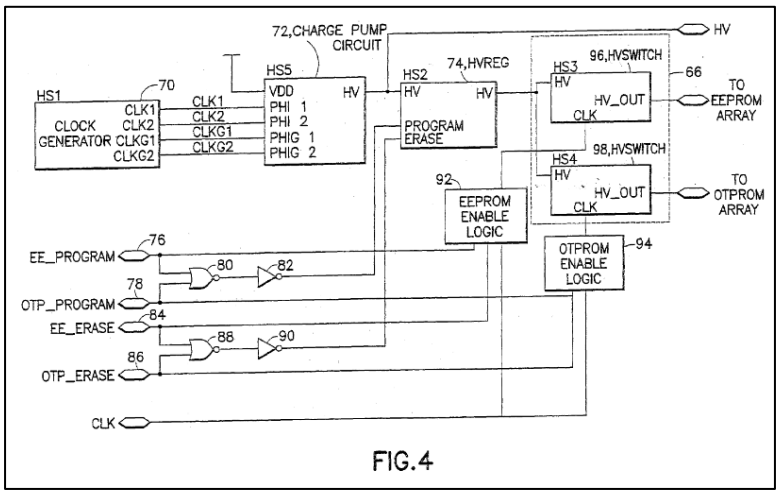


FIG.4

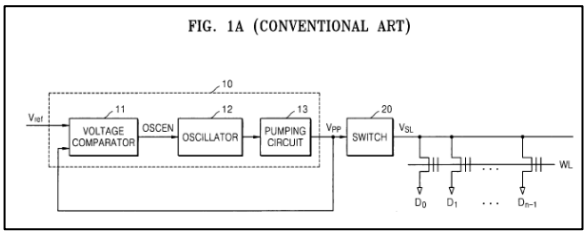
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

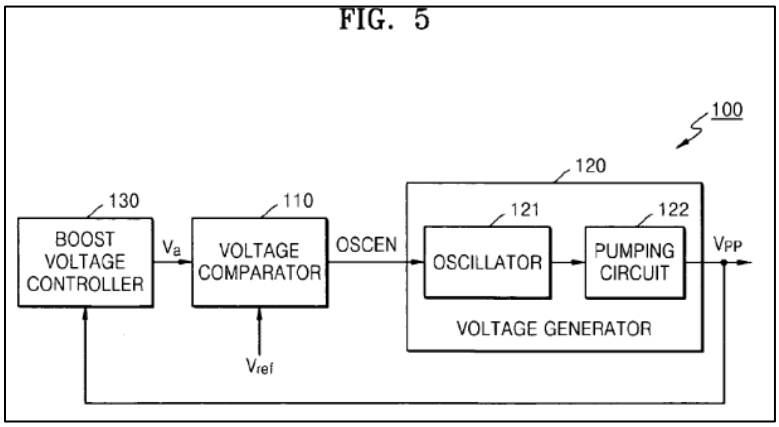
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

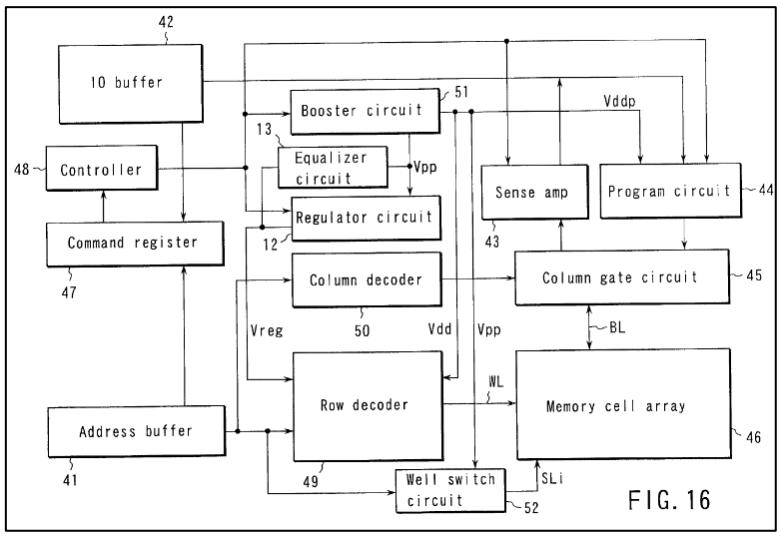
The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.



Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

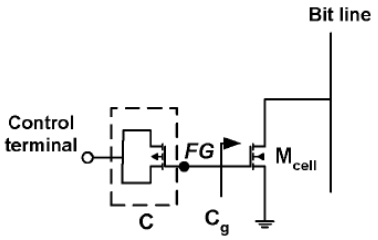


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

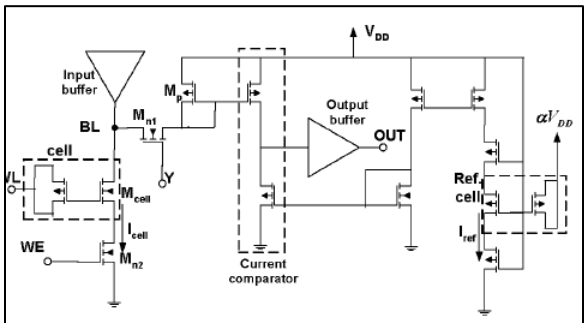


Figure 3. Current mode Sense Amplifier.

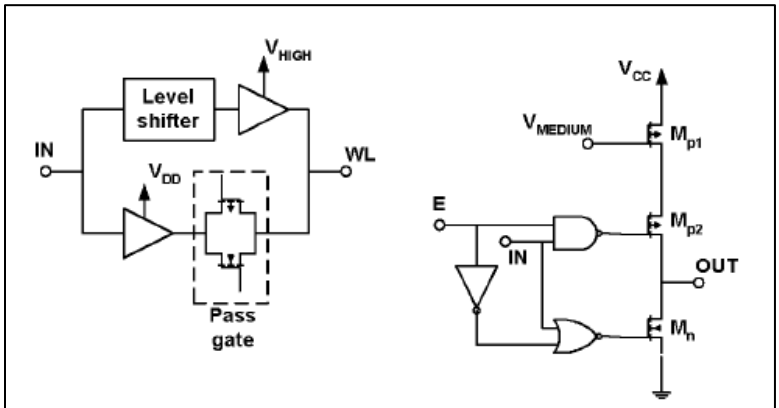


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

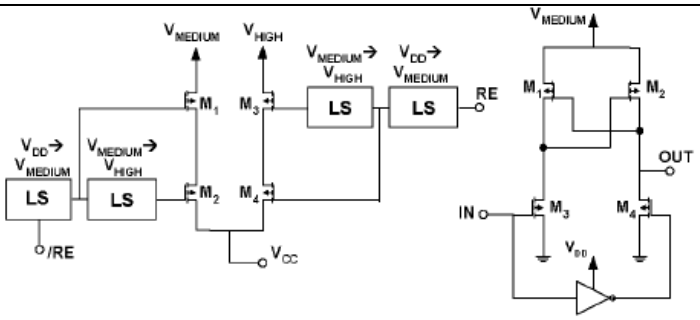


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading

1[d] an output of the first switch is coupled to a gate of the voltage applying transistor,

The Omnibus References disclose and/or render obvious an output of the first switch is coupled to a gate of the voltage applying transistor.

See, e.g.,

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a

regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

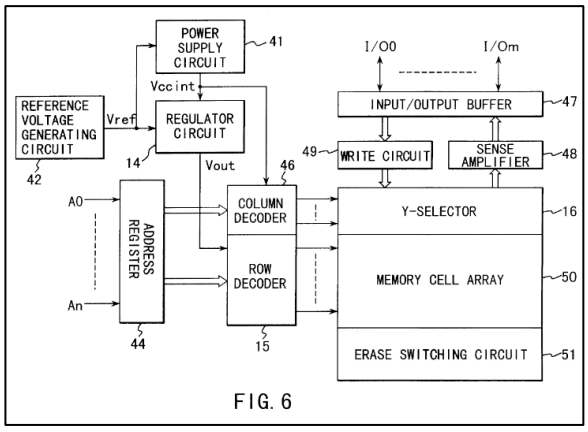


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

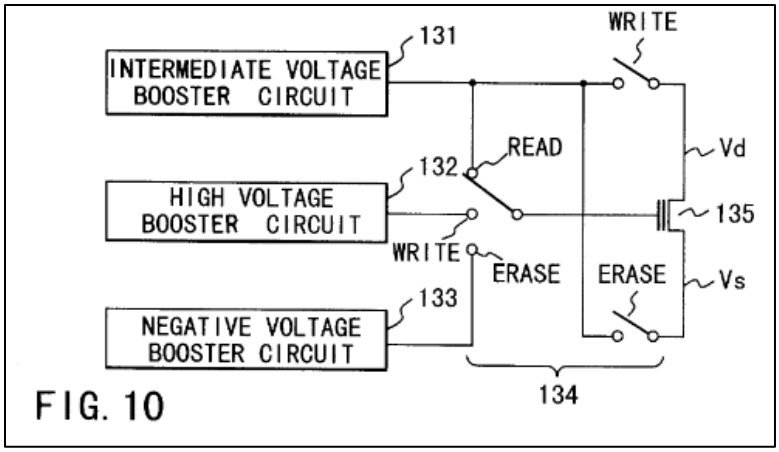


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

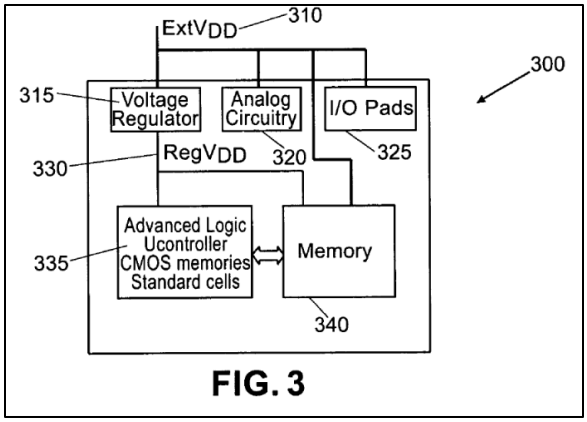


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

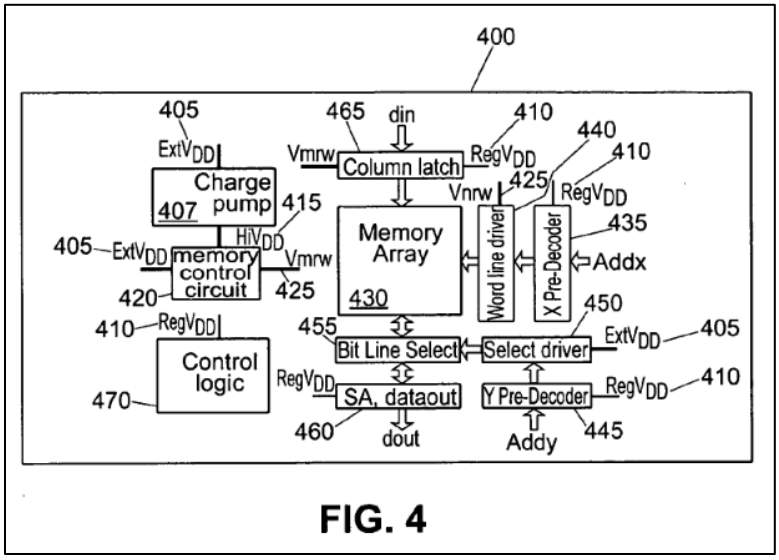


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

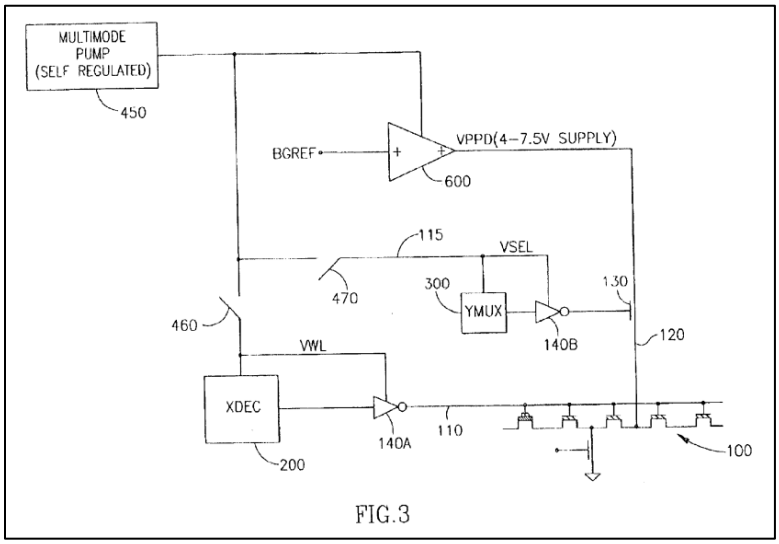


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

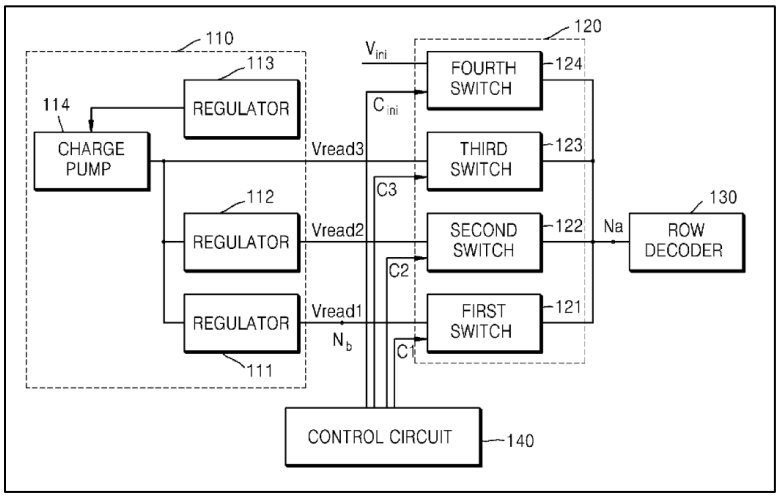
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

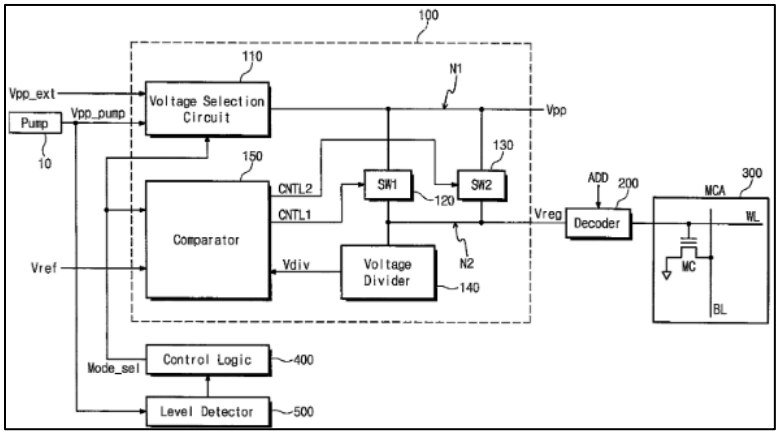
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

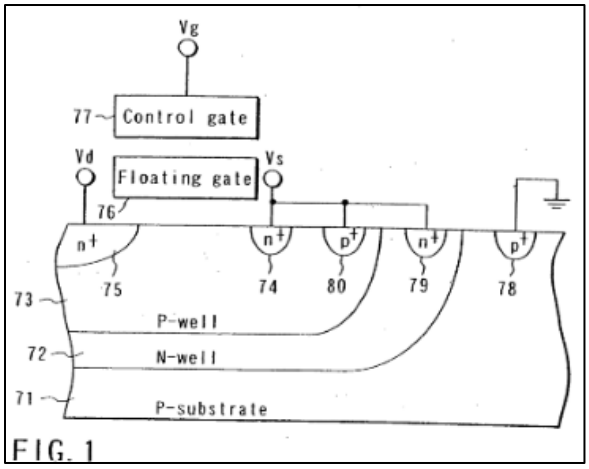


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

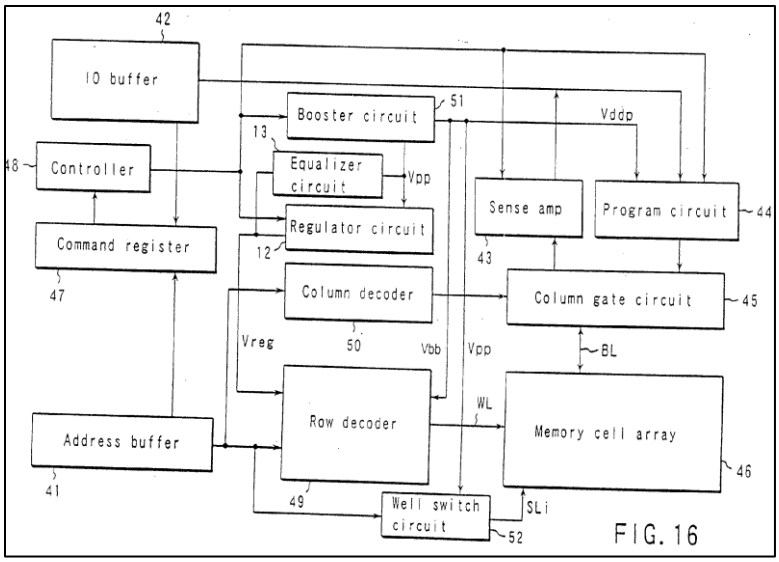


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

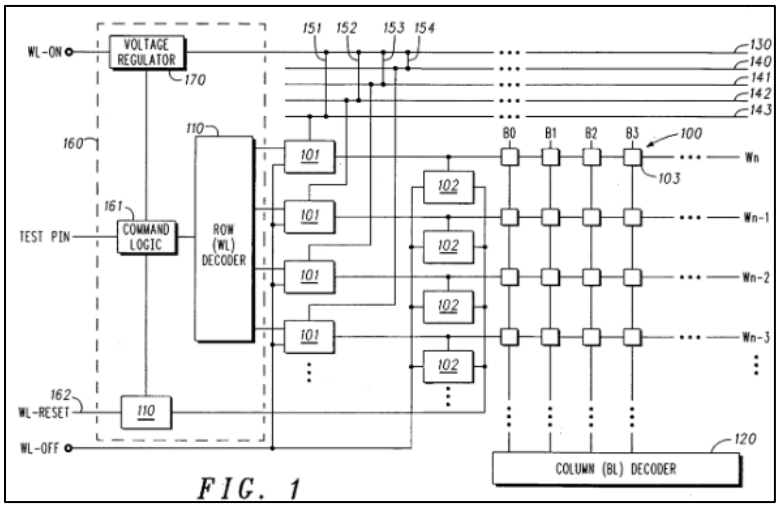


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

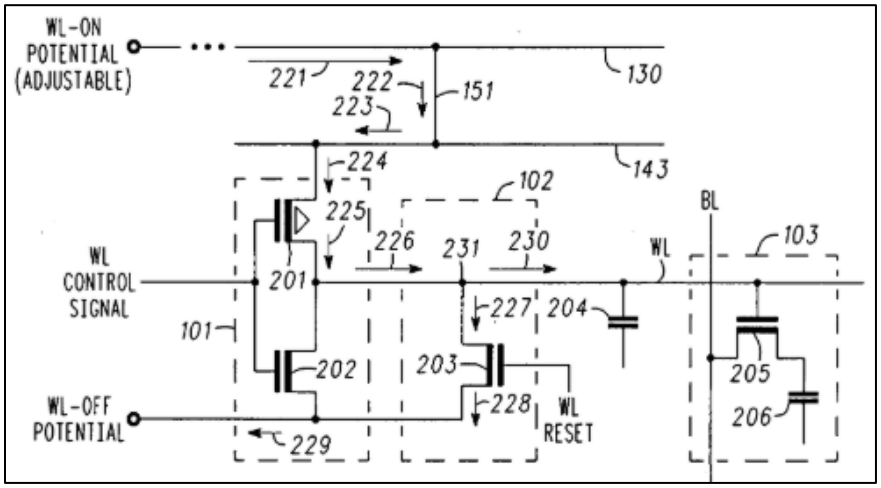


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

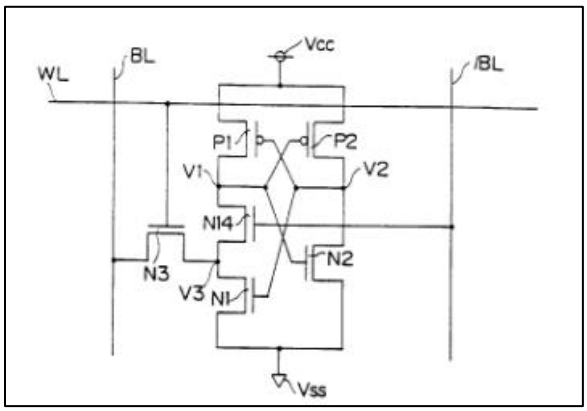
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

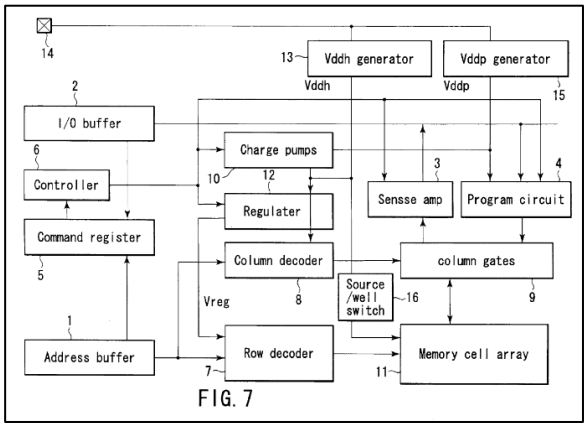


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

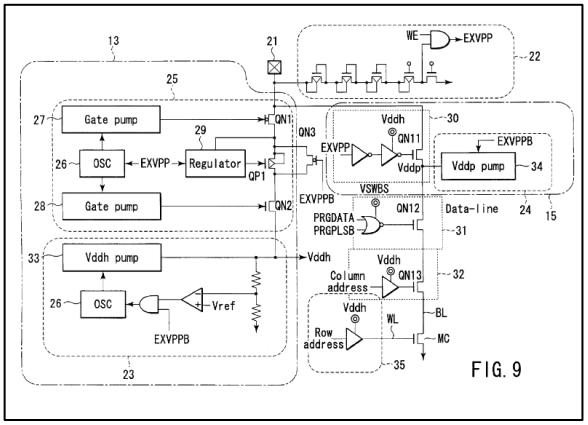


FIG. 9

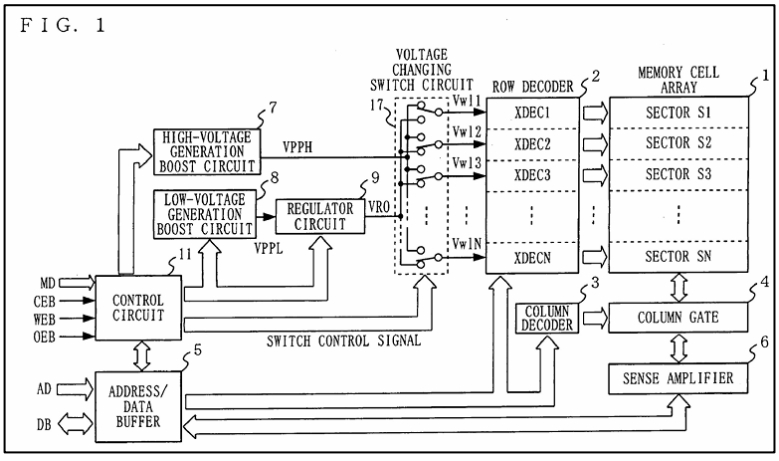
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

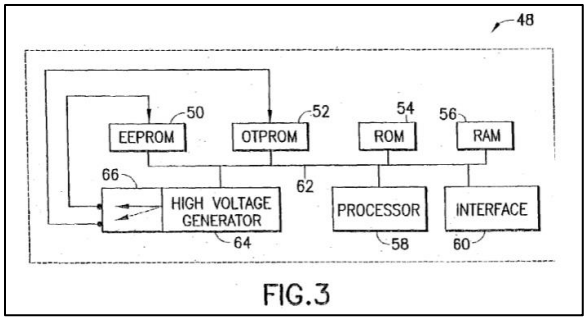


FIG.3

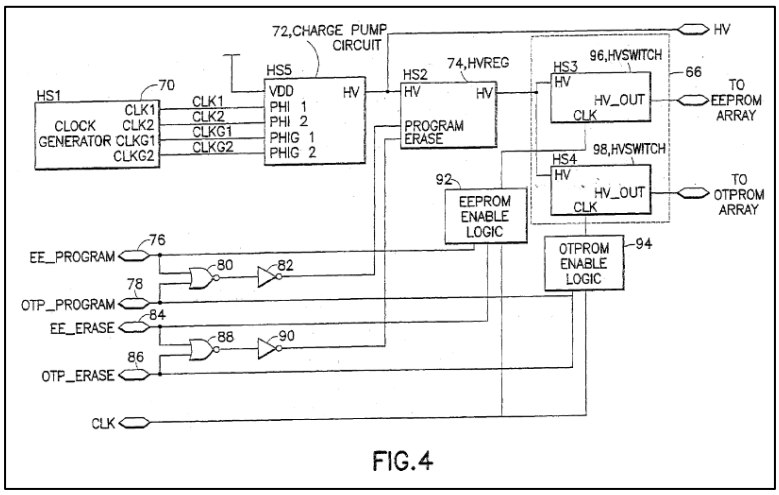


FIG.4

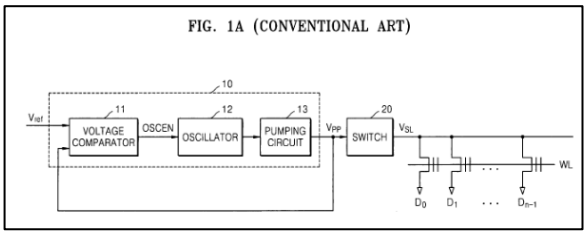
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

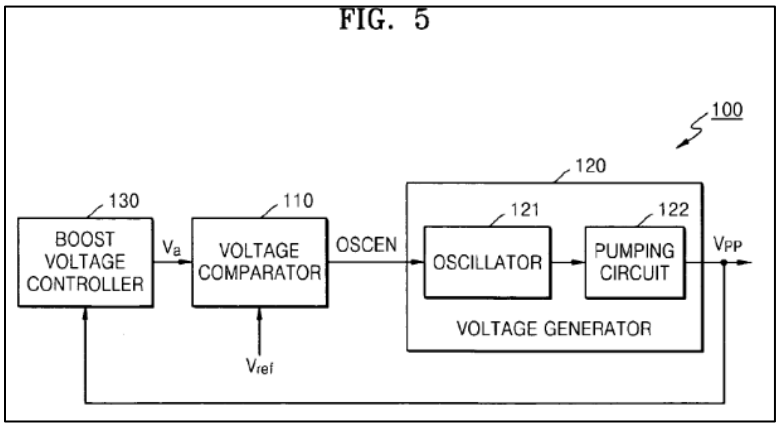
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

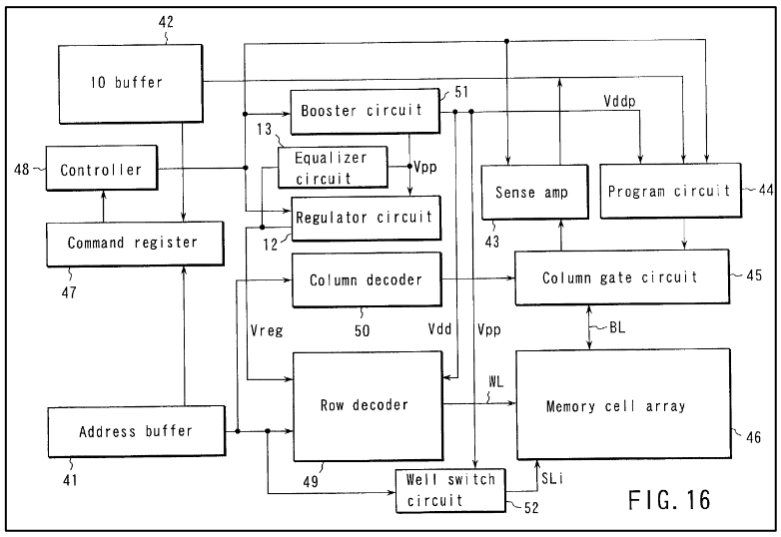


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

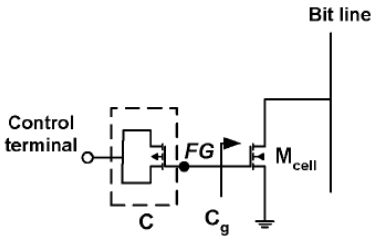


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

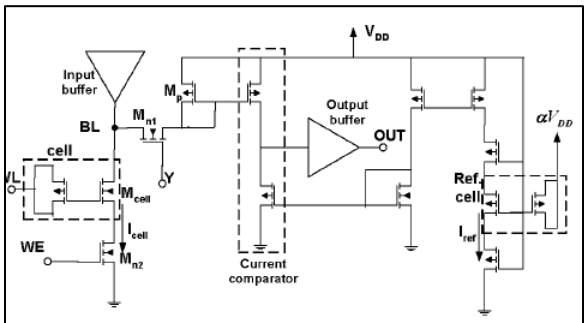


Figure 3. Current mode Sense Amplifier.

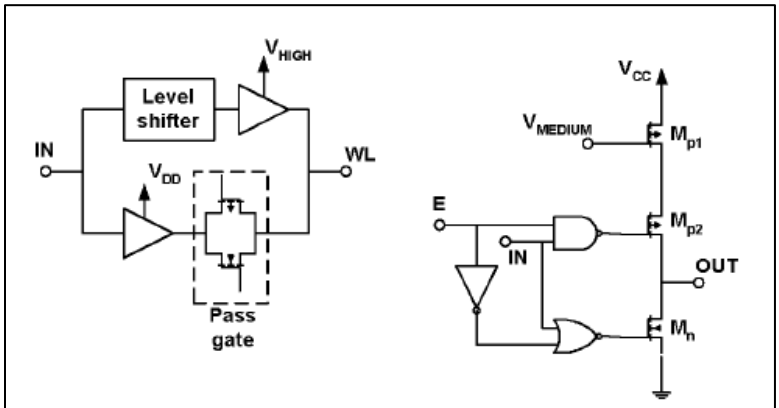


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

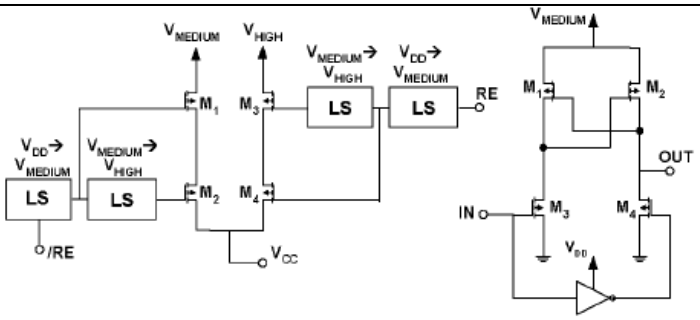


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

1[e] a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell,

The Omnibus References disclose and/or render obvious a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell.

See, e.g.:

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for

regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

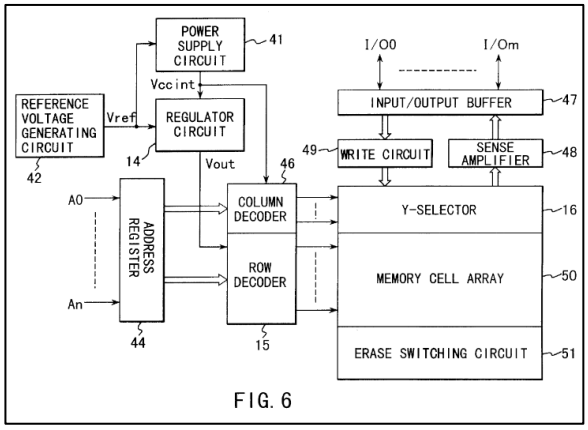


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

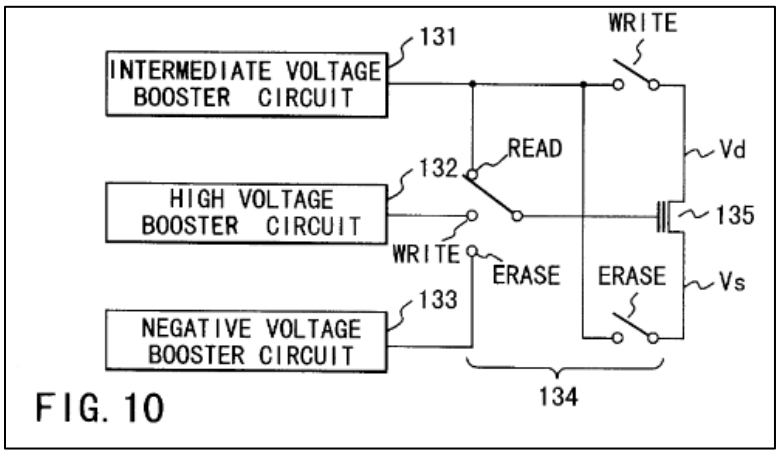


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

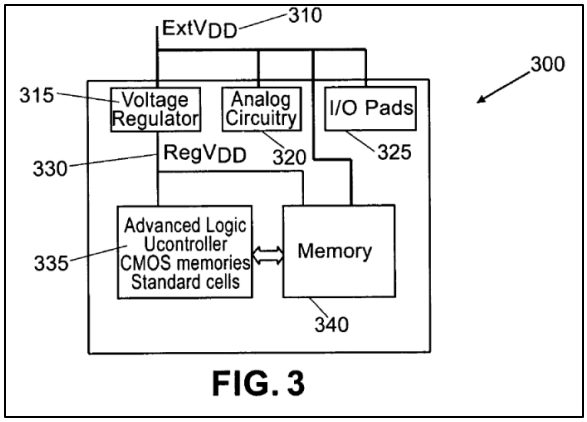


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

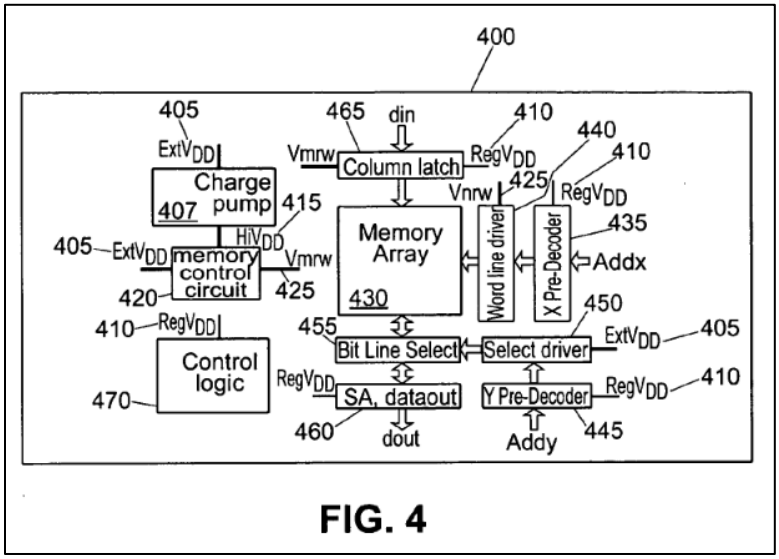


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

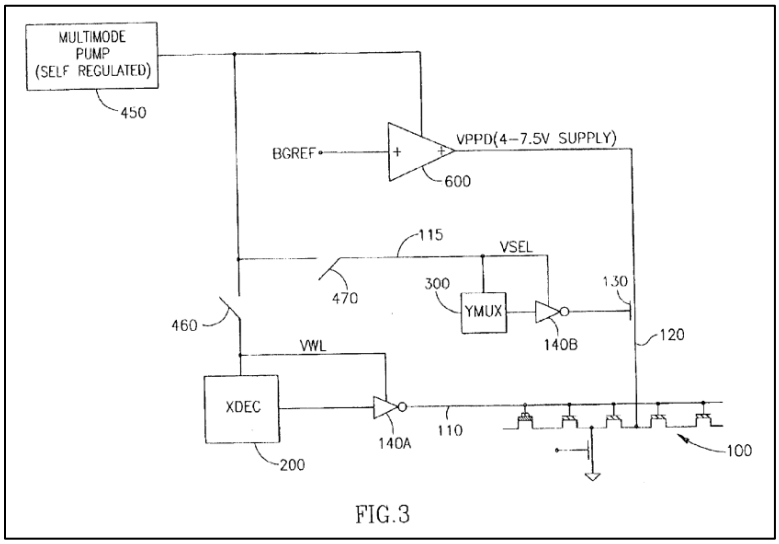


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

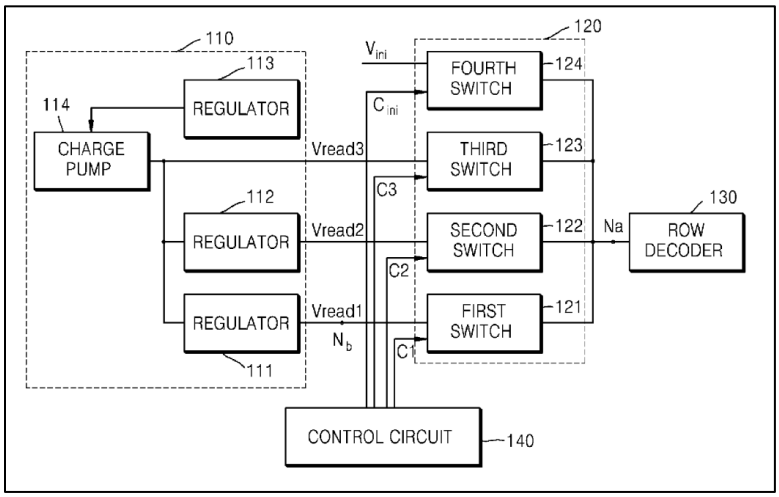
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

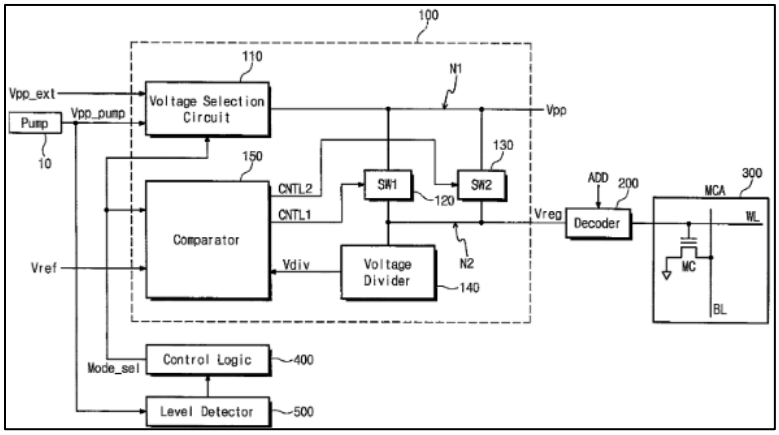
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Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

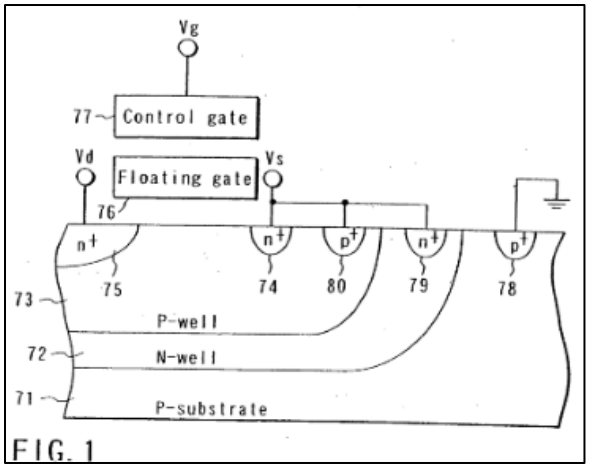


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

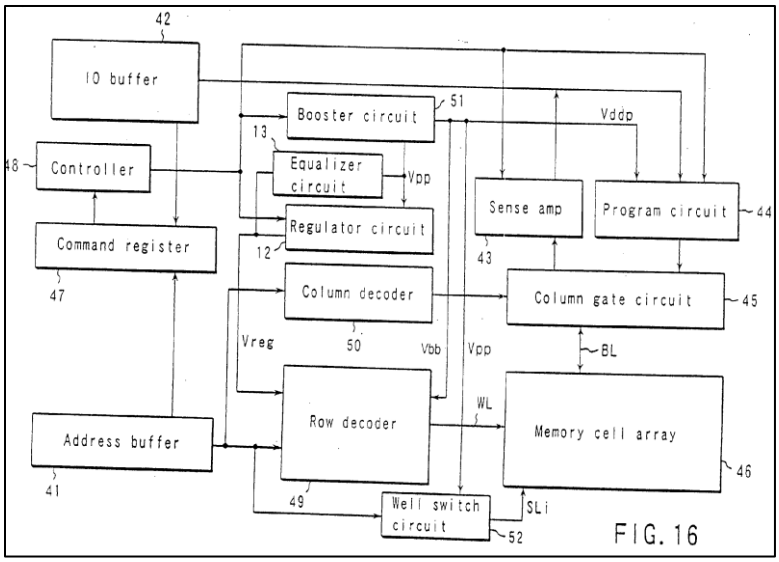


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

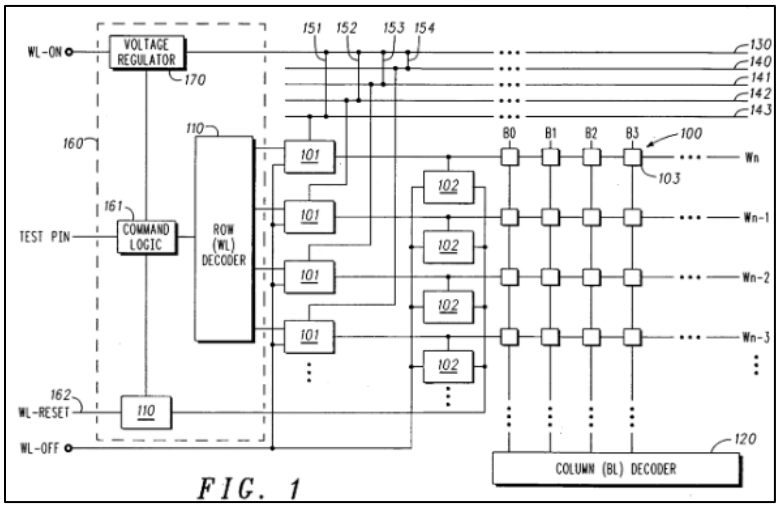


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

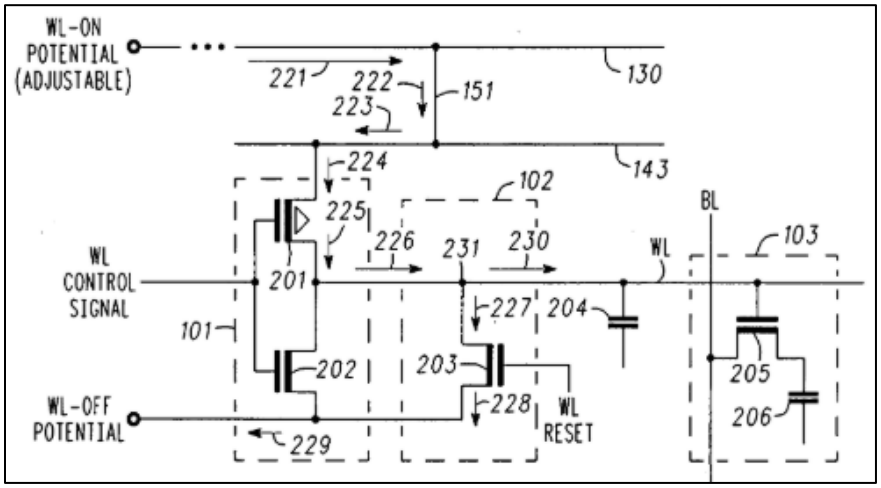


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

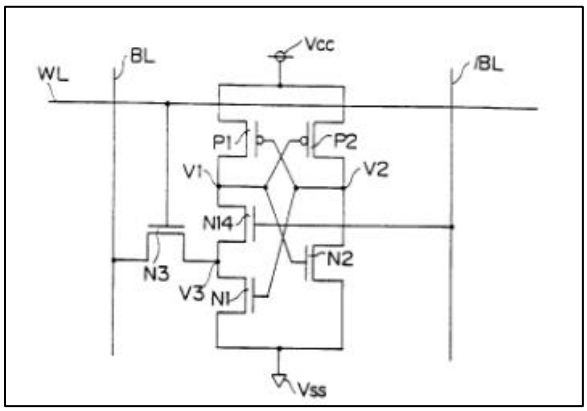
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

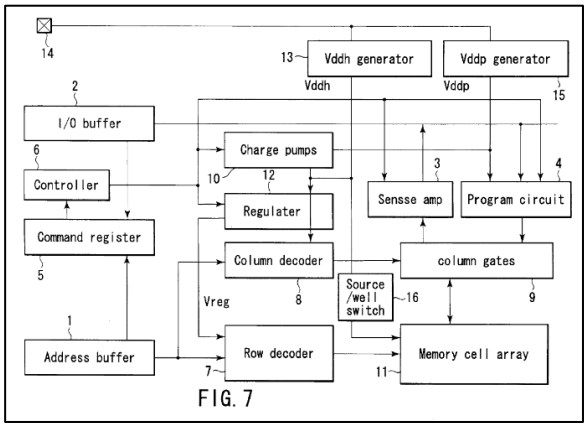


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

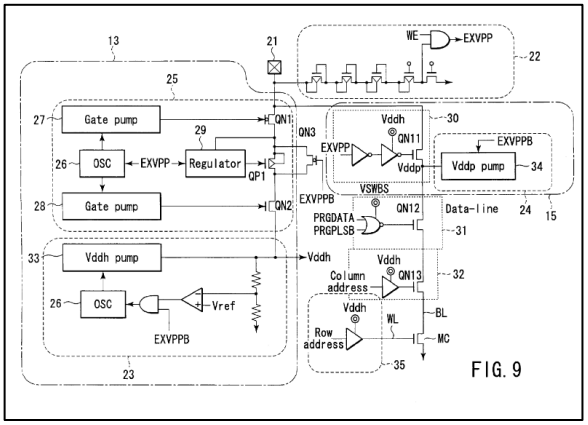


FIG. 9

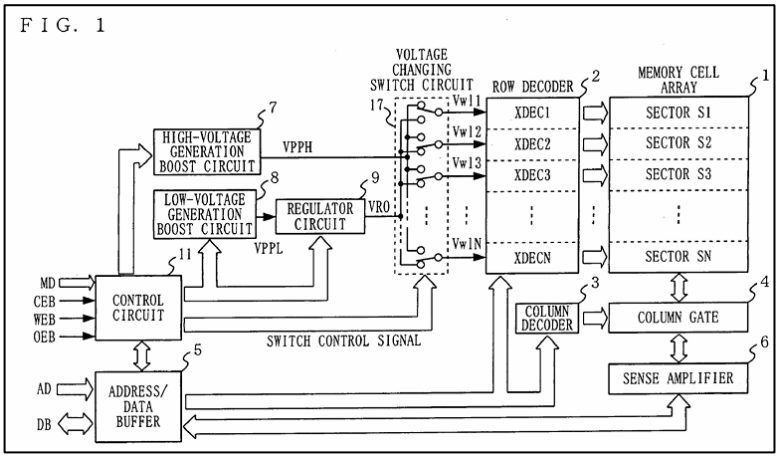
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

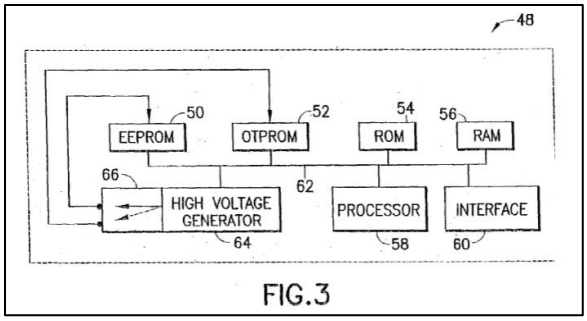


FIG.3

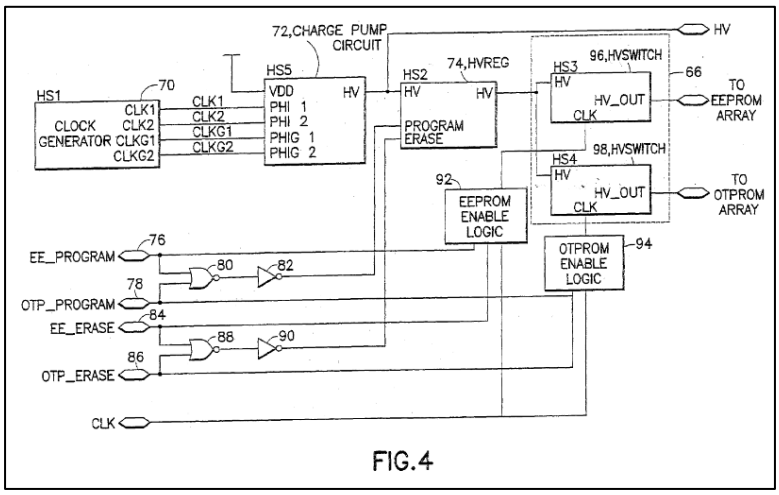


FIG.4

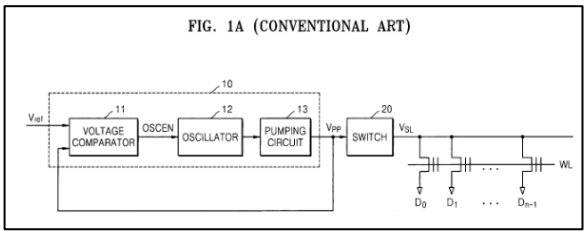
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

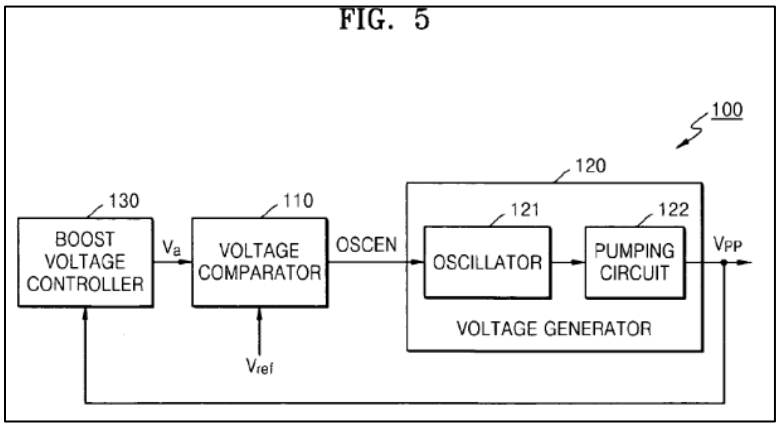
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

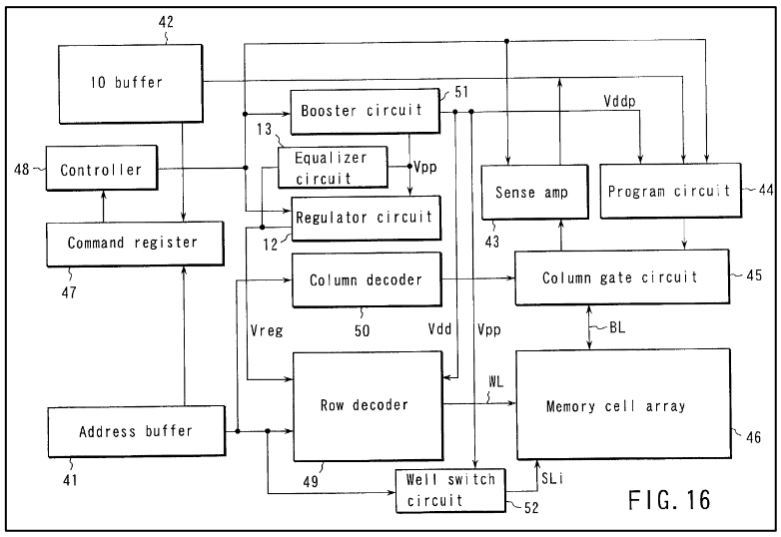
The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.



Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

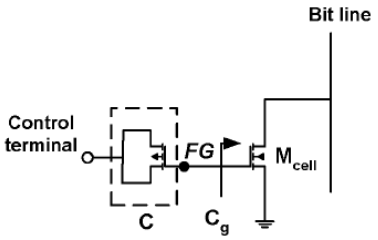


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

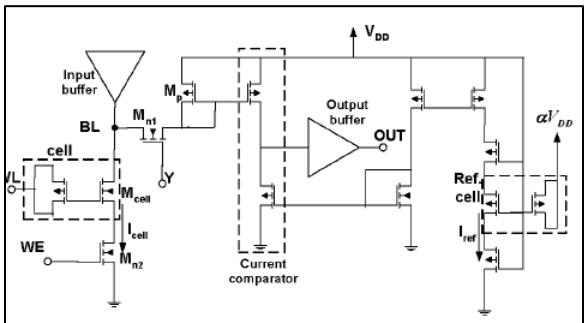


Figure 3. Current mode Sense Amplifier.

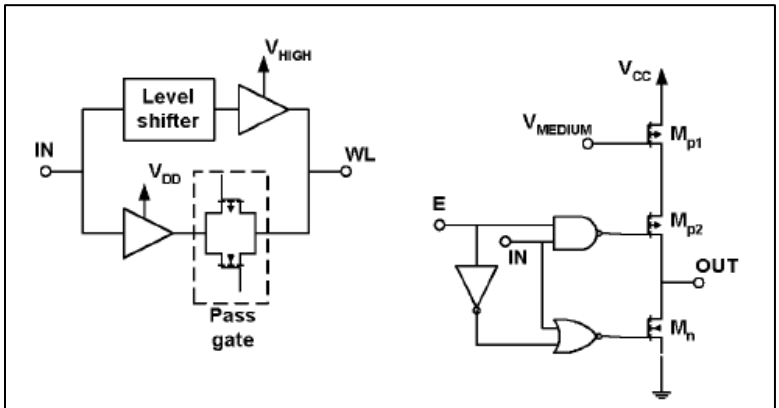


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

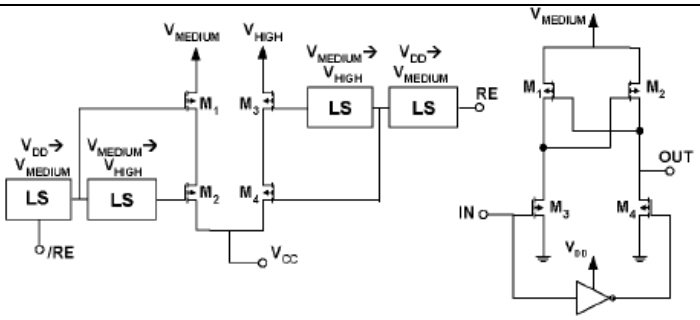


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

1[f] and an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

The Omnibus References disclose and/or render obvious and an output of the second switch is coupled to a gate of the memory cell for application of a voltage.

See, e.g.:

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for

regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

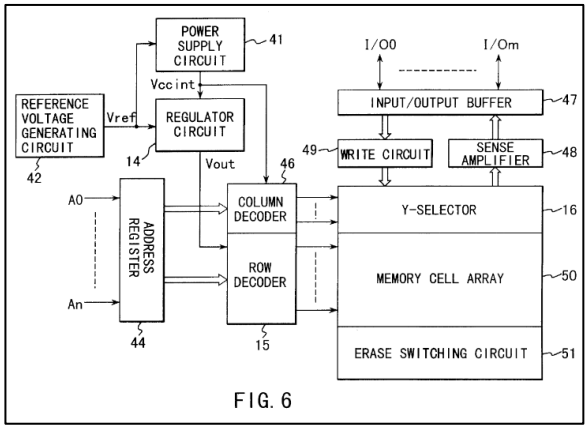


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

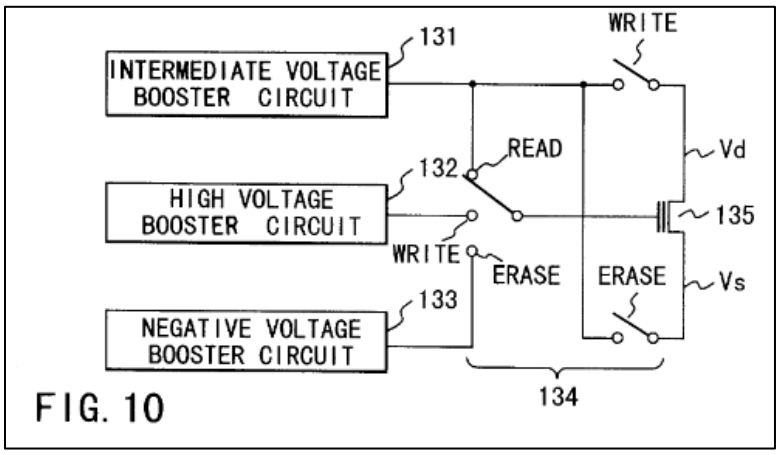


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

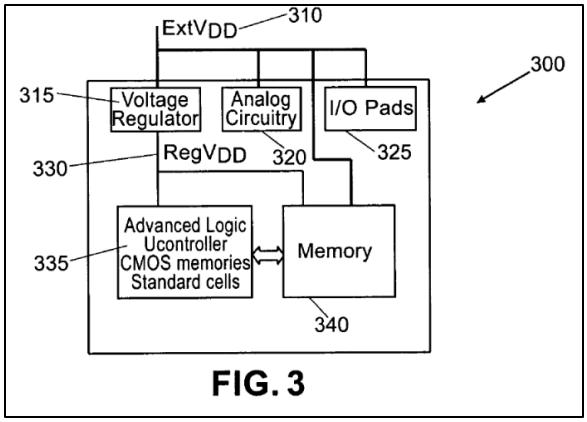


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

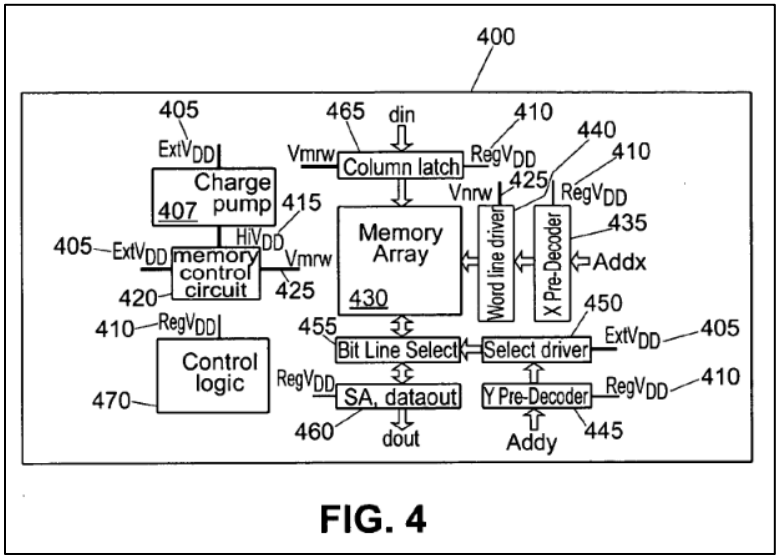


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

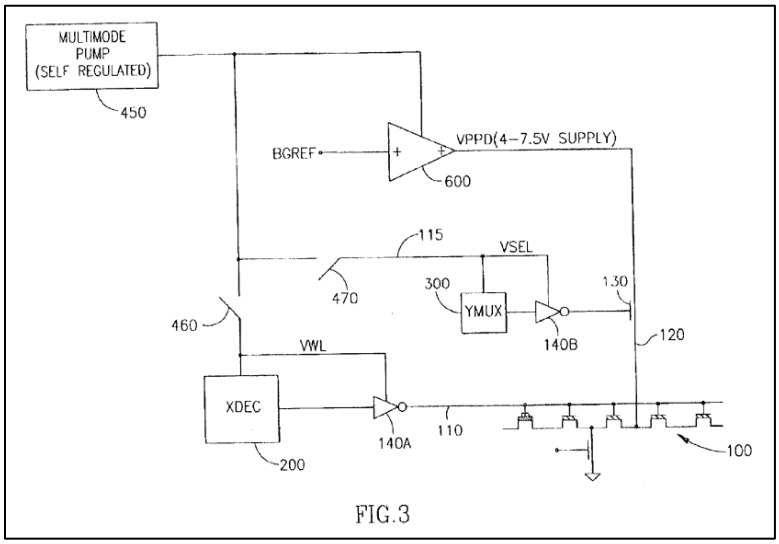


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

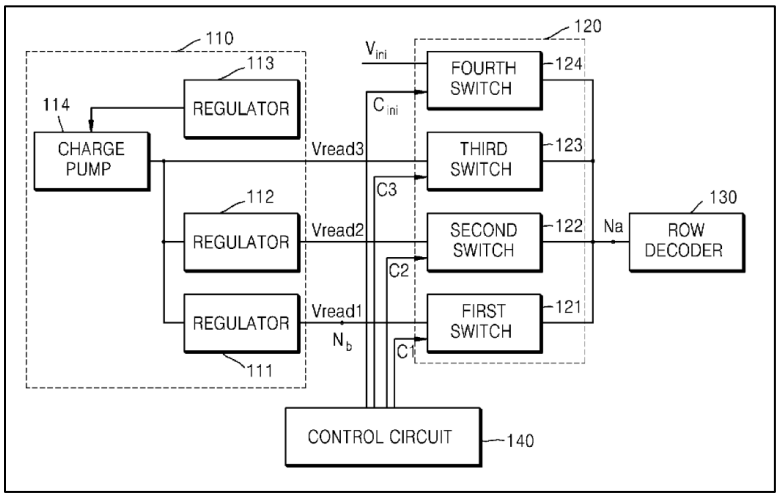
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

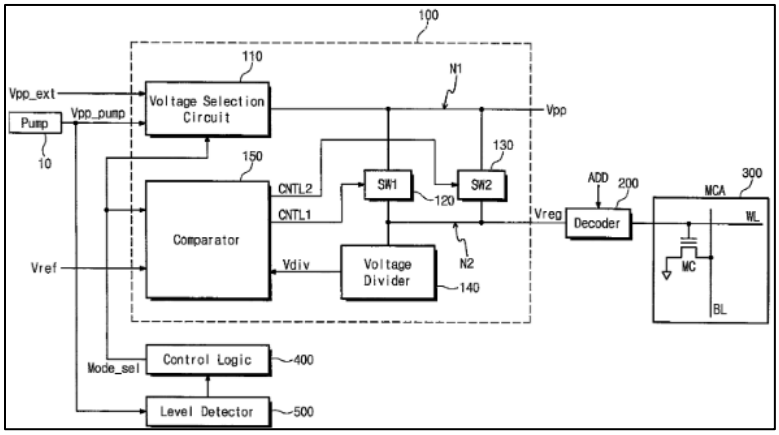
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

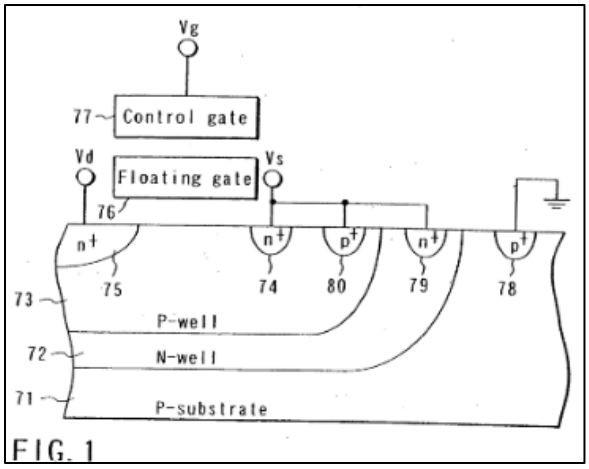


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

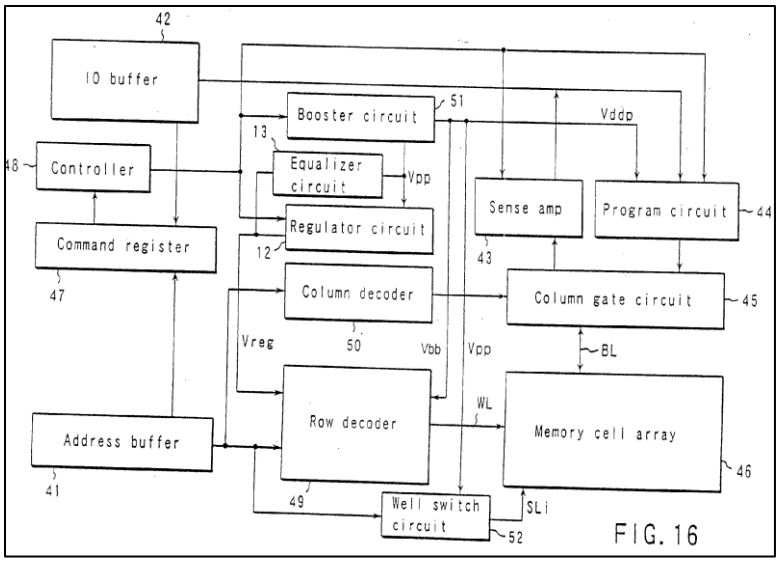


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

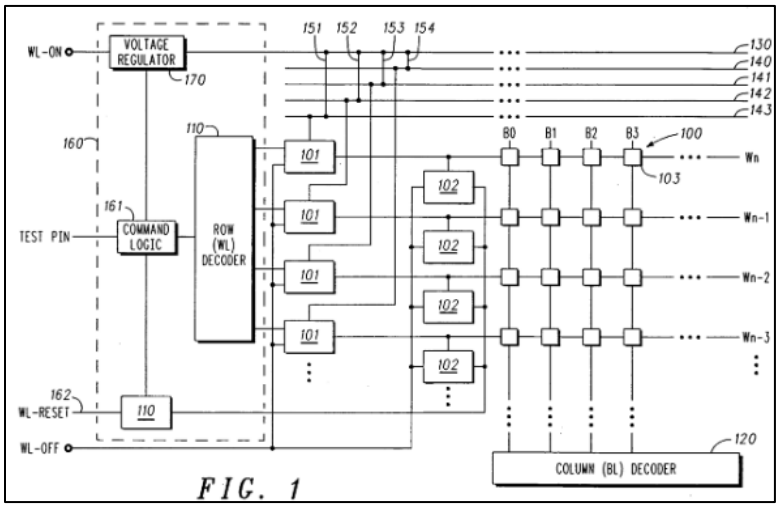


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

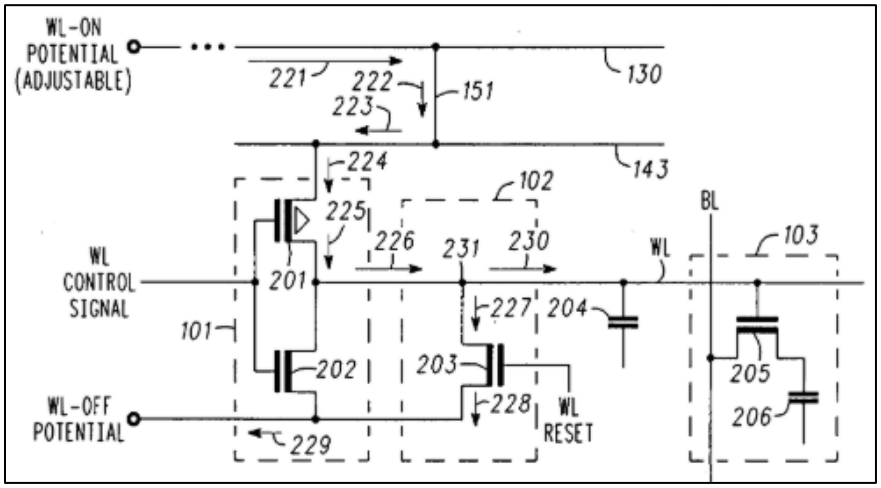


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

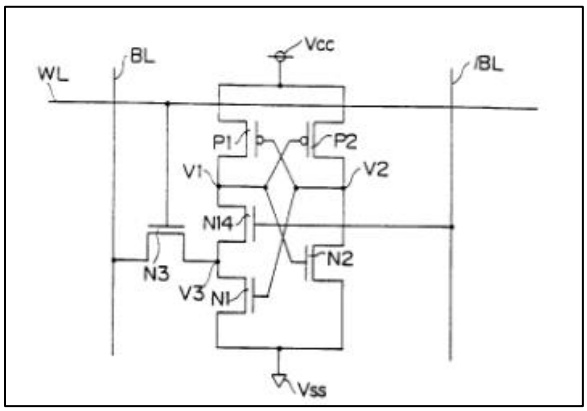
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

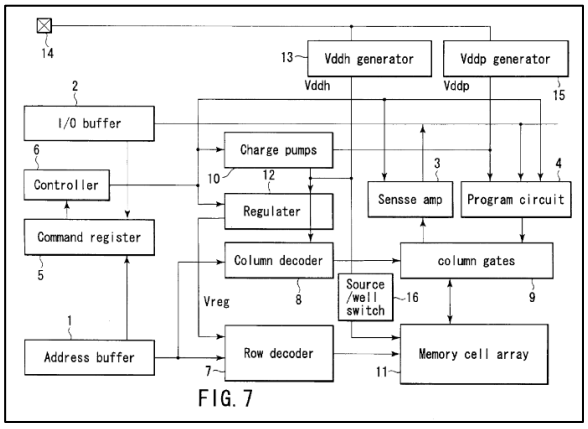


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

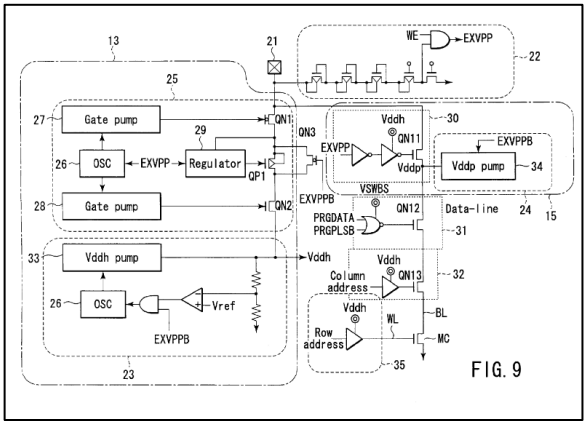


FIG. 9

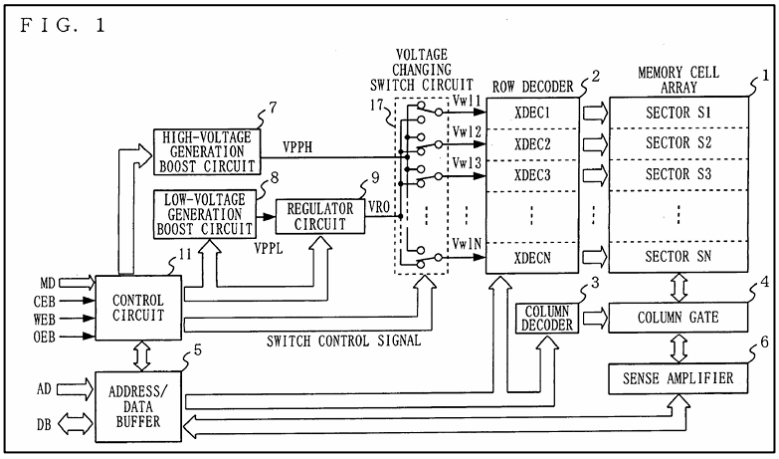
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

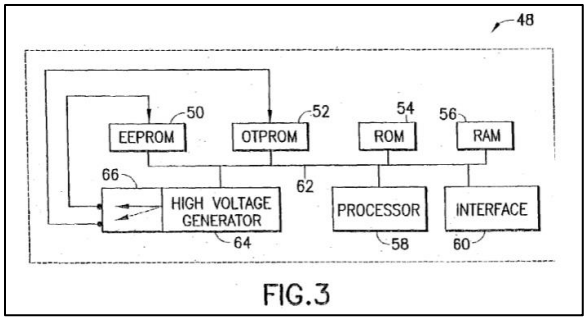


FIG.3

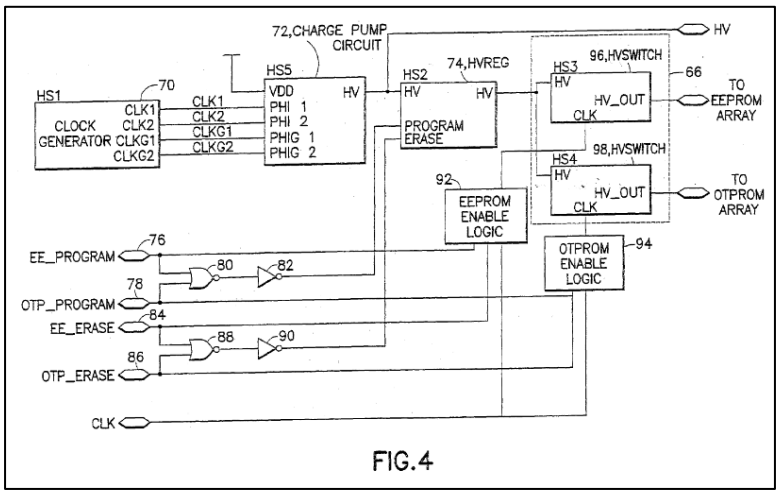


FIG.4

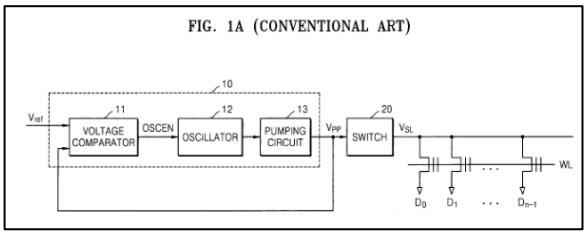
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

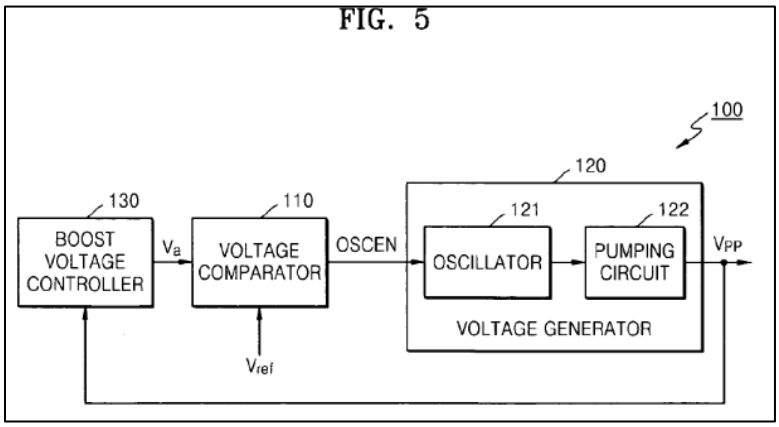
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

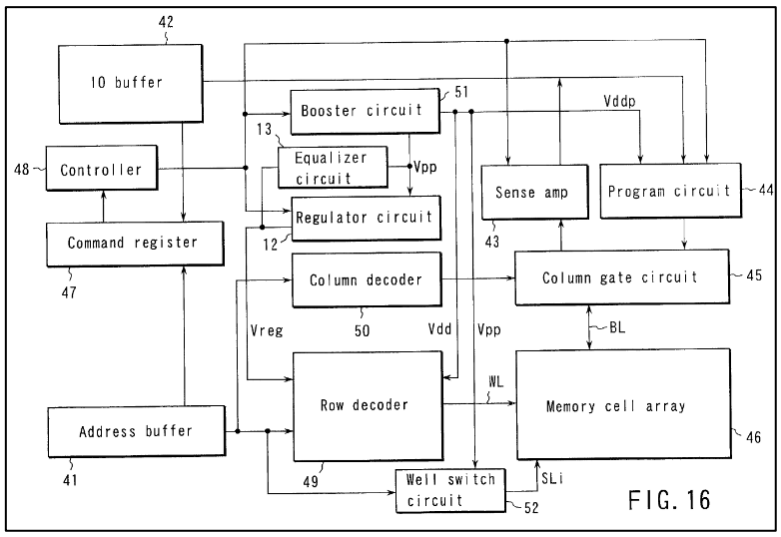


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

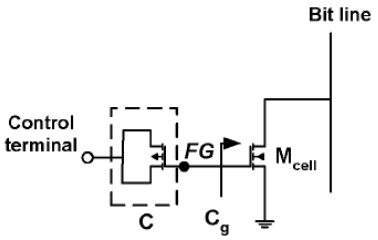


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

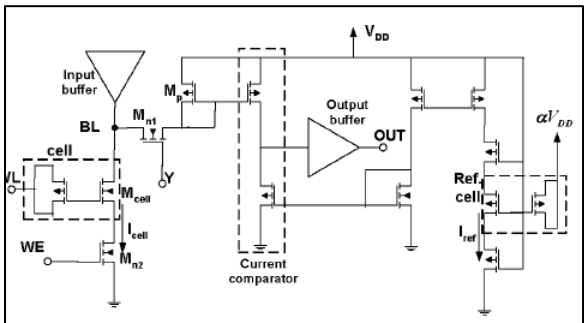


Figure 3. Current mode Sense Amplifier.

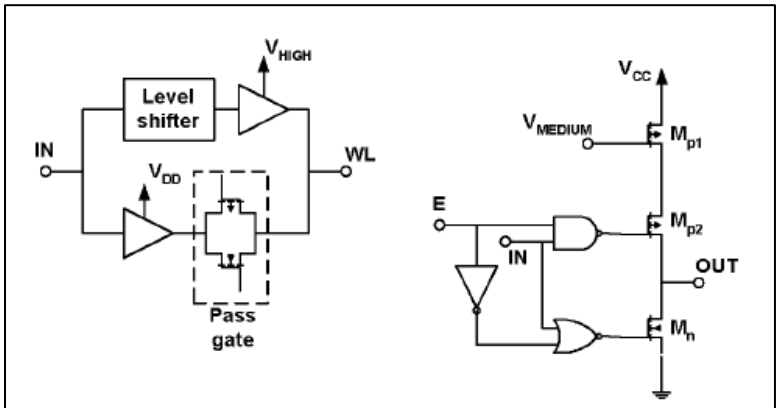


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

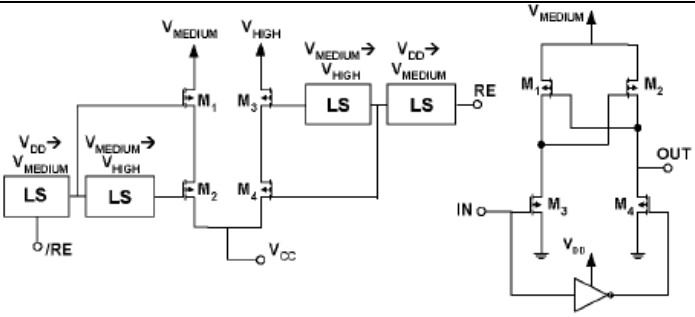


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

3[a] The semiconductor memory device of claim 1, wherein

The Omnibus References disclose and/or render obvious the semiconductor memory device of claim 1.

See, e.g.: claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

3[b] an output of a fourth switch is coupled to the output of the second switch, and

The Omnibus References disclose and/or render obvious an output of a fourth switch is coupled to the output of the second switch.

See, e.g.: claim limitation 1[b], *supra*.

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating

a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

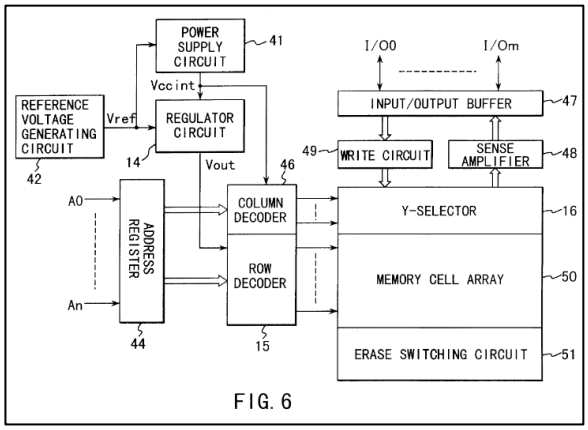


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50

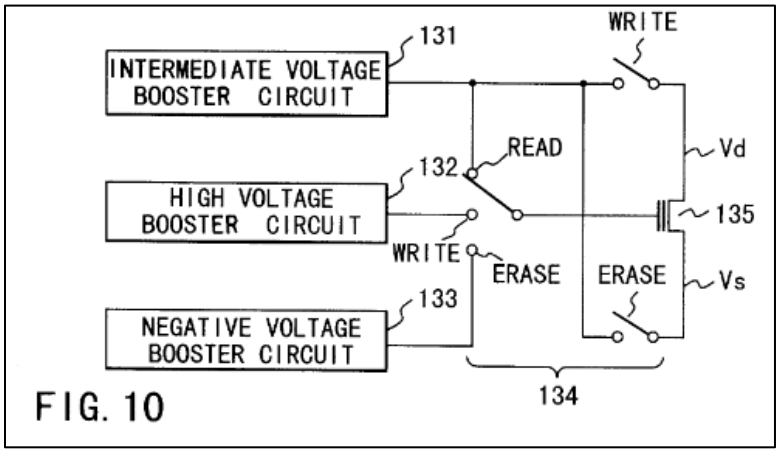
by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.



The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is

distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

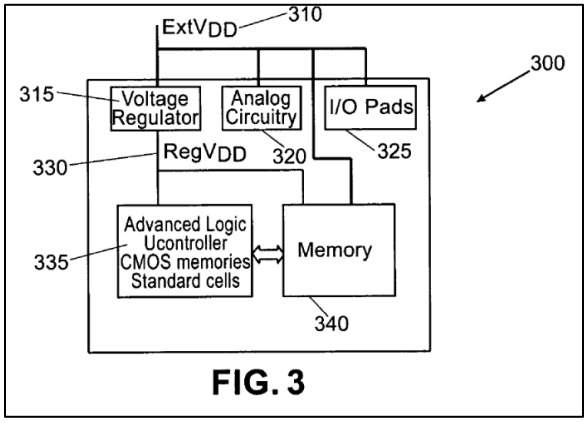


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

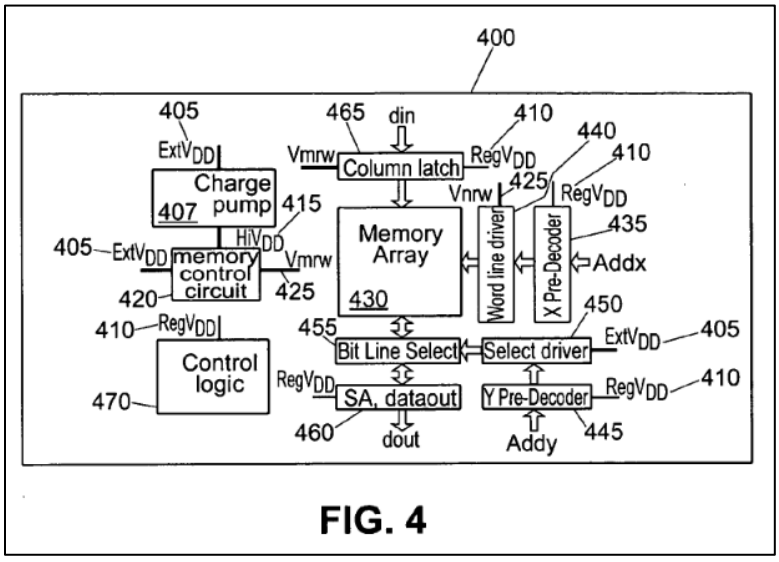


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory

control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

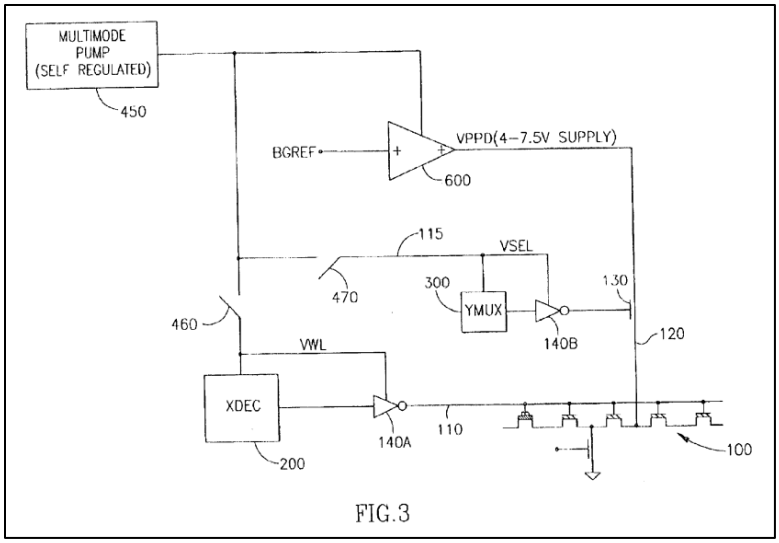


FIG.3

Shor at 2:42-61:

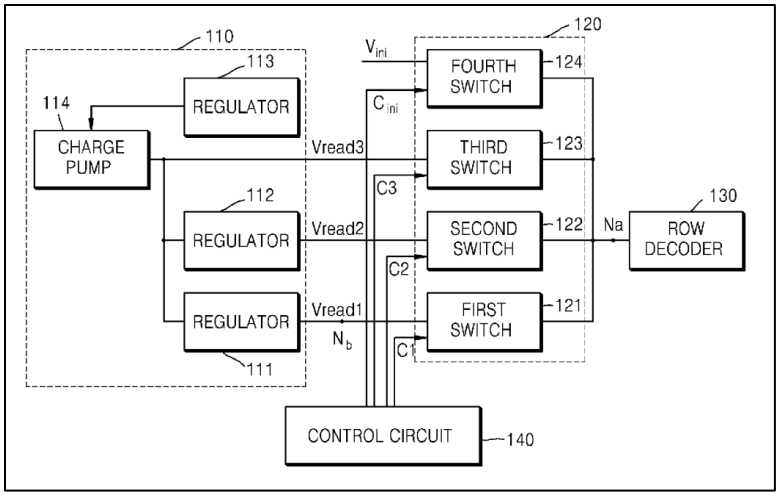
As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled “Efficient Charge Pump with Constant Boosted Output Voltage” by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively

low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

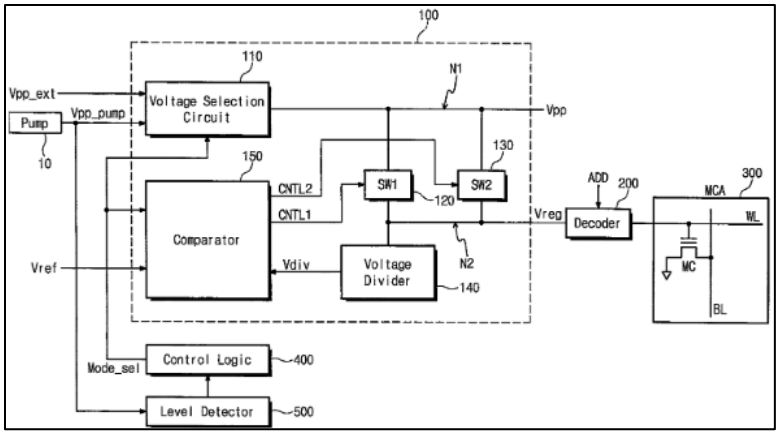
Cho at 2:24-64:

Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit, the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and

a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

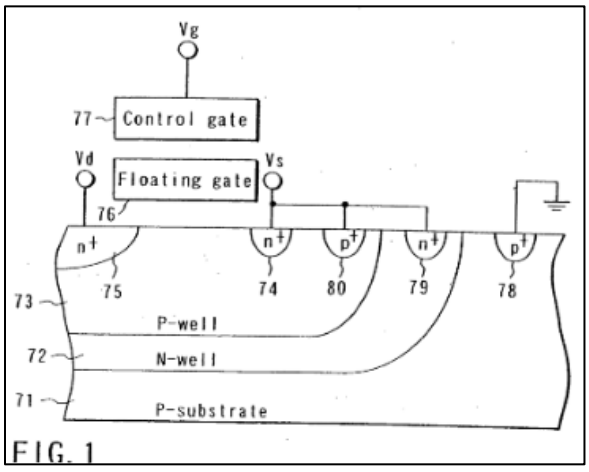


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

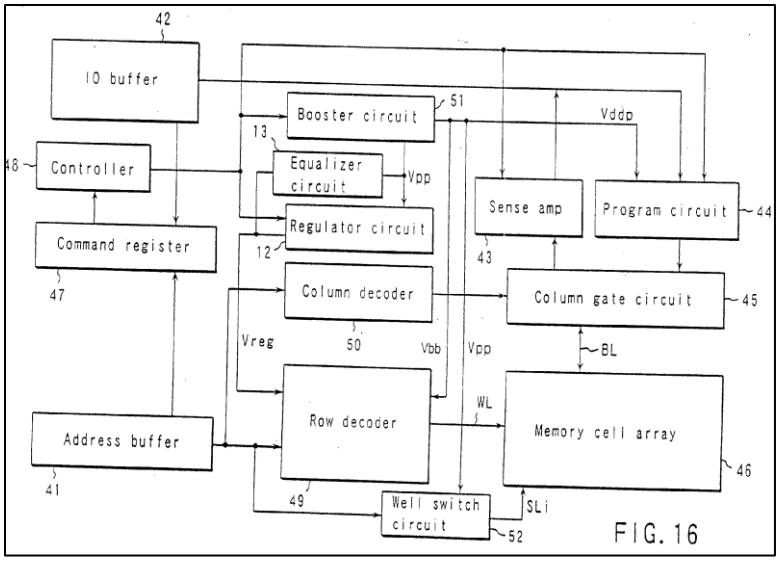


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1,

Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

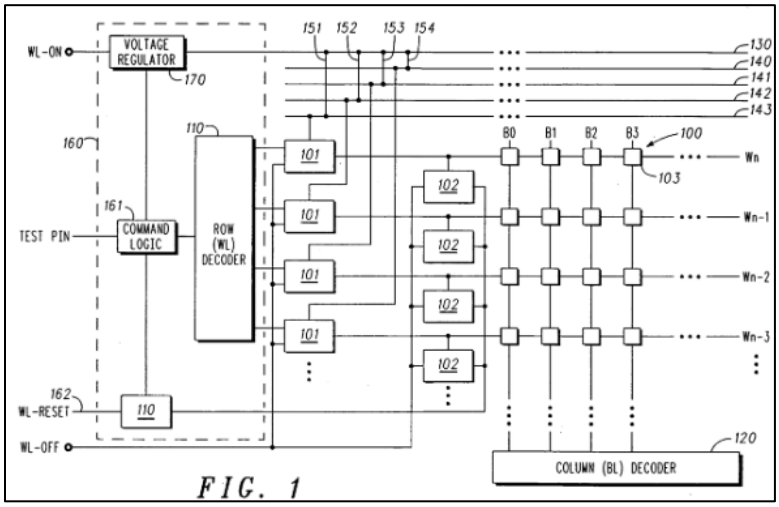


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

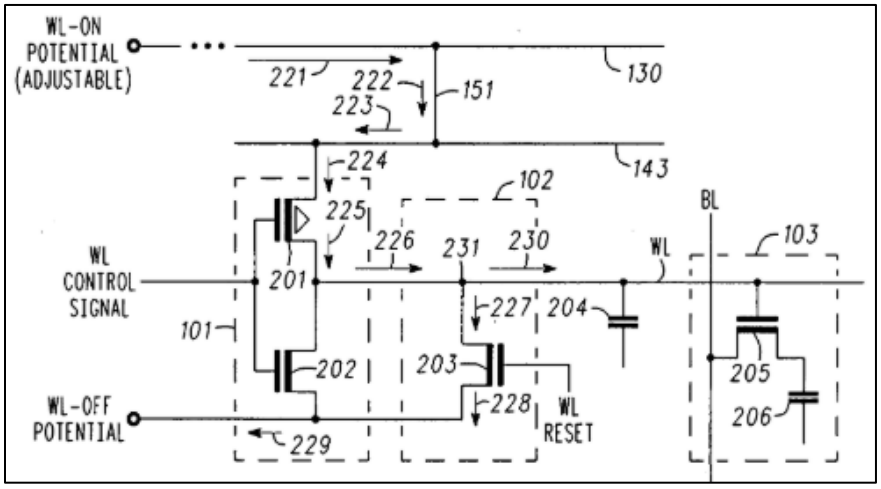


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

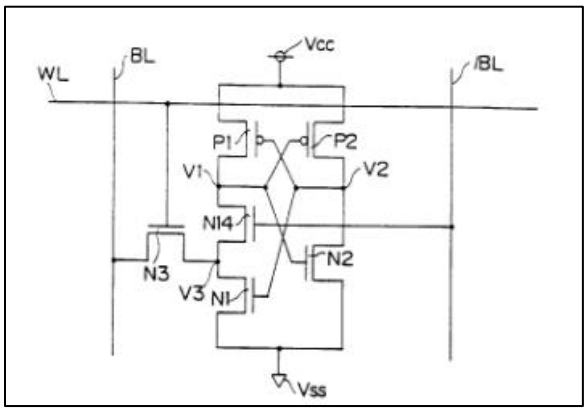
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is

controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the

columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

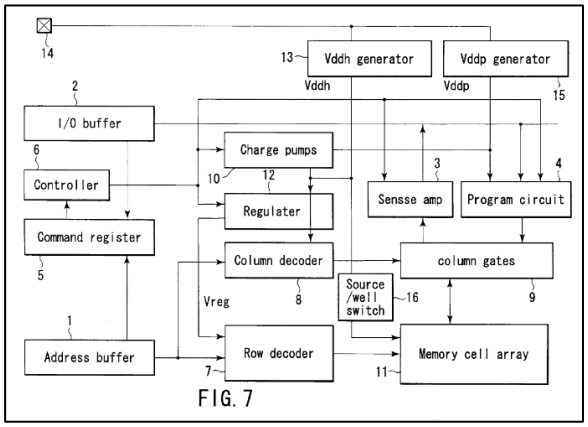


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

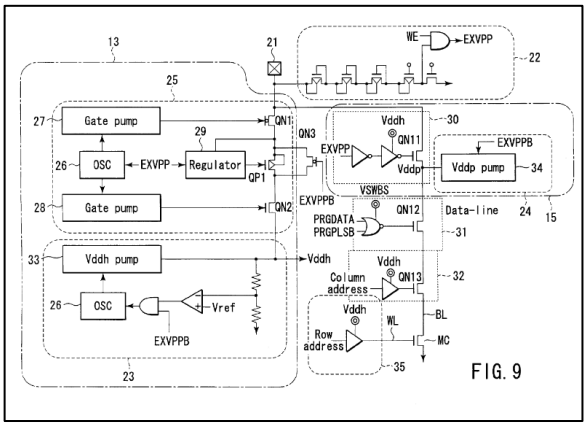


FIG. 9

Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

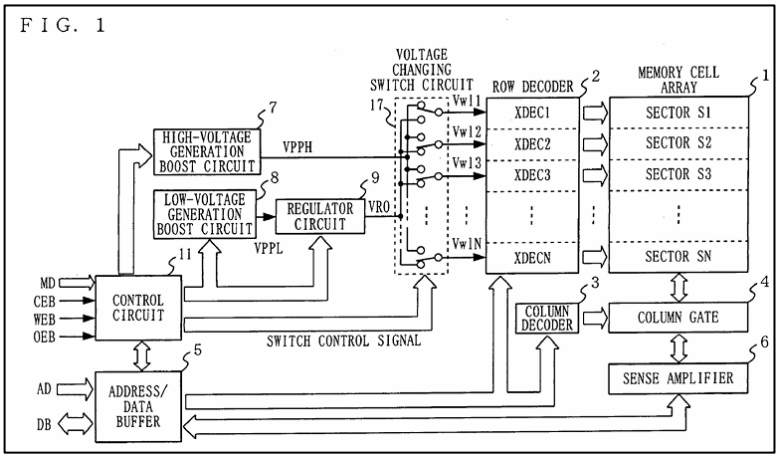
Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17

comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.

FIG. 1



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

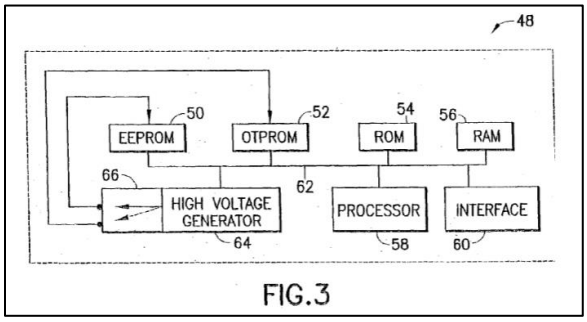


FIG.3

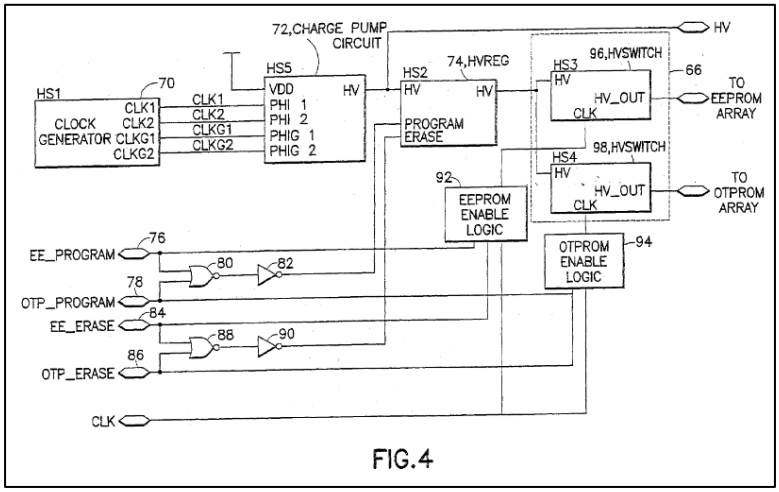


FIG.4

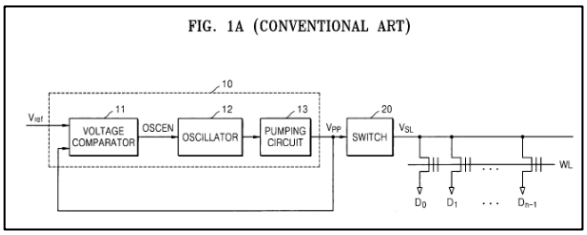
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

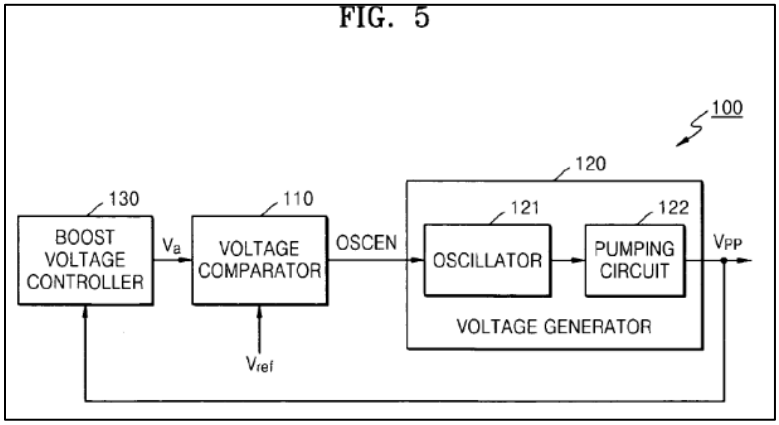
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

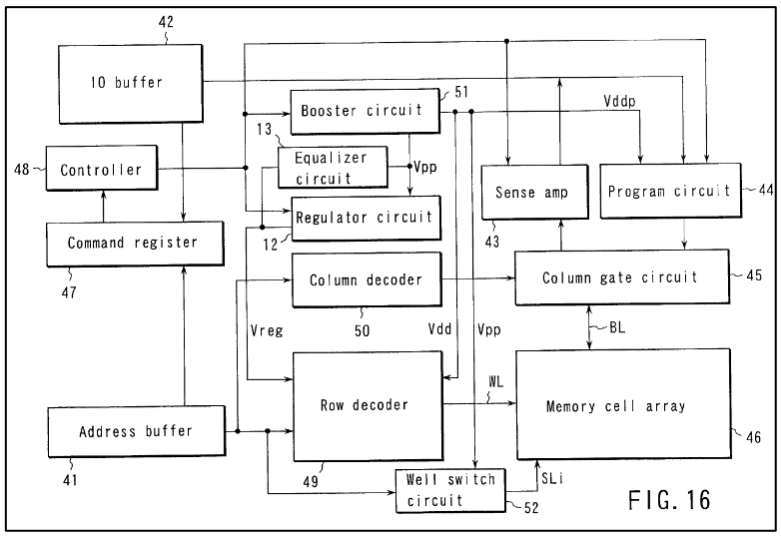


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

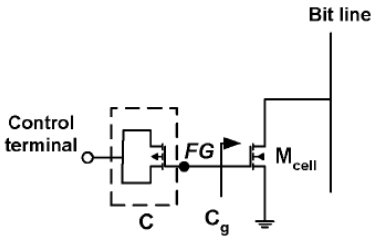


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

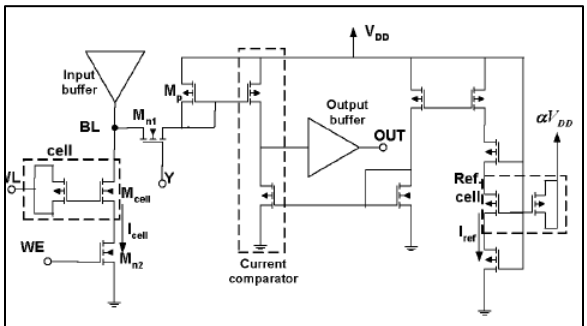


Figure 3. Current mode Sense Amplifier.

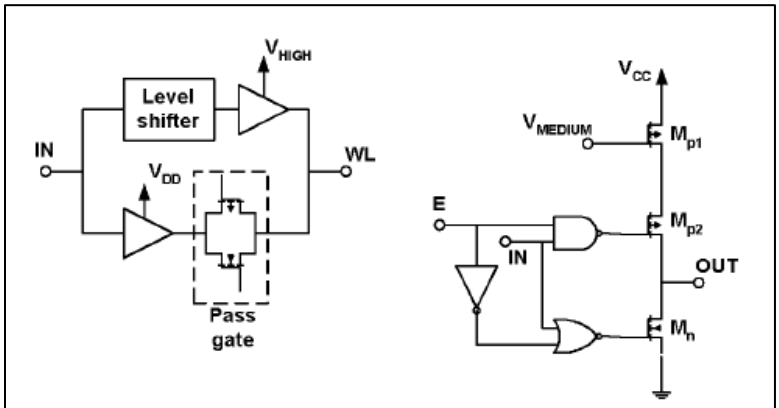


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

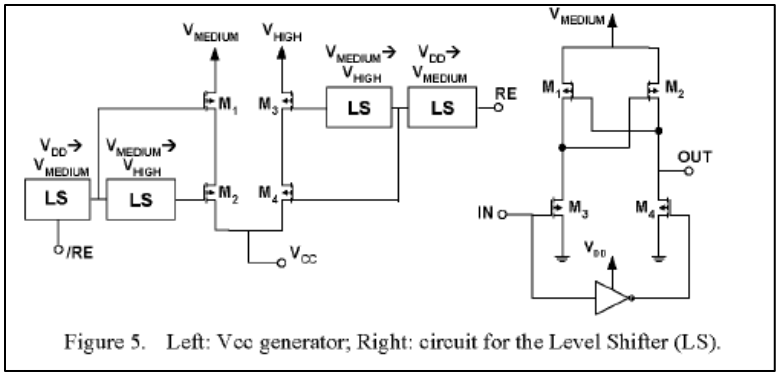


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

3[c] a voltage different from the output of the regulator is applied to the gate of the memory cell.

The Omnibus References disclose and/or render obvious a voltage different from the output of the regulator is applied to the gate of the memory cell.

See, e.g., claim limitation 1[c], *supra*.

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for

regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

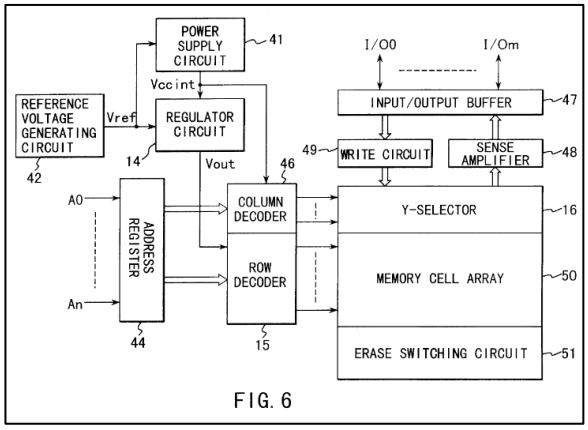


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

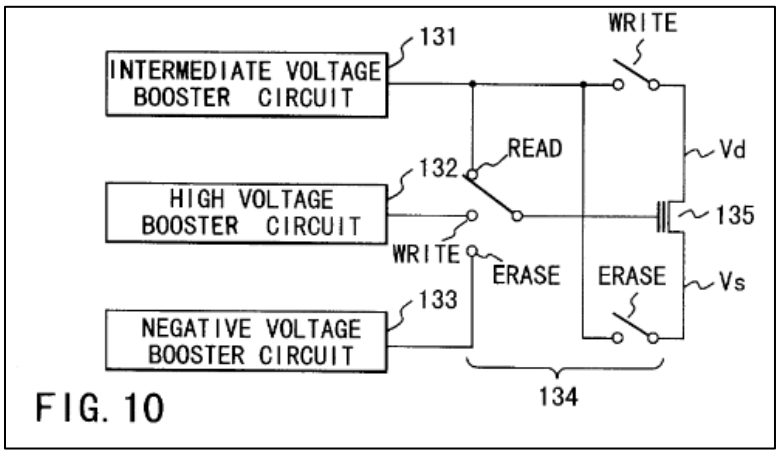


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

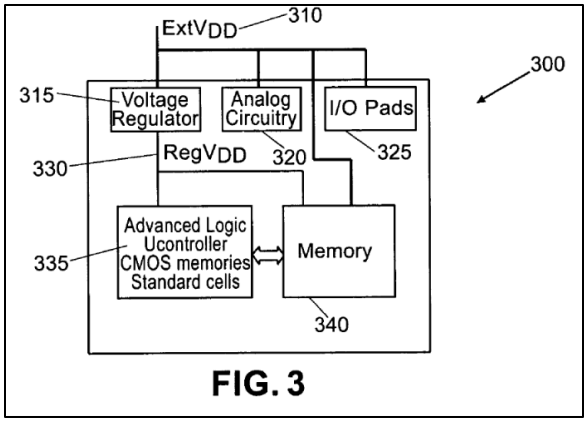


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

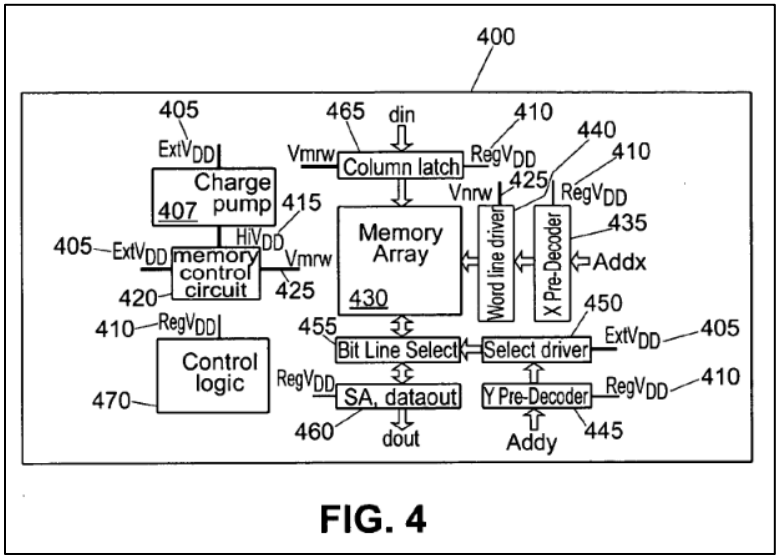


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

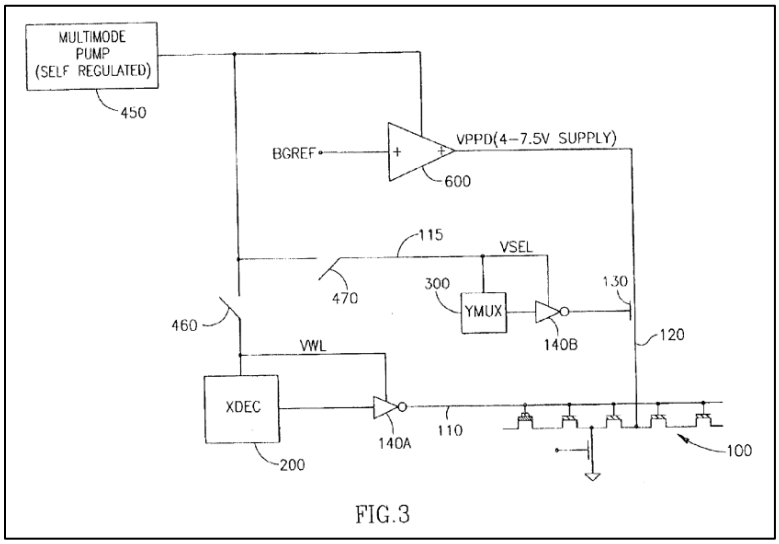


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

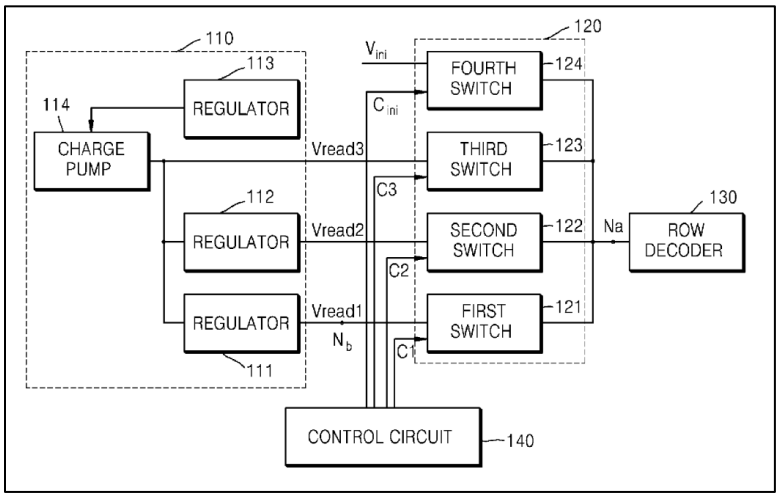
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

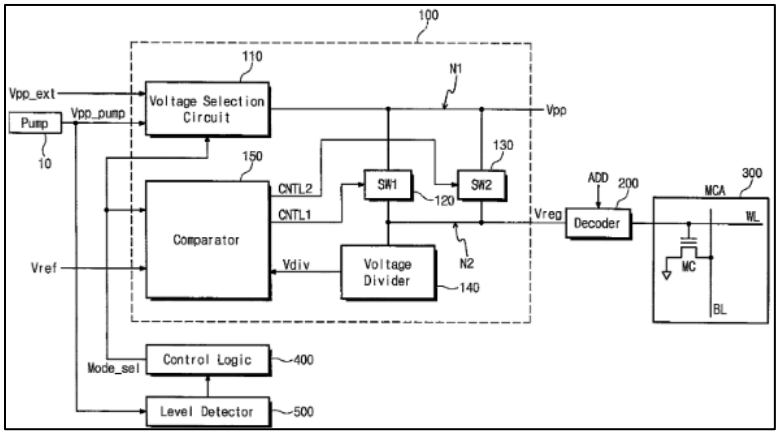
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

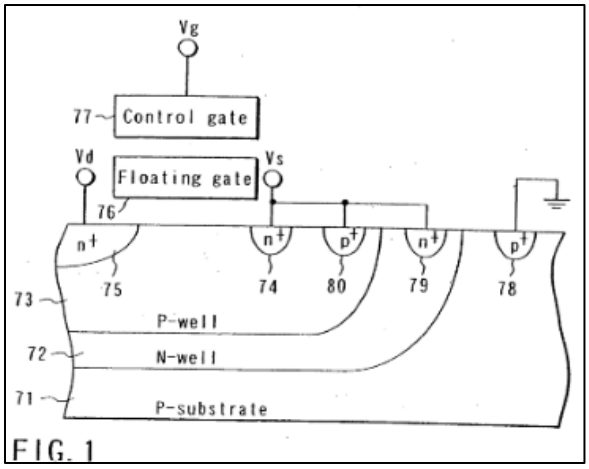


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

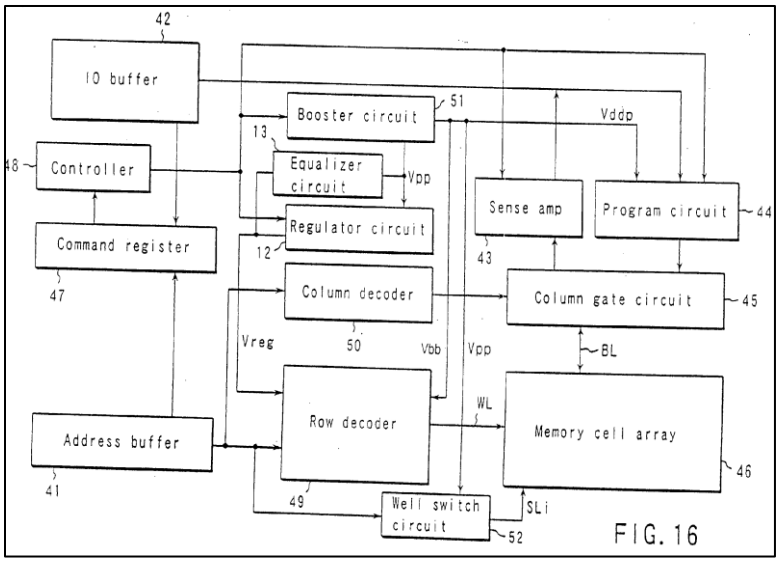


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

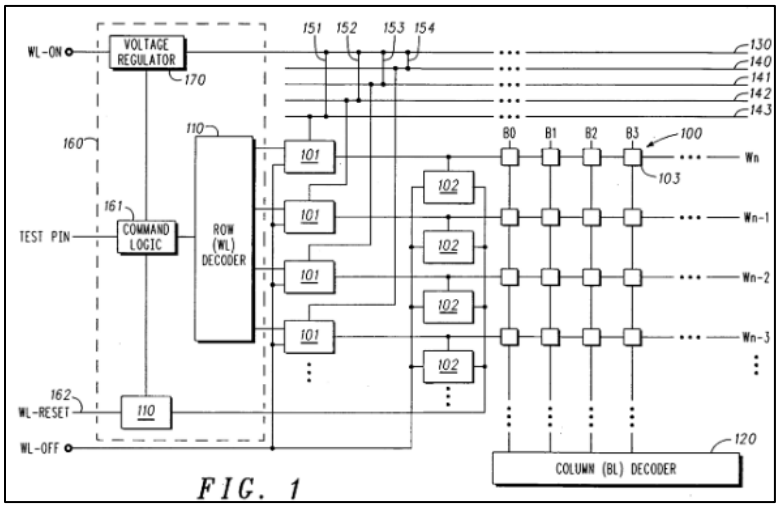


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

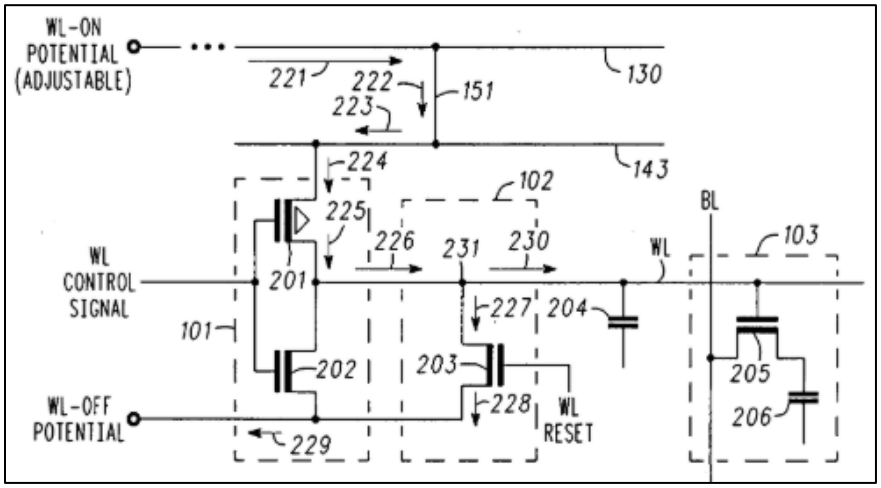


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

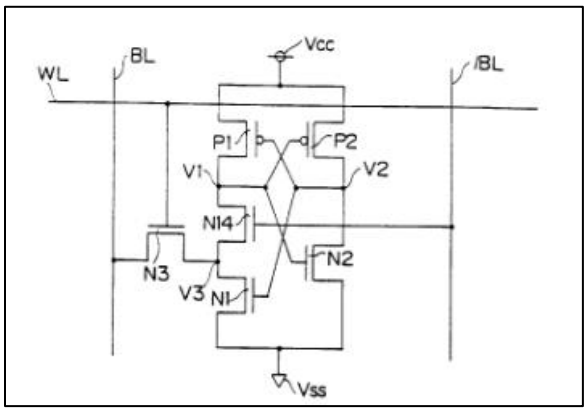
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

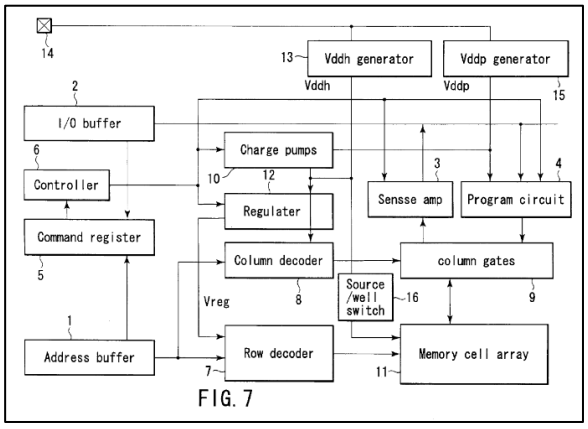


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

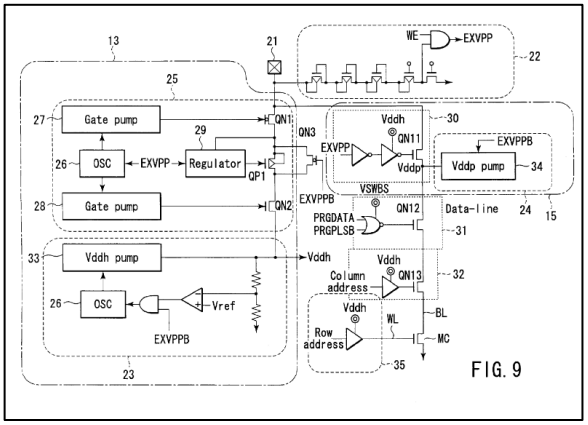


FIG. 9

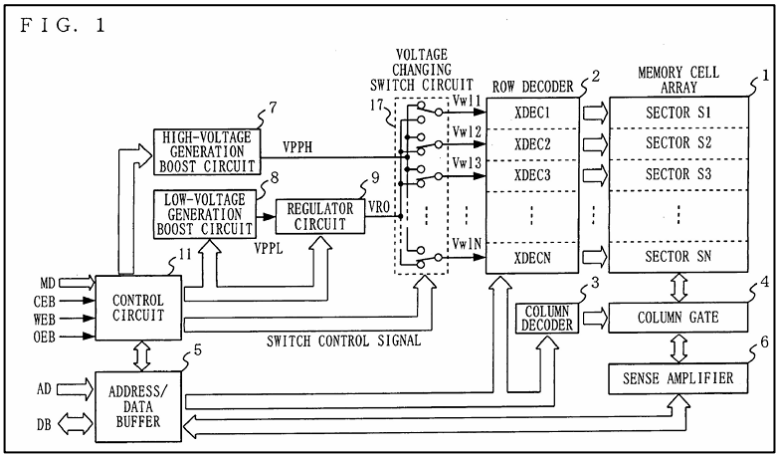
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

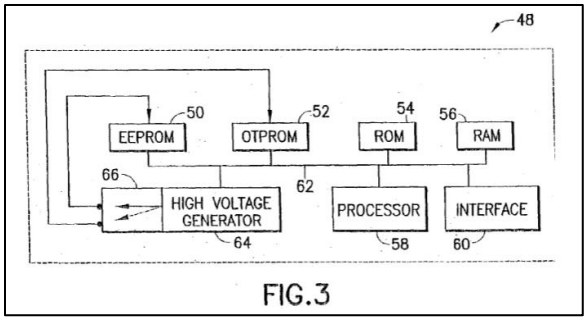


FIG.3

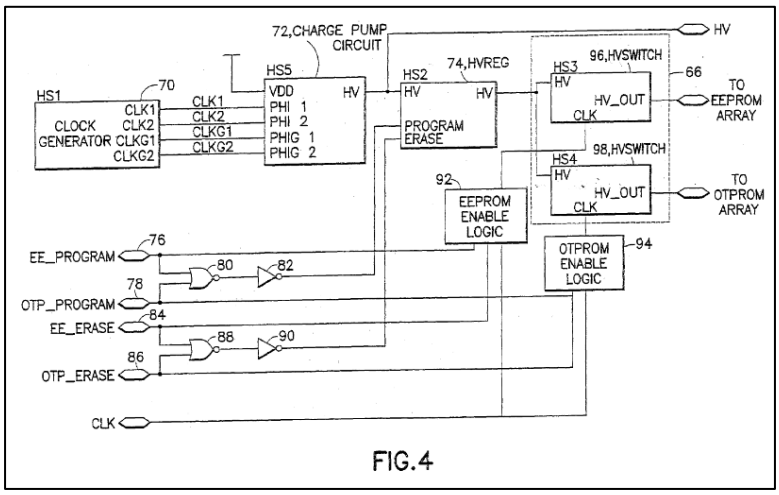


FIG.4

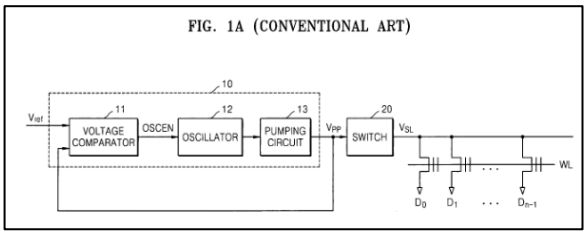
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

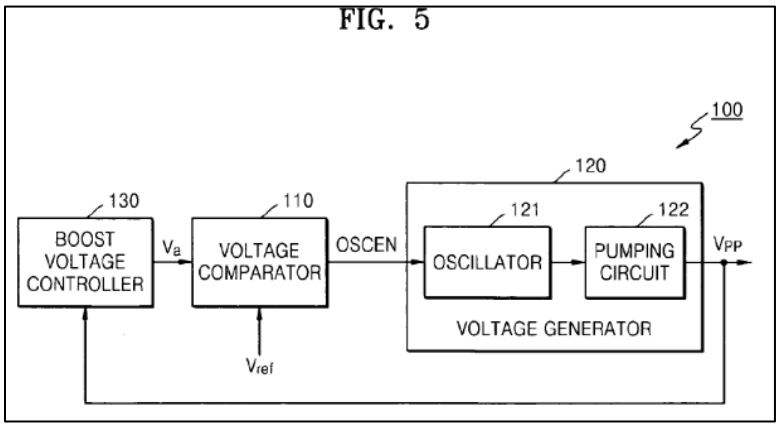
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

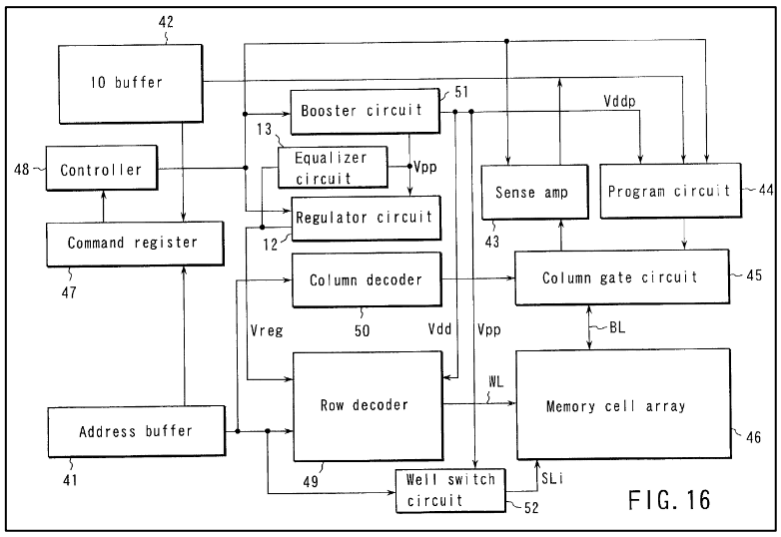


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

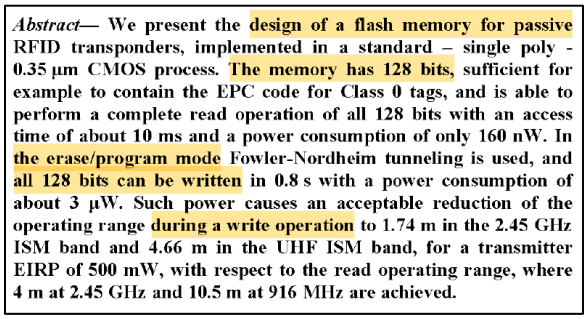
The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:



***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

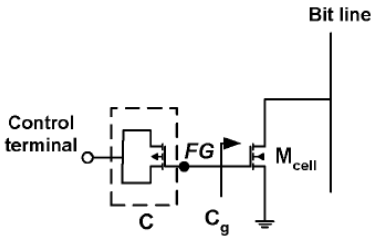


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

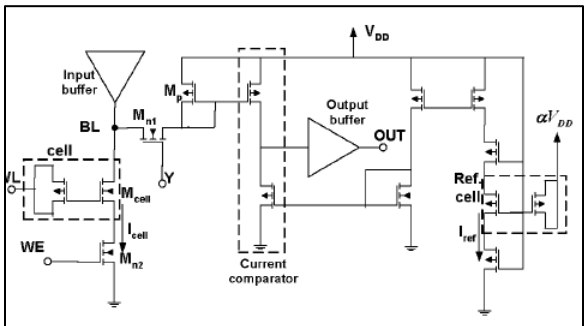


Figure 3. Current mode Sense Amplifier.

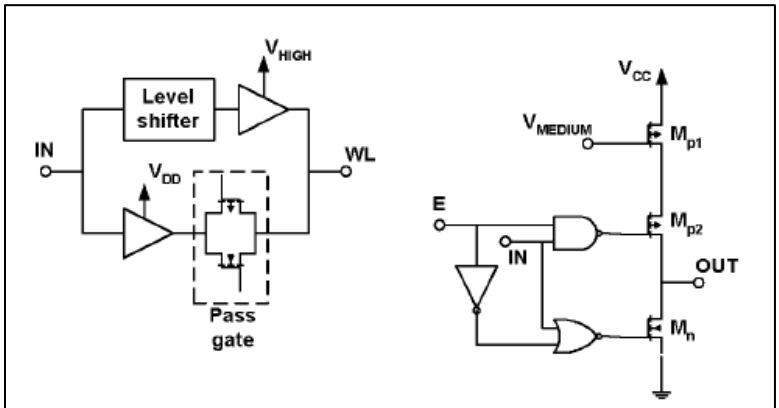


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

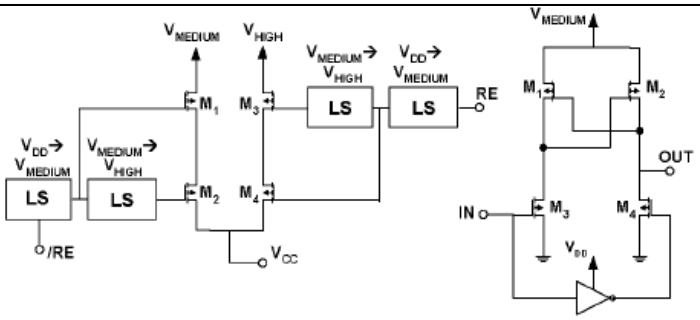


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

5[a] The semiconductor memory device of claim 3, wherein

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the semiconductor memory device of claim 3.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

5[b] in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell and

The Omnibus References disclose and/or render obvious in a first operation mode, the first and fourth switches are turned on, allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell.

See, e.g., claim limitations 1[c], 1[d], and 1[e], *supra.*

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for

generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

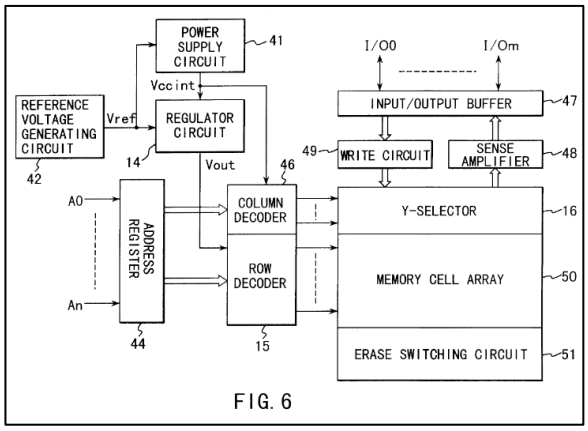


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

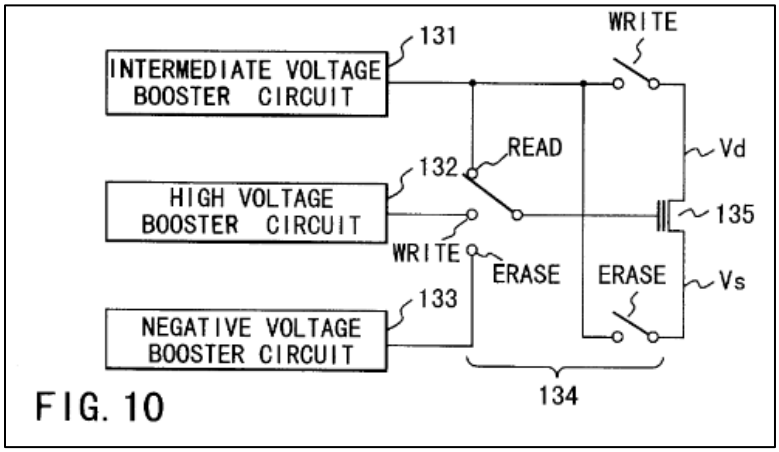


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for

memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

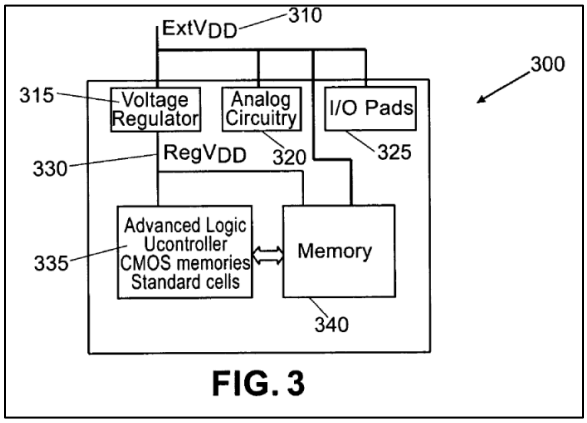


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

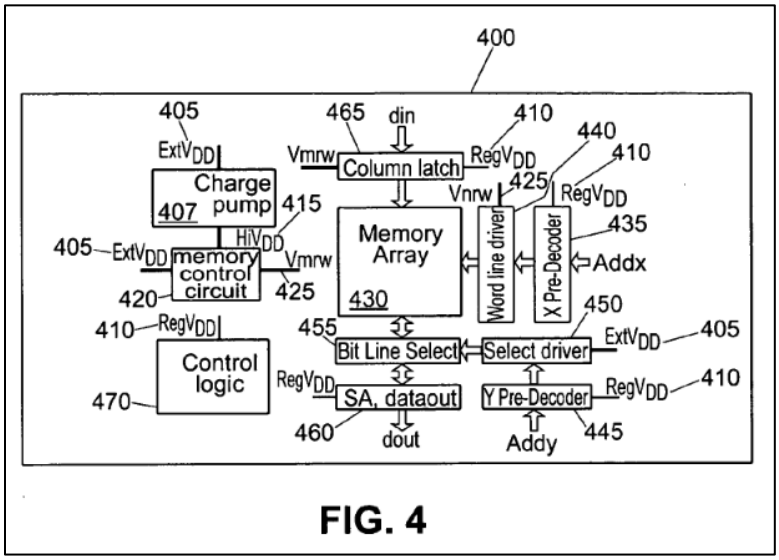


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420

supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

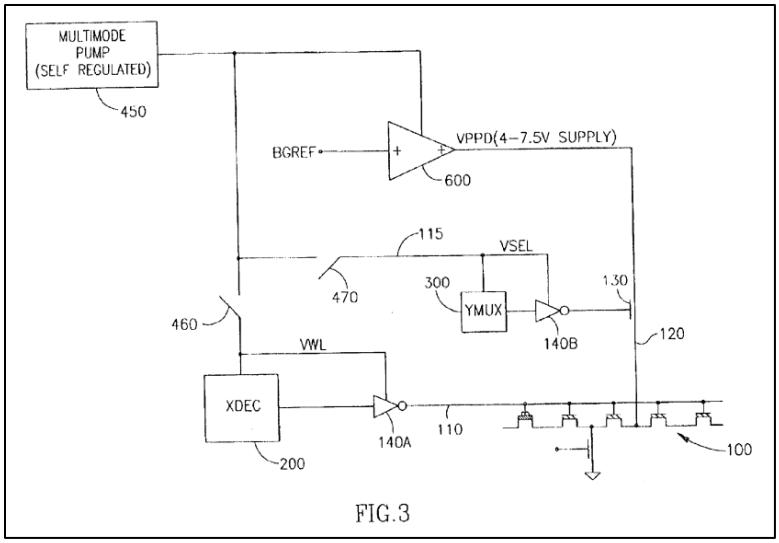


FIG.3

Shor at 2:42-61:

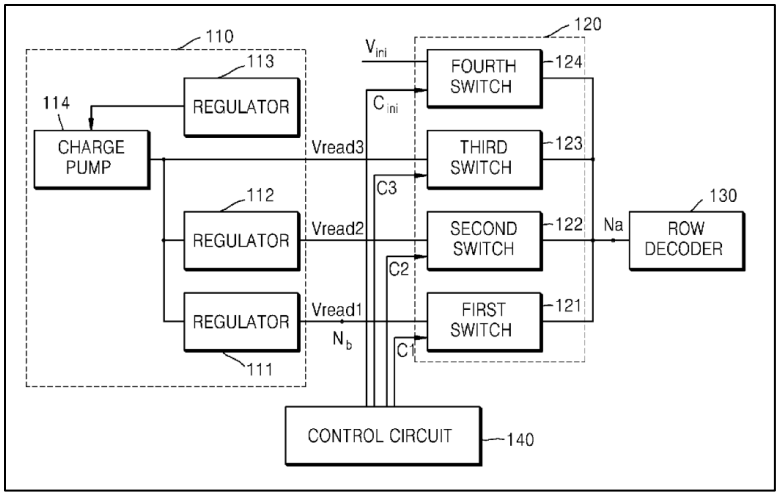
As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled “Efficient Charge Pump with Constant Boosted Output Voltage” by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively

low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

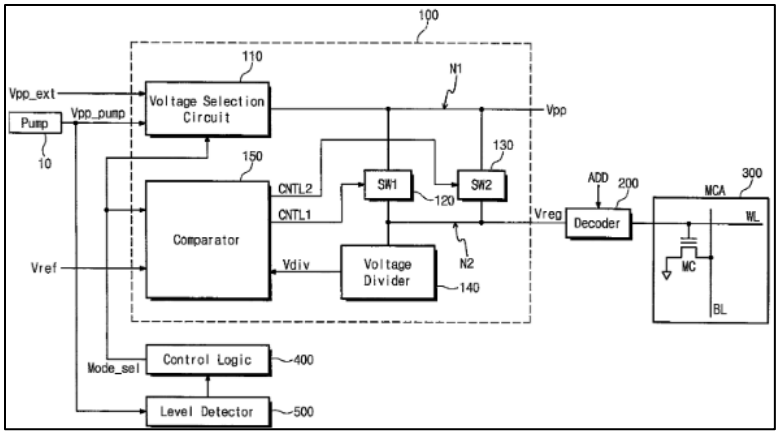
Cho at 2:24-64:

Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit, the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and

a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

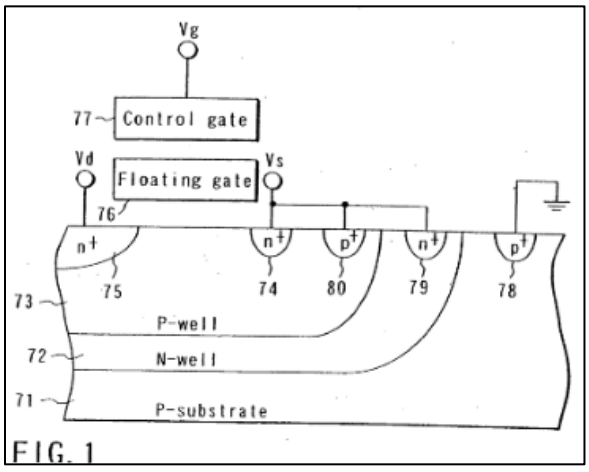


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

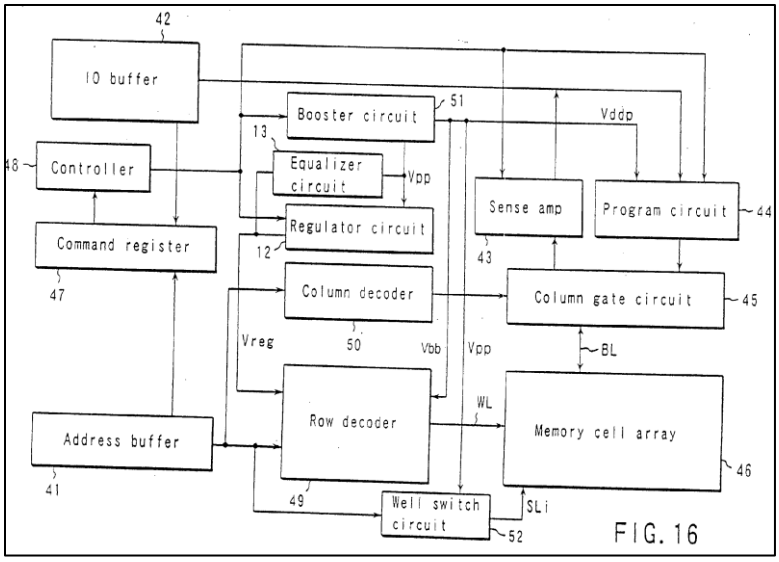


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1,

Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

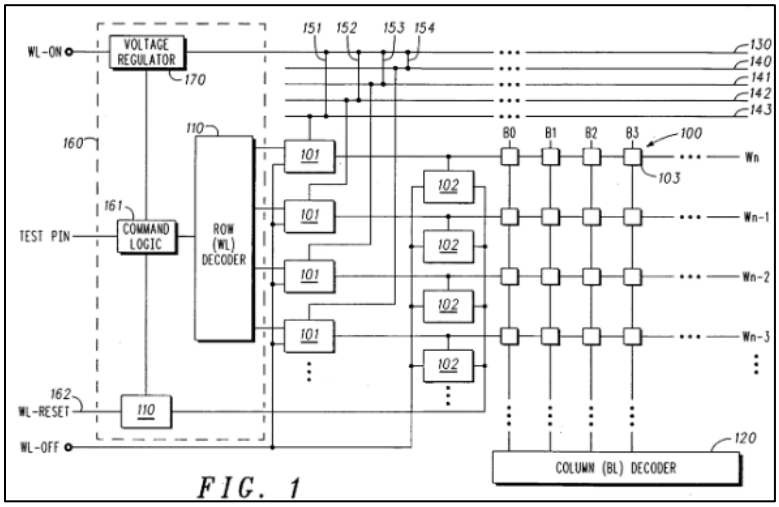


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

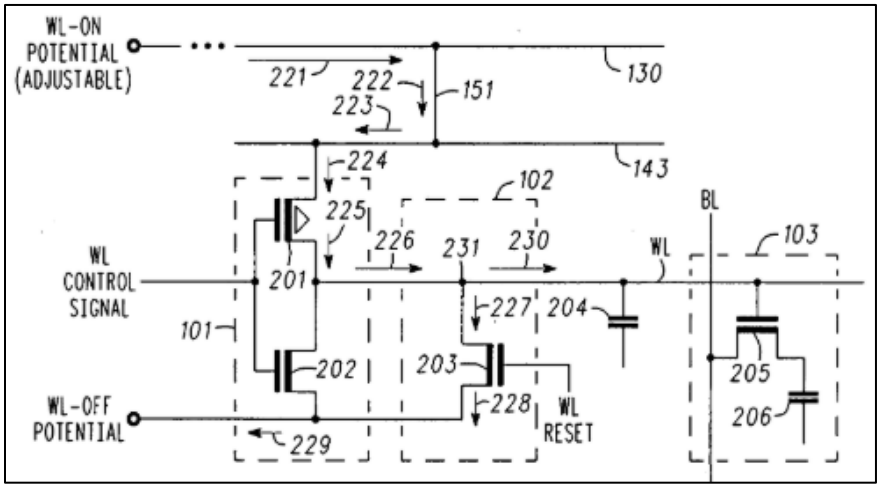


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

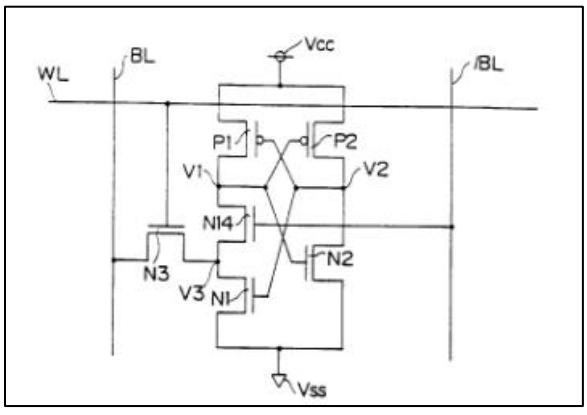
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is

controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the

columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

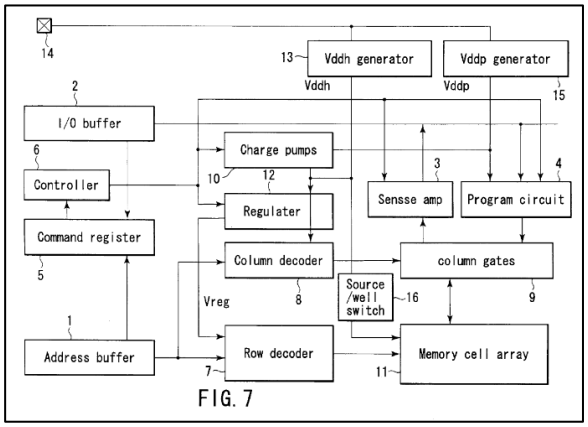


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

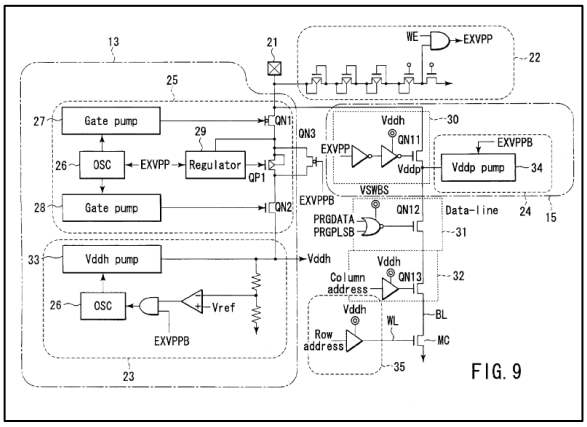
FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.



Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

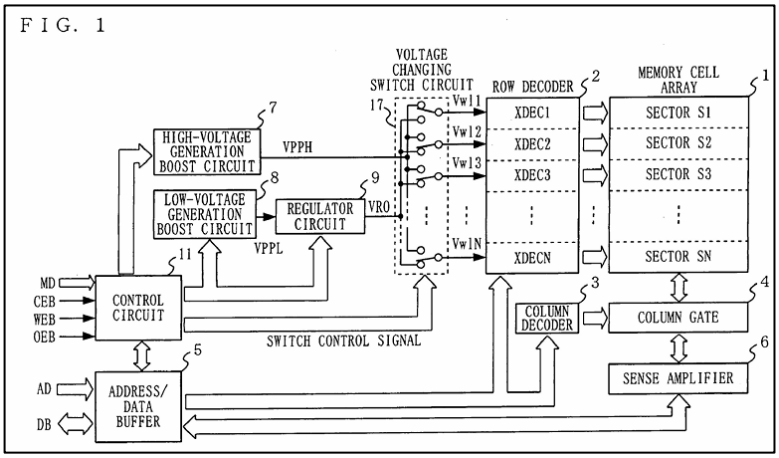
Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17

comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.

FIG. 1



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

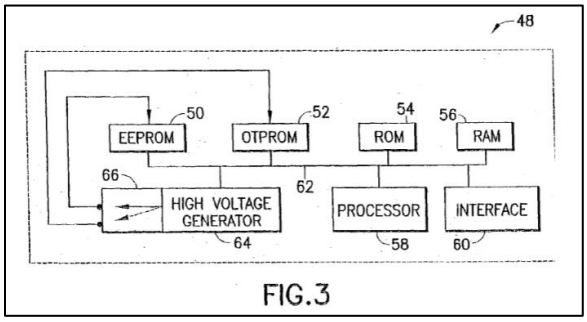


FIG.3

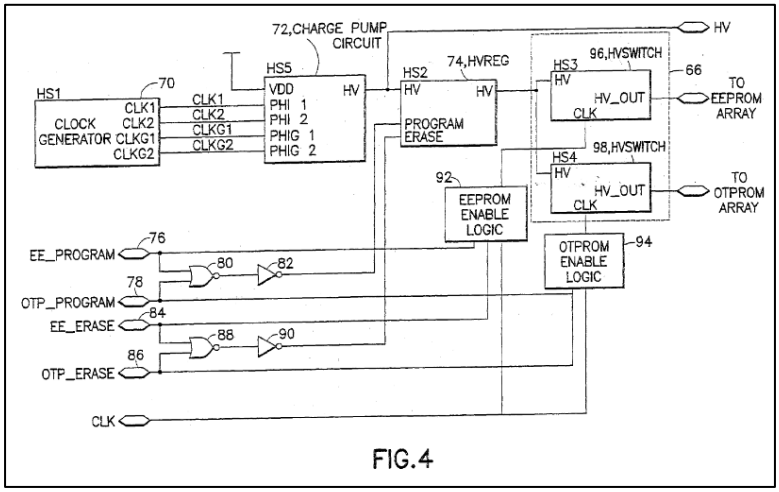


FIG.4

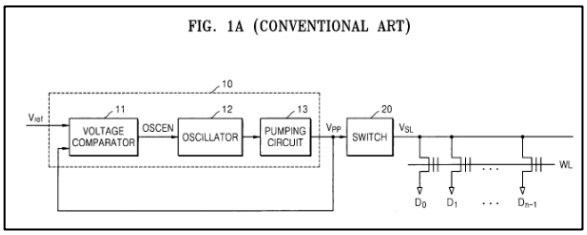
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

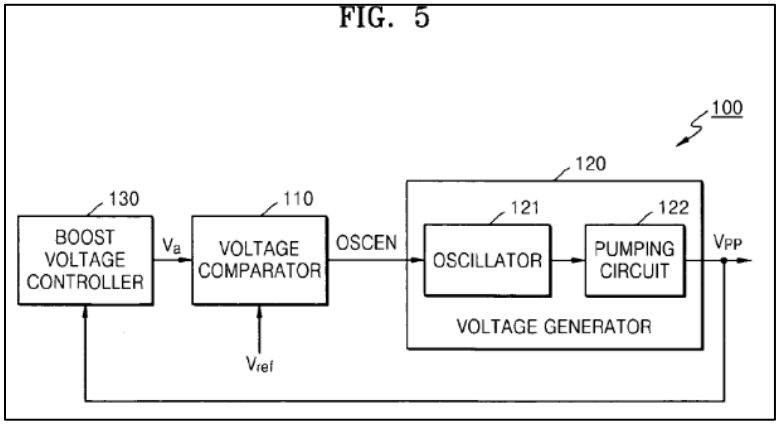
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

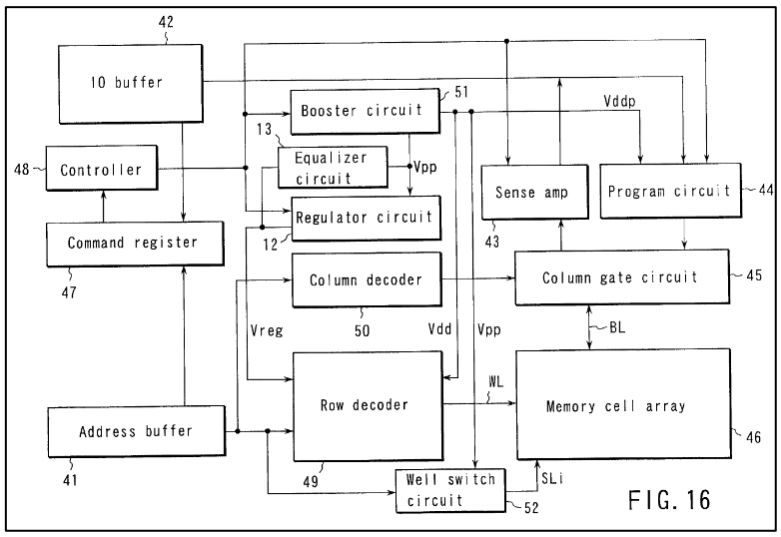


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

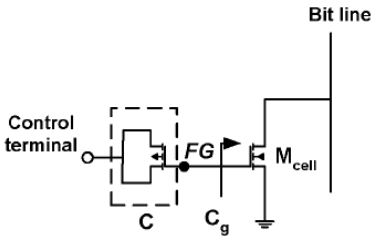


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

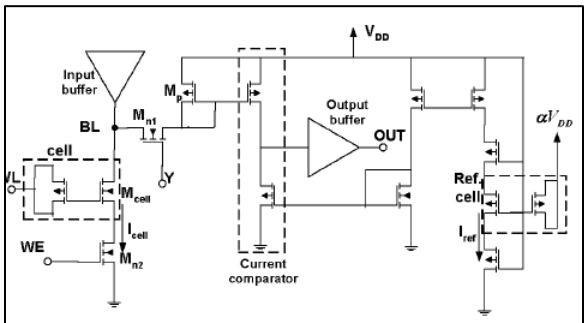


Figure 3. Current mode Sense Amplifier.

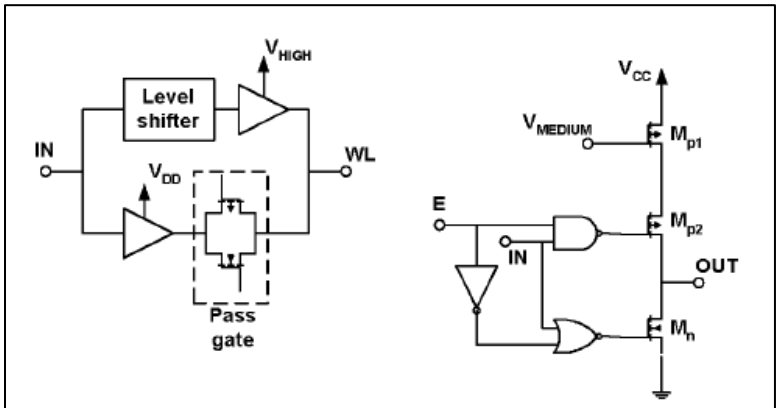


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

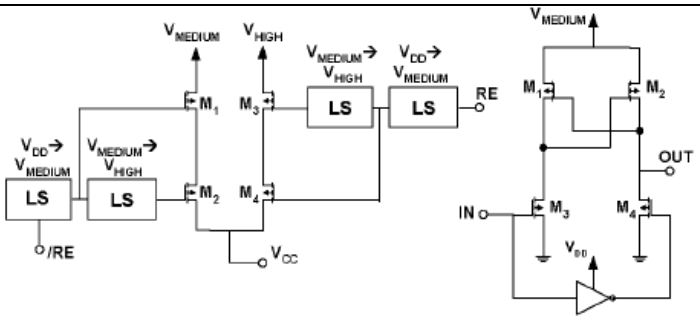


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

5[c] the voltage different from the output of the regulator to be applied to the gate of the memory cell, and

The Omnibus References disclose and/or render obvious the voltage different from the output of the regulator to be applied to the gate of the memory cell.

See, e.g., claim limitations 1[c], 1[d], and 1[e], *supra.*

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for

regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

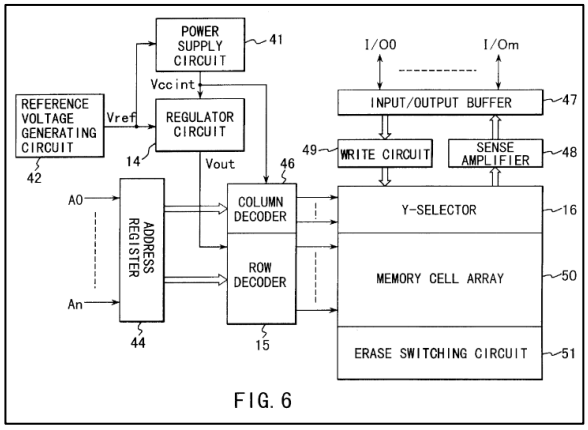


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

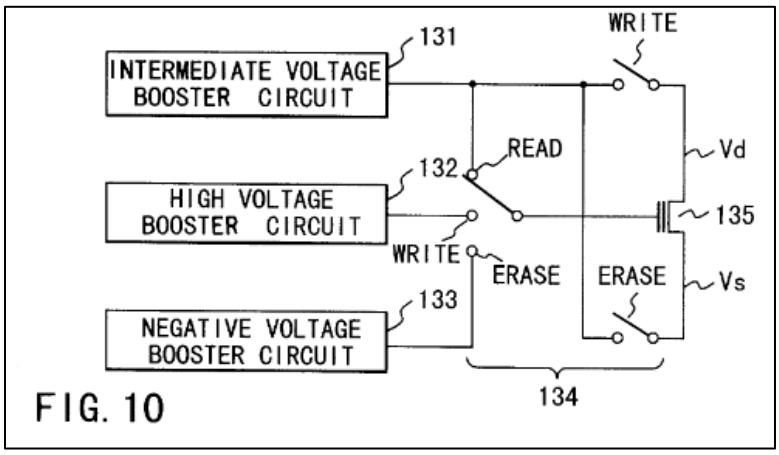


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

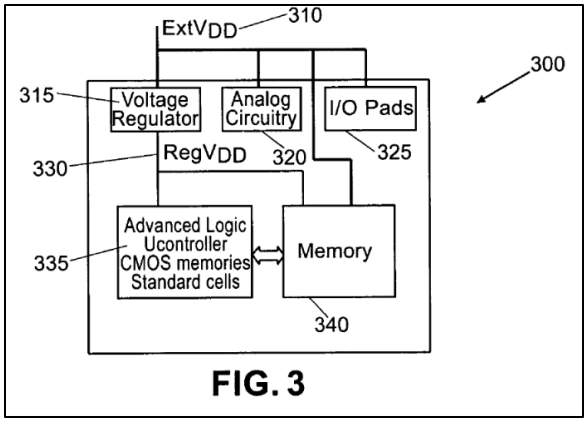


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

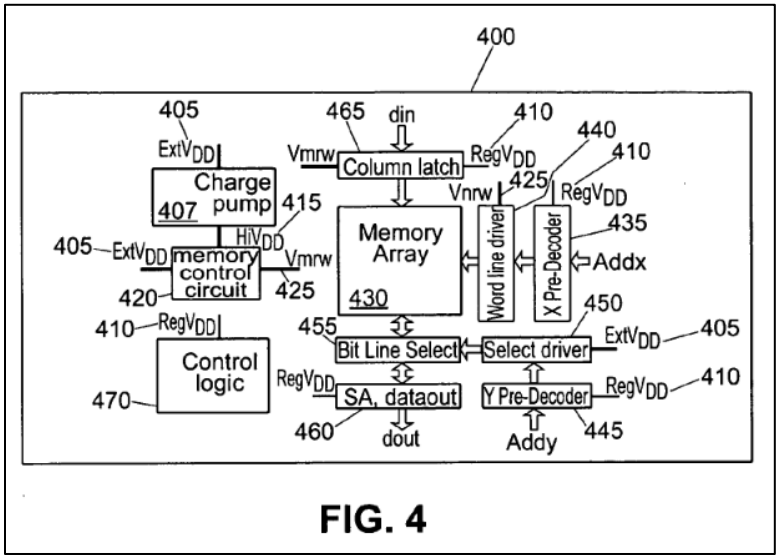


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

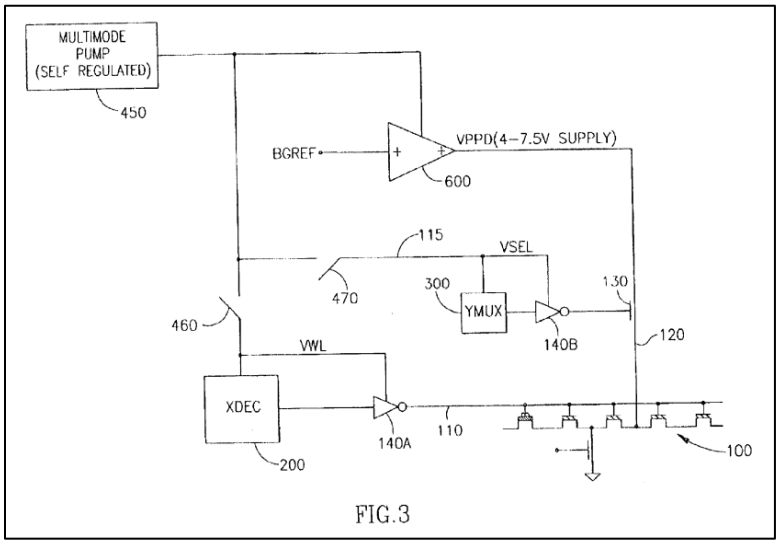


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

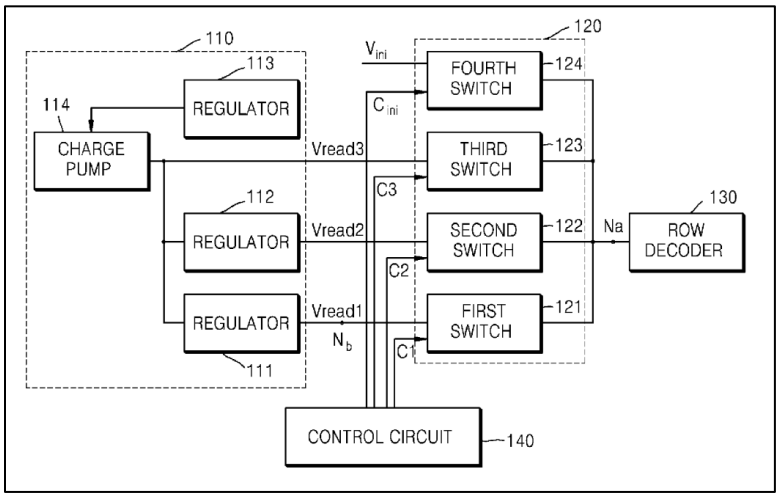
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

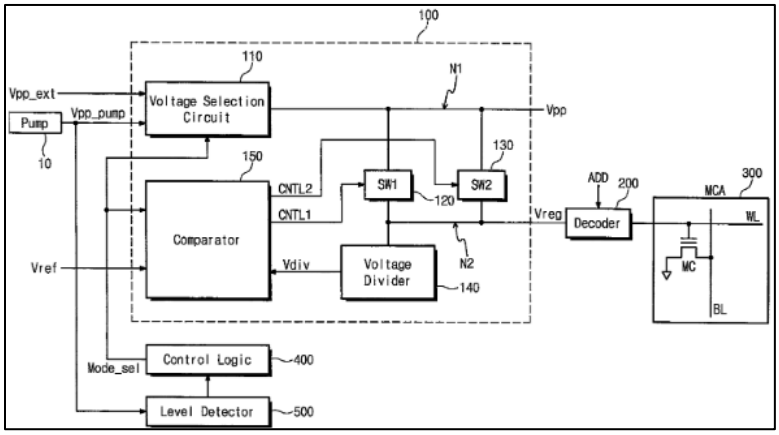
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

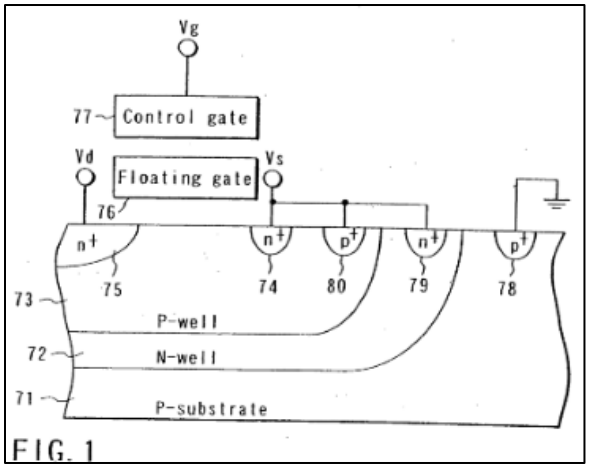


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

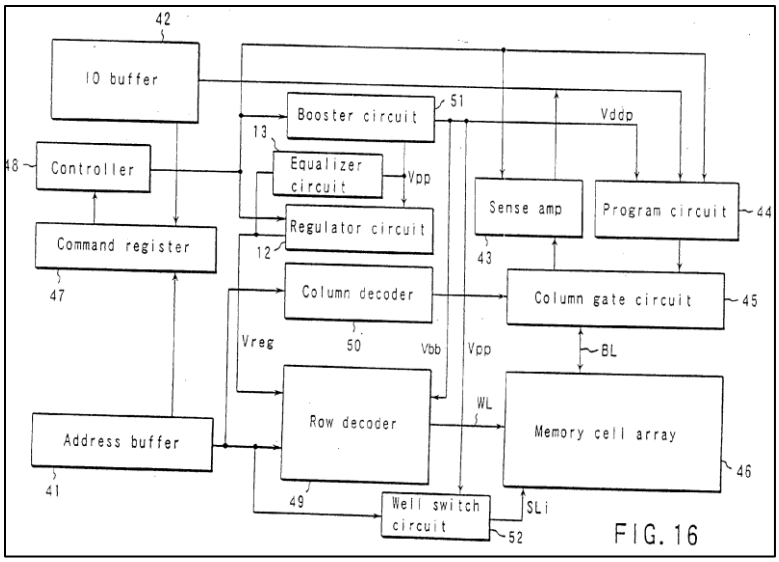


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

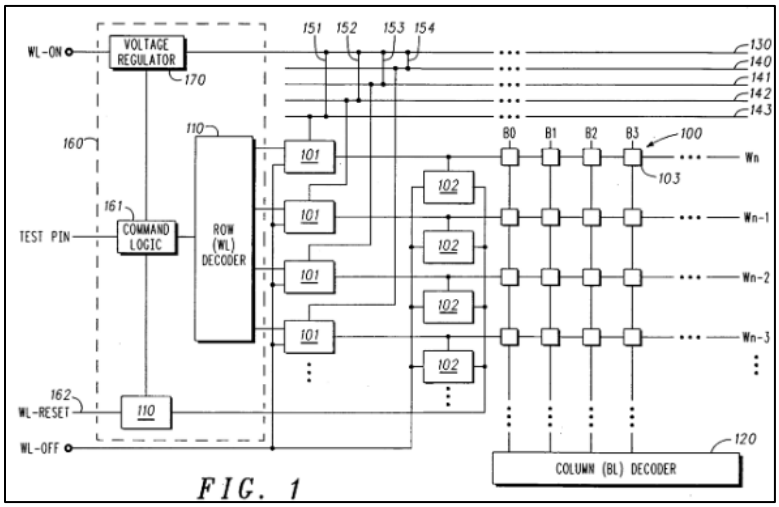


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

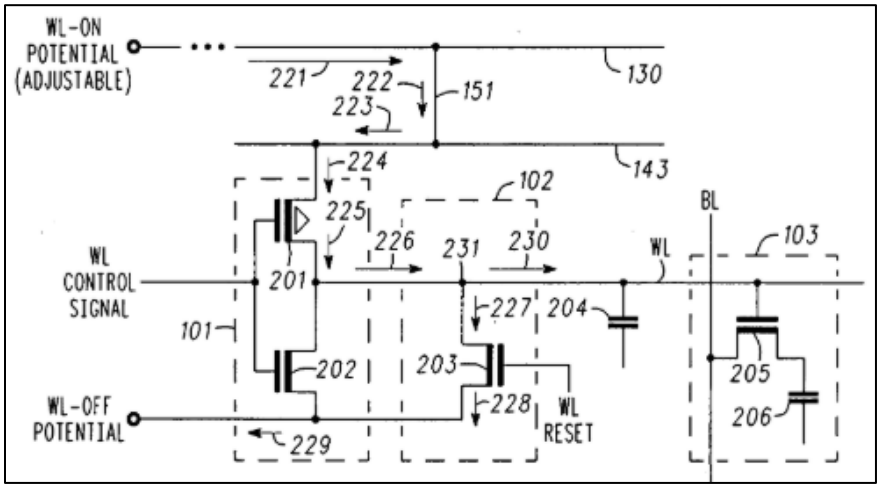


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

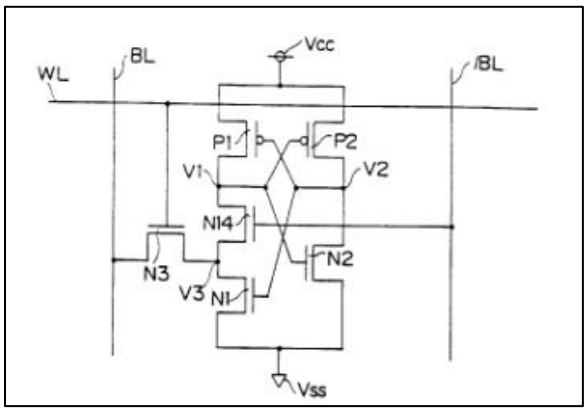
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

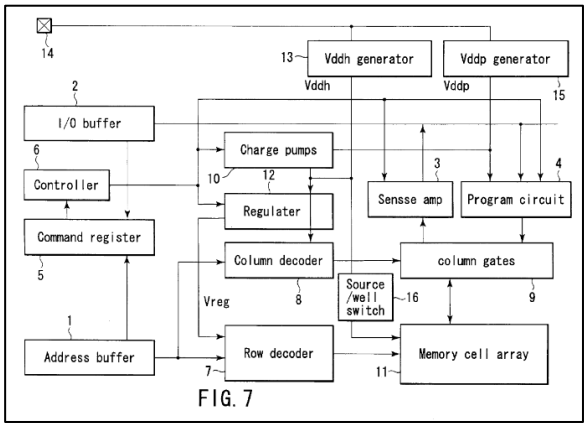


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

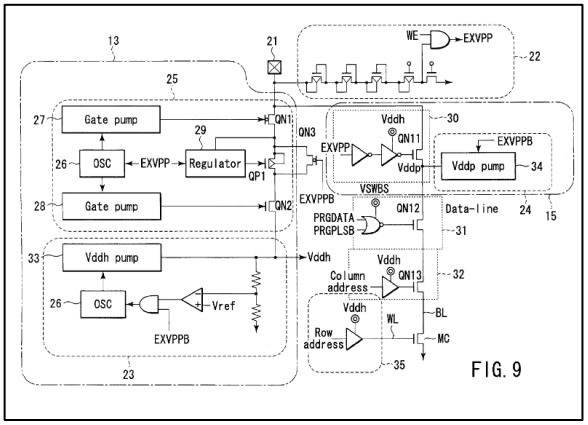


FIG. 9

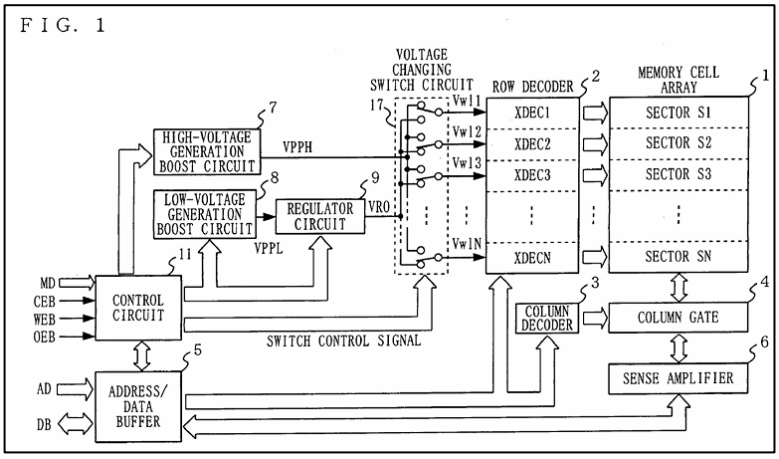
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

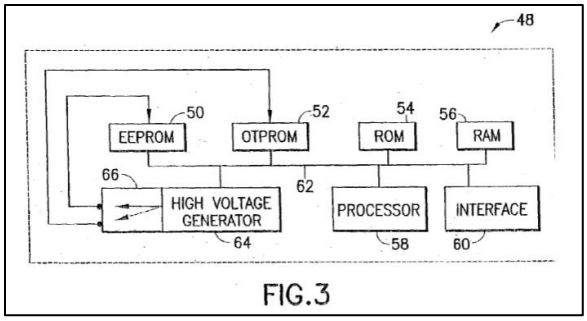


FIG.3

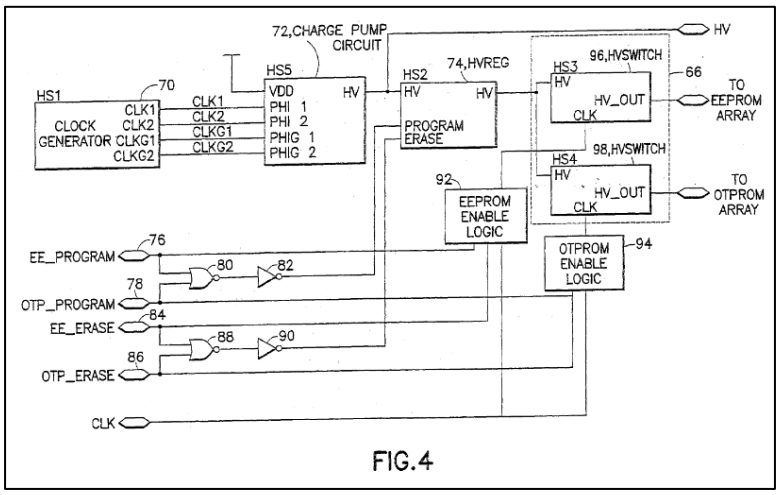


FIG.4

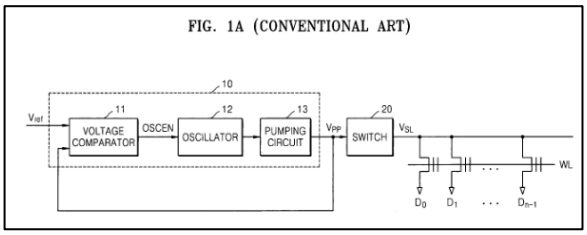
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

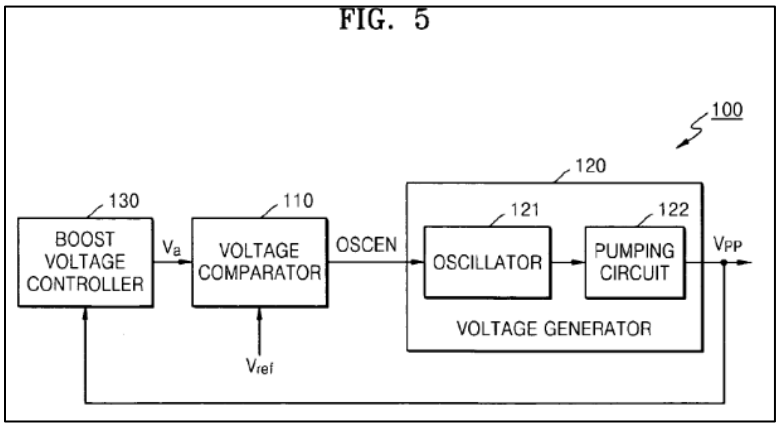
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

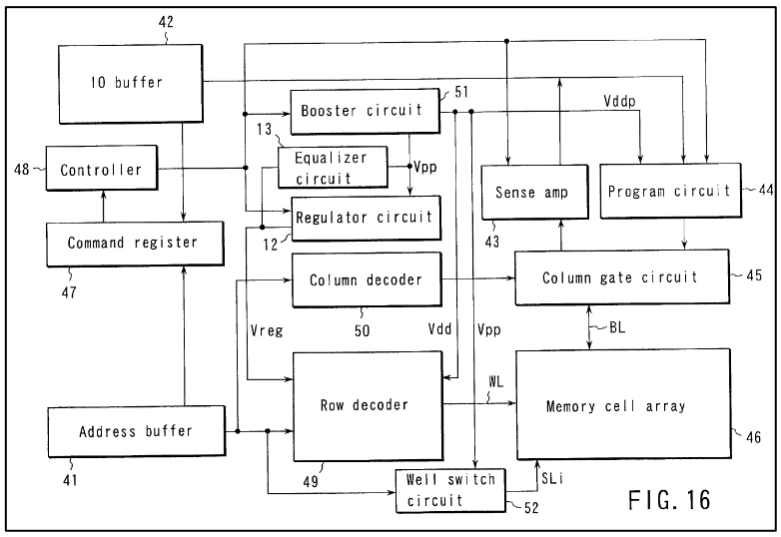


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

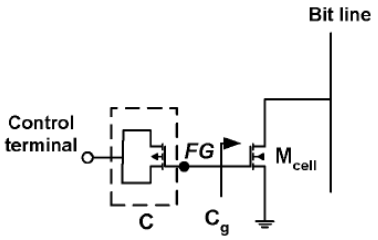


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

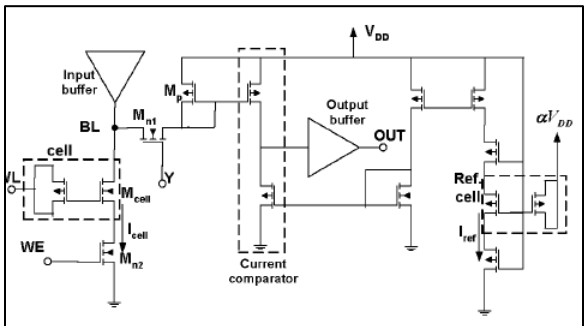


Figure 3. Current mode Sense Amplifier.

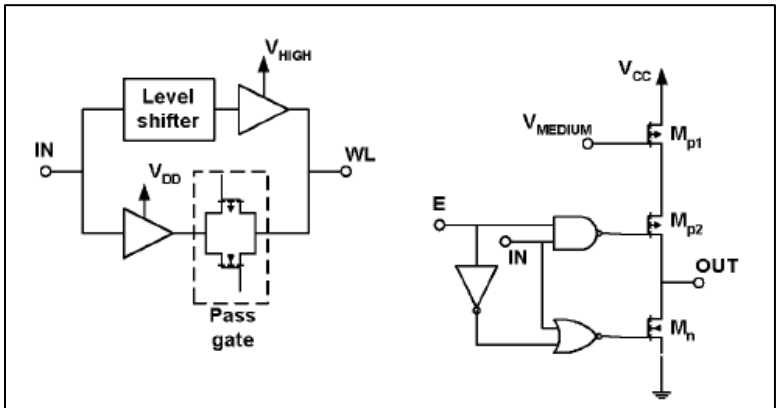


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

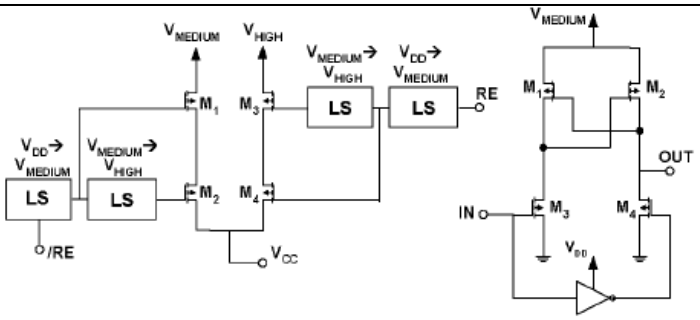


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

5[d] in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

The Omnibus References disclose and/or render obvious in a second operation mode, the second switch is turned on, allowing the output voltage of the regulator to be applied to the gate of the memory cell.

See, e.g., claim limitations 1[c], 1[d], and 1[e], *supra.*

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher

than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

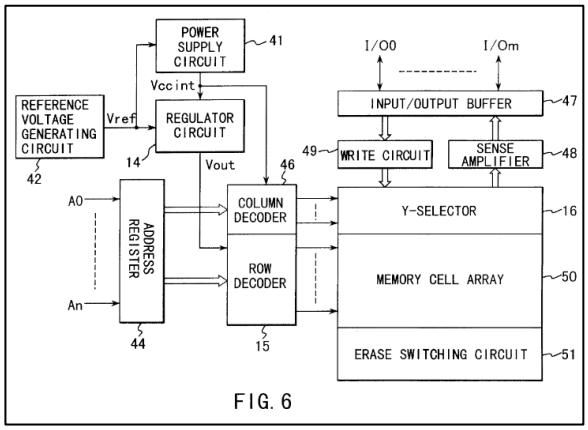


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

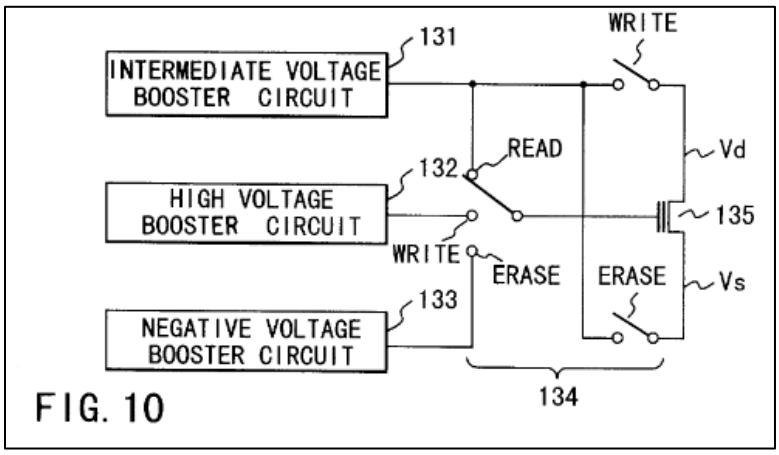


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

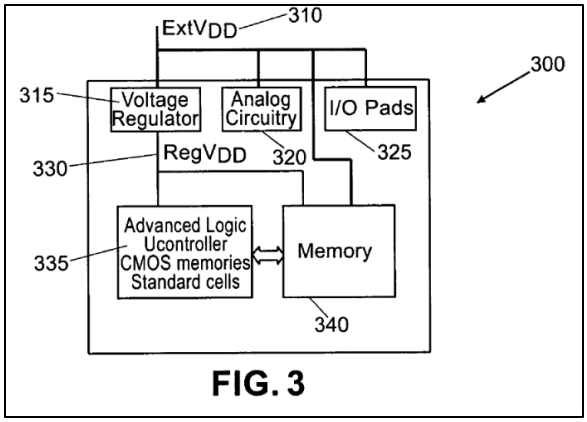


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

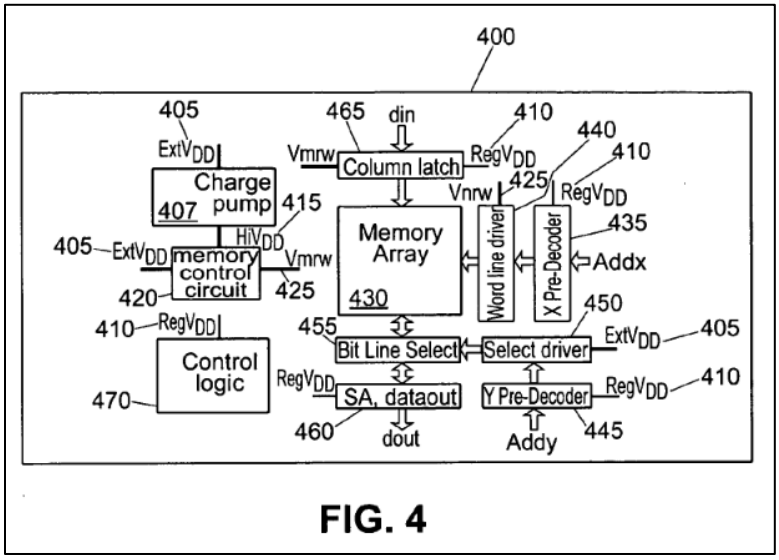


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420 supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies

the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

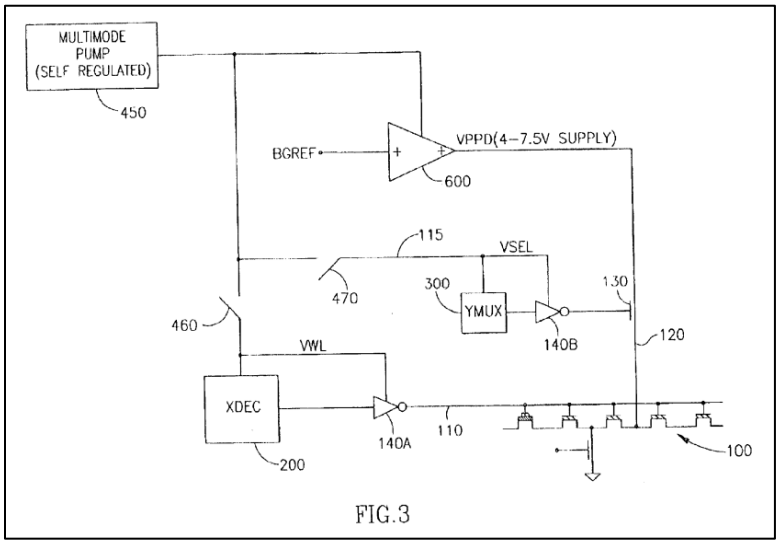


FIG.3

Shor at 2:42-61:

As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping

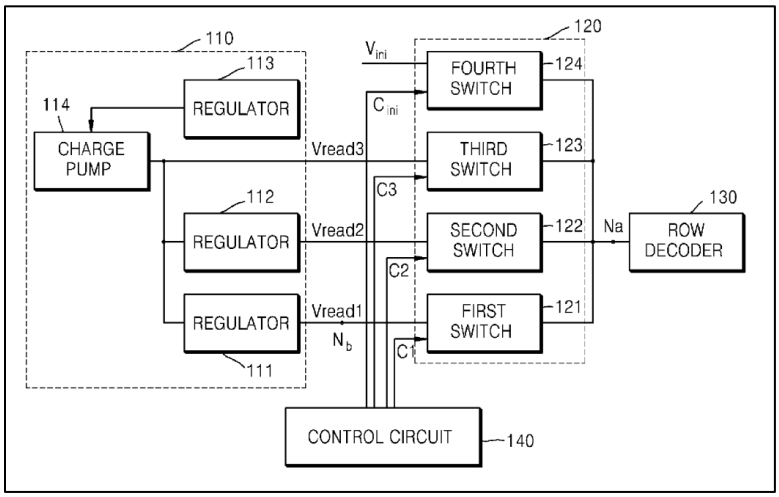
efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled "Efficient Charge Pump with Constant Boosted Output Voltage" by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a

second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Cho at 2:24-64:

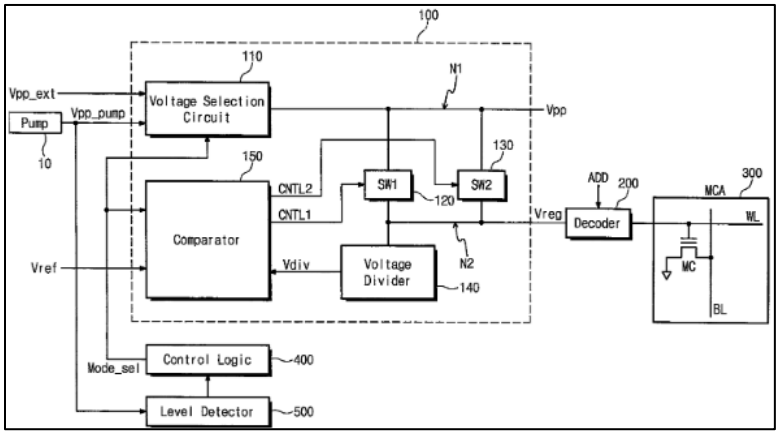
Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit,

the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address

ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

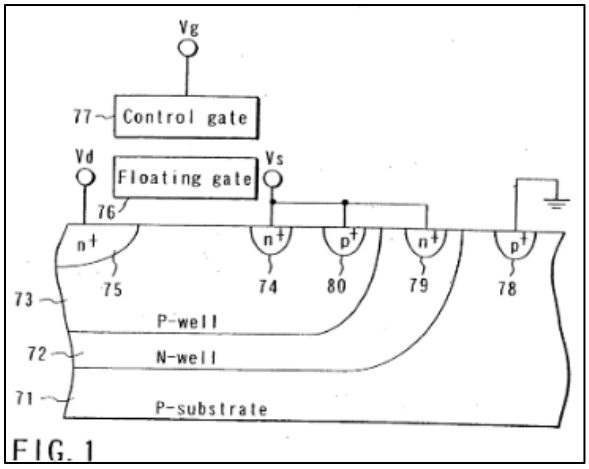


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

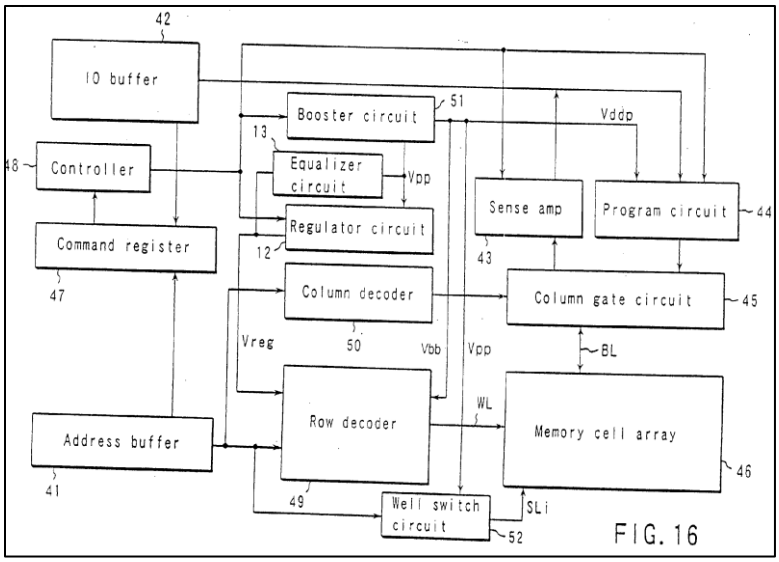


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be

supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

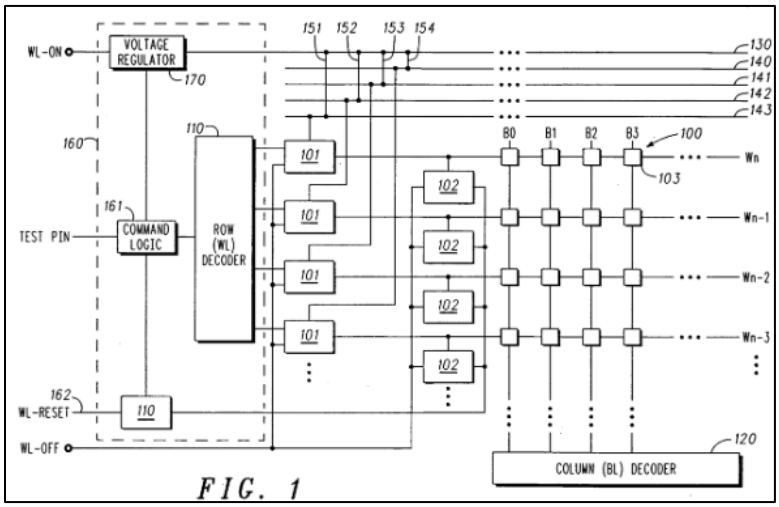


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching

device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

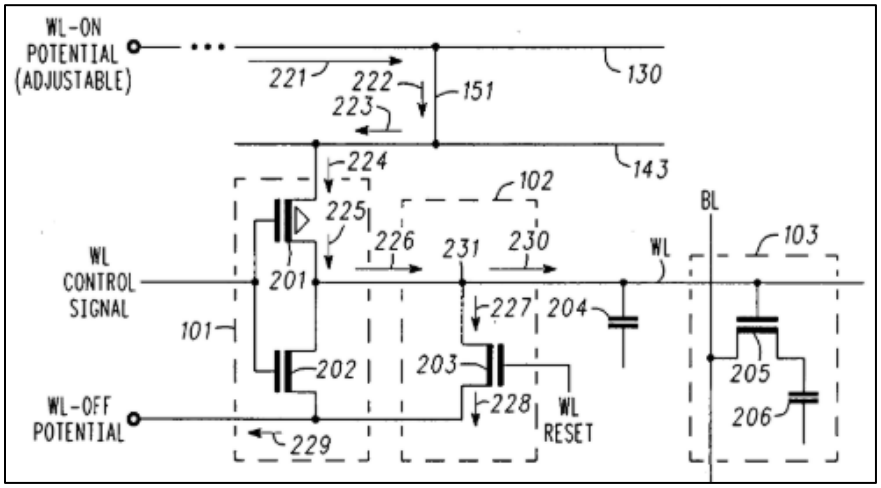


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

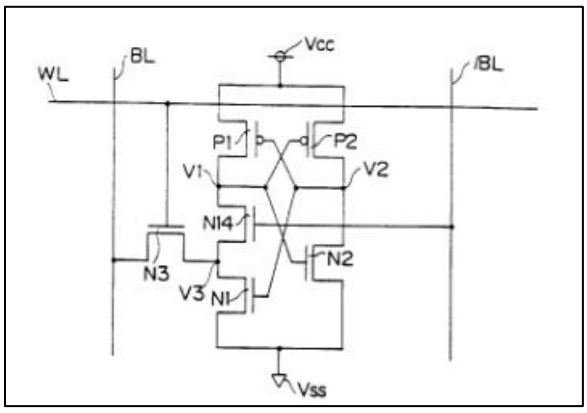
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact

point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

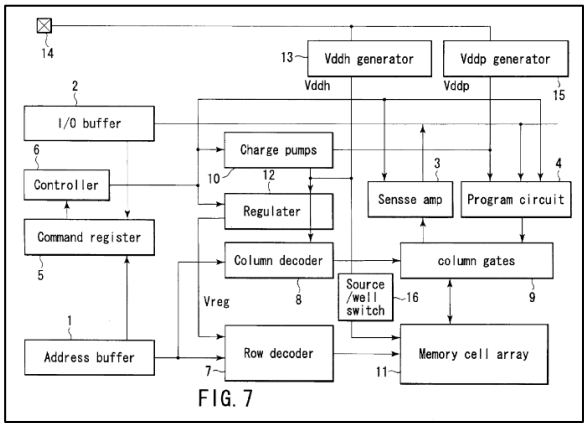


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

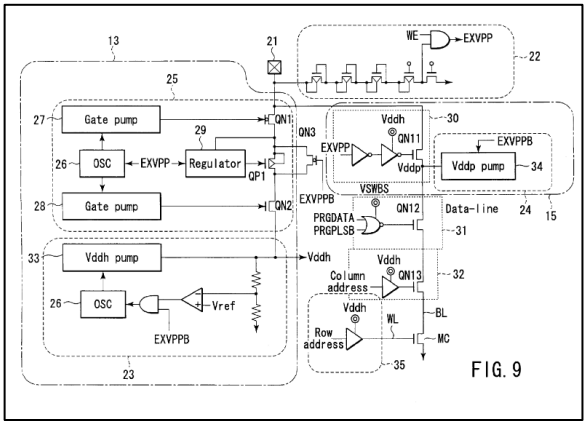


FIG. 9

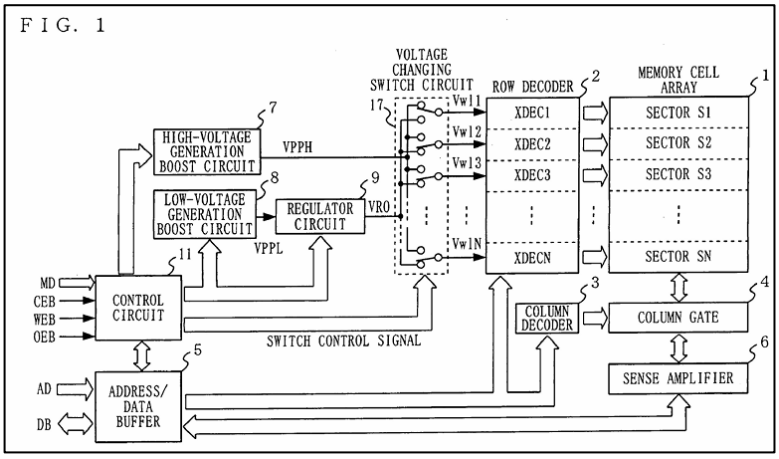
Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17 comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also

communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

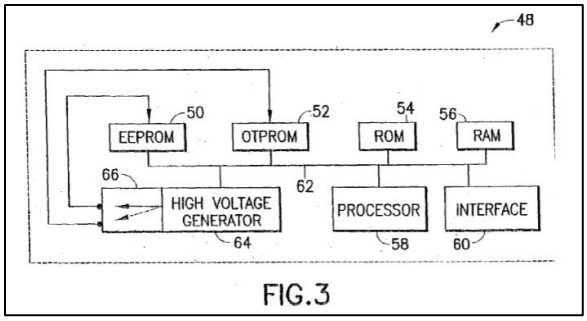


FIG.3

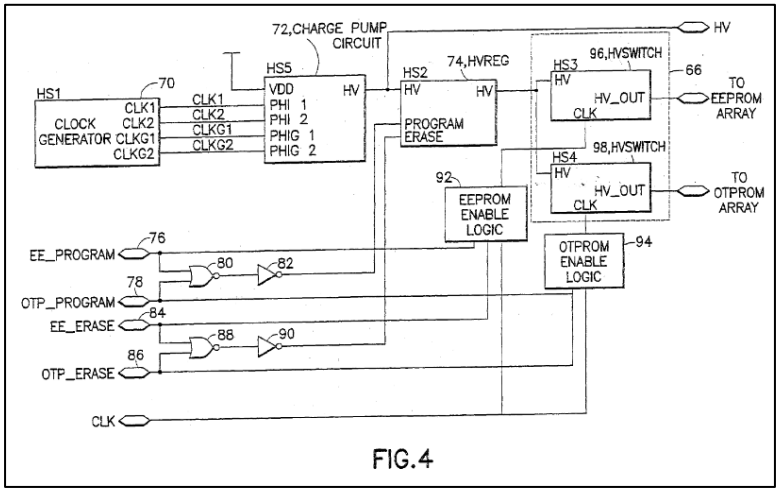


FIG.4

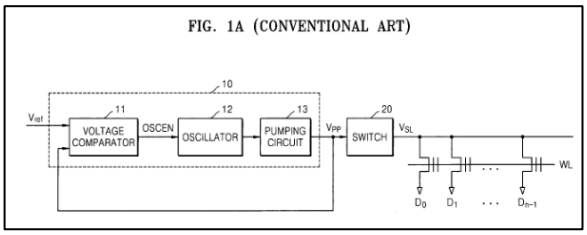
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

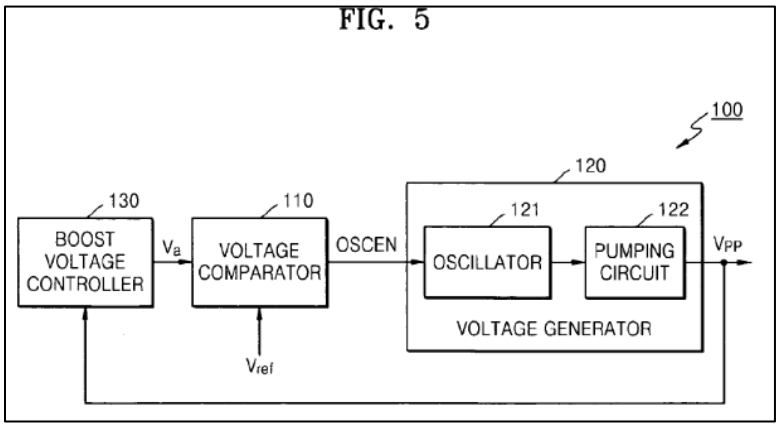
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

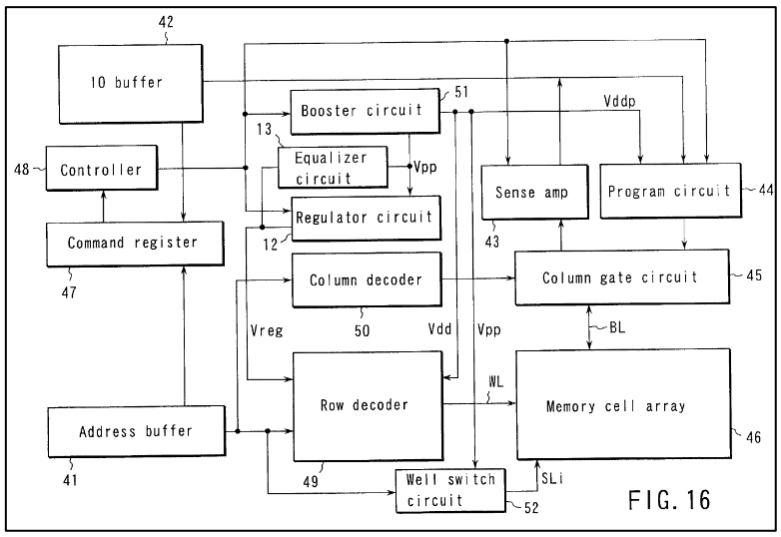
The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.



Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

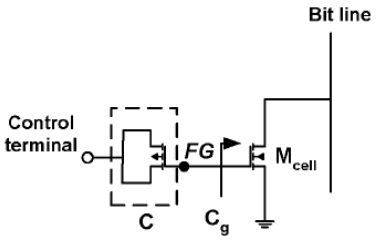


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

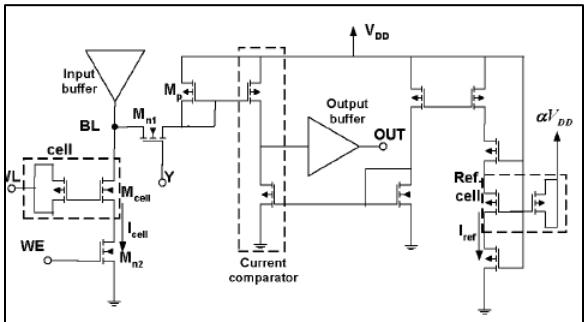


Figure 3. Current mode Sense Amplifier.

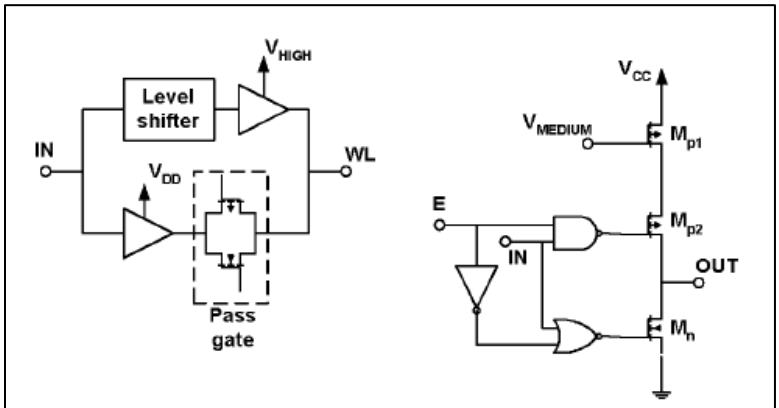


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

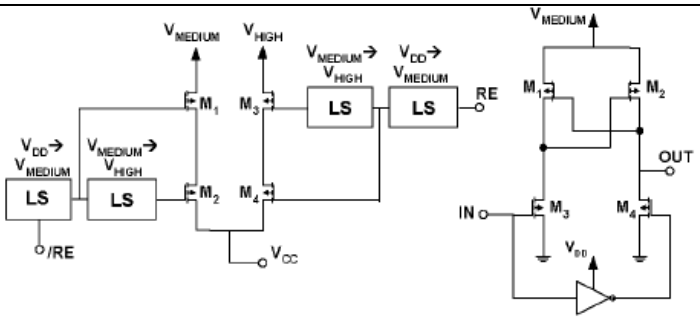


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

20[a] The semiconductor memory device of claim 3, wherein

To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious the semiconductor memory device of claim 3.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

20[b] the voltage different from the output of the regulator is an output voltage of a booster circuit.

The Omnibus References disclose and/or render obvious the voltage different from the output of the regulator is an output voltage of a booster circuit.

See, e.g., claim limitation 1[b], *supra*.

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied

to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

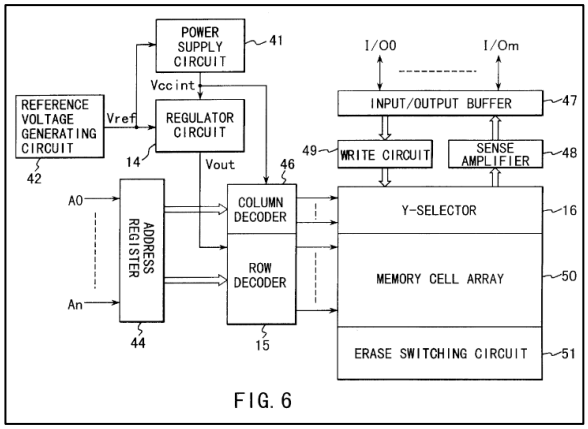


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

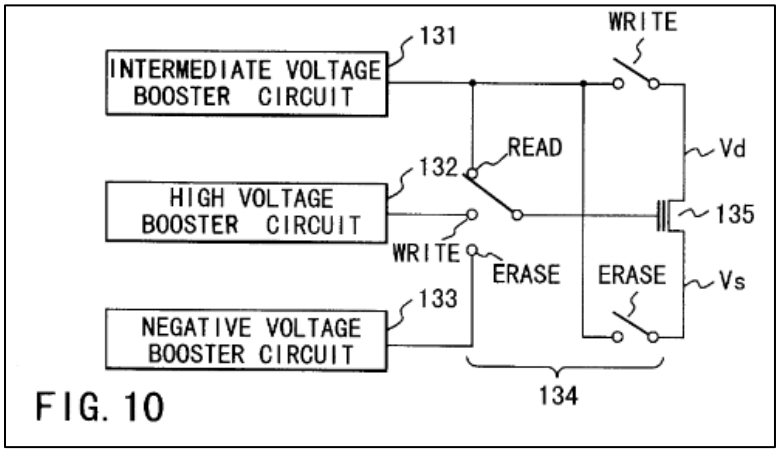


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for

memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

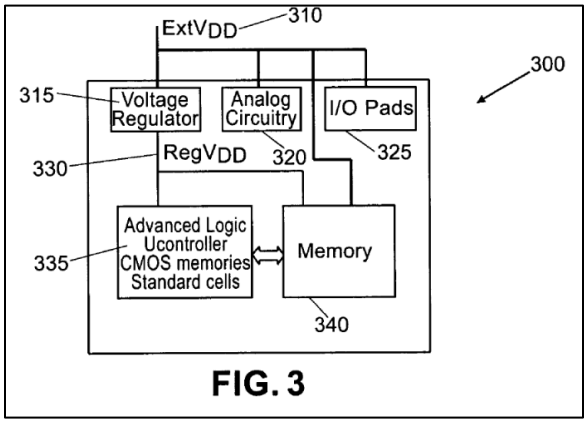


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

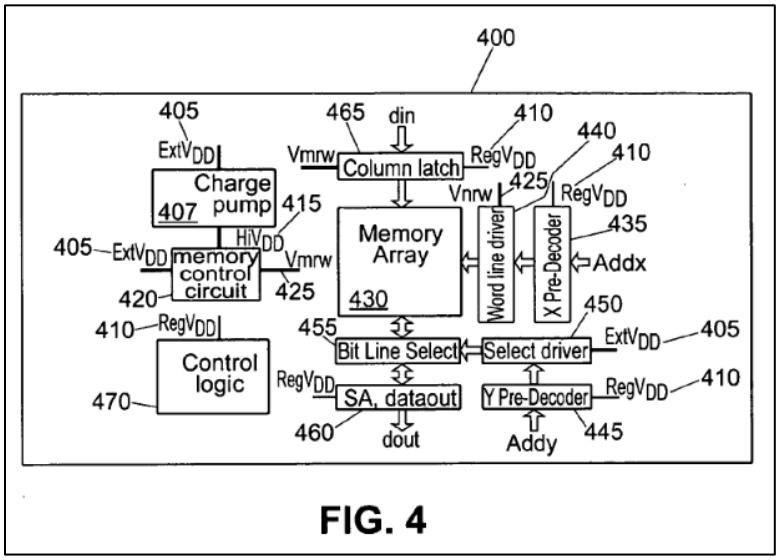


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420

supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

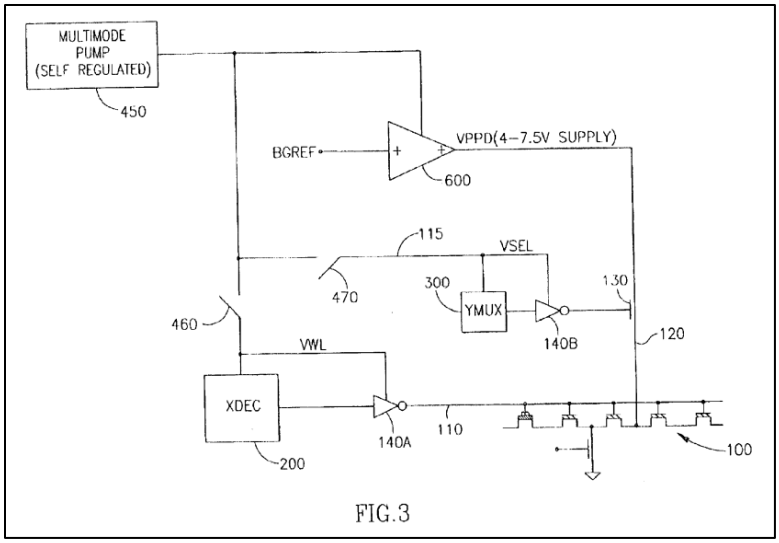


FIG.3

Shor at 2:42-61:

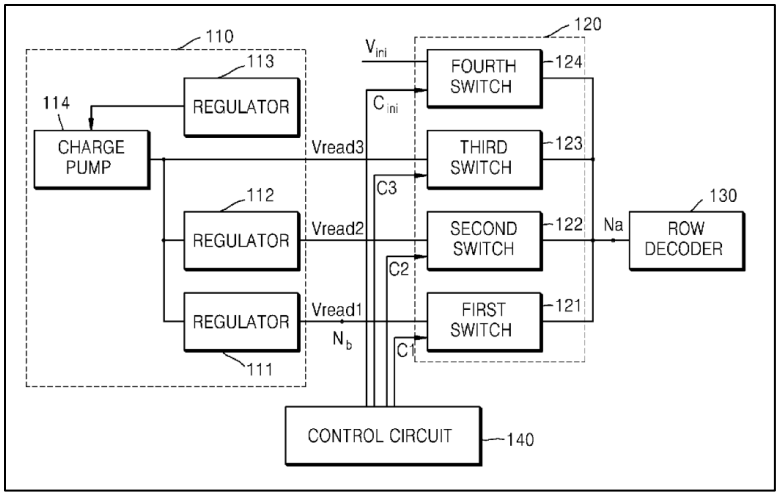
As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled “Efficient Charge Pump with Constant Boosted Output Voltage” by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively

low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

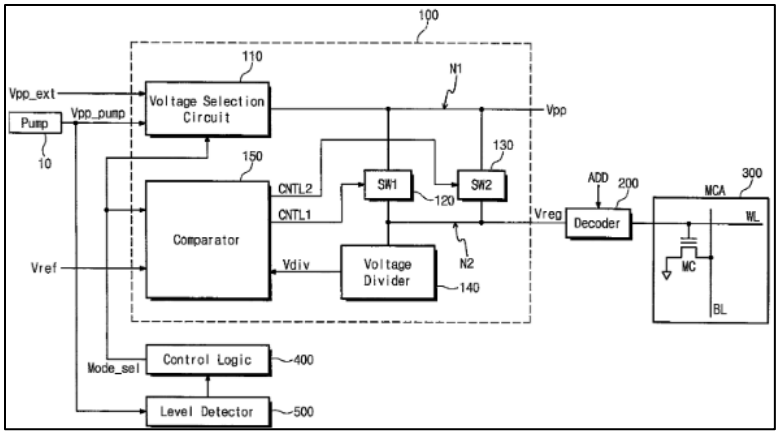
Cho at 2:24-64:

Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit, the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and

a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

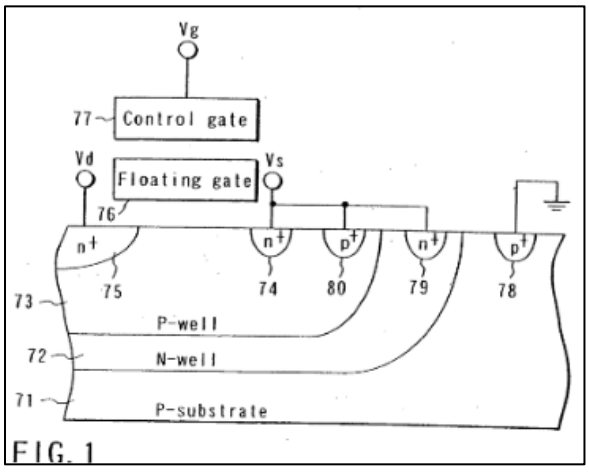


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

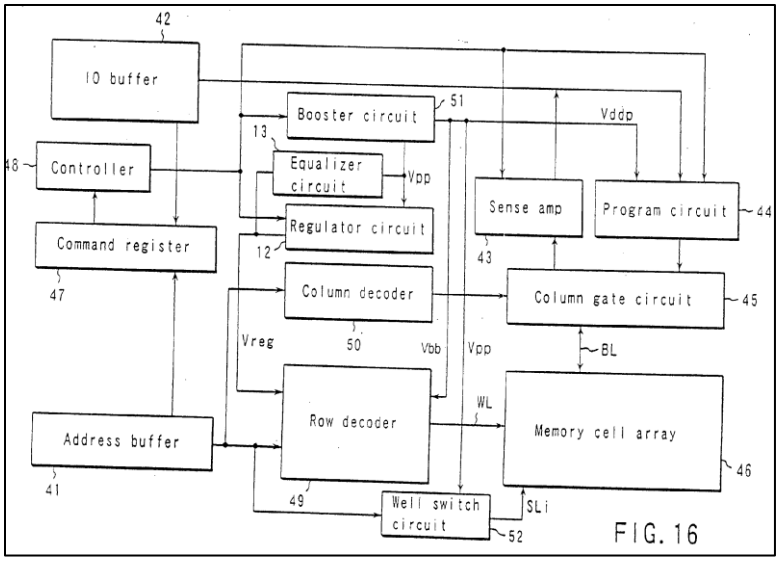


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1,

Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

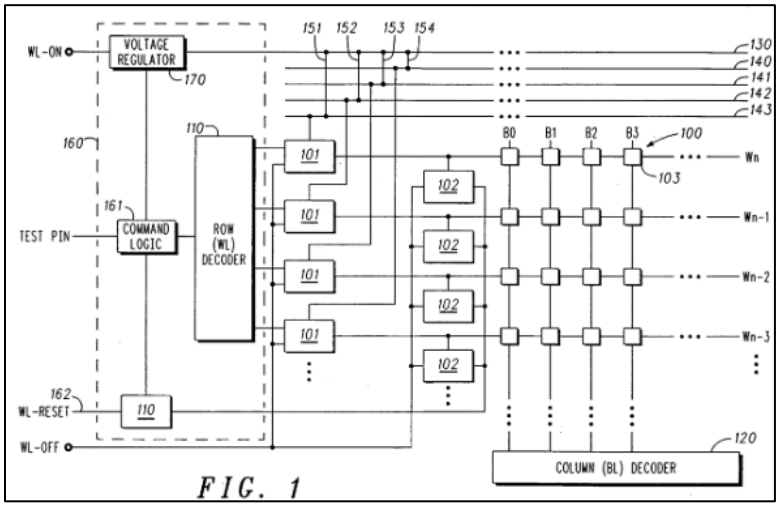


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

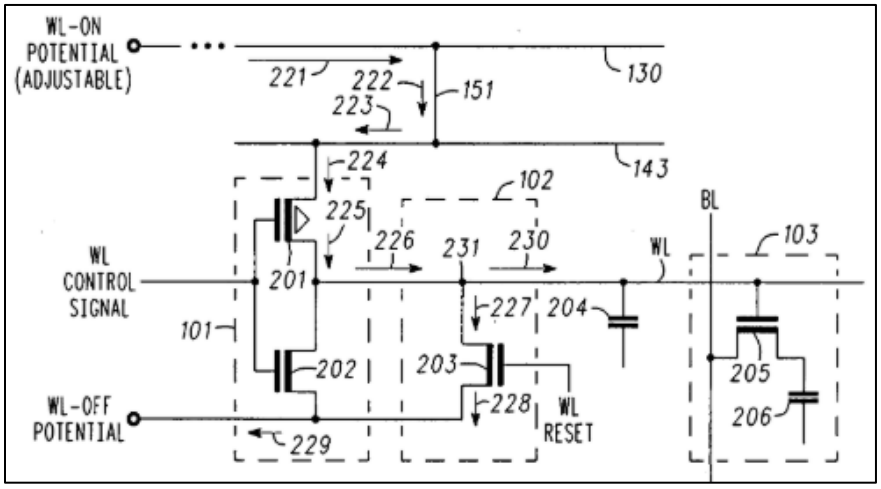


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

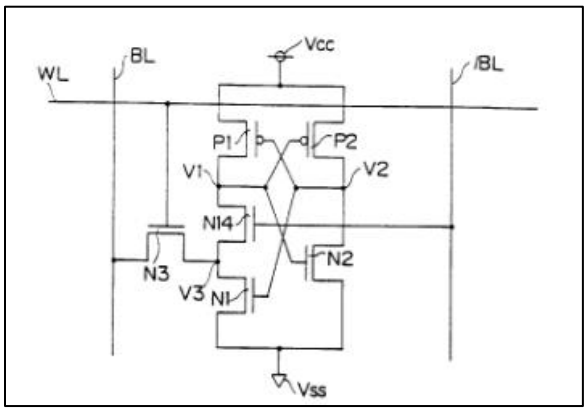
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is

controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the

columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

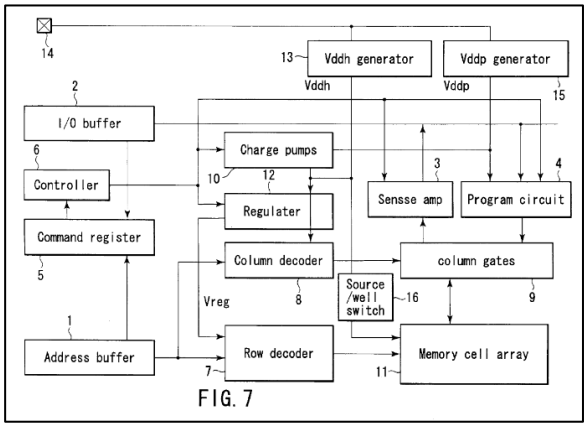


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.

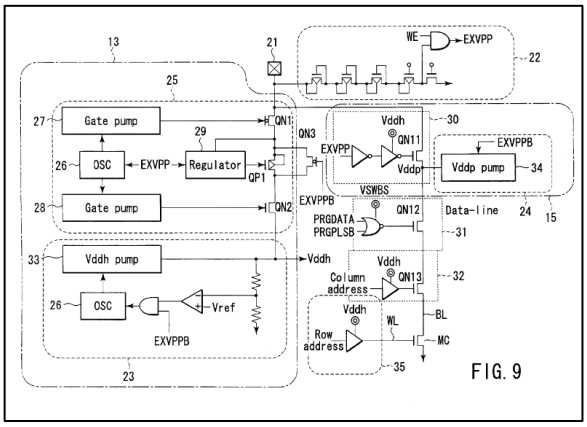


FIG. 9

Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

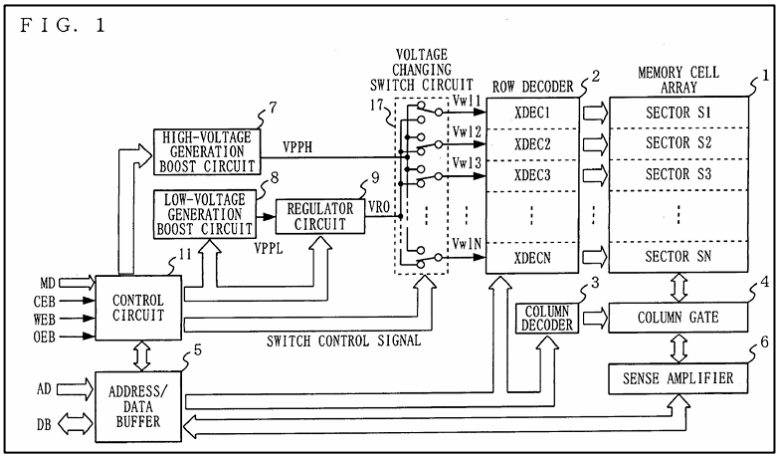
Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17

comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.

FIG. 1



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

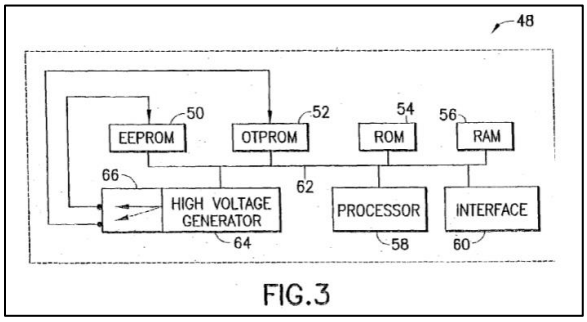


FIG.3

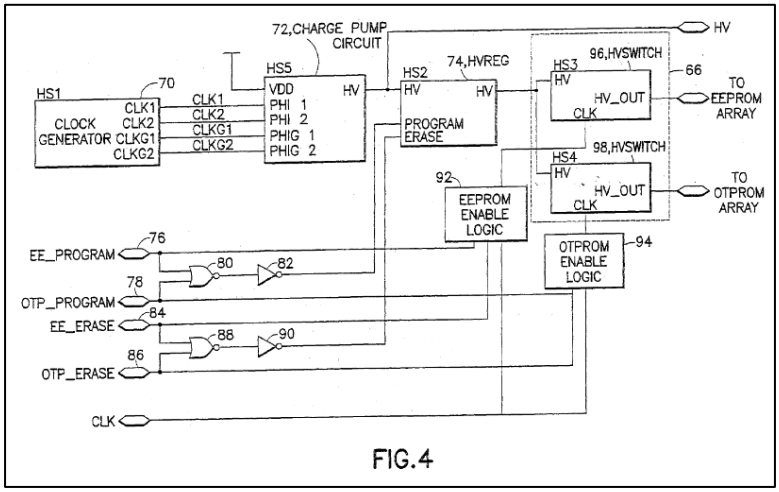


FIG.4

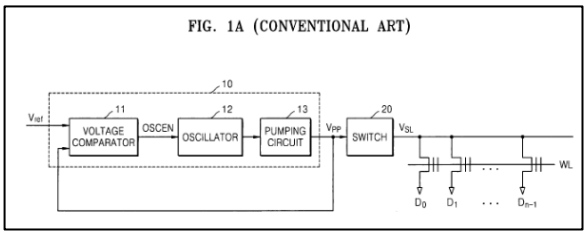
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

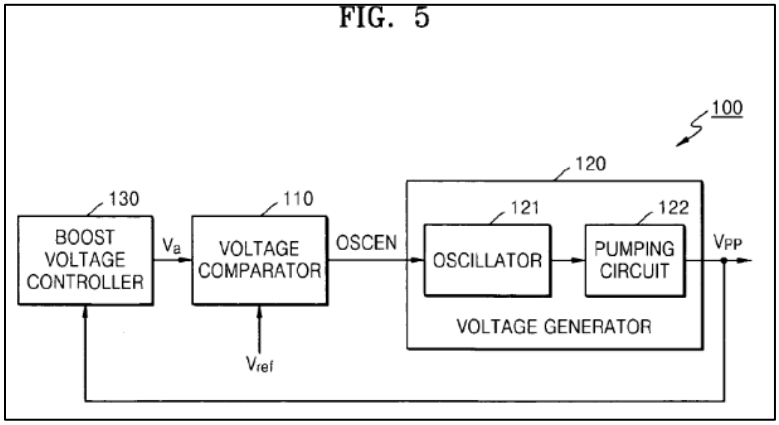
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

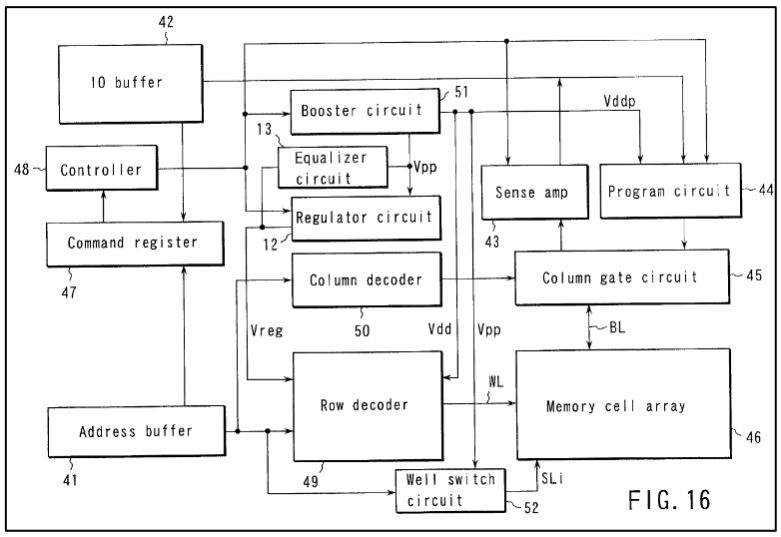
The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.



Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

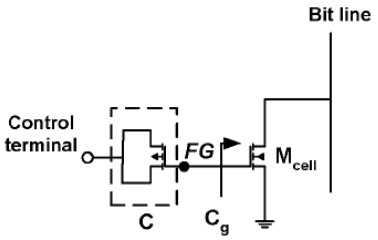


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

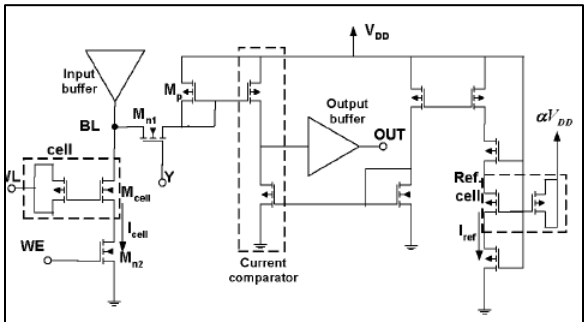


Figure 3. Current mode Sense Amplifier.

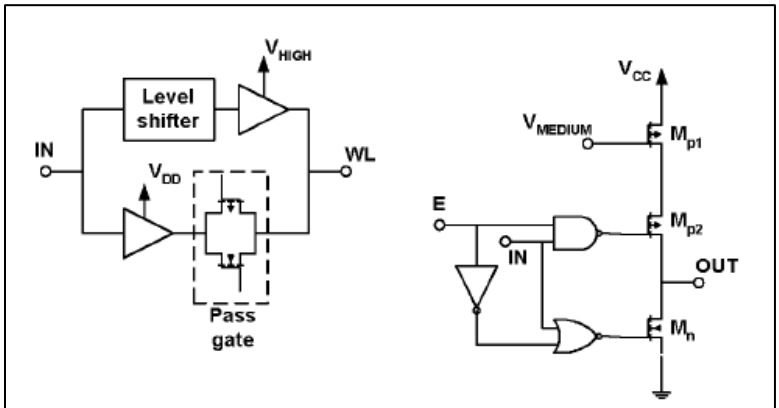


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

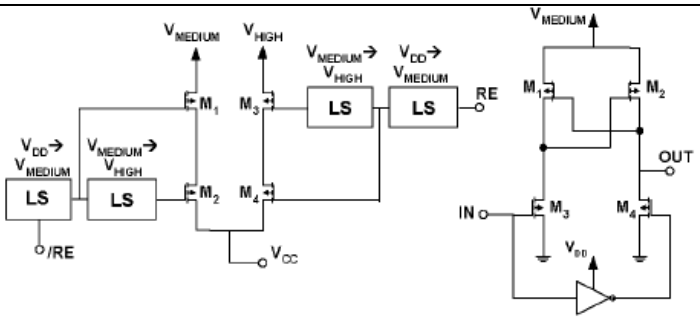


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

21[a] The semiconductor memory device of claim 1, wherein

To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious the semiconductor memory device of claim 1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.

21[b] an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

The Omnibus References disclose and/or render obvious an output of a booster circuit is coupled to a source terminal of the voltage applying transistor.

See, e.g., claim limitations 1[b] and 1[c], *supra*.

Banba at 2:66-3:5:

Meanwhile, known non-volatile semiconductor memory devices include flash EEPROMs. A flash EEPROM includes stacked transistors having a floating gate and a control gate as memory cells. Such a memory cell changes its threshold voltage for data writing/erasing operations as electrons are charged into and discharged from it through the floating gate.

Banba at 4:24-34:

According to another aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: a memory cell array having a plurality of non-volatile memory cells; a write/erase circuit for the plurality of non-volatile memory cells; and a circuit for generating desired voltages which are different from an external power supply voltage and applied

to the plurality of non-volatile memory cells, the circuit including a booster circuit for generating a boosted voltage, wherein a power of the booster circuit is set higher in a write mode and is set lower in an erase mode when the boosted voltage of the booster circuit falls below a predetermined voltage.

Banba at 4:47-62:

According to another aspect of the present invention, there is provided a semiconductor memory device comprising: a first booster circuit for outputting a first boosted voltage obtained by boosting a power supply voltage; a second booster circuit for outputting a second boosted voltage higher than the first boosted voltage by boosting the power supply voltage; a regulator circuit for regulating the second boosted voltage output from the second booster circuit to generate a regulated voltage; a transistor having a current path with an end applied with a voltage from the first booster circuit in a write or erase mode and the other end connected to an end of a current path of a memory cell; and a circuit for shifting a level of a signal to a gate of the transistor supplied to a level of the regulated voltage output from the regulator circuit.

Banba at 6:65-7:24 and Fig. 6:

FIG. 6 is a schematic block diagram of a non-volatile semiconductor memory device having a power supply circuit shown in FIG. 5.

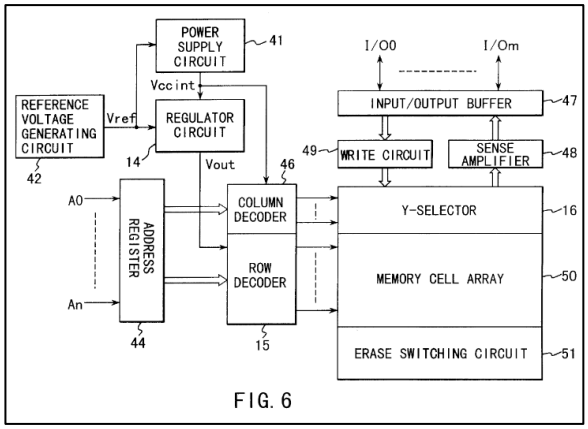


FIG. 6

The power supply circuit 41 of FIG. 6 corresponds to the power supply circuit of FIG. 5 and generates a boosted voltage of Vccint.

Reference voltage generating circuit 42 generates reference voltage Vref. Regulator circuit 14 generates a predetermined output voltage Vout based on the reference voltage Vref, in accordance with a mode of operation that may be the write mode, the erase mode, the write verify mode or the read verify mode.

Internal address signals (or external address signals) AO through An are fed to row decoder 15 and column decoder 46 by way of address register 44. The output voltage Vout of the regulator circuit 14 is applied to a predetermined word line selected by the address signals AO through An by way of the row decoder 15.

In the write (program) mode, data are fed to predetermined memory cells of memory cell array 50 by way of input/output buffer 47, write circuit 49 and Y-selector 16.

In the read mode, data are used for verification by way of the Y-selector 16 and sense amplifier 48 or output to an external chip further by way of the input/output buffer 47.

In the erase mode, the voltage applied to the sources of the memory cells is switched by erase switching circuit 51.

Banba at 9:47-67 and Fig. 10:

FIG. 10 is a schematic block diagram of a power supply circuit providing the voltages of FIG. 9.

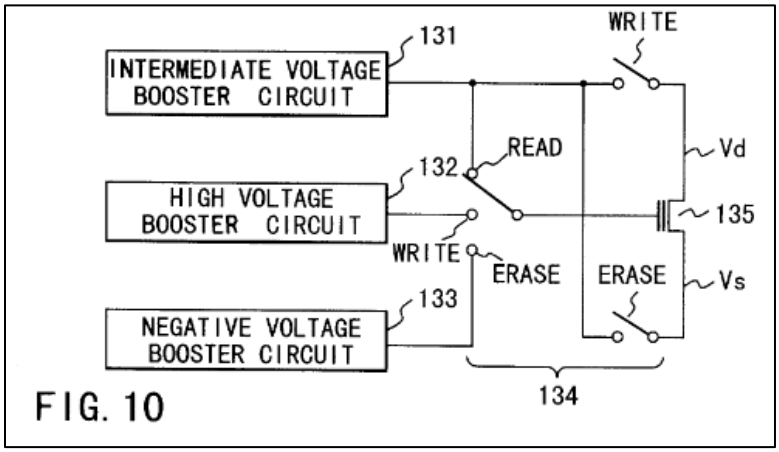


FIG. 10

The voltage to be applied to the drain in the write mode, the voltage to be applied to the source in the erase mode and the voltage to be applied to the control gate in the read mode can be supplied from a single booster circuit to reduce the number of booster circuits to three and simplify the configuration of the booster circuit system.

More specifically, as shown in FIG. 10, this embodiment adopts booster circuits of three different types. Intermediate voltage booster circuit 131 provides large electric current between several mA and tens of several mA with an intermediate voltage level of about 5 V. High voltage booster circuit 132 provides an electric current between hundreds of several micro amperes and several mA with a high voltage of about 10 V. Negative voltage booster circuit 133 provides a negative voltage of about -10 V. By way of a switching circuit 134, the intermediate voltage booster circuit 131 is connected to the control gate of memory cell 135 in the read mode, to the drain of the memory cell 135 in the write mode and the source of the memory cell 135 in the erase mode. Also by way of the switching circuit 134, the high voltage booster circuit 132 is connected to the control gate of the memory cell 135 in the write mode. Again, by way of the switching circuit 134, the negative voltage booster circuit 133 is connected to the control gate of the memory cell 135 in the erase mode.

Daga at [0021]-[0027] and Figs. 3-4:

FIG. 3 is a schematic illustrating one embodiment of a power supply management system for

memory in a system-on-a-chip (SOC). SOC 300 illustrates one example of how power is distributed. External voltage level 310, for example 3.3V or 5V, is applied to voltage regulator 315, analog circuit 320, and input/output pads 325. Voltage regulator 315 generates regulated voltage level 330, for example 1.8V for a 0.18 μm logic. Regulated voltage level 330 is applied to memory 340, for example embedded EEPROM and FLASH memory, and advanced logic 335, for example the micro-controller, CMOS memories, glue logic etc. External voltage level 310 is also applied to memory 340.

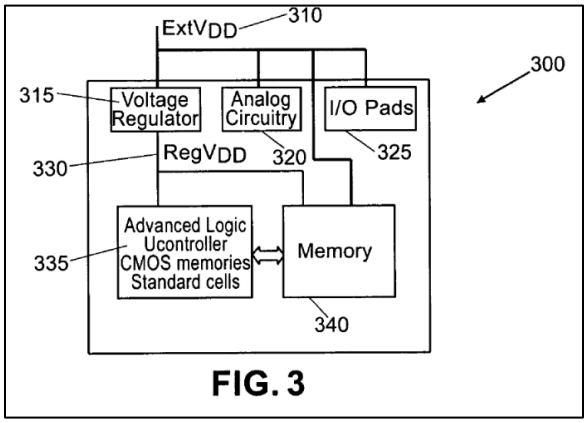


FIG. 3

FIG. 4 is a schematic diagram illustrating one embodiment of memory 340 from FIG. 3. Memory 400 receives external voltage level 405 and regulated voltage level 410 (from voltage regulator 315 of FIG. 3). Charge pump 407 receives external voltage level 405 and generates high voltage level 415, which is used to program memory cells during memory write. Because charge pump 407 is supplied with the higher, external voltage level 405, charge pump 407 may be smaller than a conventional memory charge pump supplied by regulated supply voltage 410.

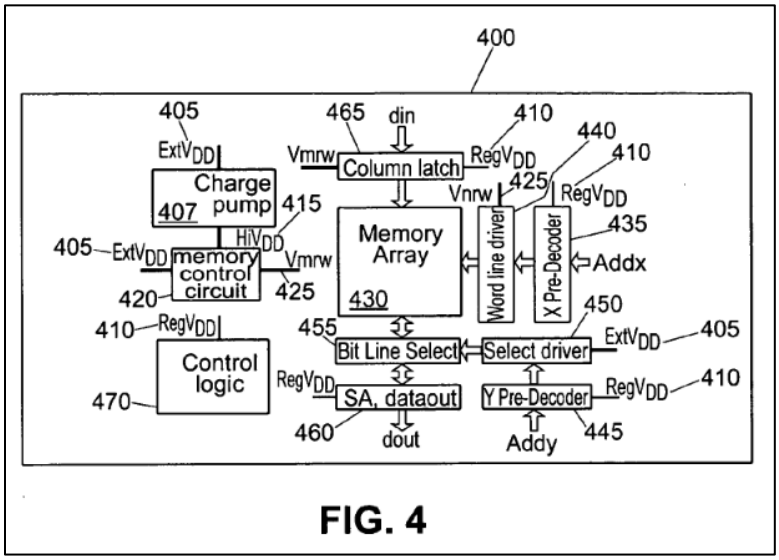


FIG. 4

Memory control circuit 420 receives high voltage level 415 from charge pump 407 and external voltage level 420. Memory control circuit 420 supplies either high voltage level 415 or external voltage level 420 to variable voltage line 425. During a memory read, memory control circuit 420

supplies external voltage level 420 to variable voltage line 425. During a memory write, memory control circuit 420 supplies high voltage level 415 to variable voltage line 425.

Memory 400 includes memory array 430 with memory cells, word lines and bit lines (not shown). X pre-decoder 435 receives and decodes an address and is powered at regulated voltage level 410. X pre-decoder 435 is connected to word line driver 440 with a word select input line (see FIG. 6). Word line driver 440 receives power from variable voltage line 425 and receives a word select that indicates a word line to supply with power. During memory read, word line driver 440 supplies the word line with external voltage level 405. During memory write, word line driver 440 supplies the word line with high voltage level 415.

Y pre-decoder 445 receives and decodes an address and is powered at regulated voltage level 410. Y pre-decoder 445 is connected to select driver 450. Select driver 450 receives external voltage level 405 and a bit select signal from Y pre-decoder 445, which is shifted to external voltage level 405 due to the level shifter.

Sense amplifier 460 with a data output is connected to bit line select 455. Sense amplifier 460 receives regulated voltage level 410.

Daga at [0053] and Fig. 9:

FIG. 9 is a flow diagram illustrating a method of driving an embedded non-volatile memory, having a word line and a bit line, at an external voltage level and at a regulated voltage level, the external voltage level higher than the regulated voltage level lower. In block 900, boost the external voltage level to a high voltage level, the high voltage level higher than the external voltage level. In block 910, supply the high voltage level to a variable voltage line during memory write. In block 920, supply the external voltage level to the variable voltage line during memory read. In block 930, switch the high voltage level from the variable voltage line to the word line during memory write. In block 940, precharge the word line with the regulated voltage level during memory read. In block 950, switch the external voltage level from the variable voltage line to the word line during memory read. In block 960, turn on a transistor in the bit line select with the external voltage level. In block 970, turn on a transistor in the bit line select with the regulated voltage level.

Shor at Fig. 3:

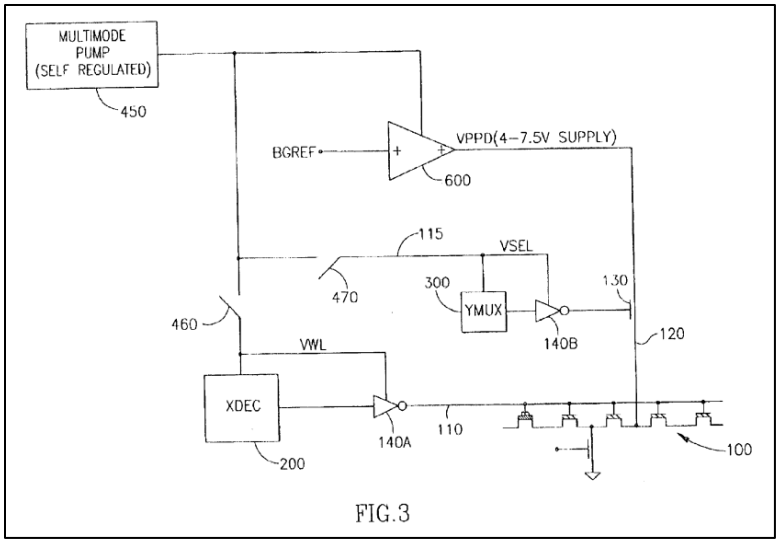


FIG.3

Shor at 2:42-61:

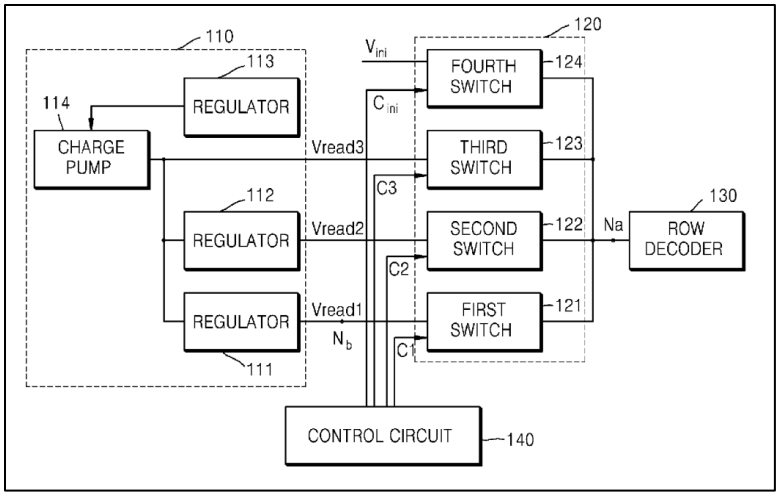
As mentioned above, charge pump circuits are required to provide all voltage levels above VDD and below VSS (VSS=GND=0). As seen in FIG. 1, according to the prior art, two or more charge pumps are required on a memory chip. Since each charge pump circuit may have a pumping efficiency (Power Out/Power In) of 20-30% (e.g. each 1 mA of current pumped at 8-10V may require 10-12 mA of VDD current), charge pump currents can comprise the majority of VDD current used by a memory chip. In addition, charge pumps are large circuits and can take up as much as 50% of a chip's die area.

What has been absent from the prior art, and is desired, is a method and circuit capable of driving the WL/select capacitive loads and efficiently driving high currents to the BL at a lower voltage, while avoiding the necessity of having two distinct positive charge pumps. Thus, it would be beneficial to reduce the number of charge pumps required for a non-volatile memory array such as an NROM EPROM array.

Shor at 3:35-41:

According to some embodiments of the present invention, the multi-mode charge pump circuit may include a multimode charge pump. This pump may have self-regulating capabilities, such as the charge pump taught in U.S. Patent No. 6,577,514, entitled “Efficient Charge Pump with Constant Boosted Output Voltage” by Shor et. al. In other embodiments of the present invention, the multimode charge pump circuit may be a combination of a conventional charge pump with an external voltage and/or current regulating circuit. Charge pump circuits are well known, and any such circuit, presently known or to be devised in the future, is applicable to the present invention.

Im at Fig. 4:



Im at 6:14-36:

As illustrated in FIG. 4, the wordline voltage generating unit **110** may include one or more regulators **111**, **112**, and **113** and a charge pump **114**. The regulator **113** regulates a predetermined power source voltage VDD and outputs it. The output of the regulator **113** is provided to the charge pump **114**, and the charge pump **114** generates a voltage having a high level based on a pumping operation and outputs the voltage, which may be used as a third wordline voltage Vread **3**.

Meanwhile, the regulators **111** and **112** may generate a first wordline voltage Vread **1** and a second wordline voltage Vread **2**, respectively, using the output of the charge pump **114**. The first through third wordline voltages Vread **1** through Vread **3** which may be generated as described above are provided to the switch unit **120**.

The switch unit **120** includes multiple switches. For example, the switch unit **120** may include a first switch unit (including the first through third switches **121**, **122**, and **123**) for switching the first through third wordline voltages Vread **1** through Vread **3**. In addition, the switch unit **120** may further include a second switch unit (including fourth switch **124**). The first through fourth switches **121**, **122**, **123**, and **124** are commonly connected to the output node Na.

Cho at Abstract:

Provided is a voltage regulator of a flash memory device. Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively

low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

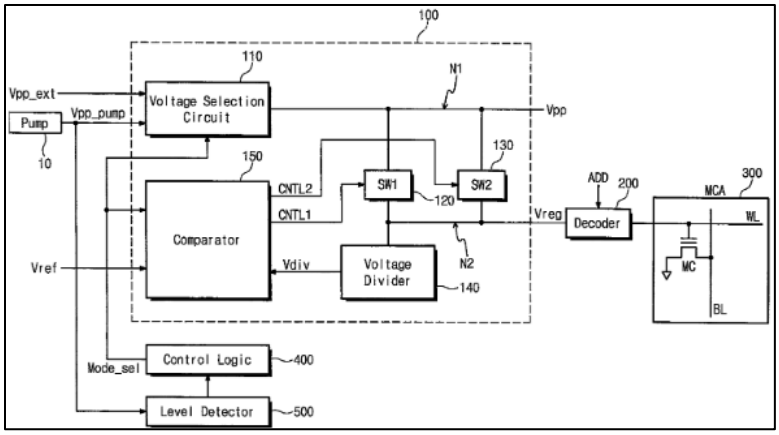
Cho at 2:24-64:

Embodiments of the invention provide a voltage regulator that is configured to regulate either an internal pumping voltage or an external high voltage. In embodiments of the invention, the voltage regulator includes two switches having different switching current characteristics: when regulating the internal pumping voltage, the voltage regulator is configured to activate a switch having a relatively high switching current to output the regulated voltage; but when regulating the high external voltage, the voltage regulator is configured to activate a switch having a relatively low switching current to output the regulated voltage during at least a set-up time. In an embodiment of the invention, the voltage regulator may be configured to activate both switches to regulate the high external voltage after the set-up time. In yet another embodiment of the invention, after the set-up time, the voltage regulator may be configured to deactivate the switch having the relatively low switching current and activate the switch having the relatively high switching current to regulate the high external voltage.

Embodiments of the present invention provide a voltage regulator of a flash memory device, the voltage regulator configured to output a regulated voltage, the voltage regulator including: a selection circuit configured to receive and selectively output at least one of an external high voltage and an internal pumping voltage, the selection being in response to a mode signal, a first state of the mode signal associated with the internal pumping voltage and a second state of the mode signal associated with the external high voltage; a first switch coupled to an output of the selection circuit, the first switch having a first switching current; a second switch coupled to the output of the selection circuit, the second switch having a second switching current, the second switching current being different from the first switching current; and a switch control circuit coupled to the first switch and the second switch, the switch control circuit configured to select at least one of the first switch and the second switch in response to the mode signal, the switch control circuit further configured to control the at least one selected switch according to the regulated voltage.

Cho at 3:44-5 and Fig. 2:

FIG. 2 is a block diagram schematically illustrating a flash memory device according to an embodiment of the present invention. Referring to FIG. 2, a voltage regulator **100** of the flash memory device according to the present invention includes respective switches **120** and **130** with different magnitudes of switching current. The voltage regulator **100** of the present invention generates a regulated voltage Vreg at node N**2** in which an overshoot and a ripple are removed even during an external high voltage mode, and it provides the regulated voltage Vreg to a decoder **200**. A voltage regulator configuration and regulating operation will be illustrated below with reference to the accompanying drawings.



Cho at 4:4-21:

A first switch 120 provides the high voltage Vpp applied to the first node N 1 as a regulated voltage Vreg of a second node N 2 in response to a first switch control signal CNTL 1 . The second switch 130 transfers the high voltage Vpp applied to the first node N 1 to the second node N 2 in response to a second switch control signal CNTL 2 . However, the first switch 120 and the second switch 130 are constructed such that the magnitudes of switching current are not equal to each other. For example, the first switch 120 and the second switch 130 may be constituted as switching devices having different aspect ratios. Thus, they may be constituted as switching devices of which current passing capabilities (current drivabilities) are different from each other when the switching devices are turned on. That is, the first and second switches 120 and 130 can switch the current with different magnitudes depending on the selected mode, and thus it is possible to set the regulated voltage Vreg in which the overshoot and the ripple are removed.

Cho at 4:45-62:

The decoder 200 selects a word line WL of a memory cell array 300 in response to an address ADD, and supplies the regulated voltage Vreg regulated by the first switch 120 or the second switch 130 to the selected word line WL. The memory cell array 300 includes a plurality of memory cells MC arranged at intersections of word lines WL and bit lines BL which are arranged in row and column directions, respectively. As the regulated voltage Vreg is supplied to the selected word line WL through the decoder 200 , a program operation, a program verify operation, a reading operation, etc, of the flash memory device will be performed in a well-known manner. However, the regulated voltage Vreg is not limited to the word line voltage only. That is, the regulated voltage Vreg may be supplied as various driving voltages in the memory device. It is well known to those skilled in the art that the regulated voltage Vreg may be supplied to a bit line, a bulk, etc., so that it can be used for other operations besides the programming operation.

Tanzawa-452 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and

a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-452 at [0002]-[0003] and Fig. 1:

This invention relates to a boosted voltage generating circuit for boosting power supply voltage and a semiconductor memory device having the same and more particularly to a semiconductor memory device having memory cells and a boosted voltage generating circuit for generating high voltage used at the data erasing or programming time of the memory cell.

A flash memory is provided as one type of a semiconductor memory device. FIG. 1 shows the cross sectional construction of one memory cell element of the flash memory. In FIG. 1, an N-type well region (N-well) 72 is formed in a P-type semiconductor substrate (P-substrate) 71. Further, a P-type well region (P-well) 73 is formed in the N-type well region 72 . In the P-type well region 73 , source and drain regions 74 , 75 of a memory cell which are formed of n + -type regions are separately formed. A floating gate electrode 76 is formed above the channel region between the source and drain regions 74 and 75 with an insulating film disposed there between and a control gate electrode 77 is formed above the floating gate electrode 76 with an insulating film disposed there between.

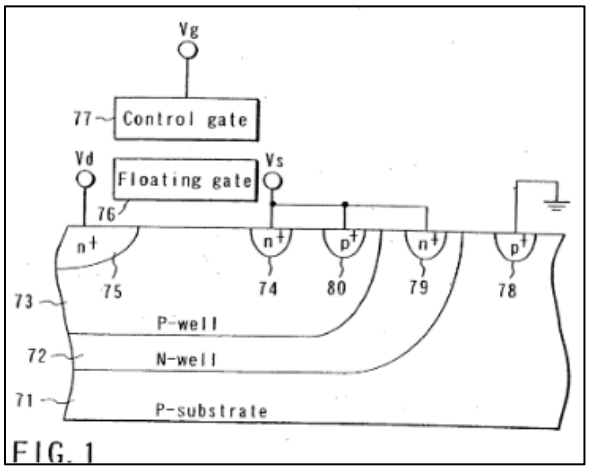


FIG. 1

Tanzawa-452 at [0110] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process.

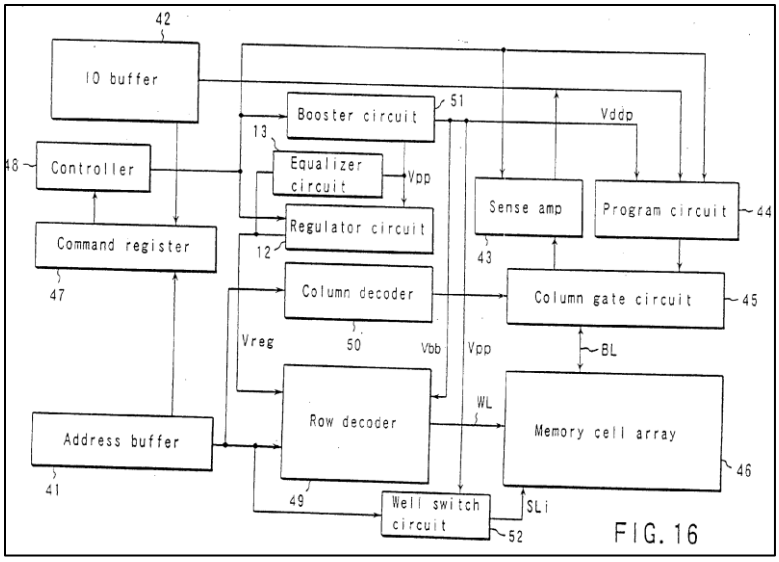


FIG. 16

Tanzawa-452 at [0048]:

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-452 at [0115]:

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12 , it becomes unnecessary to use a plurality of charge pump circuits.

Nierle at Abstract:

A device or method for effectively stressing an interconnect in a test current path of a semiconductor device, which test current path is other than a current path used during normal operation of the semiconductor device. An operational voltage is adjusted to a test voltage, the test current path is opened and the test voltage is supplied to the test current path.

Nierle at [0014] and Fig. 1:

In the memory device 100 shown in FIG. 1, the memory cells 103 are selectively connected across the word lines Wn, Wn−1, Wn−2 and Wn−3 to WL on/off switches 101 and across the bit lines B 0, B 1, B 2 and B 3 to a column (BL) decoder 120. The WL on/off switches 101 are selectively connected to a word line-off (WL-off) potential (e.g., ground) and to a row (WL) decoder 110. In addition, the memory cells 103 are also selectively connected across the word lines Wn, Wn−1,

Wn−2 and Wn−3 to the WL-off potential through WL reset switches 102. The WL on/off switches 101 are selectively connected across conductive layers 140, 141, 142 and 143 and interconnects 151, 152, 153 and 154 respectively to conductive layer 130, which in turn is connected to a word line-on (WL-on) potential through a voltage regulator 170.

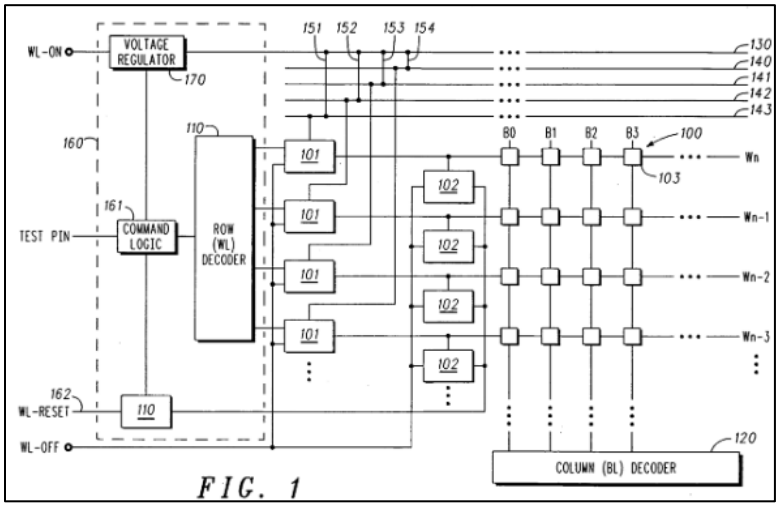


FIG. 1

Nierle at [0021]-[0024] and Fig. 2:

FIG. 2 includes a more detailed diagram of some of the components shown in FIG. 1. These include the WL on/off switches 101, the WL reset switch 102 and the memory cells 103. The WL on/off switches 101 can include p-channel MOSFET (PFET) 201 and an n-channel MOSFET (NFET) 202 or other transistors and switching devices. When a selected WL on/off switch 101 receives a WL control signal from the row (WL) controller 110, it activates the word line associated therewith. The WL reset switches 102 includes an NFET 203 or other transistor and switching device arranged between the word line and the WL-off potential. When WL reset switches 102 are reset by receiving a WL reset signal from the WL-reset controller 115, all the word lines are reset or opened, thereby establishing a current path from the selected word line through the reset switch to the WL-off potential.

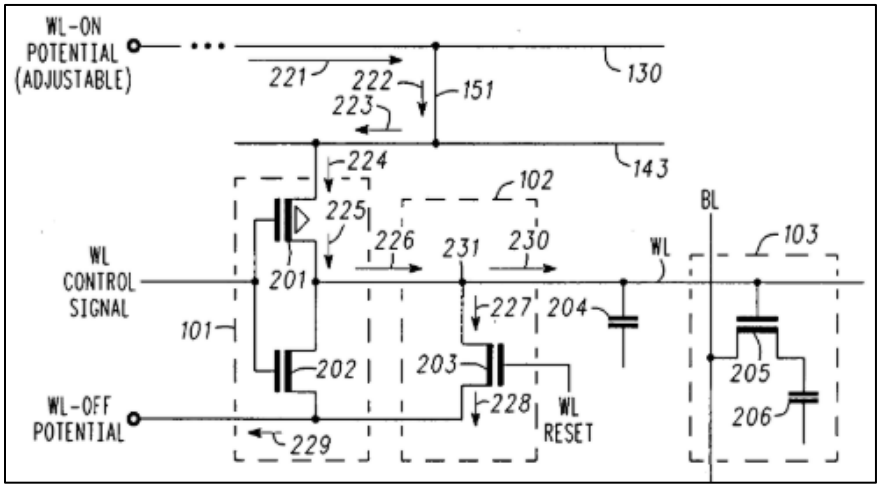


FIG. 2 could easily adapted to bit lines or other components that are powered by interconnects. A test circuitry for a bit line can include switches for activating bit lines, and switches for equaling or draining voltage on or from bit lines. An interconnect associated with a bit line can be stressed by precharging the current path to the bit line, and activating the bit line while equalizing or draining voltage on or from the bit line by appropriate switches.

Yamauchi at Abstract:

A memory cell is formed by flip-flop connection of a load transistor pair of a first load transistor and a second load transistor and a drive transistor pair of a first drive transistor and a second drive transistor. A first switch which is controlled by a wordline and a second switch which is activated only at the time of the write operation are connected in series to a first memory node. The second switch is serially coupled between the first memory node and the first drive transistor. An electric current is injected from a sense amplifier into a bitline pair selected at the time of the read operation, to detect an impedance which varies with the signal potential at the first memory node.

Yamauchi at 5:27-56:

It is preferred in the above-described SICD wherein the memory cell is formed by establishing a flip-flop connection among a first load transistor coupled to a first power supply, a second load transistor which forms a pair with the first load transistor, a first drive transistor coupled to a second power supply and a second drive transistor which forms a pair with the first drive transistor that:

the memory cell further includes:

(a) a first memory node which is coupled to the first load transistor and which holds a signal potential;

(b) a second memory node which is coupled to the second load transistor and which holds a signal potential in complementary relationship with the signal potential held by the first memory node;

(c) a first switch transistor which is serially coupled between the first memory node and the first control line and which is controlled by a third control line wherein one of source/drain electrodes of the first switch transistor is coupled to the first control line; and

(d) a second switch transistor which is controlled by the second control line wherein one of source/drain electrodes of the second switch transistor is coupled to the first memory node and the other of the source/drain electrodes of the second switch transistor is coupled to the other of the source/drain electrodes of the first switch transistor wherein the second switch transistor is serially coupled between the first memory node and the first drive transistor.

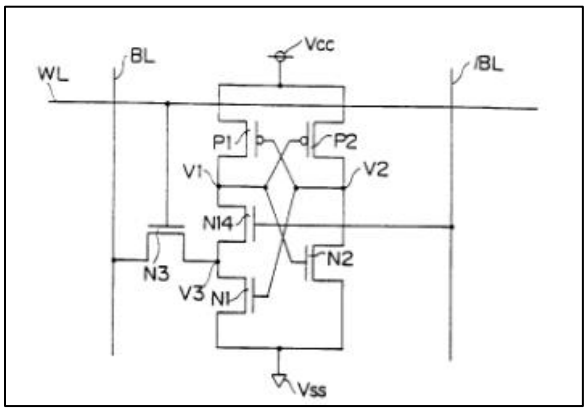
Yamauchi at 7:34-47:

It is preferred in the above-described SICD that the memory cell is coupled, in parallel with the first drive transistor, between the first memory node and the second power supply and that the memory cell further includes a fourth switch transistor which is controlled by the potential at a contact point of the first switch transistor and the second switch transistor. This arrangement causes the fourth switch transistor to start functioning earlier than the first drive transistor which is

controlled by the second memory node. As a result, the fourth switch transistor that is coupled to the first memory node which is a non-target node in write mode starts functioning earlier than the first drive transistor and the first memory node promptly approaches the reference potential. The access time can be reduced.

Yamauchi at 21:30-64 and Fig. 1A:

FIG. 1(a) is a circuit diagram of a memory cell in accordance with the first embodiment. P1 is a first load transistor of a first inverter and is coupled to a first power supply Vcc. P2 is a second load transistor of a second inverter, is coupled to first power supply Vcc and forms a pair with first load transistor P1. N1 is a first drive transistor for driving the first inverter. N2 is a second drive transistor for driving the second inverter and forms a pair with first drive transistor N1. V1 is a first memory node for holding a memory cell signal potential. V2 is a second memory node for holding an opposite potential to that of first memory node V1. BL is a bitline acting as a first control line. Bitline BL is charged to a first high data potential Vu1 (the second potential) in a write mode of operation while on the other hand in a read mode of operation bitline BL is charged to a ground potential Vx1 (the first potential) for memory cells in a designated column of the memory cell array. /BL is a complementary bitline acting as a second control line. Complementary bitline /BL, as a write control line, is charged to a second high data potential Vu2 (the third potential) in a write mode of operation while on the other hand in a read mode of operation complementary bitline /BL is referred to by bitline BL and is charged to ground potential Vx1. WL is a wordline for activating memory cells in a selected row of the memory cell array, acting as a third control line. Vcc is a first power supply for driving a memory cell. Vss is a second power supply which is at the ground potential (i.e., the reference potential for driving memory cells). N3 is a first switch that allows bitline BL to read or write first memory node V1 only when wordline WL is activated. N14 is a second switch that enables the writing of information into first memory node V1 only when complementary bitline /BL is activated in write mode. V3 is a first contact point of first drive transistor N1 and first switch N3.



Tanzawa-945 at Abstract:

A memory cell array has memory cells arranged in a matrix form. The memory cell includes a floating gate and a control gate. Word lines are each coupled to the control gates of the memory cells which are arranged on a corresponding one of the rows in the memory cell array. Bit lines are each coupled to drains of the memory cells which are arranged on a corresponding one of the

columns in the memory cell array. An external voltage is supplied from the exterior to an external voltage input terminal. A first voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the word line coupled to the control gates. A second voltage generating circuit lowers the external voltage to generate a voltage which is to be supplied to the bit line coupled to the drains.

Tanzawa-945 at [0047]-[0052] and Fig. 7:

There will now be described a semiconductor device according to a first embodiment of this invention with reference to the accompanying drawings. FIG. 7 is a block diagram of a flash memory according to the first embodiment.

A charge pump circuit 10 boosts the input power supply voltage to output voltage which is supplied to a memory cell array 11 at the time of readout, program or erase. A regulator 12 receives voltage Vpp which is higher than the power supply voltage and outputs controlled voltage Vreg. The voltage Vreg is supplied to the word line selected by the row decoder 7.

A Vddh generator 13 converts voltage Vpp supplied from a Vpp pad 14 into word line power supply voltage Vddh which is supplied to the word line connected to the control gate of the memory cell at the program time. The word line power supply voltage Vddh is supplied to the common well region or source of the memory cell at the erase time. A Vddp generator 15 converts the voltage Vpp supplied from the Vpp pad 14 into bit line power supply voltage Vddp which is supplied to the bit line connected to the drain of the memory cell at the program time.

A source/well switch 16 causes the voltage Vddh to be selectively supplied to the well region or the source of each block via the source line at the data erase time.

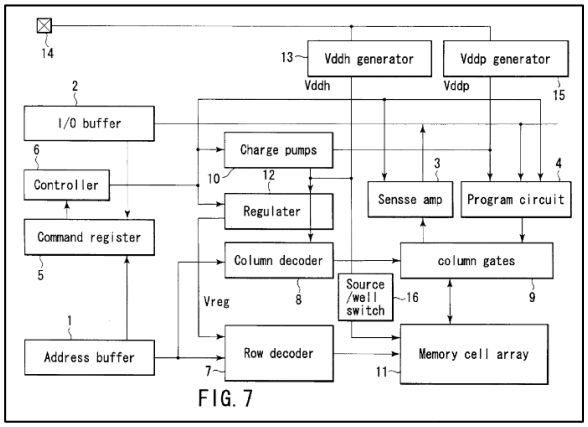


FIG. 7

Tanzawa-945 at [0058]-p0063] and Fig. 9:

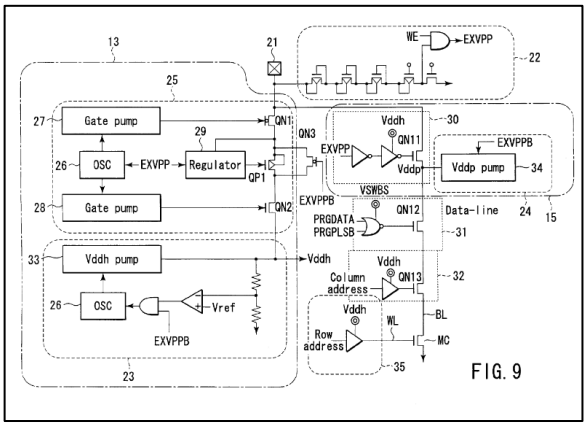
FIG. 9 shows the configurations of the Vddh generator and the Vddp generator according to the first embodiment and containing the switch circuit shown in FIGS. 8A, 8B, 8C.

While the signal EXVPPB="L" is input to a Vddh booster circuit 23 and a Vddp booster circuit 24, the Vddh booster circuit 23 and the Vddp booster circuit 24 are not operated.

If the signal EXVPP="H" is input to an oscillator circuit (OSC) 26 in a Vddh switch circuit 25, voltages of approximately 15V are generated from first and second gate pumps 27 and 28 and respectively supplied to the gates of the NMOS transistors QN1, QN2. As a result, the NMOS transistors QN1, QN2 are turned ON and the voltage Vpp supplied to the Vpp pad 21 from the exterior is transferred.

Further, if the signal EXVPP="H" is input to a regulator 29, negative feedback occurs and voltage transferred from the PMOS transistor QP1 to the NMOS transistor QN2 is controlled to be set to approximately 10V. The voltage of 10V is transferred as it is via the NMOS transistor QN2 and output as the voltage Vddh of 10V.

After this, the output voltage Vddh of 10V is input to the regulator 12 shown in FIG. 7 which in turn generates controlled voltage Vreg (=approximately 9V). The voltage Vreg is supplied to a word line selected by the row decoder 7.



Kawai at Abstract:

A plurality of switches composing a voltage changing switch circuit 17 are supplied with a plurality of types of voltages, and are provided so as to correspond to a plurality of row decoders 2, such that each switch can separately select and output any of the plurality of types of voltages to the corresponding row decoder 2. Voltage boost circuits 7, 8 generate a plurality of types of voltages by boosting a power supply voltage. A regulator circuit 9 steps down at least one of the plurality of types of voltages generated by the voltage boost circuits 7, 8 to stabilize a voltage value, and outputs the resultant voltage to each switch. Each row decoder 2 selects a memory cell by using a voltage outputted from the corresponding switch. Thus, it is possible to reduce a time required for a program/program verify operation, while reducing power consumption.

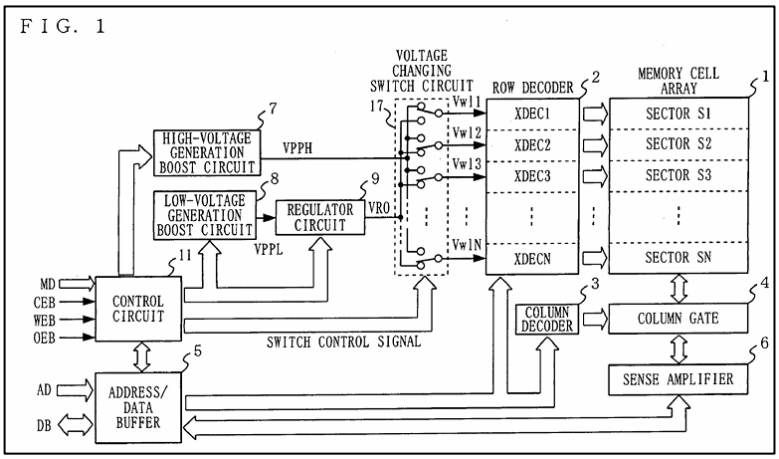
Kawai at [0059]-0060] and Fig. 1:

FIG. 1 is a block diagram showing a structure of a nonvolatile semiconductor memory device in a first embodiment of the present invention. In FIG. 1, any component elements that have similar counterparts in FIG. 16 will be denoted by the same reference numerals as those used therein, and the detailed description thereof is omitted.

[0060] The first embodiment is characterized by including a voltage changing switch circuit 17

comprising N (N is natural number) unit switches using two types of voltages: a high boost output voltage VPPH (=10V) and a regulator output voltage VRO (=5.5V) as an input, and selecting and outputting one of the two types of voltages in accordance with a switch control signal. In a stop state (STOP) or a program verify operation (PV), all unit switches of the voltage changing switch circuit 17 select the regulator output voltage VRO in accordance with a switch control signal. In a program operation (Program), only a desired one unit switch selects the high boost output voltage VPPH, whereas the other unit switches select the regulator output voltage VRO. At this time, word line supply voltages Vwl1 to VwlN, which are output voltages of the voltage changing switch circuit 17, are supplied to decoder blocks XDEC1 to XDECN, respectively.

FIG. 1



Barnett at Abstract:

A single chip embedded microcontroller has a processor that communicates with multiple non-volatile erasable PROMS which may be an OTPROM and an EEPROM. The processor also communicates with a high voltage generator that produces the erase and write voltages for the OTPROM and EEPROM. A switch communicates with the high voltage generator and switches the erase and write voltages alternately between the OTPROM and EEPROM. The OTPROM and EEPROM are FLASH arrays. The FLASH array technology allows the EEPROM and OTPROM to have similar erase and write voltages and therefore to share one high voltage generator. The high voltage generator is switched alternately between the first and second non-volatile erasable PROM arrays to enforce the principle that the EEPROM and OTPROM cannot be written to or erased at the same and may only be written to or erased one at a time.

Barnett at [0007]:

A single chip embedded microcontroller has a processor communicating with first and second non-volatile erasable PROM arrays. The processor reads, erases and writes information to and from the non-volatile erasable PROM arrays. A high voltage generator provides the erase and write voltages for the first and second non-volatile erasable PROM arrays and also communicates with the processor. A switch communicating with the high voltage generator, switches the erase and write voltages alternately between the first and second non-volatile erasable PROM arrays. The first and second non-volatile erasable PROM arrays are FLASH arrays and may be an OTPROM and EEPROM, respectively.

Barnett at [0033]-[0035] and Figs. 3-4:

FIG. 4 is a block diagram of high voltage generator 64 (shown in FIG. 3). A clock generator 70 provides clock signals clk1, clk2, clkg1, and clkg2 to a capacitive charge pump circuit 72. The clock signals provide the timing signals necessary for the charging of the capacitors in the charge pump and its operation. The output of charge pump 72 is an unregulated voltage having an amplitude of about 19 v. This voltage is provided to a high voltage regulator 74 (hvreg) which provides regulated voltages of 12 v. and 15 v. necessary for erasing and writing to EEPROM 50 and OTPROM 52 (shown in FIG. 3). Signals EE PROGRAM 76 and OTP PROGRAM 78 from processor 58 (shown in FIG. 3) help activate high voltage regulator 74 to provide the correct write voltage for EEPROM 50 and OTPROM 52 respectively. EE PROGRAM 76 and OTP PROGRAM 78 both provide a signal to NOR gate 80 and inverter 82. NOR gate 80 and inverter 82 provide an initializing signal to high voltage regulator 74 to produce the write voltage if either EE PROGRAM 76 and OTP PROGRAM 78 is present. Similarly, signals EE ERASE 84 and OTP ERASE 86 from processor 58 help activate high voltage regulator 74 to provide the correct erase voltage for EEPROM 50 and OTPROM 52, respectively. Nor gate 88 and inverter 90 allow either EE ERASE 84 and OTP ERASE 86 to initiate the erase signal.

If EE PROGRAM 76 signal is provided to high voltage regulator 74, a write high voltage of 15 v. is provided to a pair of high voltage switches 96 and 98 in switch 66 (shown in FIG. 3). EE PROGRAM 76 also enables EEPROM Enable Logic 92 which provides a clock signal to high voltage switch 96 which clocks the 15 v. write high voltage to EEPROM array 50. Similarly the other signals EE ERASE 84, OTP PROGRAM 78 and OTP ERASE 86 cause either the write or erase voltage to be applied to EEPROM array 50 or OTPROM array 52.

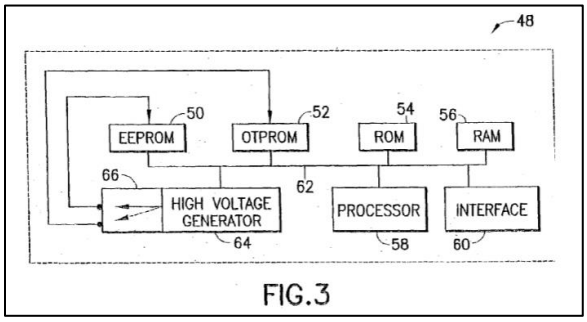


FIG.3

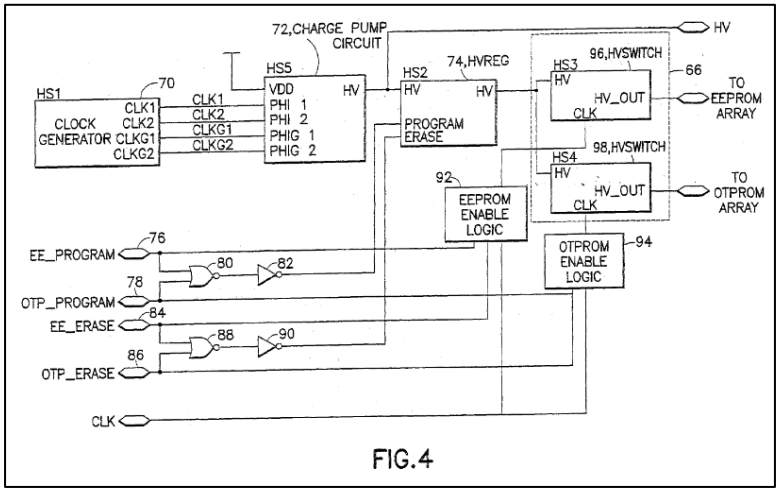


FIG.4

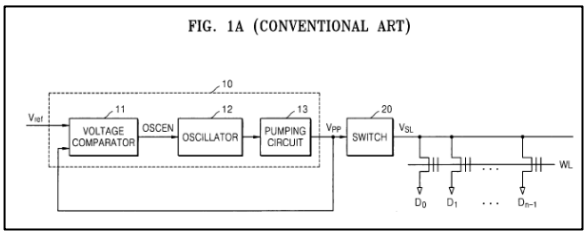
O at Abstract:

A boost voltage generating circuit and method thereof. The example boost voltage generating circuit may include a voltage comparator comparing an input voltage and a reference voltage and generating a control signal based on a result of the voltage comparison, the input voltage based on a feedback boost voltage, a voltage generator generating a boost voltage in response to the control signal and a boost voltage controller including a first resistor with a first end connected to the boost voltage and a second end connected to the voltage comparator, the boost voltage controller controlling a level of current flowing through the first resistor based on one of a number of memory cells to be programmed and a number of cell groups including at least one memory cell to be programmed. The example method may include maintaining a source line voltage for a memory device at a substantially constant voltage level by scaling a boost voltage through control of a level of current flowing through a resistor coupled between a voltage comparator and the boost voltage based on one of a number of memory cells to be programmed in a memory operation and a number of cell groups including at least one memory cell to be programmed in a memory operation.

O at [0010]-[0012] and Fig. 1:

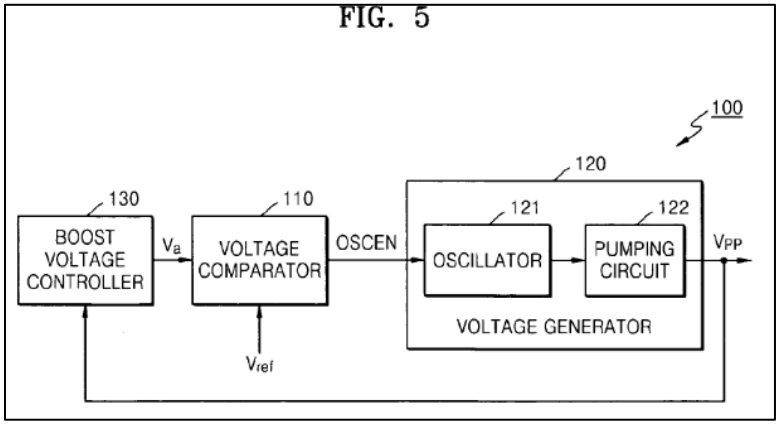
Referring to FIGS. 1A and 1B, if the boost voltage generating circuit 10 is used in a flash memory device, the boost voltage VPP and a first voltage (not shown) may be provided to a switch 20. The switch 20 may transfer a second voltage to a memory cell based on a memory operation mode (e.g., a reading mode, a programming mode, an erasing mode, etc.) of the flash memory device.

Referring to FIGS. 1A and 1B, the switch 20 may be a MOS transistor, and may have a resistive component if the MOS transistor is turned on. If the data signal set to the second logic level (e.g., a lower logic level or logic "0") is input to the memory cells, and a current flowing from the switch 20 via the memory cells increases, the boost voltage VPP may be reduced due to the MOS transistor of the switch 20. As a result, a source line voltage VSL applied to the memory cells may be less than the boost voltage VPP provided by the boost voltage generating circuit 10.



O at [0040] and Fig. 5:

FIG. 5 is a block diagram illustrating a boost voltage generating circuit 100 according to an example embodiment of the present invention. In the example embodiment of FIG. 5, the boost voltage generating circuit 100 may include a voltage comparator 110, a voltage generator 120 and a boost voltage controller 130. The voltage generator 120 may include an oscillator 121 and a pumping circuit 122.



Tanzawa-724 at Abstract:

There are provided a boosted voltage generating circuit and a semiconductor memory device having the boosted voltage generating circuit which includes a booster circuit for outputting high voltage obtained by boosting the power supply voltage, a regulator circuit supplied with the high voltage, for generating voltage whose voltage value is smaller than the value of the high voltage and which is variably set to at least two values based on the high voltage at the operating time, and a equalizer circuit connected to the booster circuit and regulator circuit, for short-circuiting an output node of the booster circuit and an output node of the regulator circuit in response to a first control signal, wherein the operative period of the regulator circuit and the short-circuiting operation period of the equalizer circuit do not overlap each other.

Tanzawa-724 at [0046]-[0048] and Fig. 4:

FIG. 4 shows the construction of a boosted voltage generating circuit of a semiconductor memory device disclosed in Jpn. Pat. Appln. KOKAI Publication No. 10-11987 in a block form. For example, the circuit shown in FIG. 4 is contained in a flash memory to generate various voltages applied to the control gate of the memory cell in various operation modes as described before. The boosted voltage generating circuit includes a booster circuit 11 and regulator circuit 12.

The booster circuit 11 is operated when a booster activation signal VPPE is activated and boosts power supply voltage Vcc supplied from the exterior to output voltage Vpp having a value larger than the power supply voltage. The voltage Vpp is supplied to the regulator circuit 12.

The regulator circuit 12 outputs voltage Vreg whose voltage value is smaller than Vpp and which is variably set to a plurality of values based on the voltage Vpp. The operation of the regulator circuit 12 is controlled according to a regulator activation signal REGE, a programming signal PROG activated at the program operation time of the memory cell, and a verifying signal VRFY activated at the program verify operation time of the memory cell.

Tanzawa-724 at [0110]-[0115] and Fig. 16:

FIG. 16 is a block diagram showing the whole construction of the memory when this invention is applied to a flash memory. An address buffer 41 receives an external address and outputs an internal address corresponding to a memory cell to be subjected to the readout process, program process or erase process. An I/O buffer 42 outputs data of a memory cell to be sensed by a sense amplifier 43 to the exterior at the readout time and inputs program data supplied from the exterior to a program circuit 44 at the program time. The program circuit 44 supplies program voltage to a corresponding one of bit lines in a memory cell array 46 via a column gate circuit 45.

A booster circuit 51 includes a charge pump circuit and the like, generates positive voltages Vpp, Vddp higher than the external power supply voltage by boosting or raising the external power supply voltage and generates 0V or negative voltage Vbb. The voltage Vddp generated from the booster circuit 51 is supplied to the program circuit 44. The voltage Vpp generated from the booster circuit 51 is supplied to the regulator circuit 12. The function of the regulator circuit 12 is the same as described before and the explanation thereof is omitted. The equalizer circuit 13 described before is connected between the booster circuit 51 and the regulator circuit 12. Also, the function of the equalizer circuit 13 is the same as described before and the explanation thereof is omitted.

In the flash memory with the above construction, since the voltage Vreg with various values to be supplied to the word line, that is, the control gate electrode of the memory cell at the program time or readout time of the memory cell is obtained by using voltage generated from one booster circuit (charge pump circuit) and changing the voltage to voltage having a plurality of values smaller than that of the above voltage by use of the regulator circuit 12, it becomes unnecessary to use a plurality of charge pump circuits. As a result, the whole area of the chip can be prevented from becoming large. In addition, since a relatively large current flows in the charge pump circuit and the consumption current is large, the whole consumption current can be reduced by reducing the number of charge pump circuits. The voltage Vreg is supplied to the word line WL of the memory cell array 46, that is, the control gate electrode of the memory cell via the row decoder 49.

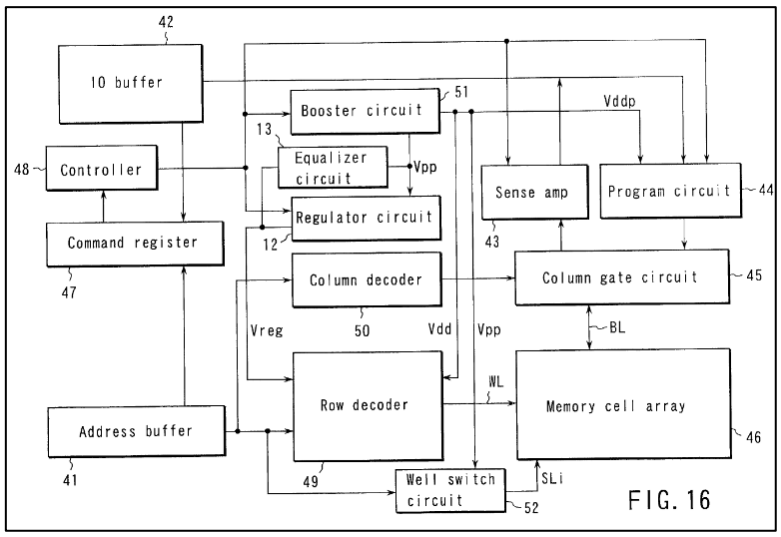


FIG. 16

Shibata at Abstract:

PROBLEM TO BE SOLVED: To set a negative threshold voltage in a memory cell due to stable operation. SOLUTION: In a memory cell array 1, a plurality of memory cells connected to a word line and a bit line are arranged in a matrix. The control circuit 7 controls the potentials of the word line and the bit line. The constant voltage generation circuit 71 generates the first voltage Vfix. When the plurality of first switches 61, 72, 73 perform a read operation from a memory cell connected to the first bit line of the bit lines, the second bit arranged adjacent to the first bit line is performed. The first voltage generated by the constant voltage generation circuit 71 is supplied to the line, the well on which the memory cell array is formed, and the source line of the memory cell array.

Shibata at [0009]:

According to a first aspect of the semiconductor memory device of the present invention, a memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, and the potentials of the word lines and bit lines are controlled. A control circuit; and a second bit line disposed adjacent to the first bit line when the control circuit performs a read operation from a memory cell connected to the first bit line of the bit lines. And supplying a first voltage to a well in which the memory cell array is formed and a source line of the memory cell array.

Shibata at [0017]-[0018]:

The word line control circuit 6 is connected to the memory cell array 1. The word line control circuit 6 selects a word line in the memory cell array 1 and applies a voltage necessary for reading, writing or erasing to the selected word line.

[Para 0018]

The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input / output buffer 4, and the word line control circuit 6 are connected to a control signal and control voltage

generation circuit 7, and the control signal and control voltage generation circuit 7 Be controlled. The control signal and control voltage generation circuit 7 is connected to the control signal input terminal 8 and is controlled by a control signal input from the outside via the control signal input terminal 8.

Shibata at Claims 1-2:

1. A memory cell array in which a plurality of memory cells connected to word lines and bit lines are arranged in a matrix, a control circuit that controls the potentials of the word lines and bit lines, and the control circuit includes: When a read operation is performed from a memory cell connected to the first bit line, a second bit line disposed adjacent to the first bit line, a well in which the memory cell array is formed, A semiconductor memory device, wherein a first voltage is supplied to a source line of a memory cell array.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one first switch connected between the constant voltage generation circuit and a source line of the memory cell array. The semiconductor memory device according to claim 1.

The control circuit includes a constant voltage generation circuit that generates the first voltage, and further includes at least one second switch connected between the constant voltage generation circuit and a well of the memory cell array. The semiconductor memory device according to claim 1.

2. The semiconductor memory device according to claim 1, further comprising at least one third switch connected to the source line and turned on during an erase operation and supplying an erase voltage to the source line and the well.

The semiconductor memory device according to claim 1, further comprising at least one fourth switch connected to the well and turned on during an erase operation and supplying an erase voltage to the source line and the well.

De Vita at Abstract:

***Abstract*— We present the design of a flash memory for passive RFID transponders, implemented in a standard – single poly - 0.35 µm CMOS process. The memory has 128 bits, sufficient for example to contain the EPC code for Class 0 tags, and is able to perform a complete read operation of all 128 bits with an access time of about 10 ms and a power consumption of only 160 nW. In the erase/program mode Fowler-Nordheim tunneling is used, and all 128 bits can be written in 0.8 s with a power consumption of about 3 µW. Such power causes an acceptable reduction of the operating range during a write operation to 1.74 m in the 2.45 GHz ISM band and 4.66 m in the UHF ISM band, for a transmitter EIRP of 500 mW, with respect to the read operating range, where 4 m at 2.45 GHz and 10.5 m at 916 MHz are achieved.**

De Vita at 3918:

III. MEMORY CELL

A nonvolatile memory can be realized in a standard CMOS process by realizing a floating node which preserves the stored charge [4,5]. In its simplest form, an EEPROM is a MOS transistor having a floating gate, as shown in Fig. 1. The capacitive divider consisting of the capacitance C, associated to the PMOS transistor, and of the gate capacitance C_g of the MOS

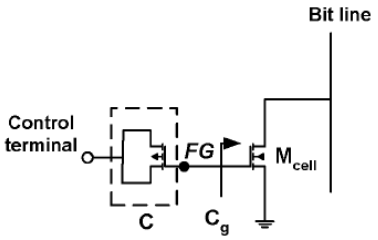


Figure 1. Circuit of the non-volatile memory cell.

transistor, transfers a large fraction of the voltage applied to the control terminal to the floating gate *FG*. Several methods exist to charge and discharge the floating node but we will limit our consideration to Fowler-Nordheim tunneling through the gate oxide of the NMOS transistor, in order to drastically reduce the power consumption during the write/erase operation. Fowler-Nordheim tunneling current was modeled by a WKB model [6],

In order to perform a write operation a high voltage is applied to the floating node through the capacitive divider and the bit line is grounded. In such a way a high voltage drops between the gate and the channel, giving rise to a tunneling current that charges the floating gate. In order to perform an erase operation the high voltage is applied to the drain of the NMOS transistor whereas the control terminal is grounded; therefore, the high voltage drops across the drain-gate terminals and a tunneling current discharges the floating node [4]. The charge in the *FG*

De Vita at 3919:

IV. MEMORY CIRCUITS

A. Sense Amplifier

As we have already mentioned, the very low supply voltage of 0.6 V requires us to implement the sense amplifier with low-voltage transistors and additional protection circuitry. The low V_{DD} leads us to prefer a current-mode sense amplifier, as shown in Fig. 3 [7] that also lets us to avoid the problem of the control of the bit line voltage biasing, which is not suitable for very low power supply. All transistors in Fig. 3 are low voltage transistors except for M_{n1} and M_{n2}, which are high voltage transistors: their use will be clarified later. During a read operation, the word line goes to the read voltage (0.6 V), the signal WE goes high, grounding the source of M_{cell}, the signal Y goes high so that the cell is selected. The current I_{cell} is injected into the current mirror and compared with the current I_{ref}, generated by biasing the reference cell with an appropriate voltage αV_{DD} ($0<\alpha<1$). As a consequence, if the selected cell is erased the current comparator compares I_{ref} with a larger current I_{cell} so that OUT goes to '1'; if the selected cell is written the current I_{cell} is much smaller than I_{ref} and then the OUT goes to '0'. The current I_{cell}, when the cell is erased, is set to only 6 nA leading to a static power during the read operation of only 0.36 nW per cell. If the cell is not selected, the pass gate is disabled and then the power consumption is zero. During an erase operation the word line is low, the signal WE is

De Vita at 3920:

B. Word Line Driver

The word line driver has to provide a signal ranging from zero to V_{DD}, during the read operation, and a signal that varies from 0 to V_{HIGH} during a program/erase operation. The word line driver is shown on the left side of Fig. 4. The two buffers are tri-state buffers. During a read operation the buffer in the upper branch is disabled and then its output is floating, while the low-voltage buffer and the pass-gate are enabled transferring the input signal to the output. During a program/erase operation the low-voltage buffer and the pass gate are disabled, while the high voltage buffer is enabled setting the output voltage to V_{HIGH} or zero, if the input voltage is V_{DD} or zero, respectively. While the low-voltage buffer is a standard tri-state buffer supplied by the read voltage (0.6 V), the high-voltage buffer has to be modified so that, during the read operation, when V_{HIGH} is zero or a very small non-regulated voltage, it ensures a floating output. Such behavior is obtained with the circuit shown in Fig. 4, on the right: it is a standard tri-state buffer implemented using high-voltage transistors, with the addition of the transistor M_{p1} and the V_{CC} generator, which ensure that the output is floating during a read

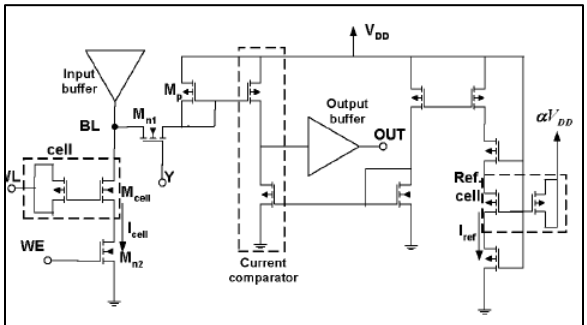


Figure 3. Current mode Sense Amplifier.

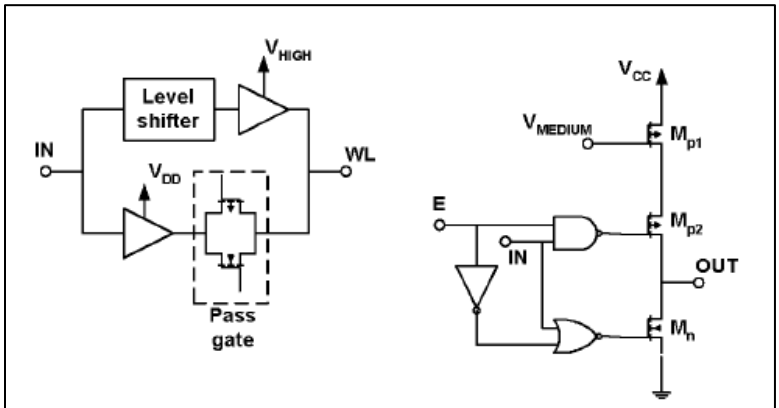


Figure 4. Left: word line driver; Right: high voltage tri-state buffer.

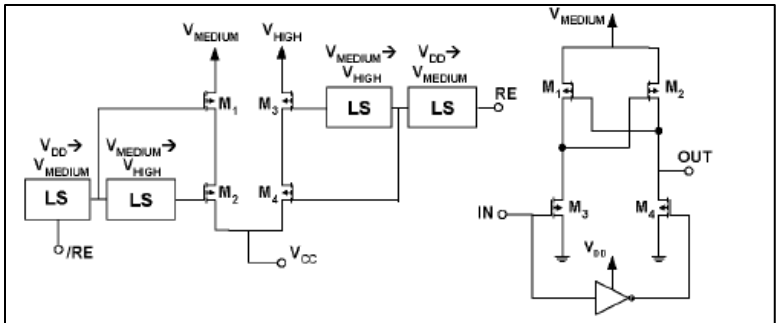


Figure 5. Left: Vcc generator; Right: circuit for the Level Shifter (LS).

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.d of its cover pleading.