

REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 085393-0241

Prior Application:

Art Unit: 2816

Examiner: JEFFERY SHAWN ZWEIZIG

BOX New Applications

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Commissioner for Patents

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Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application

No. 12/015,882, filed on January 17, 2008, entitled **BOOSTER CIRCUIT**, by the following named inventor(s):

Seiji YAMAHIRA.

1. ☒ I hereby state that the enclosed application contains no new matter.
2. Oath or Declaration
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ Deletion of inventor(s)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
3. ☒ Incorporation By Reference (useable if Box 2b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
4. ☒ Preliminary Amendment is enclosed.
5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.
6. ☒ Cancel claims 1-15.

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	12	-20	0	\$52.00	\$0.00
Independent Claims	2	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$270.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Total of Above Calculations					\$1,090.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,090.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.
9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of \$1,090.00.** Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.
10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. Not Yet Assigned or credit any overpayment to Deposit Account No. 500417.
11. ☒ Priority of Application Nos. 2007-007694, filed on January 17, 2007, and 2007-307064, filed on November 28, 2007, in Japan is claimed under 35 USC 119. The request to retrieve electronic priority documents were filed in Application No. 12/015,882 on January 17, 2008.
12. ☒ The prior application is assigned of record to
- PANASONIC CORPORATION**
Osaka, Japan
13. ☒ The power of attorney in the prior application is to:
- McDermott Will & Emery LLP
14. ☐ Also enclosed:

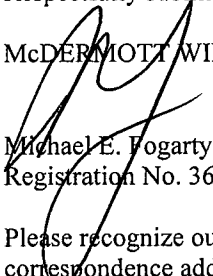
15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

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Respectfully submitted,

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BOOSTER CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a booster circuit employing a switching element having a triple-well structure.

2. Description of the Related Art

 In recent years, flash memories, which are a type of non-volatile semiconductor
10 memory devices, require data read and data write using a single power supply voltage or low power supply voltages, for which, therefore, a booster circuit for supplying a positive or negative boosted voltage is required on a chip when each operation is performed. Also, during CMOS processes, a power supply voltage generated by the booster circuit is used to improve characteristics of an analog circuit.

15 Conventionally, there is a known booster circuit employing a triple-well structure switching element (US Patent Nos. 6100557, 6121821, and 7102422).

 FIG. 25 shows an exemplary conventional booster circuit. In FIG. 25, 901 indicates a booster circuit which receives two-phase clock signals CLK1 and CLK2 and generates an output terminal voltage (boosted voltage) V_{pump} by a boosting operation.
20 902, 903, and 904 are boosting cells which constitute an exemplary three-stage configuration, where CLK1 is input to the odd-numbered-stage cells and CLK2 is input to the even-numbered-stage cell. 905 indicates a backflow preventing circuit which prevents backflow of the boosted voltage V_{pump} . 906 indicates a charge transfer transistor which functions as a switching element. 907 indicates a P well (PW) of the
25 charge transfer transistor 906. 908 indicates a deep N well (NT) including the P well 907. 909 indicates a parasitic diode between the P well 907 and the N well 908. 910 indicates boosting capacitors which boost output terminals of the boosting cells 902, 903, and 904.

911, 912, 913, and 914 indicate I/O terminals of the boosting cells. As shown in FIG. 25, the P well 907 and the N well 908 of each charge transfer transistor 906 of the boosting cells 902 to 904 is connected to the source of the charge transfer transistor 906 so that they have the same potential.

5 FIG. 26 is a waveform diagram showing the two-phase clock signals CLK1 and CLK2 in the booster circuit 901 of FIG. 25. An operation of the booster circuit 901 of FIG. 25 will be briefly described with reference to FIG. 26.

Initially, at time T1, CLK1 goes to "H" (power supply voltage Vdd) and CLK2 goes to "L" (ground voltage Vss), so that the potentials of the I/O terminals 912 and 914 are boosted. At the same time, charges are transferred from the I/O terminal 912 to the I/O terminal 913 and from the I/O terminal 914 to the output terminal of the booster circuit 901, via the charge transfer transistors 906 of the boosting cell 903 and the backflow preventing circuit 905, respectively, so that the output terminal voltages of the I/O terminal 913 and the booster circuit 901 are increased. In this case, since the P well 907 of each of the boosting cell 903 and the backflow preventing circuit 905 has the same potential as that of the source terminal of the charge transfer transistor 906, the substrate biasing effect of the charge transfer transistor 906 is suppressed, thereby making it possible to suppress a decrease in charge transfer efficiency.

At time T2 when a charge transfer period Ttrans has been passed since time T1, CLK2 goes to "H" and CLK1 goes to "L", so that the potential of the I/O terminal 913 is boosted. At the same time, charges are transferred from the I/O terminal 913 to the I/O terminal 914 via the charge transfer transistor 906 of the boosting cell 904. In this case, since the P well 907 of the boosting cell 904 has the same potential as that of the source terminal of the charge transfer transistor 906, the substrate biasing effect of the charge transfer transistor 906 is suppressed, thereby making it possible to suppress a decrease in charge transfer efficiency.

At time T3, an operation similar to that at time T1 is performed.

Thus, according to the booster circuit 901 of FIG. 25, the substrate biasing effect is suppressed, thereby making it possible to suppress a decrease in charge transfer efficiency during the boosting operation.

However, in the conventional booster circuit 901, the source and the N well 908 of the charge transfer transistor 906 are connected to each other, so that a parasitic capacitance formed by the N well 908 is charged and discharged by voltage transition widths of the clock signals CLK1 and CLK2 in response to voltage transitions of the clock signals CLK1 and CLK2.

Also, charges supplied by the clock signals CLK1 and CLK2 are used to charge and discharge the N well 908, disadvantageously resulting in a decrease in boost efficiency.

Also, since the source and the N well 908 of the charge transfer transistor 906 are connected to each other, it is necessary to separate the N wells 908 of the charge transfer transistors 906 from each other, disadvantageously resulting in an increase in layout area.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a booster circuit in which the current consumption and the layout area can be suppressed while the substrate biasing effect of a switching element used in each boosting cell can be suppressed.

To achieve the object, a booster circuit according to the present invention is provided in which the potential of an N well of each boosting cell is fixed to the input or output potential of the boosting cell stage to reduce the amount of charges which are charged and discharged between the N well and the substrate, thereby making it possible to improve the boost efficiency.

Specifically, in a first aspect, a boosting circuit comprises boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, in which the at least one switching element switches

ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, a first boosting cell row including N stages ($N \geq 1$) of the boosting cells, a second boosting cell row including M stages ($M \geq 1$) of the boosting cells, and at least one analog comparison circuit for outputting the higher or lower of an output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row. The output potential of the at least one analog comparison circuit is applied to the first well region of the at least one switching element included in the boosting cell on the (i+1)-th stage, the boosting cell on the i-th stage, or at least one of the boosting cells on less than i-th stages of the first and second boosting cell rows.

In a second aspect, a booster circuit comprises boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region, in which the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, a first boosting cell row including N stages ($N \geq 1$) of the boosting cells, a second boosting cell row including M stages ($M \geq 1$) of the boosting cells, and at least one analog comparison circuit for outputting the higher or lower of an input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row. The output potential of the at least one analog comparison circuit is applied to the first well region of the at least one switching element included in the boosting cell on the (i+1)-th stage, the boosting cell on the i-th stage, or at least one of the boosting cells on less than i-th stages of the first and second boosting cell rows.

In a third aspect, a booster circuit comprises boosting cells and backflow preventing circuits each having a first-conductivity type first well region on a substrate, a

second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the backflow preventing circuit, a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and the backflow preventing circuit, and at least one analog comparison circuit for outputting the higher or lower of an output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row. The output potential of the at least one analog comparison circuit is applied to the first well region of the at least one switching element included in the backflow preventing circuit, the boosting cell on the (i+1)-th stage, the boosting cell on the i-th stage, or at least one of the boosting cells on less than i-th stages of the first and second boosting cell rows.

In a fourth aspect, a booster circuit comprises boosting cells and backflow preventing circuits each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region, in which the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the backflow preventing circuit, a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and the backflow preventing circuit, and at least one analog comparison circuit for outputting the higher or lower of an intermediate potential of the backflow preventing circuit of the first boosting cell row and an intermediate potential of the backflow preventing circuit of the second boosting cell row. The output potential of the at least one analog comparison circuit is applied to the first well region of the at least

one switching element included in the backflow preventing circuit of the first and second boosting cell rows or at least one of the boosting cells of the first and second boosting cell rows.

In a fifth aspect, a booster circuit comprises boosting cells and backflow preventing circuits each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region, in which the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the backflow preventing circuit, a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and the backflow preventing circuit, and at least one analog comparison circuit for comparing input potentials of the boosting cells on the i -th stages ($1 \leq i \leq N$) of the first and second boosting cell rows or the backflow preventing circuits and outputting the higher or lower of the input potentials. The output potential of the at least one analog comparison circuit is applied to the first well region of the at least one switching element included in the backflow preventing circuit, the boosting cell on the $(i+1)$ -th stage, the boosting cell on the i -th stage, or at least one of the boosting cells on less than i -th stages of the first and second boosting cell rows.

In a sixth aspect, in the booster circuit of any one of the first to fifth aspects, the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.

In a seventh aspect, in the booster circuit of any one of the first to fifth aspects, the second well region and the first well region are connected to each other so that the second well region and the first well region have the same potential.

In an eighth aspect, in the booster circuit of any one of the first to fifth aspects, the at least one analog comparison circuit has a first-conductivity type first well region on the

substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and the at least one analog comparison circuit is provided one for each boosting cell stage.

5 In a ninth aspect, in the booster circuit of any one of the first to fifth aspects, the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and the at least one analog comparison circuit is provided one every arbitrary number of boosting cell stages.

10 In a tenth aspect, in the booster circuit of any one of the first to fifth aspects, a diode element is provided between the first terminal and the first well region of the boosting cell.

In an eleventh aspect, in the booster circuit of any one of the first to fifth aspects, the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region.

15 In a twelfth aspect, in the booster circuit of any one of the first to fifth aspects, the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least analog comparison circuit share a common first well region.

20 In a thirteenth aspect, in the booster circuit of any one of the first to fifth aspects, the at least one switching circuit of the boosting cell on the i -th stage of the first boosting cell row and a first element of the at least analog comparison circuit share a common first well region, and the at least one switching circuit of the boosting cell on the i -th stage of the second boosting cell row and a second element of the at least analog comparison circuit share a common first well region.

25 According to the first aspect, the amount of charges which are charged and discharged in the first-conductivity type first well region can be caused to be smaller than

the voltage swing of a clock signal, so that the apparent parasitic capacitance between the first well region and the substrate can be reduced. Thereby, it is possible to suppress current consumption during a boosting operation. Also, since the apparent parasitic capacitance between the first well region and the substrate can be reduced, boost efficiency
5 can be improved. Also, by controlling the potentials of the first well regions of a plurality of boosting cells using a single analog comparison circuit, it is possible to suppress an increase in layout area due to the analog comparison circuit.

According to the second aspect, a well control can be performed using the input potential of a boosting cell on the first stage, so that a load capacitance connected to a
10 boosting capacitor on each stage can be caused to be uniform. Thereby, a more stable boosting operation can be achieved.

According to the third aspect, the potential of the first well region of the backflow preventing circuit can be controlled, thereby making it possible to suppress a decrease in charge transfer efficiency of the backflow preventing circuit.

15 According to the fourth aspect, a well control can be performed using an intermediate potential of the backflow preventing circuit, so that a load capacitance connected to a boosting capacitor on each stage can be caused to be uniform. Thereby, a more stable boosting operation can be achieved.

According to the fifth aspect, a well control can be performed using the input
20 potential of a boosting cell on the first stage, so that a load capacitance connected to a boosting capacitor on each stage can be caused to be uniform. Thereby, a more stable boosting operation can be achieved.

According to the sixth aspect, the input terminal and the second well region of a charge transfer transistor (switching element) in the boosting cell can be connected to each
25 other, so that the current drive performance of a switching element can be suppressed from being decreased due to the substrate biasing effect.

According to the seventh aspect, the first well region and the second well region

are caused to have the same potential, so that a single well region can be shared by an N-channel transistor and a P-channel transistor, resulting in a decrease in layout area.

According to the eighth aspect, an analog comparison circuit is provided for each of all stages, so that the boosting cells can be caused to be of uniform parasitic capacitance,
5 thereby making it possible to improve easiness of design.

According to the ninth aspect, an analog comparison circuit is provided every arbitrary number of stages, so that an increase in circuit area can be suppressed while securing the margins of the breakdown voltages of the second well region and the first well region.

10 According to the tenth aspect, by supplying the input potential of a boosting cell to the first well region via a diode element, the potential increase of the first well region is caused to follow each boosting cell potential during start up of a booster circuit, thereby making it possible to prevent the occurrence of latch-up.

According to the eleventh and twelfth aspects, a common first well region is used,
15 thereby making it possible to reduce the layout area.

According to the thirteenth aspect, noise interference between the first boosting cell row and the second boosting cell row which is pumped with clocks having different phases can be reduced while reducing the amount of charges which are charged and discharged of the first well region.

20

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram showing an exemplary configuration of a booster circuit according to the present invention.

FIG. 2 is a circuit diagram showing another exemplary configuration of a booster
25 circuit according to the present invention.

FIG. 3 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 4 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 5 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

5 FIG. 6 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 7 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

10 FIG. 8 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 9 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 10 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

15 FIG. 11 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 12 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

20 FIG. 13 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 14 is a circuit diagram showing still another exemplary configuration of the booster circuit of the present invention.

FIG. 15 is a plan view showing an exemplary layout configuration of the booster circuit of the present invention.

25 FIG. 16 is a plan view showing another exemplary layout configuration of the booster circuit of the present invention.

FIG. 17 is a plan view showing still another exemplary layout configuration of the

booster circuit of the present invention.

FIG. 18 is a plan view showing still another exemplary layout configuration of the booster circuit of the present invention.

FIG. 19 is a plan view showing still another exemplary layout configuration of the
5 booster circuit of the present invention.

FIG. 20 is a plan view showing still another exemplary layout configuration of the booster circuit of the present invention.

FIG. 21 is a plan view showing still another exemplary layout configuration of the booster circuit of the present invention.

10 FIG. 22 is a plan view showing still another exemplary layout configuration of the booster circuit of the present invention.

FIG. 23 is a plan view showing still another exemplary layout configuration of the booster circuit of the present invention.

FIG. 24 is a plan view showing still another exemplary layout configuration of the
15 booster circuit of the present invention.

FIG. 25 is a circuit diagram showing a conventional booster circuit.

FIG. 26 is a waveform diagram showing a two-phase clock signal in the booster circuit of FIG. 25.

20 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a booster circuit according to the present invention will be described, by way of examples, with reference to the accompanying drawings.

FIG. 1 shows an exemplary configuration of the booster circuit of the present invention. In FIG. 1, 101 indicates a two-parallel booster circuit which receives two-
25 phase clock signals CLK1 and CLK2 and generates an output terminal voltage (boosted voltage) V_{pump} by a boosting operation. 102, 103, 104, 105, 106, and 107 indicate boosting cells which are arranged in a first line and a second line, where CLK1 is input to

the odd-numbered stages on the first line and the even-numbered stages on the second line, and CLK2 is input to the even-numbered stages on the first line and the odd-numbered stages on the second line. 108 and 109 indicate backflow preventing circuits which prevent backflow of the boosted voltage V_{pump} . 110, 111, 112, 113, 114, 115, and 116 indicate I/O terminals of the boosting cells 102 to 107. 117, 118, and 119 indicate exemplary low-voltage output analog comparison circuits which output the lower of the voltages of the I/O terminals of the boosting cells on the same stage of the first line and the second line. 120 and 121 indicate Nch (N-channel) transistors included in the low-voltage output analog comparison circuits 117, 118, and 119. 122, 123, and 124 indicate output terminals of the low-voltage output analog comparison circuits 117 to 119 connected to N wells of the corresponding boosting cells. 125 indicates a high-voltage output analog comparison circuit which outputs the higher of the voltages of the I/O terminal 113 of the third-stage boosting cell 104 on the first line and the I/O terminal 116 of the third-stage boosting cell 107 on the second line. 126 and 127 indicate Pch (P-channel) transistors included in the high-voltage output analog comparison circuit 125. 128 indicates an output terminal of the high-voltage output analog comparison circuit connected to N wells of the backflow preventing circuits 108 and 109. Note that the same elements as those of the above-described conventional example are indicated by the same reference numerals. Also, the number of boosting cells connected in series in the booster circuit 101 shown in FIG. 1 is only for illustrative purposes.

The two-phase clock signals CLK1 and CLK2 of the booster circuit 101 of FIG. 1 have waveforms similar to those of FIG. 26. An operation of the booster circuit 101 of FIG. 1 will be described with reference to FIG. 26.

At time T1, CLK1 goes from "L" to "H" and CLK2 goes from "H" to "L", so that the potentials of the I/O terminals 111, 113, and 115 of the boosting cells 102, 104, and 106 are boosted, and the boosted charges are transferred via the charge transfer transistors 906 of the boosting cell 103, the backflow preventing circuit 108, and the boosting cell 107

to the I/O terminal 112, the output terminal of the booster circuit 101, and the I/O terminal 116, respectively. In this case, in the low-voltage output analog comparison circuit 117, the Nch transistor 120 is switched OFF and the Nch transistor 121 is switched ON due to a relationship in potential between the boosted I/O terminal 111 and the non-boosted I/O terminal 114, so that the potential of the I/O terminal 114 is output from the output terminal 122 of the low-voltage output analog comparison circuit 117 and is supplied to the N wells of the boosting cell 102 and the boosting cell 105. Similarly, the potential of the I/O terminal 112 is output from the output terminal 123 of the low-voltage output analog comparison circuit 118 and is supplied to the N wells of the boosting cell 103 and the boosting cell 106. The potential of the I/O terminal 116 is output from the output terminal 124 of the low-voltage output analog comparison circuit 119 and is supplied to the N wells of the boosting cells 104 and the boosting cell 107. Also, in the high-voltage output analog comparison circuit 125, the Pch transistor 126 is switched ON and the Pch transistor 127 is switched OFF due to a relationship in potential between the boosted I/O terminal 113 and the non-boosted I/O terminal 116, so that the potential of the I/O terminal 113 is output from the output terminal 128 of the high-voltage output analog comparison circuit 125 and is supplied to the N wells of the backflow preventing circuit 108 and the backflow preventing circuit 109.

At time T2, if CLK1 goes from "H" to "L" and CLK2 goes from "L" to "H", the potentials of the I/O terminals 112, 114, and 116 of the boosting cells 103, 105, and 107 are boosted, and boosted charges are transferred via the charge transfer transistors 906 of the boosting cells 104 and 106 and the backflow preventing circuit 109 to the output terminals of the I/O terminals 113 and 115 and the booster circuit 101, respectively. In this case, in the low-voltage output analog comparison circuit 117, the Nch transistor 120 is switched ON and the Nch transistor 121 is switched OFF due to a relationship in potential between the boosted I/O terminal 114 and the non-boosted I/O terminal 111, so that the potential of the I/O terminal 111 is output from the output terminal 122 of the low-

voltage output analog comparison circuit 117 and is supplied to the N wells of the boosting cell 102 and the boosting cell 105. Similarly, the potential of the I/O terminal 115 is output from the output terminal 123 of the low-voltage output analog comparison circuit 118 and is supplied to the N wells of the boosting cell 103 and the boosting cell 106. The
5 potential of the I/O terminal 113 is output from the output terminal 124 of the low-voltage output analog comparison circuit 119 and is supplied to the N wells of the boosting cell 104 and the boosting cell 107. Also, in the high-voltage output analog comparison circuit 125, the Pch transistor 126 is switched OFF and the Pch transistor 127 is switched ON due to a relationship in potential between the boosted I/O terminal 116 and the non-boosted I/O
10 terminal 113, so that the potential of the I/O terminal 116 is output from the output terminal 128 of the high-voltage output analog comparison circuit 125 and is supplied to the N wells of the backflow preventing circuit 108 and the backflow preventing circuit 109.

Thus, according to the booster circuit 101 of FIG. 1, the potentials of the N wells of the boosting cells 102 to 107 and the backflow preventing circuits 108 and 109 can be
15 fixed to the input potentials or the output potentials of the respective boosting cell stage, so that the amount of charges which are charged and discharged between the N well and the substrate can be reduced, i.e., current consumption can be reduced. Also, by reducing the amount of charges which are charged and discharged between the N well and the substrate, the amount of charges transferred to the next stage can be increased, so that an
20 improvement in boost efficiency can be expected.

Note that, as shown in FIGS. 2 and 3, the low-voltage output analog comparison circuits 117 to 119 and the high-voltage output analog comparison circuit 125 can be provided every arbitrary number of stages of boosting cells, taking into consideration the margin of the breakdown voltage between the P well and the N well and the circuit area, so
25 that an effect similar to that of the above-described configuration can be obtained with a reduced number of elements.

FIG. 4 shows another exemplary configuration of the booster circuit of the present

invention. In FIG. 4, 701 indicates a two-parallel booster circuit which receives two-phase clock signals CLK1 and CLK2, and generates a boosted voltage V_{pump} by a boosting operation. 702, 703, 704, 705, 706, and 707 indicate the boosting cells 102 to 107 of FIG. 1, respectively, in each of which a transistor 710 diode-connected between the I/O terminal of the boosting cell and the output terminal 128 of the high-voltage output analog comparison circuit 125 is added. 708 and 709 indicate backflow preventing circuits. Note that elements similar to those of FIG. 1 are indicated by the same reference numerals. The number of boosting cells connected in series in the booster circuit 701 is only for illustrative purposes.

10 The configuration of FIG. 4 is different from that of FIG. 1 in that the low- (or high-) voltage output analog comparison circuits 117 to 119 and 125 are replaced with a single common element, thereby reducing the number of elements. Thereby, during startup of the booster circuit 701, when the potentials of the I/O terminals 111 to 116 of the boosting cells 702 to 707 increase, the N well potential is supplied as a forward current of the parasitic diode 909 from the P well 907 of each of the boosting cells 702 to 707. To suppress the forward current of the parasitic diode 909, the transistor 710 having a diode function is provided, thereby making it possible to provide a stable boosting operation even during startup of the booster circuit 701.

FIG. 5 shows still another exemplary configuration of the booster circuit of the present invention. In FIG. 5, 621 indicates a two-parallel booster circuit which receives two-phase clock signals CLK1 and CLK2, and generates a boosted voltage V_{pump} by a boosting operation. 858 and 859 indicate backflow preventing circuits in which two-phase clock signals CLK1 and CLK2 are input and transistors 861 and 862 therein are controlled to cause a charge transfer transistor 860 to be in a conductive or non-conductive state. Thereby, a decrease in transfer efficiency occurring in the backflow preventing circuits 108 and 109 of FIG. 1 is suppressed. Note that elements similar to those of FIG. 1 are indicated by the same reference numerals. The number of boosting cells connected

in series in the booster circuit 621 is only for illustrative purposes.

The configuration of FIG. 5 is different from that of FIG. 5 in that the two-phase clock signals CLK1 and CLK2 are input to control the gate potential of the charge transfer transistor 860, and a low-voltage output analog comparison circuit 501 is used for the
5 backflow preventing circuits 858 and 859 for improving charge transfer efficiency and boost efficiency.

According to FIG. 5, the low-voltage output analog comparison circuits 117, 118, 119, and 501 having a similar structure are provided on the respective stages in the booster circuit 621, so that a difference between the loads of the boosting capacitors 910 of the
10 boosting cells 104 and 107 on the final stage of FIG. 1 and the loads of the boosting capacitors 910 of the other boosting cells 102, 103, 105, and 106 can be suppressed, thereby making it possible to cause the boosting capacitors 910 on the stages to be of substantially uniform parasitic capacitance. Therefore, the boosting cells on the stages are caused to be of uniform charge transfer amount, resulting in a stable boosting operation.

Note that a booster circuit 622 of FIG. 6 is an example in which high-voltage output analog comparison circuits 511, 512, 513, and 125 are used for the boosting cells
15 102 to 107 and the backflow preventing circuits 108 and 109 of FIG. 1, and only the gates of the transistors 126 and 127 of the high-voltage output analog comparison circuit 511 which controls the N wells of the boosting cells 102 and 105 on the first stage are fixed to
20 VSS. Thereby, a stable boosting operation can be achieved as in FIG. 5.

Thus, the booster circuits employing the two-phase clock signals CLK1 and CLK2 have been described as exemplary booster circuit configurations. Alternatively, as shown in FIG. 7, a booster circuit 801 may employ four-phase clock signals CLK1, CLK2, CLK3, and CLK4. Alternatively, as shown in FIGS. 8, 9, 10, and 11, booster circuit 851,
25 881, 601, and 611 may employ two-phase clock signals CLK1 and CLK2, and Nch transistors having triple wells in boosting cells, where the low-voltage output analog comparison circuits 117 to 119, and 501 or the high-voltage output analog comparison

circuits 511 to 513 and 125 are used, thereby making it possible to a similar effect irrespective of the configuration of the boosting cell. Also, as shown in FIG. 11, the P and N wells of an Nch transistor 612 of each of boosting cells 602 to 607 can be commonly connected, and further, the P and N wells of an Nch transistor 612 and the N well of the Pch transistor 611 can be commonly connected, thereby making it possible to reduce the layout area.

Note that, in FIG. 7, 802, 803, 804, 805, 806, and 807 indicate boosting cells, 808 and 809 indicate backflow preventing circuits, 810 indicates a charge transfer transistor (Nch transistor), 811 and 813 indicates Nch transistors, and 812 indicates a boosting capacitor. In FIG. 8, 852, 853, 854, 855, 856, and 857 indicate boosting cells, 858 and 859 indicate backflow preventing circuits, 860 indicates a charge transfer transistor (Nch transistor), 861 and 863 indicate Nch transistors, and 862 indicates a Pch transistor. In FIGS. 10 and 11, 602, 603, 604, 605, 606, and 607 indicate boosting cells, 608 and 609 indicate backflow preventing circuits, 610 and 612 indicate charge transfer transistors (Nch transistors), 611 and 614 indicate charge transfer transistors (Pch transistors), and 613 indicates a connection node.

FIGS. 12, 13, and 14 show exemplary configurations including high-voltage (low-voltage) output analog comparison circuits, where either or both high- and low-voltage output analog comparison circuits can be used for all boosting cells and a backflow preventing circuit. If a boosting operation can be operated irrespective of the number of transistors (charge transfer transistors in the N wells of boosting cells, etc.) or the presence or absence of a Pch transistor and even when the P well is not necessarily connected directly to the source (e.g., the P well of the Nch transistor in a charge transfer transistor or the like is connected to the N well, the potential of the P well is supplied by switching the potentials of the drain and the source, etc.), a similar effect can be achieved.

The configuration of the low-voltage output analog comparison circuits 117 to 119 and 501 and the high-voltage output analog comparison circuits 511, 512, 513, and 125 in

the figures is only for illustrative purposes, and any other configurations that provide similar functions may be provided.

FIG. 15 is a plan view showing an exemplary layout configuration of booster circuits according to the present invention, indicating the charge transfer transistors 906 of the boosting cells 102 to 107 and the low-voltage output analog comparison circuits 117 to 119 of FIG. 1.

In FIG. 15, the output terminal 122 (or 123, 124) of the low-voltage output analog comparison circuit 117 (or 118, 119) is connected to a single N well (NT) which is shared by the charge transfer transistors 906 of the boosting cells 102 and 105 (or 103 and 106, 104 and 107).

According to FIG. 15, a single N well can be shared by the triple-well structure switching elements 906 of the two or more boosting cells 102 and 105 controlled by the output voltage of the low-voltage output analog comparison circuit 117, thereby making it possible to reduce the layout area.

Note that the layout configuration of FIG. 15 is only for illustrative purposes. Alternatively, as shown in FIGS. 16 and 17, the N well of the switching element 906 which is controlled by the output voltage of the low-voltage output analog comparison circuit 118 can be separated or shared irrespective of the number of stages of boosting cells.

Further, as shown in FIGS. 18 and 19, a single N well can be shared by the low-voltage output analog comparison circuits 117 to 119u and the switching elements 906 of the boosting cells 102 to 107, respectively.

As shown in FIGS. 20 and 21, a single N well is shared by the transistors 120 of the single low-voltage output analog comparison circuits 117, 118, 119, and 501, and the boosting cells 102, 103, and 104 and the backflow preventing circuit 108, and another single N well is shared by the transistors 121 of the low-voltage output analog comparison circuits 117, 118, 119, and 501, and the boosting cells 105, 106, and 107 and the backflow preventing circuit 109. Thereby, the influence of noise in the boosting capacitor can be

reduced while decreasing the amount of charges which are charged and discharged of the N well, thereby making it possible to achieve a stable boosting operation.

A similar layout can be applied to the high-voltage output analog comparison circuits 511, 512, 513, and 125 as shown in FIGS. 22, 23, and 24.

5 The above-described layout is only for illustrative purposes. A plurality of transistors having the same potential can share a single N or P well irrespective of the boosting cell row.

Further, in each of the above aspects, the output voltage generated by the analog comparison circuit in the boosting cell on the i -th stage can be applied to the N well of any
10 of the boosting cells on the $(i+1)$ -th stage, i -th stage, and stages anterior the i -th stage in the booster circuit in the N -th row other than the booster circuits in the first and second rows. This achieves not only reduction in area of the analog comparison circuit but also layout sharing to thus reduce the layout area.

As described above, in the booster circuit of the present invention, the substrate
15 biasing effect can be suppressed in the triple-well structure element included in each boosting cell, so that the current consumption, the circuit area, and the layout area can be reduced. Therefore, the booster circuit of the present invention is useful as a power supply generating circuit or the like for improving analog circuit characteristics in a non-volatile semiconductor memory device and a CMOS process.

20 Also, the booster circuit of the present invention is applicable to power supply circuits for a volatile semiconductor memory device (DRAM, etc.), a liquid crystal device, a mobile device, and the like.

WHAT IS CLAIMED IS:

1. A booster circuit comprising:

boosting cells each having a first-conductivity type first well region on a substrate,
5 a second-conductivity type second well region in the first well region, and at least one
switching element in either or both of the first well region and the second well region,
wherein the at least one switching element switches ON/OFF a connection between a first
terminal and a second terminal so as to transfer charges from the first terminal to the
second terminal;

10 a first boosting cell row including N stages ($N \geq 1$) of the boosting cells;
a second boosting cell row including M stages ($M \geq 1$) of the boosting cells; and
at least one analog comparison circuit for outputting the higher or lower of an
output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell
row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second
15 boosting cell row,

wherein the output potential of the at least analog comparison circuit is applied to
the first well region of the at least one switching element included in the boosting cell on
the $(i+1)$ -th stage, the boosting cell on the i -th stage, or at least one of the boosting cells on
less than i -th stages of the first and second boosting cell rows.

20

2. A booster circuit comprising:

boosting cells each having a first-conductivity type first well region on a substrate,
a second-conductivity type second well region in the first well region, and at least one
switching element in either or both of the first well region and the second well region,
25 wherein the at least one switching element switches ON/OFF a connection between a first
terminal and a second terminal so as to transfer charges from the first terminal to the
second terminal;

a first boosting cell row including N stages ($N \geq 1$) of the boosting cells;
a second boosting cell row including M stages ($M \geq 1$) of the boosting cells; and
at least one analog comparison circuit for outputting the higher or lower of an
input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row
5 and an input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second
boosting cell row,

wherein the output potential of the at least analog comparison circuit is applied to
the first well region of the at least one switching element included in the boosting cell on
the $(i+1)$ -th stage, the boosting cell on the i -th stage, or at least one of the boosting cells on
10 less than i -th stages of the first and second boosting cell rows.

3. A booster circuit comprising:

boosting cells and backflow preventing circuits each having a first-conductivity
type first well region on a substrate, a second-conductivity type second well region in the
15 first well region, and at least one switching element in either or both of the first well region
and the second well region, wherein the at least one switching element switches ON/OFF a
connection between a first terminal and a second terminal so as to transfer charges from
the first terminal to the second terminal;

a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the
20 backflow preventing circuit;

a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and
the backflow preventing circuit; and

at least one analog comparison circuit for outputting the higher or lower of an
output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell
25 row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second
boosting cell row,

wherein the output potential of the at least analog comparison circuit is applied to

the first well region of the at least one switching element included in the backflow preventing circuit, the boosting cell on the (i+1)-th stage, the boosting cell on the i-th stage, or at least one of the boosting cells on less than i-th stages of the first and second boosting cell rows.

5

4. A booster circuit comprising:

boosting cells and backflow preventing circuits each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;

a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the backflow preventing circuit;

15 a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and the backflow preventing circuit; and

an at least one analog comparison circuit for outputting the higher or lower of an intermediate potential of the backflow preventing circuit of the first boosting cell row and an intermediate potential of the backflow preventing circuit of the second boosting cell row,

20 wherein the output potential of the at least analog comparison circuit is applied to the first well region of the at least one switching element included in the backflow preventing circuit of the first and second boosting cell rows or at least one of the boosting cells of the first and second boosting cell rows.

25

5. A booster circuit comprising:

boosting cells and backflow preventing circuits each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the

first well region, and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;

5 a first boosting cell row including N stages ($N \geq 1$) of the boosting cells and the backflow preventing circuit;

 a second boosting cell row including M stages ($M \geq 1$) of the boosting cells and the backflow preventing circuit; and

 at least one analog comparison circuit for comparing input potentials of the
10 boosting cells on the i-th stages ($1 \leq i \leq N$) of the first and second boosting cell rows or the backflow preventing circuits and outputting the higher or lower of the input potentials,

 wherein the output potential of the at least analog comparison circuit is applied to the first well region of the at least one switching element included in the backflow preventing circuit, the boosting cell on the (i+1)-th stage, the boosting cell on the i-th stage,
15 or at least one of the boosting cells on less than i-th stages of the first and second boosting cell rows.

6. The booster circuit of any one of claims 1 to 5, wherein
 the second well region and the first terminal are connected to each other so that the
20 second well region and the first terminal have the same potential.

7. The booster circuit of any one of claims 1 to 5, wherein
 the second well region and the first well region are connected to each other so that
the second well region and the first well region have the same potential.

25

8. The booster circuit of any one of claims 1 to 5, wherein
 the at least analog comparison circuit has a first-conductivity type first well region

on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

the at least analog comparison circuit is provided one for each boosting cell stage.

5 9. The booster circuit of any one of claims 1 to 5, wherein

the at least analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and at least one analog comparison circuit is provided for the first and second boosting cell rows, and

10 the at least analog comparison circuit is provided one every arbitrary number of boosting cell stages.

10. The booster circuit of any one of claims 1 to 5, wherein

a diode element is provided between the first terminal and the first well region of
15 the boosting cell.

11. The booster circuit of any one of claims 1 to 5, wherein

the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region.

20

12. The booster circuit of any one of claims 1 to 5, wherein

the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region.

25

13. The booster circuit of any one of claims 1 to 5, wherein

the at least one switching circuit of the boosting cell on the i-th stage of the first

boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

the at least one switching circuit of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share
5 a common first well region.

14. A booster circuit comprising:

boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one
10 switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;

a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and

15 a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;

wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.

20

15. The booster circuit of any one of claims 1 to 5 and 14,

wherein an output potential of the analog comparison circuit is applied to the first well region of the at least one switching element included in a boosting cell of a boosting cell row different from the first and second boosting cell rows.

25

ABSTRACT OF THE DISCLOSURE

A boosting circuit comprises a first boosting cell row and a second boosting cell row. The boosting circuit further comprises an analog comparison circuit for comparing
5 the potential of boosting cells on the same stage, and selecting and outputting the lower or higher of the potentials. The potential of an N well is controlled using the output potential of the analog comparison circuit. Thereby, the amplitude of an N well potential can be suppressed, and a single N well region can be shared.

FIG. 1

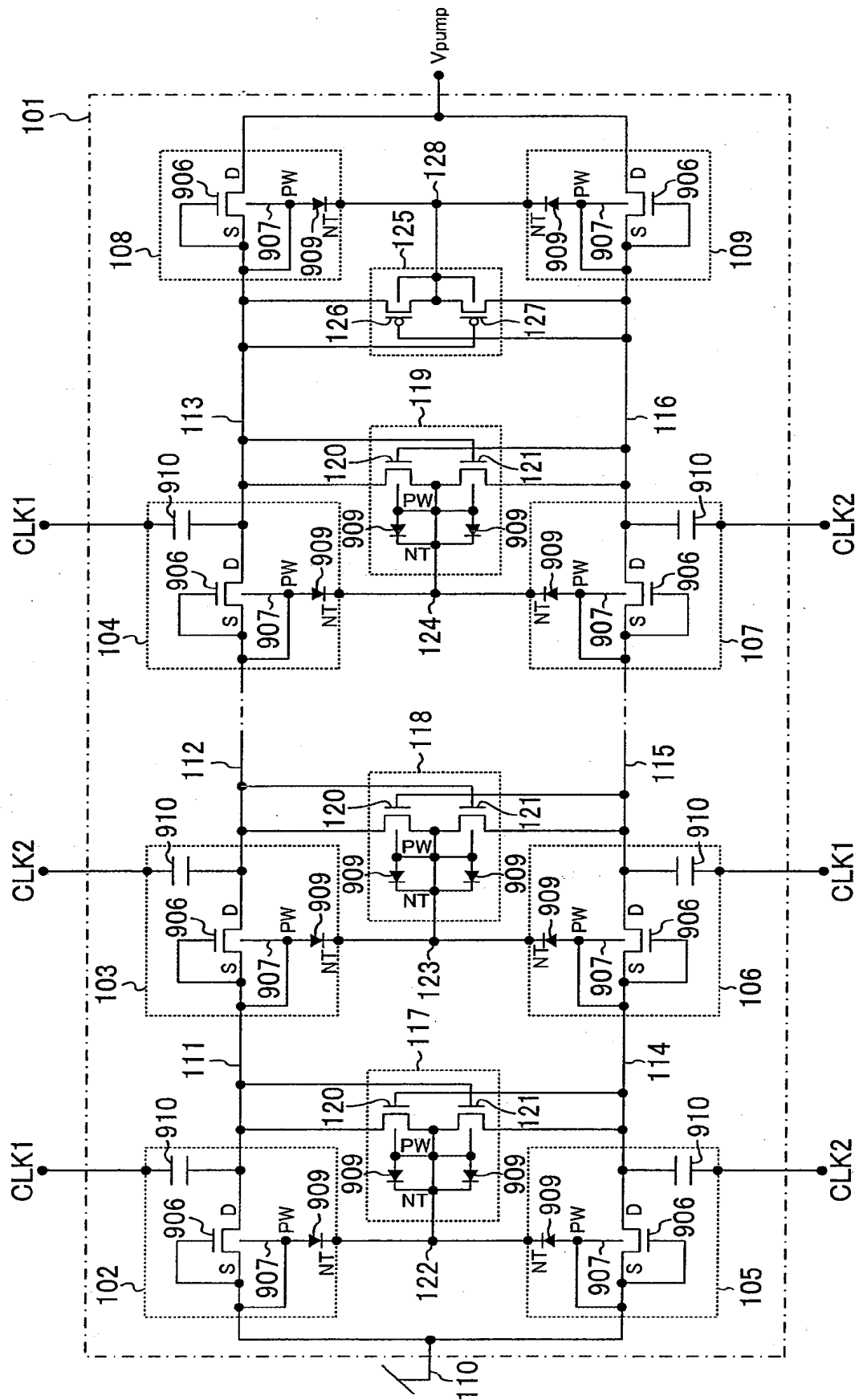


FIG. 2

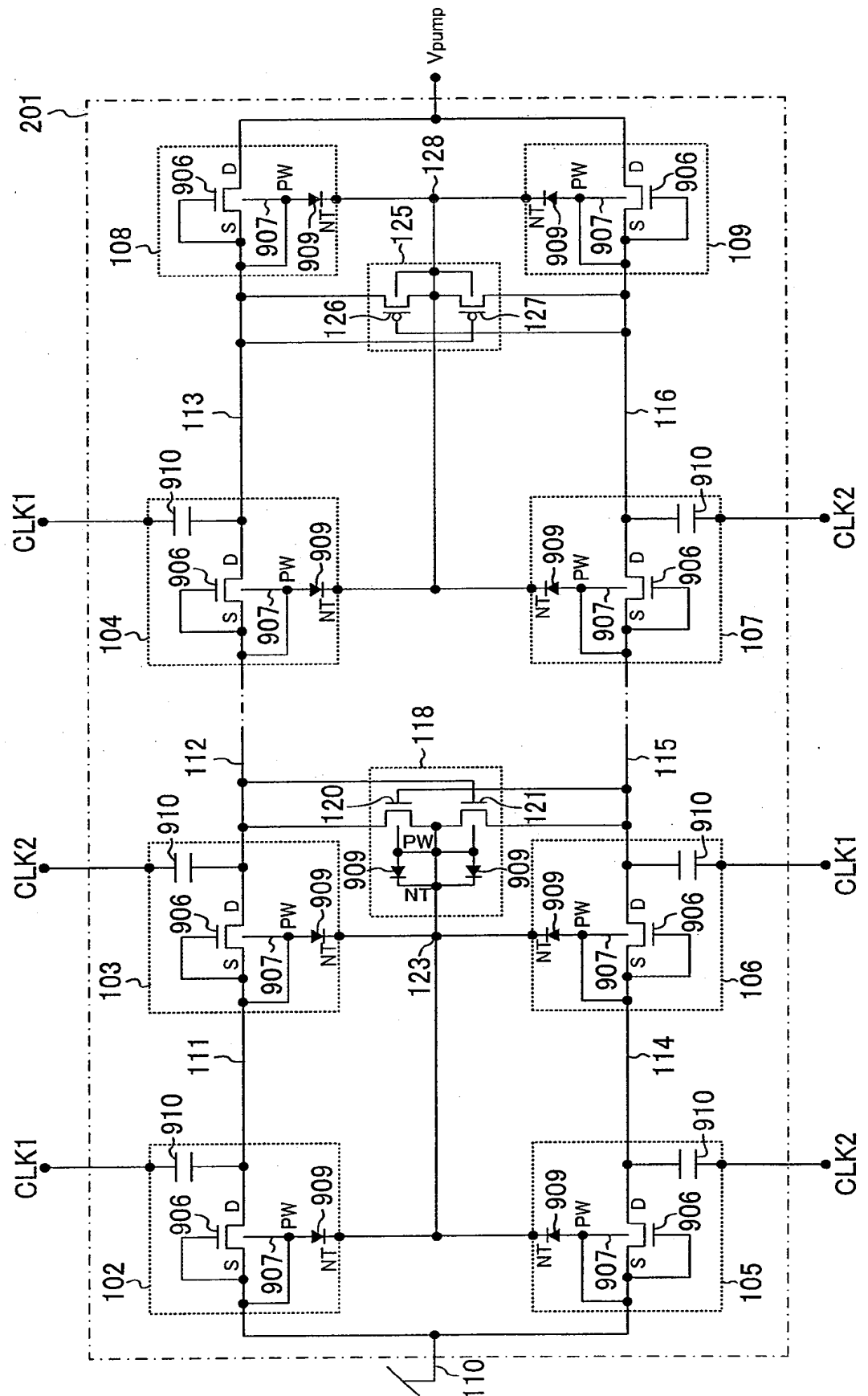


FIG. 3

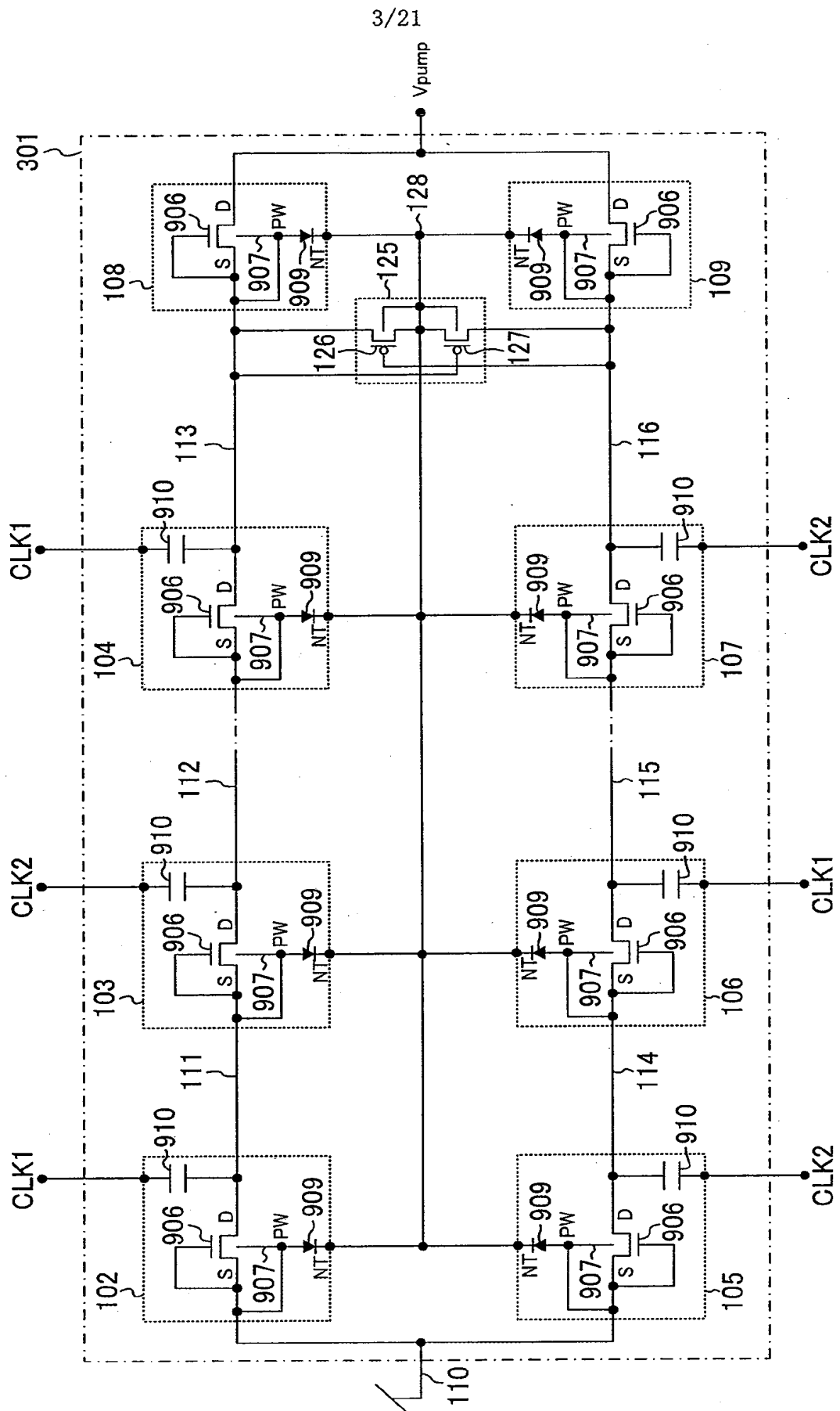


FIG. 4

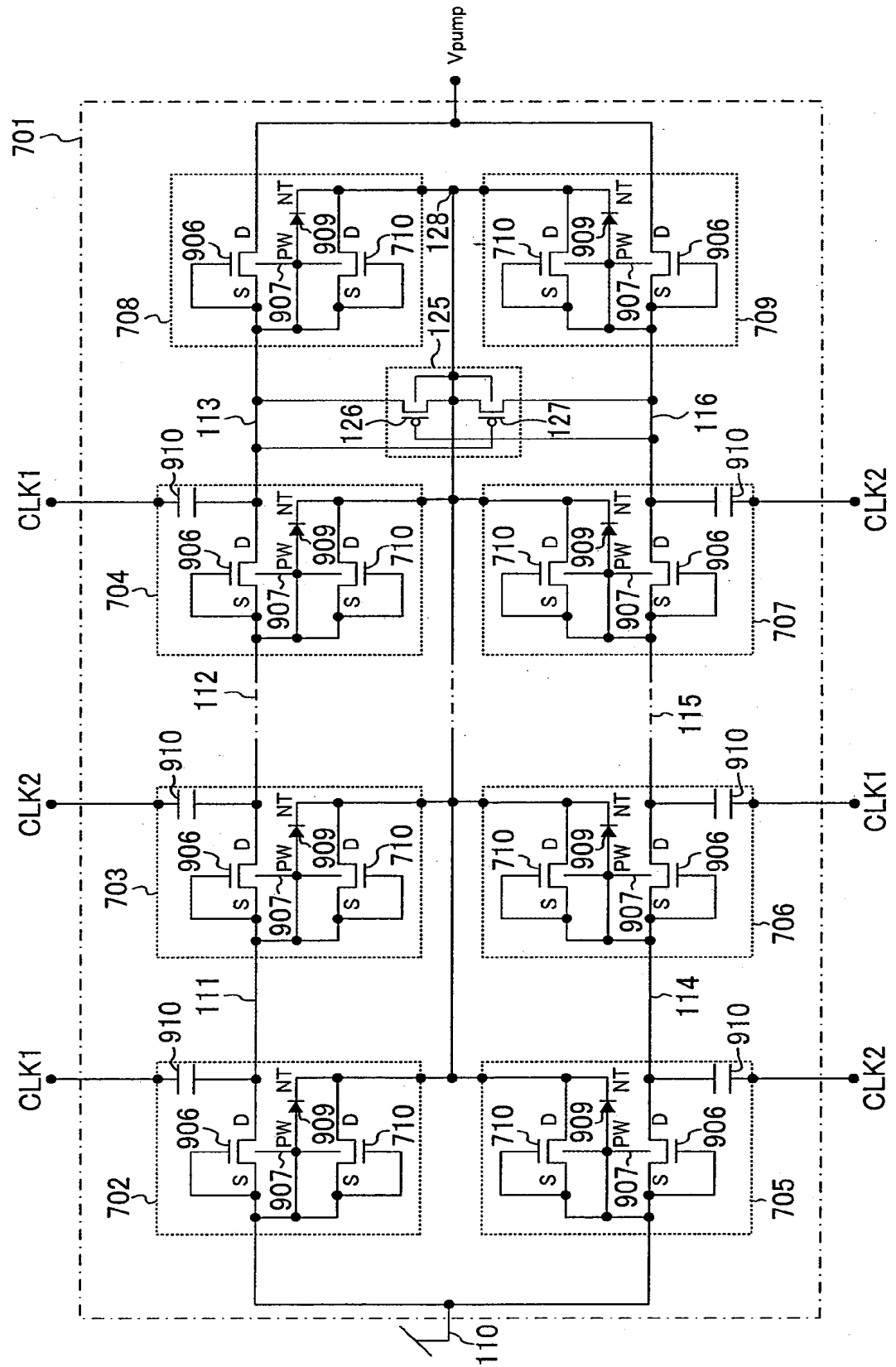


FIG. 5

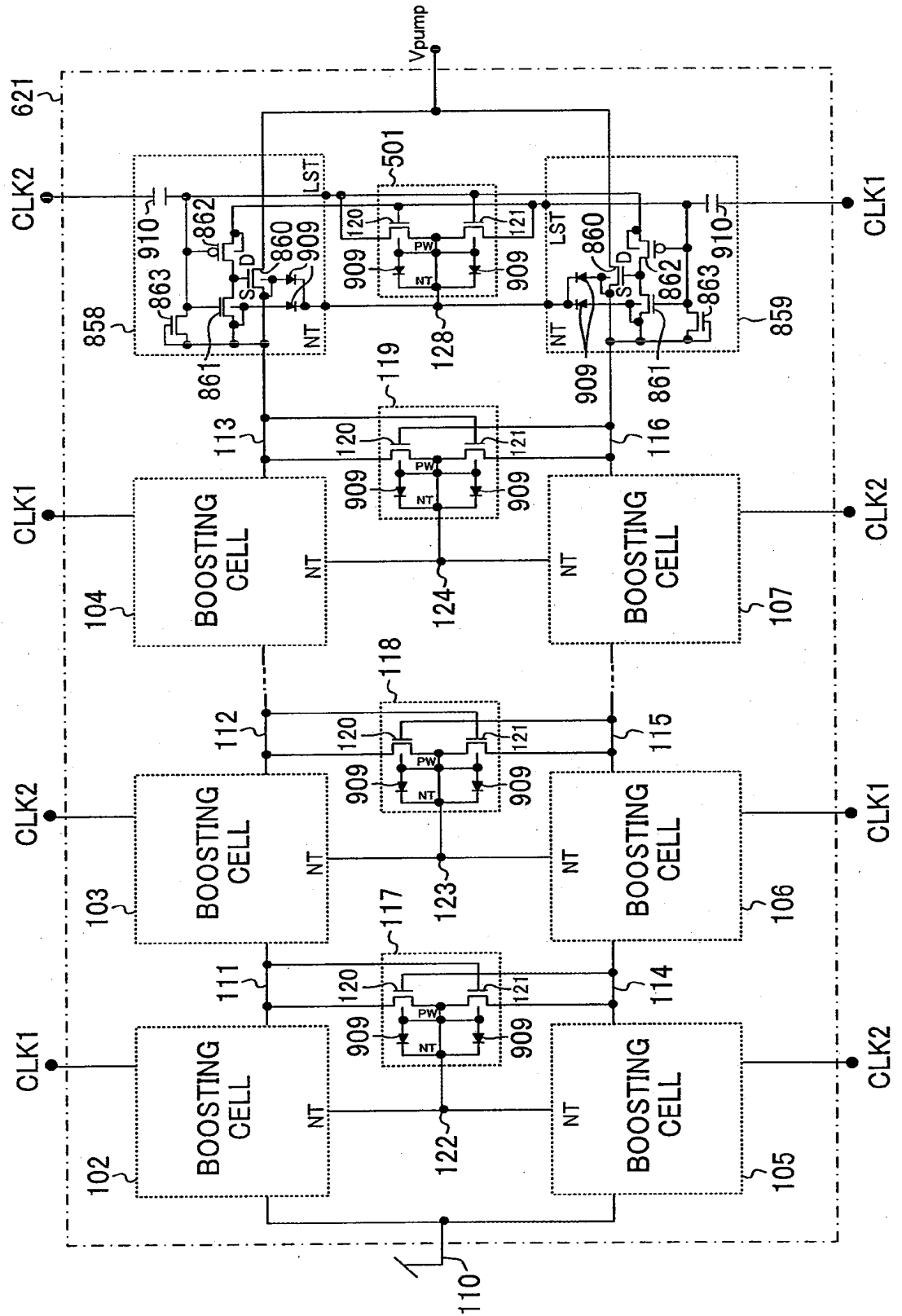


FIG. 6

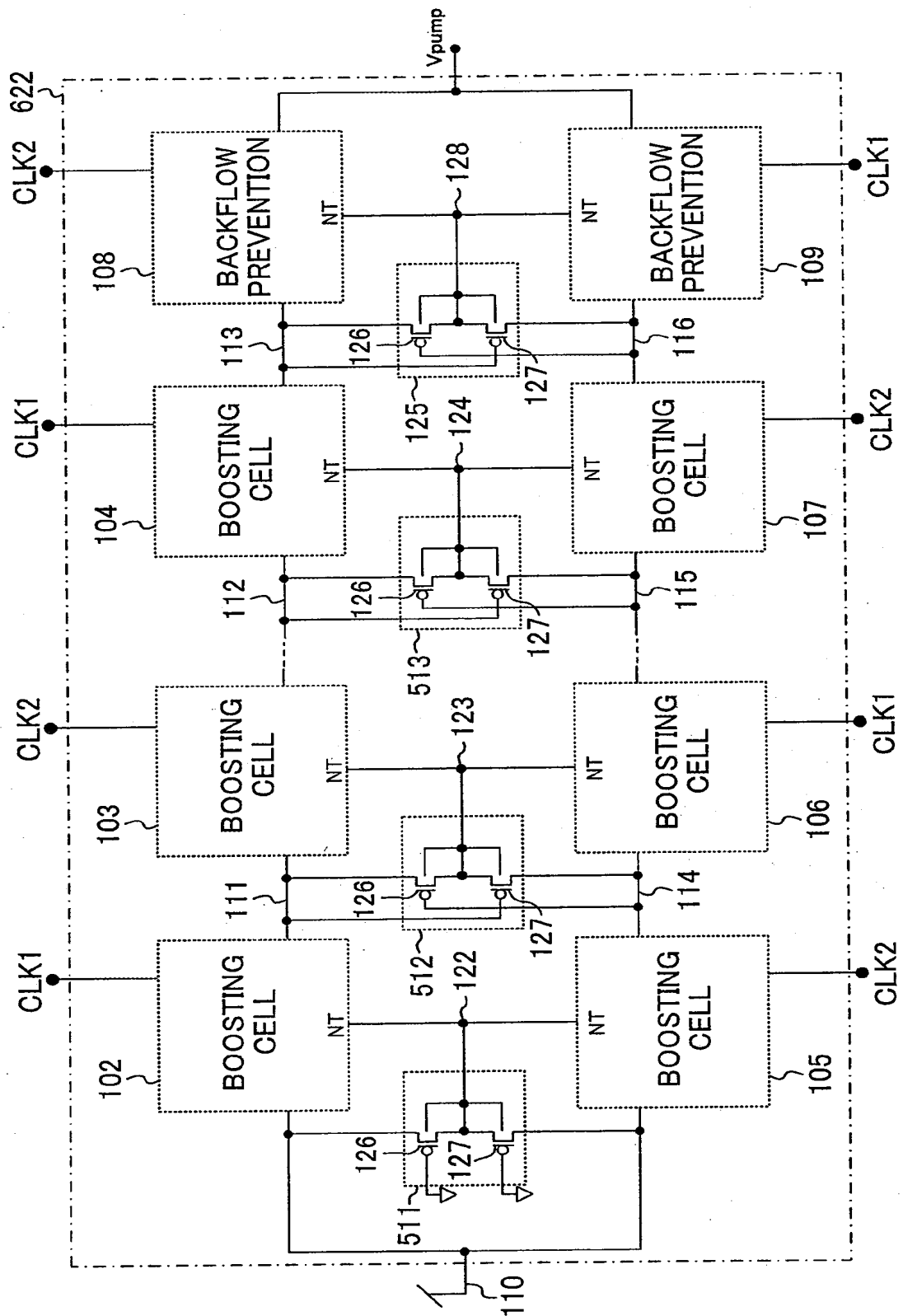




FIG. 7



FIG. 9

FIG. 10

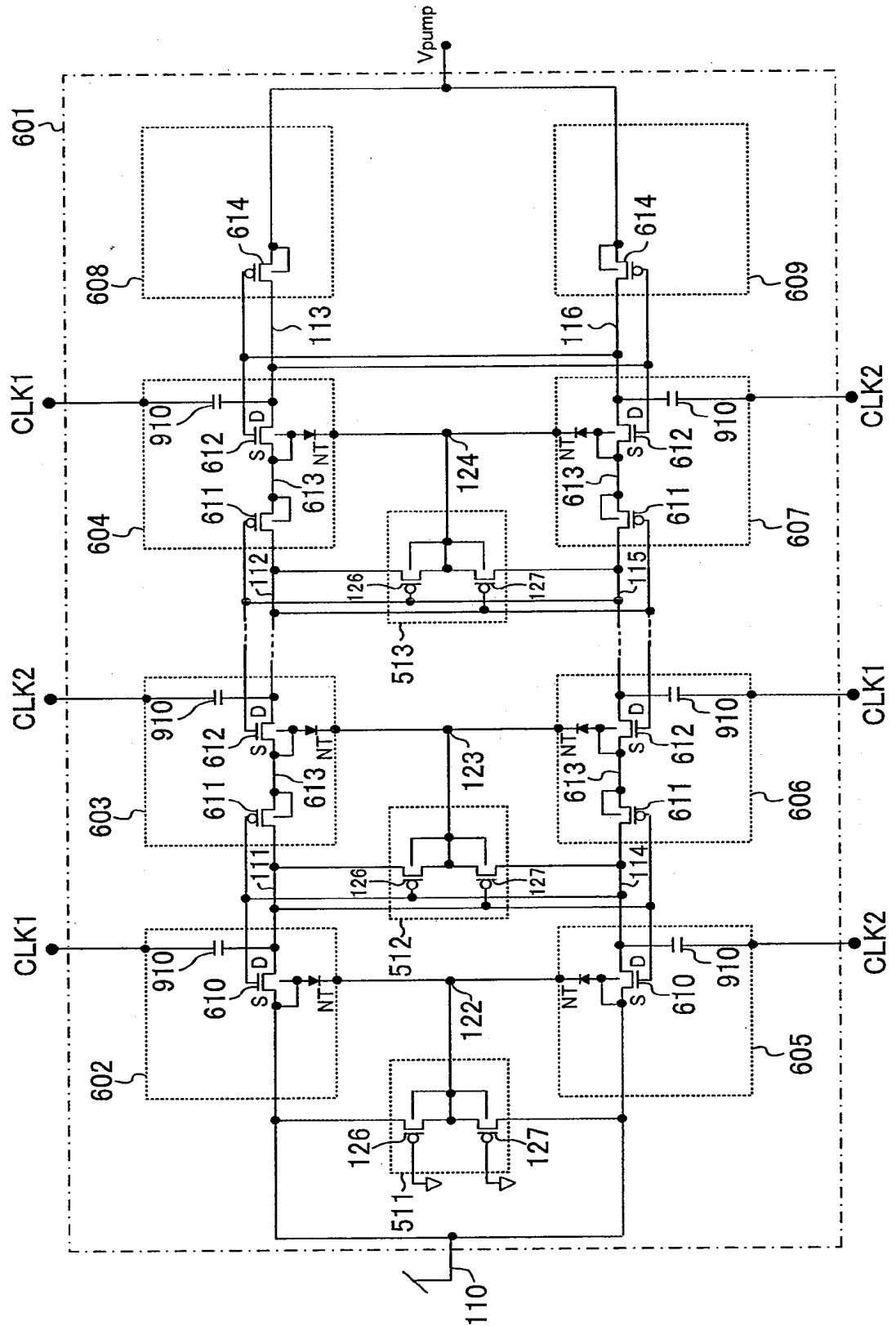


FIG. 11

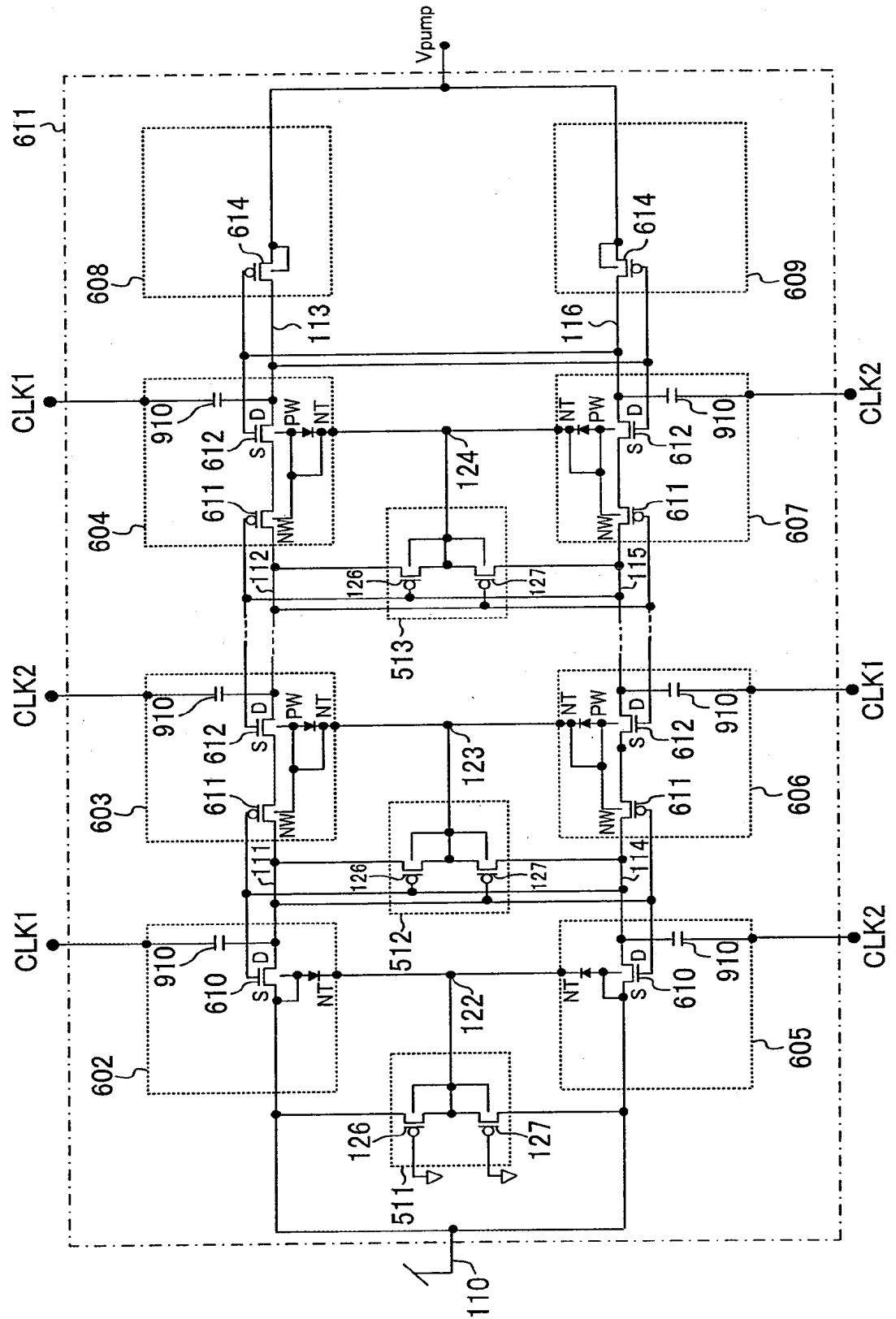


FIG. 12

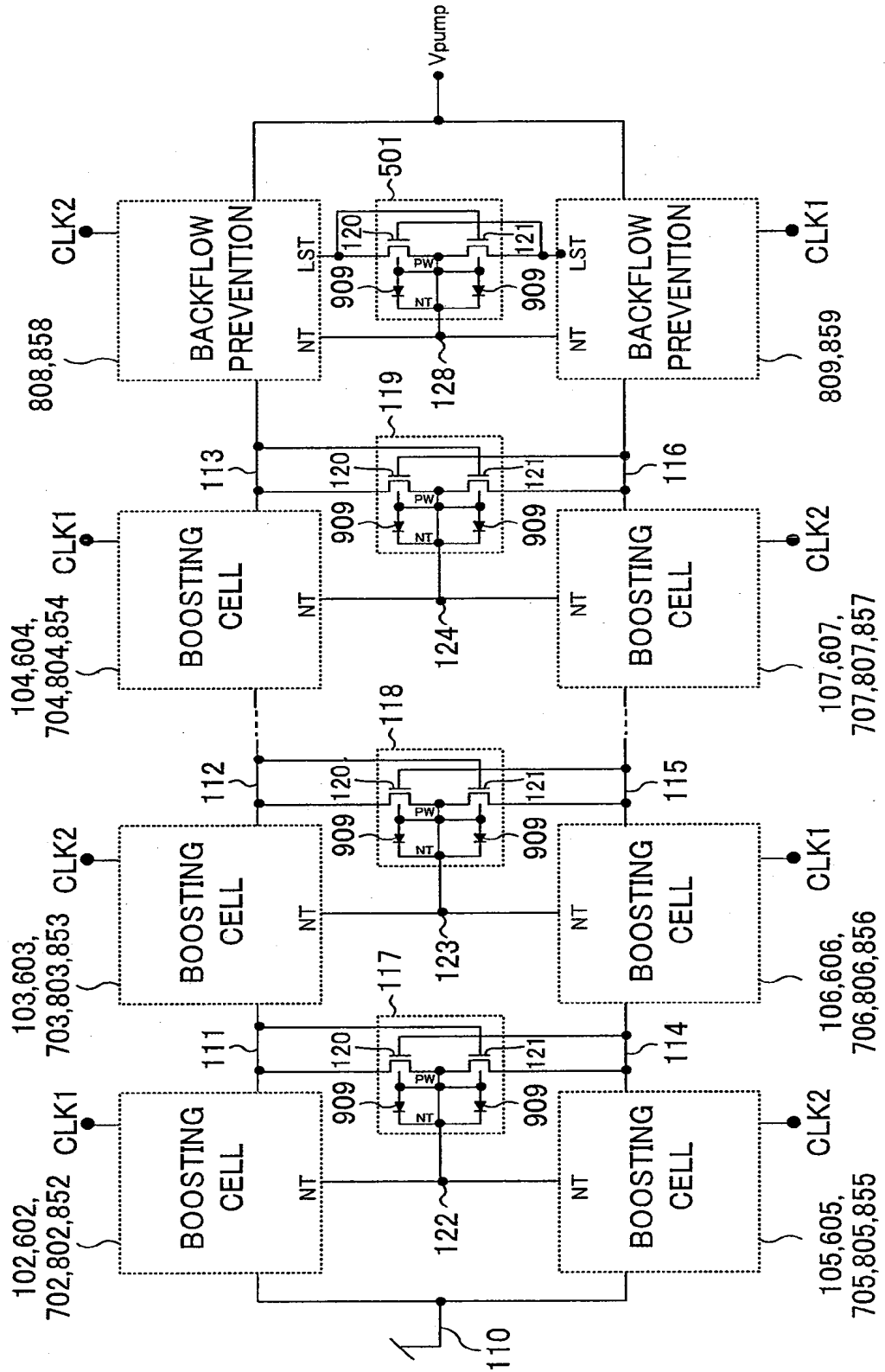


FIG. 13

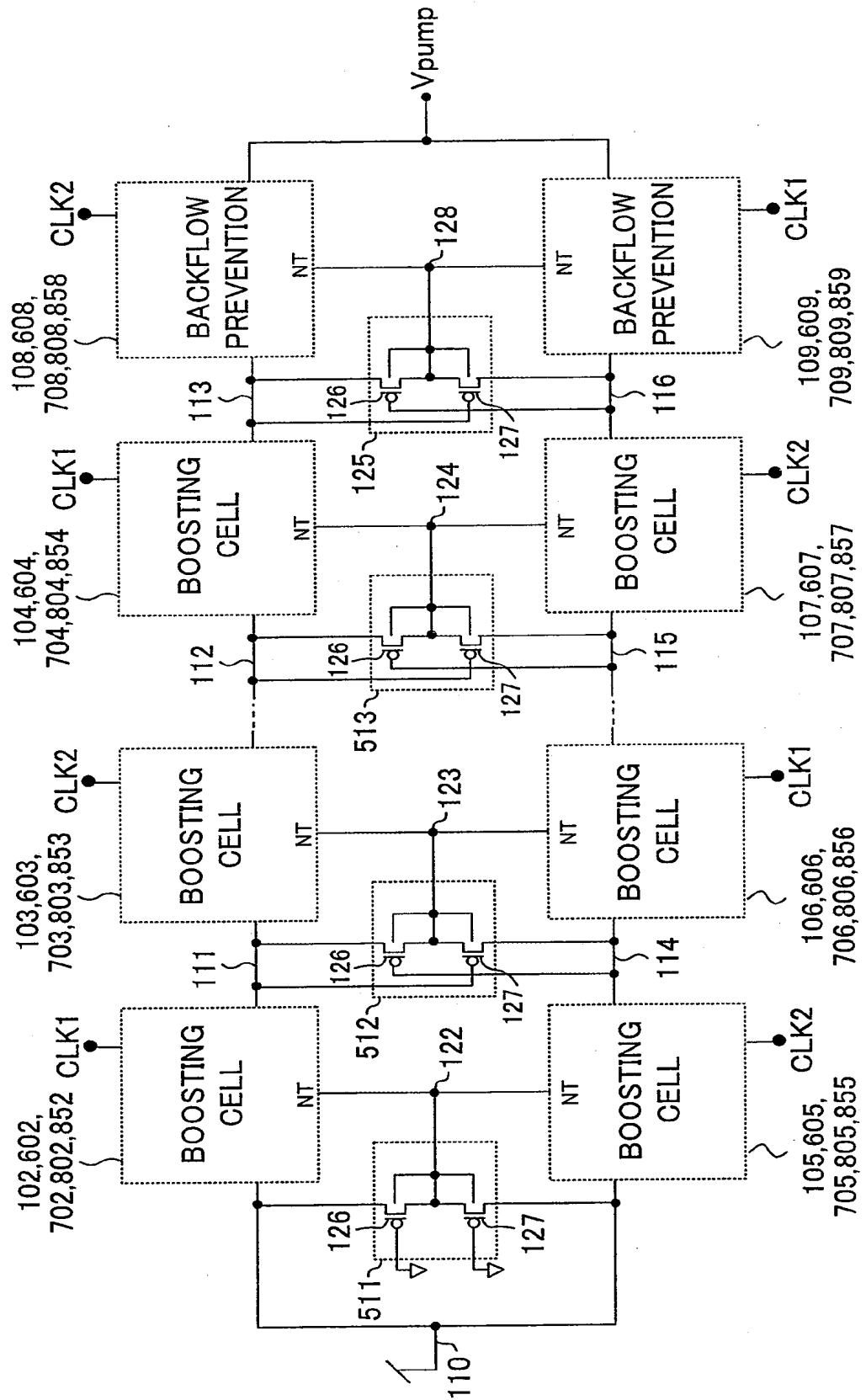


FIG. 15

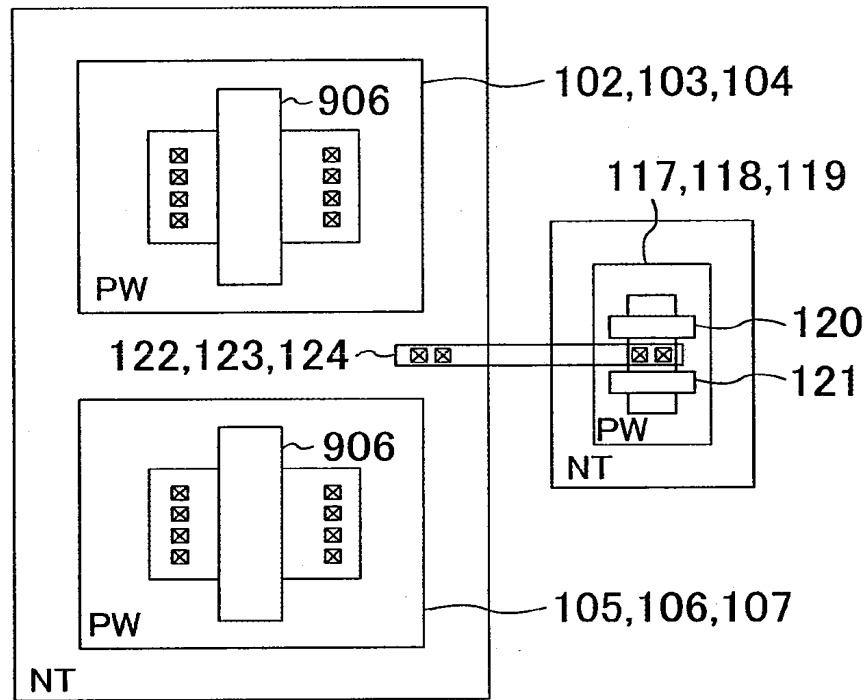


FIG. 16

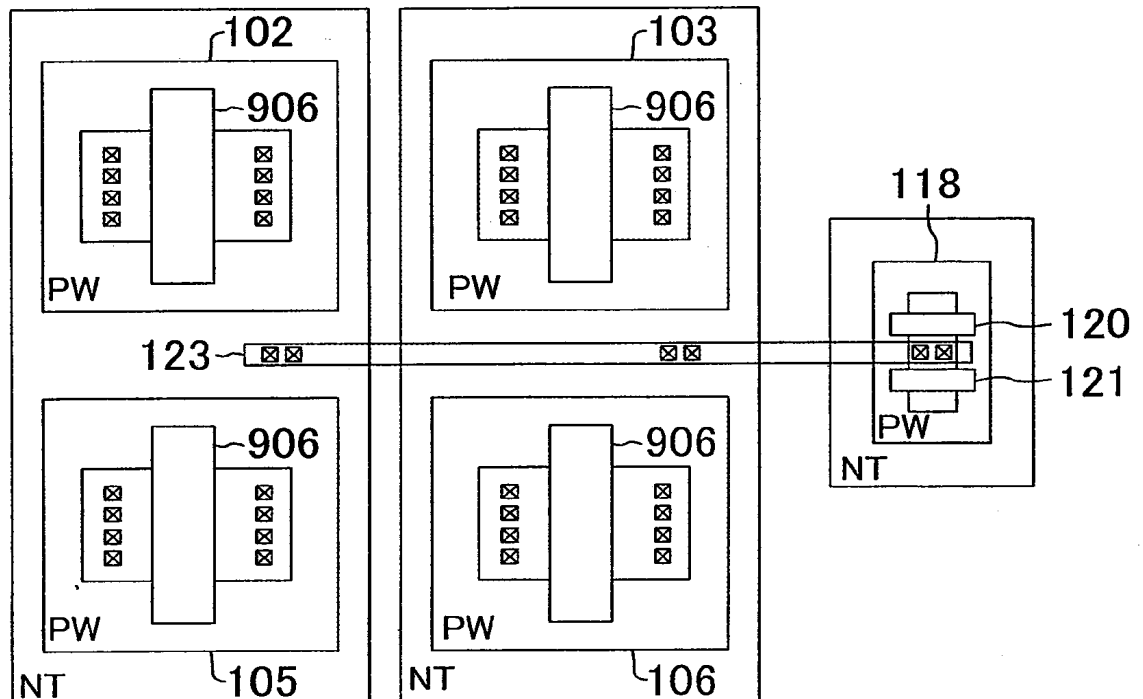


FIG. 17

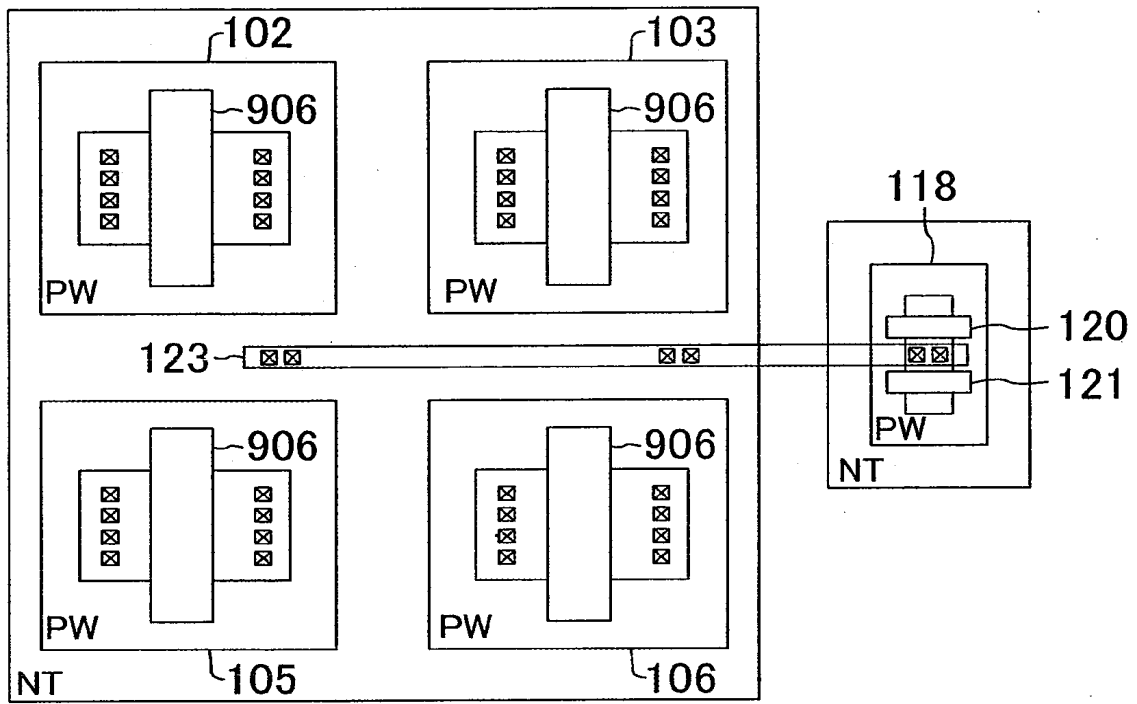


FIG. 18

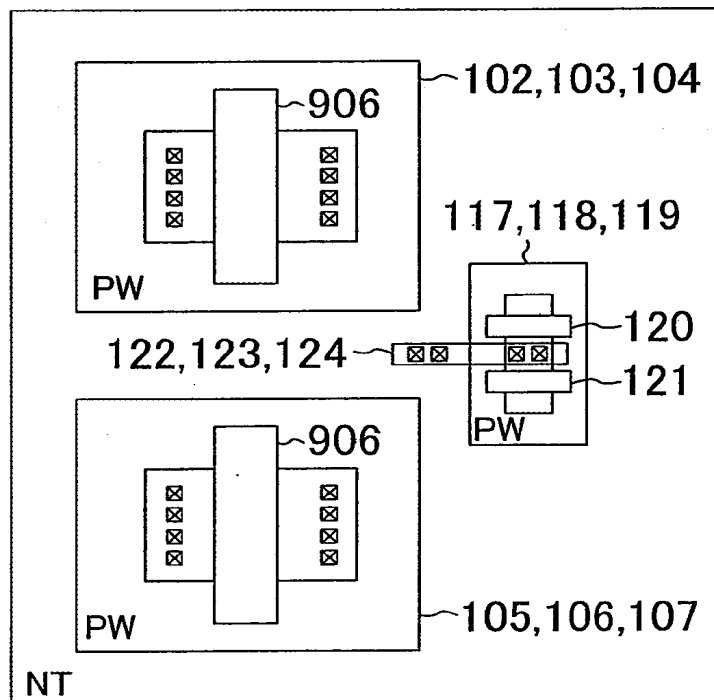


FIG. 19

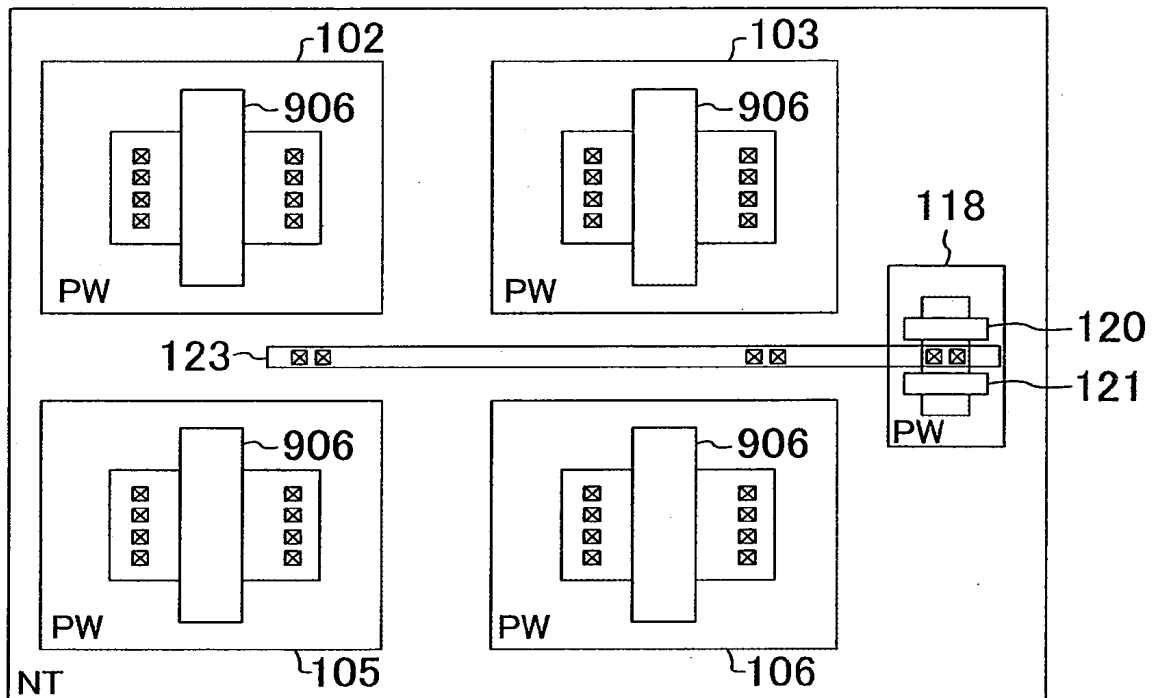


FIG. 20

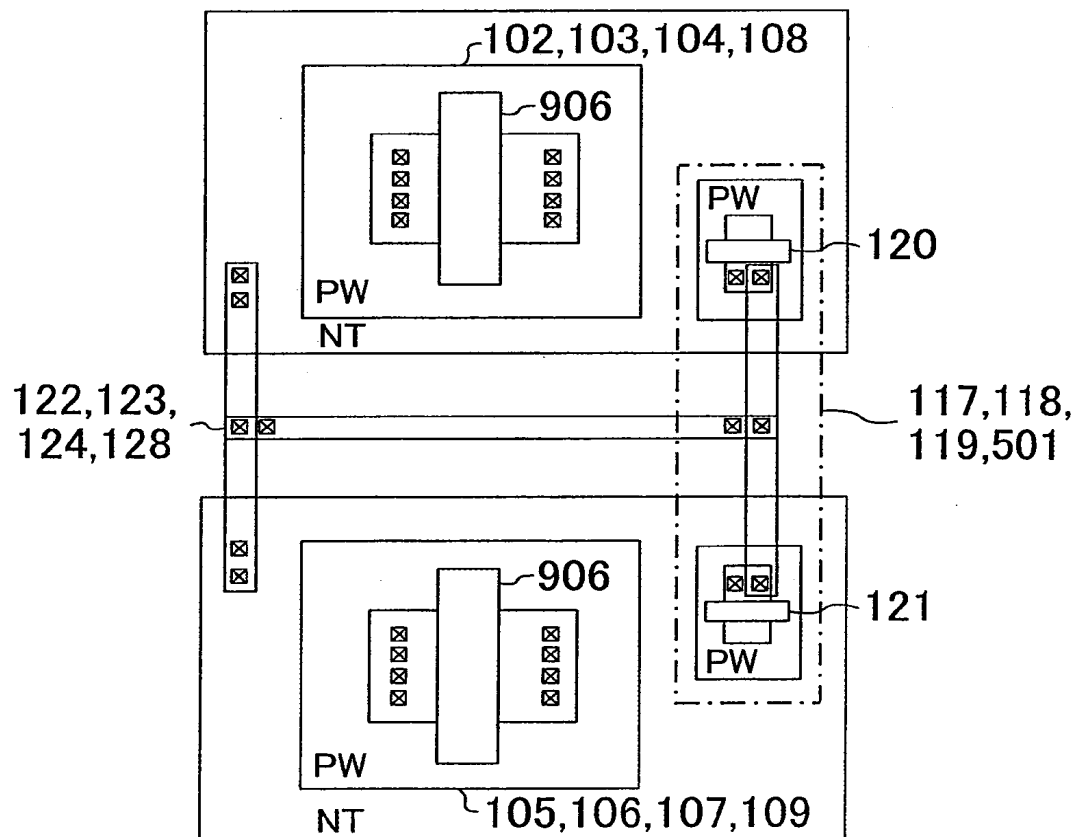


FIG. 21

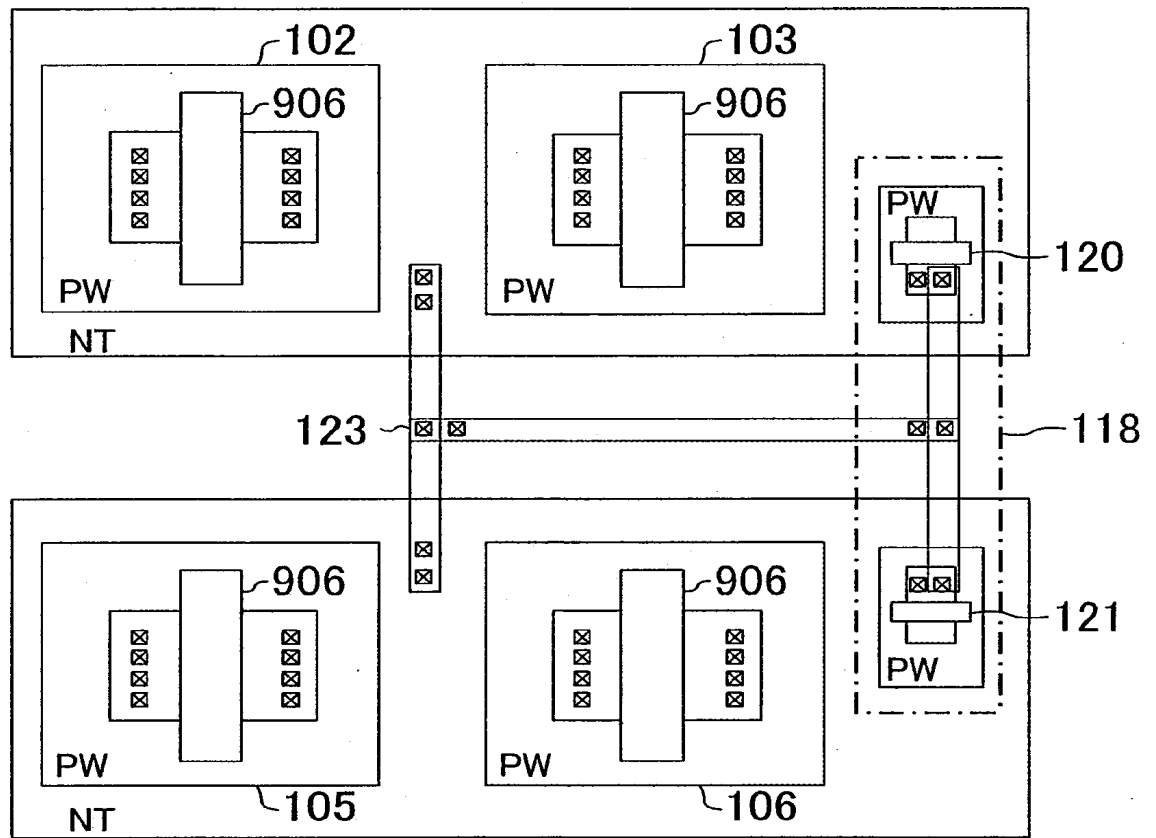


FIG. 22

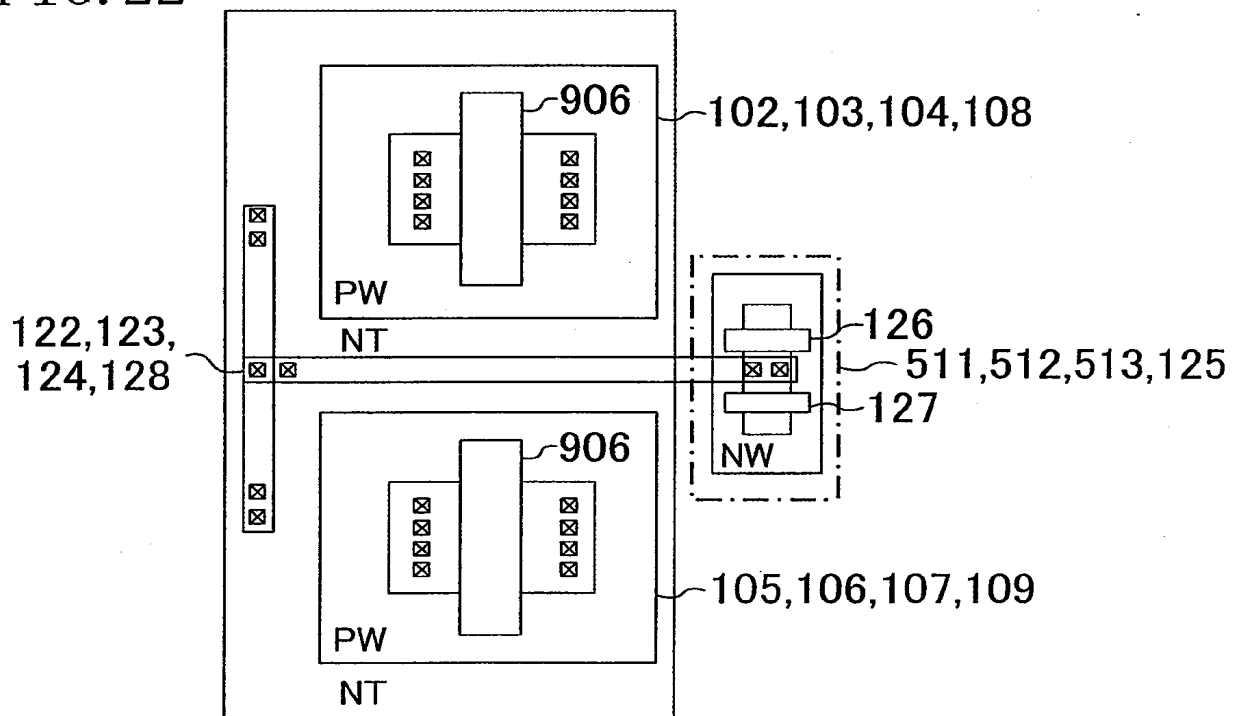


FIG. 23

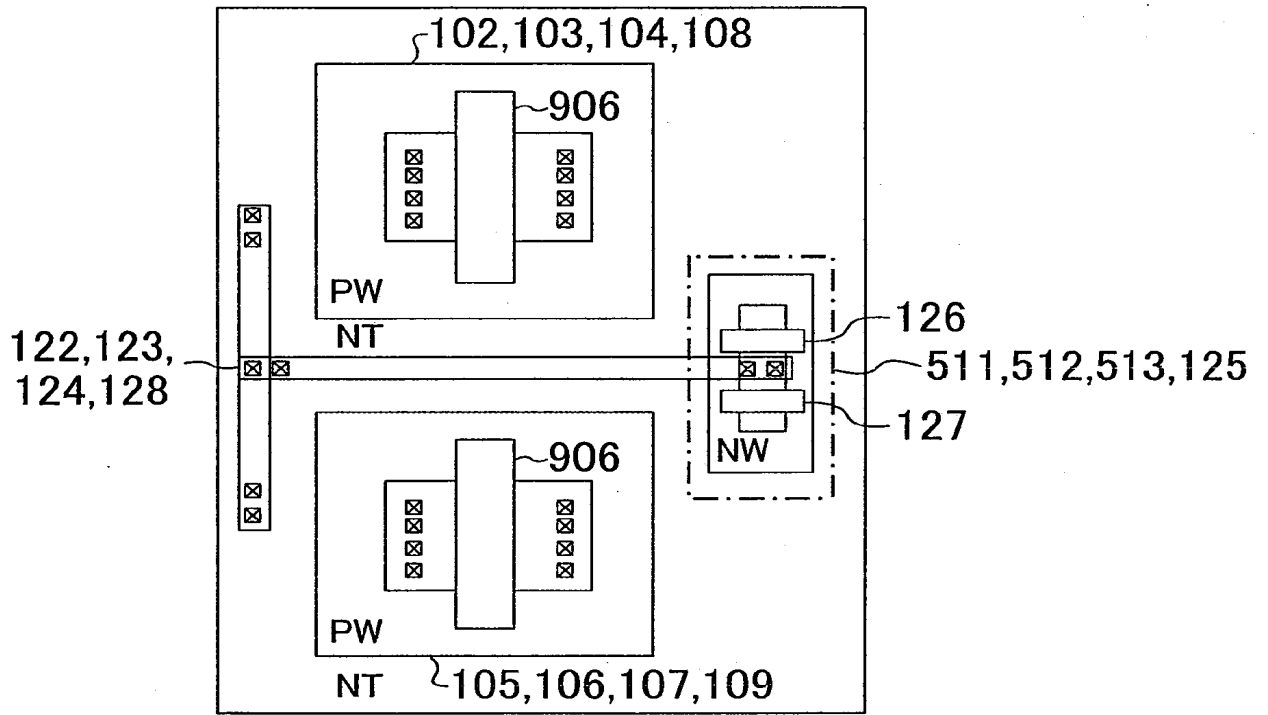


FIG. 24

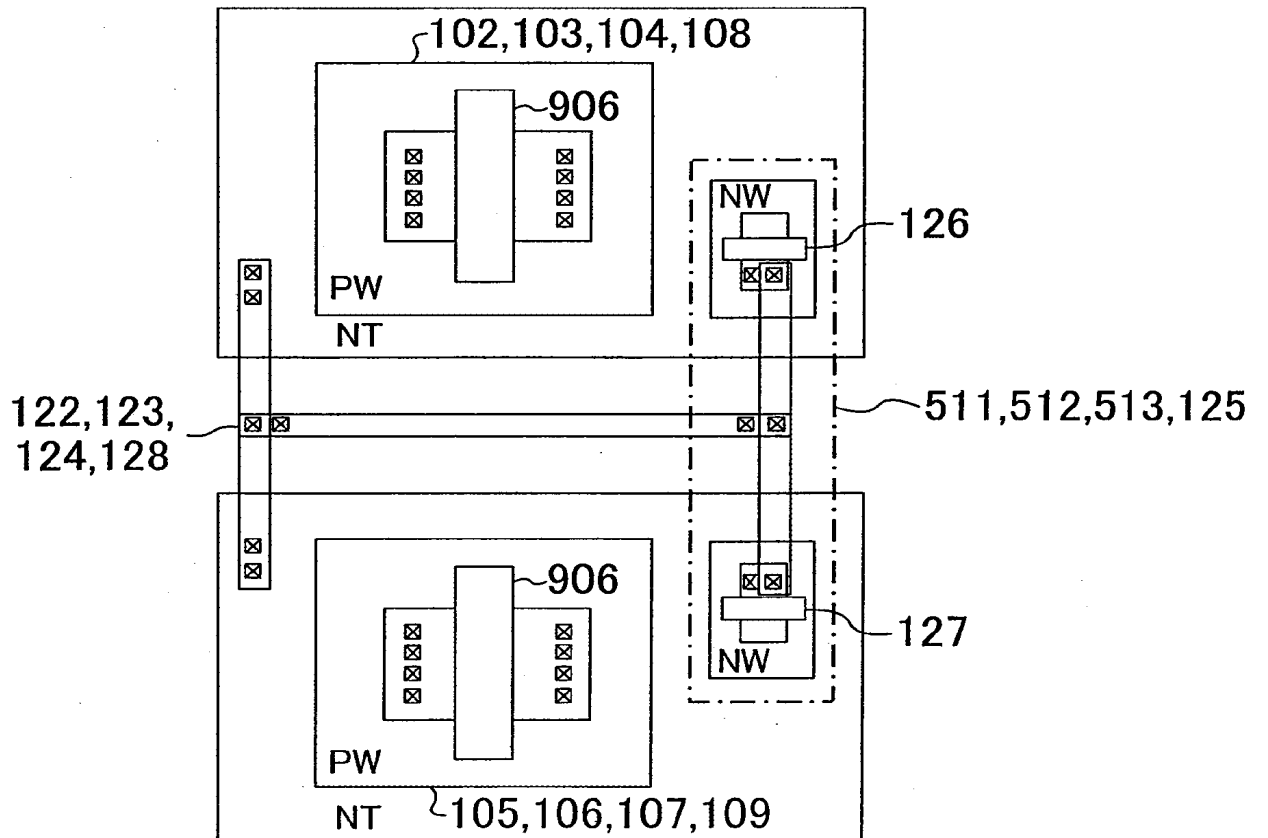


FIG. 25
PRIOR ART

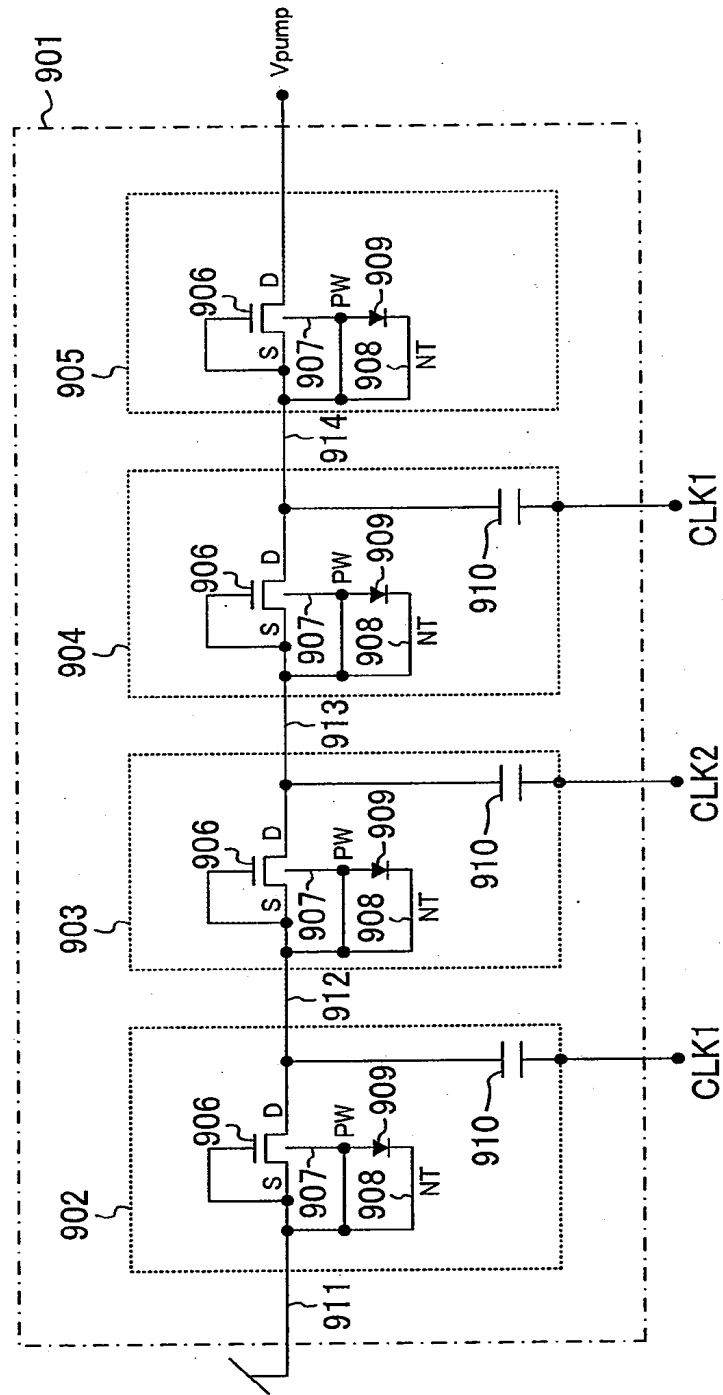
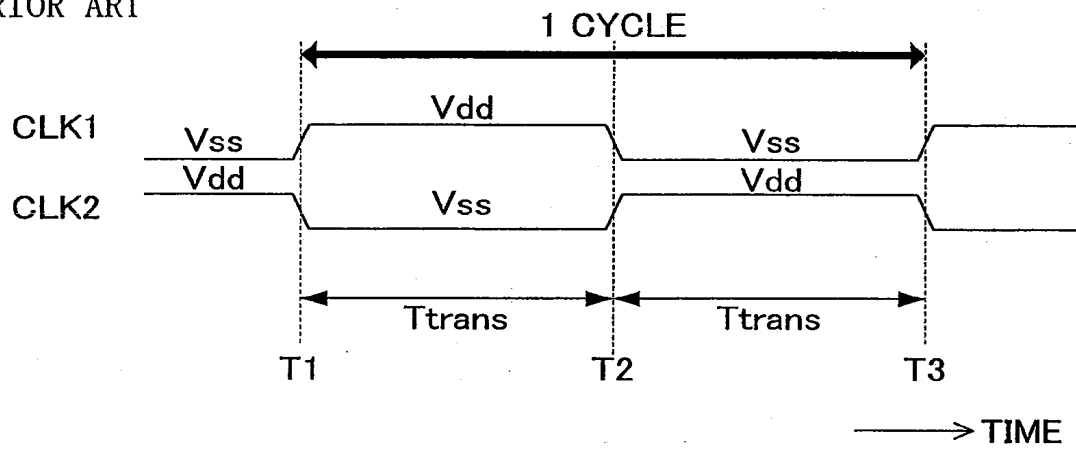


FIG. 26
PRIOR ART



Matsushita Ref*: P48465-01
 (* must be filled)
 Japan Firm Name: MAEDA PATENT OFFICE
 US Firm Name: MWE

Application Serial No. _____
 Japan Firm Ref: M07-P-543US1
 US Firm Ref: _____

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(a) ☒ Original (b) ☐ Supplemental (c) ☐ Substitute (d) ☐ PCT (e) ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title of Invention:
BOOSTER CIRCUIT

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

1. For use when submitting this Declaration prior to U.S. application filing date			
(f) ☒ the attached specification, or			
2. For use when submitting this Declaration after U.S. application filing date			
(g) ☐ the specification in the U.S. Application:	Application No. (if available)	filed on: (must be filled)	
	and with amendments (if applicable):		filed on _____, or
3. For PCT-US national entry: under 35 U.S.C. 371 (for use when filing this Declaration before and after the U.S. national entry date)			
(h) ☐ the specification in the International Application: (Check here only for US national entry under 35 U.S.C. 371.)	PCT Application No.	filed on: (PCT filing date)	
	and with amendments (if applicable):		filed on: _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

(Foreign Priority Information)

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2007-007694	January 17, 2007	Yes
JAPAN	2007-307064	November 28, 2007	Yes

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

(US Provisional Application Information)

APPLICATION NO.	U.S. PROVISIONAL APPLICATION FILING DATE

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Domestic Priority Information)

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with U.S. Patent and Trademark Office Customer Number identified below to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Matsushita Electric Industrial Co., Ltd., and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

INVENTOR (s)

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Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
	Kyoto, JAPAN			JAPAN
Post office address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE
	c/o Matsushita Electric Industrial Co., Ltd., 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Full Name of Second Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS	CITY	STATE OR COUNTRY	ZIP CODE

Docket No.: 085393-0241

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of U.S.	:	
Serial No. 12/015,882	:	Group Art Unit: Not Yet Assigned
	:	
Filed: July 14, 2010	:	Examiner: Not Yet Assigned
	:	
For: BOOSTER CIRCUIT	:	

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Amendments to the Drawings begin on page 7 of this paper.

Remarks/Arguments begin on page 8 of this paper.

An Appendix includes 2 (two) pages of Replacement Sheets of Figures 3 and 9 is attached following page 8 of this paper.

IN THE SPECIFICATION:

Please insert the following new paragraph after the Title and before the "BACKGROUND OF THE INVENTION"

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/015,882, filed on January 17, 2008, claiming priority of Japanese Patent Application Nos. 2007-007694, filed on January 17, 2007, and 2007-307064, filed on November 28, 2007, the entire contents of each of which are hereby incorporated by reference. --

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application

Listing of Claims:

Claims 1-15 (Cancelled)

16. (New) A booster circuit comprising:
a first boosting cell row including N stages ($N \geq 1$) of boosting cells;
a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and
at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row, wherein:

each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and

the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

17. (New) The booster circuit of claim 16, wherein:

the first boosting cell row includes at least one backflow preventing circuit;

the second boosting cell row includes at least one backflow preventing circuit; and

the well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.

18. (New) The booster circuit of claim 16, wherein the well bias potential is the higher potential out of the input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

19. (New) The booster circuit of claim 16, wherein the well bias potential is the lower potential out of the input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

20. (New) The booster circuit of claim 16, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.

21. (New) The booster circuit of claim 16, wherein the second well region and the first well region are connected to each other so that the second well region and the first well region have the same potential.

22. (New) The booster circuit of claim 16, wherein:

the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

the at least one analog comparison circuit is provided for each boosting cell stage in the first boosting cell row and the second boosting cell row.

23. (New) The booster circuit of claim 16, wherein:

the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

the at least one analog comparison circuit is provided for arbitrary number of boosting cell stages in the first boosting cell row and the second boosting cell row.

24. (New) The booster circuit of claim 16, wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

25. (New) The booster circuit of claim 16, wherein:

the at least one switching element of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

the at least one switching element of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

26. (New) The booster circuit of claim 16, wherein an output potential of the analog comparison circuit is applied to the first well region of the at least one switching element included in a boosting cell of a boosting cell row different from the first and second boosting cell rows.

27. (New) A booster circuit comprising:

- a first boosting cell row including N stages ($N \geq 1$) of boosting cells; and
- a second boosting cell row including M stages ($M \geq 1$) of the boosting cells, wherein:
 - each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,
 - the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, and
 - a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row and an input potential of the boosting cells of the second boosting cell row.

IN THE DRAWINGS:

Figures 3 and 9 have been amended as a response to Notice to File Corrected Application Papers mailed on January 24, 2008 in the parent application No. 12/015,882.

Replacement Sheets of Figures 3 and 9 are attached.

REMARKS

The specification in the above-referenced application has been amended to incorporate the continuity information. Figures 3 and 9 have also been amended as a response to Notice to File Corrected Application Papers mailed on January 24, 2008 in the parent application No. 12/015,882 .

Additionally, the amendment cancels claims 1-15, without prejudice. Claims 16-27 are pending for examination in this Divisional application.

No new matter has been introduced. Entry of this amendment is respectfully requested.

Respectfully submitted,

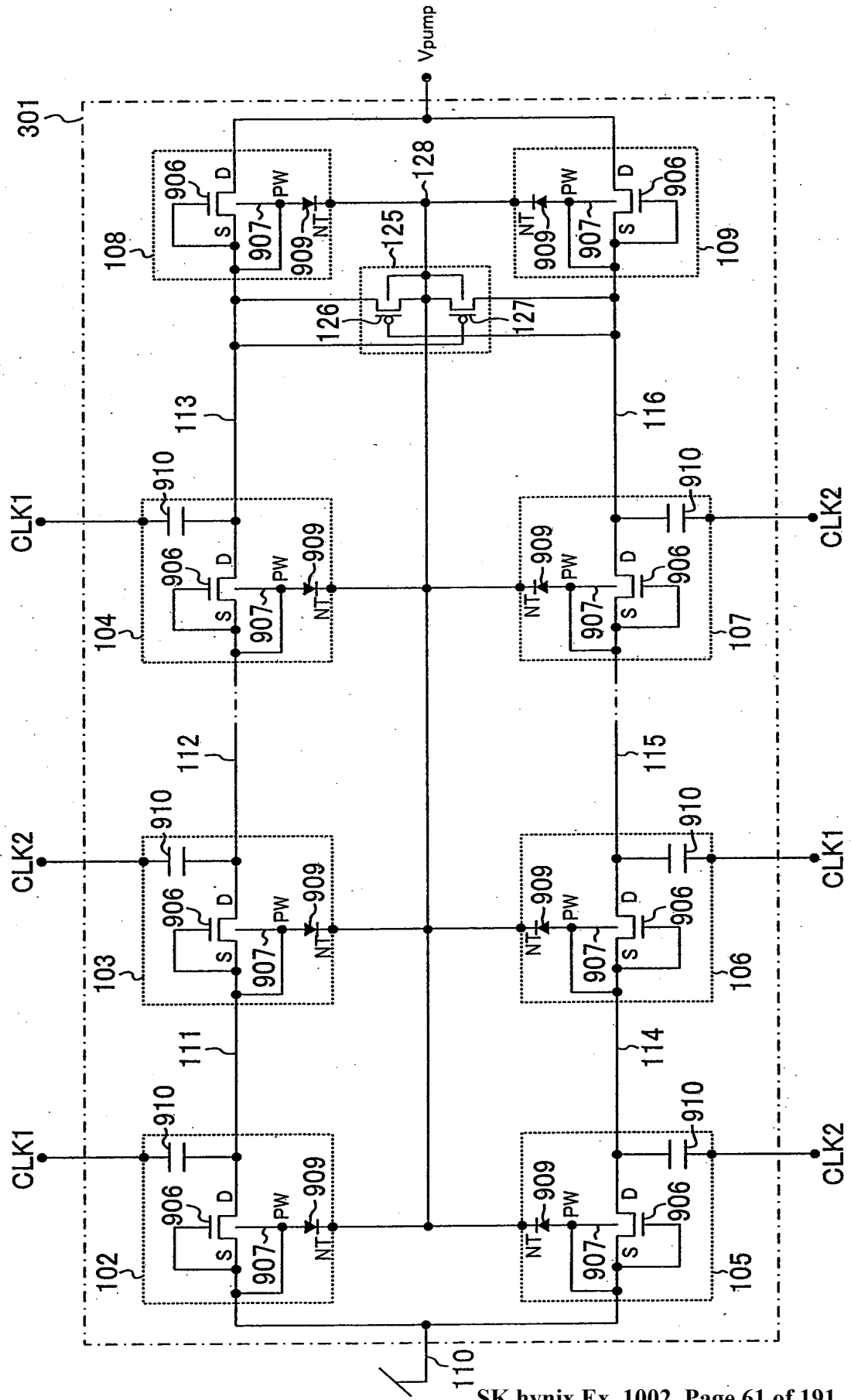
McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: July 14, 2010

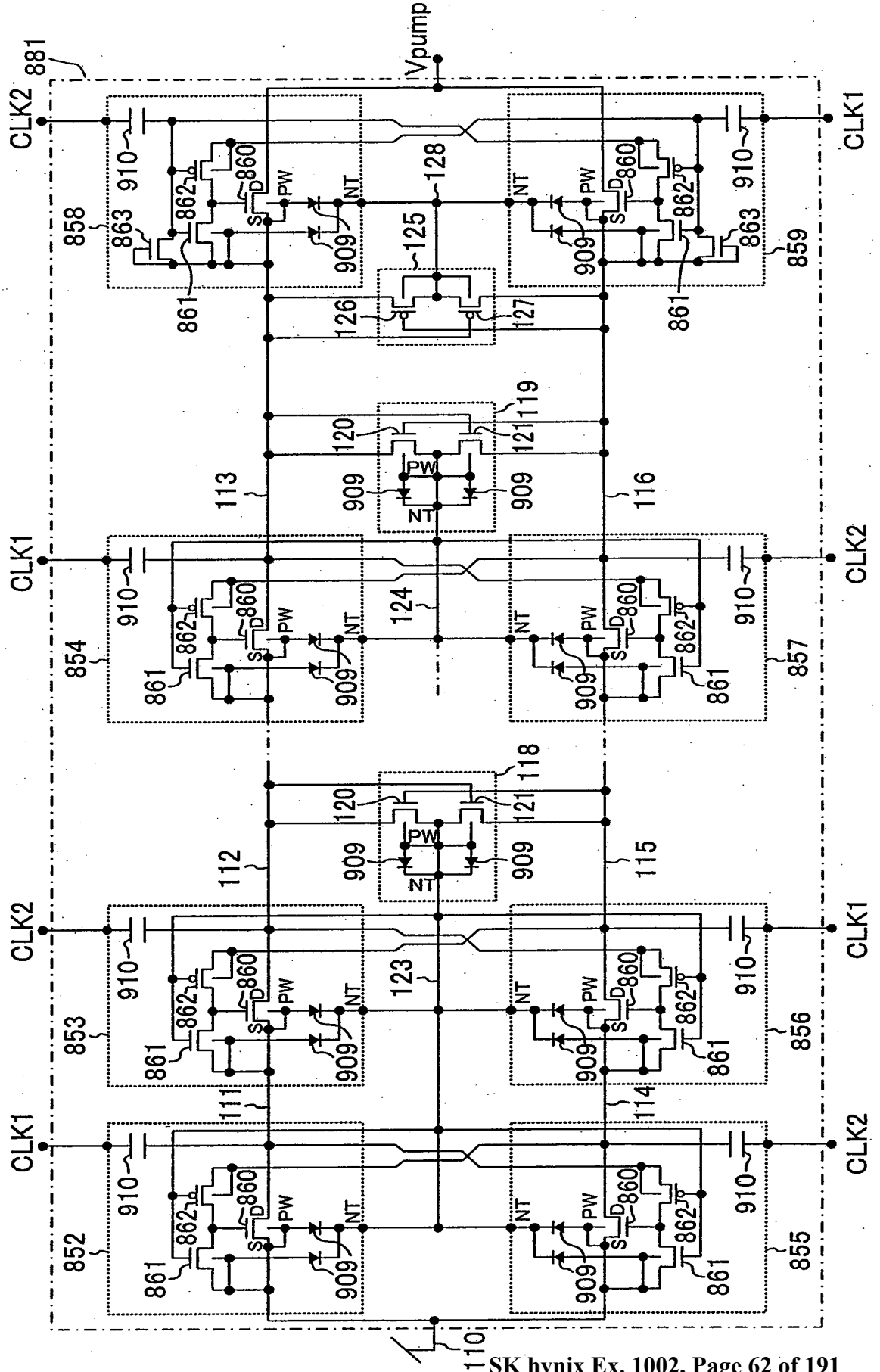
FIG. 3



REPLACEMENT SHEET

9/21

FIG. 9



REQUEST FORM FOR DIVISIONAL APPLICATION UNDER 37 CFR 1.53(b)

DOCKET NUMBER: 085393-0241

Prior Application:

Art Unit: 2816

Examiner: JEFFERY SHAWN ZWEIZIG

BOX New Applications

FEE

Mail Stop New Applications

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

This is a Request for filing a Divisional application under 37 CFR 1.53(b) of pending prior application

No. 12/015,882, filed on January 17, 2008, entitled **BOOSTER CIRCUIT**, by the following named inventor(s):

Seiji YAMAHIRA.

1. ☒ I hereby state that the enclosed application contains no new matter.
2. Oath or Declaration
 - a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ Deletion of inventor(s)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
3. ☒ Incorporation By Reference (useable if Box 2b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 2b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
4. ☒ Preliminary Amendment is enclosed.
5. ☒ An Information Disclosure Statement and PTO1449 Form are submitted herewith.
6. ☒ Cancel claims 1-15.

7. The filing fee is calculated on the basis of the claims existing in the prior application as amended at 4 and 6 above:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	12	-20	0	\$52.00	\$0.00
Independent Claims	2	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$270.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Total of Above Calculations					\$1,090.00
Less ½ for Small Entity					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,090.00

8. ☐ A Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 was filed in prior application and such status is still proper and desired.
9. ☒ **PLEASE CHARGE DEPOSIT ACCOUNT 500417 in the amount of \$1,090.00.** Commissioner is authorized to charge any fees which may be required or credit any overpayment to Deposit Account No. 500417.
10. ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 which may be required, including any extension of time fees to maintain the pendency of the parent Application No. Not Yet Assigned or credit any overpayment to Deposit Account No. 500417.
11. ☒ Priority of Application Nos. 2007-007694, filed on January 17, 2007, and 2007-307064, filed on November 28, 2007, in Japan is claimed under 35 USC 119. The request to retrieve electronic priority documents were filed in Application No. 12/015,882 on January 17, 2008.
12. ☒ The prior application is assigned of record to
- PANASONIC CORPORATION**
Osaka, Japan
13. ☒ The power of attorney in the prior application is to:
- McDermott Will & Emery LLP
14. ☐ Also enclosed:

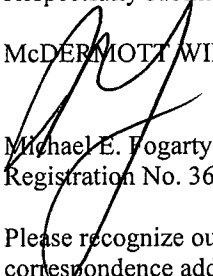
15. ☐ A petition, fee and response has been filed to extend the term in the pending prior application until .

Address all future communications to: (May only be completed by applicant, or attorney or agent of record)

McDermott Will & Emery LLP
600 13th Street, N.W.
Washington, D.C. 20005-3096

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 53080 as our
correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: July 14, 2010

Docket No.: 085393-0241

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Divisional of U.S.		
Serial No. 12/015,882	:	Group Art Unit: Not Yet Assigned
	:	
Filed: July 14, 2010	:	Examiner: Not Yet Assigned
	:	
For: BOOSTER CIRCUIT		

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

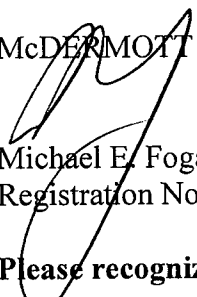
This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Divisional of U.S. Serial No. 12/015,882

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial no. 12/015,882, filed January 17, 2008, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,


McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

**Please recognize our Customer No. 53080
as our correspondence address.**

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:ln
Facsimile: 202.756.8087
Date: July 14, 2010

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0241		SERIAL NO. Divisional of U.S. Serial No. 12/015,882	
				APPLICANT Seiji YAMAHIRA			
				FILING DATE July 14, 2010		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 6,100,557	08-08-2000	HUNG et al.			
		US 6,121,821	09-19-2000	MIKI			
		US 6,878,981 B2	04-12-2005	ESHEL			
		US 6,888,400 B2	05-03-2005	LIN et al.			
		US 7,102,422 B1	09-05-2006	SAWADA et al.			
		US 6,734,717 B2	05-11-2004	MIN			
		US 6,952,129 B2	10-04-2005	LIN et al.			
		US 7,123,077 B2	10-17-2006	CHIU et al.			
		US 2007/0096796 A1	05-03-2007	FIRMANSYAH et al.			
		US 7,532,062	05-2009	Namekawa et al.			
		US 7,317,347	01-2008	Mesi et al.			
		US 6,501,325	12-2002	Meng, Anita			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:

Filing Date:

Title of Invention:

BOOSTER CIRCUIT

First Named Inventor/Applicant Name:

Seiji YAMAHIRA

Filer:

Michael E. Fogarty/Lydia Nguyen

Attorney Docket Number:

085393-0241

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220

Pages:

Claims:

Miscellaneous-Filing:

Petition:

Patent-Appeals-and-Interference:

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt

EFS ID:	8014702
Application Number:	12836122
International Application Number:	
Confirmation Number:	1536
Title of Invention:	BOOSTER CIRCUIT
First Named Inventor/Applicant Name:	Seiji YAMAHIRA
Customer Number:	53080
Filer:	Michael E. Fogarty/Lydia Nguyen
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0241
Receipt Date:	14-JUL-2010
Filing Date:	
Time Stamp:	15:28:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	1713
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	P04846503_TRN_085393-0241.pdf	82121	no	3
			980f3d2a3f6d23303cbb0b1ecc8db4e33d209c89		
Warnings:					
Information:					
2		P04846503_SPEC_085393-0241.pdf	1200261	yes	26
			d4a2b8e0645b7879b40c9316160f46a28ad191d2		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	19	
	Claims		20	25	
	Abstract		26	26	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P04846503_DRW_085393-0241.pdf	544488	no	21
			e3185e91ecd8d2d06624f62b968c0088505b4a50		
Warnings:					
Information:					
4	Oath or Declaration filed	P04846503_DEC_085393-0241.pdf	140965	no	2
			e3754127012fe8bc4d933609ab56366834106343		
Warnings:					
Information:					
5	Preliminary Amendment	P04846503_AMEND-P_085393-0241.pdf	268752	no	10
			3fe19e896f79e420f909ba8d5d4f8bda2b43c901		
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Filed (SB/08)	P04846503_IDS_085393-0241.pdf	100417	no	3
			8dcb4c603d733fe61de690de706e2d2cdd74c584		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					

7	Fee Worksheet (PTO-875)	fee-info.pdf	32860 4e7c9f829d2b2842345da6a5b028ea02345b8bd6	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2369864		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

date : 07/14/10

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/836,122	
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
OTHER THAN SMALL ENTITY						
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	12	minus 20 =	x\$26		x\$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *	x\$110		x\$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						
			195		390	
			TOTAL		TOTAL	1090
* If the difference in column 1 is less than zero, enter "0" in column 2.						
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		
SMALL ENTITY		OR		OTHER THAN SMALL ENTITY		
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	
X =		X =		X =		
X =		X =		X =		
N/A		N/A		N/A		
TOTAL ADD'T FEE			TOTAL ADD'T FEE			
(Column 1)		(Column 2)		(Column 3)		
SMALL ENTITY		OR		OTHER THAN SMALL ENTITY		
RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)	
X =		X =		X =		
X =		X =		X =		
N/A		N/A		N/A		
TOTAL ADD'T FEE			TOTAL ADD'T FEE			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/836,122		Filing Date 07/14/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		TOTAL			
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	07/14/2010	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X \$	=		X \$52=	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$	=		X \$220=	0
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	0
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
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Assignment For Published Patent Application

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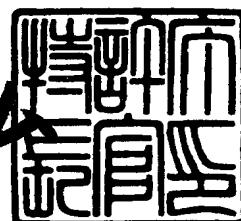
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【書類名】 特許請求の範囲

【請求項 1】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内又は前記第 2 のウエル領域内に 1 つ以上のスイッチング素子を備えて、前記 1 つ以上のスイッチング素子により第 1 の端子と第 2 の端子との間をオン・オフして前記第 1 の端子から前記第 2 の端子へ電荷を転送する昇圧セルを備えた昇圧回路であって、

N 段 ($N \geq 1$) の前記昇圧セルから構成された第 1 の昇圧セル列と、

M 段 ($M \geq 1$) の前記昇圧セルから構成された第 2 の昇圧セル列と、

前記第 1 の昇圧セル列の i 段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第 2 の昇圧セル列の i 段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第 1 及び第 2 の昇圧セル列の $i + 1$ 段目の前記昇圧セル又は i 段目の前記昇圧セル又は i 段目より前段の前記昇圧セルのうちの 1 つ以上に備えられた前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域に印加することを特徴とする昇圧回路。

【請求項 2】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内又は前記第 2 のウエル領域内に 1 つ以上のスイッチング素子を備えて、前記 1 つ以上のスイッチング素子により第 1 の端子と第 2 の端子との間をオン・オフして前記第 1 の端子から前記第 2 の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路であって、

N 段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第 1 の昇圧セル列と、

M 段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第 2 の昇圧セル列と、

各々前記第 1 の昇圧セル列の i 段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第 2 の昇圧セル列の i 段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第 1 及び第 2 の昇圧セル列の前記逆流防止回路又は $i + 1$ 段目の前記昇圧セル又は i 段目の前記昇圧セル又は i 段目より前段の前記昇圧セルのうちの 1 つ以上に備えられた前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域に印加することを特徴とする昇圧回路。

【請求項 3】

請求項 1 又は 2 に記載の昇圧回路において、

前記第 2 のウエル領域と前記第 1 の端子とが同電位となるように、前記第 2 のウエル領域と前記第 1 の端子とが互いに接続されたことを特徴とする昇圧回路。

【請求項 4】

請求項 1 又は 2 に記載の昇圧回路において、

前記アナログ比較回路は、前記基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内又は前記第 2 のウエル領域内に 1 つ以上のスイッチング素子を有するものであり、かつ前記昇圧セルの各段毎に備えられていることを特徴とする昇圧回路。

【請求項 5】

請求項 1 又は 2 に記載の昇圧回路において、

前記アナログ比較回路は、前記基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内又は前記第 2 のウエル領域内に 1 つ以上のスイッチング素子を有するものであり、前記第 1 及び第 2 の昇圧セル列に 1 つ以上備えられ、かつ前記昇圧セルの任意の段数毎に備えられていることを特徴とする昇圧回路。

【請求項 6】

請求項 1 又は 2 に記載の昇圧回路において、
前記昇圧セルの前記第 1 の端子と前記 1 のウエル領域との間にダイオード手段を備えたことを特徴とする昇圧回路。

【請求項 7】

請求項 1 又は 2 に記載の昇圧回路において、
前記第 1 のウエル領域の電位が同電位である前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域のレイアウトを共通化したことを特徴とする昇圧回路。

【請求項 8】

請求項 1 又は 2 に記載の昇圧回路において、
前記第 1 のウエル領域の電位が同電位である前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域のレイアウトと前記アナログ比較回路の前記第 1 のウエル領域のレイアウトとを共通化したことを特徴とする昇圧回路。

【書類名】明細書

【発明の名称】昇圧回路

【技術分野】

【0001】

本発明は、トリプルウエル構造のスイッチング素子を利用した昇圧回路に関するものである。

【背景技術】

【0002】

近年、不揮発性半導体記憶装置の1つであるフラッシュメモリにおいては、単一電源電圧又は低い電源電圧でのデータの読み出し、データの書き換えが要求されており、各動作を実施する際にオンチップで正又は負の昇圧電圧を供給する昇圧回路が必要とされている。また、CMOSプロセスにおいても昇圧回路で発生された電源電圧がアナログ回路の特性改善に用いられている。

【0003】

従来、トリプルウエル構造のスイッチング素子を利用した昇圧回路が知られている（特許文献1～3参照）。

【0004】

図13は、従来の昇圧回路の例を示している。図13において、901は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで出力端子電圧（昇圧電圧） V_{pump} を発生する昇圧回路である。902、903、904は3段の構成例であり、奇数段目にCLK1が入力され、偶数段目にCLK2が入力される昇圧セル、905は昇圧電圧 V_{pump} の逆流を防止する逆流防止回路、906はスイッチング素子として機能する電荷転送トランジスタ、907は電荷転送トランジスタ906のPウエル（PW）、908は当該Pウエル907を含む深いNウエル（NT）、909はPウエル907とNウエル908との間の寄生ダイオード、910は昇圧セル902、903、904の出力端子を昇圧する昇圧容量であり、911、912、913、914は昇圧セルの入出力端子である。図13に示すとおり、昇圧セル902～904の各電荷転送トランジスタ906のPウエル907とNウエル908とを各電荷転送トランジスタ906のソースと接続し、これらを同電位にしている。

【0005】

図14は、図13の昇圧回路901における2相クロック信号CLK1、CLK2の波形図である。図14を用いて、図13の昇圧回路901の動作を簡単に説明する。

【0006】

まず、時刻T1の状態では、CLK1が“H”（電源電圧 V_{dd} ）、CLK2が“L”（接地電圧 V_{ss} ）となり、入出力端子912、914の電位が昇圧される。同時に、昇圧セル903及び逆流防止回路905の各々の電荷転送トランジスタ906を介して、入出力端子912から入出力端子913へ、また入出力端子914から昇圧回路901の出力端子へそれぞれ電荷が転送され、入出力端子913及び昇圧回路901の出力端子電圧 V_{pump} がそれぞれ上昇する。このとき、昇圧セル903及び逆流防止回路905の各々のPウエル907を電荷転送トランジスタ906のソース端子と同電位としているので、電荷転送トランジスタ906の基板バイアス効果を抑制し、電荷転送効率の低下を抑制することができる。

【0007】

時刻T1から電荷転送期間 T_{trans} が経過して時刻T2の状態になると、CLK2が“H”、CLK1が“L”となり、入出力端子913の電位が昇圧される。同時に、昇圧セル904の電荷転送トランジスタ906を介して、入出力端子913から入出力端子914へ電荷が転送される。このとき、昇圧セル904のPウエル907を電荷転送トランジスタ906のソース端子と同電位としているので、電荷転送トランジスタ906の基板バイアス効果を抑制し、電荷転送効率の低下を抑制することができる。

【0008】

時刻T 3の状態になると、時刻T 1と同様の動作となる。

【0009】

以上のとおり、図13の昇圧回路901によれば、基板バイアス効果を抑制し、昇圧動作時の電荷転送効率の低下を抑制することができる。

【特許文献1】特開平8-125133号公報

【特許文献2】特開平11-283392号公報

【特許文献3】米国特許第6100557号明細書

【発明の開示】

【発明が解決しようとする課題】

【0010】

しかしながら、上記従来の昇圧回路901は、電荷転送トランジスタ906のソースとNウエル908とを接続するため、クロック信号CLK1、CLK2の電圧遷移に応じて、Nウエル908が形成する寄生容量をクロック信号CLK1、CLK2の電圧遷移幅で充放電する結果、消費電流が増加する課題があった。

【0011】

また、クロック信号CLK1、CLK2で供給する電荷をNウエル908の充放電電荷として使用するため、昇圧効率が低下する課題があった。

【0012】

また、電荷転送トランジスタ906のソースとNウエル908とを接続するため、Nウエル908を各電荷転送トランジスタ906間で分離する必要があり、レイアウト面積が増大する課題があった。

【0013】

本発明の目的は、各昇圧セルに使用されているスイッチング素子の基板バイアス効果を抑制するとともに、消費電流の抑制とレイアウト面積抑制とを可能とする昇圧回路を提供することにある。

【課題を解決するための手段】

【0014】

上記目的を達成するため、本発明による昇圧回路は、各昇圧セルのNウエルの電位を昇圧セル各段の入力電位又は出力電位に固定することにより、Nウエル-基板間の充放電電荷量を削減し、以て昇圧効率を向上させることとしたものである。

【0015】

具体的に説明すると、請求項1の発明では、基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セルを備えた昇圧回路において、N段($N \geq 1$)の前記昇圧セルから構成された第1の昇圧セル列と、M段($M \geq 1$)の前記昇圧セルから構成された第2の昇圧セル列と、前記第1の昇圧セル列のi段目($1 \leq i \leq N$)の前記昇圧セルの出力電位と、前記第2の昇圧セル列のi段目($1 \leq i \leq M$)の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列のi+1段目の前記昇圧セル又はi段目の前記昇圧セル又はi段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0016】

請求項2の発明では、基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路において、N段($N \geq$

1) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、各々前記第1の昇圧セル列のi段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第2の昇圧セル列のi段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又はi+1段目の前記昇圧セル又はi段目の前記昇圧セル又はi段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0017】

請求項3の発明では、請求項1又は2の発明に係る昇圧回路において、前記第2のウエル領域と前記第1の端子とが同電位となるように、前記第2のウエル領域と前記第1の端子とを互いに接続した。

【0018】

請求項4の発明では、請求項1又は2の発明に係る昇圧回路において、前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、かつ前記昇圧セルの各段毎に備えられている。

【0019】

請求項5の発明では、請求項1又は2の発明に係る昇圧回路において、前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、前記第1及び第2の昇圧セル列に1つ以上備えられ、かつ前記昇圧セルの任意の段数毎に備えられている。

【0020】

請求項6の発明では、請求項1又は2の発明に係る昇圧回路において、前記昇圧セルの前記第1の端子と前記第1のウエル領域との間にダイオード手段を備える。

【0021】

請求項7の発明では、請求項1又は2の発明に係る昇圧回路において、前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトを共通化した。

【0022】

請求項8の発明では、請求項1又は2の発明に係る昇圧回路において、前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の前記第1のウエル領域のレイアウトとを共通化した。

。【発明の効果】

【0023】

請求項1の発明によれば、第1導電型の第1のウエル領域の充放電電荷量をクロック信号信号の電圧スイングより小さくでき、見かけ上の第1のウエル領域－基板間の寄生容量を削減できるため、昇圧動作時の消費電流を抑制できる。また、見かけ上の第1のウエル領域－基板間の寄生容量を削減できるため、昇圧効率を向上できる。また、1つのアナログ比較回路で複数の昇圧セルの第1のウエル領域の電位を制御することで、アナログ比較回路によるレイアウト面積増大を抑制できる。

【0024】

請求項2の発明によれば、逆流防止回路の第1のウエル領域の電位制御も可能であり、逆流防止回路における電荷転送効率の低下を抑制することができる。

【0025】

請求項3の発明によれば、昇圧セル内の電荷転送トランジスタ（スイッチング素子）の入力端子と第2のウエル領域とを接続することで、基板バイアス効果によるスイッチング

素子の電流駆動能力低下を抑制することができる。

【0026】

請求項4の発明によれば、全ての段にアナログ比較回路を備えることで、昇圧セルの寄生容量を同一にし、設計容易性を向上することができる。

【0027】

請求項5の発明によれば、任意の段数にアナログ比較回路を備えることで、第2のウエル領域と第1のウエル領域との耐圧マージンを確保した上で、回路面積増大を抑制することができる。

【0028】

請求項6の発明によれば、ダイオード手段を介して第1のウエル領域に昇圧セルの入力電圧を供給することで、昇圧回路起動時に第1のウエル領域の電位上昇を各昇圧セル電位に追従させ、ラッチアップ発生を抑制することができる。

【0029】

請求項7及び8の発明によれば、第1のウエル領域のレイアウトを共通化することでレイアウト面積を削減することができる。

【発明を実施するための最良の形態】

【0030】

以下、本発明の実施の形態による昇圧回路について、図面を参照しながら説明する。

【0031】

図1は、本発明に係る昇圧回路の構成例を示している。図1において、101は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで出力端子電圧（昇圧電圧）V_{pump}を発生する2並列の昇圧回路である。102、103、104、105、106、107は第1列と第2列との構成を持ち、第1列の奇数段目にはCLK1が入力され、第1列の偶数段目にはCLK2が入力され、第2列の奇数段目にCLK2が入力され、第2列の偶数段目にはCLK1が入力される昇圧セル、108、109は昇圧電圧V_{pump}の逆流を防止する逆流防止回路、110、111、112、113、114、115、116は昇圧セル102～107の入出力端子、117、118、119は第1列と第2列との同じ段の昇圧セルの各々の入出力端子の電圧のうち低い側の電圧を出力する低電圧出力アナログ比較回路の一例であり、120、121は低電圧出力アナログ比較回路117、118、119に用いられるNch（Nチャネル）トランジスタ、122、123、124は各昇圧セルのNウエルに接続された低電圧出力アナログ比較回路117～119の出力端子、125は第1列の3段目の昇圧セル104と第2列の3段目の昇圧セル107との各々の入出力端子113、116の電圧のうち高い側の電圧を出力する高電圧出力アナログ比較回路の一例であり、126、127は高電圧出力アナログ比較回路125に用いられるPch（Pチャネル）トランジスタ、128は逆流防止回路108、109のNウエルに接続された高電圧出力アナログ比較回路の出力端子である。なお、従来例と同一符号の要素は、従来例と同様であることを示す。また、本昇圧回路101の直列接続数は一例である。

【0032】

図1の昇圧回路101における2相クロック信号CLK1、CLK2の波形は、図14と同様である。図14を用いて、図1の昇圧回路101の動作を説明する。

【0033】

時刻T1の状態ではCLK1が“L”から“H”へ遷移し、CLK2が“H”から“L”へと遷移すると、昇圧セル102、104、106の入出力端子111、113、115の電位が昇圧され、昇圧された電荷は、昇圧セル103、逆流防止回路108、昇圧セル107の各々の電荷転送トランジスタ906を介して入出力端子112、昇圧回路101の出力端子、入出力端子116にそれぞれ転送される。このとき、低電圧出力アナログ比較回路117は、昇圧された入出力端子111と昇圧されていない入出力端子114との電位の関係により、Nchトランジスタ120はオフ状態、Nchトランジスタ121はオン状態となり、低電圧出力アナログ比較回路117の出力端子122には入出力端子1

14の電位が出力されて、昇圧セル102と昇圧セル105とのNウエルに供給される。同様に、低電圧出力アナログ比較回路118の出力端子123には入出力端子112の電位が出力されて、昇圧セル103と昇圧セル106とのNウエルに供給され、低電圧出力アナログ比較回路119の出力端子124には入出力端子116の電位が出力されて、昇圧セル104と昇圧セル107とのNウエルに供給される。また、高電圧出力アナログ比較回路125は、昇圧された入出力端子113と昇圧されていない入出力端子116との電位の関係により、Pchトランジスタ126はオン状態、Pchトランジスタ127はオフ状態となり、高電圧出力アナログ比較回路125の出力端子128には入出力端子113の電位が出力されて、逆流防止回路108と逆流防止回路109とのNウエルに供給される。

【0034】

時刻T2の状態 CLK1が“H”から“L”へ遷移し、CLK2が“L”から“H”へと遷移すると、昇圧セル103、105、107の入出力端子112、114、116の電位が昇圧され、昇圧された電荷は、昇圧セル104、106、逆流防止回路109の各々の電荷転送トランジスタ906を介して入出力端子113、115、昇圧回路101の出力端子にそれぞれ転送される。このとき、低電圧出力アナログ比較回路117は、昇圧された入出力端子114と昇圧されていない入出力端子111との電位の関係により、Nchトランジスタ120はオン状態、Nchトランジスタ121はオフ状態となり、低電圧出力アナログ比較回路117の出力端子122には入出力端子111の電位が出力されて、昇圧セル102と昇圧セル105とのNウエルに供給される。同様に、低電圧出力アナログ比較回路118の出力端子123には入出力端子115の電位が出力されて、昇圧セル103と昇圧セル106とのNウエルに供給され、低電圧出力アナログ比較回路119の出力端子124には入出力端子113の電位が出力されて、昇圧セル104と昇圧セル107とのNウエルに供給される。また、高電圧出力アナログ比較回路125は、昇圧された入出力端子116と昇圧されていない入出力端子113との電位の関係により、Pchトランジスタ126はオフ状態、Pchトランジスタ127はオン状態となり、高電圧出力アナログ比較回路125の出力端子128には入出力端子116の電位が出力されて、逆流防止回路108と逆流防止回路109とのNウエルに供給される。

【0035】

このように、図1の昇圧回路101によれば、各昇圧セル102～107及び各逆流防止回路108、109のNウエルの電位を昇圧セル各段の入力電位又は出力電位に固定することが可能となり、Nウエルー基板間の充放電電荷量を削減し、消費電流の削減が可能となる。また、Nウエルー基板間の充放電電荷量を削減することで次段へ転送される電荷量を増やすことが可能となり、昇圧効率の向上が期待できる。

【0036】

なお、図2、図3に示すように、低電圧出力アナログ比較回路117～119及び高電圧出力アナログ比較回路125は、PウエルーNウエルの耐圧マージン及び回路面積を考慮して、任意の段数の昇圧セルに対して設けることが可能であり、素子数を削減したうえでも上記に示す構成と同様の効果を有することができる。

【0037】

図4は、本発明に係る昇圧回路の更に他の構成例を示している。図4において、701は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで昇圧電圧V_{pump}を発生する2並列の昇圧回路である。702、703、704、705、706、707は、図1の昇圧セル102～107に対して、各昇圧セルの入出力端子と高電圧出力アナログ比較回路125の出力端子128との間にダイオード接続されたトランジスタ710を追加したものである。708、709は逆流防止回路である。なお、図1と同一符号は、それらと同様であることを示す。また、本昇圧回路701の直列接続数は一例である。

【0038】

図1との差分として、図4の構成では、低電圧（又は高電圧）出力アナログ比較回路1

117～119, 125を共通化し、素子数を削減している。これにより、昇圧回路701の起動時、各昇圧セル702～707の入出力端子111～116の電位が上昇する際、Nウエル電位は各昇圧セル702～707のPウエル907より寄生ダイオード909の順方向電流として供給されることとなる。この寄生ダイオード909の順方向電流を抑制するために、ダイオード機能を有するトランジスタ710を備えることで、昇圧回路701の起動時においても安定した昇圧動作が可能となる。

【0039】

以上、昇圧回路構成として、2相クロック信号CLK1, CLK2を用いる昇圧回路を例としたが、図5に示す4相クロック信号CLK1, CLK2, CLK3, CLK4を用いた昇圧回路801や、図6、図7に示すような2相クロック信号CLK1, CLK2を用いた昇圧回路851, 881等、昇圧セルにトリプルウエルのNchトランジスタを使用している場合には、低電圧出力アナログ比較回路117～119又は高電圧出力アナログ比較回路125を用いることで、昇圧セルの構成にかかわらず同様の効果を有することが可能である。なお、図5において、802, 803, 804, 805, 806, 807は昇圧セル、808, 809は逆流防止回路、810は電荷転送トランジスタ(Nchトランジスタ)、811, 813はNchトランジスタ、812は昇圧容量である。また、図6において、852, 853, 854, 855, 856, 857は昇圧セル、858, 859は逆流防止回路、860は電荷転送トランジスタ(Nchトランジスタ)、861, 863はNchトランジスタ、862はPchトランジスタである。

【0040】

また、図示の低電圧出力アナログ比較回路117～119及び高電圧出力アナログ比較回路125の構成は一例であり、同様の機能を有するものであればよい。

【0041】

図8は、本発明に係る昇圧回路におけるレイアウト構成例を示す平面図であり、図1で示した昇圧セル102～107の電荷転送トランジスタ906と低電圧出力アナログ比較回路117～119とを図示している。

【0042】

図8より、低電圧出力アナログ比較回路117(又は118, 119)の出力端子122(又は123, 124)は、昇圧セル102と105(又は103と106、又は104と107)の電荷転送トランジスタ906のNウエル(NT)に接続され、かつ、当該Nウエルは2つの昇圧セル102, 105の電荷転送トランジスタ906に対して共通にレイアウトされている。

【0043】

図8によれば、低電圧出力アナログ比較回路117の出力電圧により制御される2つ以上の昇圧セル102, 105内に存在するトリプルウエル構造のスイッチング素子906において、Nウエルを共通にレイアウトすることが可能となり、レイアウト面積を削減することができる。

【0044】

なお、図8のレイアウト構成は一例であり、図9、図10のように、低電圧出力アナログ比較回路118の出力電圧により制御されるスイッチング素子906のNウエルのレイアウトを昇圧セルの段数に関係なく任意に分離、共通化することができる。

【0045】

更に、図11、図12のように、低電圧出力アナログ比較回路117～119のNウエルも昇圧セル102～107のスイッチング素子906のNウエルと共通にレイアウトすることが可能である。これらは、高電圧出力アナログ比較回路125においても同様のレイアウトが可能である。

【産業上の利用可能性】

【0046】

以上説明してきたとおり、本発明に係る昇圧回路は、昇圧セルを構成するトリプルウエル構造の素子において、基板バイアス効果を抑制したうえで、消費電流の削減、回路面積

、レイアウト面積を削減できる特徴を有し、不揮発性半導体記憶装置、CMOSプロセスでのアナログ回路特性改善のための電源発生回路等として有用である。

【0047】

また、DRAM等の揮発性半導体記憶装置、液晶装置、携帯機器の電源回路等の用途にも応用できる。

【図面の簡単な説明】

【0048】

【図1】本発明に係る昇圧回路の構成例を示す回路図である。

【図2】本発明に係る昇圧回路の他の構成例を示す回路図である。

【図3】本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図4】本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図5】本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図6】本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図7】本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図8】本発明に係る昇圧回路におけるレイアウト構成例を示す平面図である。

【図9】本発明に係る昇圧回路における他のレイアウト構成例を示す平面図である。

【図10】本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図11】本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図12】本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図13】従来の昇圧回路の例を示す回路図である。

【図14】図13の昇圧回路における2相クロック信号の波形図である。

【符号の説明】

【0049】

101, 201, 301 昇圧回路

102～107 昇圧セル

108, 109 逆流防止回路

110～116 昇圧セルの入出力端子

117～119 低電圧出力アナログ比較回路

120, 121 Nchトランジスタ

122～124 低電圧出力アナログ比較回路の出力端子

125 高電圧出力アナログ比較回路

126, 127 Pchトランジスタ

128 高電圧出力アナログ比較回路の出力端子

701 昇圧回路

702～707 昇圧セル

708, 709 逆流防止回路

710 ダイオード接続トランジスタ

801 昇圧回路

802～807 昇圧セル

808, 809 逆流防止回路

810 電荷転送トランジスタ (Nchトランジスタ)

811, 813 Nchトランジスタ

812 昇圧容量

851, 881 昇圧回路

852～857 昇圧セル

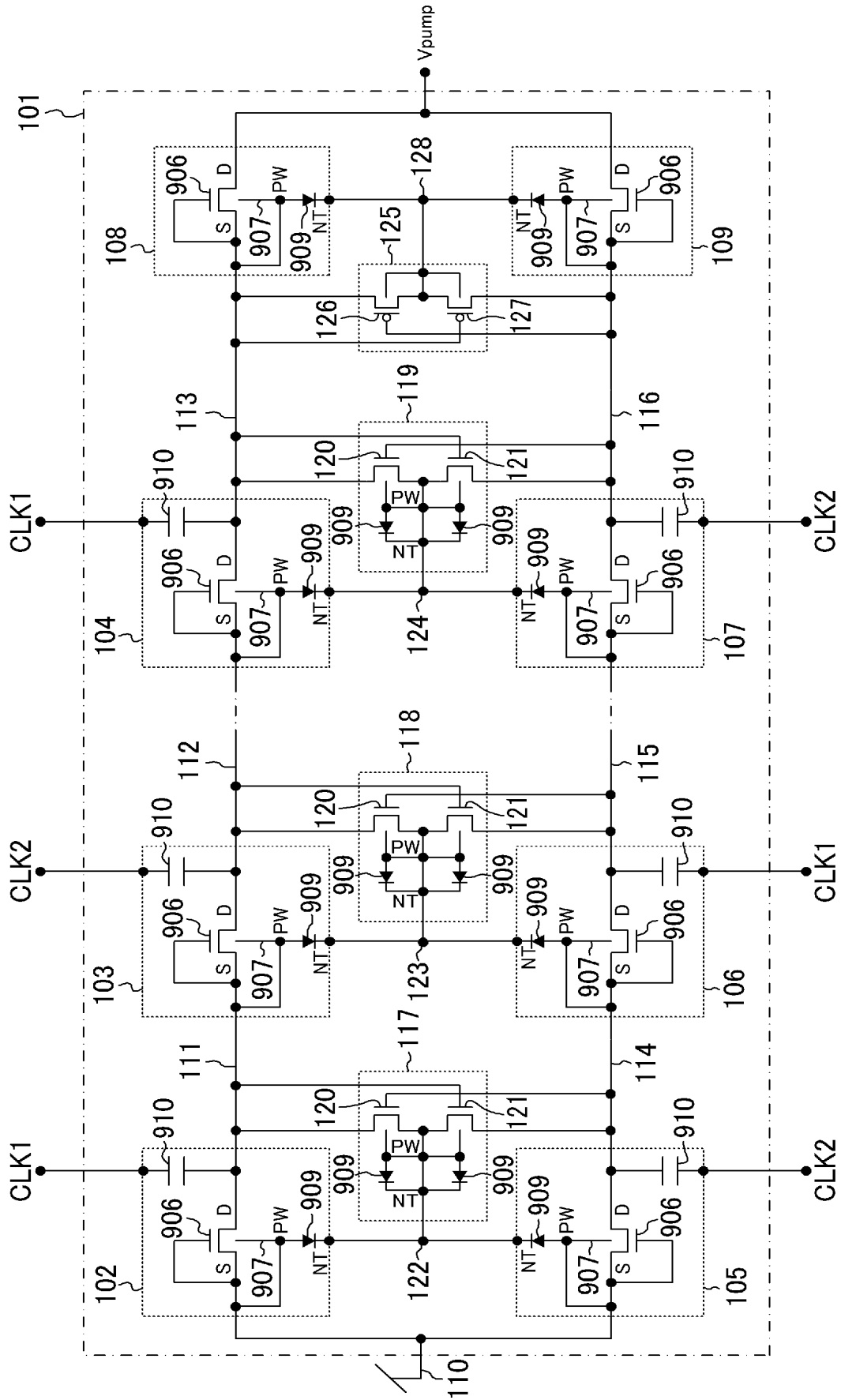
858, 859 逆流防止回路

860 電荷転送トランジスタ (Nchトランジスタ)

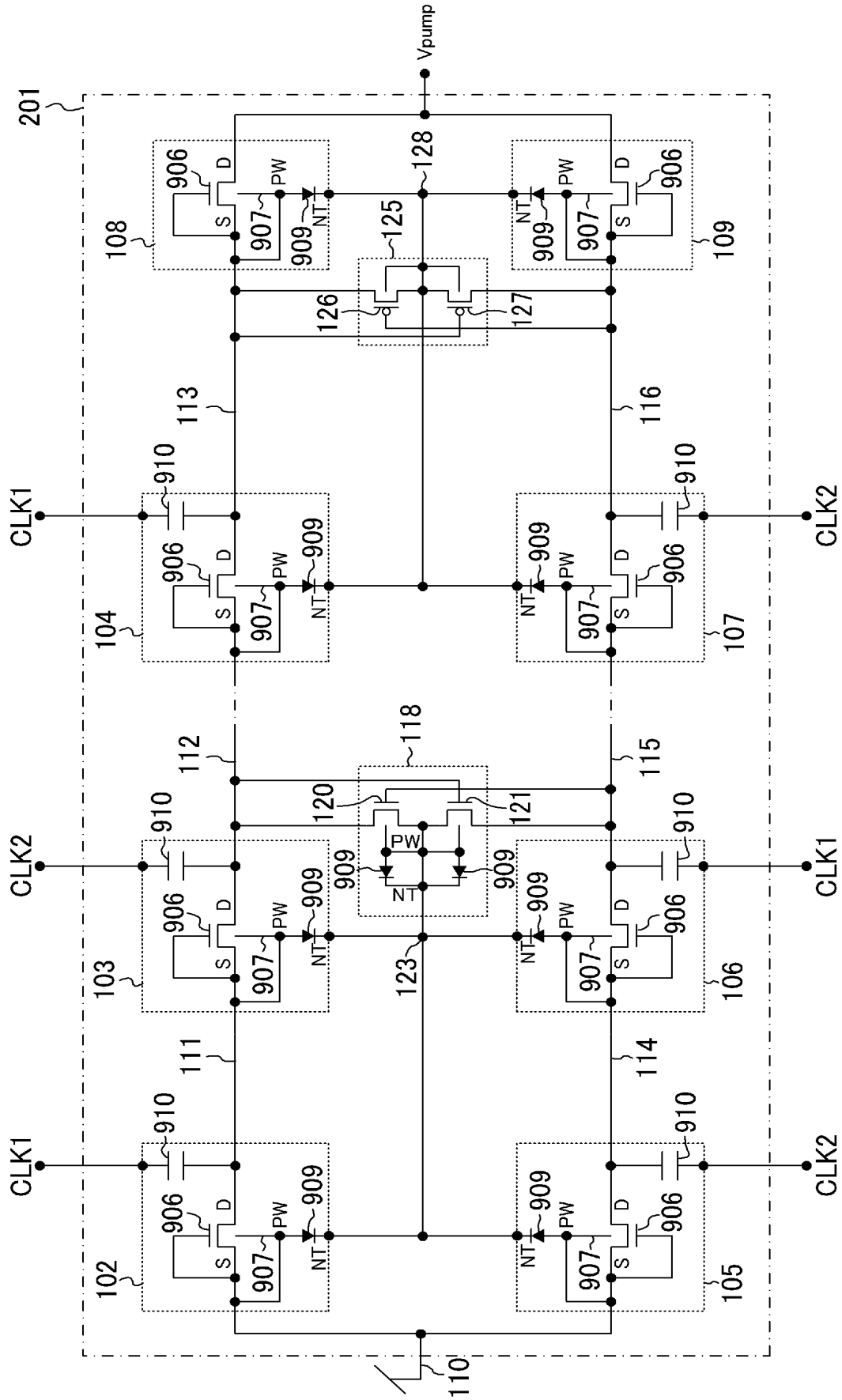
861, 863 Nchトランジスタ
862 Pchトランジスタ
901 昇圧回路
902~904 昇圧セル
905 逆流防止回路
906 電荷転送トランジスタ (Nchトランジスタ)
907 Pウエル (PW)
908 Nウエル (NT)
909 PウエルとNウエルとの間の寄生ダイオード
910 昇圧容量
911~914 昇圧セルの入出力端子
CLK1~CLK4 クロック信号
Ttrans 電荷転送期間
Vpump 出力端子電圧 (昇圧電圧)

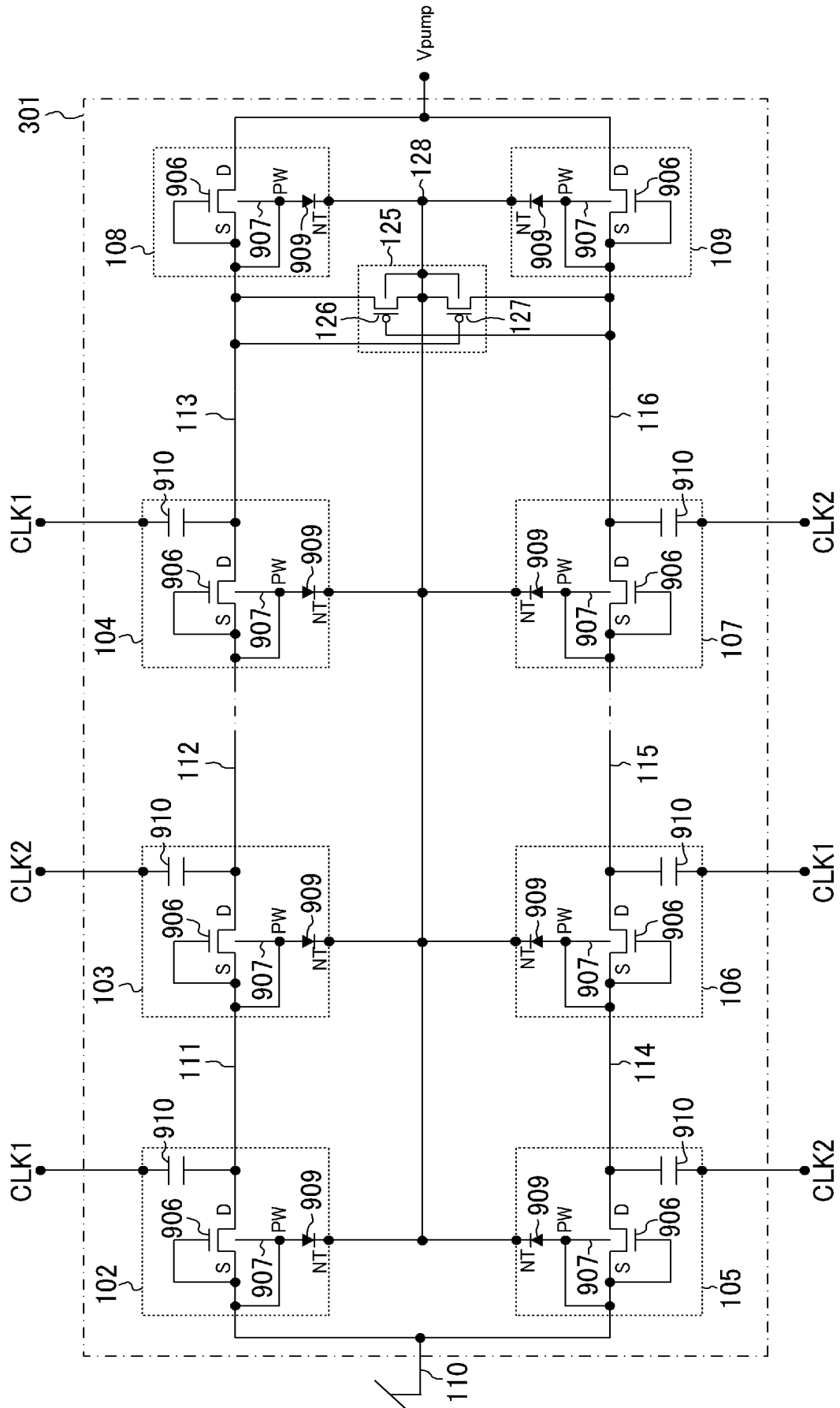
【書類名】 図面

【図 1】

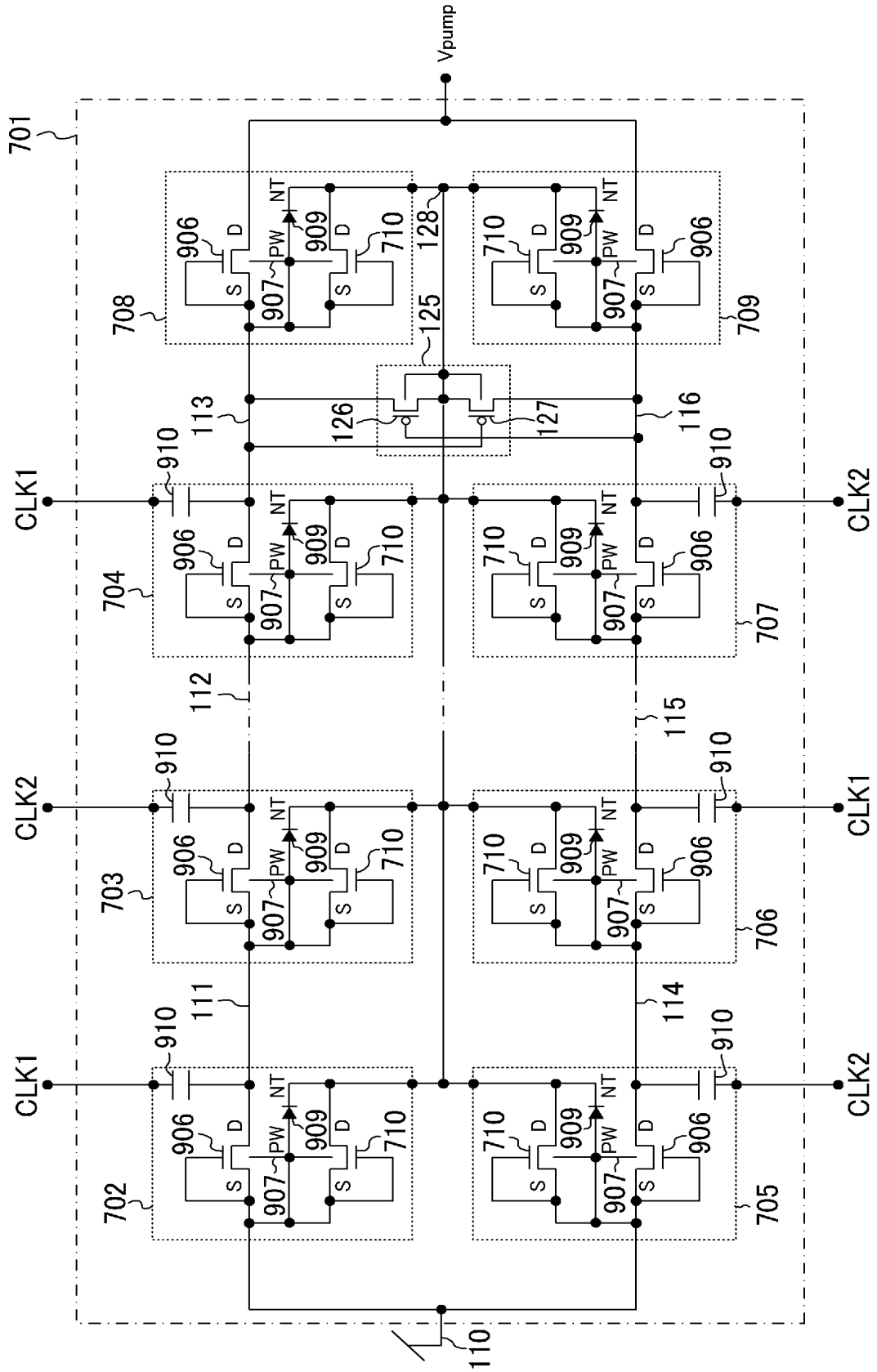


【図 2】

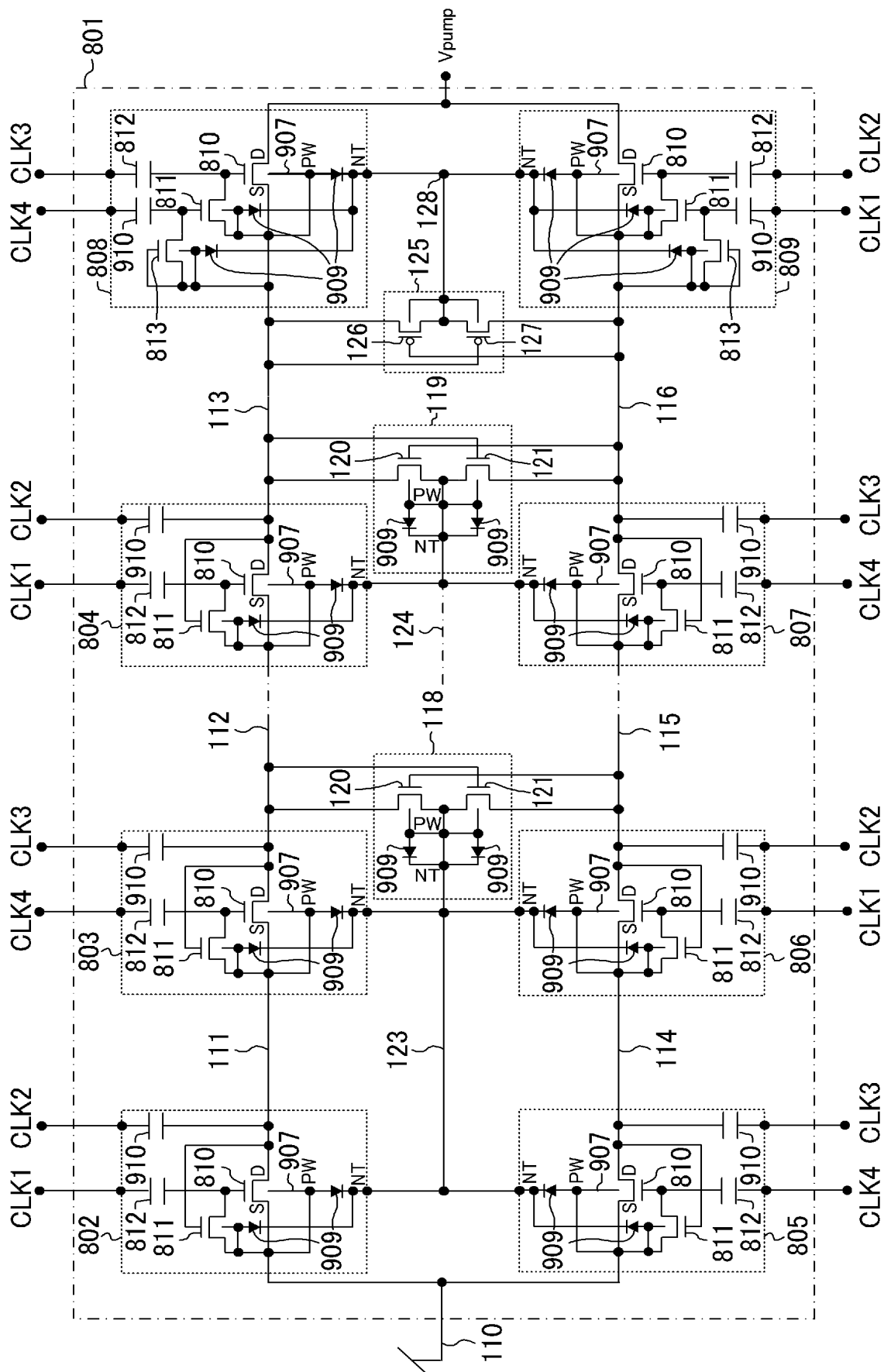




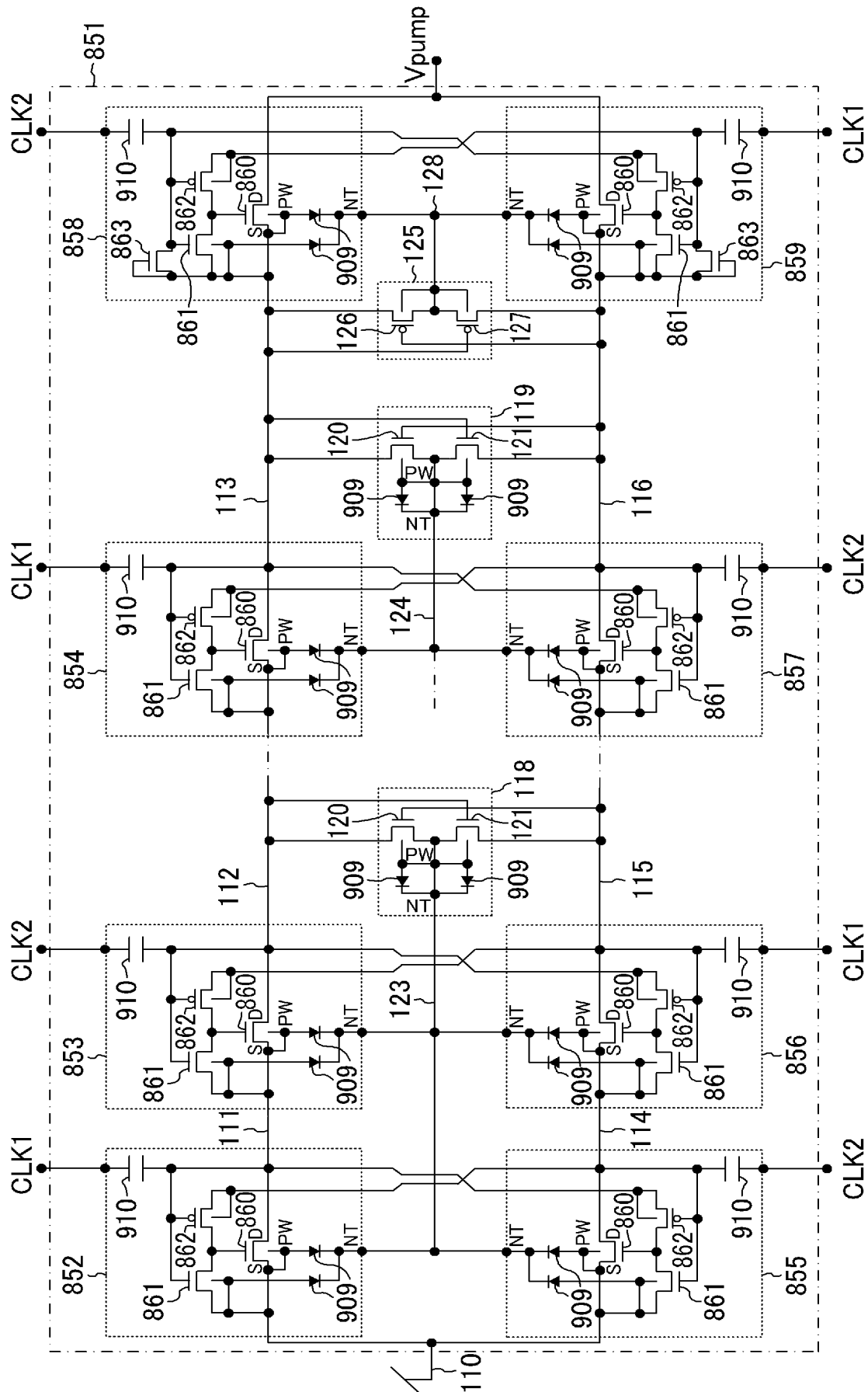
【図4】

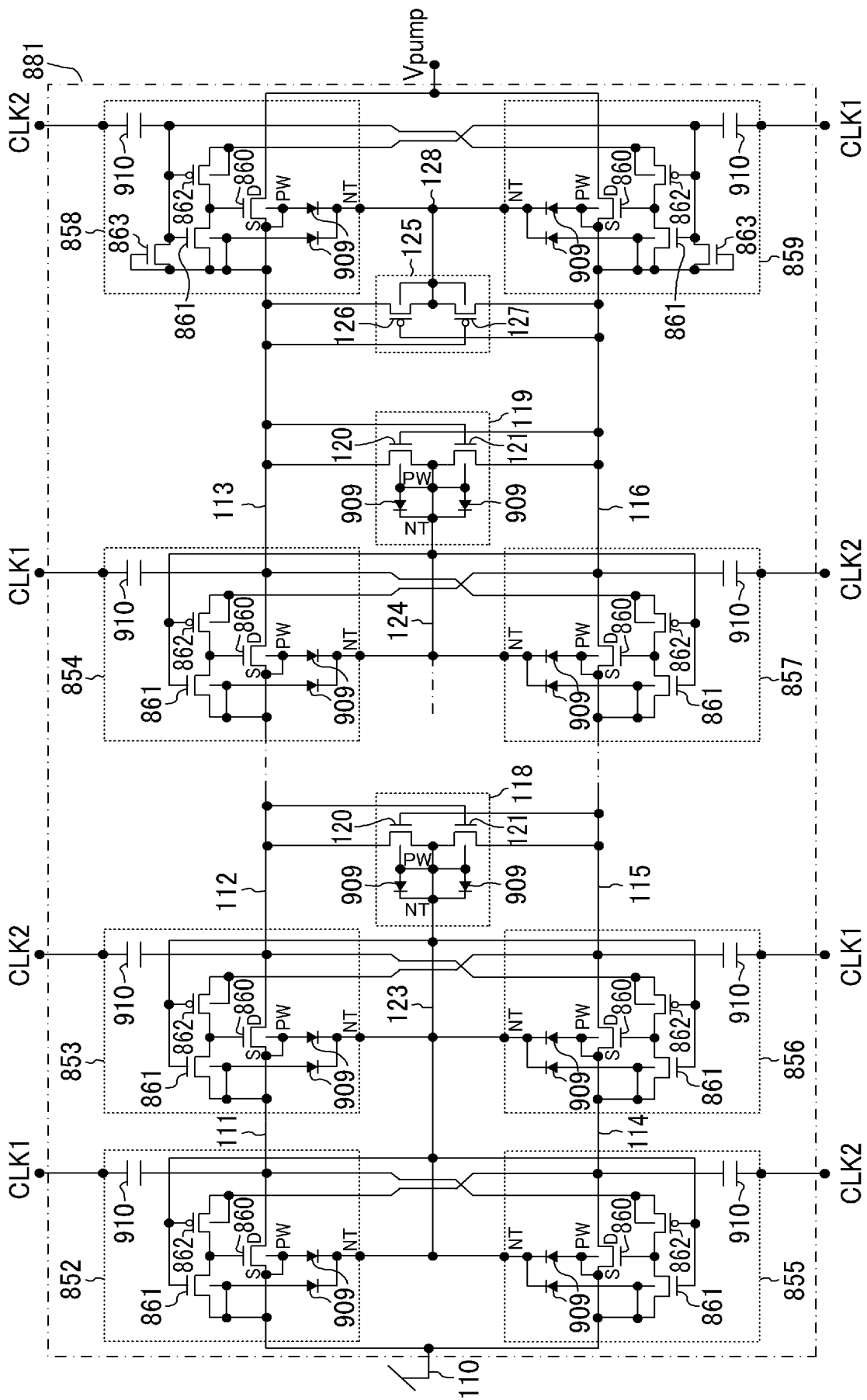


【図 5】

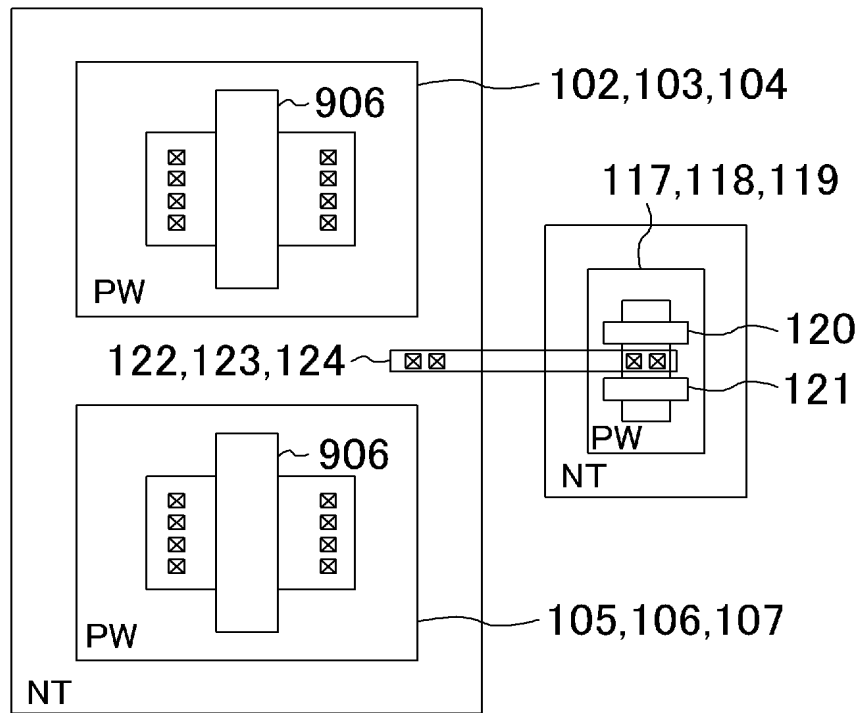


【図 6】

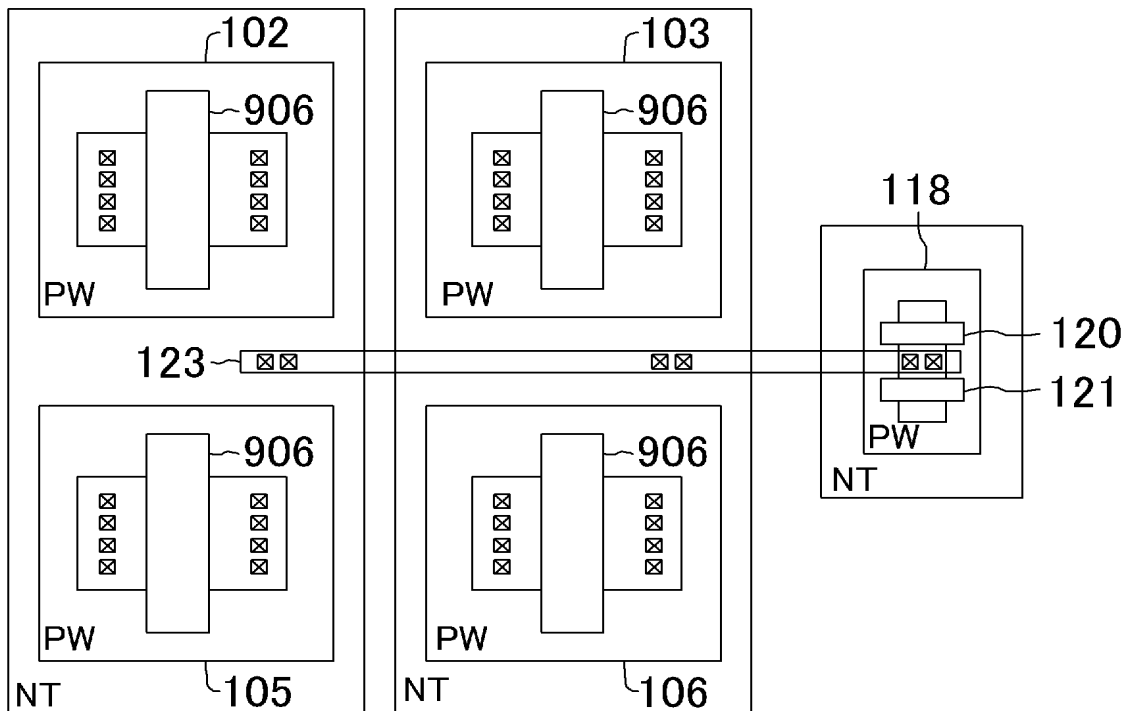




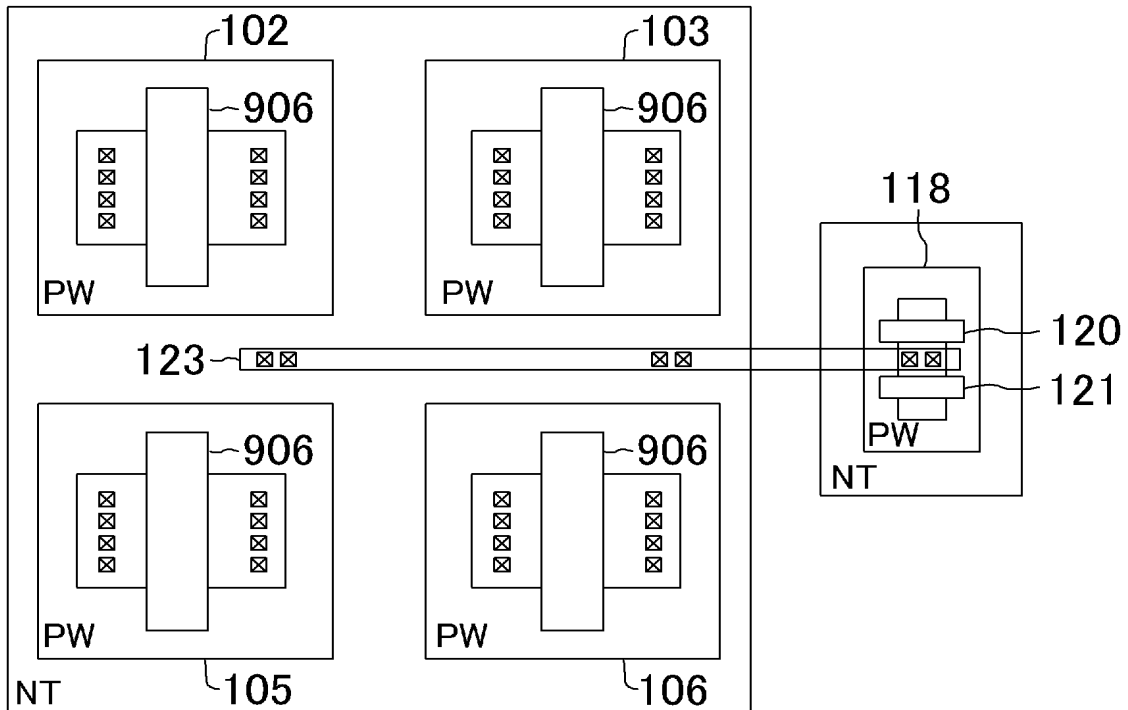
【図 8】



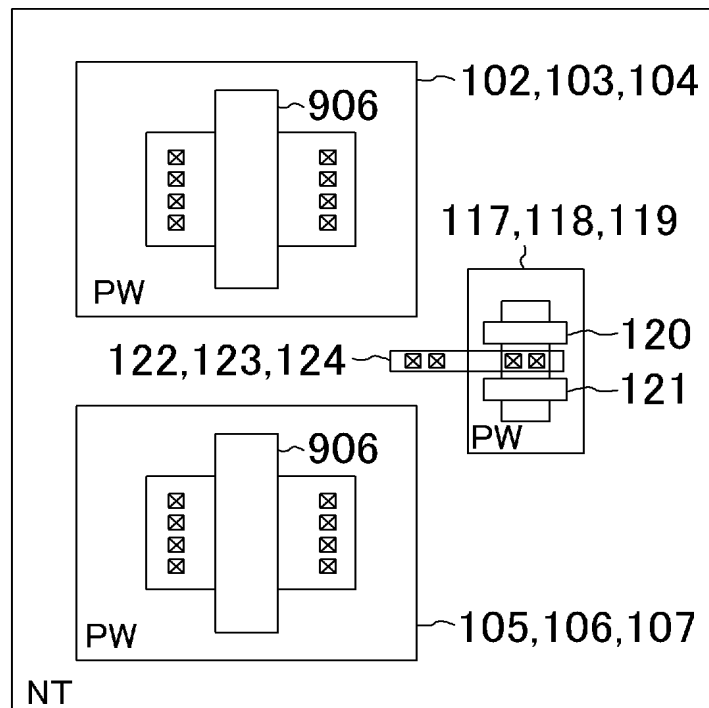
【図 9】



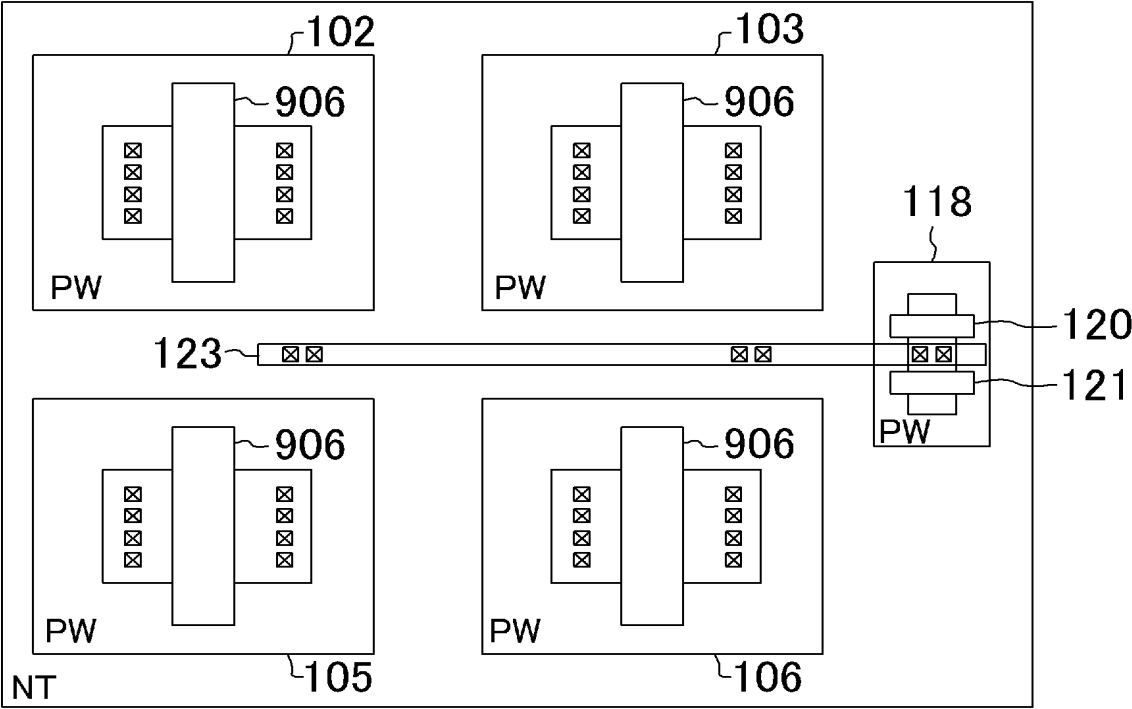
【図 10】



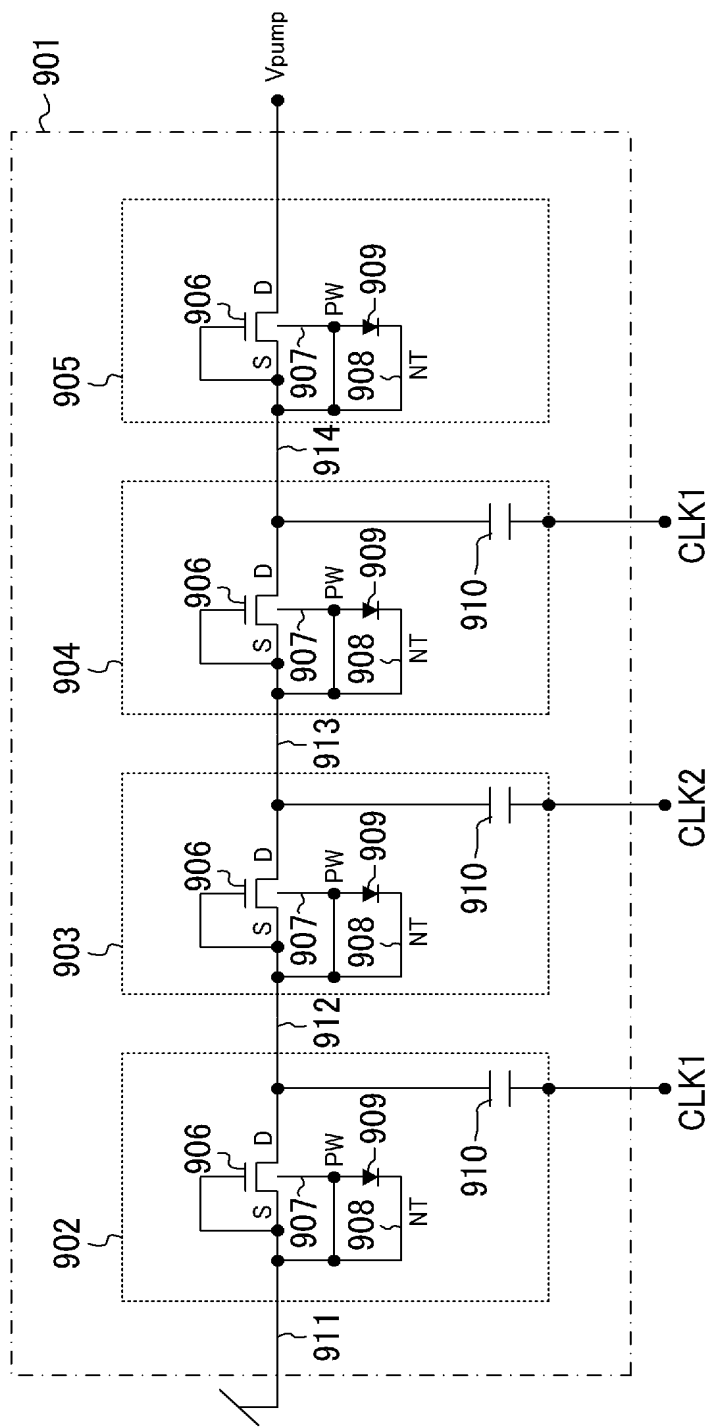
【図 11】



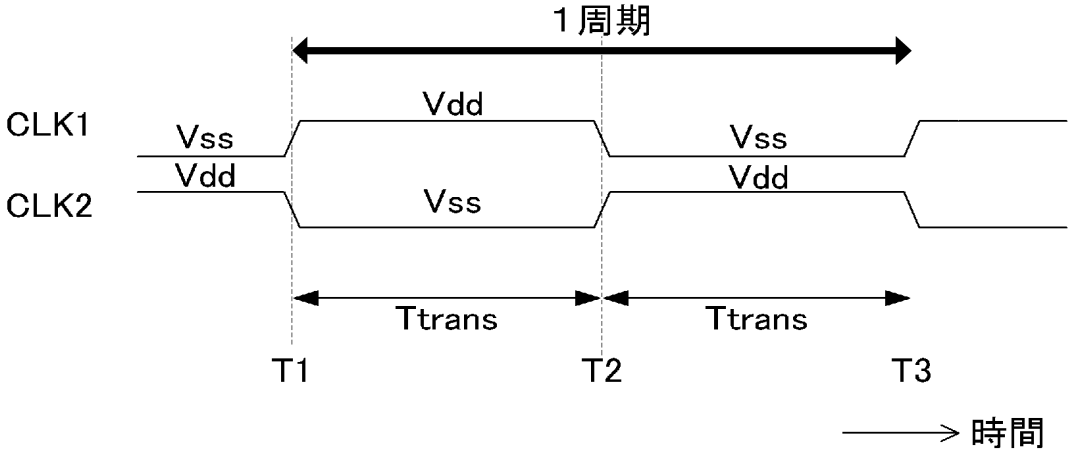
【図 1 2】



【图 1 3】



【図 1 4】



【書類名】 要約書

【要約】

【課題】 電荷転送効率の低下を抑制し、トリプルウエル構造を持つスイッチング素子のNウエル電位を制御することで、低消費電力化とレイアウト面積削減とを可能とする。

【解決手段】 第1の昇圧セル列102, 103, 104と、第2の昇圧セル列105, 106, 107とを備え、各々の昇圧セルの同じ段の電位を比較し、低い側の電位又は高い側の電位を選択して出力するアナログ比較回路117, 118, 119を更に備え、これらアナログ比較回路の出力電位により、Nウエル（NT）の電位を制御する。これにより、Nウエル電位の振幅を抑制し、かつNウエル領域のレイアウトの共通化を可能とする。

【選択図】 図1

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JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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The country code and number
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to be used for filing abroad
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J P 2007-307064

出 願 人

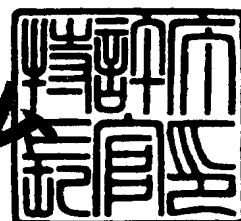
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2010年 7月29日

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【物件名】 明細書 1

【物件名】 図面 1

【物件名】 要約書 1

【包括委任状番号】 0505962

【書類名】 特許請求の範囲

【請求項 1】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内と前記第 2 のウエル領域内とのうちいずれか一方又は両方に 1 つ以上のスイッチング素子を備えて、前記 1 つ以上のスイッチング素子により第 1 の端子と第 2 の端子との間をオン・オフして前記第 1 の端子から前記第 2 の端子へ電荷を転送する昇圧セルを備えた昇圧回路であって、

N 段 ($N \geq 1$) の前記昇圧セルから構成された第 1 の昇圧セル列と、

M 段 ($M \geq 1$) の前記昇圧セルから構成された第 2 の昇圧セル列と、

前記第 1 の昇圧セル列の i 段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第 2 の昇圧セル列の i 段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第 1 及び第 2 の昇圧セル列の $i + 1$ 段目の前記昇圧セル又は i 段目の前記昇圧セル又は i 段目より前段の前記昇圧セルのうちの 1 つ以上に備えられた前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域に印加することを特徴とする昇圧回路。

【請求項 2】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内と前記第 2 のウエル領域内とのうちいずれか一方又は両方に 1 つ以上のスイッチング素子を備えて、前記 1 つ以上のスイッチング素子により第 1 の端子と第 2 の端子との間をオン・オフして前記第 1 の端子から前記第 2 の端子へ電荷を転送する昇圧セルを備えた昇圧回路であって、

N 段 ($N \geq 1$) の前記昇圧セルから構成された第 1 の昇圧セル列と、

M 段 ($M \geq 1$) の前記昇圧セルから構成された第 2 の昇圧セル列と、

前記第 1 の昇圧セル列の i 段目 ($1 \leq i \leq N$) の前記昇圧セルの入力電位と、前記第 2 の昇圧セル列の i 段目 ($1 \leq i \leq M$) の前記昇圧セルの入力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第 1 及び第 2 の昇圧セル列の $i + 1$ 段目の前記昇圧セル又は i 段目の前記昇圧セル又は i 段目より前段の前記昇圧セルのうちの 1 つ以上に備えられた前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域に印加することを特徴とする昇圧回路。

【請求項 3】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型の第 2 のウエル領域を有し、前記第 1 のウエル領域内と前記第 2 のウエル領域内とのうちいずれか一方又は両方に 1 つ以上のスイッチング素子を備えて、前記 1 つ以上のスイッチング素子により第 1 の端子と第 2 の端子との間をオン・オフして前記第 1 の端子から前記第 2 の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路であって、

N 段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第 1 の昇圧セル列と、

M 段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第 2 の昇圧セル列と、

各々前記第 1 の昇圧セル列の i 段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第 2 の昇圧セル列の i 段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第 1 及び第 2 の昇圧セル列の前記逆流防止回路又は $i + 1$ 段目の前記昇圧セル又は i 段目の前記昇圧セル又は i 段目より前段の前記昇圧セルのうちの 1 つ以上に備えられた前記 1 つ以上のスイッチング素子の前記第 1 のウエル領域に印加することを特徴とする昇圧回路。

【請求項 4】

基板上に第 1 導電型の第 1 のウエル領域を有し、前記第 1 のウエル領域内に第 2 導電型

の第2のウエル領域を有し、前記第1のウエル領域内と前記第2のウエル領域内とのうちいずれか一方又は両方に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路であって、

N段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、

M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、

各々前記第1の昇圧セル列の逆流防止回路の中間電位と、前記第2の昇圧セル列の逆流防止回路の中間電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又は前記第1の昇圧セル列及び前記第2の昇圧セル列に含まれる前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することを特徴とする昇圧回路。

【請求項5】

基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内と前記第2のウエル領域内とのうちいずれか一方又は両方に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路であって、

N段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、

M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、

各々前記第1及び第2の昇圧セル列の*i*段目 ($1 \leq i \leq N$) の前記昇圧セル同士又は逆流防止回路同士の入力電位を比較し、前記入力電位のうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、

前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又は*i*+1段目の前記昇圧セル又は*i*段目の前記昇圧セル又は*i*段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することを特徴とする昇圧回路。

【請求項6】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記第2のウエル領域と前記第1の端子とが同電位となるように、前記第2のウエル領域と前記第1の端子とが互いに接続されたことを特徴とする昇圧回路。

【請求項7】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記第2のウエル領域と前記第1のウエル領域とが同電位となるように、前記第2のウエル領域と前記第1のウエル領域とが互いに接続されたことを特徴とする昇圧回路。

【請求項8】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、かつ前記昇圧セルの各段毎に備えられていることを特徴とする昇圧回路。

【請求項9】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は

前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、前記第1及び第2の昇圧セル列に1つ以上備えられ、かつ前記昇圧セルの任意の段数毎に備えられていることを特徴とする昇圧回路。

【請求項10】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記昇圧セルの前記第1の端子と前記1のウエル領域との間にダイオード手段を備えたことを特徴とする昇圧回路。

【請求項11】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記第1及び第2の昇圧セル列の前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトを共通化したことを特徴とする昇圧回路。

【請求項12】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記第1及び第2の昇圧セル列の前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の前記第1のウエル領域のレイアウトとを共通化したことを特徴とする昇圧回路。

【請求項13】

請求項1～5のいずれか1項に記載の昇圧回路において、

前記第1の昇圧セル列の*i*段目の昇圧セルの前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の第1の素子の前記第1のウエル領域のレイアウトとを共通化し、

前記第2の昇圧セル列の*i*段目の昇圧セルの前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の第2の素子の前記第1のウエル領域のレイアウトとを共通化したことを特徴とする昇圧回路。

【書類名】明細書

【発明の名称】昇圧回路

【技術分野】

【0001】

本発明は、トリプルウエル構造のスイッチング素子を利用した昇圧回路に関するものである。

【背景技術】

【0002】

近年、不揮発性半導体記憶装置の1つであるフラッシュメモリにおいては、単一電源電圧又は低い電源電圧でのデータの読み出し、データの書き換えが要求されており、各動作を実施する際にオンチップで正又は負の昇圧電圧を供給する昇圧回路が必要とされている。また、CMOSプロセスにおいても昇圧回路で発生された電源電圧がアナログ回路の特性改善に用いられている。

【0003】

従来、トリプルウエル構造のスイッチング素子を利用した昇圧回路が知られている（特許文献1～3参照）。

【0004】

図25は、従来の昇圧回路の例を示している。図25において、901は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで出力端子電圧（昇圧電圧）V_{pump}を発生する昇圧回路である。902、903、904は3段の構成例であり、奇数段目にCLK1が入力され、偶数段目にCLK2が入力される昇圧セル、905は昇圧電圧V_{pump}の逆流を防止する逆流防止回路、906はスイッチング素子として機能する電荷転送トランジスタ、907は電荷転送トランジスタ906のPウエル（PW）、908は当該Pウエル907を含む深いNウエル（NT）、909はPウエル907とNウエル908との間の寄生ダイオード、910は昇圧セル902、903、904の出力端子を昇圧する昇圧容量であり、911、912、913、914は昇圧セルの入出力端子である。図25に示すとおり、昇圧セル902～904の各電荷転送トランジスタ906のPウエル907とNウエル908とを各電荷転送トランジスタ906のソースと接続し、これらを同電位にしている。

【0005】

図26は、図25の昇圧回路901における2相クロック信号CLK1、CLK2の波形図である。図26を用いて、図25の昇圧回路901の動作を簡単に説明する。

【0006】

まず、時刻T1の状態では、CLK1が“H”（電源電圧V_{dd}）、CLK2が“L”（接地電圧V_{ss}）となり、入出力端子912、914の電位が昇圧される。同時に、昇圧セル903及び逆流防止回路905の各々の電荷転送トランジスタ906を介して、入出力端子912から入出力端子913へ、また入出力端子914から昇圧回路901の出力端子へそれぞれ電荷が転送され、入出力端子913及び昇圧回路901の出力端子電圧V_{pump}がそれぞれ上昇する。このとき、昇圧セル903及び逆流防止回路905の各々のPウエル907を電荷転送トランジスタ906のソース端子と同電位としているので、電荷転送トランジスタ906の基板バイアス効果を抑制し、電荷転送効率の低下を抑制することができる。

【0007】

時刻T1から電荷転送期間T_{trans}が経過して時刻T2の状態になると、CLK2が“H”、CLK1が“L”となり、入出力端子913の電位が昇圧される。同時に、昇圧セル904の電荷転送トランジスタ906を介して、入出力端子913から入出力端子914へ電荷が転送される。このとき、昇圧セル904のPウエル907を電荷転送トランジスタ906のソース端子と同電位としているので、電荷転送トランジスタ906の基板バイアス効果を抑制し、電荷転送効率の低下を抑制することができる。

【0008】

時刻T3の状態になると、時刻T1と同様の動作となる。

【0009】

以上のとおり、図25の昇圧回路901によれば、基板バイアス効果を抑制し、昇圧動作時の電荷転送効率の低下を抑制することができる。

【特許文献1】特開平8-125133号公報

【特許文献2】特開平11-283392号公報

【特許文献3】米国特許第6100557号明細書

【発明の開示】

【発明が解決しようとする課題】

【0010】

しかしながら、上記従来の昇圧回路901は、電荷転送トランジスタ906のソースとNウェル908とを接続するため、クロック信号CLK1、CLK2の電圧遷移に応じて、Nウェル908が形成する寄生容量をクロック信号CLK1、CLK2の電圧遷移幅で充放電する結果、消費電流が増加する課題があった。

【0011】

また、クロック信号CLK1、CLK2で供給する電荷をNウェル908の充放電電荷として使用するため、昇圧効率が低下する課題があった。

【0012】

また、電荷転送トランジスタ906のソースとNウェル908とを接続するため、Nウェル908を各電荷転送トランジスタ906間で分離する必要があり、レイアウト面積が増大する課題があった。

【0013】

本発明の目的は、各昇圧セルに使用されているスイッチング素子の基板バイアス効果を抑制するとともに、消費電流の抑制とレイアウト面積抑制とを可能とする昇圧回路を提供することにある。

【課題を解決するための手段】

【0014】

上記目的を達成するため、本発明による昇圧回路は、各昇圧セルのNウェルの電位を昇圧セル各段の入力電位又は出力電位に固定することにより、Nウェル-基板間の充放電電荷量を削減し、以て昇圧効率を向上させることとしたものである。

【0015】

具体的に説明すると、請求項1の発明では、基板上に第1導電型の第1のウェル領域を有し、前記第1のウェル領域内に第2導電型の第2のウェル領域を有し、前記第1のウェル領域内又は前記第2のウェル領域内に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セルを備えた昇圧回路において、N段($N \geq 1$)の前記昇圧セルから構成された第1の昇圧セル列と、M段($M \geq 1$)の前記昇圧セルから構成された第2の昇圧セル列と、前記第1の昇圧セル列のi段目($1 \leq i \leq N$)の前記昇圧セルの出力電位と、前記第2の昇圧セル列のi段目($1 \leq i \leq M$)の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列のi+1段目の前記昇圧セル又はi段目の前記昇圧セル又はi段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウェル領域に印加することとした。

【0016】

請求項2の発明では、基板上に第1導電型の第1のウェル領域を有し、前記第1のウェル領域内に第2導電型の第2のウェル領域を有し、前記第1のウェル領域内と前記第2のウェル領域内とのうちいずれか一方又は両方に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セルを備えた昇圧回路において、

N段 ($N \geq 1$) の前記昇圧セルから構成された第1の昇圧セル列と、M段 ($M \geq 1$) の前記昇圧セルから構成された第2の昇圧セル列と、前記第1の昇圧セル列の*i*段目 ($1 \leq i \leq N$) の前記昇圧セルの入力電位と、前記第2の昇圧セル列の*i*段目 ($1 \leq i \leq M$) の前記昇圧セルの入力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の*i*+1段目の前記昇圧セル又は*i*段目の前記昇圧セル又は*i*段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0017】

請求項3の発明では、基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路において、N段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、各々前記第1の昇圧セル列の*i*段目 ($1 \leq i \leq N$) の前記昇圧セルの出力電位と、前記第2の昇圧セル列の*i*段目 ($1 \leq i \leq M$) の前記昇圧セルの出力電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又は*i*+1段目の前記昇圧セル又は*i*段目の前記昇圧セル又は*i*段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0018】

請求項4の発明では、基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内と前記第2のウエル領域内とのうちいずれか一方又は両方に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路において、N段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、各々前記第1の昇圧セル列の逆流防止回路の中間電位と、前記第2の昇圧セル列の逆流防止回路の中間電位とのうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又は前記第1の昇圧セル列及び前記第2の昇圧セル列に含まれる前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0019】

請求項5の発明では、基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内と前記第2のウエル領域内とのうちいずれか一方又は両方に1つ以上のスイッチング素子を備えて、前記1つ以上のスイッチング素子により第1の端子と第2の端子との間をオン・オフして前記第1の端子から前記第2の端子へ電荷を転送する昇圧セル及び逆流防止回路を備えた昇圧回路において、N段 ($N \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第1の昇圧セル列と、M段 ($M \geq 1$) の前記昇圧セルと前記逆流防止回路とから構成された第2の昇圧セル列と、各々前記第1及び第2の昇圧セル列の*i*段目 ($1 \leq i \leq N$) の前記昇圧セル同士又は逆流防止回路同士の入力電位を比較し、前記入力電位のうち、高い側の電位又は低い側の電位を出力するアナログ比較回路とを有し、前記アナログ比較回路の出力電位を前記第1及び第2の昇圧セル列の前記逆流防止回路又は*i*+1段目の前記昇圧セル又は*i*段目の前記昇圧セル又は*i*段目より前段の前記昇圧セルのうちの1つ以上に備えられた前記1つ以上のスイッチング素子の前記第1のウエル領域に印加することとした。

【0020】

請求項6の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記第2のウエル領域と前記第1の端子とが同電位となるように、前記第2のウエル領域と前記第1の端子とを互いに接続した。

【0021】

請求項7の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記第2のウエル領域と前記第1のウエル領域とが同電位となるように、前記第2のウエル領域と前記第1のウエル領域とを互いに接続した。

【0022】

請求項8の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、かつ前記昇圧セルの各段毎に備えられている。

【0023】

請求項9の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記アナログ比較回路は、前記基板上に第1導電型の第1のウエル領域を有し、前記第1のウエル領域内に第2導電型の第2のウエル領域を有し、前記第1のウエル領域内又は前記第2のウエル領域内に1つ以上のスイッチング素子を有するものであり、前記第1及び第2の昇圧セル列に1つ以上備えられ、かつ前記昇圧セルの任意の段数毎に備えられている。

【0024】

請求項10の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記昇圧セルの前記第1の端子と前記第1のウエル領域との間にダイオード手段を備える。

【0025】

請求項11の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記第1及び第2の昇圧セル列の前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトを共通化した。

【0026】

請求項12の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記第1及び第2の昇圧セル列の前記第1のウエル領域の電位が同電位である前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の前記第1のウエル領域のレイアウトとを共通化した。

【0027】

請求項13の発明では、請求項1～5のいずれかの発明に係る昇圧回路において、前記第1の昇圧セル列のi段目の昇圧セルの前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の第1の素子の前記第1のウエル領域のレイアウトとを共通化し、前記第2の昇圧セル列のi段目の昇圧セルの前記1つ以上のスイッチング素子の前記第1のウエル領域のレイアウトと前記アナログ比較回路の第2の素子の前記第1のウエル領域のレイアウトとを共通化した。

【発明の効果】

【0028】

請求項1の発明によれば、第1導電型の第1のウエル領域の充放電電荷量をクロック信号信号の電圧スイングより小さくでき、見かけ上の第1のウエル領域－基板間の寄生容量を削減できるため、昇圧動作時の消費電流を抑制できる。また、見かけ上の第1のウエル領域－基板間の寄生容量を削減できるため、昇圧効率を向上できる。また、1つのアナログ比較回路で複数の昇圧セルの第1のウエル領域の電位を制御することで、アナログ比較回路によるレイアウト面積増大を抑制できる。

【0029】

請求項2の発明によれば、初段の昇圧セルの入力電位を用いたウエル制御が可能となり、各段の昇圧容量に接続される負荷容量を均等化することができる。これにより、より安

定した昇圧動作が可能となる。

【0030】

請求項3の発明によれば、逆流防止回路の第1のウエル領域の電位制御も可能であり、逆流防止回路における電荷転送効率の低下を抑制することができる。

【0031】

請求項4の発明によれば、逆流防止回路の中間電位を用いたウエル制御が可能となり、各段の昇圧容量に接続される負荷容量を均等化することができる。これにより、より安定した昇圧動作が可能となる。

【0032】

請求項5の発明によれば、初段の昇圧セルの入力電位を用いたウエル制御が可能となり、各段の昇圧容量に接続される負荷容量を均等化することができる。これにより、より安定した昇圧動作が可能となる。

【0033】

請求項6の発明によれば、昇圧セル内の電荷転送トランジスタ（スイッチング素子）の入力端子と第2のウエル領域とを接続することで、基板バイアス効果によるスイッチング素子の電流駆動能力低下を抑制することができる。

【0034】

請求項7の発明によれば、第1のウエル領域と第2のウエル領域とを同電位にすることで、NチャネルトランジスタとPチャネルトランジスタとのウエル領域を共通化できるため、レイアウト面積の削減が可能となる。

【0035】

請求項8の発明によれば、全ての段にアナログ比較回路を備えることで、昇圧セルの寄生容量を同一にし、設計容易性を向上することができる。

【0036】

請求項9の発明によれば、任意の段数にアナログ比較回路を備えることで、第2のウエル領域と第1のウエル領域との耐圧マージンを確保した上で、回路面積増大を抑制することができる。

【0037】

請求項10の発明によれば、ダイオード手段を介して第1のウエル領域に昇圧セルの入力電位を供給することで、昇圧回路起動時に第1のウエル領域の電位上昇を各昇圧セル電位に追従させ、ラッチアップ発生を抑制することができる。

【0038】

請求項11及び12の発明によれば、第1のウエル領域のレイアウトを共通化することでレイアウト面積を削減することができる。

【0039】

請求項13の発明によれば、第1のウエル領域の充放電電荷量を削減したうえで、位相の異なるクロックでポンピングされる第1の昇圧セル列と第2の昇圧セル列との間のノイズ干渉を削減することができる。

【発明を実施するための最良の形態】

【0040】

以下、本発明の実施の形態による昇圧回路について、図面を参照しながら説明する。

【0041】

図1は、本発明に係る昇圧回路の構成例を示している。図1において、101は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで出力端子電圧（昇圧電圧）V_{pump}を発生する2並列の昇圧回路である。102、103、104、105、106、107は第1列と第2列との構成を持ち、第1列の奇数段目にはCLK1が入力され、第1列の偶数段目にはCLK2が入力され、第2列の奇数段目にCLK2が入力され、第2列の偶数段目にはCLK1が入力される昇圧セル、108、109は昇圧電圧V_{pump}の逆流を防止する逆流防止回路、110、111、112、113、114、115、116は昇圧セル102～107の入出力端子、117、118、119は第1列と

第2列との同じ段の昇圧セルの各々の入出力端子の電圧のうち低い側の電圧を出力する低電圧出力アナログ比較回路の一例であり、120、121は低電圧出力アナログ比較回路117、118、119に用いられるNch（Nチャネル）トランジスタ、122、123、124は各昇圧セルのNウエルに接続された低電圧出力アナログ比較回路117～119の出力端子、125は第1列の3段目の昇圧セル104と第2列の3段目の昇圧セル107との各々の入出力端子113、116の電圧のうち高い側の電圧を出力する高電圧出力アナログ比較回路の一例であり、126、127は高電圧出力アナログ比較回路125に用いられるPch（Pチャネル）トランジスタ、128は逆流防止回路108、109のNウエルに接続された高電圧出力アナログ比較回路の出力端子である。なお、従来例と同一符号の要素は、従来例と同様であることを示す。また、本昇圧回路101の直列接続数は一例である。

【0042】

図1の昇圧回路101における2相クロック信号CLK1、CLK2の波形は、図26と同様である。図26を用いて、図1の昇圧回路101の動作を説明する。

【0043】

時刻T1の状態ではCLK1が“L”から“H”へ遷移し、CLK2が“H”から“L”へと遷移すると、昇圧セル102、104、106の入出力端子111、113、115の電位が昇圧され、昇圧された電荷は、昇圧セル103、逆流防止回路108、昇圧セル107の各々の電荷転送トランジスタ906を介して入出力端子112、昇圧回路101の出力端子、入出力端子116にそれぞれ転送される。このとき、低電圧出力アナログ比較回路117は、昇圧された入出力端子111と昇圧されていない入出力端子114との電位の関係により、Nchトランジスタ120はオフ状態、Nchトランジスタ121はオン状態となり、低電圧出力アナログ比較回路117の出力端子122には入出力端子114の電位が出力されて、昇圧セル102と昇圧セル105とのNウエルに供給される。同様に、低電圧出力アナログ比較回路118の出力端子123には入出力端子112の電位が出力されて、昇圧セル103と昇圧セル106とのNウエルに供給され、低電圧出力アナログ比較回路119の出力端子124には入出力端子116の電位が出力されて、昇圧セル104と昇圧セル107とのNウエルに供給される。また、高電圧出力アナログ比較回路125は、昇圧された入出力端子113と昇圧されていない入出力端子116との電位の関係により、Pchトランジスタ126はオン状態、Pchトランジスタ127はオフ状態となり、高電圧出力アナログ比較回路125の出力端子128には入出力端子113の電位が出力されて、逆流防止回路108と逆流防止回路109とのNウエルに供給される。

【0044】

時刻T2の状態ではCLK1が“H”から“L”へ遷移し、CLK2が“L”から“H”へと遷移すると、昇圧セル103、105、107の入出力端子112、114、116の電位が昇圧され、昇圧された電荷は、昇圧セル104、106、逆流防止回路109の各々の電荷転送トランジスタ906を介して入出力端子113、115、昇圧回路101の出力端子にそれぞれ転送される。このとき、低電圧出力アナログ比較回路117は、昇圧された入出力端子114と昇圧されていない入出力端子111との電位の関係により、Nchトランジスタ120はオン状態、Nchトランジスタ121はオフ状態となり、低電圧出力アナログ比較回路117の出力端子122には入出力端子111の電位が出力されて、昇圧セル102と昇圧セル105とのNウエルに供給される。同様に、低電圧出力アナログ比較回路118の出力端子123には入出力端子115の電位が出力されて、昇圧セル103と昇圧セル106とのNウエルに供給され、低電圧出力アナログ比較回路119の出力端子124には入出力端子113の電位が出力されて、昇圧セル104と昇圧セル107とのNウエルに供給される。また、高電圧出力アナログ比較回路125は、昇圧された入出力端子116と昇圧されていない入出力端子113との電位の関係により、Pchトランジスタ126はオフ状態、Pchトランジスタ127はオン状態となり、高電圧出力アナログ比較回路125の出力端子128には入出力端子116の電位が出力さ

れて、逆流防止回路108と逆流防止回路109とのNウエルに供給される。

【0045】

このように、図1の昇圧回路101によれば、各昇圧セル102～107及び各逆流防止回路108、109のNウエルの電位を昇圧セル各段の入力電位又は出力電位に固定することが可能となり、Nウエルー基板間の充放電電荷量を削減し、消費電流の削減が可能となる。また、Nウエルー基板間の充放電電荷量を削減することで次段へ転送される電荷量を増やすことが可能となり、昇圧効率の向上が期待できる。

【0046】

なお、図2、図3に示すように、低電圧出力アナログ比較回路117～119及び高電圧出力アナログ比較回路125は、PウエルーNウエルの耐圧マージン及び回路面積を考慮して、任意の段数の昇圧セルに対して設けることが可能であり、素子数を削減したうえでも上記に示す構成と同様の効果を有することができる。

【0047】

図4は、本発明に係る昇圧回路の更に他の構成例を示している。図4において、701は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで昇圧電圧V_{pump}を発生する2並列の昇圧回路である。702、703、704、705、706、707は、図1の昇圧セル102～107に対して、各昇圧セルの入出力端子と高電圧出力アナログ比較回路125の出力端子128との間にダイオード接続されたトランジスタ710を追加したものである。708、709は逆流防止回路である。なお、図1と同一符号は、それらと同様であることを示す。また、本昇圧回路701の直列接続数は一例である。

【0048】

図1との差分として、図4の構成では、低電圧（又は高電圧）出力アナログ比較回路117～119、125を共通化し、素子数を削減している。これにより、昇圧回路701の起動時、各昇圧セル702～707の入出力端子111～116の電位が上昇する際、Nウエル電位は各昇圧セル702～707のPウエル907より寄生ダイオード909の順方向電流として供給されることとなる。この寄生ダイオード909の順方向電流を抑制するために、ダイオード機能を有するトランジスタ710を備えることで、昇圧回路701の起動時においても安定した昇圧動作が可能となる。

【0049】

図5は、本発明に係る昇圧回路の更に他の構成例を示している。図5において、621は2相クロック信号CLK1、CLK2を入力して昇圧動作を行うことで昇圧電圧V_{pump}を発生する2並列の昇圧回路である。858、859は逆流防止回路であり、2相クロック信号CLK1、CLK2を入力して逆流防止回路858、859のトランジスタ861、862を制御することで、電荷転送トランジスタ860を導通、非導通状態にする。これにより、図1の逆流防止回路108、109で生じる転送効率の低下を抑制する構成である。なお、図1と同一符号は、それらと同様であることを示す。また、本昇圧回路621の直列接続数は一例である。

【0050】

図1との差分として、図5の構成では、2相クロック信号CLK1、CLK2を入力して電荷転送トランジスタ860のゲート電位を制御し、電荷転送効率と昇圧効率を向上させる逆流防止回路858、859においても、低電圧出力アナログ比較回路501を用いていることである。

【0051】

図5によれば、昇圧回路621の各段に同様の構成である低電圧出力アナログ比較回路117、118、119、501を用いることにより、図1における最終段の昇圧セル104、107の昇圧容量910の負荷と、他の昇圧セル102、103、105、106の昇圧容量910の負荷との相違を抑制でき、各段の昇圧容量910における寄生容量をほぼ均等化することができ、各段の昇圧セルの電荷転送量が均等になり、安定した昇圧動作が可能となる。

【0052】

なお、図6の昇圧回路622は、図1中の全ての昇圧セル102～107及び逆流防止回路108、109に対して高電圧出力アナログ比較回路511、512、513、125を用いた例であり、初段の昇圧セル102、105のNウエルを制御する高電圧出力アナログ比較回路511のトランジスタ126、127のゲートのみVSSに固定する。これにより、図5と同様に安定した昇圧動作が可能となる。

【0053】

以上、昇圧回路構成として、2相クロック信号CLK1、CLK2を用いる昇圧回路を例としたが、図7に示す4相クロック信号CLK1、CLK2、CLK3、CLK4を用いた昇圧回路801や、図8、図9、図10、図11に示すような2相クロック信号CLK1、CLK2を用いた昇圧回路851、881、601、611等、昇圧セルにトリプルウエルのNchトランジスタを使用している場合には、低電圧出力アナログ比較回路117～119、501又は高電圧出力アナログ比較回路511～513、125を用いることで、昇圧セルの構成にかかわらず同様の効果を有することが可能である。また、図11に示すように、昇圧セル602～607のNchトランジスタ612のPウエルをNウエルと共通に接続することも可能であり、更にPchトランジスタ611のNウエルも共通接続することでレイアウト面積を削減することもできる。

【0054】

なお、図7において、802、803、804、805、806、807は昇圧セル、808、809は逆流防止回路、810は電荷転送トランジスタ（Nchトランジスタ）、811、813はNchトランジスタ、812は昇圧容量である。また、図8において、852、853、854、855、856、857は昇圧セル、858、859は逆流防止回路、860は電荷転送トランジスタ（Nchトランジスタ）、861、863はNchトランジスタ、862はPchトランジスタである。また、図10、図11において、602、603、604、605、605、607は昇圧セル、608、609は逆流防止回路、610、612は電荷転送トランジスタ（Nchトランジスタ）、611、614は電荷転送トランジスタ（Pchトランジスタ）、613は接続ノードである。

【0055】

図12、図13、図14は、高電圧（低電圧）出力アナログ比較回路の構成例であり、全昇圧セル、逆流防止回路に対して、高電圧（低電圧）出力アナログ比較回路のいずれか一方、又は両方を混同して用いることも可能である。また、各昇圧セルにおけるNウエル内の電荷転送トランジスタ等のトランジスタの個数やPchトランジスタの有無に関係なく、更に電荷転送トランジスタ等のNchトランジスタのPウエルがNウエルに接続された場合や、Pウエルの電位がドレイン、ソースの電位を切り替えて供給される場合など、Pウエルの接続は必ずしもソースと直接接続されていなくても、昇圧動作が可能であれば、同様の効果を有することができる。

【0056】

また、図示の低電圧出力アナログ比較回路117～119、501及び高電圧出力アナログ比較回路511、512、513、125の構成は一例であり、同様の機能を有するものであればよい。

【0057】

図15は、本発明に係る昇圧回路におけるレイアウト構成例を示す平面図であり、図1で示した昇圧セル102～107の電荷転送トランジスタ906と低電圧出力アナログ比較回路117～119とを図示している。

【0058】

図15より、低電圧出力アナログ比較回路117（又は118、119）の出力端子122（又は123、124）は、昇圧セル102と105（又は103と106、又は104と107）の電荷転送トランジスタ906のNウエル（NT）に接続され、かつ、当該Nウエルは2つの昇圧セル102、105の電荷転送トランジスタ906に対して共通にレイアウトされている。

【0059】

図15によれば、低電圧出力アナログ比較回路117の出力電圧により制御される2つ以上の昇圧セル102, 105内に存在するトリプルウエル構造のスイッチング素子906において、Nウエルを共通にレイアウトすることが可能となり、レイアウト面積を削減することができる。

【0060】

なお、図15のレイアウト構成は一例であり、図16、図17のように、低電圧出力アナログ比較回路118の出力電圧により制御されるスイッチング素子906のNウエルのレイアウトを昇圧セルの段数に関係なく任意に分離、共通化することができる。

【0061】

更に、図18、図19のように、低電圧出力アナログ比較回路117～119のNウエルも昇圧セル102～107のスイッチング素子906のNウエルと共通にレイアウトすることが可能である。

【0062】

また、図20、図21のように、低電圧出力アナログ比較回路117, 118, 119, 501のトランジスタ120と昇圧セル102, 103, 104及び逆流防止回路108とのNウエルを共通化し、かつ低電圧出力アナログ比較回路117, 118, 119, 501のトランジスタ121と昇圧セル105, 106, 107及び逆流防止回路109とのNウエルを共通化することも可能である。これにより、Nウエルの充放電電荷量を削減しつつ、昇圧容量におけるノイズの影響を削減し、安定した昇圧動作を行うことが可能となる。

【0063】

これらは、図22、図23、図24に構成例を示すとおり、高電圧出力アナログ比較回路511, 512, 513, 125においても同様のレイアウトが可能である。

【0064】

また、上記レイアウトは一例であり、昇圧セル列に関わらず、同電位である複数個のトランジスタのNウエル領域、Pウエル領域は、任意に共通化することが可能である。

【産業上の利用可能性】

【0065】

以上説明してきたとおり、本発明に係る昇圧回路は、昇圧セルを構成するトリプルウエル構造の素子において、基板バイアス効果を抑制したうえで、消費電流の削減、回路面積、レイアウト面積を削減できる特徴を有し、不揮発性半導体記憶装置、CMOSプロセスでのアナログ回路特性改善のための電源発生回路等として有用である。

【0066】

また、DRAM等の揮発性半導体記憶装置、液晶装置、携帯機器の電源回路等の用途にも応用できる。

【図面の簡単な説明】

【0067】

- 【図1】 本発明に係る昇圧回路の構成例を示す回路図である。
- 【図2】 本発明に係る昇圧回路の他の構成例を示す回路図である。
- 【図3】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図4】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図5】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図6】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図7】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図8】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図9】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図10】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図11】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
- 【図12】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。

【図 1 3】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
【図 1 4】 本発明に係る昇圧回路の更に他の構成例を示す回路図である。
【図 1 5】 本発明に係る昇圧回路におけるレイアウト構成例を示す平面図である。
【図 1 6】 本発明に係る昇圧回路における他のレイアウト構成例を示す平面図である。

。【図 1 7】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 1 8】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 1 9】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 0】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 1】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 2】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 3】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 4】 本発明に係る昇圧回路における更に他のレイアウト構成例を示す平面図である。

【図 2 5】 従来の昇圧回路の例を示す回路図である。

【図 2 6】 図 2 5 の昇圧回路における 2 相クロック信号の波形図である。

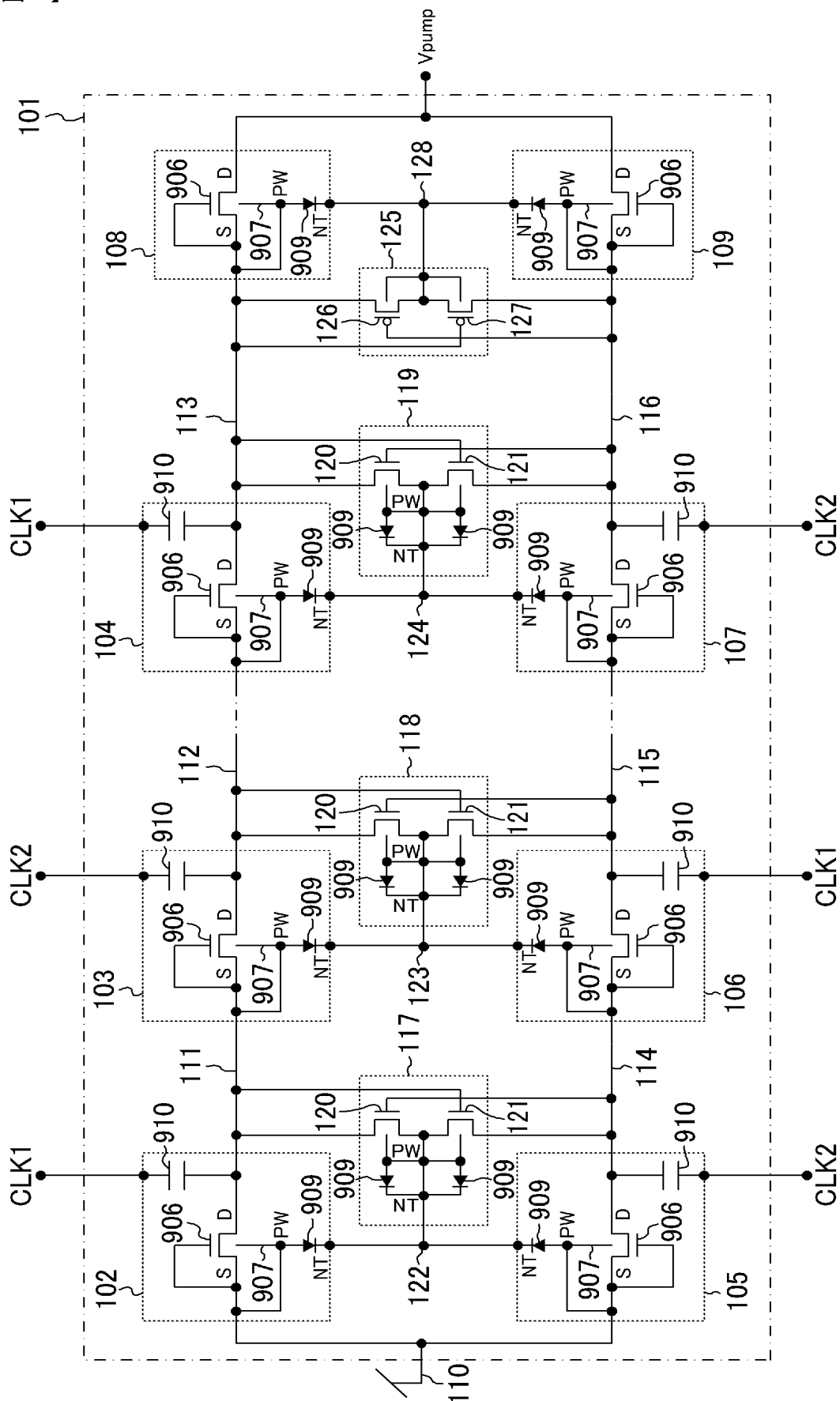
【符号の説明】

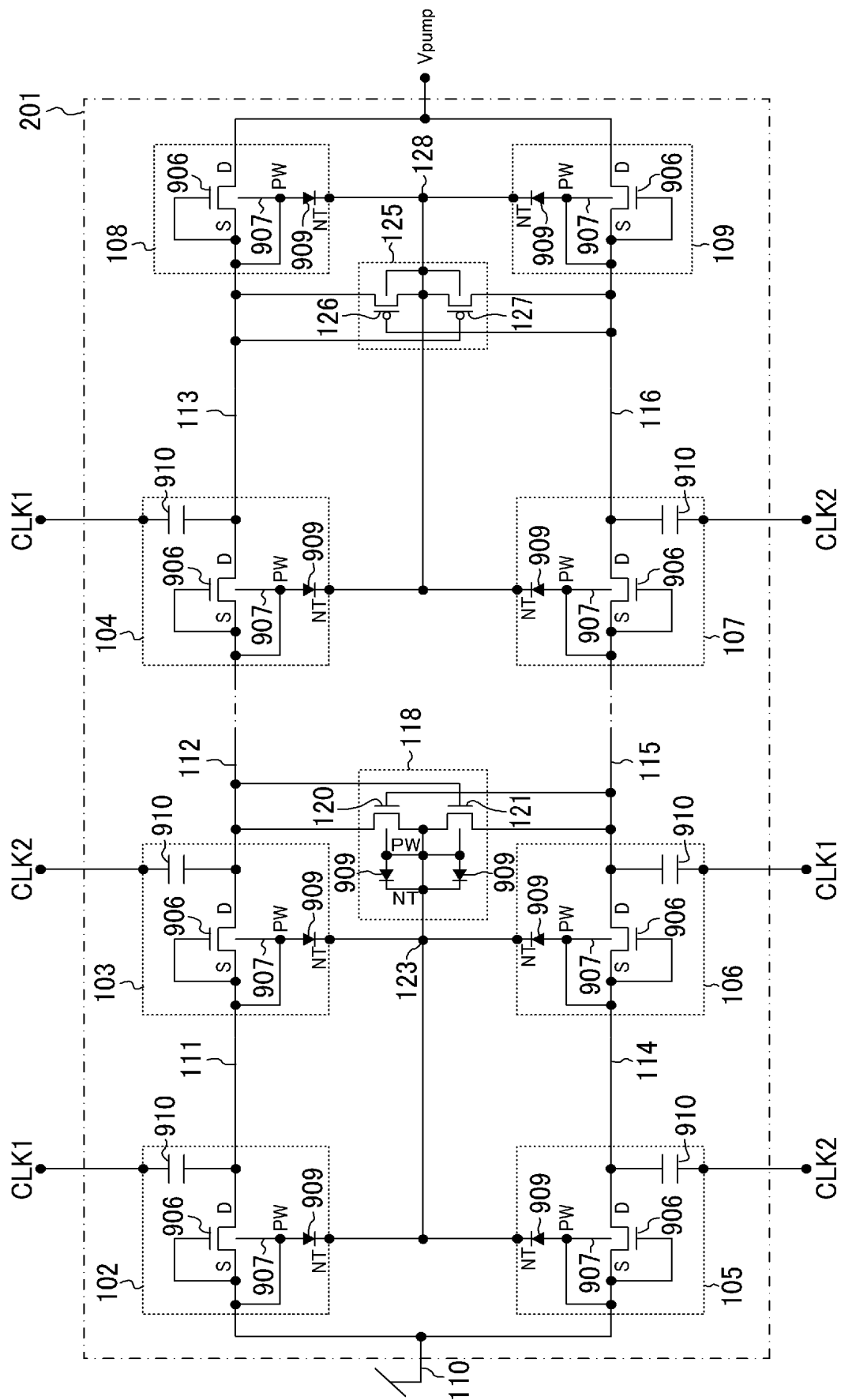
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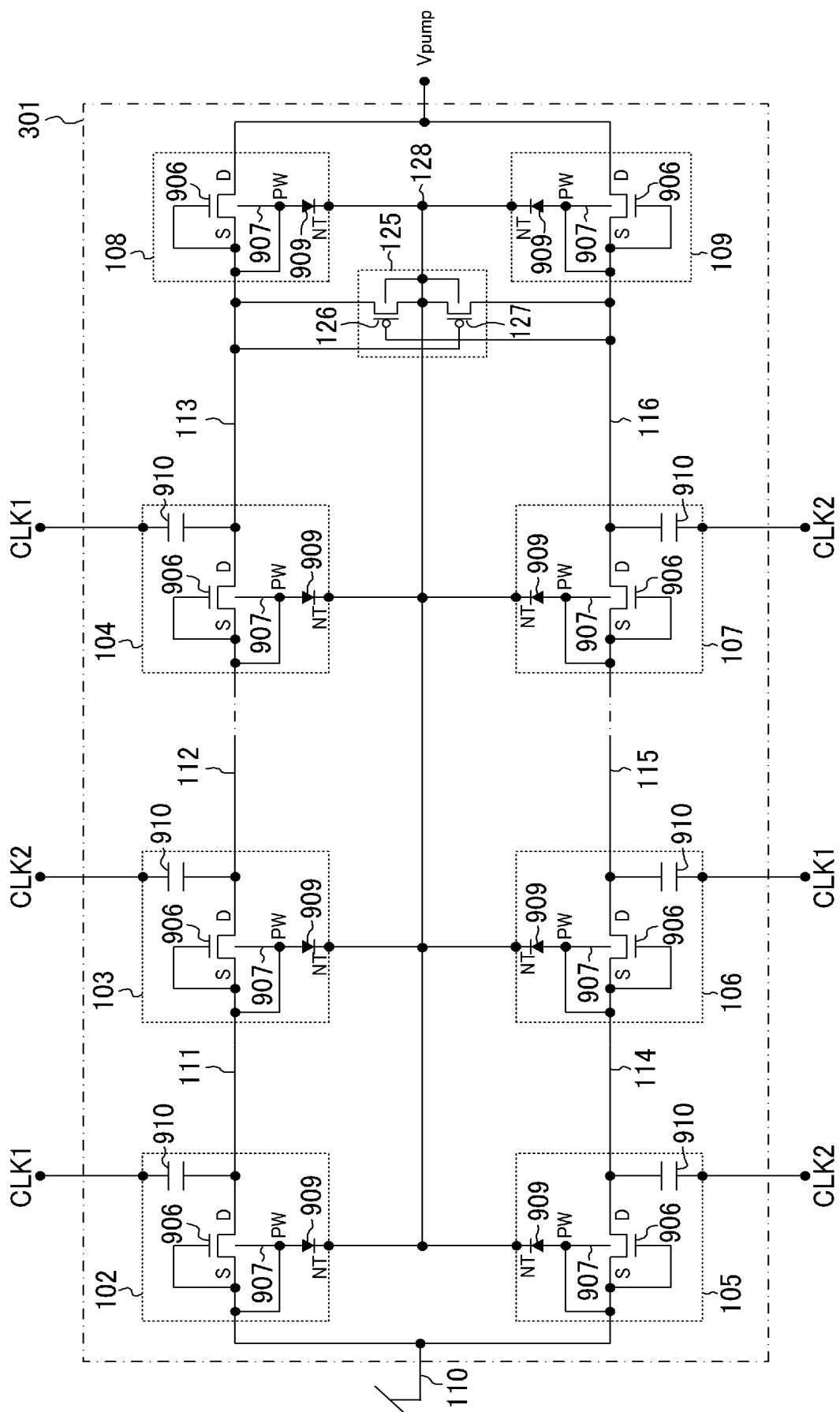
101, 201, 301 昇圧回路
102~107 昇圧セル
108, 109 逆流防止回路
110~116 昇圧セルの入出力端子
117~119 低電圧出力アナログ比較回路
120, 121 Nchトランジスタ
122~124 低電圧出力アナログ比較回路の出力端子
125 高電圧出力アナログ比較回路
126, 127 Pchトランジスタ
128 高電圧出力アナログ比較回路の出力端子
501 低電圧出力アナログ比較回路
511~513 高電圧出力アナログ比較回路
601, 611 昇圧回路
602~607 昇圧セル
608, 609 逆流防止回路
610, 612 電荷転送トランジスタ (Nchトランジスタ)
611, 614 電荷転送トランジスタ (Pchトランジスタ)
613 接続ノード
621, 622 昇圧回路
701 昇圧回路
702~707 昇圧セル
708, 709 逆流防止回路
710 ダイオード接続トランジスタ
801 昇圧回路
802~807 昇圧セル

808, 809 逆流防止回路
810 電荷転送トランジスタ (Nchトランジスタ)
811, 813 Nchトランジスタ
812 昇圧容量
851, 881 昇圧回路
852~857 昇圧セル
858, 859 逆流防止回路
860 電荷転送トランジスタ (Nchトランジスタ)
861, 863 Nchトランジスタ
862 Pchトランジスタ
901 昇圧回路
902~904 昇圧セル
905 逆流防止回路
906 電荷転送トランジスタ (Nchトランジスタ)
907 Pウエル (PW)
908 Nウエル (NT)
909 PウエルとNウエルとの間の寄生ダイオード
910 昇圧容量
911~914 昇圧セルの入出力端子
CLK1~CLK4 クロック信号
Ttrans 電荷転送期間
Vpump 出力端子電圧 (昇圧電圧)

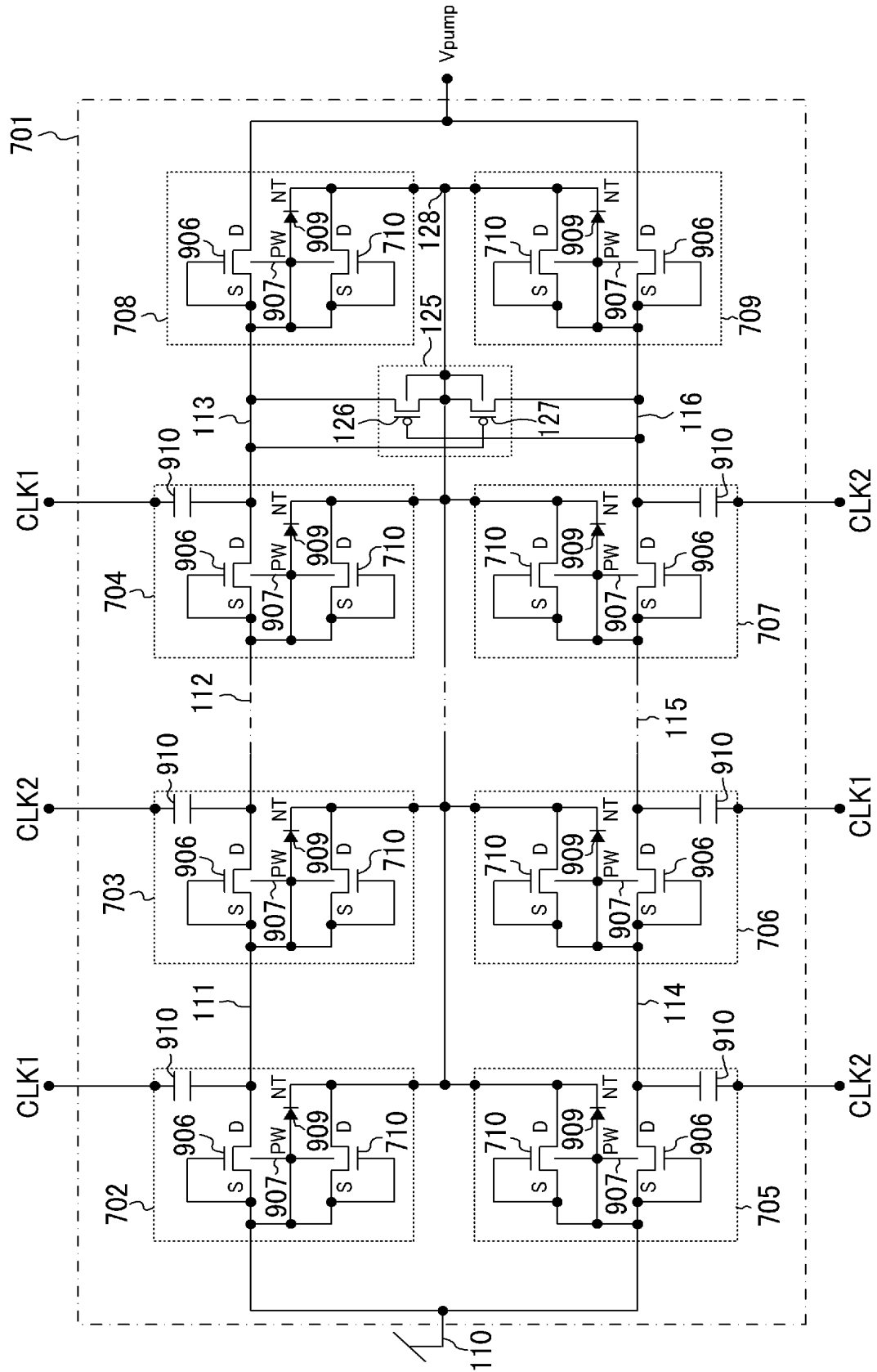
【書類名】 図面
【図 1】



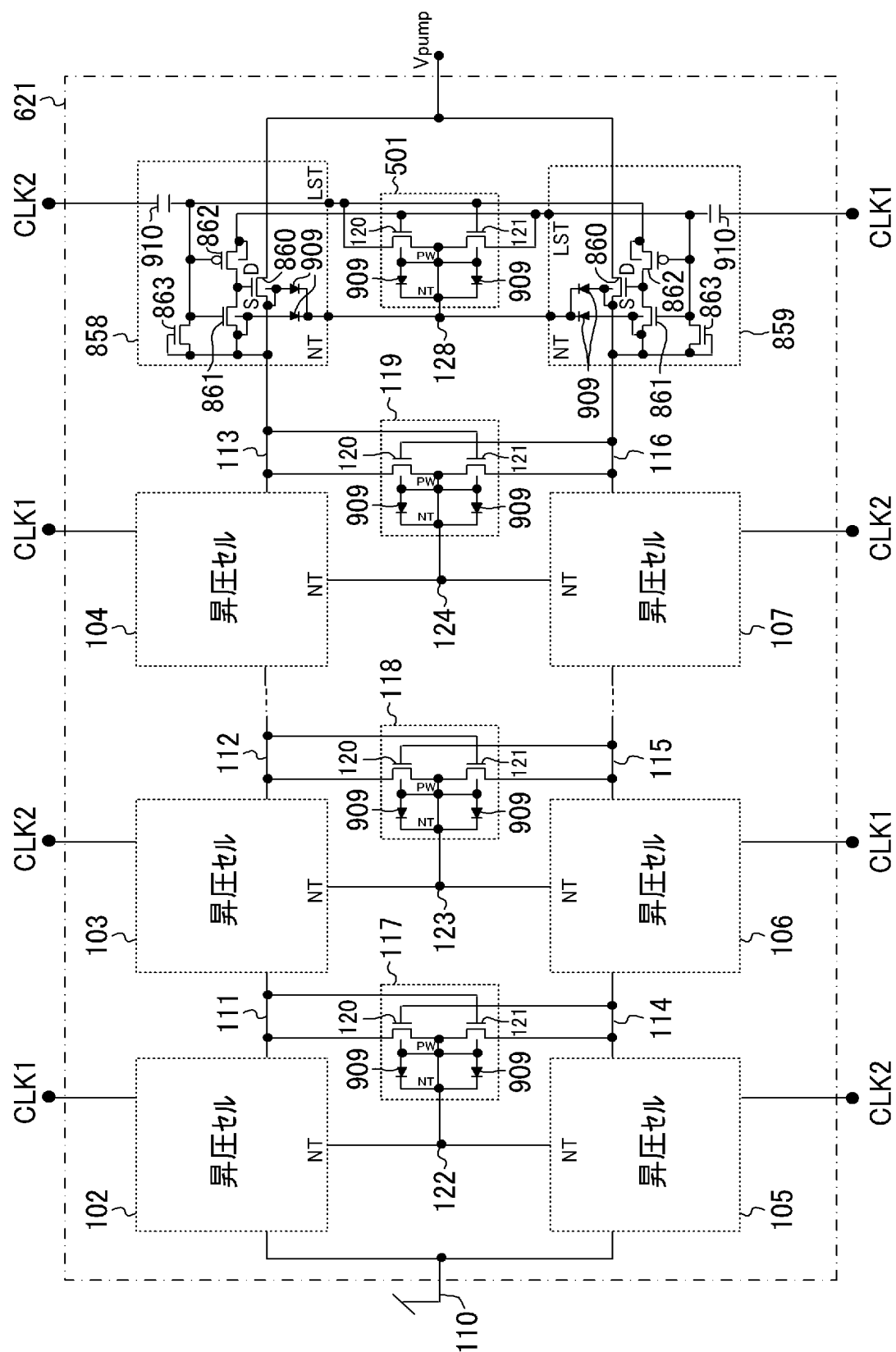




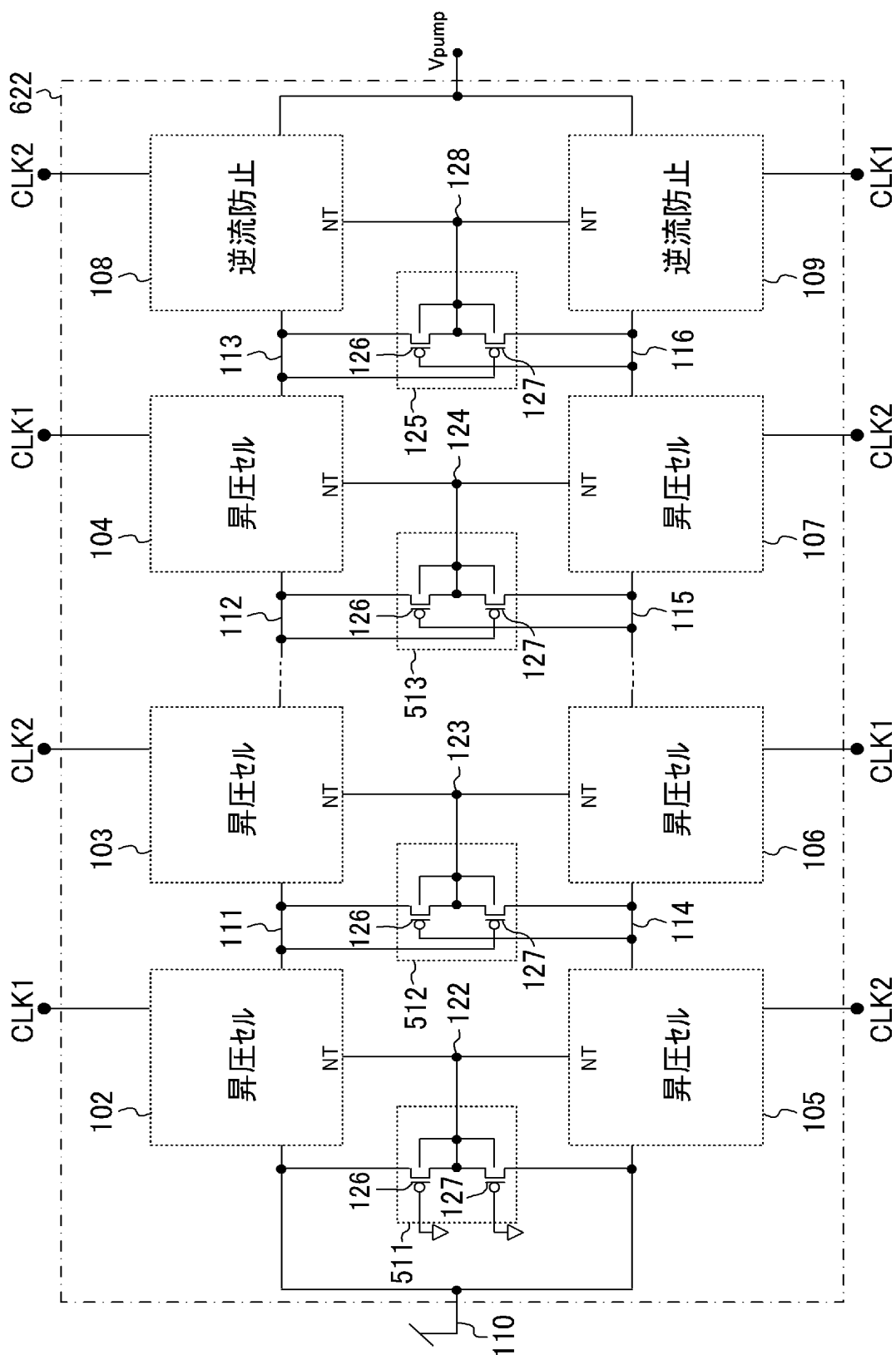
【図4】



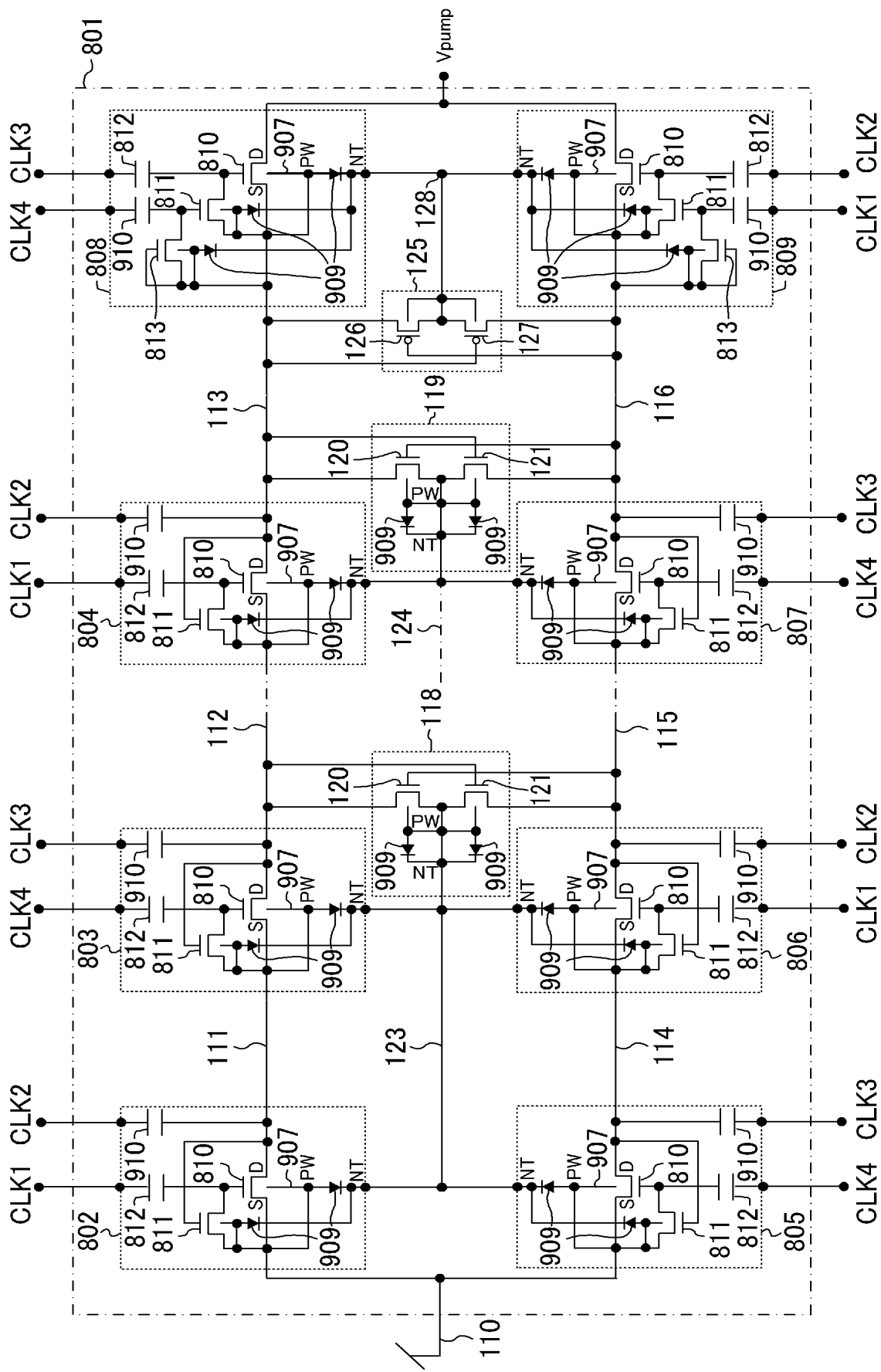
【図 5】

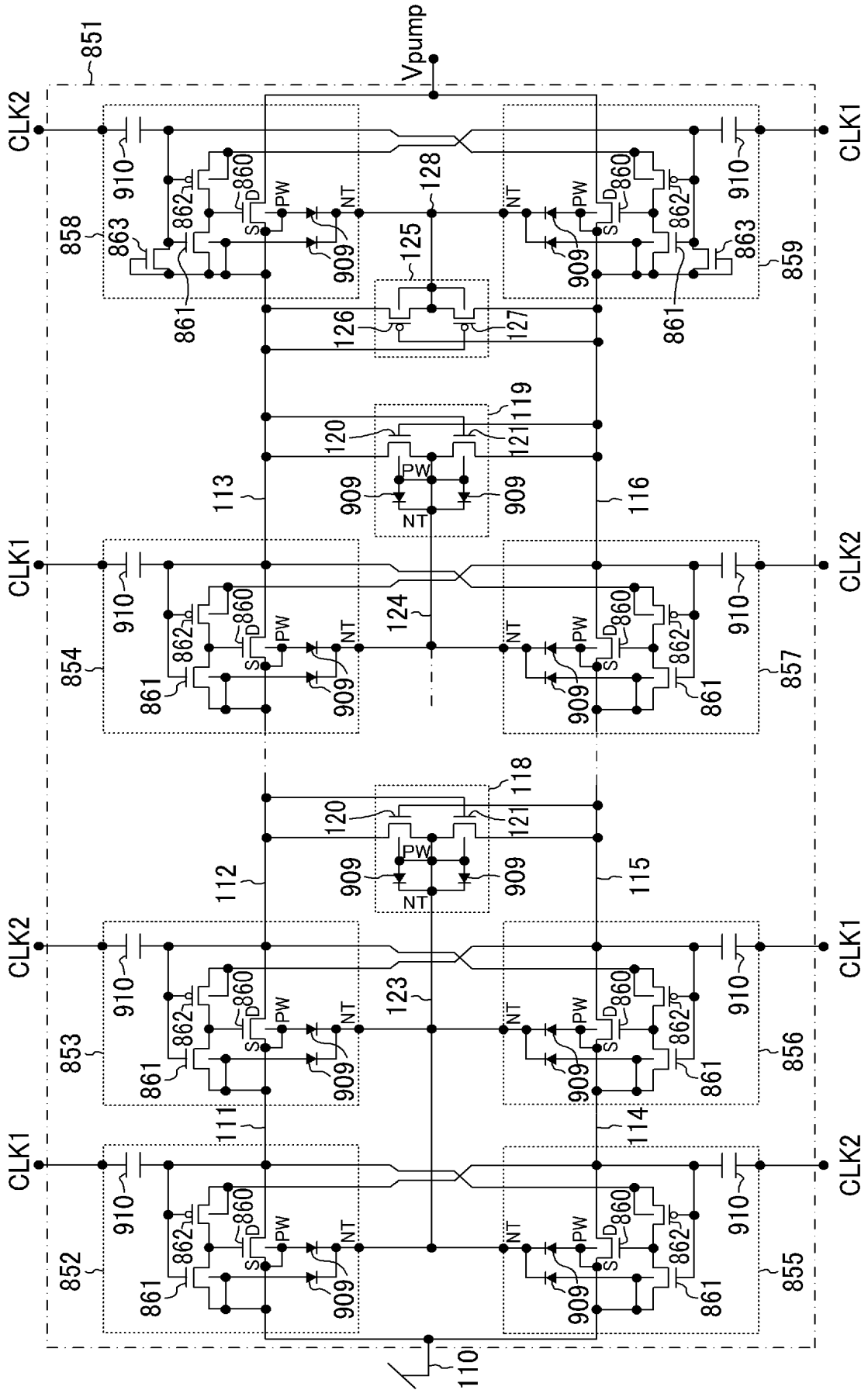


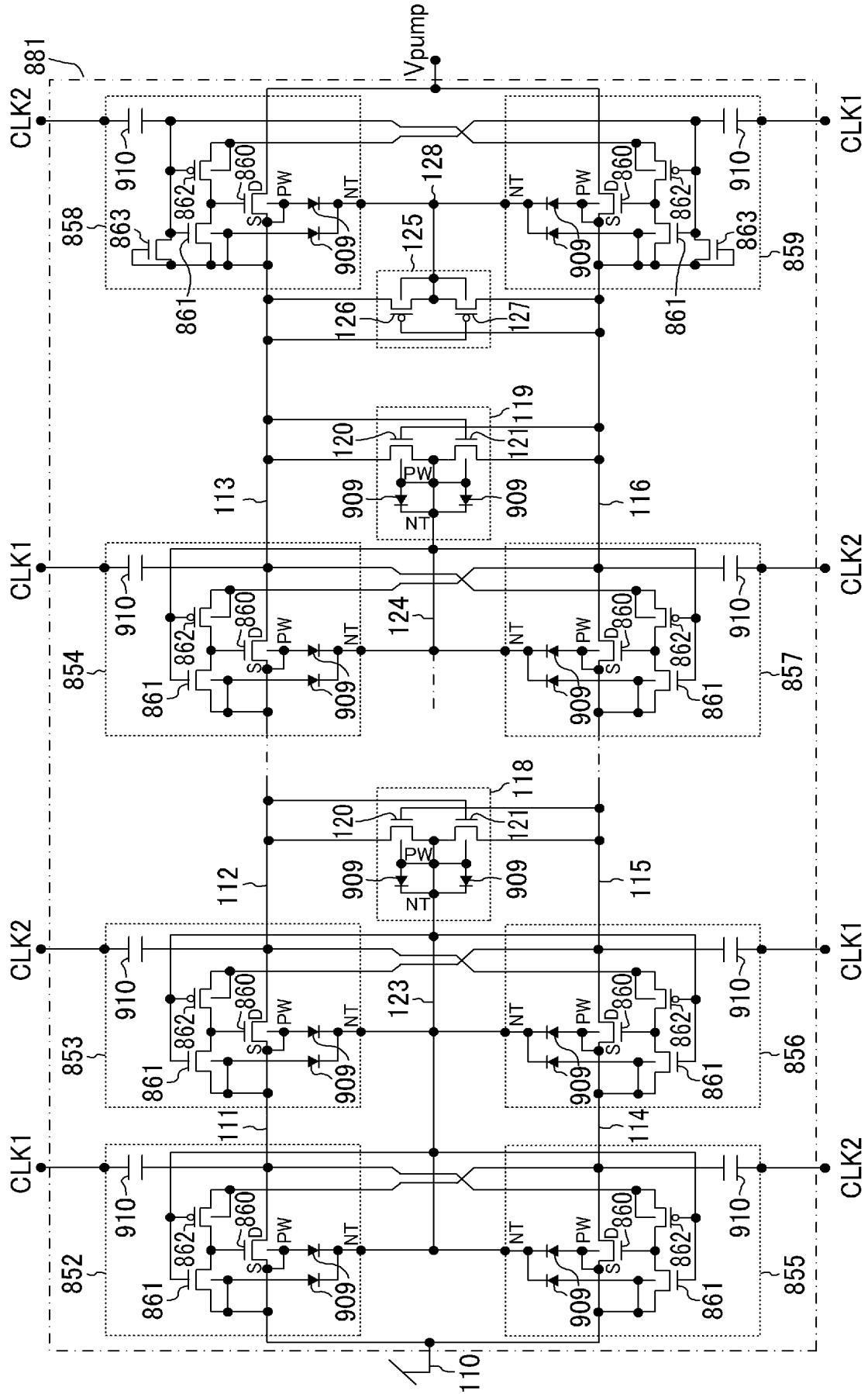
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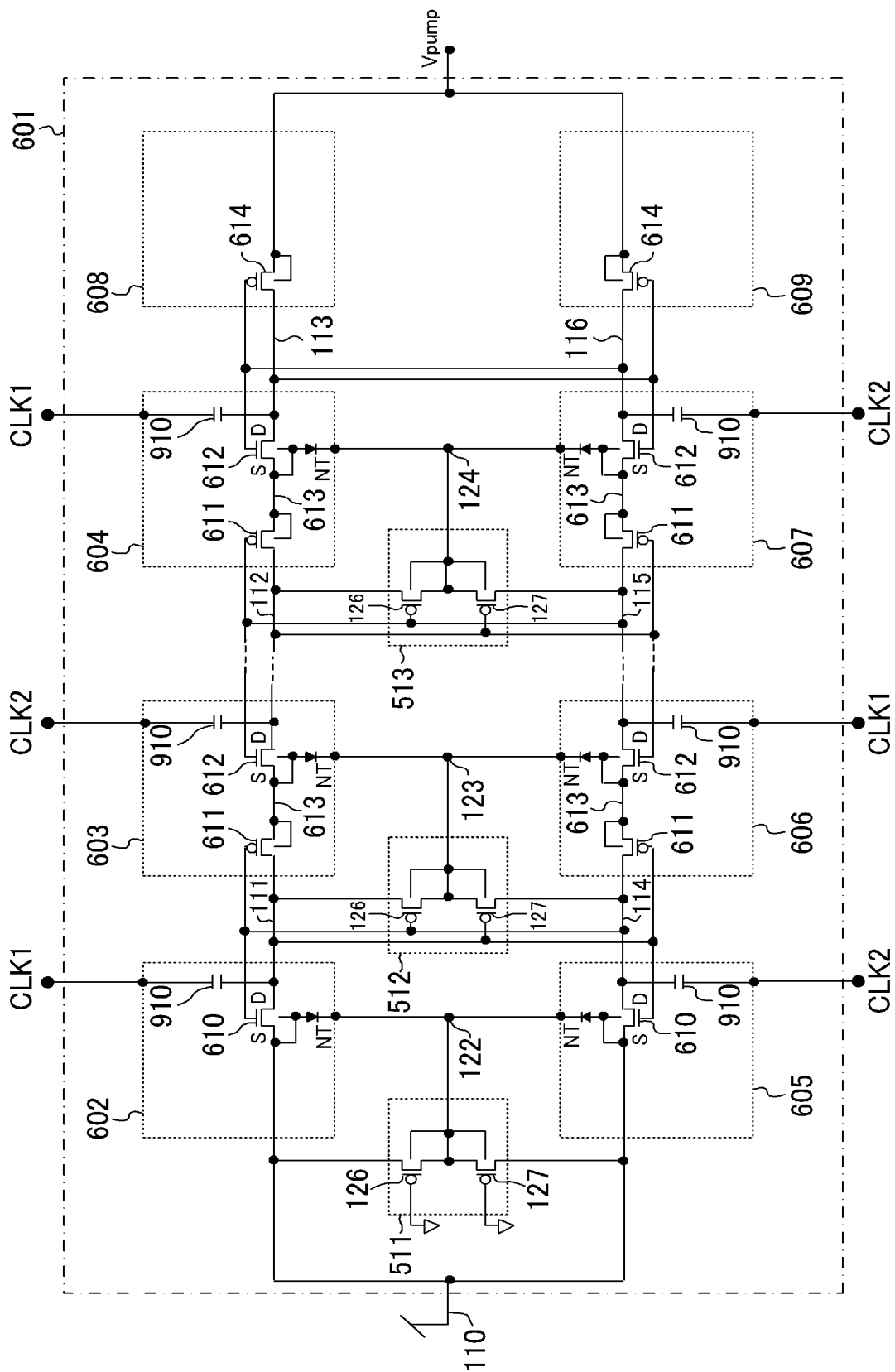


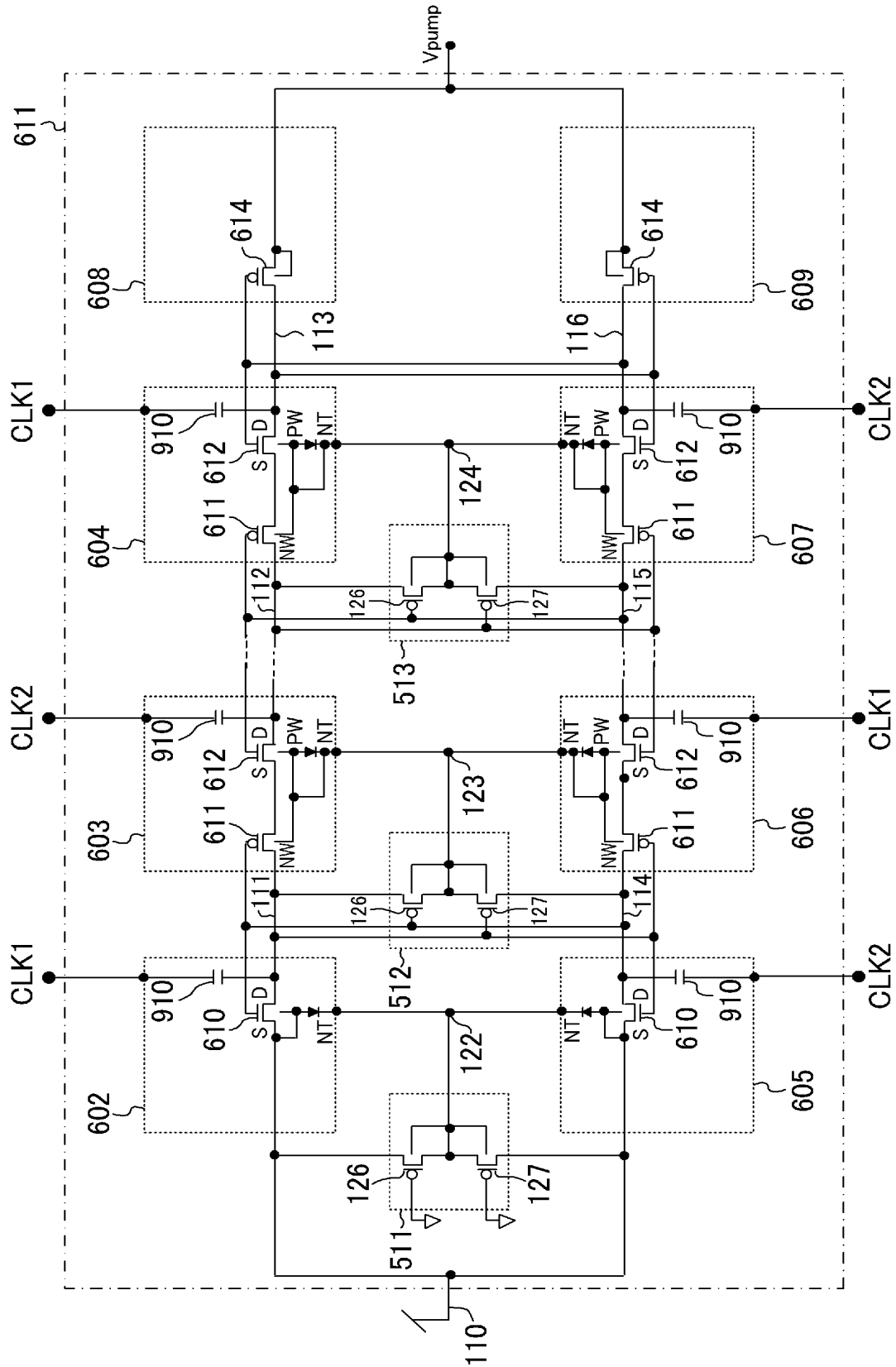
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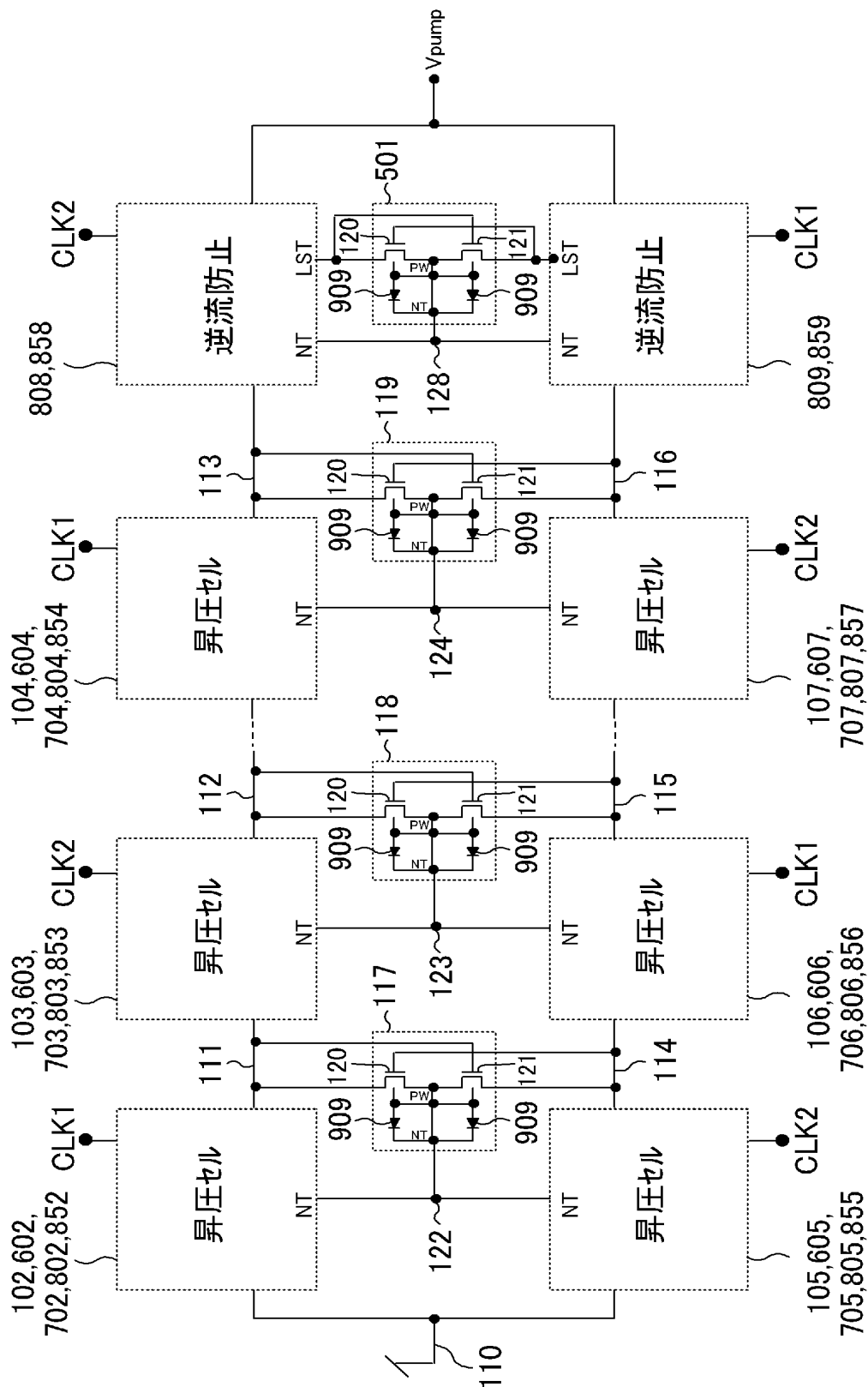




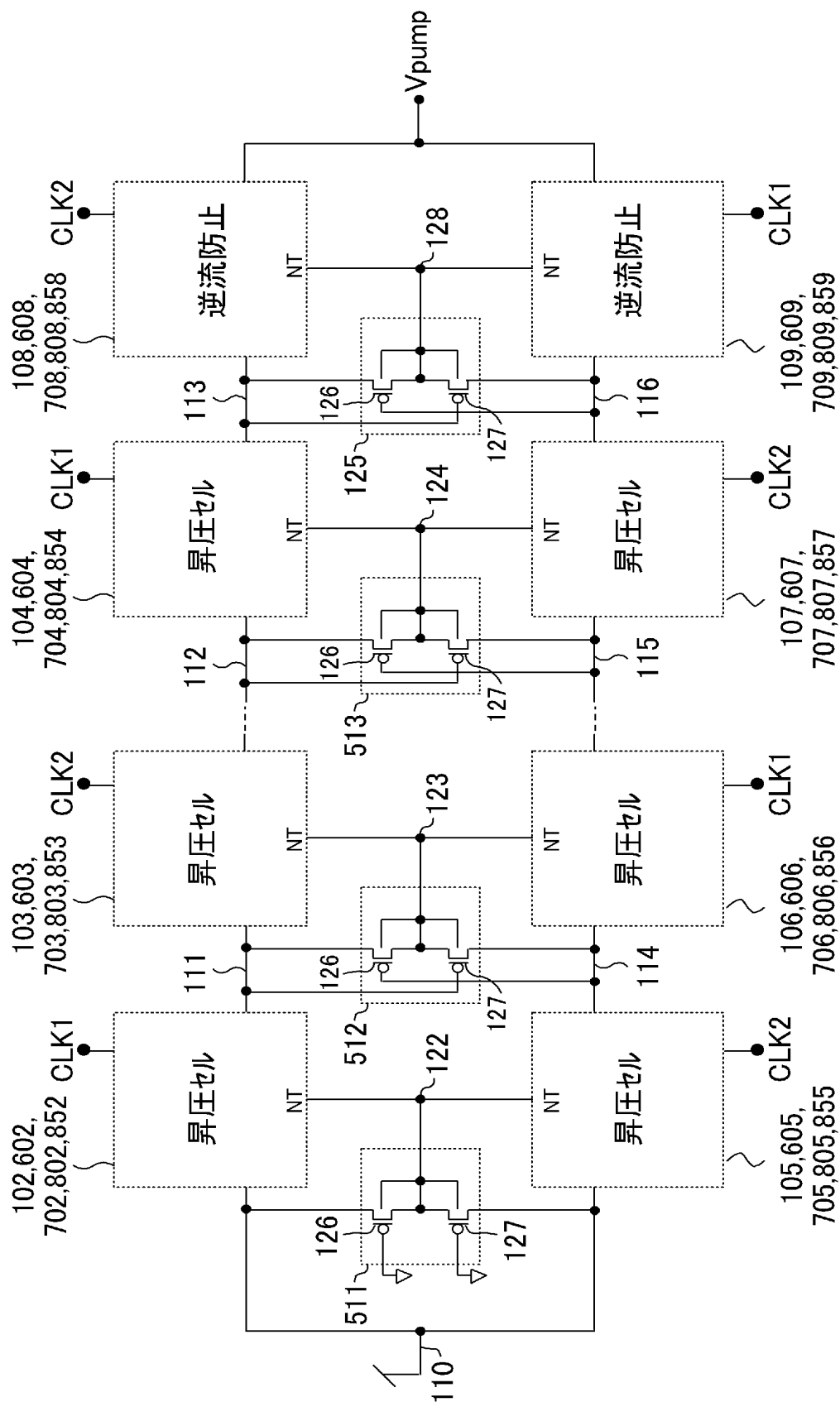




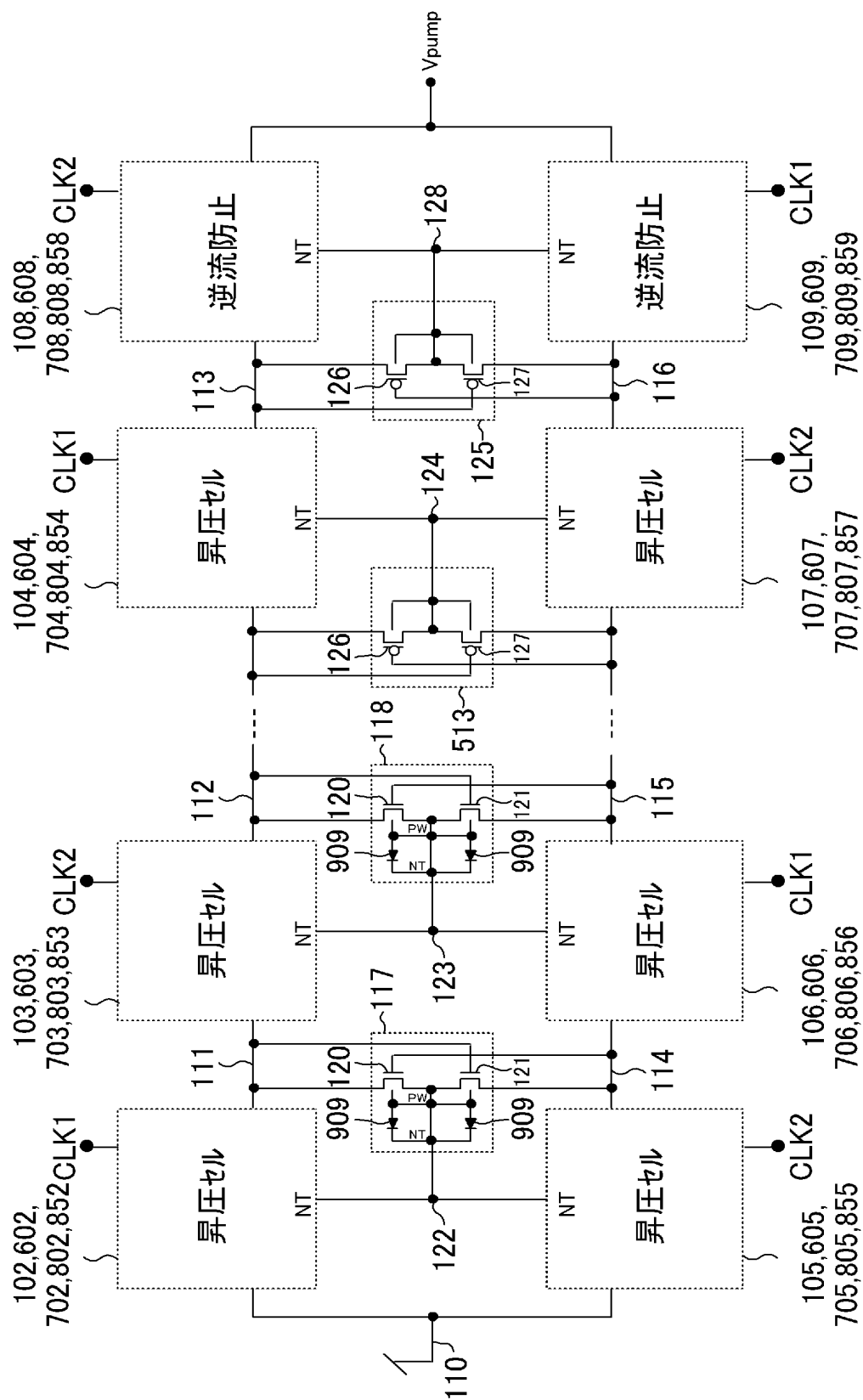




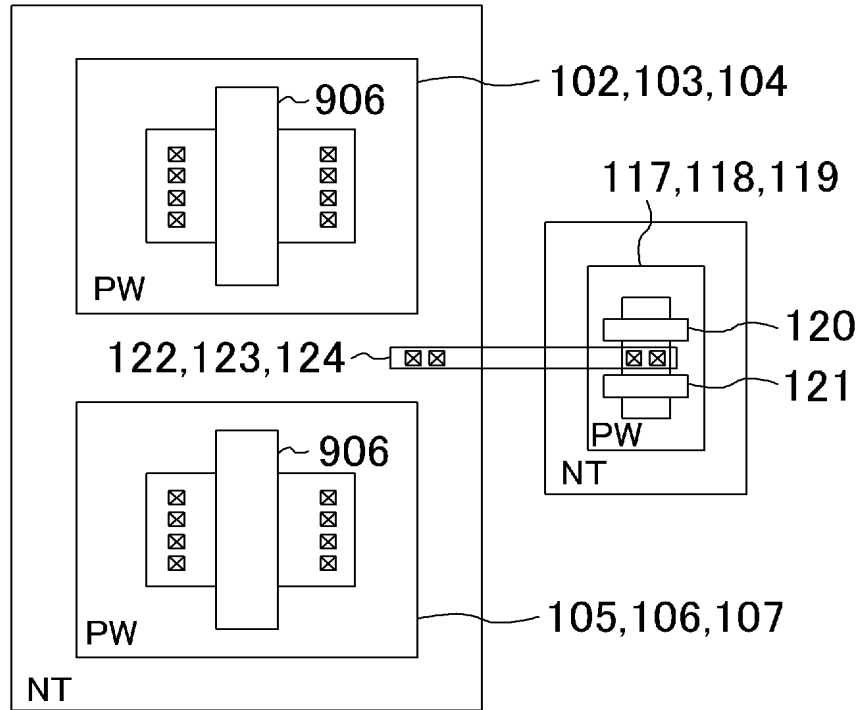
【図 13】



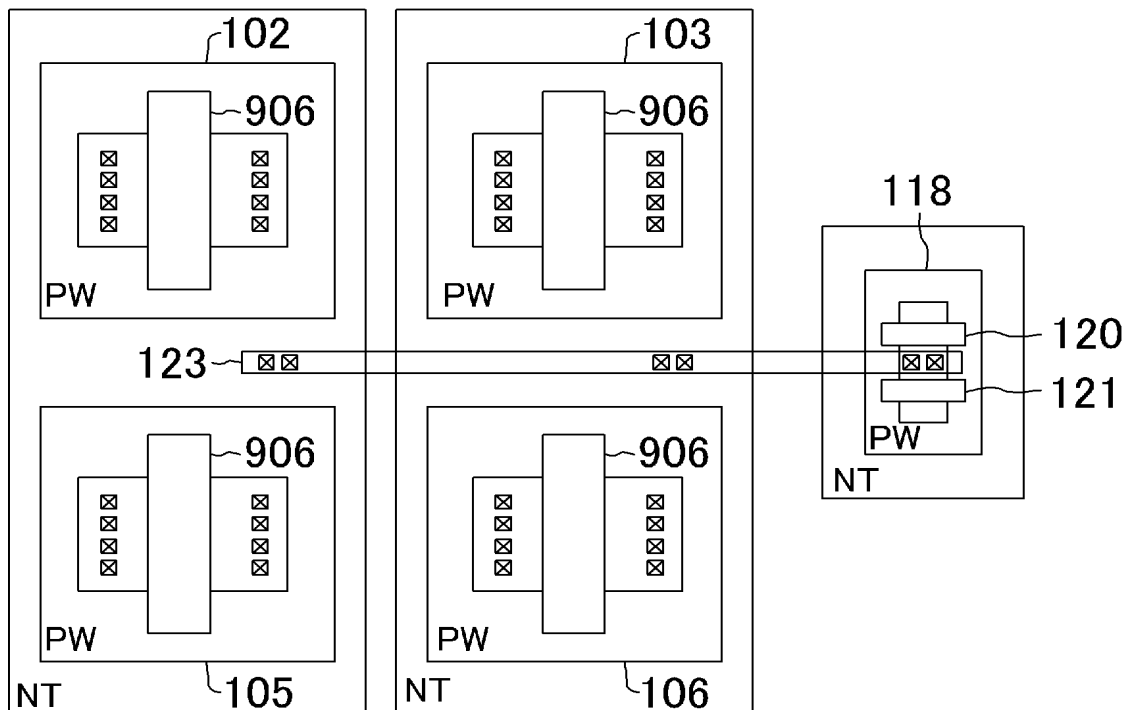
【図 14】



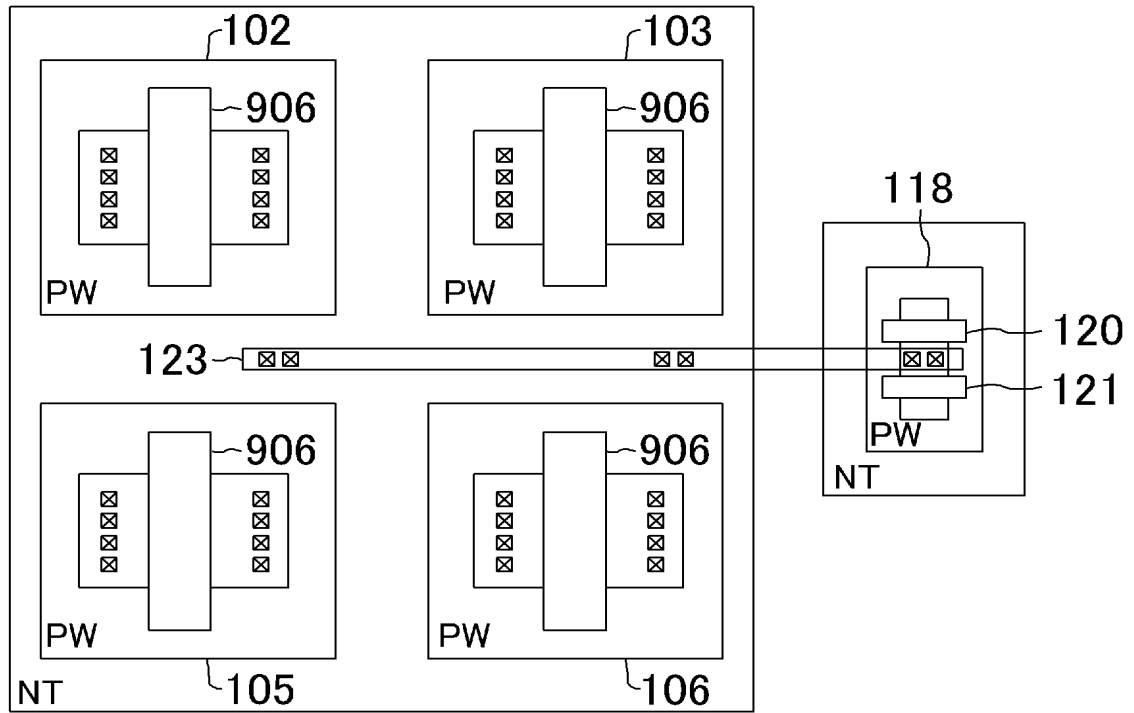
【図 1 5】



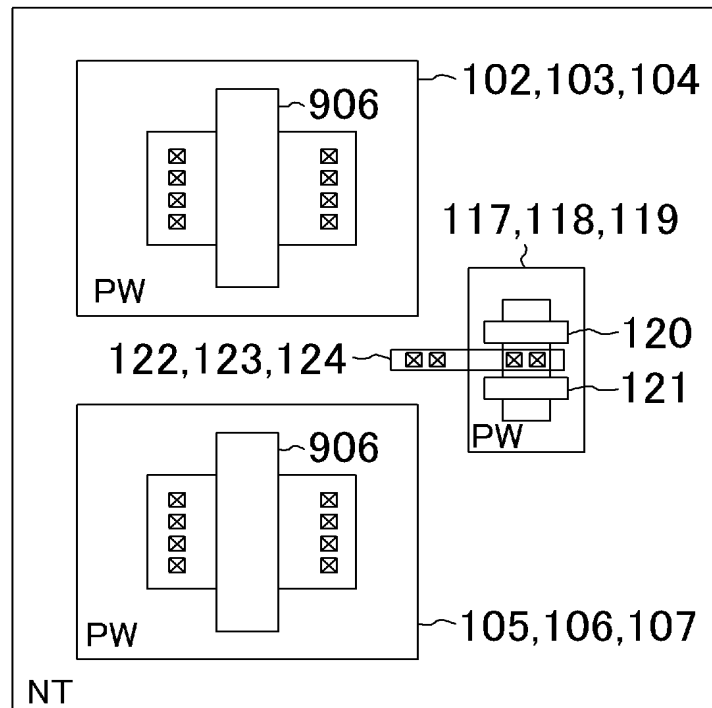
【図 1 6】



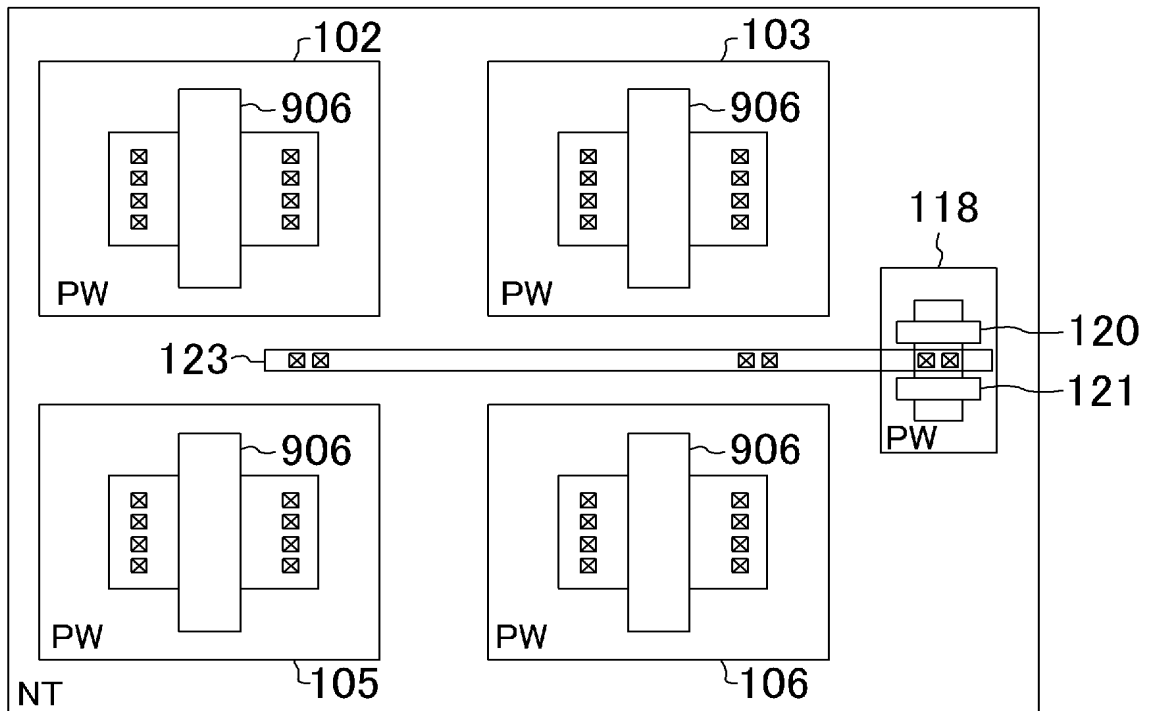
【図 1 7】



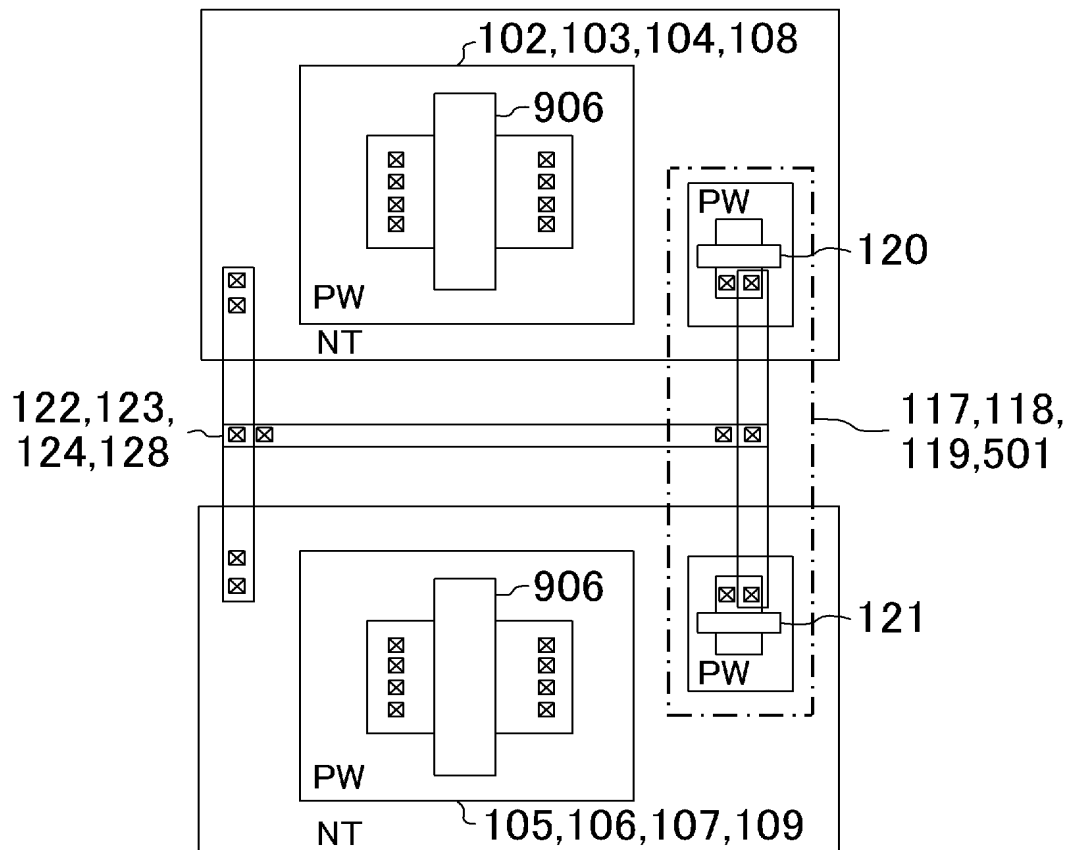
【図 1 8】



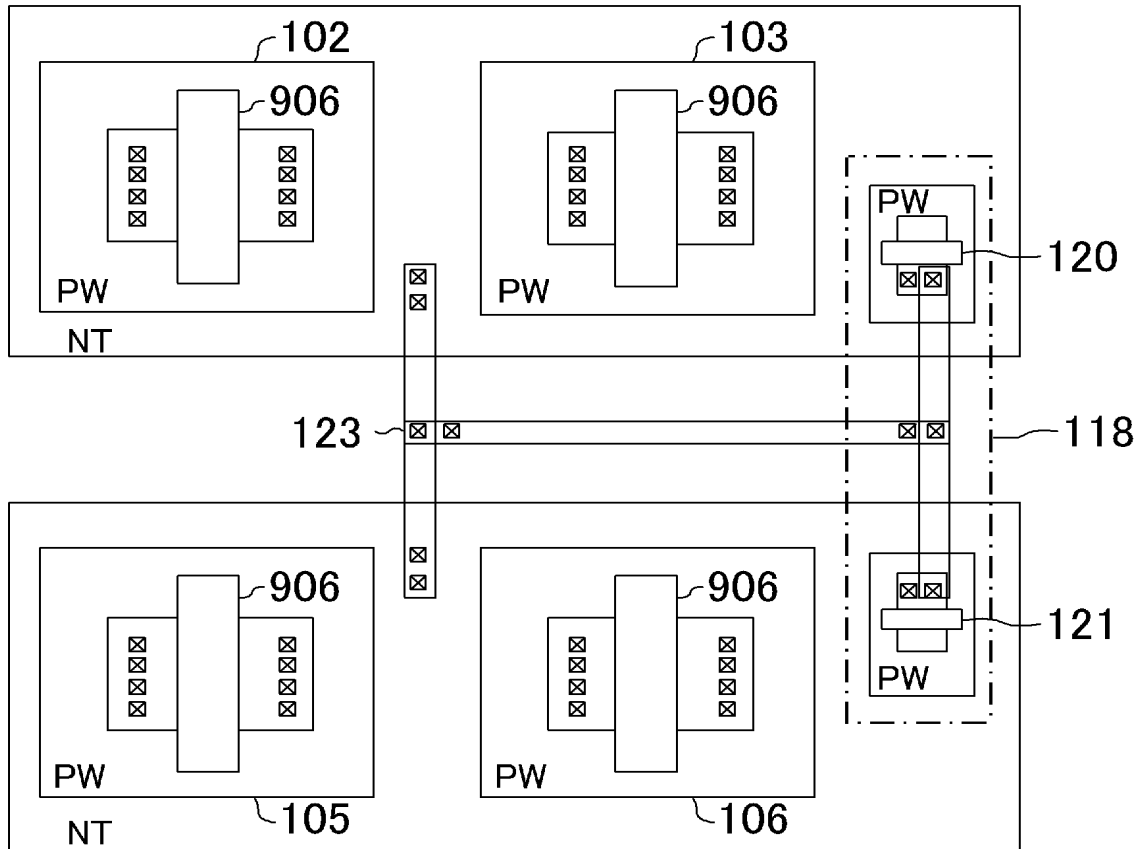
【図 19】



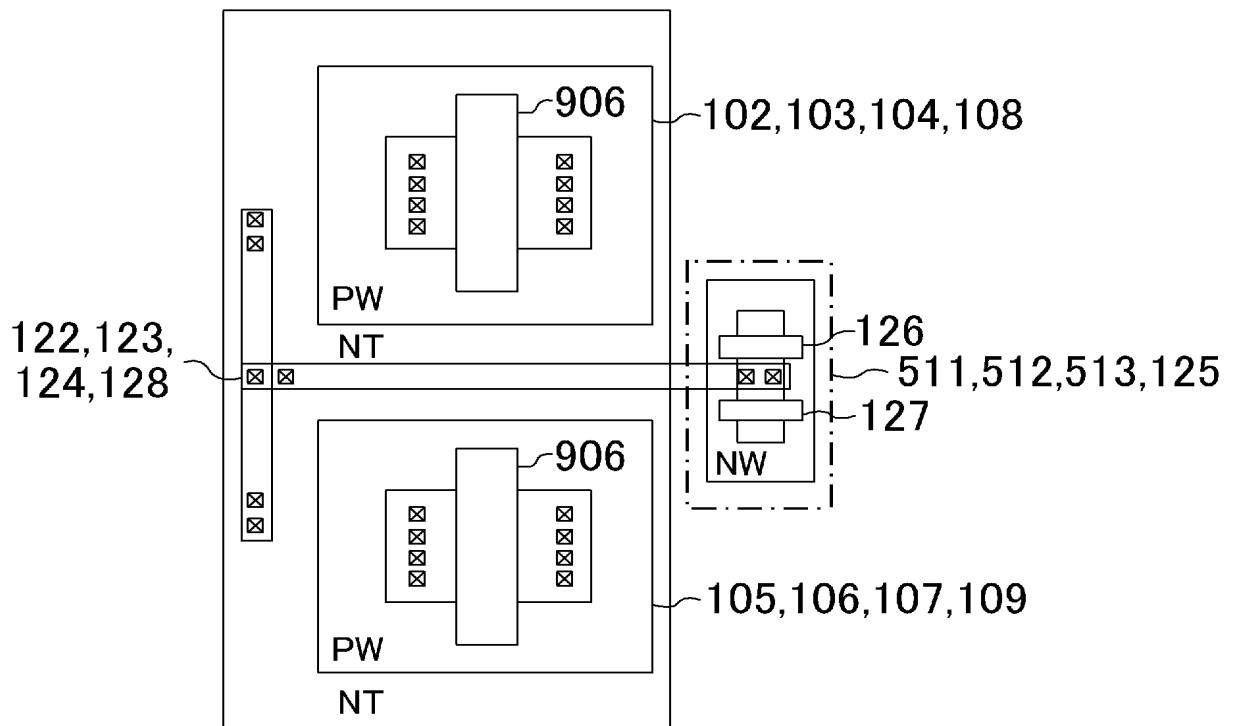
【図 20】



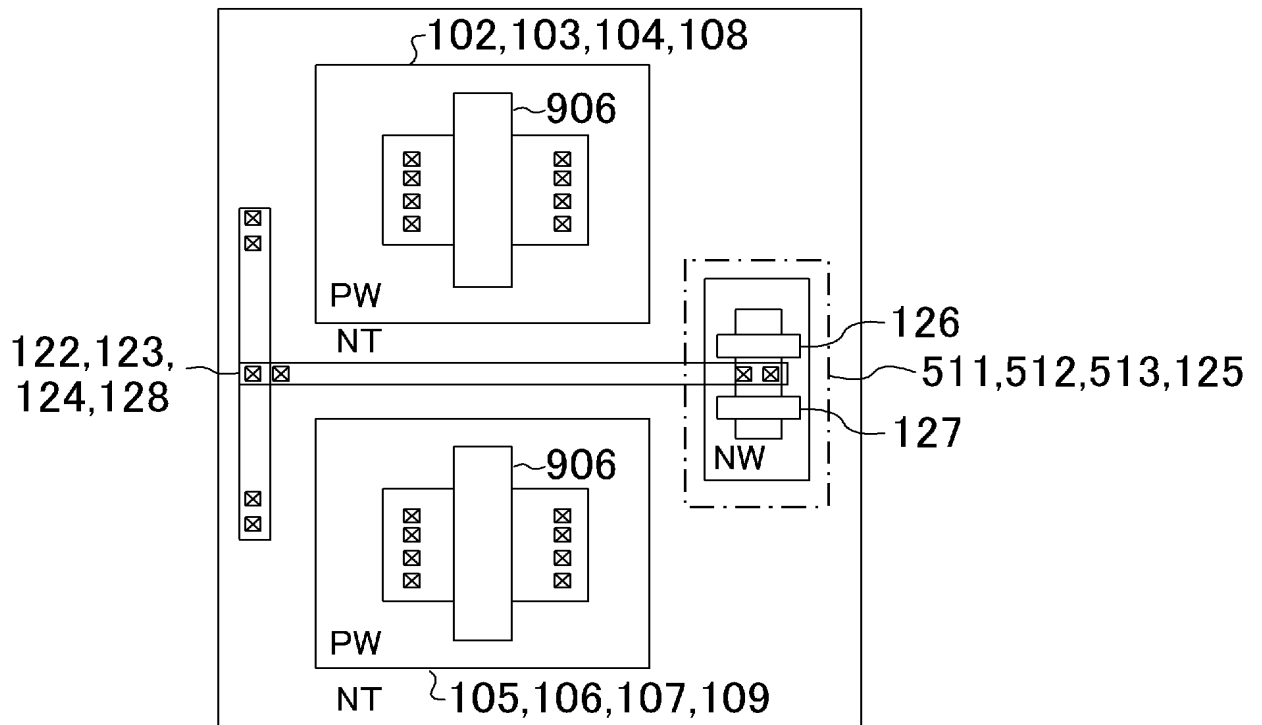
【図 2 1】



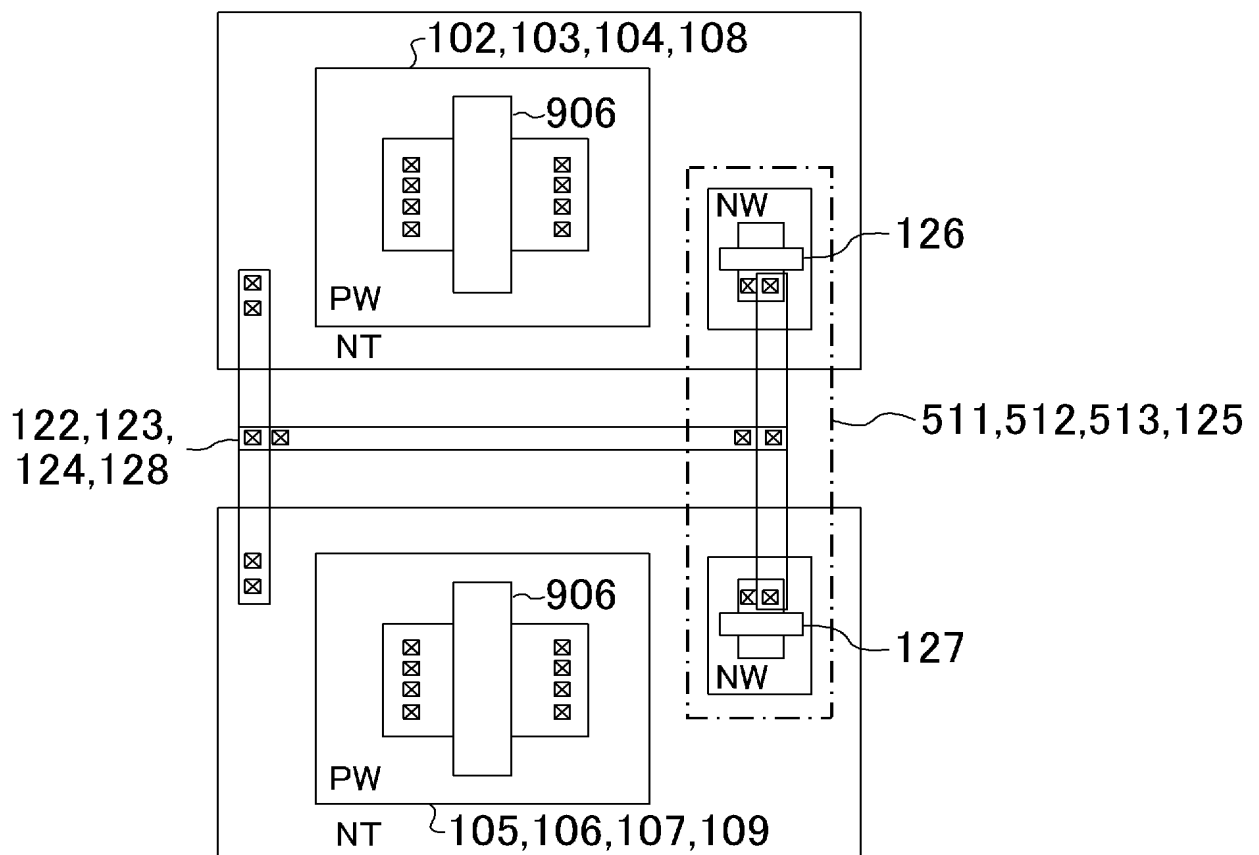
【図 2 2】

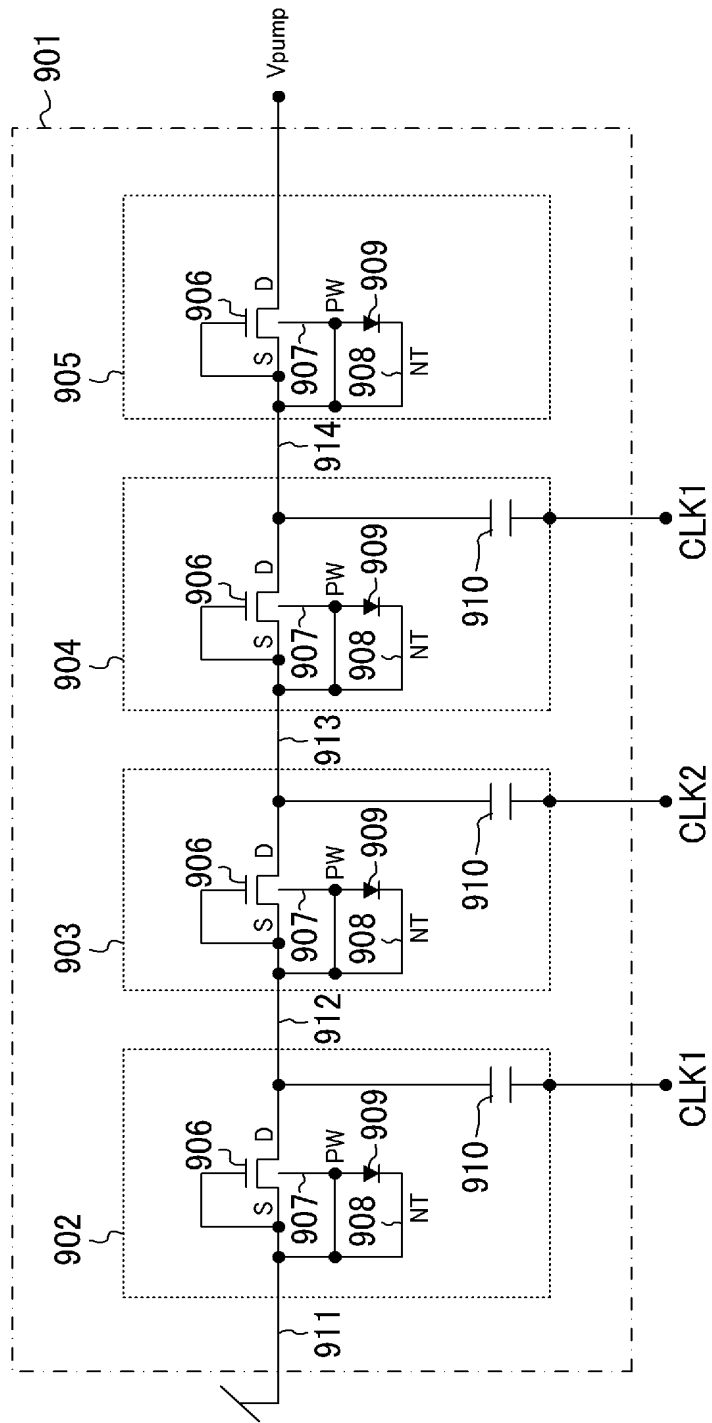


【図 2 3】

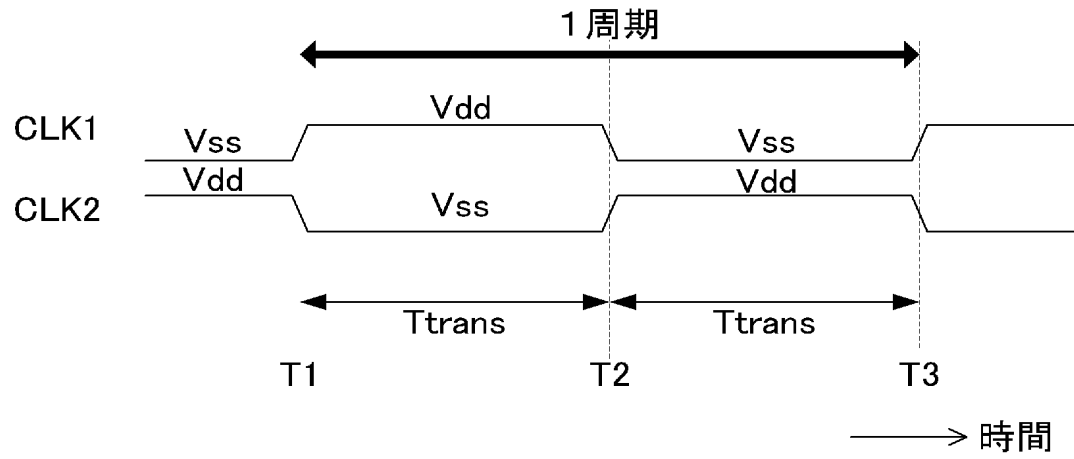


【図 2 4】





【図 2 6】



【書類名】 要約書

【要約】

【課題】 電荷転送効率の低下を抑制し、トリプルウエル構造を持つスイッチング素子のNウエル電位を制御することで、低消費電力化とレイアウト面積削減とを可能とする。

【解決手段】 第1の昇圧セル列102, 103, 104と、第2の昇圧セル列105, 106, 107とを備え、各々の昇圧セルの同じ段の電位を比較し、低い側の電位又は高い側の電位を選択して出力するアナログ比較回路117, 118, 119を更に備え、これらアナログ比較回路の出力電位により、Nウエル（NT）の電位を制御する。これにより、Nウエル電位の振幅を抑制し、かつNウエル領域のレイアウトの共通化を可能とする。

【選択図】 図1

出願人履歴

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新規登録

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パナソニック株式会社



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/836,122

07/14/2010

Seiji Yamahira

085393-0241

1536

53080 7590 08/11/2010
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

ZWEIZIG, JEFFERY SHAWN

ART UNIT

PAPER NUMBER

2816

MAIL DATE

DELIVERY MODE

08/11/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/836,122	Applicant(s) YAMAHIRA, SEIJI	
	Examiner Jeffrey S. Zweizig	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 16-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16-26 is/are allowed.
- 6) ☒ Claim(s) 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 July 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>7/14/10</u> . | 6) ☐ Other: _____ |

Specification

The beginning of the specification should be amended to include the patent number of the parent application (7,777,557).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 27 is rejected under 35 U.S.C. 102(b) as being anticipated by Miki (6,121,821).

Fig. 9 shows a first row 3 and a second row 4. Fig. 6 shows an ON/OFF switch MJn with a substrate 200, first well 210 and second well 220. Referring back to Fig. 9, the first well of MJ0, for example, is controlled by Vcc, which is also input to the cells of the first row and the second row. Likewise, the first well of MJ2, for example, is controlled by #3, which is also input to the cells of the first and second rows. Claim 27 is anticipated.

Conclusion

Claims 16-26 appear to be allowable over the Prior Art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

536f1
/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

Search Notes 	Application/Control No. 12836122	Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI
	Examiner Jeffrey S Zweizig	Art Unit 2816

SEARCHED			
Class	Subclass	Date	Examiner
327	535, 536, 537	8/9/10	/JJZ/

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

--	--

SHEET 1 OF 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 085393-0241		SERIAL NO. Divisional of U.S. Serial No. 12/015,882	
				APPLICANT Seiji YAMAHIRA			
				FILING DATE July 14, 2010		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codez (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 6,100,557	08-08-2000	HUNG et al.	<div style="border: 1px solid black; width: 100%; height: 100%; position: relative;"> </div>		
		US 6,121,821	09-19-2000	MIKI			
		US 6,878,981 B2	04-12-2005	ESHEL			
		US 6,888,400 B2	05-03-2005	LIN et al.			
		US 7,102,422 B1	09-05-2006	SAWADA et al.			
		US 6,734,717 B2	05-11-2004	MIN			
		US 6,952,129 B2	10-04-2005	LIN et al.			
		US 7,123,077 B2	10-17-2006	CHIU et al.			
		US 2007/0096796 A1	05-03-2007	FIRMANSYAH et al.			
		US 7,532,062	05-2009	Namekawa et al.			
		US 7,317,347	01-2008	Mesi et al.			
		US 6,501,325	12-2002	Meng, Anita			
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER /Jeffery Zweizig/				DATE CONSIDERED 08/09/2010			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered.
 Include copy of this form with next communication to applicant.
 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,122	07/14/2010	Seiji Yamahira	085393-0241

CONFIRMATION NO. 1536

PUBLICATION NOTICE



OC000000044346019

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Title:BOOSTER CIRCUIT

Publication No.US-2010-0277228-A1

Publication Date:11/04/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Docket No.: 085393-0241

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: 1536
	:	
Application No.: 12/836,122	:	Group Art Unit: 2816
	:	
Filed: July 14, 2010	:	Examiner: ZWEIZIG, JEFFERY SHAWN
	:	
For: BOOSTER CIRCUIT	:	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated August 11, 2010, having a three-month shortened statutory period for response set to expire on November 11, 2010, and one-month extension of time up to and including December 11, 2010 is being filed concurrently herewith, reconsideration of the above-identified application is respectfully requested in view of the following amendments and remarks.

AMENDMENT TO THE SPECIFICATION

Please amend the specification of the instant application as follows:

Please amend the paragraph after the Title and before the “BACKGROUND OF THE INVENTION” as follows:

-- RELATED APPLICATIONS

This application is a Divisional of U.S. Patent Application No. 12/015,882, filed on January 17, 2008, now U.S. Patent Number 7,777,557, issued on August 17, 2010, claiming priority of Japanese Patent Application Nos. 2007-007694, filed on January 17, 2007, and 2007-307064, filed on November 28, 2007, the entire contents of each of which are hereby incorporated by reference. --

AMENDMENT TO THE CLAIMS

Please amend the claims of the instant application as follows:

1-15. (Cancelled)

16. (Previously presented) A booster circuit comprising:

a first boosting cell row including N stages ($N \geq 1$) of boosting cells;

a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and

at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row, wherein:

each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and

the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

17. (Previously presented) The booster circuit of claim 16, wherein:

the first boosting cell row includes at least one backflow preventing circuit;

the second boosting cell row includes at least one backflow preventing circuit; and

the well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.

18. (Previously presented) The booster circuit of claim 16, wherein the well bias potential is the higher potential out of the input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

19. (Previously presented) The booster circuit of claim 16, wherein the well bias potential is the lower potential out of the input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

20. (Previously presented) The booster circuit of claim 16, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.

21. (Previously presented) The booster circuit of claim 16, wherein the second well region and the first well region are connected to each other so that the second well region and the first well region have the same potential.

22. (Previously presented) The booster circuit of claim 16, wherein:

the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

the at least one analog comparison circuit is provided for each boosting cell stage in the first boosting cell row and the second boosting cell row.

23. (Previously presented) The booster circuit of claim 16, wherein:

the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

the at least one analog comparison circuit is provided for arbitrary number of boosting cell stages in the first boosting cell row and the second boosting cell row.

24. (Previously presented) The booster circuit of claim 16, wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

25. (Previously presented) The booster circuit of claim 16, wherein:

the at least one switching element of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

the at least one switching element of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

26. (Previously presented) The booster circuit of claim 16, wherein an output potential of the analog comparison circuit is applied to the first well region of the at least one switching element included in a boosting cell of a boosting cell row different from the first and second boosting cell rows.

27. (Currently amended) A booster circuit comprising:
a first boosting cell row including N stages ($N \geq 2$) of boosting cells; and
a second boosting cell row including M stages ($M \geq 2$) of the boosting cells,
wherein:

each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal, ~~[[and]]~~

a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row and an input potential of the boosting cells of the second boosting cell row, and

an input potential of each of the boosting cells of the first boosting cell row is different from an input potential of each of the boosting cells of the second boosting cell row.

REMARKS

In view of the foregoing amendments and the following remarks, Applicants respectfully submit the instant application is in condition for allowance, an indication of which is respectfully requested.

Patentability - 35 U.S.C. § 102

Claim 27 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Number 6,121,821 ("Miki"). This rejection is traversed for at least the following reasons.

Applicants respectfully submit that Miki, at a minimum, fails to describe or suggest a booster circuit that includes, among other features, a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row *and* an input potential of the boosting cells of the second boosting cell row, and an input potential of each of the boosting cells of the first boosting cell row is *different* from an input potential of each of the boosting cells of the second boosting cell row, as recited in amended claim 27. Support for this amendment may be found in the instant application at, for example, page 13, lines 2-5; page 16, lines 15-17; and FIG. 6.

Miki, in FIG. 9, shows that the potential of the first well region of the alleged switching element MJ_n included in the boosting cells is controlled according to one type of input potential and *not* two different types of input potentials. For example, as noted in the Office Action, the potential of the first well of MJ₀ is controlled by V_{cc}, and the potential of the first well of MJ₂ is controlled by clock #3. However, Miki fails to show that a potential of the first well region in

the boosting cells on a second stage or stages succeeding the second stage is controlled by two different types of input potentials.

As such, Miki fails to describe or suggest a booster circuit that includes, among other features, a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row *and* an input potential of the boosting cells of the second boosting cell row, and an input potential of each of the boosting cells of the first boosting cell row is *different* from an input potential of each of the boosting cells of the second boosting cell row, as recited in amended claim 27.

For at least the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 27.

Conclusion

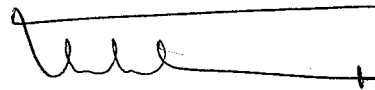
Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Application No.: 12/836,122

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read 'Babak Akhlaghi', written over a horizontal line.

Babak Akhlaghi
Limited Recognition No. L0250

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BA:MWE
Facsimile: 202.756.8087
Date: December 13, 2010

**Please recognize our Customer No. 53080
as our correspondence address.**

Electronic Patent Application Fee Transmittal

Application Number:	12836122			
Filing Date:	14-Jul-2010			
Title of Invention:	BOOSTER CIRCUIT			
First Named Inventor/Applicant Name:	Seiji Yamahira			
Filer:	Michael E. Fogarty/3328/Matilda Mason			
Attorney Docket Number:	085393-0241			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				130

Electronic Acknowledgement Receipt

EFS ID:	9026192
Application Number:	12836122
International Application Number:	
Confirmation Number:	1536
Title of Invention:	BOOSTER CIRCUIT
First Named Inventor/Applicant Name:	Seiji Yamahira
Customer Number:	53080
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0241
Receipt Date:	13-DEC-2010
Filing Date:	14-JUL-2010
Time Stamp:	22:17:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 130
RAM confirmation Number	7450
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous Fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		085393-0241EOT.pdf	311068 18cca935998b5d925736fd94b2ec580b714241e3	yes	11
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Extension of Time		1	1	
	Amendment/Req. Reconsideration-After Non-Final Reject		2	2	
	Specification		3	3	
	Claims		4	8	
	Applicant Arguments/Remarks Made in an Amendment		9	11	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30161 d83973e50d579a25cdcb0d67c1ce0fbc32664bef	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			341229		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Docket No.: 085393-0241

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
Seiji YAMAHIRA	:	Confirmation Number: 1536
Application No.: 12/836,122	:	Group Art Unit: 2816
Filed: July 14, 2010	:	Examiner: ZWEIZIG, JEFFERY SHAWN
For: BOOSTER CIRCUIT	:	

PETITION FOR EXTENSION OF TIME

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

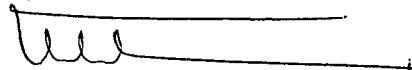
Sir:

It is respectfully requested that the time for response to the Office Action dated August 11, 2010, now due to expire November 11, 2010, be extended for one month(s) and set to expire on December 11, 2010 (Saturday).

Please charge the extension fee of \$130.00 to Deposit Account No. 500417. Please charge any additional fees or credit any overpayment to Deposit Account No. 500417.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Babak Akhlaghi
Limited Recognition No. L0250

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 BA:MWE
Facsimile: 202.756.8087
Date: December 13, 2010

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as our correspondence address.**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/836,122		Filing Date 07/14/2010		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT	12/13/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X \$ =	OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	X \$ =	OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.</p>										

Legal Instrument Examiner:
/LINDA W. BADIE/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 01/07/2011

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

ZWEIZIG, JEFFERY SHAWN

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 01/07/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/836,122

07/14/2010

Seiji Yamahira

085393-0241

1536

TITLE OF INVENTION: BOOSTER CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/07/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 01/07/2011

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,122	07/14/2010	Seiji Yamahira	085393-0241	1536

TITLE OF INVENTION: BOOSTER CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/07/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZWEIZIG, JEFFERY SHAWN	2816	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,122	07/14/2010	Seiji Yamahira	085393-0241	1536
53080	7590	01/07/2011	EXAMINER	
MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			ZWEIZIG, JEFFERY SHAWN	
			ART UNIT	PAPER NUMBER
			2816	
DATE MAILED: 01/07/2011				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/836,122	YAMAHIRA, SEIJI	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 12/13/10.
2. ☒ The allowed claim(s) is/are 16-27.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 - * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☐ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other _____. |

/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

<i>Issue Classification</i> 	Application/Control No. 12836122	Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI
	Examiner Jeffrey S Zweizig	Art Unit 2816

[illegible][illegible]

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/Jeffrey S Zwezig/ Primary Examiner.Art Unit 2816	12/27/10	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

Search Notes 	Application/Control No. 12836122	Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI
	Examiner Jeffrey S Zweizig	Art Unit 2816

SEARCHED			
Class	Subclass	Date	Examiner
327	535, 536, 537	8/9/10	/JZ/
update	above	12/27/10	/JZ/

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
327	536	12/27/10	/JZ/

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BIB DATA SHEET

CONFIRMATION NO. 1536

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/836,122	07/14/2010	327	2816	085393-0241		
RULE						
APPLICANTS Seiji Yamahira, Kyoto, JAPAN; ** CONTINUING DATA ***** This application is a DIV of 12/015,882 01/17/2008 PAT 7,777,557 /JZ/ ** FOREIGN APPLICATIONS ***** JAPAN 2007-007694 01/17/2007 /JZ/ JAPAN 2007-307064 11/28/2007 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/23/2010						
Foreign Priority claimed ☒ Yes ☐ No	35 USC 119(a-d) conditions met ☒ Yes ☐ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Verified and /JEFFREY SHAWN ZWEIZIG/ Acknowledged Examiner's Signature		Initials	JAPAN	21	12	2
ADDRESS MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096 UNITED STATES						
TITLE BOOSTER CIRCUIT						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
			☐ Credit			

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

53080 7590 01/07/2011

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Customer No: 53080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,122	07/14/2010	Seiji Yamahira	085393-0241	1536

TITLE OF INVENTION: BOOSTER CIRCUIT

APPL. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	04/07/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZWEIZIG, JEFFERY SHAWN	2816	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

MCDERMOTT WILL & EMERY LLP
 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PANASONIC CORPORATION

Osaka, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies **Four (4)**

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **500417** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date **March 1, 2011**

Typed or printed name **Michael E. Fogarty**

Registration No. **36,139**

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	12836122			
Filing Date:	14-Jul-2010			
Title of Invention:	BOOSTER CIRCUIT			
First Named Inventor/Applicant Name:	Seiji Yamahira			
Filer:	Michael E. Fogarty/stephanie sharrett			
Attorney Docket Number:	085393-0241			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				1822

Electronic Acknowledgement Receipt

EFS ID:	9563062
Application Number:	12836122
International Application Number:	
Confirmation Number:	1536
Title of Invention:	BOOSTER CIRCUIT
First Named Inventor/Applicant Name:	Seiji Yamahira
Customer Number:	53080
Filer:	Michael E. Fogarty/stephanie sharrett
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	085393-0241
Receipt Date:	01-MAR-2011
Filing Date:	14-JUL-2010
Time Stamp:	17:04:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1822
RAM confirmation Number	3948
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /Zip	Pages (if appl.)
		SK hynix Ex_1002	Page 180 of 191		

1	Issue Fee Payment (PTO-85B)	IF.PDF	100079 a52696cd8f460d721d66c4473b11f1dd87ccf33	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33471 95ed705857db275f94ec831ec3c2018148a6dfa3	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			133550		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/836,122	04/05/2011	7920018	085393-0241	1536

53080 7590 03/16/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Seiji Yamahira, Kyoto, JAPAN;

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PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	7920018
	Issue Date	Apr 5, 2011
	First Named Inventor	Seiji YAMAHIRA
	Title	BOOSTER CIRCUIT
	Attorney Docket No.	0870-04135 US

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

27197

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

Country

Telephone

State

Zip

I am the:

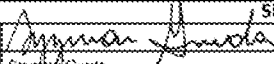
☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature		Date	December 28, 2024
Name	Seiji Yamahira	Telephone	
Title and Company	Authorized Signatory, ADVANCED MEMORY TECHNOLOGIES LLC		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: ADVANCED MEMORY TECHNOLOGIES LLCApplication No./Patent No.: 7920018Filed/Issue Date: April 5, 2011Titled: BOOSTER CIRCUITADVANCED MEMORY TECHNOLOGIES LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: the inventor(s) To: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.The document was recorded in the United States Patent and Trademark Office at
Reel 021034, Frame 0634, or for which a copy thereof is attached.2. From: MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD. To: PANASONIC CORPORATIONThe document was recorded in the United States Patent and Trademark Office at
Reel 021897, Frame 0516, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

SK hynix Ex. 1002, Page 185 of 191

STATEMENT UNDER 37 CFR 3.73(c)

3. From: PANASONIC CORPORATION To: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD.

The document was recorded in the United States Patent and Trademark Office at
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4. From: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD. To: NUVOTON TECHNOLOGY CORPORATION JAPAN

The document was recorded in the United States Patent and Trademark Office at
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5. From: NUVOTON TECHNOLOGY CORPORATION JAPAN To: ADVANCED MEMORY TECHNOLOGIES LLC

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/

Signature

Szymon M. Gurda

Printed or Typed Name

December 30, 2024

Date

58451

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
12/836,122

RECEIPT DATE / TIME
12/30/2024 10:23:10 PM Z ET

ATTORNEY DOCKET #
085393-0241

Title of Invention

BOOSTER CIRCUIT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 7920018

CONFIRMATION # 1536

FILED BY Yi Lu

PATENT CENTER # 68561140

FILING DATE 07/14/2010

CUSTOMER # 53080

FIRST NAMED
INVENTOR Seiji Yamahira

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA.pdf	2	Power of Attorney	1147 KB
aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	121 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA.pdf	50CB5FC9D64C98F6A0260403507A7D35AFB95AFFE9CFAED3 4BB726C12E4851FF8CB0488BDE54269B4FB39A1E4961289CA 4879325C464800F1AEB7028647D9EBD
aia0096.pdf	2317EE3569A6903E7F26200B29928C1B4E91D9530700577CC6 255A6D7F401573EB4B47DC01EEF7D0D337BC94AA868F70FC

93697EE53483D5C787AA98224EA767

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,122	07/14/2010	Seiji Yamahira	085393-0241

CONFIRMATION NO. 1536

53080
Rimon PC - Panasonic Corporation
8300 Greensboro Dr.
Suite 500
McLean, VA 22102

POWER OF ATTORNEY NOTICE



OC000000082992047

Date Mailed: 01/14/2025

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/836,122	07/14/2010	Seiji Yamahira	085393-0241

27197
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CONFIRMATION NO. 1536
POA ACCEPTANCE LETTER



OC000000082992076

Date Mailed: 01/14/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/