Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes

Ming-Dou Ker, *Senior Member, IEEE*, Shih-Lun Chen, *Student Member, IEEE*, and Chia-Shen Tsai

***Abstract*—A new charge pump circuit with consideration of gate-oxide reliability is designed with two pumping branches in this paper. The charge transfer switches in the new proposed circuit can be completely turned on and turned off, so its pumping efficiency is higher than that of the traditional designs. Moreover, the maximum gate-source and gate-drain voltages of all devices in the proposed charge pump circuit do not exceed the normal operating power supply voltage (VDD). Two test chips have been implemented in a 0.35-μm 3.3-V CMOS process to verify the new proposed charge pump circuit. The measured output voltage of the new proposed four-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive output load is around 8.8 V under 3.3-V power supply (VDD = 3.3 V), which is limited by the junction breakdown voltage of the parasitic pn-junction in the given process. The new proposed circuit is suitable for applications in low-voltage CMOS processes because of its high pumping efficiency and no overstress across the gate oxide of devices.**

***Index Terms*—Body effect, charge pump circuit, gate-oxide reliability, high-voltage generator, low voltage.**

I. Introduction

CHARGE pump circuits have been often used to generate dc voltages those are higher than the normal power supply voltage (VDD) or lower than the ground voltage (GND) of the chip. Charge pump circuits are usually applied to the nonvolatile memories, such as EEPROM or flash memories, to write or to erase the floating-gate devices [1]–[4]. In addition, charge pump circuits had been used in some low-voltage designs to improve the circuit performance [5], [6]. The four-stage diode charge pump circuit using the pn-junction diodes as the charge transfer devices is shown in Fig. 1(a). The charges are pushed from the power supply (VDD) to the output node ($V_{\rm out}$), stage by stage. Thus, the output voltage of the charge pump circuit can be pumped high. The voltage fluctuation of each pumping node can be expressed as

$$\Delta V = V_{\rm clk} \cdot \frac{C_{\rm pump}}{C_{\rm pump} + C_{\rm par}} - \frac{I_o}{f \cdot (C_{\rm pump} + C_{\rm par})} \quad (1)$$

where $V_{\rm clk}$ is the voltage amplitude of the clock signals, $C_{\rm pump}$ is the pumping capacitance, $C_{\rm par}$ is the parasitic capacitance at each pumping node, I_o is output current, and f is the clock frequency. If $C_{\rm par}$ and I_o are small enough and $C_{\rm pump}$ is large enough, $C_{\rm par}$ and I_o can be ignored from (1). Because $V_{\rm clk}$ is usually with the same voltage level as the normal power supply voltage (VDD), the voltage fluctuation of each pumping node can be simply expressed as

$$\Delta V \approx V_{\rm clk} = {\rm VDD}. \quad (2)$$

Hence, the output voltage of the four-stage charge pump circuit with diodes can be expressed as

$$V_{\rm out} = 5 \cdot ({\rm VDD} - V_D) \quad (3)$$

where V_D is the cut-in voltage of the pn-junction diode. However, it is difficult to implement the fully independent diodes in the common silicon substrate. In other words, the charge pump circuit with diodes shown in Fig. 1(a) cannot be easily integrated into the standard CMOS process. Therefore, most charge pump circuits are based on the circuit proposed by Dickson [7]–[9]. Fig. 1(b) shows the four-stage Dickson charge pump circuit, where the diode-connected MOSFETs are used to transfer the charges from the present stage to the next stage. Thus, it can be easily integrated into standard CMOS processes. However, the voltage difference between the drain terminal and the source terminal of the diode-connected MOSFET is the threshold voltage when the diode-connected MOSFET is turned on. Therefore,

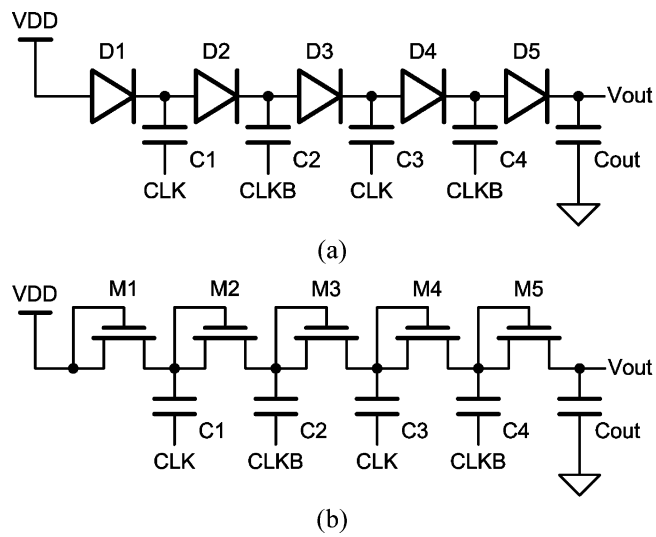

Fig. 1. Four-stage (a) diode and (b) Dickson charge pump circuits.

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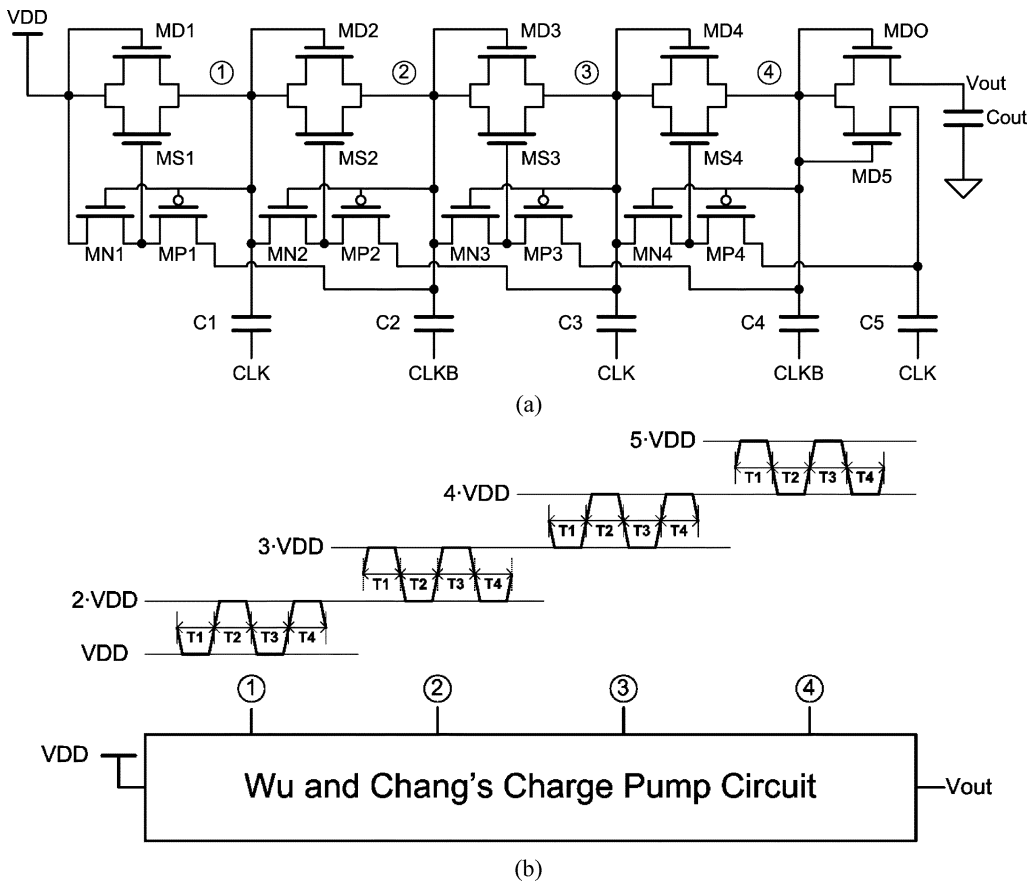

Fig. 2. (a) Circuit and (b) corresponding voltage waveforms of the four-stage Wu and Chang charge pump circuit.

the output voltage of the four-stage Dickson charge pump circuit has been derived as

$$V_{\text{out}} = \sum_{i=1}^{5} \left(\text{VDD} - V_{t(M_i)}\right) \tag{4}$$

where $V_{t(Mi)}$ denotes the threshold voltage of the diode-connected MOSFET Mi. Traditionally, the bulk terminals of the diode-connected MOSFETs in the Dickson charge pump circuit are connected to ground (GND). The threshold voltage $(V_{t(Mi)})$ of the diode-connected MOSFET becomes larger due to the body effect when the voltage on each pumping node is pumped higher. Therefore, the pumping efficiency of the Dickson charge pump circuit is degraded by the body effect when the number of pumping stages is increased.

Several modified charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency [10]–[18]. In the triple-well process, the floating-well technique [10] or the source-bulk connected devices were used to eliminate the body effect issue on the diode-connected MOSFETs in the Dickson charge pump circuit. But, the floating-well technique may generate substrate current in the floating-well devices to influence other circuits in the same chip. The source-bulk connected technique increases the parasitic capacitance at each pumping node due to the large bulk-to-well pn-junction capacitance, so the pumping capacitors have to be enlarged. The auxiliary MOSFETs used to dynamically control the body terminals of the diode-connected MOSFETs [11] may also generate the substrate current in the floating-well devices. Four-phase clock generator was applied in the charge pump circuits to improve pumping efficiency [12]–[15], but the complex clock generator would consume more power. In [16], [17], an extra small charge pump circuit, which has more pumping stages than the main charge pump circuit, was used to control the main charge pump circuit, so the pumping efficiency of the main charge pump circuit can be enhanced. However, the charge pump circuits [16], [17] occupy larger silicon area than others because of the extra charge pump circuits. In addition, the extra small charge pump circuit consumes extra power. In [18], the charge sharing concept was used in the charge pump circuit to reduce the power consumption. However, the charge sharing concept requires the special clock generator. The four-stage charge pump circuit reported by Wu and Chang [19] is shown in Fig. 2(a). The charge transfer switch (CTS) controlled by the dynamic control circuit in the Wu and Chang charge pump circuit is used to transfer the charges from the present stage to the next stage without suffering the limitation of threshold voltage. Fig. 2(b) shows the corresponding voltage waveforms of the four-stage Wu and Chang charge pump circuit. When the clock signal CLK is low and the clock signal CLKB is high during the time interval T1 in Fig. 2(b), the voltage on node 1 is VDD and the voltage on node 2 is $3 \times$ VDD. Because transistor MN1 is turned off and transistor MP1 is turned on,

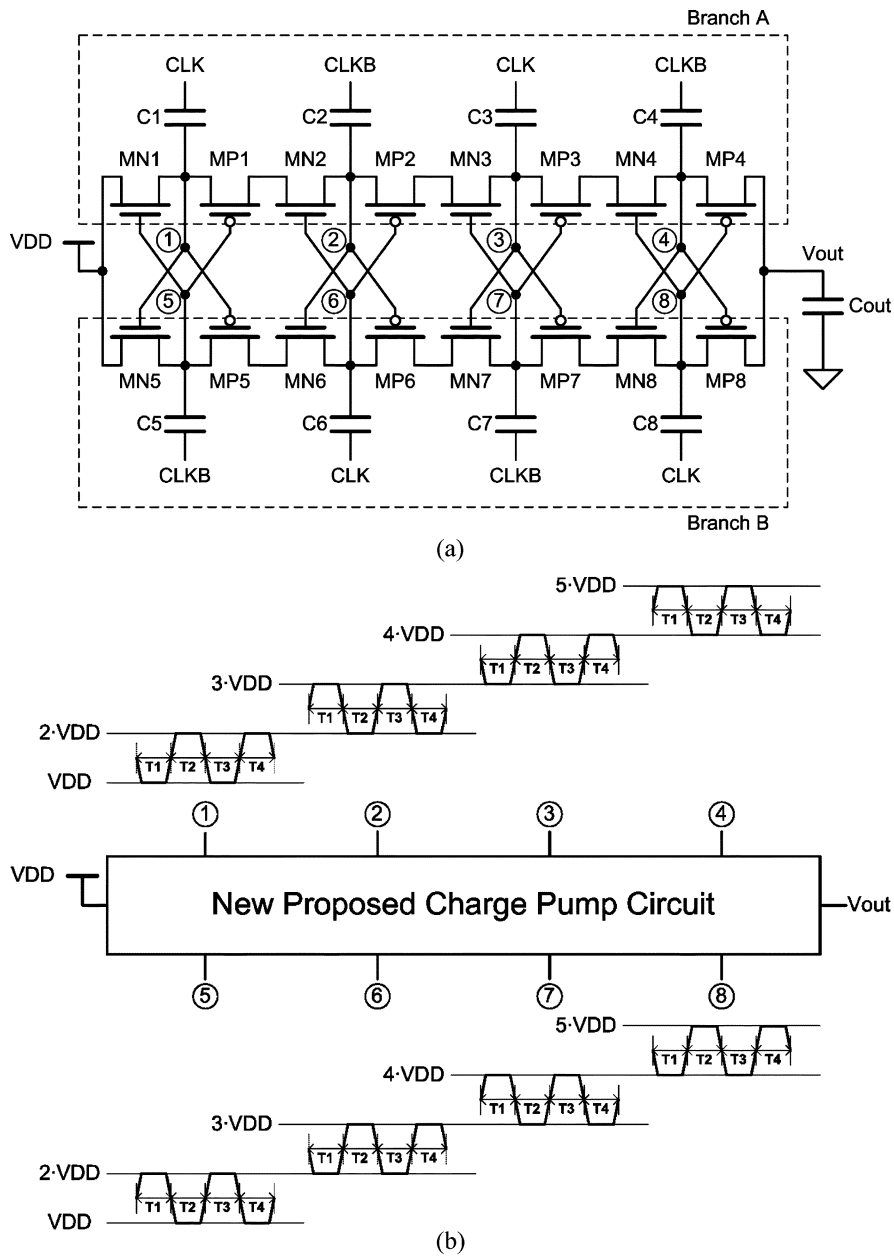

Fig. 3. (a) Circuit and (b) corresponding waveforms of the new proposed charge pump circuit with four pumping stages.

the charge transfer switch, MS1, can be completely turned on to transfer charges from the power supply (VDD) to node 1. During the time interval T2, the voltage on node 2 can be pumped as high as $2 \times$ VDD to turn on transistor MN1 and to turn off transistor MP1. Thus, the charge transfer switch, MS1, can be completely turned off to prevent the charges back to the power supply (VDD). The operation of next stages in Wu and Chang's charge pump circuit is similar to that of the first stage. Because the CTSs can be completely turned on or turned off by the dynamic control circuits, the pumping efficiency has been enhanced with ideal output voltage of $5 \times$ VDD. However, the output stage (MDO) of Wu and Chang's charge pump circuit is still a diode-connected MOSFET, so it also suffers the body effect issue. Besides, because the maximum voltage difference of each stage is $2 \times$ VDD, all devices of Wu and Chang's charge pump circuit suffer the high-voltage overstress on their gate oxides.

With the advanced CMOS processes, the thickness of the gate oxide becomes thinner so the operation voltage of transistor must be lowered due to the reliability issue [20]. Thus, the gate-oxide reliability issue [21] must be also considered into the design of charge pump circuits, especially in the low-voltage CMOS processes. In this paper, a new charge pump circuit that has better pumping efficiency but without the gate-oxide reliability issue in low-voltage processes is proposed [22]. The new proposed charge pump circuit has been successfully verified in a 0.35-μm 3.3-V CMOS process.

II. New Proposed Charge Pump Circuit

The circuit and the corresponding voltage waveforms of the new proposed charge pump circuit with four stages are shown in Fig. 3(a) and (b). To avoid the body effect, the bulks of the devices in the proposed charge pump circuit are recommended to be connected to their sources respectively if the given process

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provides the deep n-well layer. Clock signals CLK and CLKB are out-of-phase but with the amplitudes of VDD. As shown in Fig. 3(a), there are two charge transfer branches, branch A and branch B, in the new proposed charge pump circuit. Branch A is comprised of transistors MN1, MN2, MN3, MN4, MP1, MP2, MP3, and MP4 with the capacitors C1, C2, C3, and C4. Branch B is comprised of transistors MN5, MN6, MN7, MN8, MP5, MP6, MP7, and MP8 with the capacitors C5, C6, C7, and C8. The control signals of branches A and B are intertwined. Besides, clock signals of branches A and B are out-of-phase. When the clock signals of the first and the third pumping stages in the branch A are CLK, those in the branch B are CLKB. Similarly, when the clock signals of the second and the forth pumping stages in the branch A are CLKB, those in the branch B are CLK. Thus, branches A and B can see as two independent charge pump circuits but their output nodes are connected together. Because the clock signals of the branch A and those of the branch B are out-of-phase, the voltage waveforms of nodes 1–4 and those of nodes 5–8 are also out-of-phase. Hence, branches A and B can pump the output voltage to high, alternately. The detailed operations of the new proposed charge pump circuit are described below.

A. First Pumping Stage

As illustrated in Fig. 3(b), the clock signal CLK is low and the clock signal CLKB is high during the time interval T1. At this moment, the voltage difference (V_{15}) between node 1 and node 5 is $-$VDD. Therefore, transistor MN1 is turned on to transfer the charges from the power supply (VDD) to node 1, but the transistor MN5 is turned off to cut off the path from node 5 back to the power supply. Similarly, V_{15} becomes VDD during the time interval T2. Transistor MN1 is turned off to cut off the leakage path from node 1 back to the power supply, but the transistor MN5 is turned on to transfer the charges from the power supply to node 5.

B. Second and Third Pumping Stages

In the second stage, when the clock signal CLK is low and the clock signal CLKB is high during the time interval T1, V_{15} and the voltage difference (V_{26}) between node 2 and node 6 are $-$VDD and VDD, respectively. Therefore, transistors MP5 and MN6 are turned on to transfer the charges from node 5 to node 6, but transistors MP1 and MN2 are turned off to cut off the path from node 2 back to node 1. Similarly, V_{15} and V_{26} are VDD and $-$VDD during the time interval T2, respectively. Transistors MP5 and MN6 are turned off in order to cut off the path from node 6 back to node 5, but transistors MP1 and MN2 are turned on to transfer the charges from node 1 to node 2. The operation of the third pumping stage is similar to that of the second pumping stage.

C. Output Stage

As shown in Fig. 3(a), the output nodes of braches A and B are connected together. When the clock signal CLK is low and the clock signal CLKB is high during the time interval T1, the voltage difference (V_{48}) between node 4 and node 8 is VDD. Therefore, transistor MP4 is turned on to transfer the charges from node 4 to the output node, but transistor MP8 is turned off to cut off the path from the output node back to node 8. On the other hand, V_{48} is $-$VDD during the time interval T2. Hence, the transistor MP4 is turned off and the current path from the output node back to node 4 is cut off. In addition, the transistor MP8 is turned on to transfer the charges from node 8 to the output node.

As shown in Fig. 3(b), the gate-source voltage (V_{gs}) and gate-drain voltage (V_{gd}) of all MOSFETs in the new proposed charge pump circuit do not exceed VDD. Thus, there is no high-voltage overstress on the gate oxide of the devices in the new proposed charge pump circuit.

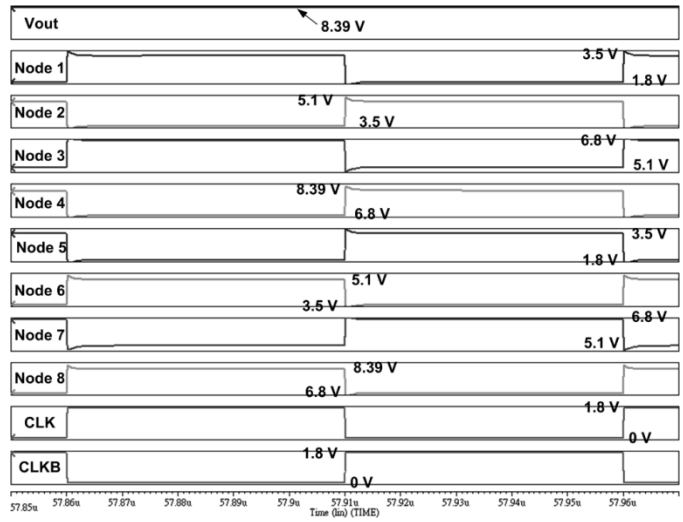


Fig. 4. Simulated waveforms on CLK, CLKB, nodes 1–8, and V_{out} in the new proposed four-stage charge pump circuit.

III. Verifications and Discussions

A. Simulations and Comparisons

A 0.18-μm 1.8-V CMOS device model is used to verify the design of the new proposed charge pump circuit in HSPICE simulation. Fig. 4 shows the simulated voltage waveforms of the new proposed four-stage charge pump circuit with each pumping pumping capacitor of 1 pF and 5-μA output current. The expected waveforms shown in Fig. 3(b) are similar to the simulated waveforms shown in Fig. 4. Ideally, the output voltage of the new proposed four-stage charge pump circuit with 1.8-V power supply voltage $(\mathrm{VDD} = 1.8\ \mathrm{V})$ should be as high as 9 V $(1.8 \times 5 = 9)$. However, due to the parasitic capacitance at each pumping node and the loading of the output current, the simulated output voltage of the new proposed charge pump circuit is around 8.39 V.

Fig. 5 shows the simulated output voltages of the proposed charge pump circuit under different output currents and power supply voltages (VDD). When the output current is increased, the output voltages of the proposed charge pump circuit under different power supply voltages (VDD) are decreased. If the new proposed charge pump circuit only drives the capacitive load, the output voltages of the proposed charge pump circuit under different power supply voltages (VDD) are close to $5 \times$ VDD. If the supply voltage is too low and the output current is too

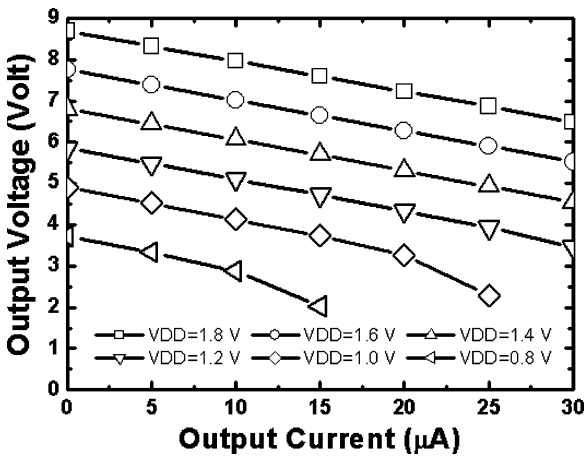


Fig. 5. Simulated output voltages of the new proposed four-stage charge pump circuit under different output currents and power supply voltages (VDD).

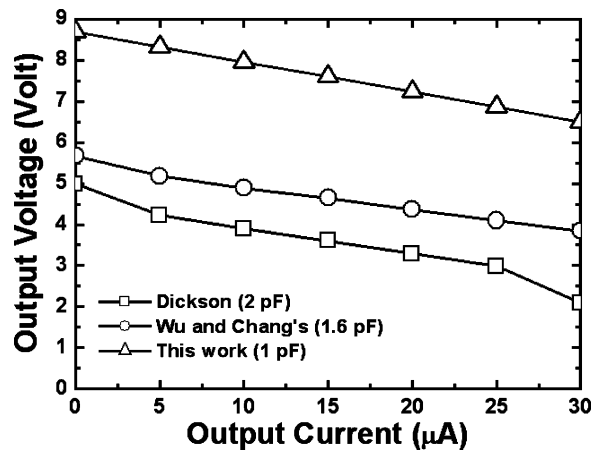


Fig. 6. Simulated output voltages of the Dickson, Wu and Chang, and the proposed charge pump circuits with four stages under different output currents with 1.8-V power supply (VDD = 1.8 V).

high, the proposed charge pump circuit cannot pump the output voltage high.

The simulated output voltages of the Dickson charge pump circuit [7], Wu and Chang's charge pump circuit [18], and the new proposed charge pump circuit with different output currents are compared in Fig. 6. Actually, the pumping capacitors of a charge pump circuit take a great part in silicon area. For fair comparison, the total pumping capacitors of these charge pump circuits must be equaled. Therefore, the pumping capacitors in the proposed charge pump circuit, in Wu and Chang's charge pump circuit, and in the Dickson charge pump circuit are set to 1 pF, 1.6 pF ($1 \times 8/5 = 1.6$), and 2 pF ($1 \times 8/4 = 2$), respectively. As shown in Fig. 6, the output voltages of the proposed charge pump circuit with different output currents are much higher than those of other charge pump circuits. Especially, with the higher output current of 30 μA, the proposed charge pump circuit still has the better pumping performance than others. Since the proposed charge pump circuit has two pumping branches pushing the charges to the output node alternately, the degradation of the output voltage is smaller while the output current increases. In addition, the MOSFET switches in the new proposed charge pump circuit are fully turned on to transfer the charges, but all MOSFET switches in the Dickson charge pump circuit and the output stage of Wu and Chang's charge pump circuit are diode-connected transistors, which have the threshold voltage drop problem. Thus, the proposed charge pump circuit has better pumping performance, as shown in Fig. 6.

Fig. 7 compares the simulated output voltages of the Dickson, Wu and Chang, and the new proposed charge pump circuits under different power supply voltages (VDD) without output current loading. As shown in Fig. 7, the output voltages of these three charge pump circuits are degraded when the power supply voltage is decreased. However, the new proposed charge pump circuit still has higher output voltages under the lower power supply voltage because the proposed charge pump circuit has better pumping efficiency. Thus, the proposed charge pump circuit is more suitable in low-voltage processes than the prior designs.

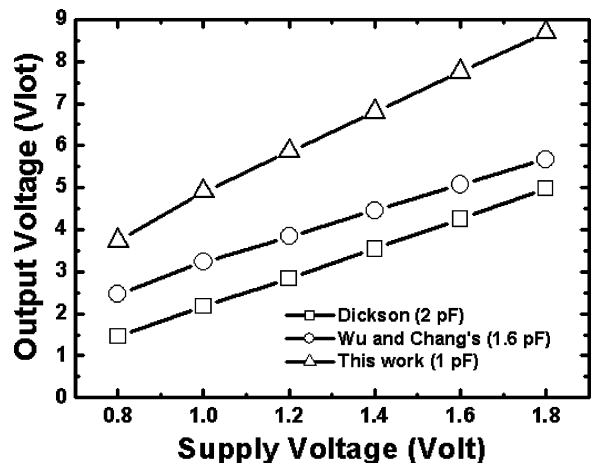


Fig. 7. Simulated output voltages of the Dickson, Wu and Chang, and the proposed charge pump circuits with four stages under different supply voltages (VDD) without output current loading.

Branches A and B in the new proposed charge pump circuit can pump the output voltage alternately, but Wu and Chang's charge pump circuit and the Dickson charge pump circuit only pump the charges to the output node per clock cycle. The simulated output waveforms of these charge pump circuits with 20-μA output current are shown in Fig. 8, where ΔV is the amplitude of the output voltage ripple. As shown in Fig. 8, the output voltage ripple of the proposed charge pump circuit (0.166%) is much smaller than those of Wu and Chang's charge pump circuit (0.457%) and the Dickson charge pump circuit (0.762%). Therefore, the output voltage of the new proposed charge pump circuit is more stable than those of the other charge pump circuits. If the output voltage ripple is still large, a low-pass filter should be connected to the output node of the charge pump circuit to filter the voltage ripple [23].

B. Silicon Verifications

In this work, two test chips have been fabricated in a 0.35-μm 3.3-V CMOS process to verify the proposed charge pump circuit. Fig. 9 shows the simulated output voltages of proposed charge pump with each pumping capacitor of 2 pF, the Dickson

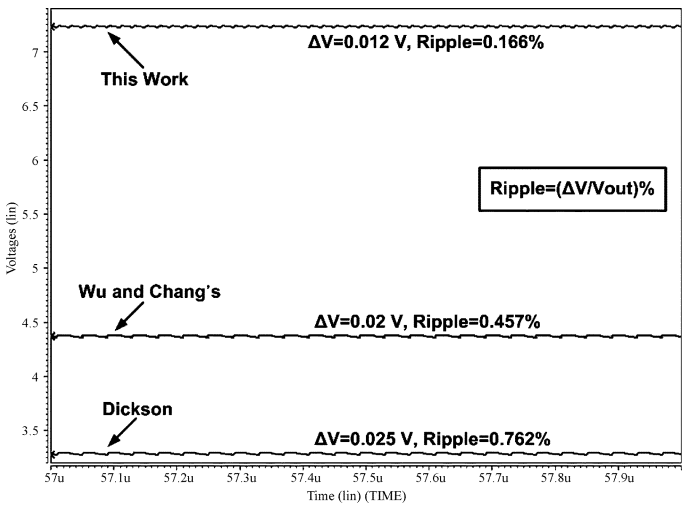


Fig. 8. Simulated output waveforms of the Dickson, Wu and Chang, and the proposed charge pump circuits of four stages with 20-μA output current and 1.8-V power supply (VDD $=$ 1.8 V).

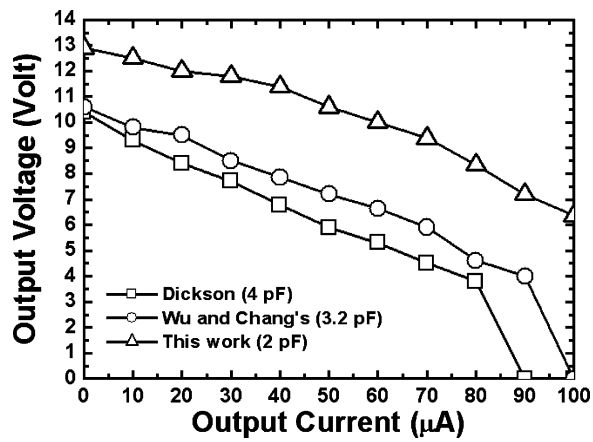


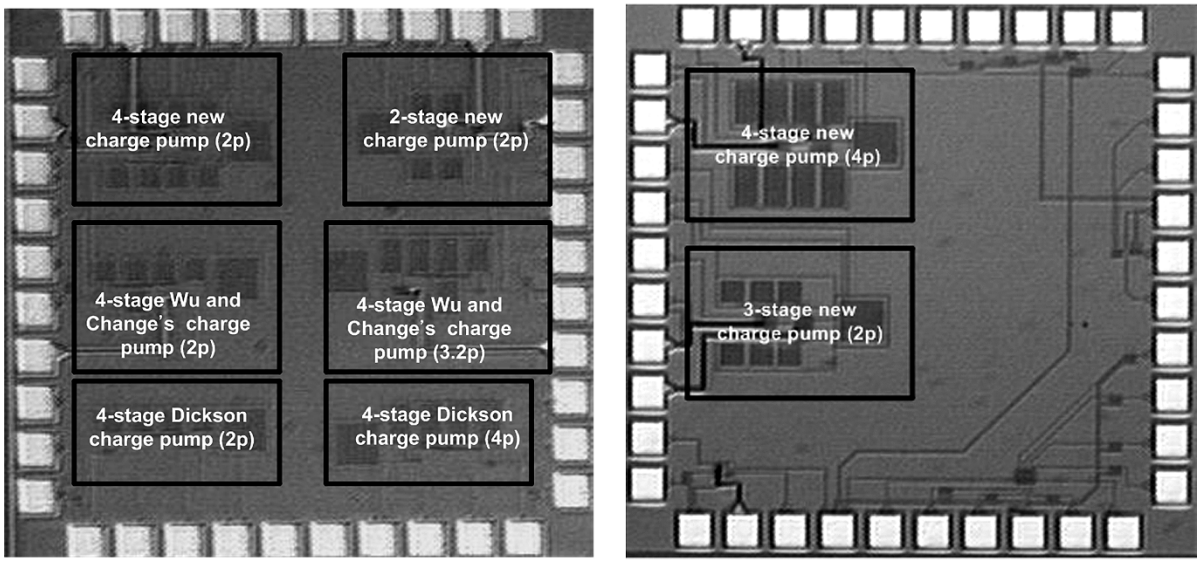
Fig. 9. Simulated output voltages of different four-stage charge pump circuits in the 0.35-μm 3.3-V CMOS process under different output currents with the power supply voltage (VDD) of 3.3 V.

charge pump circuit with each pumping capacitor of 4 pF, and Wu and Chang's charge pump circuit with each pumping capacitor of 3.2 pF in the 0.35-μm 3.3-V CMOS process. As shown in Fig. 9, the proposed charge pump circuit has better pumping performance. The photographs of these two test chips are shown in Fig. 10(a) and (b). These two test chips include the proposed four-stage charge pump circuit with each pumping capacitors of 2 pF, the proposed two-stage charge pump circuit with each pumping capacitor of 2 pF, Wu and Chang's four-stage charge pump circuit with each pumping capacitor of 2 pF, Wu and Chang's four-stage charge pump circuit with each pumping capacitor of 3.2 pF, the Dickson four-stage charge pump circuit with each pumping capacitor of 2 pF, the Dickson four-stage charge pump circuit with each pumping capacitor of 4 pF, the proposed four-stage charge pump circuit with each pumping capacitor of 4 pF, and the proposed three-stage charge pump circuit with each pumping capacitor of 2 pF. To drive capacitive load, the measured output voltage of the new proposed four-stage charge pump circuit with each pumping capacitor of 2 pF is around 8.8 V under 3.3-V power supply voltage (VDD $=$ 3.3 V). Fig. 11 shows the measured output voltages of the four-stage charge pump circuits with different output currents. The measured results in Fig. 11 is little lower than the simulated results in Fig. 9 because of the parasitic resistance and capacitance from the test chips, the bonding wires, and the packages. The parasitic resistance and capacitance may results in the overlapping clock signals, which will lower the pumping efficiency. However, similar to the simulation results, the proposed charge pump circuit has better pumping performance than others, as shown in Fig. 11. Besides, the output voltage ($\sim$9 V) of the proposed charge pump circuit is limited by the breakdown voltage of the parasitic drain-to-bulk pn-junction diode under the low output current. If the output voltage of the charge pump circuit is larger than the breakdown voltage of the pn-junction diode, the charges leak through this diode and the output voltage of the charge pump circuit is kept at the breakdown voltage. Fig. 12 compares the measured output voltages of the proposed two-stage, three-stage, and four-stage charge pump circuits with each pumping capacitor of 2 pF under 2-V power supply (VDD $=$ 2 V), respectively. Similarly, the measured output voltage of the proposed four-stage charge pump circuit in Fig. 12 is also limited by the breakdown voltage of the parasitic pn-junction diode at low output current.

C. Discussion

Gate-oxide reliability is a time-dependent issue [24], [25]. The time period during the voltage overstress on the gate oxide is accumulated to induce the oxide breakdown. Hence, the DC stress is more harmful to the gate oxide than the short AC stress (transient stress). The diode-connected MOSFET in the Dickson charge pump circuit is used to transfer charges from the present stage to the next stage. When the diode-connected MOSFET is turned off to prevent the charges flowing back to the previous stage, the voltage across the gate oxide of the diode-connected MOSFET is around $2 \times$ VDD $- V_t$, where V_t is the threshold voltage of the diode-connected MOSFET. The diode-connected MOSFET will suffer serious gate-oxide overstress, so the gate oxide of the diode-connected MOSFET may be damaged after operation. In Wu and Chang's charge pump circuit, not only these diode-connected MOSFETs but also the charge transfer switches (CTSs) and their control circuits will suffer serious high-voltage overstress on the gate oxide. In the proposed charge pump circuit, the gate-oxide reliability issue has been considered. The gate-to-source voltages ($V_{\rm gs}$) and gate-to-drain voltages ($V_{\rm gd}$) of devices in the proposed charge pump circuit do not exceed VDD whenever it is in the normal operation, start-up, or turn-off states. Therefore, the proposed charge pump circuit is better for applications in low-voltage CMOS processes.

As shown in Figs. 11 and 12, the output voltage of the proposed charge pump circuit will be limited by the breakdown voltages of the parasitic pn-junctions. As the CMOS process is scaled down, the breakdown voltages of the parasitic pn-junctions become lower. Thus, the output voltage limitation of the charge pump circuit will become more serious. In [26], the charge pump circuit is designed in the SOI process without the limitation of the breakdown voltages of the pn-junctions. However, the SOI process is more expensive than the bulk CMOS process. The charge pump circuit consisting of the



(a) (b)

Fig. 10. Photographs of charge pump circuits in (a) chip 1, and (b) chip 2, fabricated in the 0.35-μm 3.3-V CMOS process.

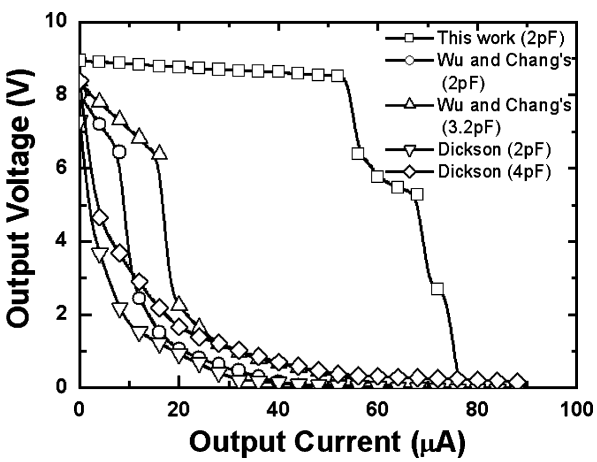


Fig. 11. Measured output voltages of different charge pump circuits with 3.3-V power supply (VDD = 3.3 V), where the stage number is 4.

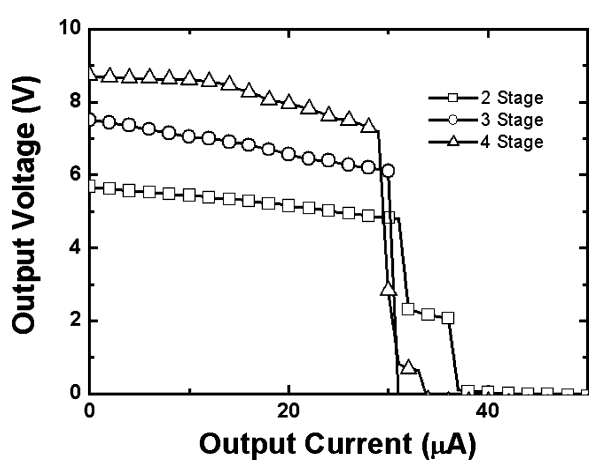


Fig. 12. Measured output voltages of the new proposed two-stage, three-stage, and four-stage charge pump circuits with 2-V power supply (VDD = 2 V) under different output currents.

polysilicon diodes, which is fully compatible to the standard bulk CMOS process, may be a good candidate to implement the charge pump circuit without the limitation of the breakdown voltages of the parasitic pn-junctions in the future [27].

IV. Conclusion

A new charge pump circuit realized with only low-voltage devices without suffering the gate-oxide reliability issue has been presented. Because the charge transfer switches of the new proposed charge pump circuit can be fully turned on and turned off, as well as the output stage does not have the threshold drop problem, its pumping efficiency is higher than that of the prior designs. The gate-drain and the gate-source voltages of all devices in the proposed charge pump circuit do not exceed VDD, so the proposed charge pump circuit does not suffer the gate-oxide reliability problem. Two test chips have been implemented in a 0.35-μm 3.3-V CMOS process. The experimental results have shown that the new proposed four-stage charge pump circuit with each pumping capacitor of 2 pF to drive the capacitive load is around 8.8 V under 3.3-V power supply (VDD = 3.3 V). With the higher pumping gain and no overstress across the gate oxide, the new proposed charge pump circuit is more suitable for applications in low-voltage CMOS integrated circuits to generate the specified high voltage.

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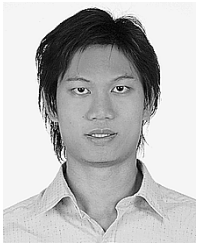

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