

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK hynix Inc.
Petitioner

v.

Advanced Memory Technologies, LLC
Patent Owner

IPR2025-01450
Patent No. 7,920,018

PETITION FOR *INTER PARTES* REVIEW

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EXHIBIT LIST

Ex.	Description
1001	U.S. Patent No. 7,920,018 (“’018 Patent”)
1002	File History for U.S. Patent No. 7,920,018
1003	Declaration of Dr. Carl Sechen
1004	<i>Curriculum vitae</i> of Dr. Carl Sechen
1005	U.S. Patent No. 7,382,177 (“Cordoba”)
1006	U.S. Patent No. 6,501,325 (“Meng”)
1007	U.S. Patent No. 6,914,791 (“Park”)
1008	<i>Advanced Memory Techs., LLC v. SK hynix Inc.</i> , No. 2:24-cv-01078-JRG-RSP (E.D. Tex. Apr. 2, 2025), Infringement Contentions Exhibit C (Patent Owner’s infringement claim chart for ’018 patent)
1009	G. Campardo et al., <i>VLSI-Design of Non-Volatile Memories</i> , Springer (2005)
1010	M.-D. Ker et al., “Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 41, No. 5, pp. 1100-07 (May 2006)
1011	J. F. Dickson, “On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-11, No. 3, pp. 374-78 (June 1976)

LIST OF CHALLENGED CLAIMS

Claim	Limitation
1[pre]	A booster circuit comprising:
1[a]	a first boosting cell row including N stages ($N \geq 1$) of boosting cells; a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and
1[b]	at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row, wherein:
1[c]	each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,
1[d]	the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and
1[e]	the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.
2[pre]	The booster circuit of claim 1, wherein:
2[a]	the first boosting cell row includes at least one backflow preventing circuit; the second boosting cell row includes at least one backflow preventing circuit; and

Claim	Limitation
2[b]	the well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.
3	The booster circuit of claim 1, wherein the well bias potential is the higher potential out of the input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row.
4	The booster circuit of claim 1, wherein the well bias potential is the lower potential out of the input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row.
5	The booster circuit of claim 1, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.
6	The booster circuit of claim 1, wherein the second well region and the first well region are connected to each other so that the second well region and the first well region have the same potential.
7[pre]	The booster circuit of claim 1, wherein:

Claim	Limitation
7[a]	the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and
7[b]	the at least one analog comparison circuit is provided for each boosting cell stage in the first boosting cell row and the second boosting cell row.
8[pre]	The booster circuit of claim 1, wherein:
8[a]	the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and
8[b]	the at least one analog comparison circuit is provided for arbitrary number of boosting cell stages in the first boosting cell row and the second boosting cell row.
9	The booster circuit of claim 1, wherein a diode element is provided between the first terminal and the first well region of the boosting cell.
10[pre]	The booster circuit of claim 1, wherein:
10[a]	the at least one switching element of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

Claim	Limitation
10[b]	the at least one switching element of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.
12[pre]	A booster circuit comprising:
12[a]	a first boosting cell row including N stages ($N \geq 2$) of boosting cells; and a second boosting cell row including M stages ($M \geq 2$) of the boosting cells, wherein:
12[b]	each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,
12[c]	the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal,
12[d]	a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row and an input potential of the boosting cells of the second boosting cell row, and
12[e]	an input potential of each of the boosting cells of the first boosting cell row is different from an input potential of each of the boosting cells of the second boosting cell row.

I. INTRODUCTION

The '018 patent is directed to a well-known apparatus of a charge pump comprising two rows of boosting cells coupled to one or more analog comparison circuits. The claims of the '018 patent recite the basic structure of a two-row charge pump comprising multiple well regions, and the use of analog comparison circuits to output a well bias potential to the well regions of the charge pump.

The '018 patent's purported improvement over the prior art was the design of a booster circuit "in which the potential of an N well of each boosting cell is fixed to the input or output potential of the boosting cell stage" through the use of analog comparison circuits. EX1001, 2:45-48. Such analog comparison circuits would apply an appropriate level of well biasing to the well regions of the charge pump. The stated goal of this design was to suppress current consumption and minimize the layout area of the circuit, as well as the suppression of substrate biasing (*i.e.*, body effect). EX1001, 2:40-44.

But the purported solution had been known for years before the priority date of the '018 patent, including as disclosed in the Petition's two primary references from Micron Technology ("Cordoba") and Cypress Semiconductor ("Meng"). These early- to mid-2000s references disclose two-row charge pumps using analog comparison circuits to provide appropriate levels of well biasing to the well regions on which the circuits are built. Moreover, these references are directed to

minimizing the same issues facing charge pumps, namely, the body effect and forward biasing of well regions. For these reasons, the challenged claims of the '018 patent are unpatentable.

II. IDENTIFICATION OF GROUNDS

Petitioner requests cancellation of claims 1-10 and 12 on the following grounds:

Ground	Reference(s)	Basis	Claims
1	Cordoba	§102	1, 3, 4, 7
2	Meng	§102	1-3, 9, 10, 12
3	Meng, Park	§103	1-10, 12

III. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) as of January 17, 2007, would have had a master’s degree in electrical engineering, computer engineering, physics, or a related field, with at least two years of experience in the field of integrated circuits and/or memory devices. EX1003, ¶27. Less work experience may be compensated by a higher level of education or vice versa. *Id.* Petitioner’s expert, Dr. Carl Sechen, exceeded this definition by the priority date. *Id.*, ¶¶5-16, 27.

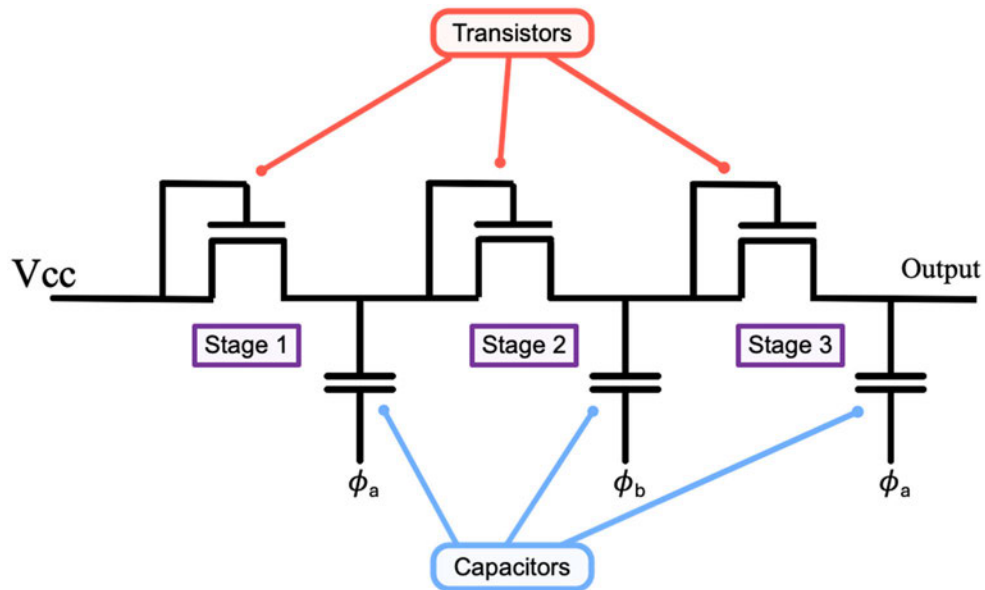
IV. TECHNOLOGY OVERVIEW

A. Booster Circuit

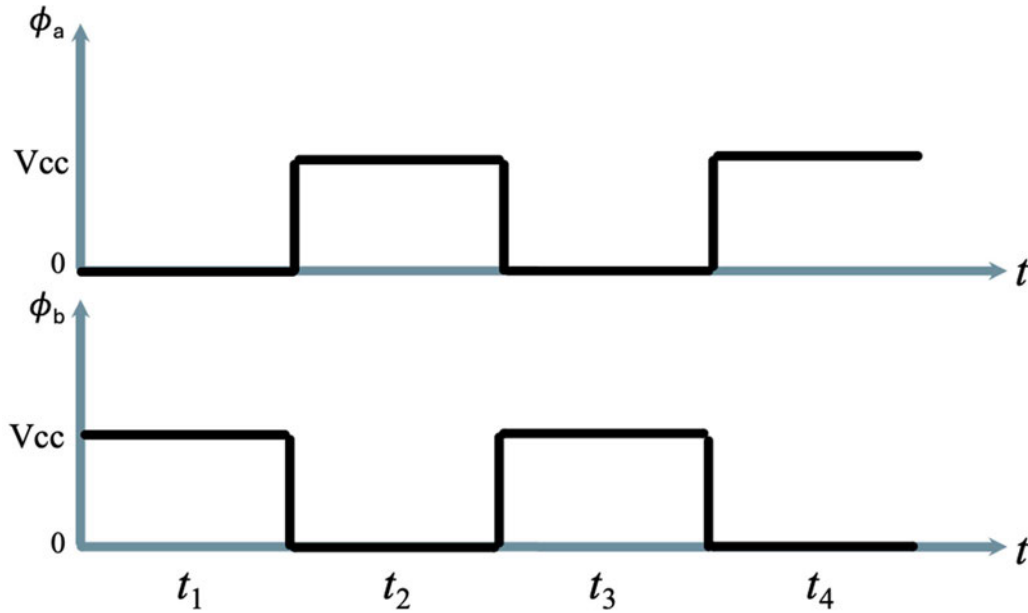
Booster circuits (*i.e.*, charge pumps) are circuits that take a supply voltage and increase, or “boost,” the voltage to output a voltage that is higher than the supply

voltage. EX1003, ¶34. Long before the critical date of the '018 patent, a booster circuit was a widely used in memory devices such as a flash memory because the higher voltage output of a booster circuit was used for writing and erasing programmable elements. *Id.*

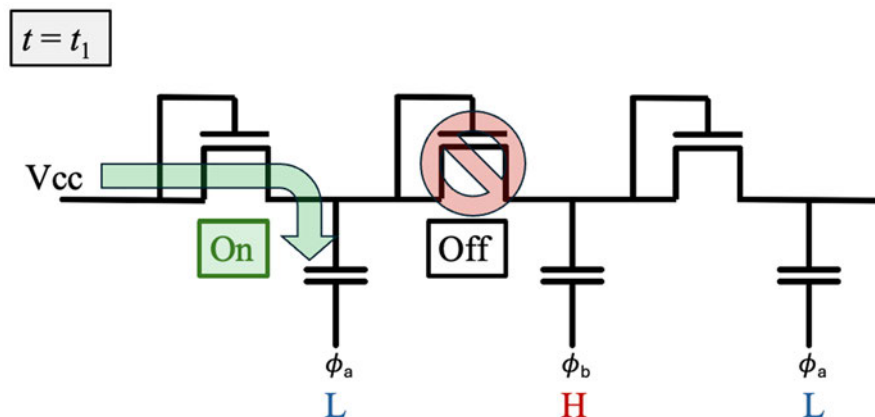
A conventional, single row charge pump was first introduced in 1976 by John F. Dickson. EX1011, Fig. 2, 375; EX1003, ¶35. The so-called Dickson charge pump circuit is shown in the schematic below. EX1011, Fig. 2. The charge pump shown below is a three-stage charge pump, where each stage comprises a diode-connected transistor (*e.g.*, an NMOS transistor) and a capacitor that is switched. For an NMOS transistor, the drain terminal is at a voltage that is higher than (or equal) to the source terminal voltage. The diode-connected transistors in the figure permit conduction from left to right if the left (drain) terminal of a transistor is at a higher voltage than the right (source) terminal. EX1011, 375. Such transistors, however, prevent current conduction from right to left even if the right (drain) terminal is at a higher voltage than the left (source) terminal since the gate-to-source voltage would be exactly zero due to the connection between gate and source. *Id.*



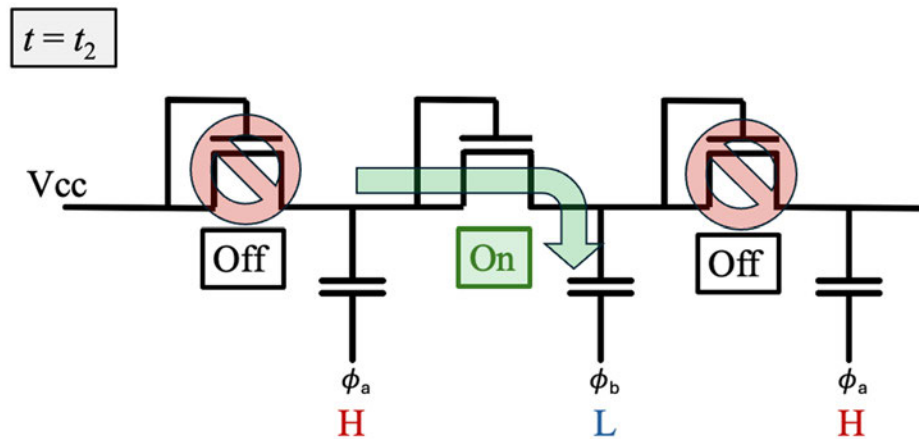
The capacitors are driven by two clock signals, ϕ_a and ϕ_b , each of which is characterized as a periodic square-wave where the maximum is the supply voltage (V_{cc}) and the minimum is set to ground (0V). As illustrated below, ϕ_a and ϕ_b are identical except that they are out of phase with one another (*e.g.*, ϕ_b is at a minimum when ϕ_a is at a maximum). At time t_1 , ϕ_a is at a minimum voltage (*i.e.*, “low”) and ϕ_b is at a maximum voltage (*i.e.*, “high”). EX1011, Fig. 3, 375; EX1003, ¶36.



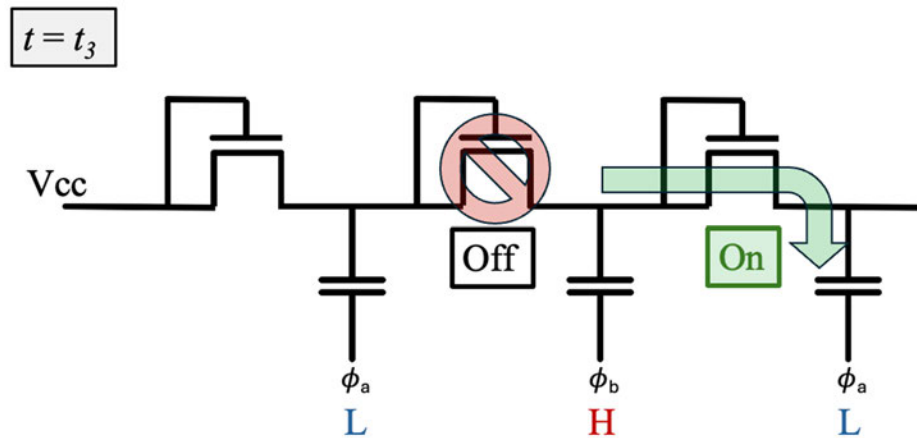
When ϕ_a is low, the first stage transistor is turned on since the gate (and drain) voltage (V_{cc}) is greater than the voltage at the source (right terminal) of the first stage transistor due to ϕ_a pulling low. Meanwhile, the second stage transistor is turned off since its gate-to-source voltage is zero due to ϕ_a pulling low and ϕ_b pulling high (making the left terminal of the second stage transistor the source). This allows the first stage capacitor to charge to a voltage of $V_{cc} - V_t$, where V_t is the threshold voltage drop across the transistor. EX1003, ¶37.



At t_2 , ϕ_a goes high while ϕ_b goes low, resulting in the first stage transistor and third stage transistor turning off and the second stage transistor turning on. The signal ϕ_a going high raises the voltage of the bottom terminal of the first stage capacitor by V_{cc} , in turn causing the voltage at the top terminal of the first stage capacitor to increase by V_{cc} (due to the nature of a capacitor, the voltage across it does not change instantaneously). As a result, the top terminal of the first stage capacitor is thus $2V_{cc}-V_t$, which is subsequently transmitted across the second stage transistor to charge the second stage capacitor to a voltage of $2V_{cc}-2V_t$ (accounting for the threshold voltage drop across the second stage transistor). EX1003, ¶38.



At t_3 , ϕ_b goes high while ϕ_a goes low, resulting in the second stage transistor turning off and the third stage transistor turning on. As a result, the voltage at the top of the second stage capacitor increases by V_{cc} , thus increasing to $3V_{cc}-2V_t$. This voltage is subsequently transmitted across the third stage transistor to charge the third stage capacitor to a voltage of $3V_{cc}-3V_t$. EX1003, ¶39.



As a result of the multiple booster stages and the alternating clock signals providing periodic voltage boosts, a booster circuit is capable of taking an input voltage (V_{cc}) and amplifying it to a higher output voltage ($3V_{cc}-3V_t$). EX1011, Fig. 3, 375-76; EX1003, ¶40.

B. Deep N-well Layer

Before the priority date of the '018 patent, a structure employing multiple layers of different conductivity (*i.e.*, well regions) was commonly used in integrated circuits. EX1009, 32-33; EX1003, ¶41. A cross-sectional illustration of a multiple-well structure for NMOS transistors is shown below, and comprises two well regions of different conductivity types: an N-type layer (*i.e.*, a deep N-well) fabricated on a P-type substrate, and a P-type layer (*i.e.*, a P-well) fabricated in the deep N-well. EX1007, Fig. 9; *see also* EX1009, Fig. 15.17.

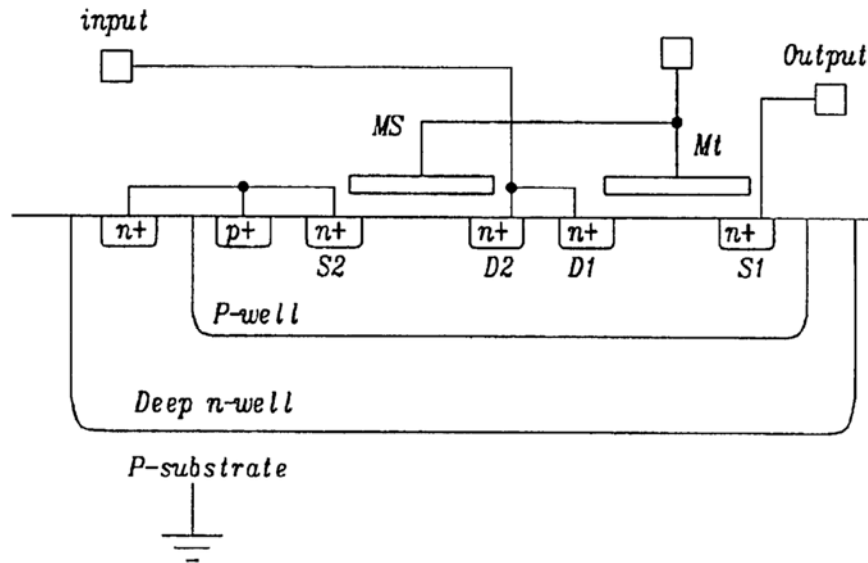


FIG. 9

It was well known that the use of multiple wells enabled a reduction of the body effect of a transistor (*i.e.*, reduction of the threshold voltage associated with a transistor by reducing the reverse bias of the body-source PN-junction), since the body of one or more transistors can have their body voltages individually tuned. EX1009, 100, 329, 371-73, 383; EX1003, ¶42. This reduction in body effect makes it easier to turn on a transistor and reduces the supply voltages necessary for operating a booster circuit. EX1009, 41; EX1003, ¶42. It was also well known that the use of multiple well regions, specifically a deep N-well, improved the isolation of switching elements from the bulk substrate and helped suppress occurrences of latch-up. EX1009, 142; EX1003, ¶42.

C. Two-Row Structure of a Booster Circuit

It was conventional, before the priority date of the '018 patent, to construct a charge pump circuit using two rows of boosting cells. EX1010, Fig. 3; EX1009, Figs. 15.19-15.21; EX1003, ¶43. For example, in 2001, Meng taught a two-row booster circuit where each row serves as a separate booster circuit capable of amplifying an input voltage. EX1006, 3:31-62, 4:10-50, Figs. 5, 7; *see also* EX1005, Figs. 2-4, 8:15-40; EX1010, Figs. 3(a)-(b), 1103; EX1009, 15.19-15.21, 376-79. In a two-row structure, for any given stage in a boosting operation, the boosting cells of the two rows are connected to complementary clock signals (*e.g.*, for a given boosting stage, the boosting cell of the first row will be connected to ϕ_a while the boosting cell of the second row will be connected to ϕ_b). EX1006, Fig. 7, 3:17-30; *see also* EX1010, Fig. 3(a), 1103; EX1009, Figs. 15.19-15.20.

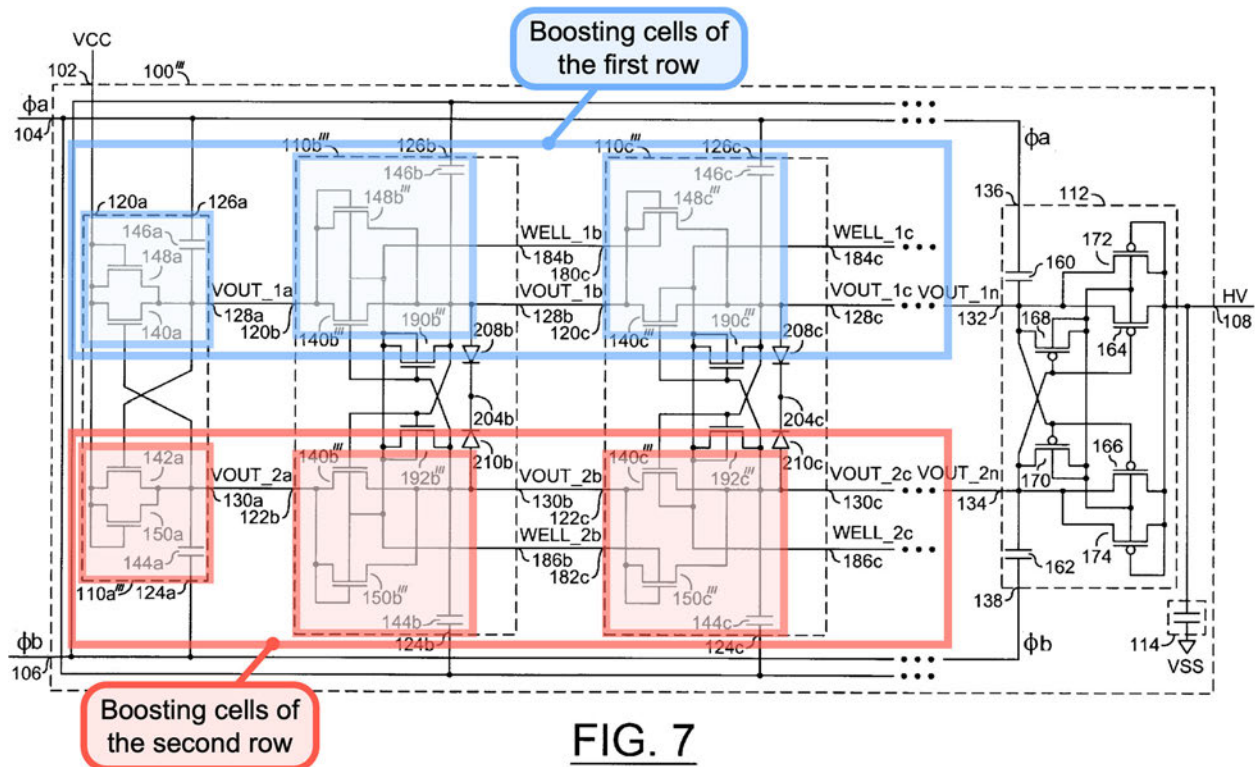


FIG. 7

A two-row structure was known to enable a variety of advantages in the structure and function of booster circuits. EX1003, ¶44. For example, two-row structures can exploit the complementary clock signals ϕ_a and ϕ_b that are applied to a given boosting stage by using those complementary clock signals to control the switching elements contained in that boosting stage. EX1010, Fig. 3(a), 1102-03; EX1003, ¶44. This concept is further demonstrated in Figure 7 of Meng, shown below. EX1006, Fig. 7. The complementary clock signals applied to a given stage are at a **high voltage** for one boosting cell (**first row**) and a **low voltage** for the other boosting cell (**second row**). EX1006, Fig. 7, 3:21-27, 5:26-48. The complementary clock signals affect the voltage at nodes 128*i* and 130*i*, which in turn control (*i.e.*, activate) switches 192"*i* and 190"*i*, respectively. EX1006, 9:9-32; EX1003, ¶44.

For example, a high voltage present at node 128 i will turn on 192 $'''i$ while the corresponding low voltage present at node 130 i will turn off 190 $'''i$. EX1003, ¶44.

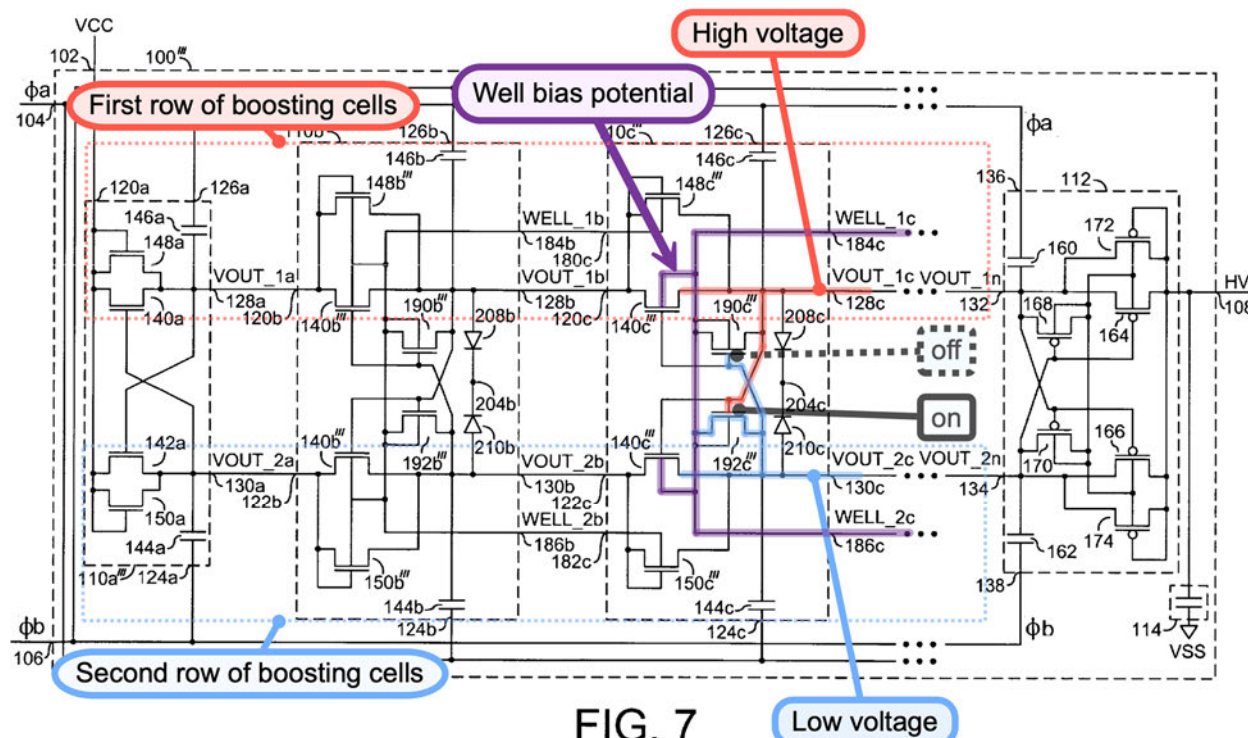


FIG. 7

Two-row structures exploit the complementary clocks signals to improve the efficiency of a booster circuit. EX1010, Fig. 7, 1104; EX1003, ¶45. With a single-row structure, the output of a boosting row is boosted or driven for half of a clock cycle, and that output voltage decays (*i.e.*, leaks away) over the subsequent half cycle. EX1010, 1104. By contrast, for a two-row structure having the final outputs of the two rows tied together, the final output common to both rows is boosted by one of the two rows while the other row is not boosting (and vice versa for the next half of the clock cycle). EX1010, Figs. 4, 8, 1104. Thus the final output of a two-row structure is being boosted over both halves of the clock cycle, helping prevent

decay of the output voltage that would otherwise occur for half the clock cycle in a single-row structure. EX1003, ¶45; *see also* EX1005, Fig. 6, 5:27-36, 8:41-67; EX1010, Figs. 3(b), 4, 8, 1103-04. Moreover, the final output of a two-row structure is boosted twice as often over the same clock period, thereby enhancing the overall efficiency of the booster circuit. EX1003, ¶45; EX1010, Fig. 8, 1104-06.

Another benefit of the two-row structure is the reduction in the body effect (*i.e.*, the increase in the threshold voltage caused by an increase in the reverse bias from transistor source to body). A two-row structure minimizes the body effect by bootstrapping the well bias potential across the boosting stages. EX1010, 1102-03; EX1009, Fig. 15.20, 378. Both the low-side and high-side voltages present on the boosting cell rows increase with each successive boosting cell stage. EX1010, Fig. 3(b). By adjusting the well bias potential to reflect the increased voltages of both rows (*e.g.*, setting the well bias potential to be the low-side voltage present at each boosting cell stage instead of leaving the body at a fixed voltage such as ground), one obtains two well-known benefits of two-row structures: prevention of forward biasing at drain-source junctions, and a reduction of the body effect at each boosting cell stage. EX1010, 1102-03; EX1009, 378; EX1003, ¶46.

D. Comparison Circuits

A comparison circuit is a circuit that receives two inputs and produces an output in response to a comparison of those two inputs, *e.g.*, an output corresponding

to which input is higher. Example comparison circuits include a pair of cross-coupled transistors, or a pair of diodes with their outputs tied together. EX1006, Fig. 7, 8:16-22; EX1009, Fig. 15.20, 378; EX1003, ¶47. In both of these cases, the circuits take two inputs and produce an output depending on which input is higher or lower. EX1006, Fig. 8. Such comparison circuits can be utilized to apply a consistent and appropriate well bias potential to the well region(s) underlying a booster circuit. *Id.*; EX1003, ¶47. An example of a comparison circuit being used to select and output a well bias potential based on a comparison of two voltage inputs was presented in §IV.C above, where elements 190*"i* and 192*"i* (*i.e.*, a pair of cross-coupled transistors) together form a comparison circuit. §IV.C, *supra*; EX1006, Fig. 7; EX1003, ¶47.

V. THE '018 PATENT

A. Overview

U.S. Pat. No. 7,920,018 is directed to a two-row booster circuit comprising at least one boosting cell stage and an analog comparison circuit that outputs a well bias potential that is applied to a deep N-well. EX1001, Abstract. Each boosting cell utilizes a switching element and a capacitor to transmit and store a charge as part of the voltage amplification process. EX1001, Fig. 1, 1:31-51, 7:55-62. The boosting cells further utilize a deep N-well for the switching elements. EX1001, 1:40-51, Fig. 1. An analog comparison circuit is used to compare the output voltages

FIG. 1



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The Examiner's initial communication allowed claims 1-11, but relied on U.S. Patent No. 6,121,821 ("Miki") in concluding that claim 12 was anticipated. *Id.*, 149. Miki discloses a two-row charge pump comprising switching elements and multiple well regions. The Examiner relied upon Miki's disclosure of a switching element whose application of a well bias potential to a first well region was controlled according to a clock signal input. *Id.*

In response, Applicant amended claim 12 to add a limitation requiring the "input potential of each of the boosting cells of the first boosting cell row [to be] different from an input potential of each of the boosting cells of the second boosting cell row." *Id.*, 160-61. Applicant further noted that the potential of the first well region, according to Miki, was "controlled according to one type of input potential and not two different types of input potentials." *Id.*, 161. Applicant's argument was supported by the amendment made to claim 12.

Following this amendment and argument, the Examiner issued a Notice of Allowance without any further comment. *Id.*, 170. The Examiner did not take into consideration any of the references discussed in this Petition.

VI. CLAIM CONSTRUCTION

Petitioner has applied the plain and ordinary meaning understood by a POSITA at the time of the alleged invention, in the context of the '018 patent and its prosecution history. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

VII. GROUND 1: CORDOBA ANTICIPATES CLAIMS 1, 3, 4, AND 7**A. Overview of Cordoba**

U.S. Patent No. 7,382,177 (“Cordoba”) was published on April 27, 2006, and therefore qualifies as prior art under pre-AIA 35 U.S.C. §102(a) and (e). Cordoba teaches a two-row booster circuit comprising a single boosting cell stage. EX1005, Fig. 3, 8:15-32; EX1003, ¶58. Cordoba further teaches a comparison circuit designed to compare the input voltages of the two rows and to output one of those two voltages (either the higher or the lower one) as a well bias potential. *Id.*, 8:44-54, 8:58-67. The booster circuit described by Cordoba has a P-well in a deep N-well with the deep N-well positioned on top of a P-type substrate. *Id.*, Fig. 15, 7:9-17. The well bias potential outputted by the analog comparison circuit is applied to the deep N-well in order to prevent the occurrence of forward biasing at the junctions of the well regions. *Id.*, 8:44-54, 8:58-67, Fig. 15; EX1003, ¶58.

B. Claim 1**1. 1[pre]: A booster circuit comprising:**

To the extent this preamble is limiting, Cordoba discloses a booster circuit. EX1005, Fig. 3; *id.*, 1:6-8 (“The present invention relates generally to a voltage charge pump and more particularly to a voltage charge pump for use in integrated circuits.”). A “charge pump circuit,” which receives a supply voltage and outputs a

voltage that has been charged to a level higher than the supply voltage, is a “booster circuit.” §IV.A, *supra*; EX1003, ¶59.

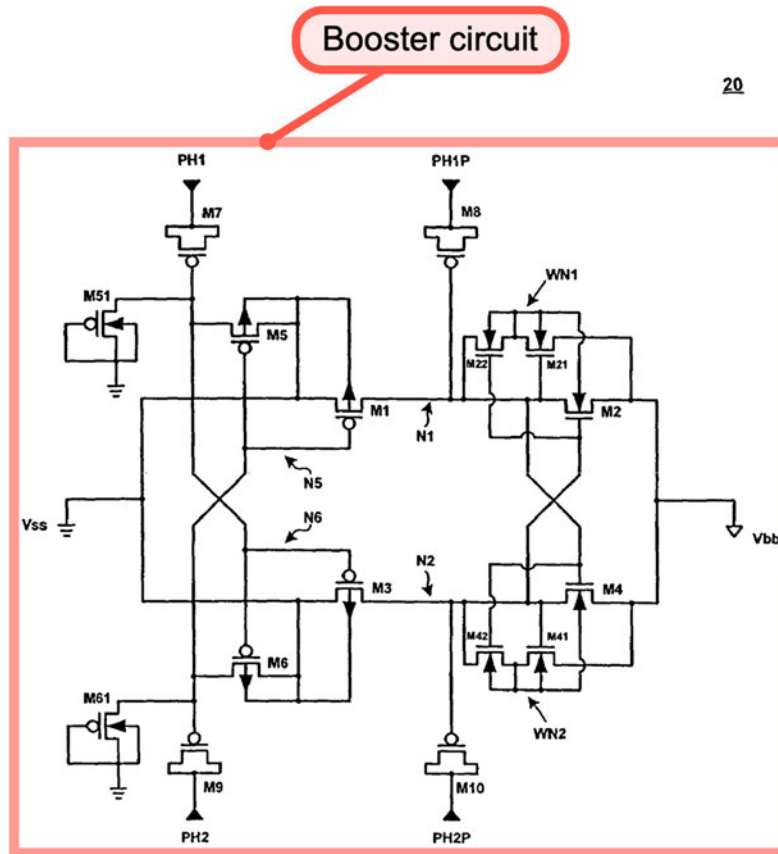


FIG. 3

2. 1[a]: a first boosting cell row including N stages ($N \geq 1$) of boosting cells; a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and

Cordoba discloses 1[a]. Cordoba discloses a “Vbb pump [*i.e.*, booster circuit] 15 [that] is comprised of first and second stages.” EX1005, 5:15-16. An annotated version of Cordoba’s Figure 3 shown below identifies the first stage (*i.e.*, *first boosting cell row*), which “is comprised of transistors M51, M5, M7, M1, M8, and

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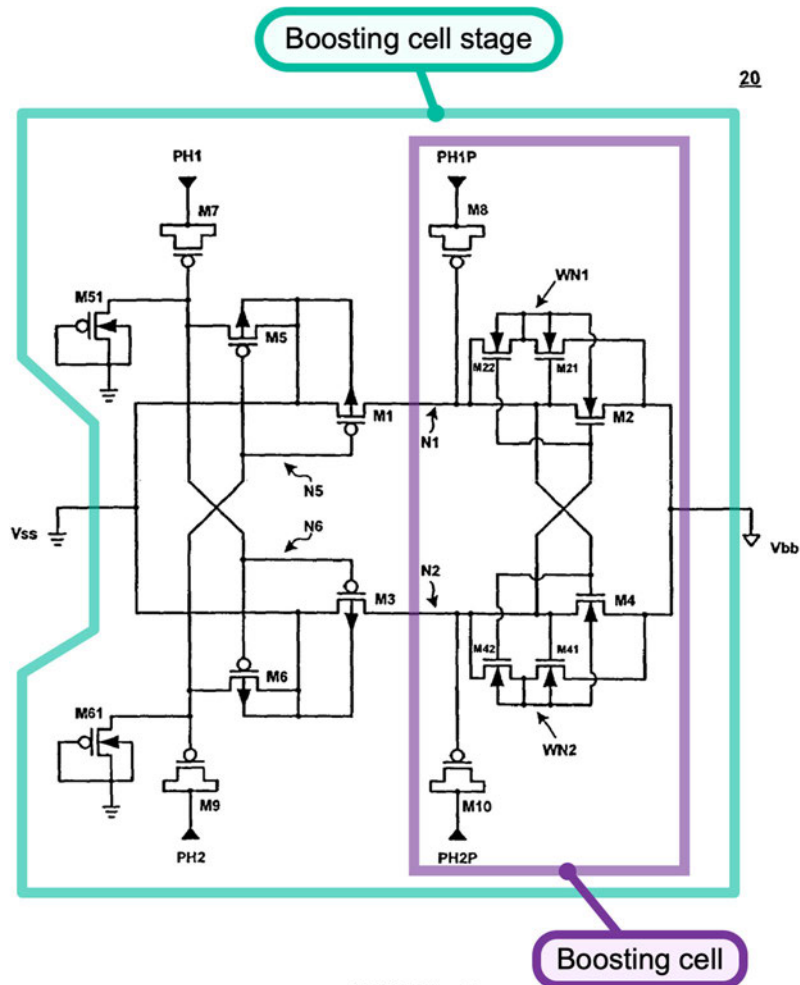
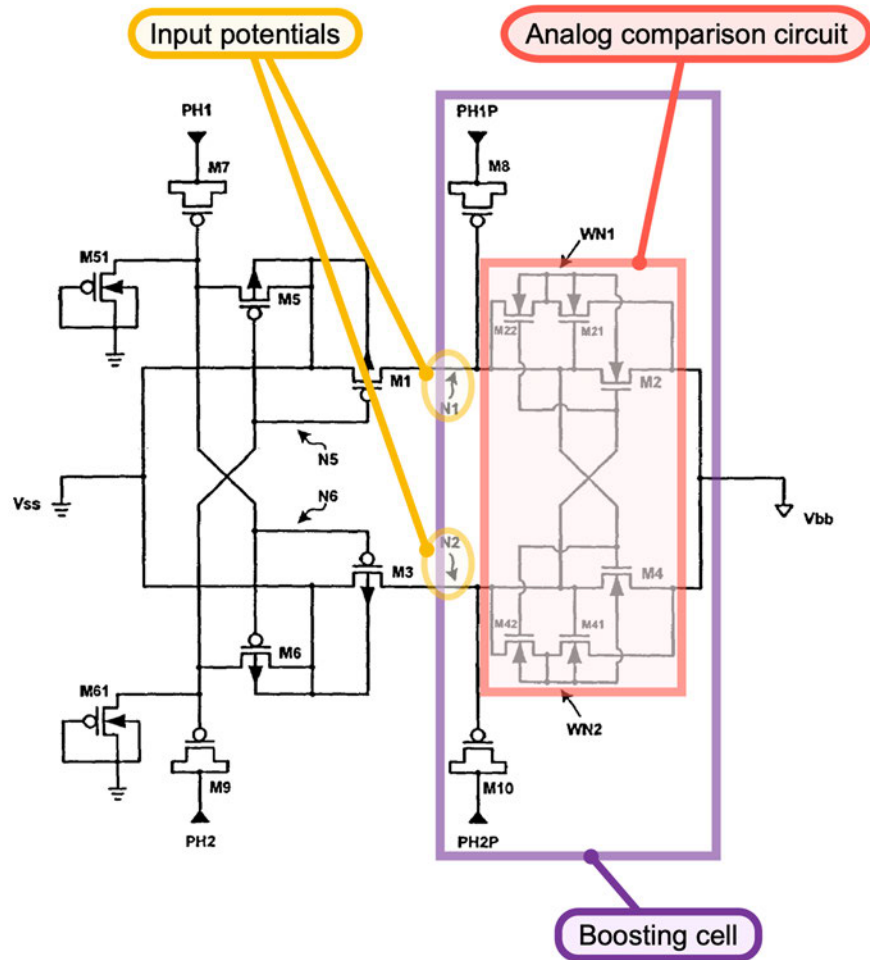


FIG. 3

3. 1[b]: at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row, wherein:

Cordoba discloses 1[b]. Cordoba discloses an analog comparison circuit comprising transistors M2, M21, and M22 in the first row and transistors M4, M41, and M42 in the second row, as shown below in Figure 3. EX1005, Fig. 3; EX1003, ¶62.

**FIG. 3**

Cordoba teaches that “when N1 is more negative than Vbb ... [then] M22 is conductive and N1 is connected to node WN1.” EX1005, 8:44-47. Node N1 represents an *input potential* of the boosting cell, as shown in Figure 3 above. EX1005, Fig. 3; EX1003, ¶63. When the input potential of the boosting cell (*i.e.*, node N1) is connected to node WN1 (*i.e.*, when node N2 is high), the input potential becomes a well bias potential applied to “the wells of transistors M2, M21, and M22 [which] are switched to node WN1” as shown below in the annotated version of Figure 3. EX1005, 8:30-31, Fig. 3. At the same time, the low voltage at N1 is passed

[illegible]

Similarly, with respect to the second row, Cordoba teaches that “when N2 is more negative than Vbb ... [then] M42 is on and N2 is connected to node WN2.” EX1005, 8:58-60. The potential at N2 (*i.e.*, an input potential to the boosting cell) is applied as a well bias potential to “the wells of transistors M4, M41, and M42 [which] are switched to node WN2.” EX1005, 8:31:32. The operation of applying

the input potential at N2 as a well bias potential to transistors M4, M41, and M42 is illustrated below in the annotated version of Figure 3. EX1005, Fig. 3; EX1003, ¶64. At the same time, the low voltage at N2 is passed through M4, and since M21 is switched on (due to N1 being high), the wells of transistors M2, M21, and M22—which are connected to WN1—are switched to the same low voltage of N2 that is passed through M4. EX1003, ¶64.

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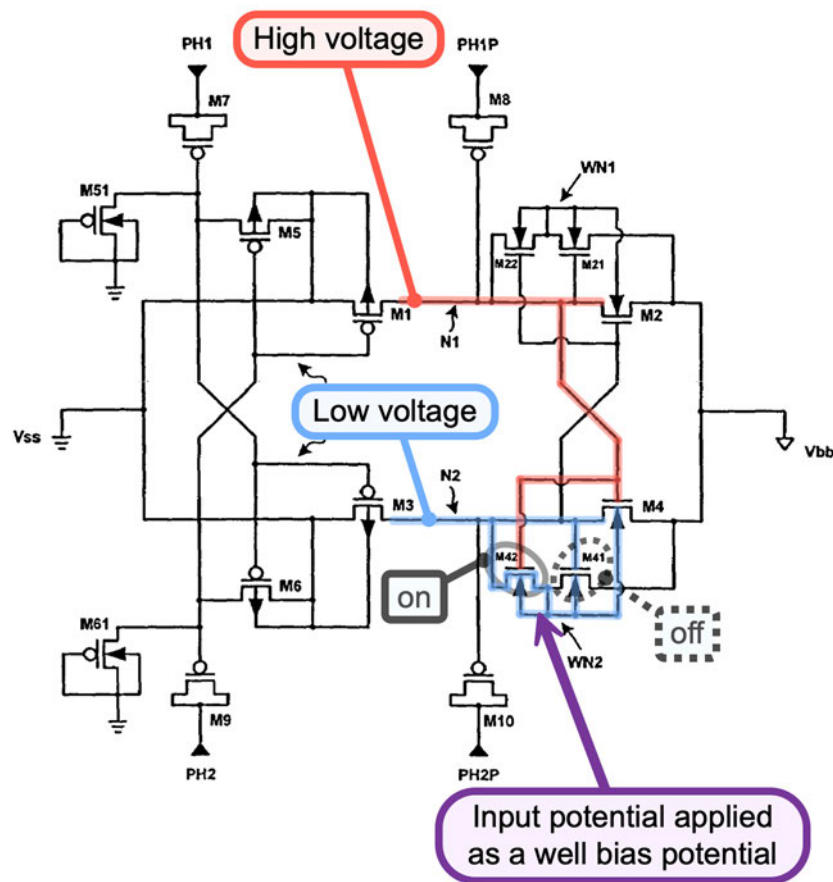


FIG. 3

4. 1[c]: each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching

element in either or both of the first well region and the second well region,

Cordoba discloses 1[c]. Figure 15, shown below, presents “a cross-sectional diagram illustrating the electrical connections for an n-channel *transistor* utilizing a *deep n-well*.” EX1005, Fig. 15, 7:10-12. Cordoba teaches boosting cells that include at least one *switching element* in a first-conductivity type first well region on a substrate. EX1005, 7:13-15 (“The n-channel *transistor* includes a p⁻ *substrate* 110 having a n⁺ doped *deep well* 111 *therein*.”). As identified in Figure 15 below, Cordoba also teaches the placement of a p⁻ *doped well region* 110 (*i.e.*, a second-conductivity type second well region) in the *deep N-well* 111 (*i.e.*, first well region). EX1005, Fig. 15; EX1003, ¶65.

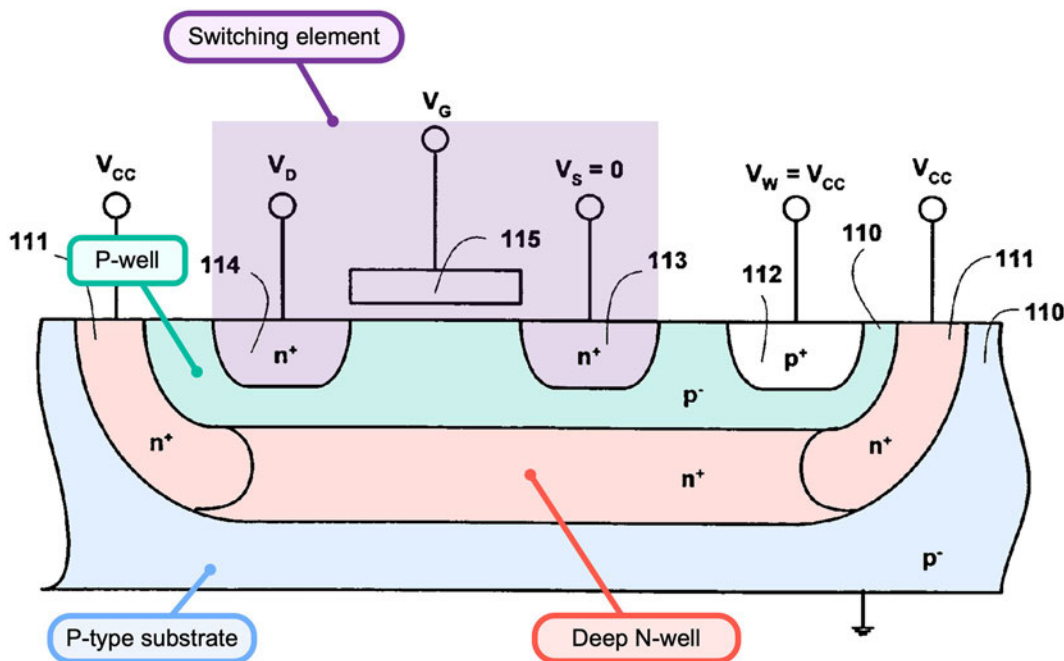


FIG. 15

5. 1[d]: the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and

Cordoba discloses 1[d]. Cordoba discloses switching elements (*i.e.*, pumping transistors M2 and M4) configured to transfer charges from a first terminal (*i.e.*, nodes N1 and N2) to a second terminal (*i.e.*, output of the boosting cell), as shown in Figure 3 below. EX1005, Fig. 3; *id.*, 6:5-9 (“Because it is used to pump the charge stored on node N1 to the output line, transistor M2 may be referred to as a ‘pumping transistor.’ ... [T]he second stage operates in a similar manner.”); EX1003, ¶66.

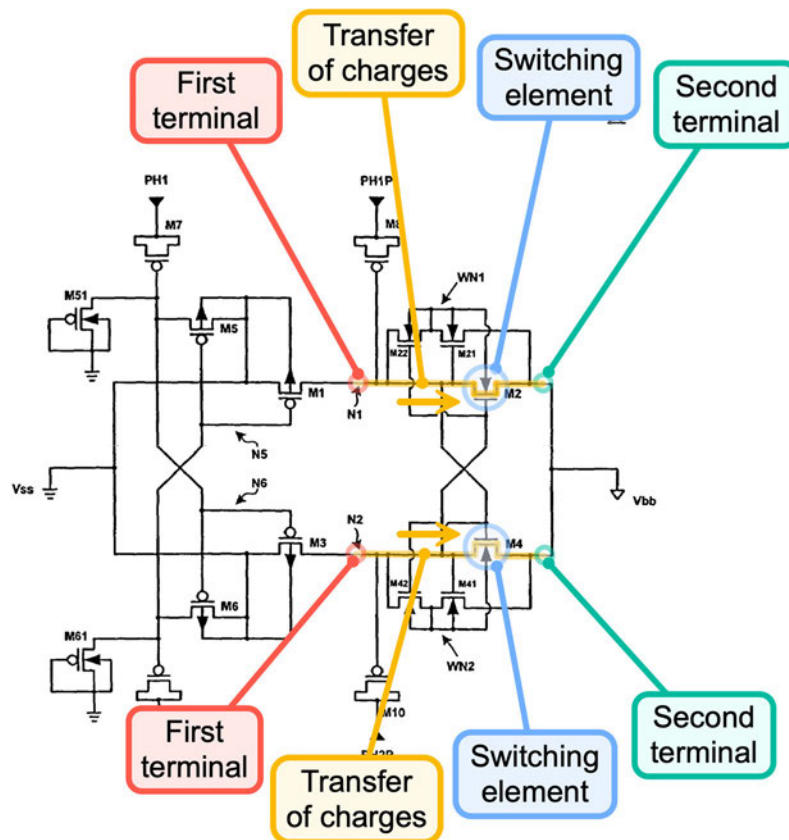


FIG. 3

6. 1[e]: the well bias potential of the at least one analog comparison circuit is applied to the first well region of the

switching element included in the at least one boosting cell of the first and second boosting cell rows.

Cordoba discloses 1[e]. As discussed in 1[b], Cordoba discloses an analog comparison circuit designed to output either the potential at node N1 or N2 (*i.e.*, the input potentials of the boosting cell of the first and second row). §VII.B.3, *supra*. Cordoba teaches the application of that well bias potential to the first well region (*i.e.*, deep N-well) of the switching elements of the first and second boosting cell rows. EX1005, 8:51-54 (“[E]ither Vbb or the voltage at node N1 (whichever is more negative) may be used [by the analog comparison circuit] *to drive the* p-well and *deep n-well of the n-channel transistors* M2, M21, and M22.”); *id.*, 8:65-67 (“[E]ither Vbb or the voltage at node N2 (whichever is more negative) may be used [by the analog comparison circuit] *to drive the* p-well and *deep n-well of the n-channel transistors* M4, M41, and M42.”); EX1003, ¶67. Cordoba therefore teaches the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows. EX1003, ¶67.

- C. Claim 4: The booster circuit of claim 1, wherein the well bias potential is the lower potential out of the input potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row.**

Cordoba discloses claim 4. As discussed in 1[b], when N1 is higher than N2, transistor M42 is switched on while M41 is switched off. §VII.B.3, *supra*.

Moreover, as shown below in Figure 3, transistors M4 and M21 are also switched on given how their gate voltage exceeds their source voltage by virtue of N2 being pulled lower than N1. EX1005, Fig. 3; EX1003, ¶68. As a result, the lower potential of N2 is transmitted across transistors M42, M4, and M21, and applied as a well bias potential as shown below in Figure 3. EX1005, Fig. 3; *id.*, 8:65-67 (“[E]ither Vbb or the voltage at node N2 (*whichever is more negative*) may be used to drive the p-well and deep n-well of the n-channel transistors M4, M41, and M42.”); EX1003, ¶68.

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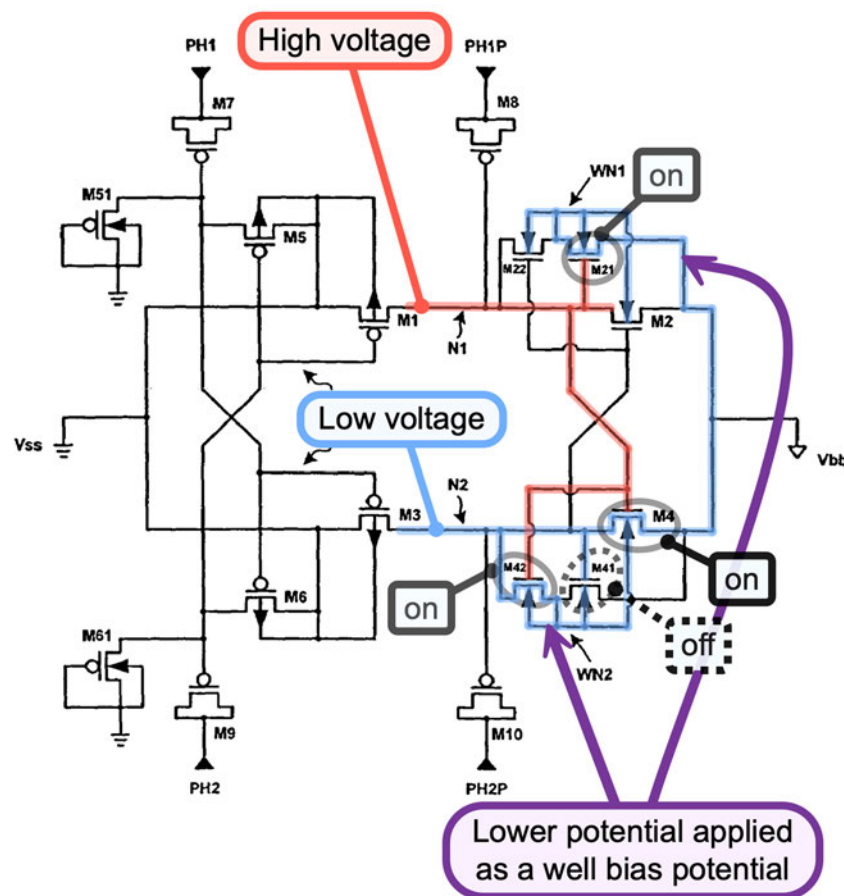


FIG. 3

Alternatively, when N2 is higher than N1, the lower potential of N1 is applied as a well bias potential. As discussed in 1[b], when N2 is higher than N1, transistor M22 is switched on while M21 is switched off. §VII.B.3, *supra*. Moreover, as shown below in Figure 3, transistors M2 and M41 are also switched on given how their gate voltage exceeds their source voltage by virtue of N1 being pulled lower than N2. EX1005, Fig. 3; EX1003, ¶69. As a result, the lower potential of N1 is transmitted across transistors M22, M2, and M41, and applied as a well bias potential as shown below in Figure 3. EX1005, Fig. 3; *id.*, 8:51-54 (“[E]ither Vbb or the voltage at node N1 (*whichever is more negative*) may be used [by the analog comparison circuit] to drive [*i.e.*, applied as a well bias to] the p-well and deep n-well of the n-channel transistors M2, M21, and M22.”); EX1003, ¶69.

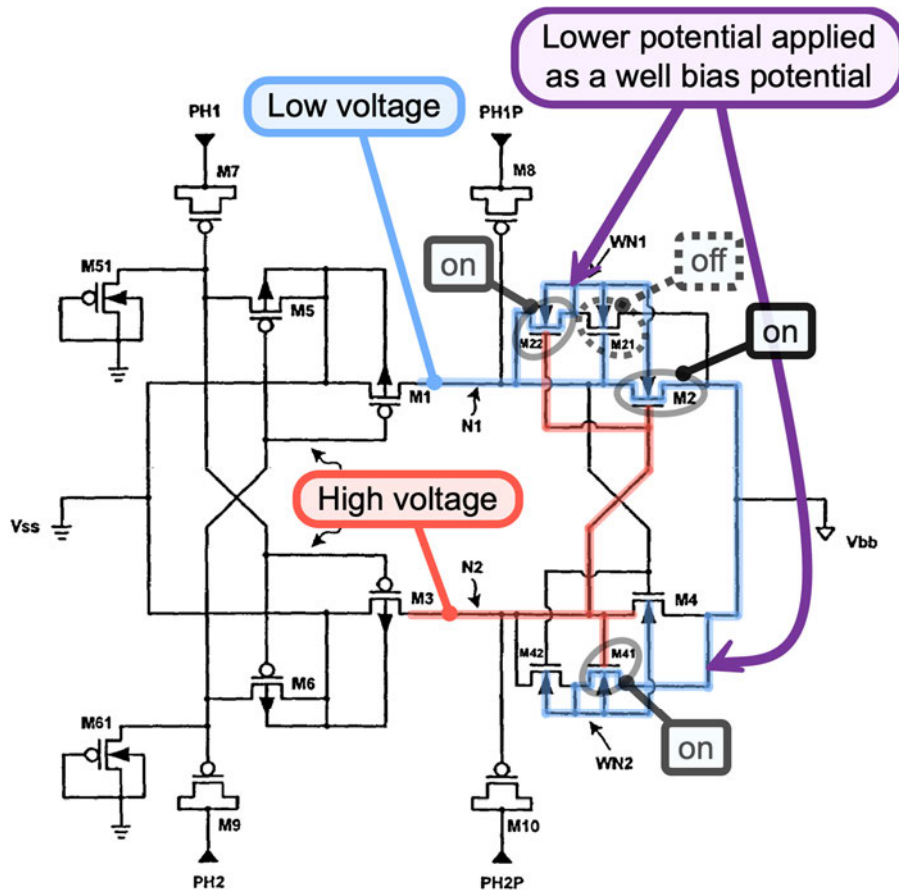


FIG. 3

Cordoba therefore discloses a well bias potential that is the *lower* input potential of the first stage (*i.e.*, $i=1$) out of the input potentials of the first and second boosting cell rows. EX1003, ¶70.

D. Claim 7

1. 7[pre]: The booster circuit of claim 1, wherein:

Cordoba discloses 7[pre] as discussed in claim 1. §VII.B, *supra*.

2. 7[a]: the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-

**conductivity type second well region in the first well region,
and at least one switching element in the first well region or
the second well region, and**

Cordoba discloses 7[a]. Cordoba discloses an analog comparison circuit that has a deep N-well (*i.e.*, a first-conductivity type first well region) on a substrate, and a P-well (*i.e.*, a second-conductivity type second well region) in the deep N-well, with a switching element located in both the P-well and the deep N-well. EX1005, 8:49-51 (“To facilitate well switching, *the n-channel transistors* [*i.e.*, switching elements M2, M21, and M22, which correspond to the analog comparison circuit] of the current embodiment *are formed in a p-well inside of a deep [N-]well.*”); *id.*, 8:62-64 (“To facilitate well switching, *the n-channel transistors* [*i.e.*, switching elements M4, M41, and M42, which correspond to the analog comparison circuit] of the current embodiment *are formed in a p-well inside of a deep [N-]well.*”); EX1003, ¶72.

Figure 15 shown below also illustrates Cordoba’s teaching of a switching element (such as one of the n-channel transistors comprising the analog comparison circuit) in both a P-well and a deep N-well. EX1005, Fig. 15; EX1003, ¶73.

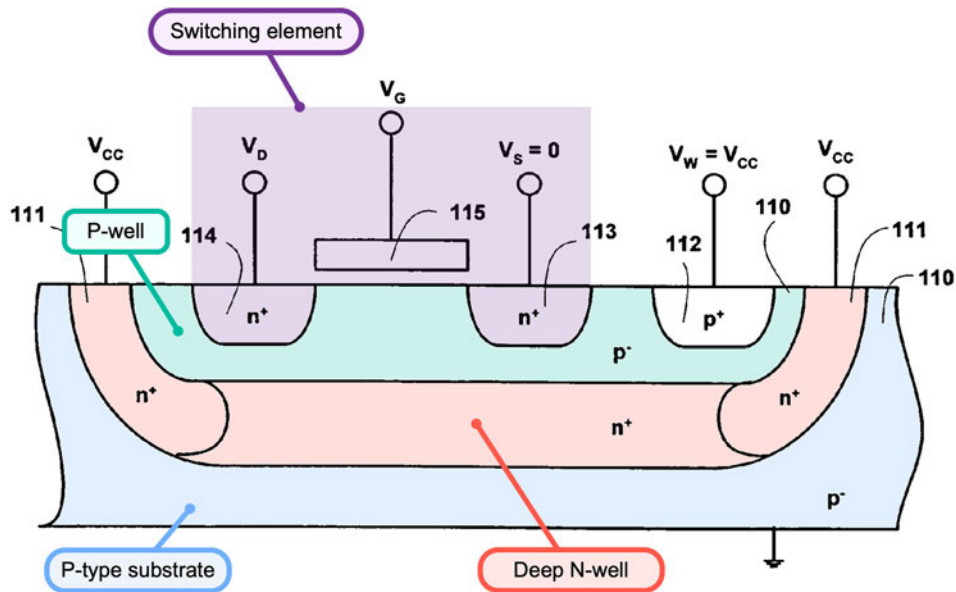


FIG. 15

3. 7[b]: the at least one analog comparison circuit is provided for each boosting cell stage in the first boosting cell row and the second boosting cell row.

Cordoba discloses 7[b]. Cordoba teaches placing an analog comparison circuit for each boosting cell stage in the first and second boosting cell rows. For example, Cordoba's Figure 3, shown below, illustrates the inclusion of one *analog comparison circuit* for the one *boosting cell stage* (i.e., one analog comparison circuit for each boosting cell stage) in the first and second rows. EX1003, Fig. 3; EX1003, ¶74.

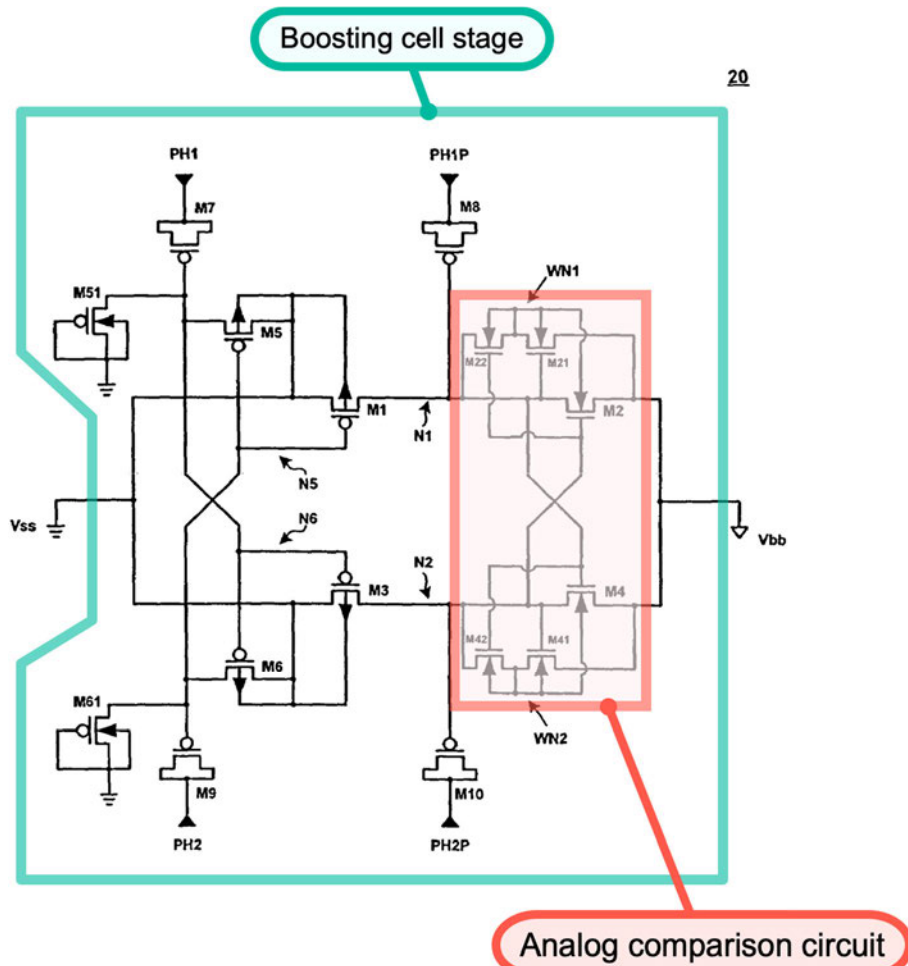


FIG. 3

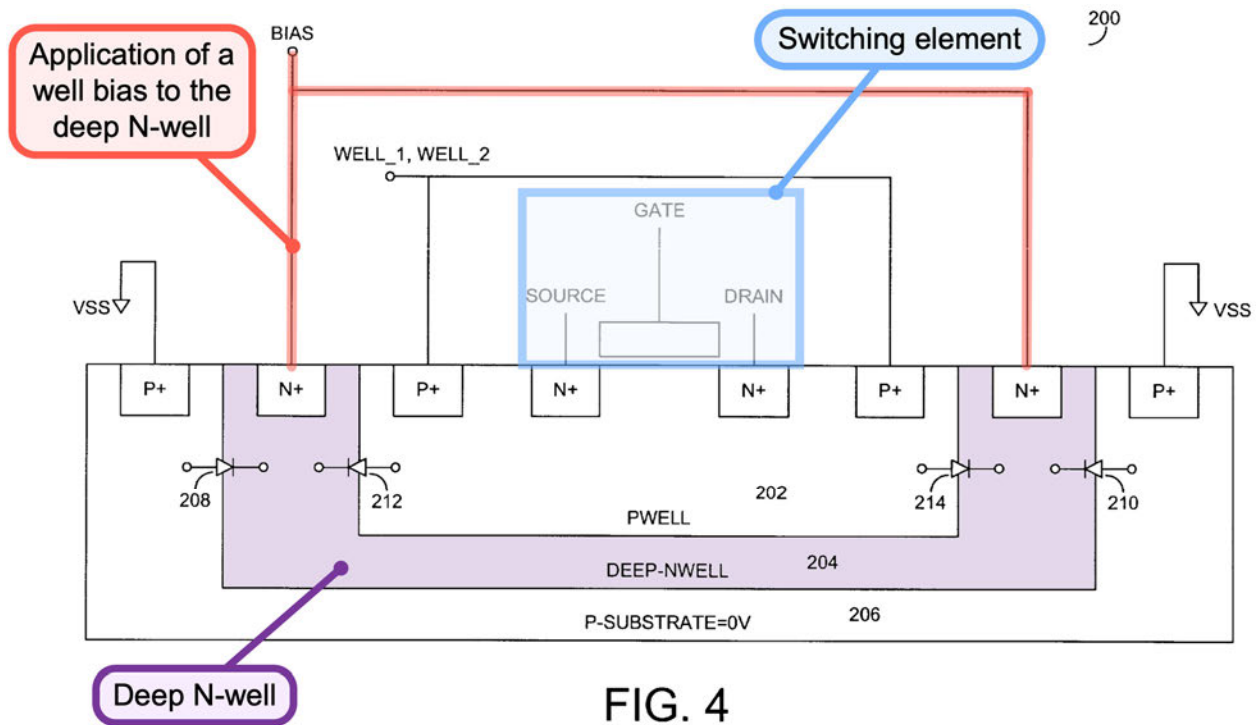
VIII. GROUND 2: MENG ANTICIPATES CLAIMS 1-3, 9, 10, AND 12

A. Overview of Meng

U.S. Patent No. 6,501,325 (“Meng”) was published on December 31, 2002, and therefore qualifies as prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e). Meng teaches a two-row booster circuit comprising “cross-coupled charge pump stages configured to generate an output voltage ... [that] has a greater magnitude than the supply voltage.” EX1006, 2:24-29; EX1003, ¶76. Figure 7 of Meng, shown below with annotations, illustrates the booster circuit and its two-row structure, as

FIG. 7

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**FIG. 4**

The architecture of the booster circuit disclosed in Meng is designed to “(i) have improved efficiency, (ii) have reduced diode drop, (iii) perform well at low supply voltages, (iv) reduce the need for higher breakdown voltage transistors, (v) require little extra die area, and/or (vi) be easily implemented.” EX1006, 2:33-37.

B. Claim 1

1. 1[pre]: A booster circuit comprising:

To the extent this preamble is limiting, Meng discloses a booster circuit. EX1006, Fig. 7; *id.*, 1:7-10 (“The present invention relates to a method and/or architecture for *charge pumps* generally and ... to a method and/or architecture for low voltage supply high efficiency cross-coupled high voltage charge pumps.”); *id.*, 3:15-25 (“The circuit 100 may be implemented, as ... cross-coupled high voltage

charge pump circuit.”). A “charge pump circuit,” which receives a supply voltage and outputs a voltage that has been charged to a level higher than the supply voltage, is a “booster circuit.” EX1003, ¶80; §VII.B.1, *supra*.

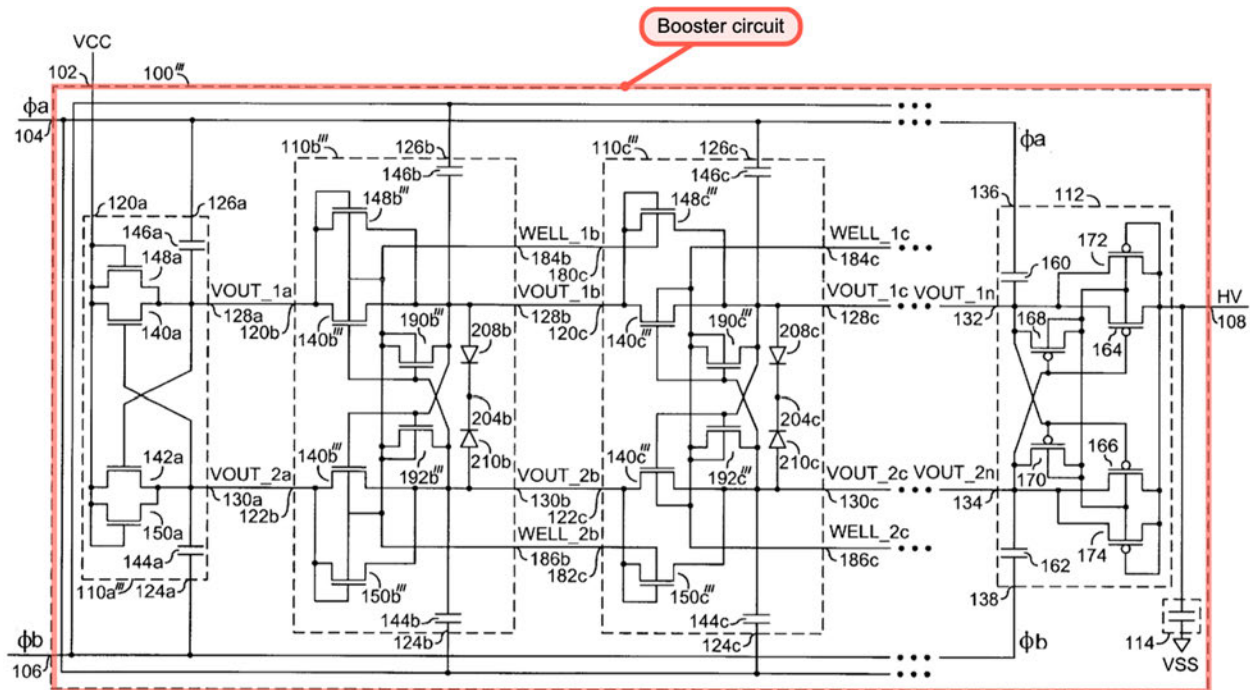


FIG. 7

2. 1[a]: a first boosting cell row including N stages ($N \geq 1$) of boosting cells; a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and

Meng discloses 1[a]. Meng discloses a booster circuit that “may comprise a number of circuits 110^a-110ⁿ,” with each circuit representing a “stage” that comprises two “*boosting cells*.” EX1006, 8:43-46. As illustrated with annotations in Meng’s Figure 7 below, in the **boosting cell stage** 110^b, the **top boosting cell** includes transistors 140^b and 148^b and capacitor 146^b, and the **bottom boosting**

cell includes transistors 142b^{'''} and 150b^{'''} and capacitor 144b. EX1006, Fig. 7, 8:51-65; EX1003, ¶81.

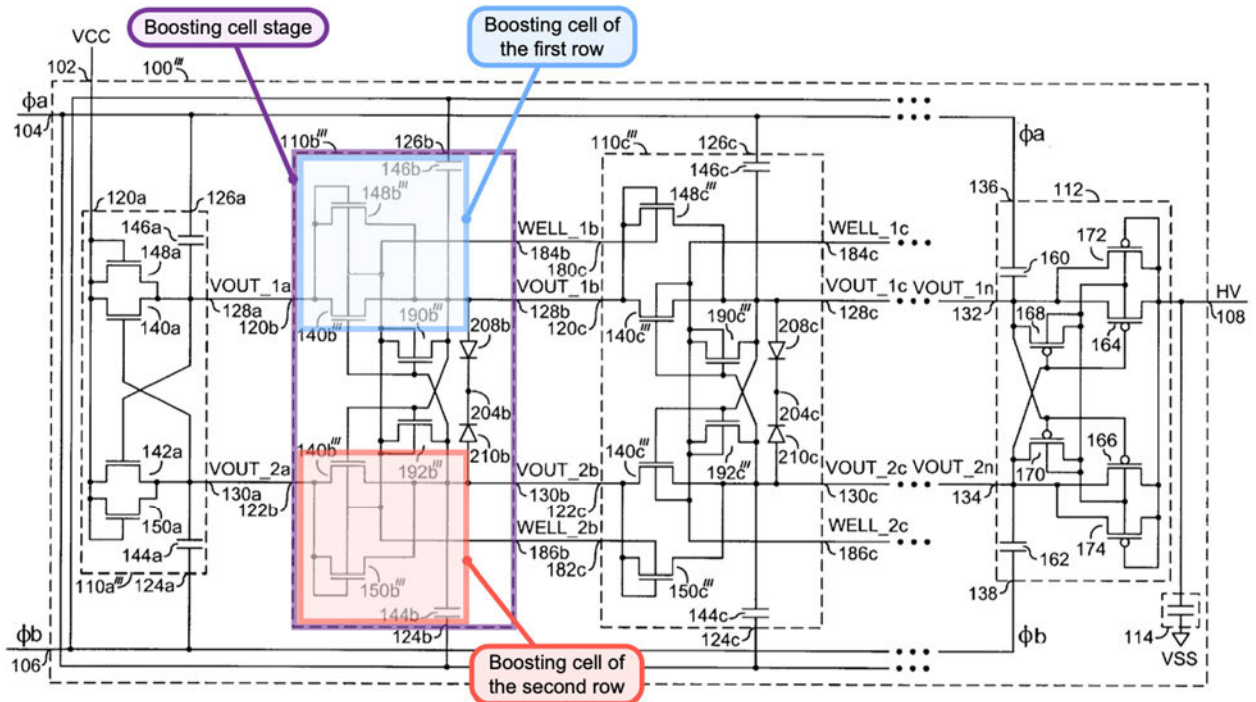
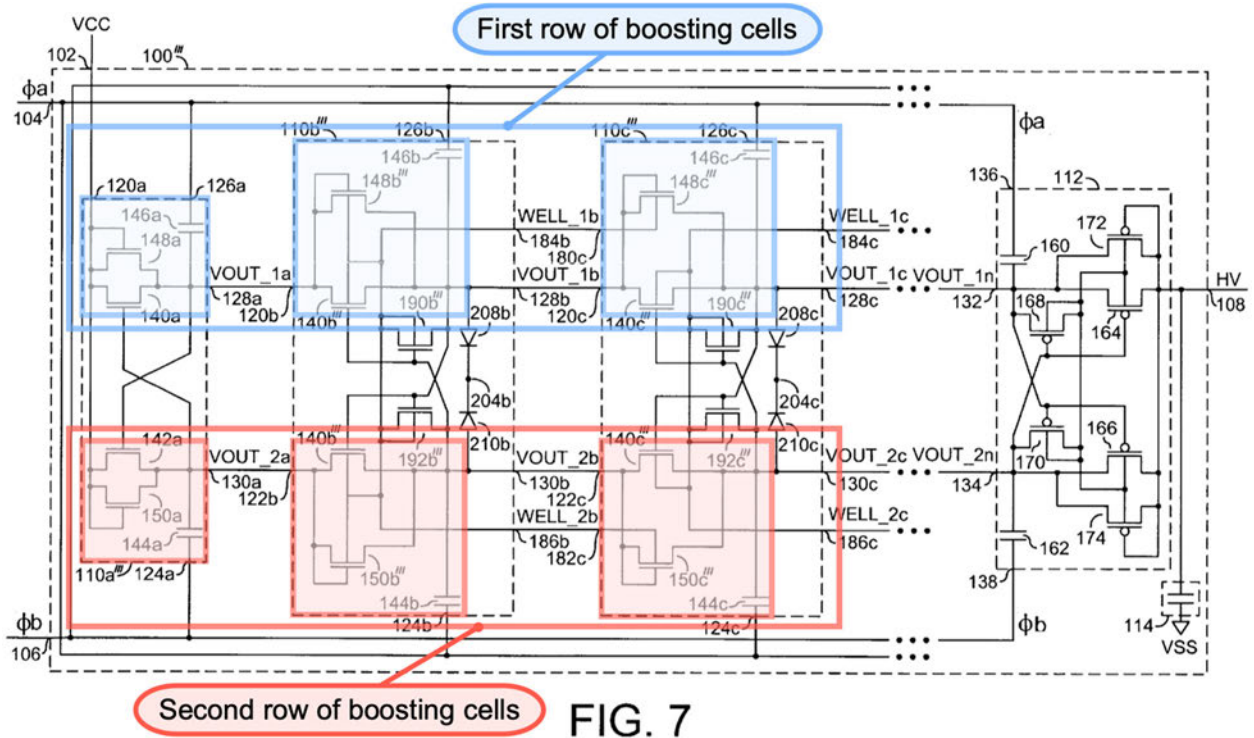


FIG. 7

Meng discloses boosting cell stages with each stage comprising a boosting cell on the first row and a boosting cell on the second row. EX1003, ¶82. Figure 7, shown below, illustrates “a **first boosting cell row**” including at least three stages of boosting cells (N=3) and “a **second boosting cell row**” also including at least three stages of boosting cells (M=3). EX1006, Fig. 7.

¹ Meng’s Figure 7 incorrectly refers to the pumping transistor of the boosting cell in both the first and second boosting cell rows as 140i^{'''}, but a POSITA would have identified this as a typographical error and understood the pumping transistor of the second boosting cell row to be 142i^{'''}, consistent with Meng’s specification. EX1003, ¶81.



- Meng discloses 1[b]. As illustrated with annotations in Figure 7 below, Meng discloses an **analog comparison circuit** for outputting a **well bias potential** generated by the input potentials of the i -th boosting cell stage of the first and second rows (**red** and **blue**, respectively). EX1006, Fig. 7; EX1003, ¶¶83-90.

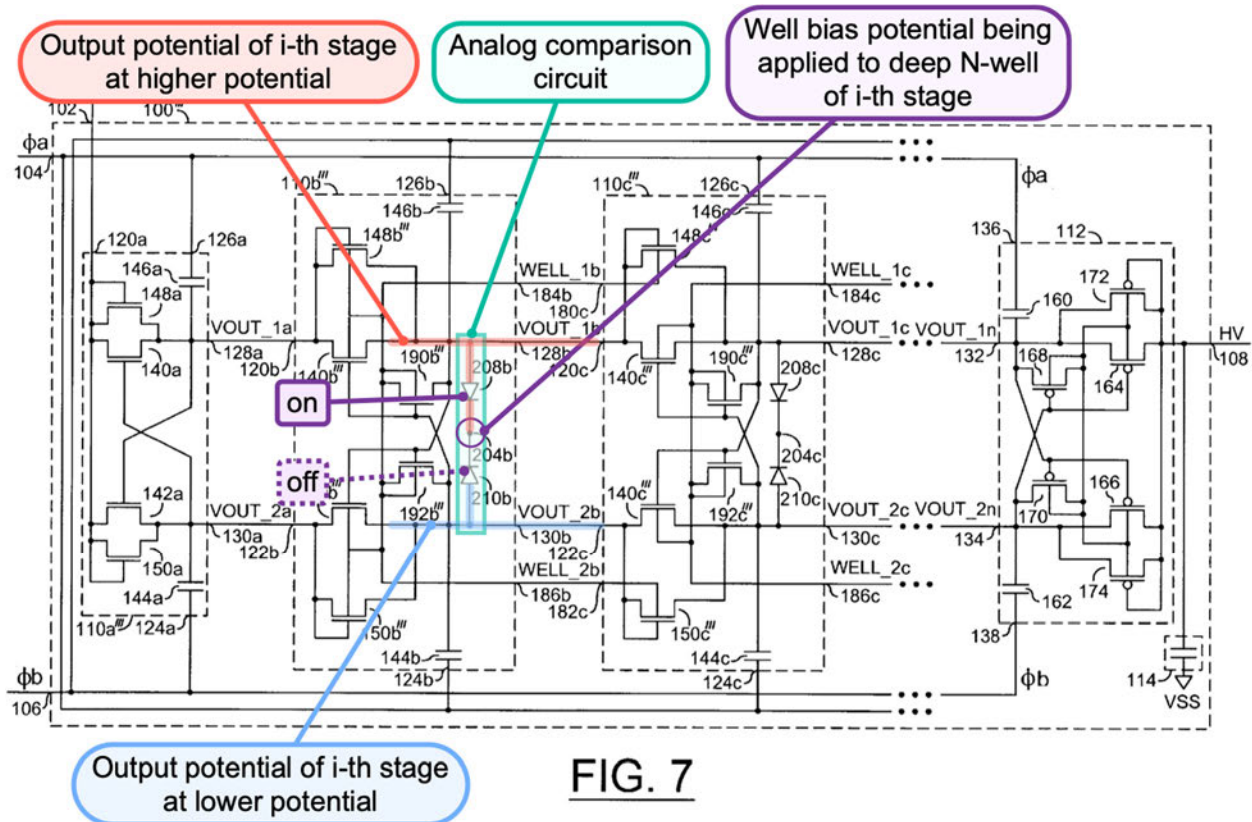


FIG. 7

The analog comparison circuit, as shown above in Figure 7, comprises two explicit diodes (*i.e.*, NMOS transistors with their drains tied to their gates, and with the input being the drain-gate connection and the output being the source terminal), namely, elements 208 i and 210 i , with inputs that correspond to the output potentials of the i -th stage of the first and second boosting cell rows, respectively. EX1006, Fig. 7; EX1003, ¶¶84-89. As discussed above in §IV.C, for any given stage, one row of the boosting stage will have an output potential that is higher than the output potential of the other row due to the alternating clock signals that are applied to the boosting stage. Whichever of the two diodes in the analog comparison circuit 208 i and 210 i has the higher potential at its input terminal is the diode that switches on

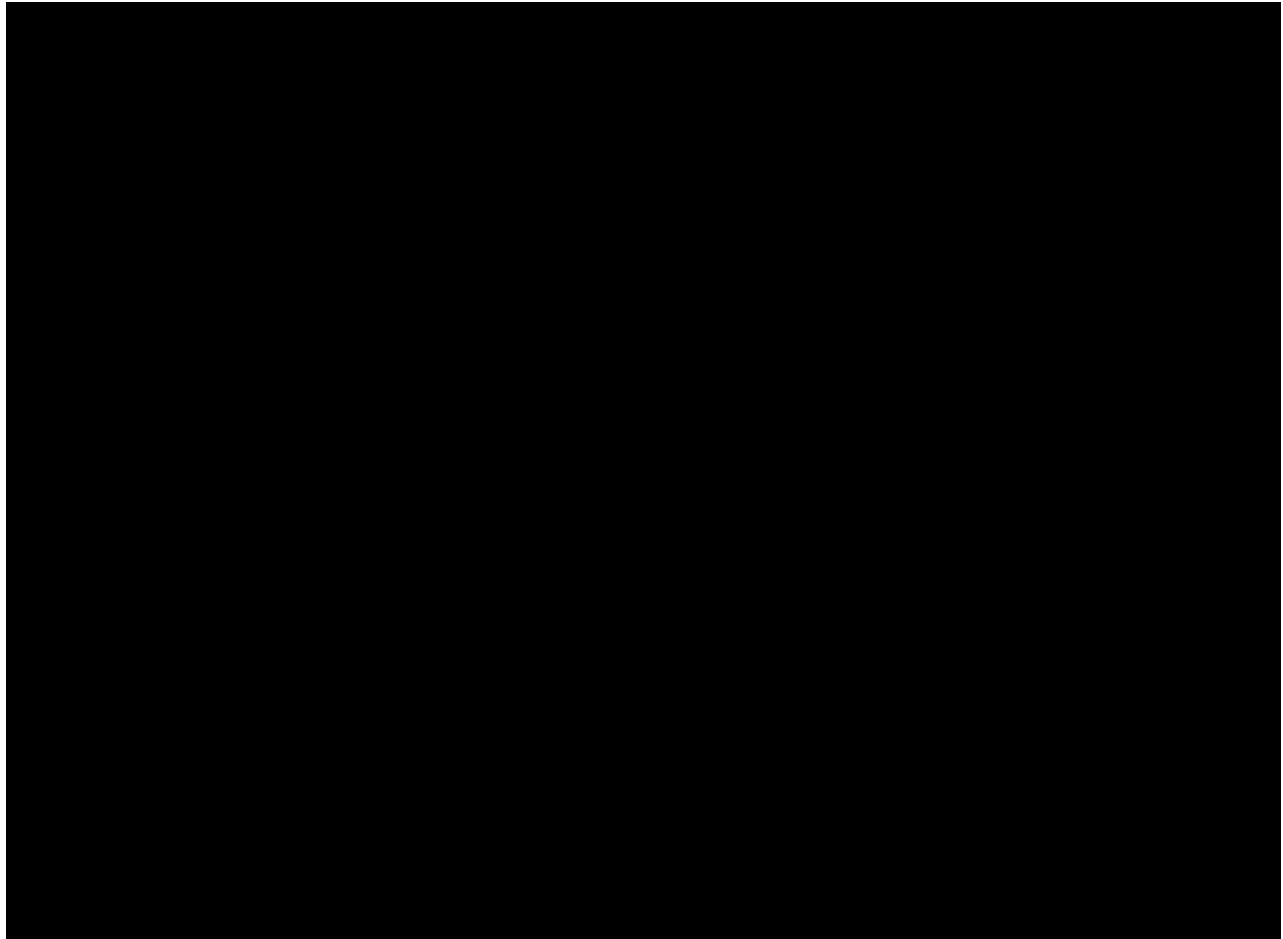
and outputs a well bias potential generated by the higher input potential; the opposing diode in the analog comparison circuit remains off thereby blocking any charge transmission. EX1003, ¶90. The diode (*i.e.*, transistor) that switches on does so because the voltage difference between its input and output is greater than the threshold voltage V_t (*i.e.*, the minimum voltage needed for activation) for that diode; the opposing diode remains off because the voltage difference between its input and output would be negative and far less than the threshold voltage. EX1003, ¶90; *see also* EX1006, Fig. 8 (illustrating the relationship between V_t and the activation of a diode-connected transistor). Meng therefore discloses an analog comparison circuit that outputs a well bias potential generated by the output potentials of the first and second rows of the boosting stage. EX1003, ¶¶83-90.

Identifying the output potential of the i -th stage as an “input potential” in accordance with the claim language is consistent with how the Patent Owner interpreted limitation 1[b]. In particular, in the infringement contentions in the related district court litigation, the Patent Owner contended that the [REDACTED]

[REDACTED]

[REDACTED],

as shown below. EX1008, 7-8; EX1003, ¶91.

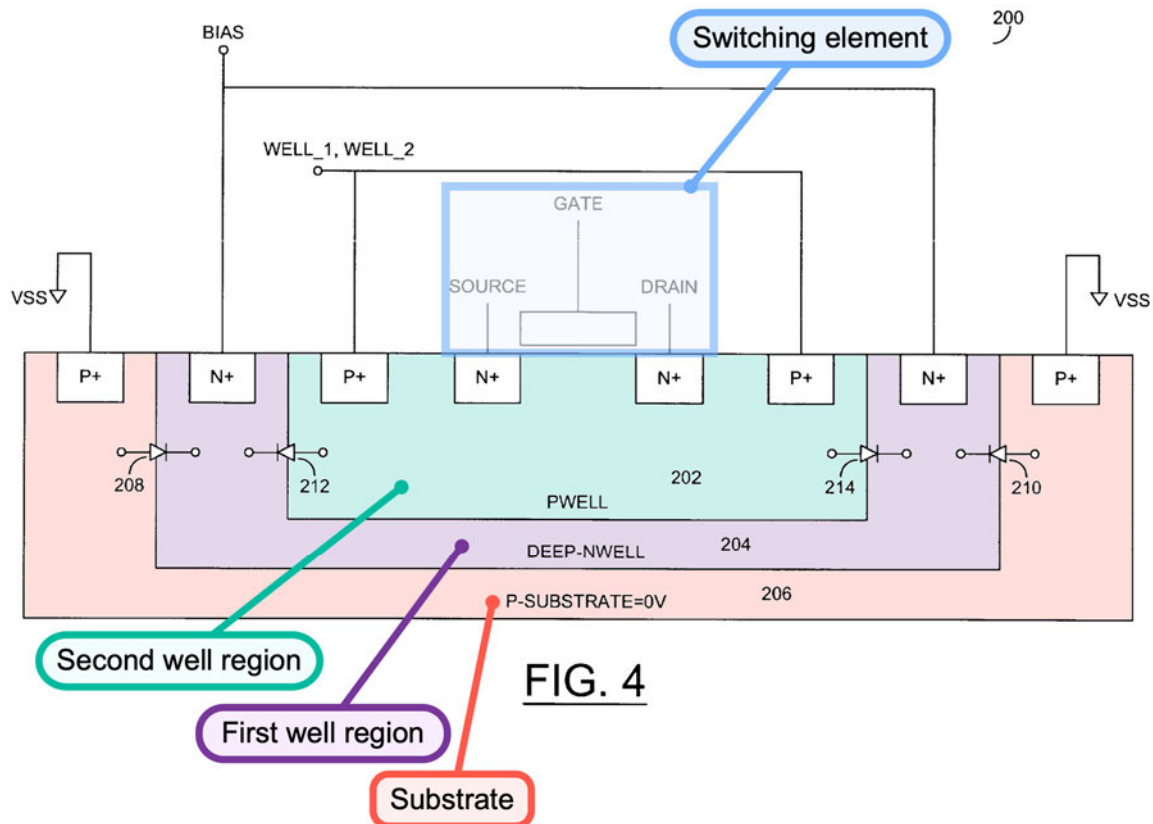


Accordingly, based on at least the Patent Owner's apparent interpretation, Meng also discloses an analog comparison circuit outputting a well bias potential generated by an "input potential." EX1003, ¶92.

4. **1[c]: each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,**

Meng discloses 1[c]. Meng's Figure 4, shown below, provides a cross-sectional illustration of a transistor in Meng's boosting cells. EX1006, 8:61-65 ("The transistors [shown in the boosting stage of Fig. 7] may be implemented as one

or more deep N-well NMOS transistors as shown in FIG. 4.”); EX1003, ¶93. According to Meng, the transistors in each boosting cell “may have a ***P-well region*** ..., a ***deep N-well region*** ..., and a ***P-substrate region***[.]” EX1006, 7:5-10. The deep N-well region—which is a first-conductivity type first well region—is placed on a substrate, and the P-well region—which is a second-conductivity type second well region—is placed in the deep N-well region (*i.e.*, the first well region). EX1003, ¶93. Meng also discloses “at least one switching element,” comprising a source, gate, and drain, in both “the first well region” (*i.e.*, DEEP-NWELL 204) and “the second well region” (*i.e.*, PWELL 202). EX1006, 7:5-10, Fig. 4. The source, gate, and drain form a transistor, which is a “switching element” because the transistor switches the channel between its source and drain on and off based on a change in the voltage at its gate. EX1003, ¶93.



5. 1[d]: the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and

Meng discloses 1[d]. The “transistors 140''b-140''n, 142''b-142''n, 148''b-148''n, 150''b-150''n, 190''b-190''n, and 192''b-192''n [in Meng’s booster circuit] may be implemented as one or more deep N-well *NMOS transistors*.” EX1006, 8:61-64. Switching on transistors 140''b-140''n and 142''b-142''n transfers charges from a “first terminal” (e.g., source) to a “second terminal” (e.g., drain), as do transistors 148''b-148''n and 150''b-150''n. EX1006, 8:61-65; EX1003, ¶94. For example, transistor 140''b (“a **switching element**”) in Figure 7 shown below is

designed to transfer charges from input node 120*b* (“a **first terminal**”) to output node 128*b* (“a **second terminal**”). EX1006, Fig. 7.

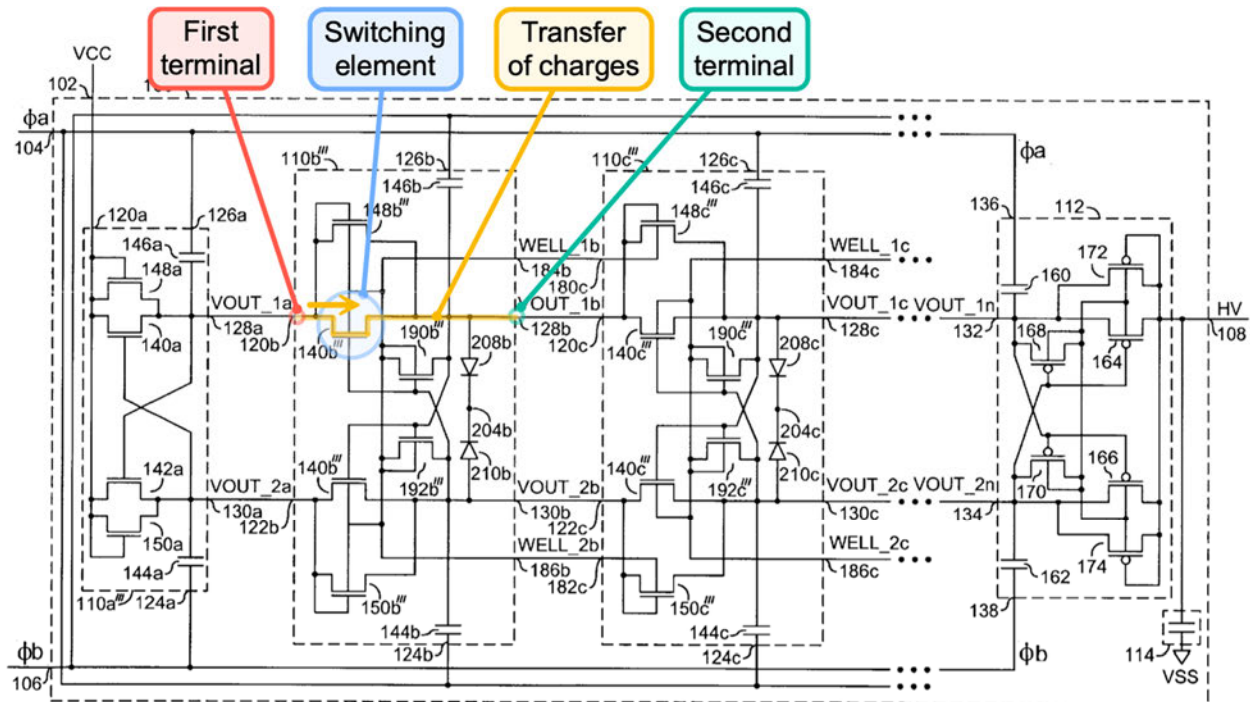
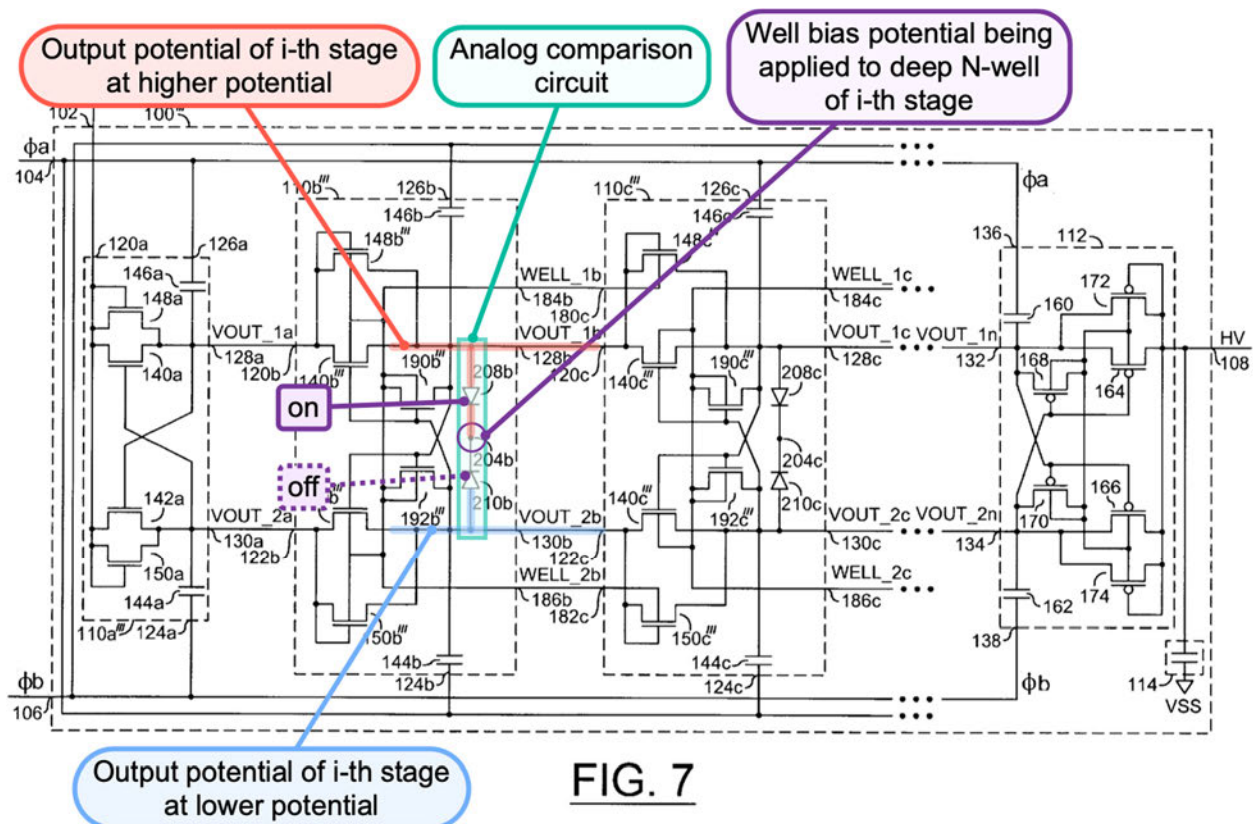


FIG. 7

6. 1[e]: the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

Meng discloses 1[e]. Meng teaches that “[t]he circuit 100” [i.e., the booster circuit] may be implemented using P-well biasing and deep N-well biasing.” EX1006, 8:46-48. As discussed above in 1[b] and shown below in Figure 7, Meng teaches an analog comparison circuit that outputs a well bias potential to a node 204*i*. EX1006, Fig. 7. According to Meng, “[t]he node 204*i* may be the *deep N-well region* of the transistors 140”*i*, 142”*i*, 148”*i*, 150”*i*, 190”*i*, and 192”*i*,” where

transistor 140^{'''i} is the switching element included in the *i*-th boosting cell of the first boosting cell row and transistor 142^{'''i} is the switching element included in the *i*-th boosting cell of the second boosting cell row. EX1006, 9:6-8, Fig. 7. The analog comparison circuit therefore applies a well bias potential to a deep N-well region (*i.e.*, first well region) of the switching elements included in the at least one boosting cell of the first and second boosting cell rows. EX1003, ¶95.



That the well bias potential is applied to the deep N-well (*i.e.*, first well region) is further confirmed by Meng's Figure 8, which "illustrat[es] example [voltage] waveforms of the circuit 100^{'''} of FIG. 7" for "a stage 110^{'''i} of the circuit 100^{'''} over a number of cycles of the signals ϕa and ϕb during pump up." EX1006, Fig. 8,

9:37-41; EX1003, ¶96. As shown below in Figure 8, waveforms 262 and 264 illustrate the output potentials of the i -th stage of the first and second boosting cell rows (VOUT_1i and VOUT_2i), respectively, while “waveform 266 may illustrate the **bias voltage** [*i.e.*, well bias potential] **at the deep N-well region** 204i [*i.e.*, first well region].” EX1006, 9:41-44, Fig. 8. And as would be expected for voltage transmission across a switching element, “[t]he waveforms 262 and 264 [*i.e.*, the output potentials of the i -th boosting cell that are inputs to the analog comparison circuit] and the waveform 266 [*i.e.*, well bias potential applied to the deep N-well region] may have a difference 270” which “may be the threshold voltage V_t ” of the diodes (diode-connected transistors) 208i and 210i. EX1006, 9:46-48; EX1003, ¶96.

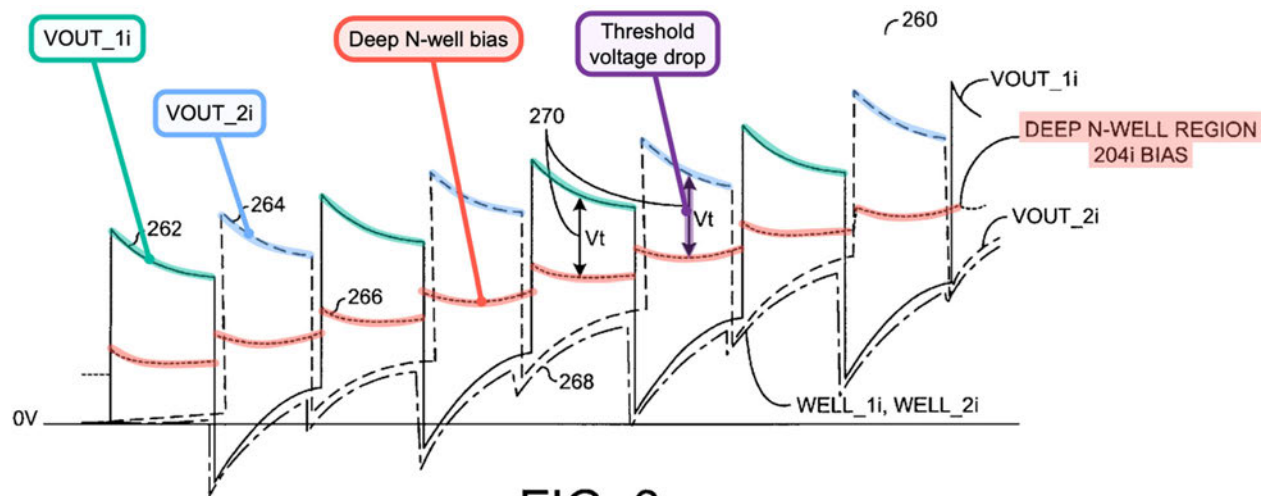


FIG. 8

C. Claim 2

1. 2[pre]: The booster circuit of claim 1, wherein:

Meng discloses 2[pre] as discussed in claim 1. §VIII.B, *supra*.

2. 2[a]: the first boosting cell row includes at least one backflow preventing circuit; the second boosting cell row includes at least one backflow preventing circuit; and

Meng discloses 2[a]. As discussed in 1[a], Meng discloses two boosting cell rows (*i.e.*, a first and a second boosting cell row), each including at least one boosting cell stage. §VIII.B.2, *supra*; EX1003, ¶98.

Meng also discloses at least one backflow preventing circuit in both the first and second boosting cell rows. As shown in Figure 7 below, transistors 140^{'''i} and 148^{'''i} serve as the backflow preventing circuit for the first boosting cell row, and transistors 142^{'''i} and 150^{'''i} serve as the backflow preventing circuit for the second boosting cell row. EX1006, Fig. 7; EX1003, ¶99. As discussed in 1[d], there is charge transfer in the desired rightward direction across transistor 140^{'''i} and 148^{'''i} in the first row, and also across transistors 142^{'''i} and 150^{'''i} in the second row. §VIII.B.5, *supra*; EX1003, ¶99. This rightward charge transfer occurs when the input node of the *i*-th boosting stage (*i.e.*, 120ⁱ and 122ⁱ) has a higher voltage than the output node (*i.e.*, 128ⁱ and 130ⁱ) since pump transistors 140^{'''i} and 148^{'''i} for the first row, and pump transistors 142^{'''i} and 150^{'''i} for the second row are switched on by virtue of their gate potentials being greater than their source (right terminal) potentials. EX1003, ¶99. The occurrence of backflow (*i.e.*, undesirable charge transfer in the leftward direction) is prevented by the backflow preventing circuits 148^{'''i} and 150^{'''i} since they switch off whenever the output nodes 128ⁱ and 130ⁱ have

a higher voltage than the input nodes $120i$ and $122i$; they switch off and prevent charge transfer because the gate and source (left terminals) potentials are equivalent.

Id. Transistor $140'''i$ is also a backflow preventing circuit since once it charges its output $128i$ high, the output on the opposite row $130i$ is pulled low by the clock signal, which then switches transistor $140'''i$ off thereby preventing backflow (leftward). *Id.* Similarly, transistor $142'''i$ is also a backflow preventing circuit since once it charges its output $130i$ high, the output on the opposite row $128i$ is pulled low by the clock signal, which then switches transistor $142'''i$ off thereby preventing backflow (leftward). *Id.*

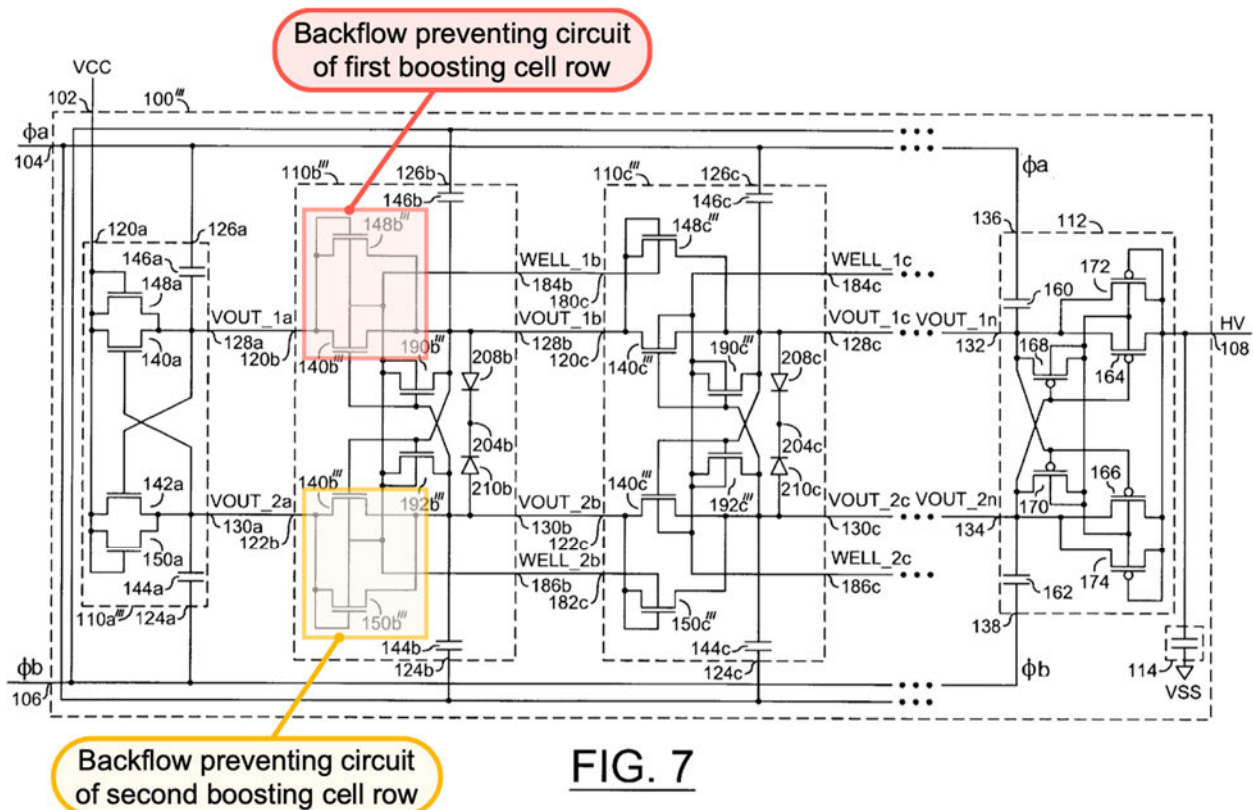
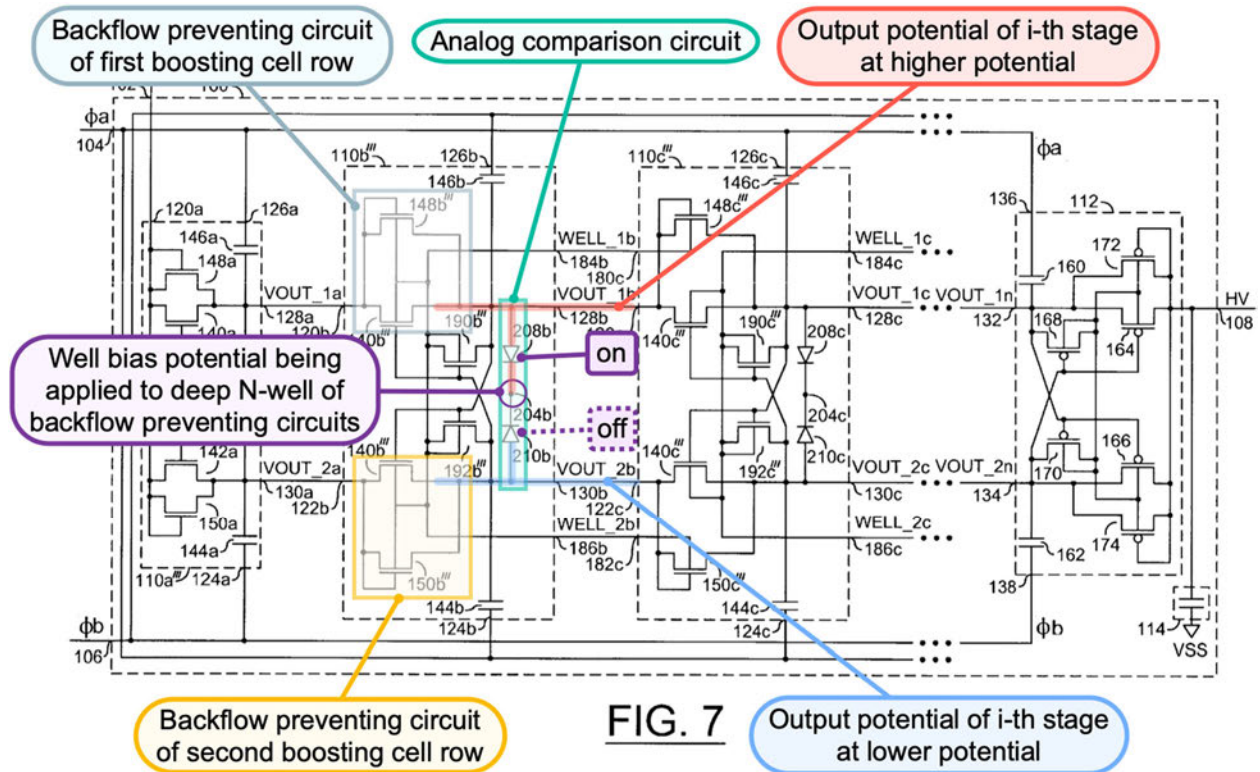


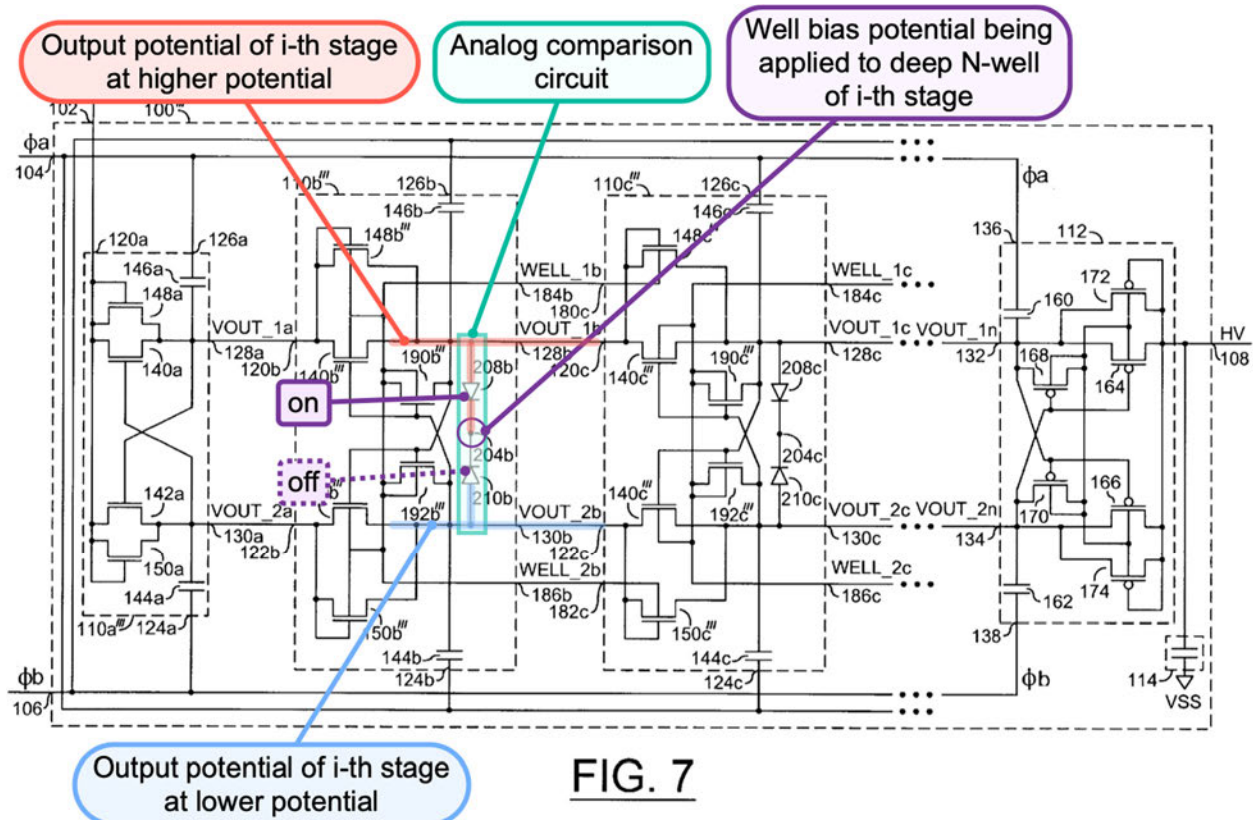
FIG. 7

3. 2[b]: the well bias potential of the at least one analog comparison circuit is applied to a first well region of a

switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.

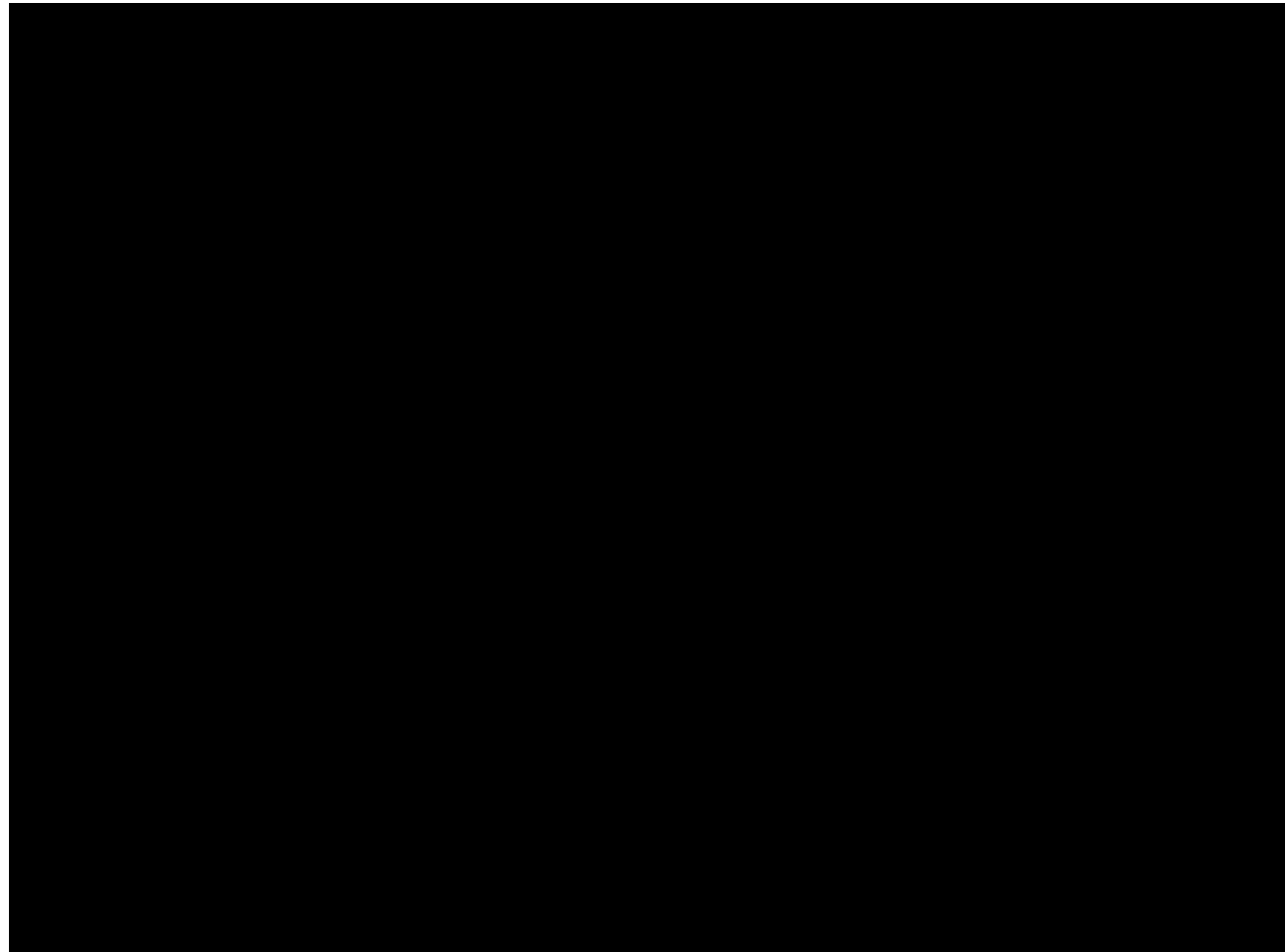
Meng discloses 2[b]. As discussed in 1[b], and as shown below in Figure 7, Meng teaches an analog comparison circuit that outputs a well bias potential to a node 204*i*. §VIII.B.3, *supra*; EX1006, Fig. 7. According to Meng, “[t]he node 204*i* may be the **deep N-well region** of the transistors 140'''*i*, 142'''*i*, 148'''*i*, [and] 150'''*i*,” where, as discussed in 2[a], transistor 140'''*i* is the switching element included in the backflow preventing circuit of the first boosting cell row, and transistor 142'''*i* is the switching element included in the backflow preventing circuit of the second boosting cell row. EX1006, 9:6-8, Fig. 7; §VIII.C.2, *supra*. The analog comparison circuit therefore applies a well bias potential to a deep N-well region (*i.e.*, first well region) of the switching elements included in the at least one backflow preventing circuit of the first and second boosting cell rows. EX1003, ¶100.





Identifying the output potential of the *i*-th stage as an “input potential” in accordance with the claim language is consistent with how the Patent Owner interpreted limitation 1[b]. In particular, in the infringement contentions in the related district court litigation, the Patent Owner contended that the [REDACTED]

[REDACTED], as shown below. EX1008, 7-8; EX1003,
¶102.



Accordingly, based on at least the Patent Owner's apparent interpretation, Meng discloses a well bias potential that is the higher potential out of the input potentials of the boosting cells on the i -th stage of the first and second boosting cell rows. EX1003, ¶103.

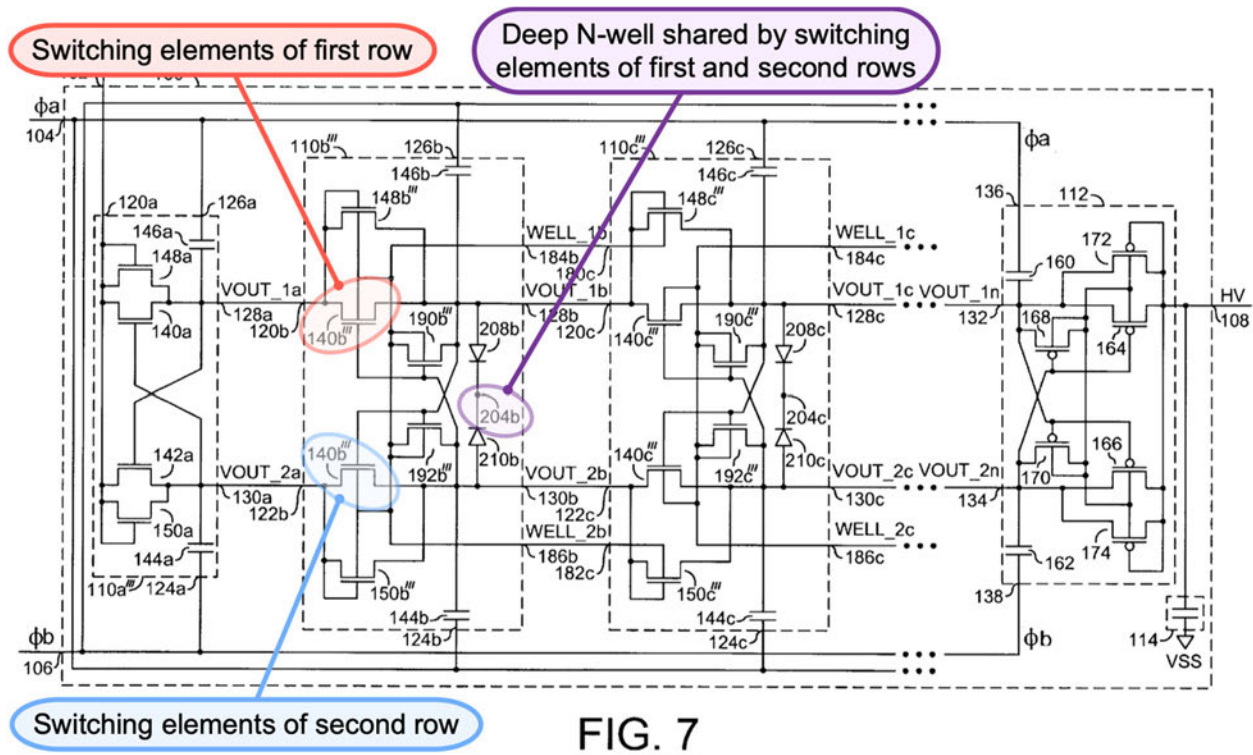
E. Claim 9: The booster circuit of claim 1, wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

Meng discloses claim 9. As discussed in 1[b] and as shown below in Figure 7, Meng discloses a diode 208 i that is provided between a first terminal 128 i and the deep N-well node 204 i (*i.e.*, first well region), as well as a diode 210 i that is provided

1. 10[pre]: The booster circuit of claim 1, wherein:

2. **10[a]:** the at least one switching element of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

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As identified by the annotations to Figure 7 above, transistor 140'''i is the ***switching element*** of the first boosting cell row, and transistor 142'''i is the switching element of the second boosting cell row. EX1006, Fig. 7. And Meng teaches transistors 140'''i and 142'''i (*i.e.*, switching elements of the first and second boosting cell rows, respectively) all share a common deep N-well (*i.e.*, first well region). EX1006, 9:6-7 (“The node 204i may be the deep N-well region of the transistors 140'''i [and] 142'''i.”); EX1003, ¶107.

3. **10[b]:** the at least one switching element of the boosting cell on the i-th stage of the second boosting cell row and a second

element of the at least one analog comparison circuit share a common first well region.

As discussed in 10[a], Meng discloses the switching element of the i -th stage of the second boosting cell row and a second element of the analog comparison circuit sharing a common first well region. §VIII.F.2, *supra*; EX1003, ¶108.

G. Claim 12

1. 12[pre]: A booster circuit comprising:

Meng discloses 12[pre] as discussed in 1[pre]. §VIII.B.1, *supra*.

2. 12[a]: a first boosting cell row including N stages ($N \geq 2$) of boosting cells; and a second boosting cell row including M stages ($M \geq 2$) of the boosting cells, wherein:

As discussed in 1[a], Meng discloses two boosting cells rows (*i.e.*, a first and a second boosting cell row) with each boosting cell row including at least three stages of boosting cells ($N=M=3$). §VIII.B.2, *supra*.

3. 12[b]: each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

As discussed in 1[c], Meng discloses boosting cells each having a deep N-well (*i.e.*, first-conductivity type first well region) on a P-type substrate, and a P-well (*i.e.*, second-conductivity type second well region) in the deep N-well. §VIII.B.4, *supra*. Also as discussed in 1[c], Meng discloses a switching element in both the P-well and deep N-well. §VIII.B.4, *supra*.

4. **12[c]: the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal,**

As discussed in 1[d], Meng discloses switching elements that transfer charges from a first terminal to a second terminal. §VIII.B.5, *supra*. As discussed in 1[d] and 1[e], Meng discloses switching elements that are capable of switching on and off in order to transfer or block charges between terminals on opposing sides of the switching element. §§VIII.B.5, VIII.B.6, *supra*; EX1003, ¶112.

5. **12[d]: a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row and an input potential of the boosting cells of the second boosting cell row, and**

As discussed in 1[b], Meng discloses an analog comparison circuit that outputs a well bias potential. §VIII.B.3, *supra*. As discussed in 1[e], the well bias potential outputted by the analog comparison circuit is applied to the deep N-well (*i.e.*, first well region) of the switching element(s) included in the boosting cell on a second stage, and on stages succeeding the second stage, in the first and second boosting cell rows. §VIII.B.6, *supra*; EX1003, ¶113. And as discussed in 1[b] and 1[e], the operation of the analog comparison circuit, and by extension the generation of the well bias potential, is controlled according to the input potentials of the

boosting cells of the first and second boosting cell rows. §§VIII.B.3, VIII.B.6, *supra*; EX1003, ¶113.

6. 12[e]: an input potential of each of the boosting cells of the first boosting cell row is different from an input potential of each of the boosting cells of the second boosting cell row.

Meng discloses 12[e]. As shown below in Figure 7, Meng discloses, for each boosting cell of both the first and second boosting cell rows, a separate input potential; node 120*i* is the input potential of the boosting cell of the first boosting cell row and node 122*i* is the input potential of the boosting cell of the second boosting cell row. EX1006, Fig. 7; EX1003, ¶114. The input potentials represented by nodes 120*i* and 122*i* reflect two separate nodes and potentials, and are therefore *different* from one another. EX1003, ¶114.

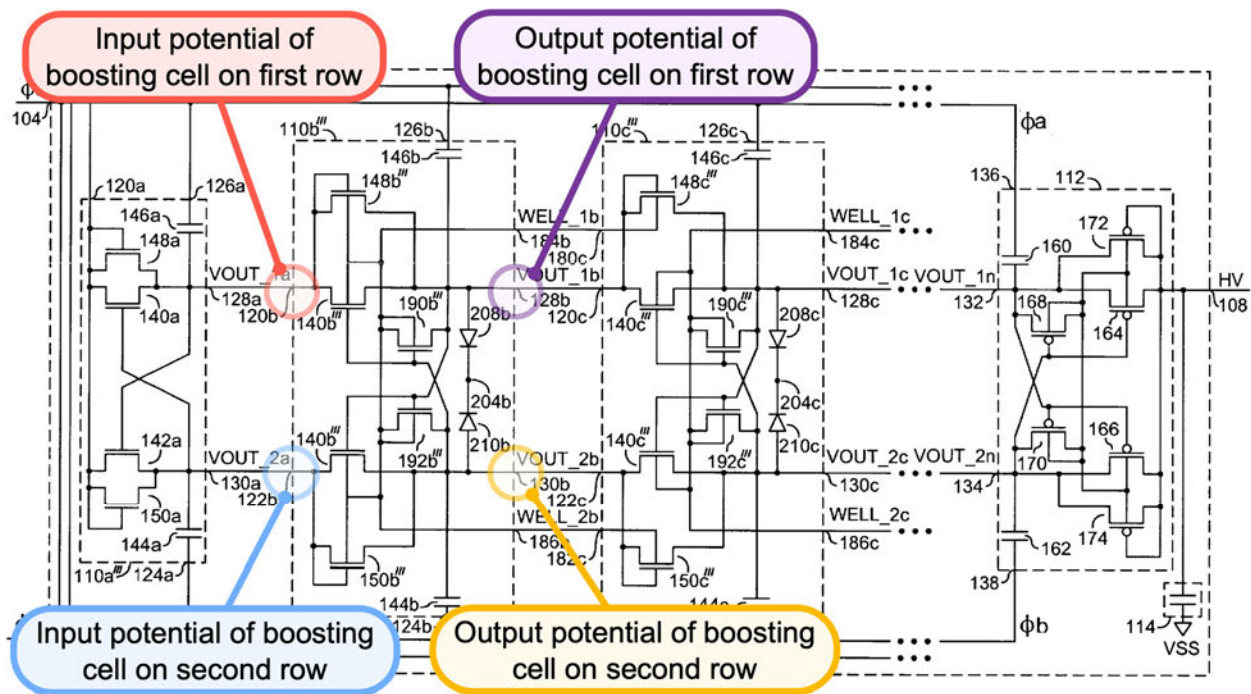
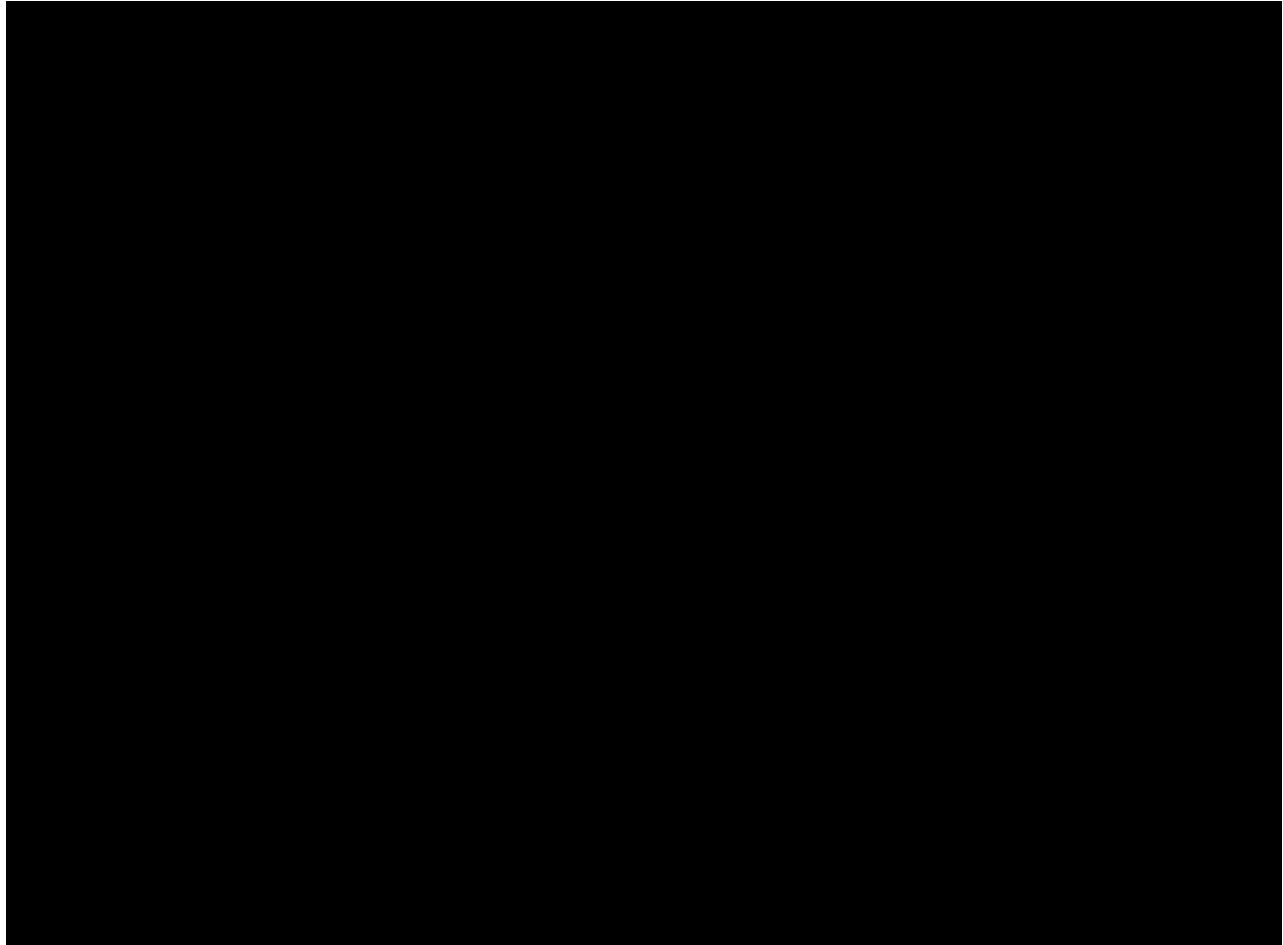


FIG. 7

Further, as discussed in 1[b], Meng discloses an analog comparison circuit that takes as its two inputs both the higher and lower output potentials of the i -th stage boosting cells of the first and second boosting cell rows. §VIII.B.3, *supra*; EX1003, ¶115. Identifying the output potentials of the i -th stage boosting cells of the first and second boosting cell rows as an “input potential” in accordance with the claim language is consistent with how the Patent Owner interpreted limitation 1[b]. In particular, in the infringement contentions in the related district court litigation, the Patent Owner contended that the [REDACTED]

[REDACTED]

[REDACTED], as shown below. EX1008, 7-8; EX1003, ¶116.



Accordingly, based on at least the Patent Owner's apparent interpretation, Meng also discloses "input potentials" of each of the boosting cells of the first and second rows being different from one another. EX1003, ¶¶117-118.

IX. GROUND 3: MENG AND PARK RENDER OBVIOUS CLAIMS 1-10, AND 12

Ground 3 relies on Meng and Park. Park provides an express disclosure of applying a well bias potential to a first well region of a switching element. Thus, to the extent the Board finds that Meng does not disclose "the well bias potential of the at least one analog comparison circuit is applied to the first well region of the

switching element,” that limitation is rendered obvious by Park, as set forth in Ground 3.

A. Overview of Park

U.S. Patent No. 6,914,791 (“Park”) was published on July 5, 2005, and therefore qualifies as prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e). Park teaches a “multi-stage charge pump circuit” comprising “MOSFET devices within a triple well.” EX1007, 3:38-44; EX1003, ¶121. The charge pump detailed by Park includes “an auxiliary device Ms that couples a boosted drain potential of the charge transfer MOS device to the P-well and the deep N-well to switch the coupling between the charge transfer MOS device and the substrate region, thus ... reducing the body effect on the charge transfer MOS device.” EX1007, 5:31-36. By having “the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt” whenever Mt is turned on, the “charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without any voltage loss caused by the body effect.” EX1007, 6:60-7:1. In other words, the application of a well bias potential to both the P-well and deep N-well reduces the body effect, thereby “allow[ing] [the charge pump] to provide more voltage and current at the output so that the charge pump circuit can be implemented in fewer stages.” EX1007, 6:24-26; EX1003, ¶121.

B. Combining Meng with Park

A POSITA would have been motivated to combine Meng's two-row booster circuit structure comprising multiple well regions and an analog comparison circuit with Park's teaching of applying a well bias potential to both the P-well and deep N-well. EX1003, ¶122. The figure shown below illustrates how Park can be combined with Meng to yield a two-row booster circuit with an analog comparison circuit that outputs a well bias potential to a deep N-well. EX1006, Fig. 7; EX1007, Fig. 9.

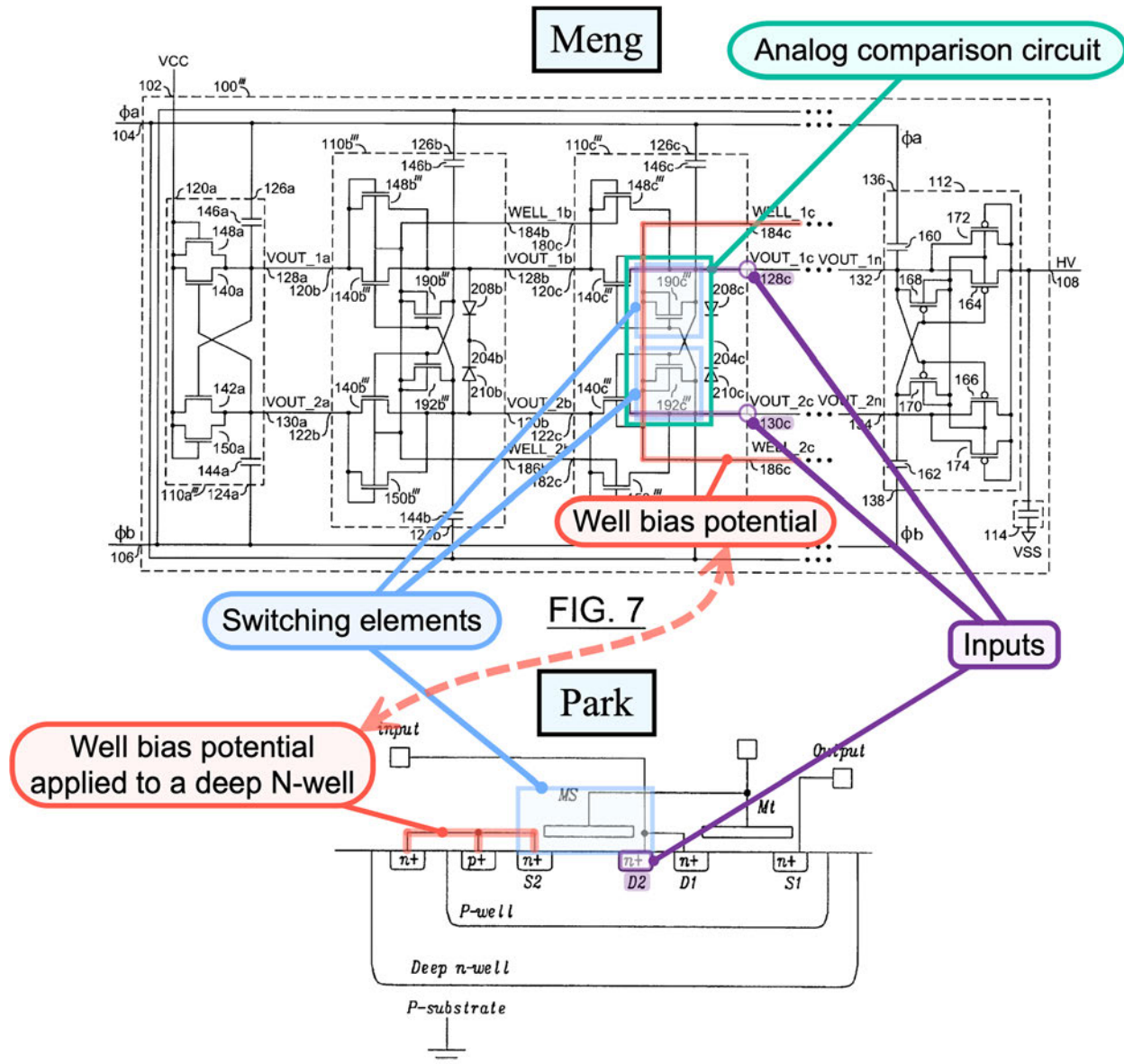


FIG. 9

A POSITA would have found it obvious to combine Meng and Park in order to effectuate Meng's teaching that "[t]he combination of P-well biasing and deep N-well biasing ... may (i) *reduce body effect* and (ii) minimize the threshold voltage V_t across all of the [charge pump] stages." EX1006, 8:30-33; *see also id.*, 9:32-36 ("The combination of P-well biasing and deep N-well biasing ... may (i) reduce

body effect and (ii) minimize the threshold voltage V_t across all of the [charge pump] stages.”). Park states that it is “an *objective* of the present invention to *reduce the body effect* to the charge transfer MOSFET device [*i.e.*, the pump transistor] by the transfer of the boosted source voltage by an auxiliary MOSFET device to the P-well and N-well of each stage.” EX1007, 3:62-66. A POSITA would therefore have been motivated to give effect to Meng’s teachings by incorporating Park’s disclosure of an “auxiliary device [that] *reduces a body effect* on [a] charge transfer device by transferring a boosted ... voltage of the charge transfer device *to the P-well and the deep N-well*.” EX1007, cl. 10; EX1003, ¶123.

Both Meng and Park offer a charge pump design that offers *greater efficiency*, which in turn enables a *reduction in the silicon die area* utilized by the charge pump. EX1006, 2:30-37 (“The objects, features and advantages of the present invention include ... [an] architecture for ... [a] charge pump that may (i) have *improved efficiency*, ... [and] (v) require *little extra die area*.”); EX1007, 6:21-27 (the reduction of the body effect “allows [the charge pump] to provide more voltage and current at the output [*i.e.*, *increased efficiency*] so that the charge pump circuit can be implemented in fewer stages, which results in *less silicon die area*”). A POSITA would have been motivated to incorporate Park’s teachings into Meng because the benefits and improvements offered by Park were aligned with the design objectives described by Meng. EX1003, ¶124.

Indeed, a POSITA would have had a reasonable expectation of success in the combination of Meng and Park. Both Meng and Park provide significant detail regarding the architecture of the charge pump circuit, and both utilize the same set of well-known, conventional circuit components in their charge pump circuit designs. EX1003, ¶125. Implementing Meng using Park's wired connection between the P-well and deep N-well would have been straightforward and well within the capabilities of a POSITA at the time of the '018 patent. *Id.* Moreover, the combination of Meng and Park would have yielded predictable results because both references were directed to charge pump circuits utilizing a multiple-well structure incorporating the same set of circuit components and operating under the same set of parameters. *Id.*

Finally, Meng, Park, and the '018 patent are directed to the same field of endeavor, namely, the design of charge pump circuits that apply a well bias potential to the well regions of a multiple-well structure. EX1001, Abstract, 1:16-17; EX1006, 1:7-10, 7:5-14, 7:49-56; EX1007, Abstract; EX1003, ¶126.

C. Claim 1

1. 1[pre]: A booster circuit comprising:

To the extent this preamble is limiting, Meng discloses a booster circuit for the reasons set forth in Ground 2. §VIII.B.1, *supra*. Meng also discloses an

alternative embodiment shown in Figure 5 below that is a booster circuit. EX1006, Fig. 5; EX1003, ¶127.

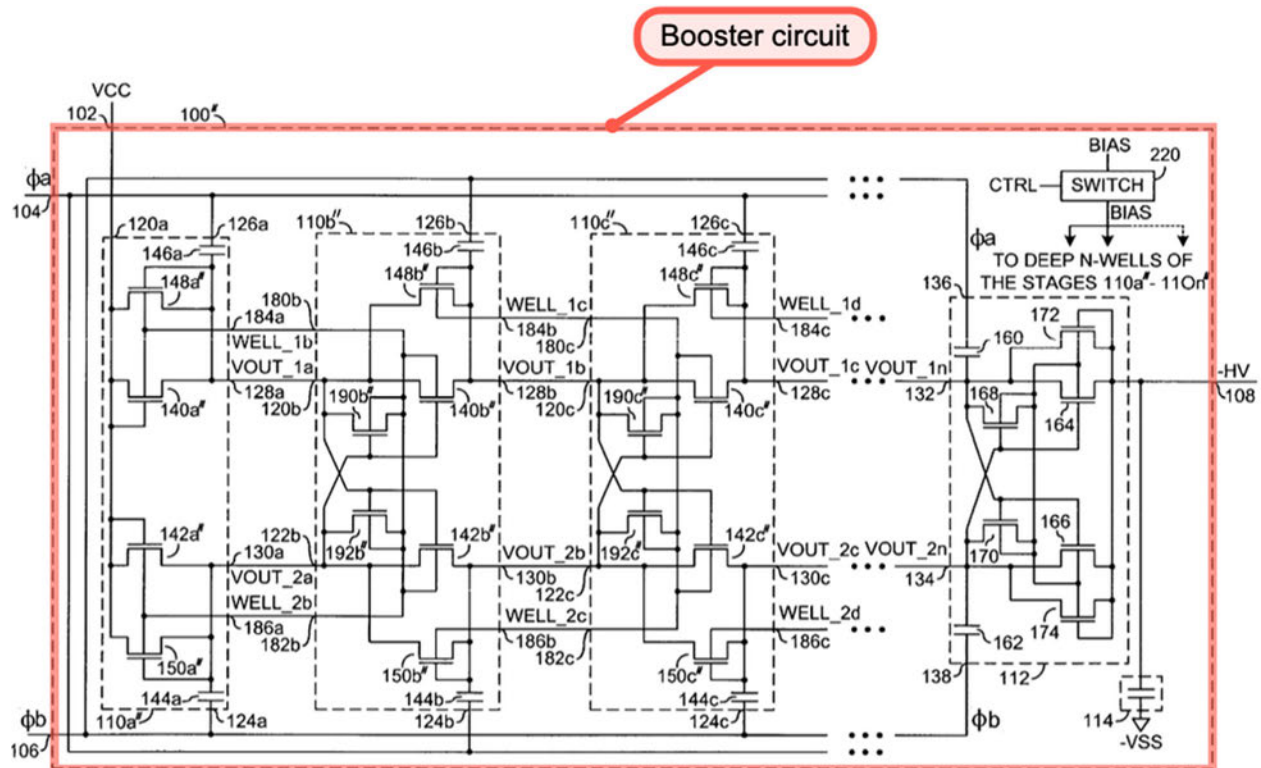


FIG. 5

Park also discloses a booster circuit. EX1007, Fig. 7; *id.*, 1:10-12 (“The present invention relates to integrated circuits and more specifically to charge pump circuits providing high output voltage and current at low power supply voltages.”). As discussed above in Ground 2, limitation 1[pre], a “charge pump” is a “booster circuit.” §VIII.B.1, *supra*; EX1003, ¶128.

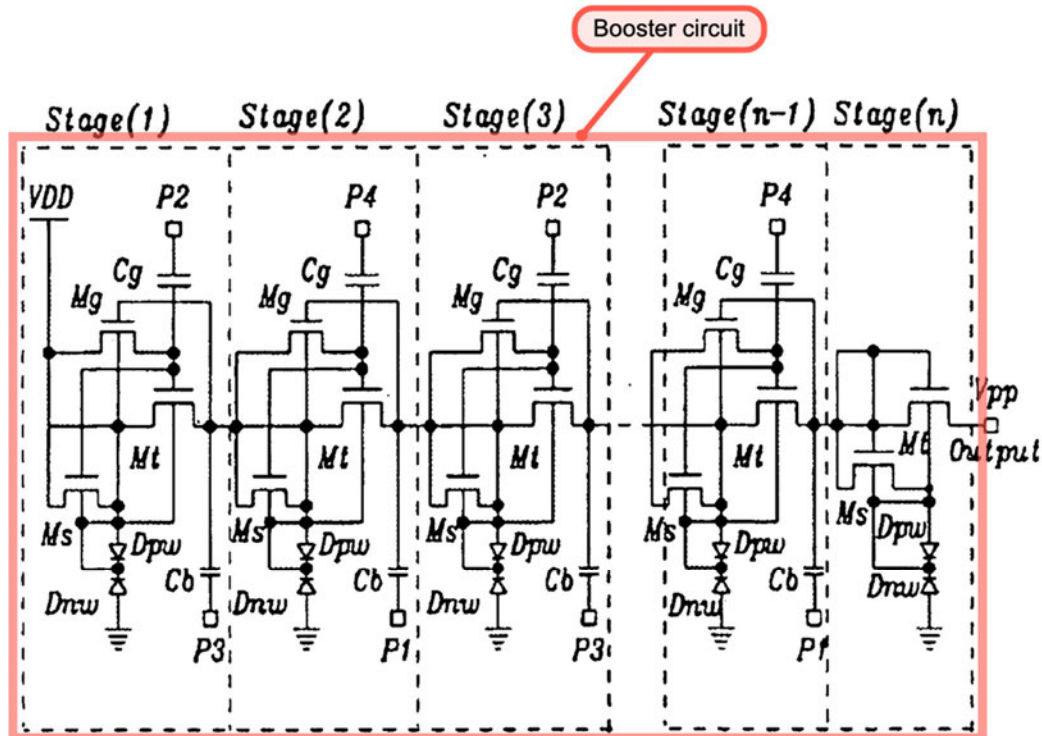
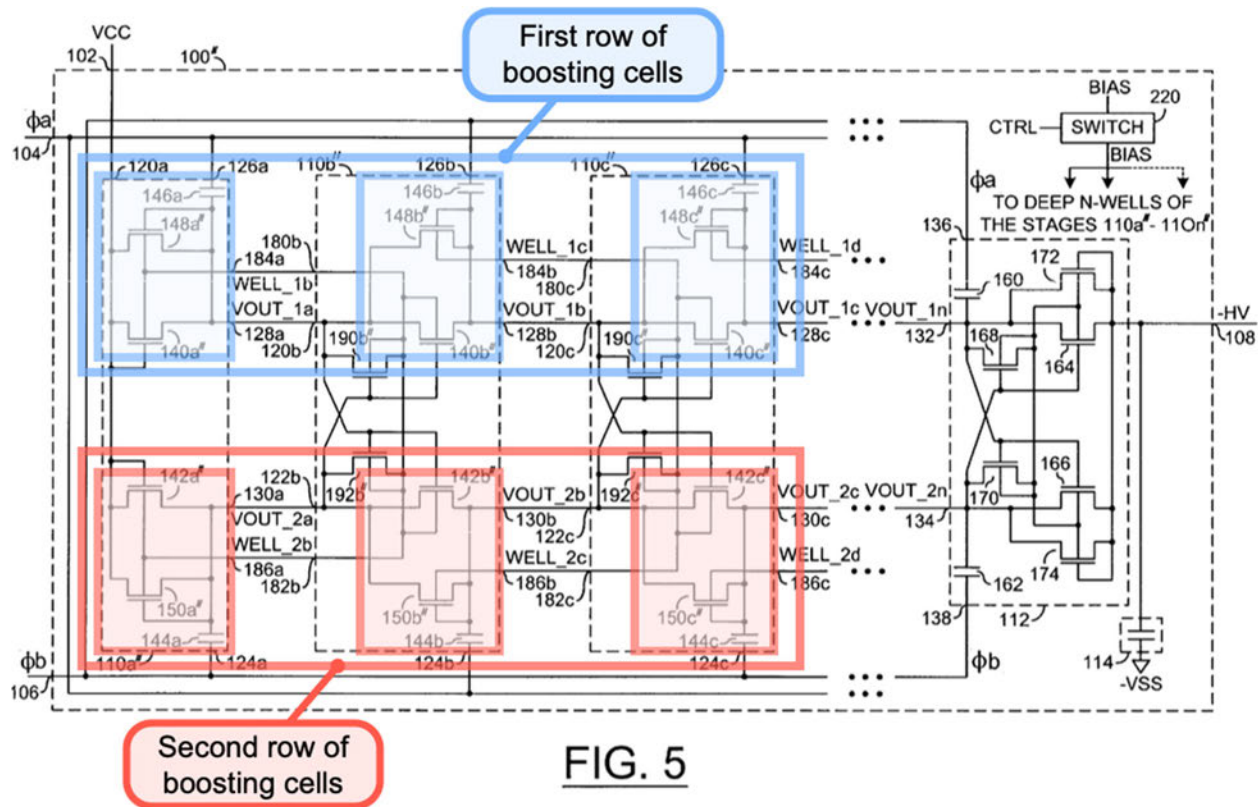


FIG. 7

2. 1[a]: a first boosting cell row including N stages ($N \geq 1$) of boosting cells; a second boosting cell row including M stages ($M \geq 1$) of boosting cells; and

Meng discloses 1[a] for the reasons set forth in Ground 2. §VIII.B.2, *supra*.

Meng's alternative embodiment illustrated in Figure 5 also discloses 1[a]. Figure 5, shown below, illustrates "a **first boosting cell row**" including three stages of boosting cells ($N=3$) and "a **second boosting cell row**" also including three stages of boosting cells ($M=3$). EX1006, Fig. 5; EX1003, ¶129.



3. 1[b]: at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row, wherein:

Meng discloses 1[b]. As illustrated with annotations in Figure 7 below, Meng discloses an **analog comparison circuit** for outputting a **well bias potential** generated by the output potentials of the i -th boosting cell stage of the first and second rows (**red** and **blue**, respectively). EX1006, Fig. 7; EX1003, ¶¶130-132.

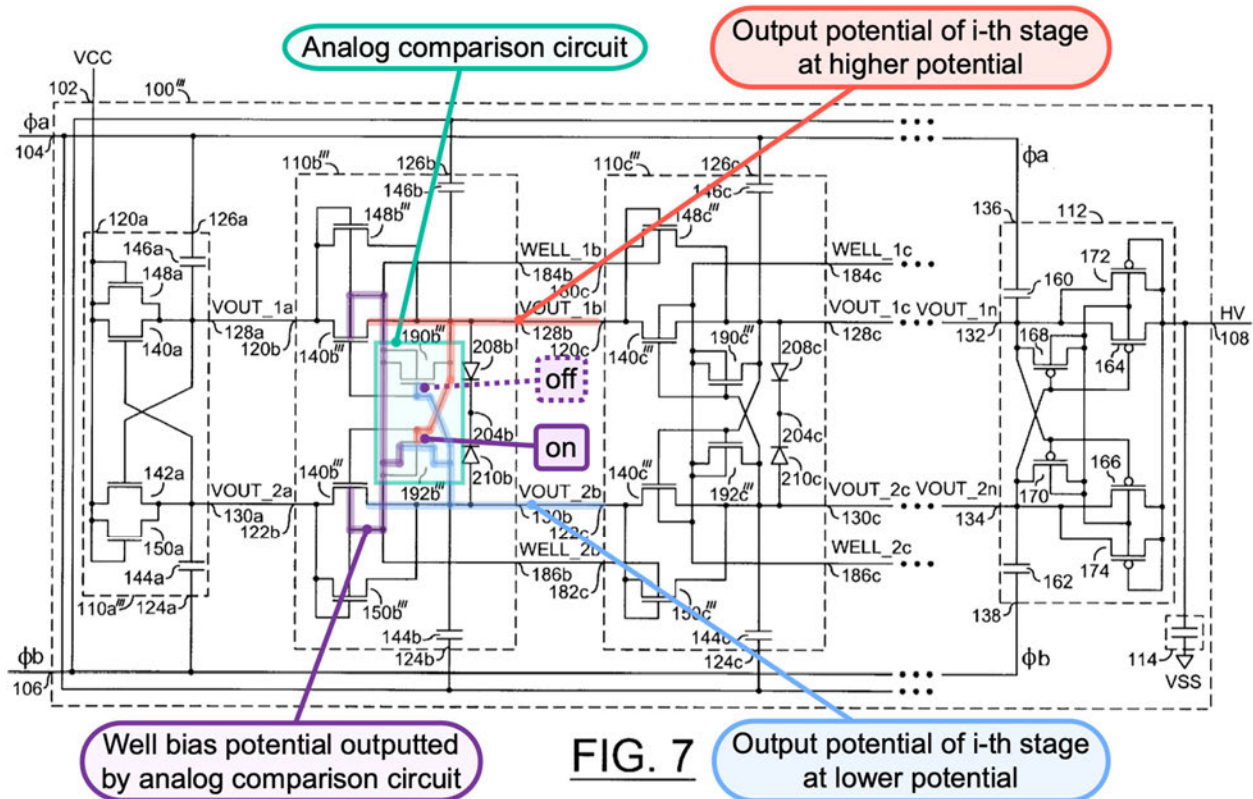


FIG. 7

The analog comparison circuit, as shown above in Figure 7, comprises two cross-coupled NMOS transistors, elements 190ⁱ and 192ⁱ, with inputs that correspond to the output potentials of the *i*-th stage of the first and second boosting cell rows, respectively. EX1006, Fig. 7; *id.*, 9:17-28 (“The signal VOUT_1i may be presented at ... a source of the transistor 190ⁱ, a gate of the transistor 192ⁱ [...] ... The signal VOUT_2i may be presented at ... a gate of the transistor 190ⁱ, a source of the transistor 192ⁱ [...]”); EX1003, ¶131. As discussed above in §IV.C, for any given stage, one row will have an output that has a higher potential than the other due to the alternating clock signals that are applied to the boosting cells of that stage. §IV.C, *supra*. Whichever of the two NMOS transistors in the analog comparison

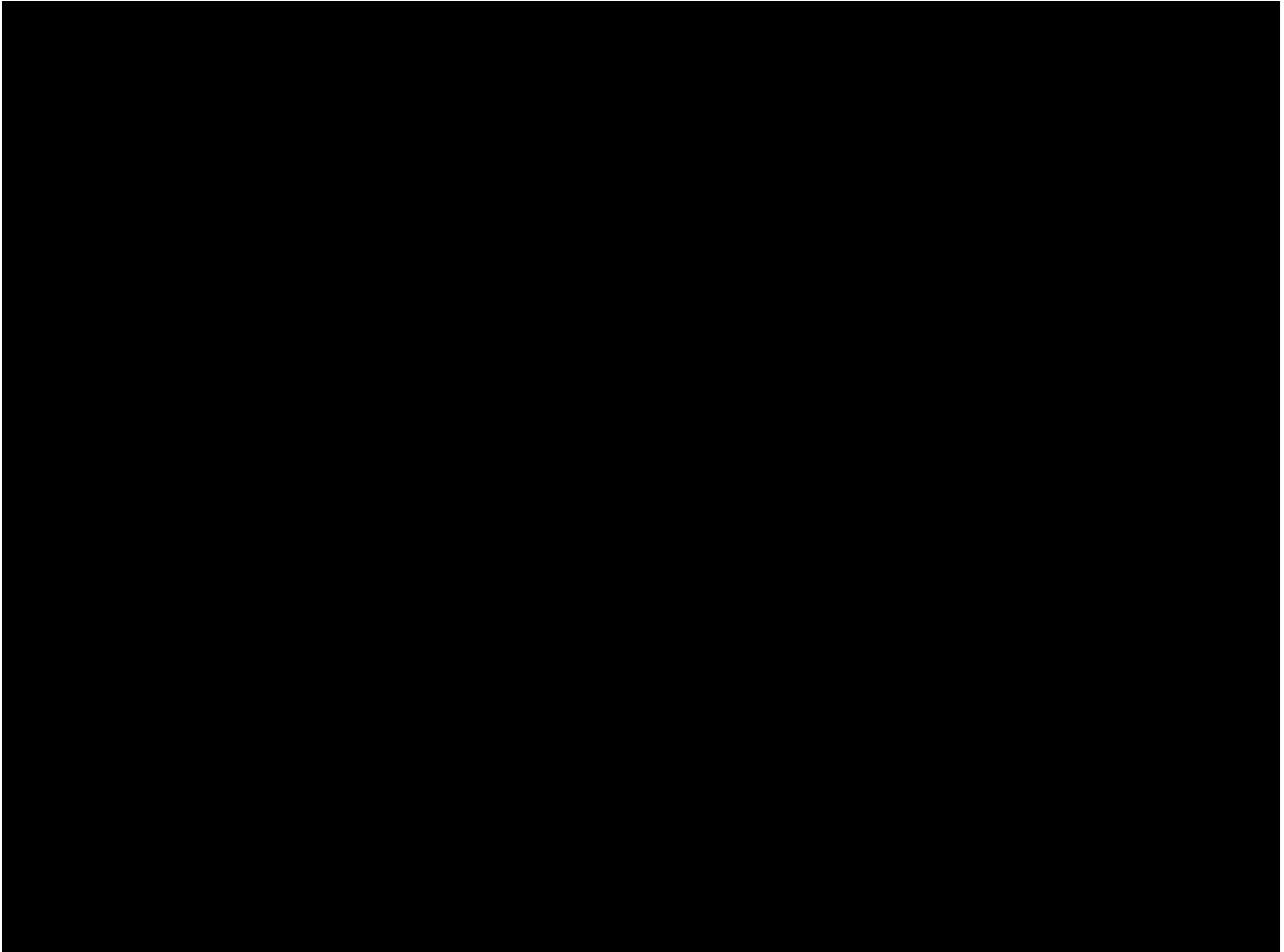
circuit 190*"i* and 192*"i* has the higher potential applied to its gate is the transistor that switches on and outputs a well bias potential; the opposing NMOS transistor in the analog comparison circuit remains off thereby blocking any charge transmission. EX1006, 9:9-10 (“The ***bias signals*** WELL_1*i* and WELL_2*i* may be ***generated by*** the transistors 190*"i* and 192*"i* [*i.e.*, an ***analog comparison circuit***].”); EX1003, ¶131. The NMOS transistor that switches on does so because the voltage difference between the gate and source (*i.e.*, the terminal with the lower potential) is greater than the threshold voltage; the opposing NMOS transistor remains off because the voltage difference between the gate and the source less than zero. EX1003, ¶131.

Given that the NMOS transistors 190*"i* and 192*"i* have gates that are cross-coupled to the output potential of the opposite boosting cell row (VOUT_1*i* or VOUT_2*i*), one of the NMOS transistors will have a higher potential applied to its ***gate***, and therefore will be switched on, due to its gate being cross-coupled to an opposing boosting cell row that has a ***higher*** output potential (*e.g.*, VOUT_1*i*). EX1006, Fig. 7; EX1003, ¶132. The NMOS transistor that is switched on will have an ***input*** that is the ***lower*** boosting stage output potential (*e.g.*, VOUT_2*i*), which means that the well bias potential that is outputted by the analog comparison circuit is ***generated*** by the ***lower*** of the two boosting stage output potentials (*i.e.*, VOUT_1*i* and VOUT_2*i*). EX1006, Fig. 7; EX1003, ¶132. Meng therefore teaches an analog comparison circuit (*i.e.*, transistors 190*"i* and 192*"i*) for outputting a well bias

potential (*i.e.*, bias signals WELL_1*i* and WELL_2*i*) generated by the output potentials of the boosting cells of the first and second boosting cell rows (*i.e.*, signals VOUT_1*i* and VOUT_2*i*). EX1003, ¶132. Identifying the output potential of the *i*-th stage as an “input potential” in accordance with the claim language is consistent with how the Patent Owner interpreted limitation 1[b]. In particular, in the infringement contentions in the related district court litigation, the Patent Owner contended that the [REDACTED]

[REDACTED]

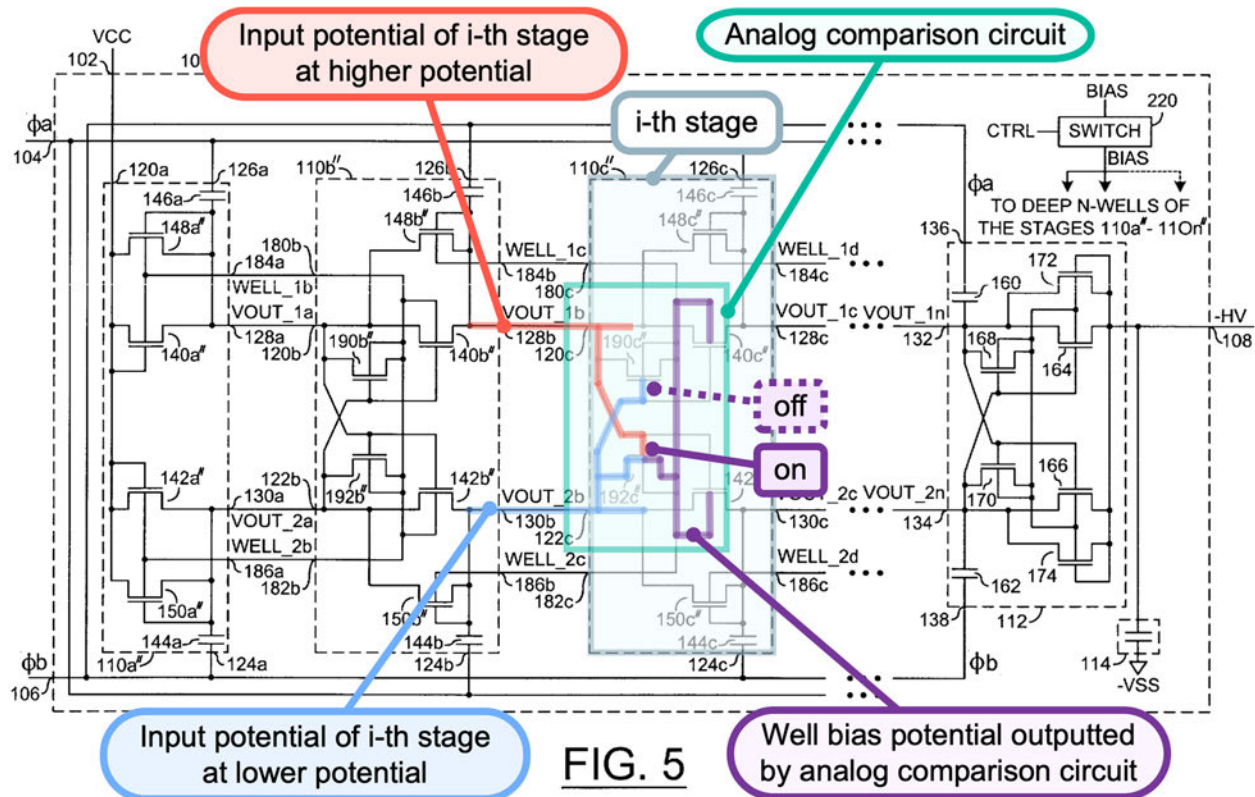
[REDACTED], as shown below. EX1008, 7-8; EX1003, ¶133.



Accordingly, based on at least the Patent Owner's apparent interpretation, Meng also discloses an analog comparison circuit outputting a well bias potential generated by an "input potential." EX1003, ¶134.

In an alternative embodiment, Meng teaches an analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cells of the first and second rows. As illustrated with annotations in Figure 5 below, Meng discloses an **analog comparison circuit** comprising transistors 190"*i* and 192"*i* for outputting a **well bias potential** generated by the input potentials of the *i*-th boosting stage of the first and second rows (**red** and **blue**, respectively). EX1006, Fig. 5. The

cross-coupled transistors 190"*i* and 192"*i* operate in the same manner as the transistors 190"*i* and 192"*i* described above with respect to the embodiment illustrated in Figure 7. EX1003, ¶135. For the analog comparison circuit identified below in Figure 5, one of the transistors 190"*i* and 192"*i* will switch on (*i.e.*, the transistor with a gate that is cross-coupled to the boosting cell row with the higher potential), thereby outputting a well bias potential. EX1006, Fig. 5; *see also id.*, 8:16-18 (“Where a stage 110"*i* is any one of the stages 110"*b*-110"*n*, at each stage 110"*i*, the ***bias signals*** WELL_1*i* and WELL_2*i* may be ***generated by*** the transistors 190"*i* and 192"*i* [*i.e.*, an ***analog comparison circuit***].”); EX1003, ¶135. And as discussed above with respect to the embodiment illustrated in Figure 7, the analog comparison circuit comprising transistors 190"*i* and 192"*i* will output a well bias potential that is the lower of the two boosting stage input potentials. EX1006, 8:18-22 (“The bias signals WELL_1*i* and WELL_2*i* may ***bias*** the P-wells of the transistors 148"(i-1), 150"(i-1), 140"*i*, 142"*i*, 190"*i* and 192"*i* to the ***lower*** voltage VOUT_1 and VOUT_2 of the stage 110"(i-1) [*i.e.*, inputs to stage 110"*i*].”).

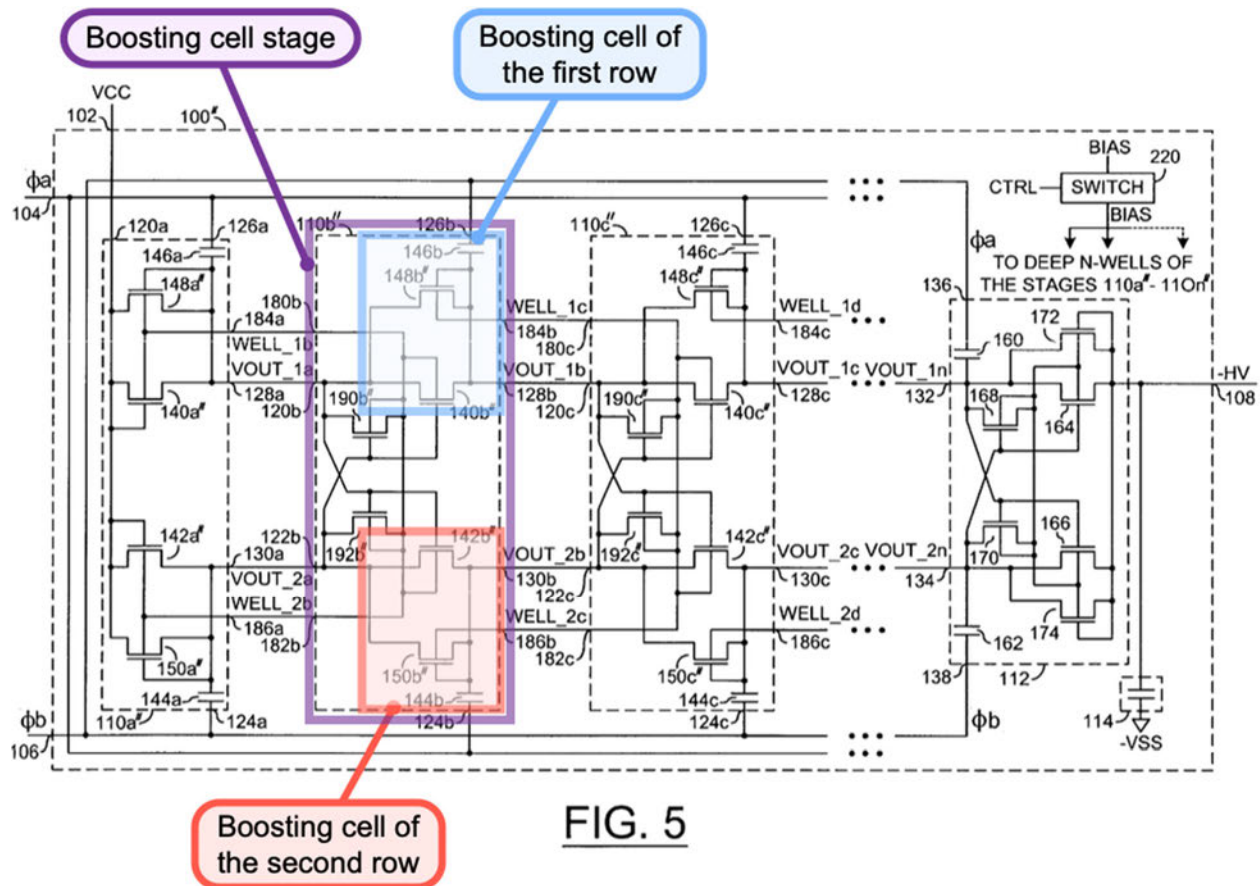


4. 1[c]: each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

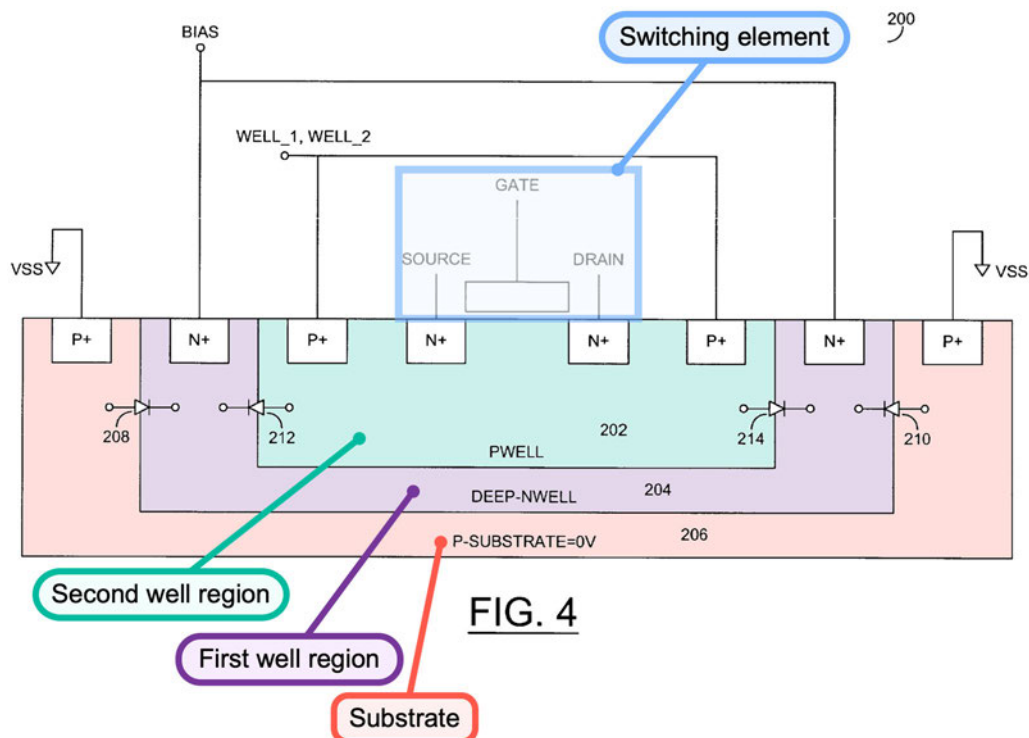
Meng discloses 1[c] for the reasons set forth in Ground 2. §VIII.B.4, *supra*.

Meng discloses an alternative embodiment in Figure 5 that “comprise[s] a number of circuits 110”a-110”n,” with each circuit representing a “stage” that comprises two “*boosting cells*.” EX1006, 7:49-52. As illustrated with annotations in Meng’s Figure 5 below, in the *i*-th *boosting cell stage* 110”*i*, the *top boosting cell* includes transistors 140”*i* and 148”*i* and capacitor 146”*i*, and the *bottom boosting cell* includes

transistors 142ⁱ and 150ⁱ and capacitor 144ⁱ. EX1006, Fig. 5, 7:63-65; EX1003, ¶136.



drain, in both “the first well region” (*i.e.*, DEEP-NWELL 204) and “the second well region” (*i.e.*, PWELL 202). EX1006, 7:5-10, Fig. 4. The source, gate, and drain form a transistor, which is a “switching element” because the transistor switches the channel between its source and drain on and off based on a change in the voltage at its gate. EX1003, ¶137.



Park also discloses 1[c]. Park discloses a booster circuit comprising a series of “pumping stages,” which are “boosting cells” because they output a voltage that is greater in magnitude than the input. EX1007, 5:37-45 (“[The booster circuit] includes a plurality of stages [*i.e.*, boosting cells] each having the same formation as represented by the first stage. The input to the first stage is the power supply voltage Vdd, and ... [t]he output of the final stage produces a voltage Vpp that has been

pumped up to a higher voltage than the power supply voltage.”); EX1003, ¶138. Park teaches that “[e]ach pumping stage is formed in its own P-well [*i.e.*, second-conductivity type second well region] and deep N-well [*i.e.*, first-conductivity type first well region].” EX1007, 5:22-25. Figure 9, shown below, provides a cross-sectional illustration of the switching elements of a boosting cell. EX1007, Fig. 9; EX1003, ¶138. According to Park, “[t]he MOS devices Mt and Ms [sic] [*i.e.*, Mt and Ms are switching elements of a boosting cell] are shown in a ***P-well*** within the ***deep N-well*** of a stage of the charge pump residing on a ***P-substrate***.” EX1007, 6:32-34.

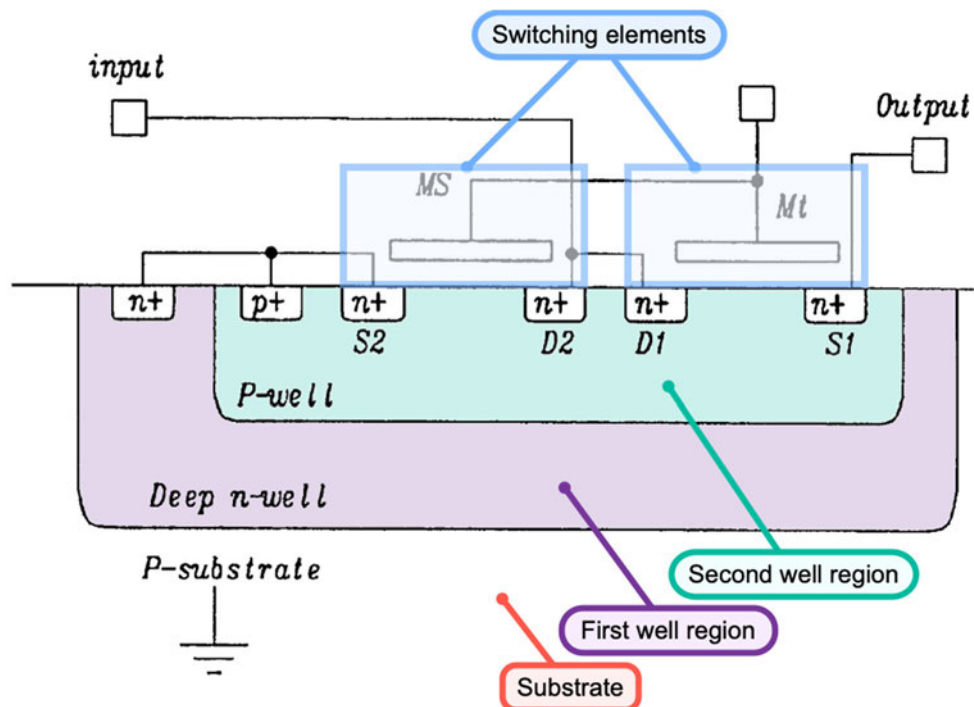


FIG. 9

5. 1[d]: the at least one switching element is configured to transfer charges from a first terminal to a second terminal, and

Meng discloses 1[d] for the reasons set forth in Ground 2. §VIII.B.5, *supra*.

Meng's alternative embodiment also discloses 1[d]. As discussed in 1[c], Meng's alternative embodiment illustrated in Figure 5 discloses switching elements in both "the first well region" (*i.e.*, DEEP-NWELL 204) and "the second well region" (*i.e.*, PWELL 202). EX1006, 7:5-10, Fig. 4; EX1003, ¶139. Also as discussed in 1[c], the "transistors [in Meng's alternative embodiment shown in Fig. 5] may be implemented as one or more deep N-well *NMOS transistors*," which transfer charges from a "first terminal" (*e.g.*, source) to a "second terminal" (*e.g.*, drain). EX1006, 7:58-61; EX1003, ¶139. For example, transistor 140***b*** ("a **switching element**") in Figure 5 shown below is designed to transfer charges from input node 120***b*** ("a **first terminal**") to output node 128***b*** ("a **second terminal**"). EX1006, Fig. 5.

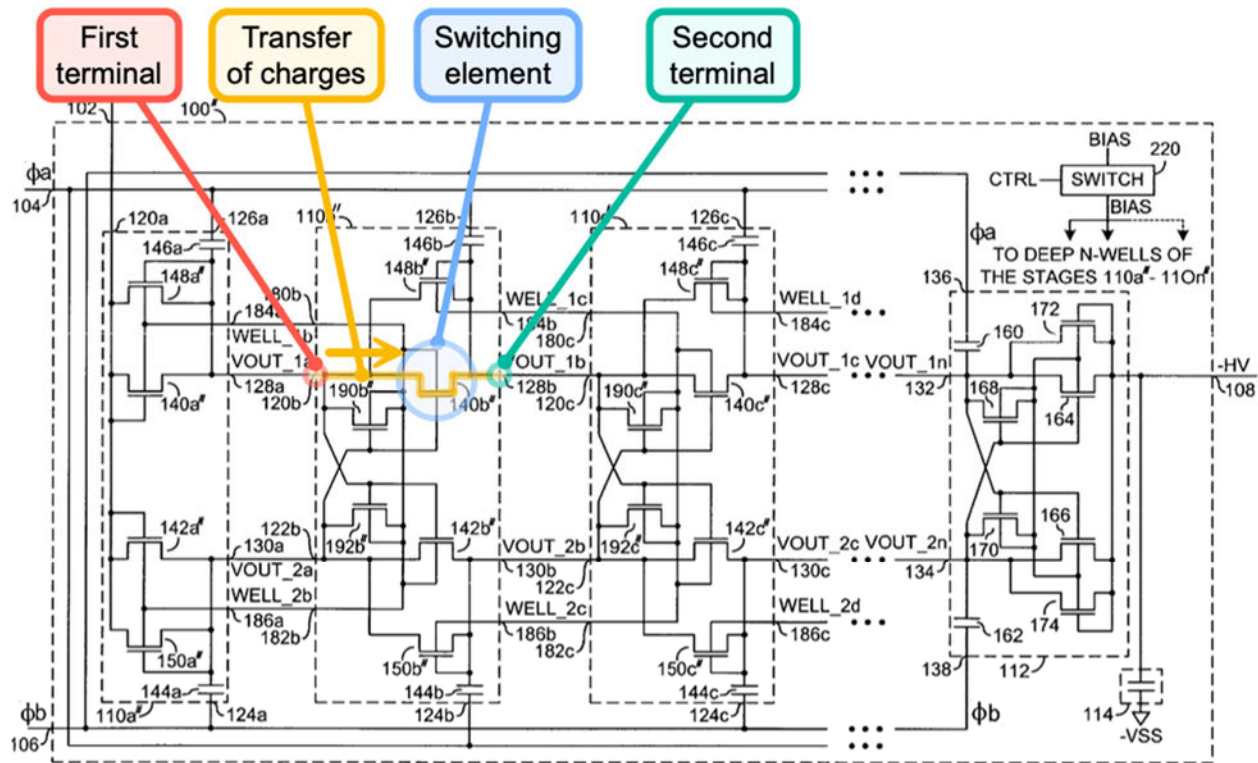


FIG. 5

Park also discloses 1[d]. As discussed in 1[c], Park discloses “MOS device[] Mt [*i.e.*, a switching element] ... shown [below in Figure 9 to be] ***in a P-well within the deep N-well*** of a stage of the charge pump residing on a P-substrate.” EX1007, 6:32-34; EX1003, ¶140.

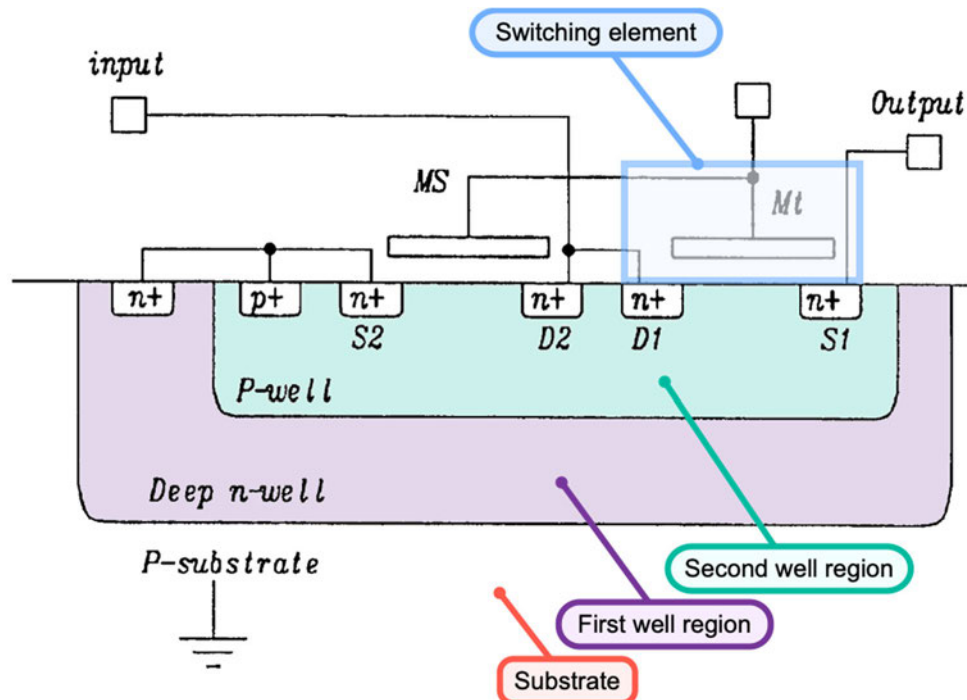


FIG. 9

Moreover, according to Park, the MOS device *Mt* is “a **charge transfer MOS device**” that transfers charges between a first and second terminal. EX1007, 5:27-33; EX1003, ¶141. The switching element *Mt* and its corresponding first and second terminals is shown below in Figure 9. EX1007, Fig. 9.

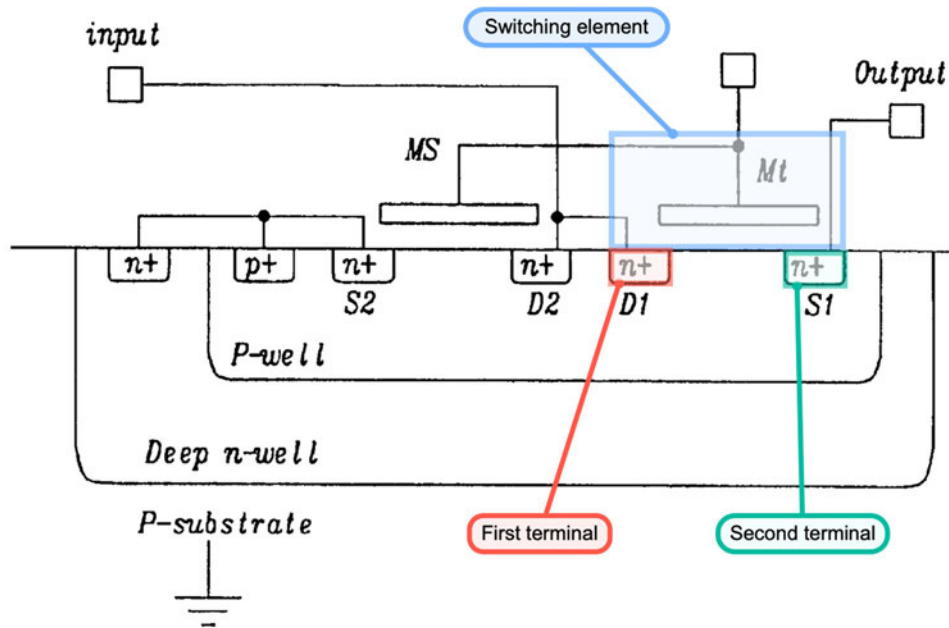


FIG. 9

6. 1[e]: the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

To the extent there is any argument that Meng does not disclose 1[e], it is rendered obvious by Meng in view of Park. Specifically, Meng, modified to apply the well bias potential outputted by the analog comparison circuit to the first well region as taught by Park, meets limitation 1[e]. EX1003, ¶142.

For the reasons set forth in 1[b], Meng discloses an analog comparison circuit that outputs a well bias potential. §IX.C.3, *supra*. Park teaches applying a well bias potential to the first well region (*i.e.*, deep N-well) of a boosting cell. EX1007, Figs. 7, 9, 6:38-40, 6:53-56. As illustrated with annotations in Figure 9 below, Park teaches that “[t]he source S2 [*i.e.*, node that outputs a well bias potential] of the

auxiliary MOSFET device Ms is *connected to both the P-well and the deep N-well* [i.e., second and first well regions, respectively].” EX1007, Fig. 9, 6:38-40; EX1003, ¶143.

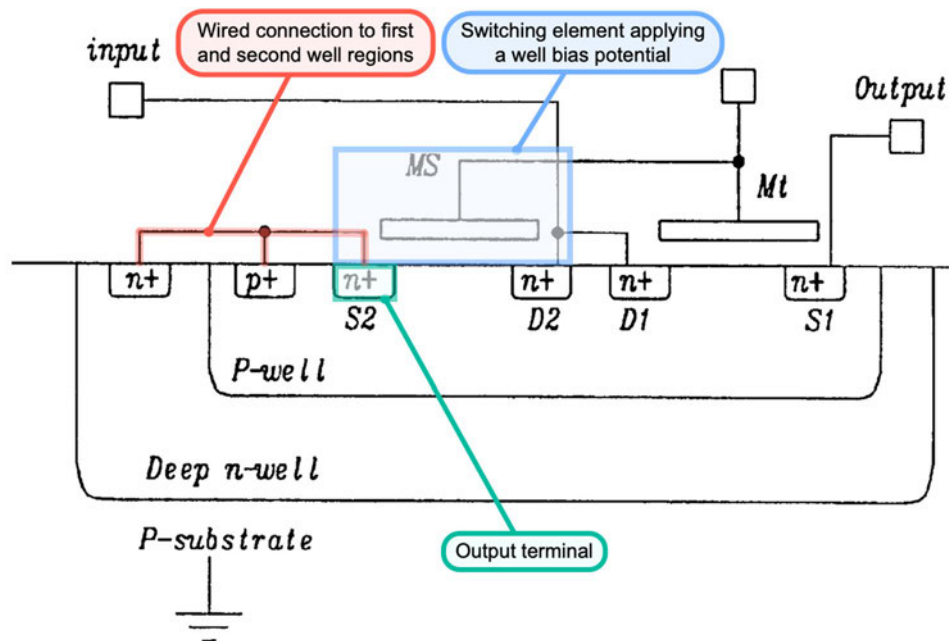
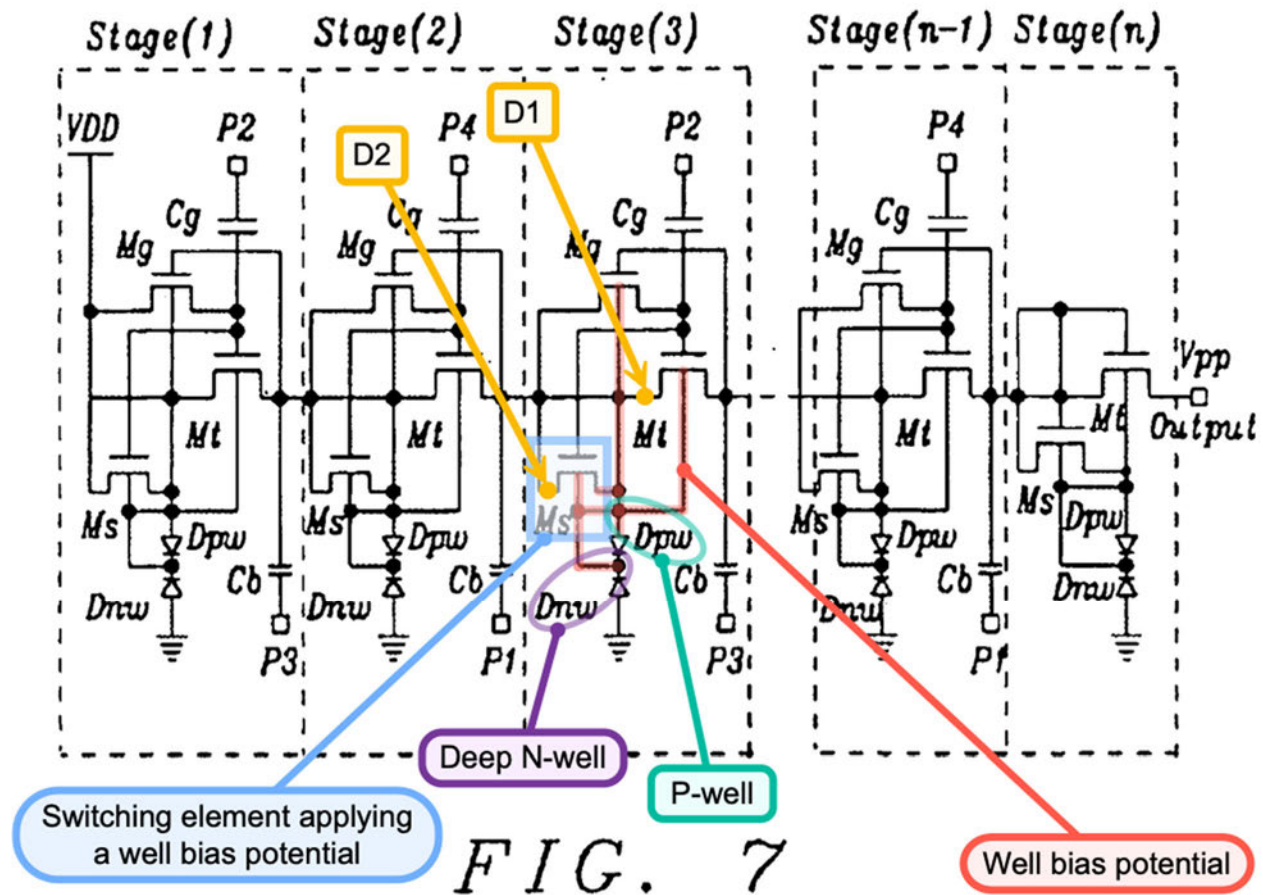


FIG. 9

Another view of Park’s teaching is presented below in Figure 7², which illustrates how “[t]he *input voltage* at the drains D1 and D2 *of* the charge transfer MOS device Mt and *the auxiliary MOS device Ms*, respectively, *is coupled to the*

² The node to the immediate upper left of the label “Mt” in Park’s Figure 7 is erroneously placed and should be removed. Park does not reference this erroneously placed node in its specification. Further, a POSITA would have understood that the inclusion of this erroneously placed node would result in the transistor Ms being turned off at all times and that its inclusion would render the circuit taught by Park unworkable. EX1003, ¶144.

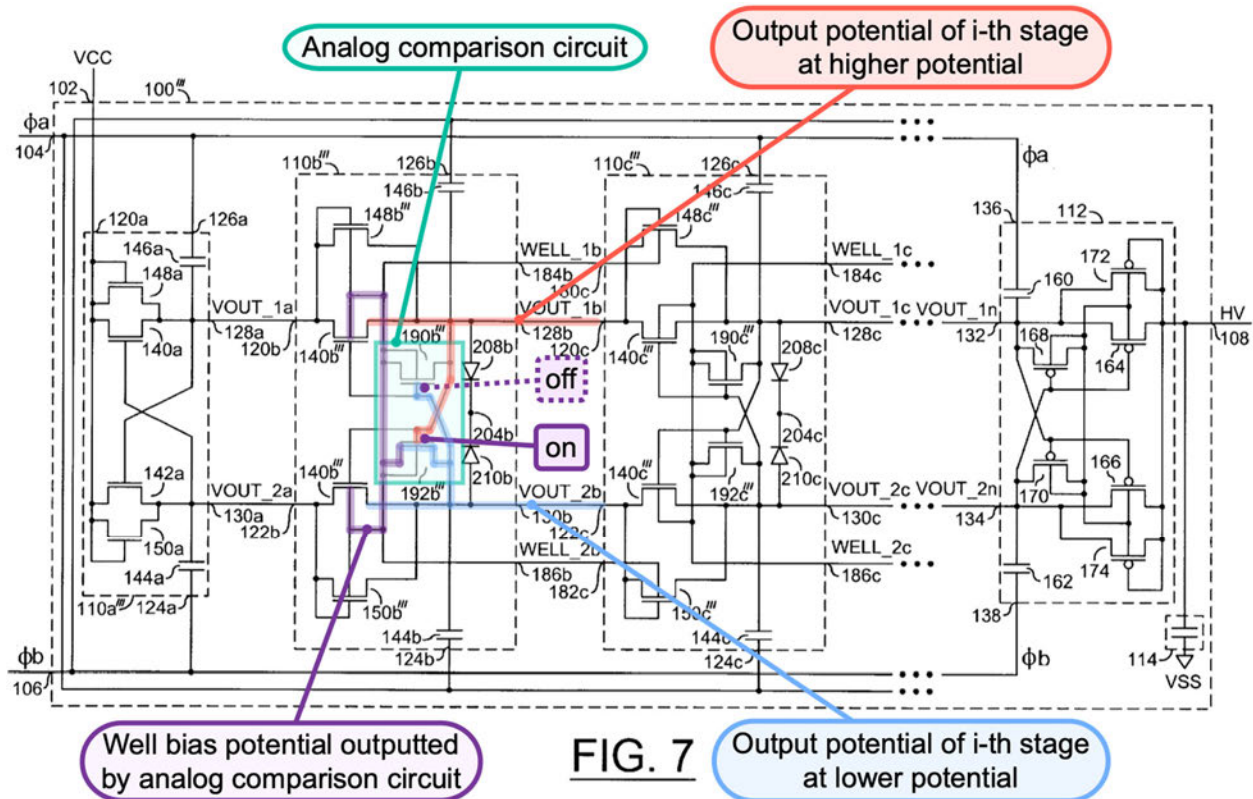
P-well and the deep N-well by the auxiliary MOS device *Ms*.” EX1007, Fig. 7, 6:53-56; EX1003, ¶144.

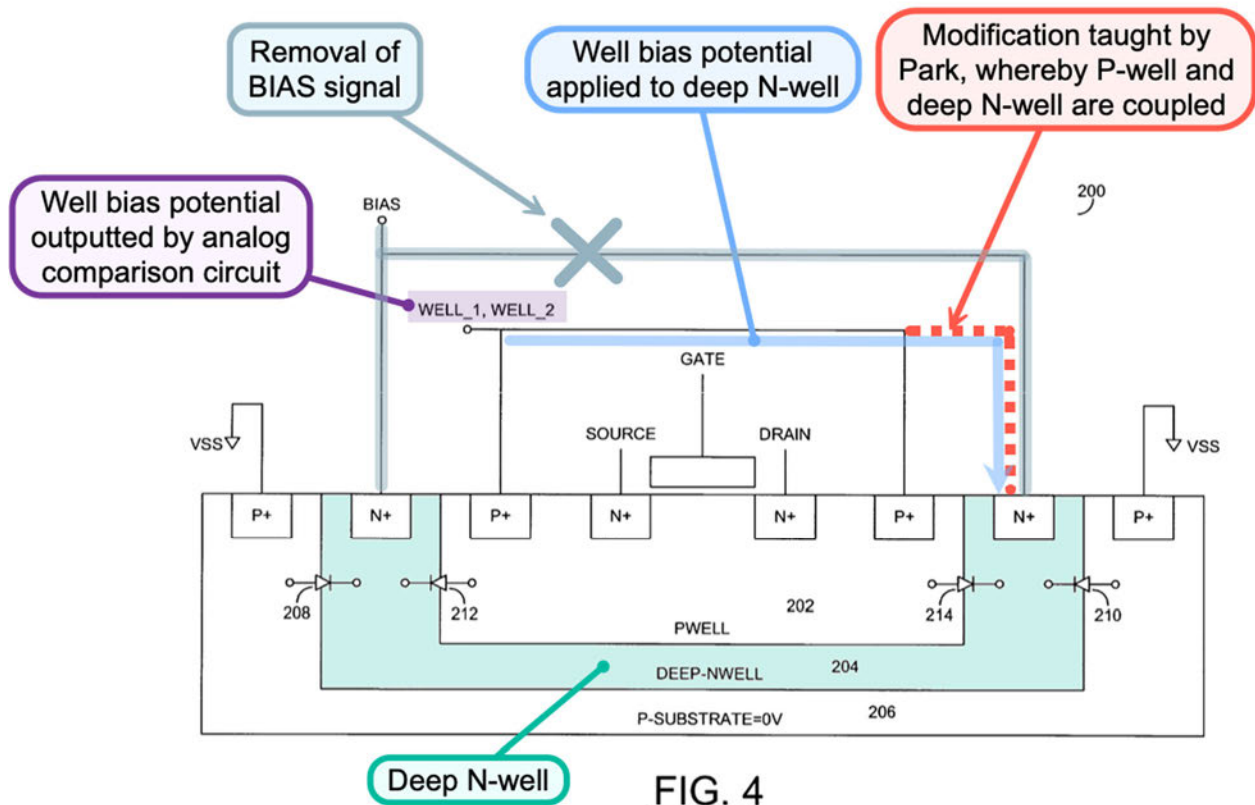


As discussed above in 1[b], Meng discloses two embodiments, illustrated in Figures 5 and 7, that include an analog comparison circuit that outputs a well bias potential generated by the lower of the two boosting stage potentials (*i.e.*, VOUT_{1i} or VOUT_{2i}). §IX.C.3, *supra*; EX1003, ¶145. As shown in Meng’s Figures 5 and 7 below, the well bias potential outputted by the analog comparison circuit is applied to the switching elements included in the *i*-th boosting cell of the first and second

¶145.





**D. Claims 2, 3, 9, and 10**

Meng discloses claims 2, 3, 9, and 10 for the reasons set forth in Ground 2.

§§VIII.C, VIII.D, VIII.E, VIII.F, *supra*.

E. Claim 4: The booster circuit of claim 1, wherein the well bias potential is the lower potential out of the input potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the input potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

As discussed in 1[b], Meng discloses an analog comparison circuit outputting a well bias potential that is the lower potential out of the input potentials of the i -th boosting cells of the first and second rows. §IX.C.3, *supra*.

- F. Claim 5: The booster circuit of claim 1, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.**

Meng in view of Park discloses claim 5. Meng discloses the booster circuit of claim 1. §IX.C, *supra*. Park discloses a **direct connection** between the second well region (*i.e.*, P-well) and the second terminal of the switching element, as shown below in Park's Figure 9. EX1007, Fig. 9; EX1003, ¶149. The direct connection between the first and second terminal via the switching element therefore enables a direct connection between the first terminal and the second well region such that they have the same potential. EX1003, ¶149.

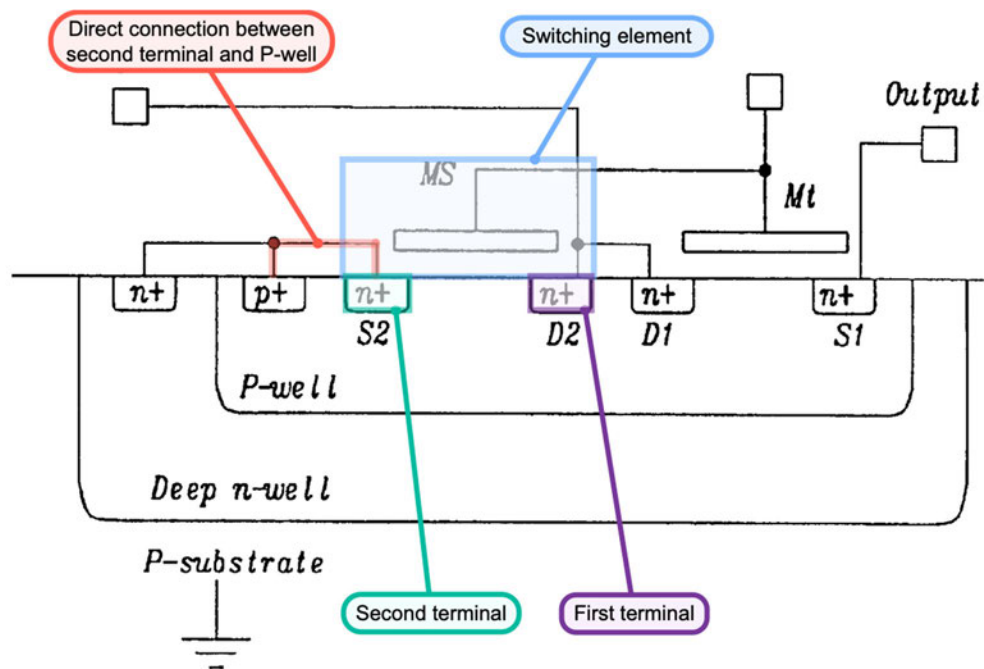


FIG. 9

- G. Claim 6: The booster circuit of claim 1, wherein the second well region and the first well region are connected to each other so that**

the second well region and the first well region have the same potential.

Meng in view of Park discloses claim 6. Meng discloses the booster circuit of claim 1. §IX.C, *supra*. Park discloses a **direct connection** between the first well region (*i.e.*, deep N-well) and the second well region (*i.e.*, P-well), as shown below in Park's Figure 9, so that the second well region and the first well region have the same potential. EX1007, Fig. 9; EX1003, ¶150.

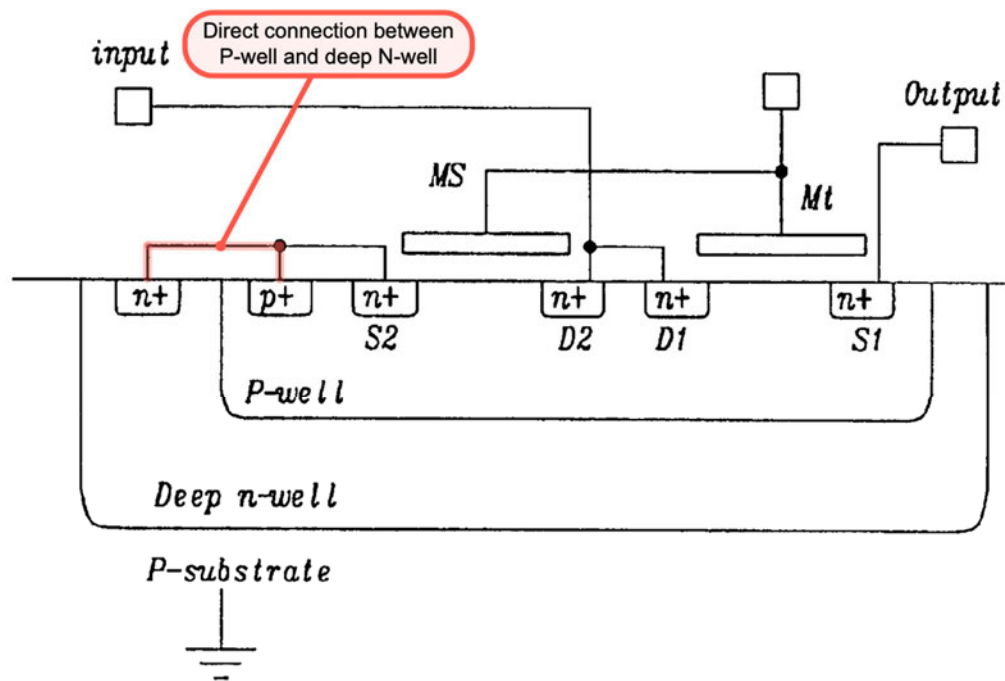


FIG. 9

H. Claim 7

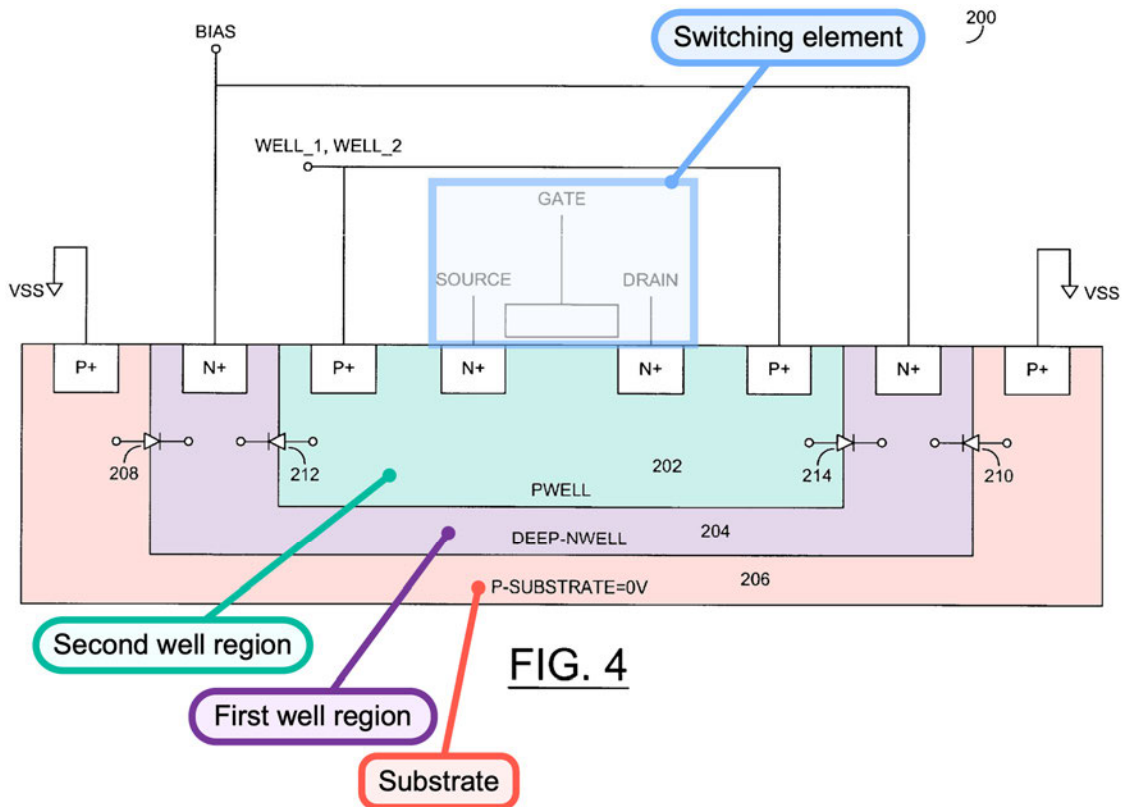
1. 7[pre]: The booster circuit of claim 1, wherein:

Both Meng and Park disclose 7[pre] as discussed in claim 1. §IX.C, *supra*.

2. 7[a]: the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-

**conductivity type second well region in the first well region,
and at least one switching element in the first well region or
the second well region, and**

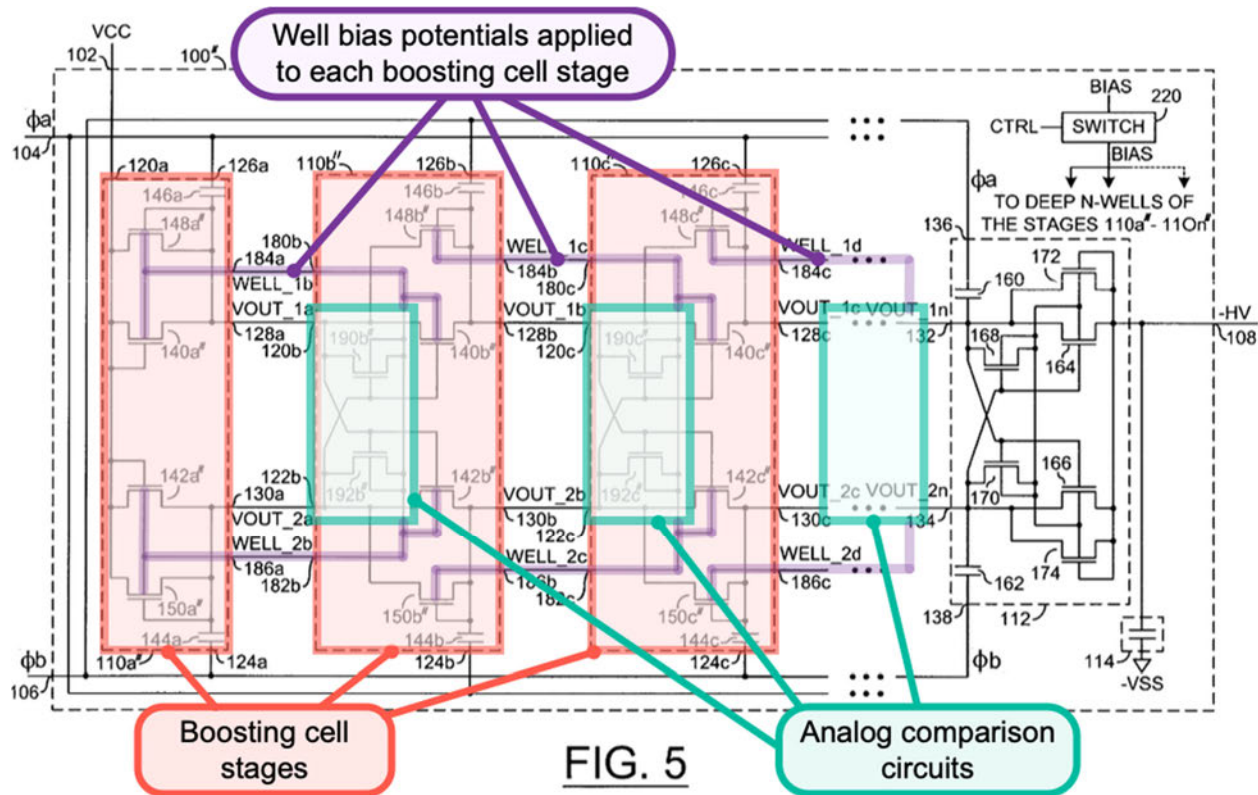
Meng discloses 7[a]. As discussed in 1[b], Meng discloses an analog comparison circuit comprising transistors 190*"i* and 192*"i*. §IX.C.3, *supra*; EX1006, Fig. 5; EX1003, ¶152. And according to Meng, the analog comparison circuit's transistors 190*"i* and 192*"i* “may be implemented as one or more *deep N-well* NMOS transistors as shown in FIG. 4.” EX1006, 7:58-61. The cross-section of a deep N-well NMOS transistor, shown below in Meng's Figure 4, confirms that the analog comparison circuit comprising the NMOS transistors 190*"i* and 192*"i* has “a P-well region 202 [*i.e.*, second-conductivity type second well region] ..., a deep N-well region 204 [*i.e.*, first-conductivity type first well region] ..., and a P-substrate region 206[.]” EX1006, Fig. 4, 7:5-10; EX1003, ¶152. Meng therefore discloses at least one analog comparison circuit that has a first well region on a substrate, a second well region in the first well region, and at least one switching element (*i.e.*, transistors 190*"i* and 192*"i*) in the first or second well regions. EX1003, ¶152.



3. 7[b]: the at least one analog comparison circuit is provided for each boosting cell stage in the first boosting cell row and the second boosting cell row.

Meng discloses 7[b]. As shown with annotations in Figure 5 below, Meng discloses a booster circuit that includes an **analog comparison circuit** that is provided for **each boosting cell stage** in the first and second boosting cell rows. EX1006, Fig. 5; *see also id.*, 8:16-18 (“Where a stage 110”*i* is any one of the stages 110”*b*-110”*n*, **at each [boosting cell] stage** 110”*i*, the bias signals WELL_1*i* and WELL_2*i* may be generated by the transistors 190”*i* and 192”*i* [*i.e.*, an **analog comparison circuit**]. The bias signals WELL_1*i* and WELL_2*i* may bias the P-wells of the transistors 148”(i-1), [and] 150”(i-1)[.]”); EX1003, ¶153. Meng teaches

each boosting cell stage receiving a well bias from the at least one analog comparison circuit. EX1006, Fig. 5; EX1003, ¶153.



I. Claim 8

1. 8[pre]: The booster circuit of claim 1, wherein:

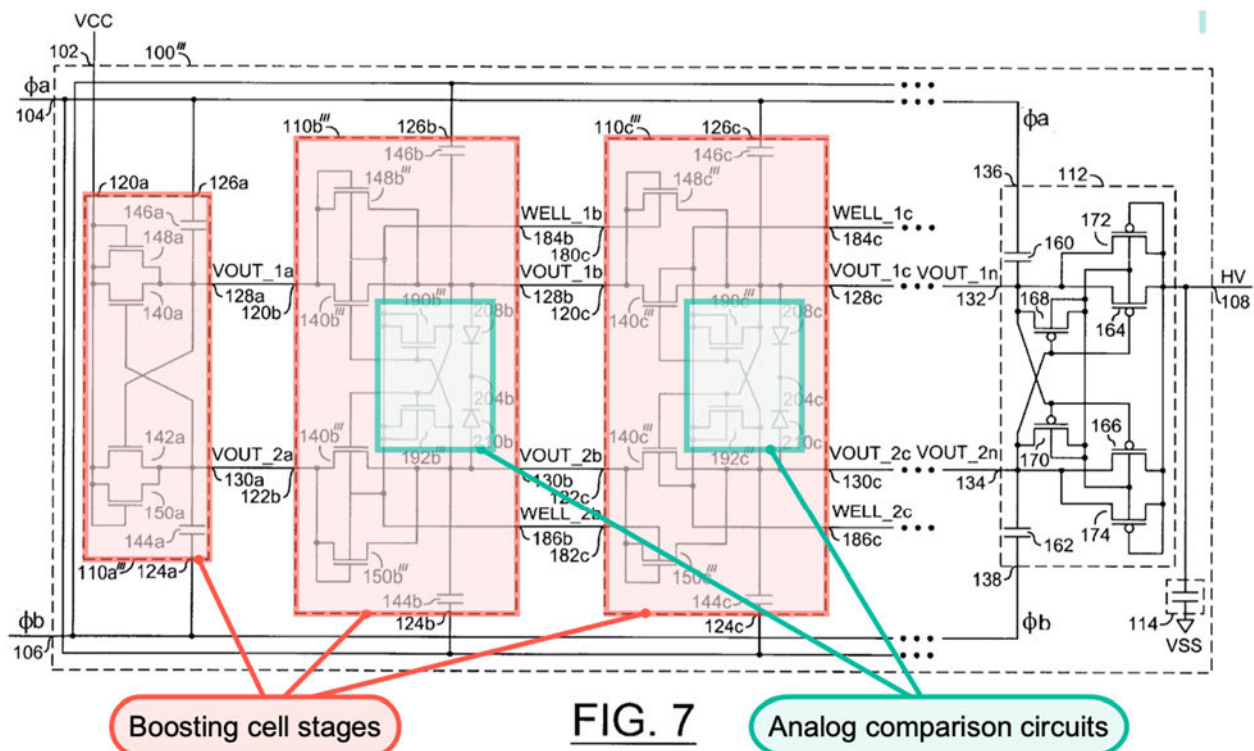
Both Meng and Park disclose 8[pre] as discussed in claim 1. §IX.C, *supra*.

2. 8[a]: the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

Meng discloses 8[a] as discussed in 7[a]. §IX.H.2, *supra*.

3. 8[b]: the at least one analog comparison circuit is provided for arbitrary number of boosting cell stages in the first boosting cell row and the second boosting cell row.

Meng discloses 8[b]. As shown with annotations in Figure 7 below, Meng discloses a booster circuit that includes two **analog comparison circuits** for at least three **boosting cell stages**, *i.e.*, an “arbitrary number of boosting cell stages.” EX1006, Fig. 7; EX1003, ¶156.



J. Claim 12

1. 12[pre]: A booster circuit comprising:

Both Meng and Park disclose 12[pre] as discussed in 1[pre]. §IX.C.1, *supra*.

2. **12[a]: a first boosting cell row including N stages ($N \geq 2$) of boosting cells; and a second boosting cell row including M stages ($M \geq 2$) of the boosting cells, wherein:**

Meng discloses 12[a] as discussed in 1[a]. §IX.C.2, *supra*.

3. **12[b]: each boosting cell includes a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,**

Meng discloses 12[b] as discussed in 1[c]. §IX.C.4, *supra*.

4. **12[c]: the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal,**

As discussed in 1[d], both Meng and Park disclose switching elements that transfer charges from a first terminal to a second terminal. §IX.C.5, *supra*. Switching elements, by definition, are capable of switching on and off in order to transfer or block charges between terminals on opposing sides of the switching element. EX1003, ¶160.

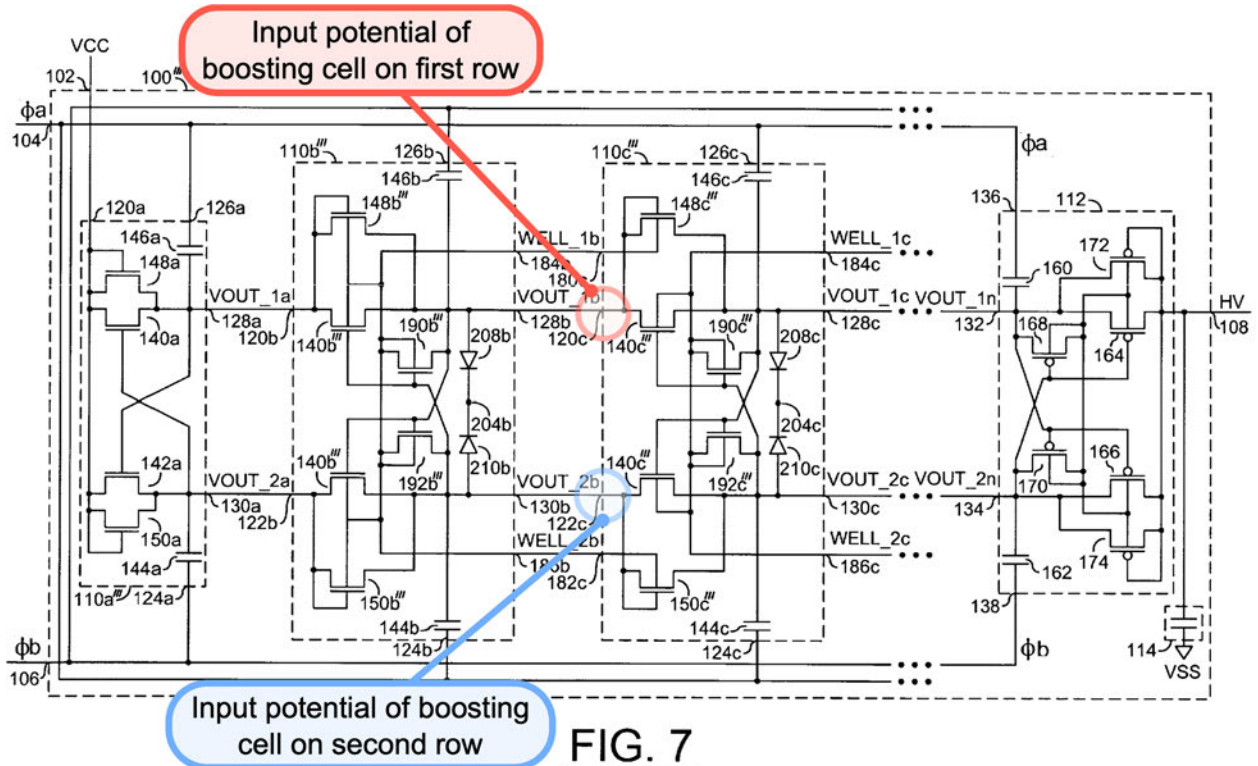
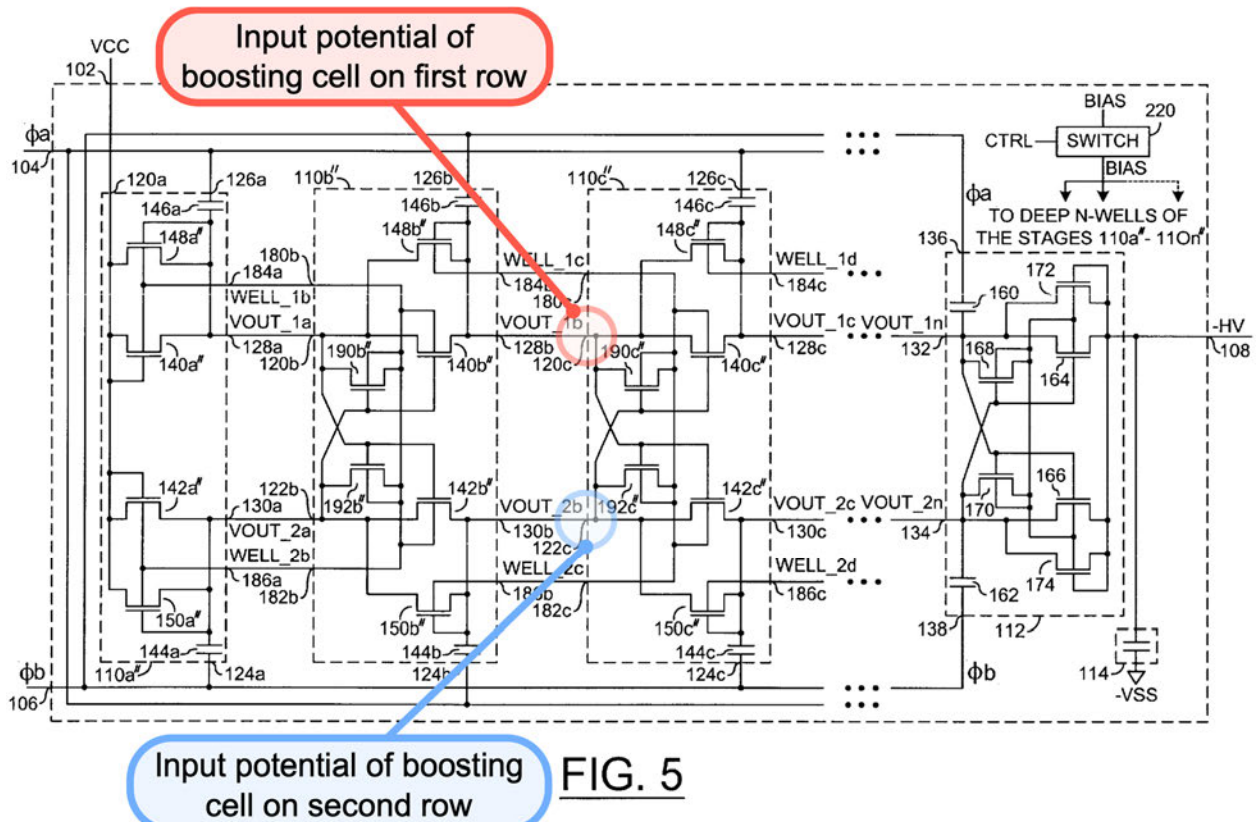
5. **12[d]: a potential of the first well region of the at least one switching element included in the boosting cells on a second stage or stages succeeding the second stage in the first and second boosting cell rows is controlled according to an input potential of the boosting cells of the first boosting cell row and an input potential of the boosting cells of the second boosting cell row, and**

As discussed in 1[b], Meng discloses an analog comparison circuit that outputs a well bias potential. §IX.C.3, *supra*. As discussed in 1[e], the well bias

potential outputted by the analog comparison circuit is applied to the deep N-well (*i.e.*, first well region) of the switching element(s) included in the boosting cell on a second stage, and on stages succeeding the second stage, in the first and second boosting cell rows. §IX.C.6, *supra*; EX1003, ¶161. And as discussed in 1[b] and 1[e], the operation of the analog comparison circuit, and by extension the generation of the well bias potential, is controlled according to the input potentials of the boosting cells of the first and second boosting cell rows. §§IX.C.3, IX.C.6, *supra*; EX1003, ¶161.

6. **12[e]: an input potential of each of the boosting cells of the first boosting cell row is different from an input potential of each of the boosting cells of the second boosting cell row.**

Meng discloses 12[e]. As shown below in Figures 5 and 7, Meng discloses, for each boosting cell of both the first and second boosting cell rows, a separate input potential; node 120*i* is the input potential of the boosting cell of the first boosting cell row and node 122*i* is the input potential of the boosting cell of the second boosting cell row. EX1006, Fig. 7; EX1003, ¶162. The input potentials represented by nodes 120*i* and 122*i* reflect two separate nodes and potentials, and are therefore *different* from one another. EX1003, ¶162.



X. MANDATORY DISCLOSURES

Pursuant to 37 C.F.R. § 42.8(a)(1), the following mandatory notices are provided as part of this Petition.

A. Standing

Petitioner certifies that it is not barred or estopped from requesting review of the Challenged Claims.

B. Real Party-In-Interest

The real party-in-interest for Petitioner is SK hynix Inc.

C. Related Matters

The '018 patent was asserted against Petitioner in *Advanced Memory Technologies, LLC v. SK hynix Inc.*, Case No. 2:24-cv-01078-JRG (E.D. Tex., filed Aug. 21, 2024).

D. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)) and Service Information (37 C.F.R. § 42.8(b)(3)-(4))

Petitioner provides the following counsel and service information. Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition. Petitioner agrees to accept electronic service at the email addresses listed below.

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E. Payment of Fees (37 C.F.R. § 42.15(a))

The undersigned authorizes the Office to charge the fee required for this Petition for *Inter Partes* Review to Deposit Account No. 50-5708. Any additional fees that might be due are also authorized.

XI. CONCLUSION

Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Date: August 29, 2025

Respectfully submitted,

By: /s/ James M. Glass

James M. Glass (Reg. No. 46729)

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CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 C.F.R. § 42.24, the undersigned hereby certifies that the word count for the foregoing Petition for *inter partes* review (excluding the table of contents, table of authorities, mandatory notices, certificate of service or word count, and appendix of exhibits or claim listing) totals 12,946 words, which is within the word limit allowed under 37 C.F.R. § 42.24(a)(i).

Date: August 29, 2025

By: /s/ James M. Glass
James M. Glass (Reg. No. 46729)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e), 42.105(a), the undersigned hereby certifies that a copy of this Petition and its respective exhibits were served via FedEx on the correspondence address of record below indicated in the U.S. Patent Office's Patent Center for U.S. Patent No. 7,920,018:

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SZYMON M. GURDA
Re U.S. Pat. No. 7,920,018
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