IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

ADVANCED MEMORY TECHNOLOGIES, LLC, Plaintiff, v. SK HYNIX INC., Defendant.	Case No. 2:24-CV-1078-JRG-RSP **JURY TRIAL DEMANDED**

DEFENDANT SK HYNIX'S PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to Local Patent Rules ("P. R.") 3-3 and 3-4, Defendant SK hynix Inc. ("SK hynix" or "Defendant") hereby serves its Invalidity Contentions, Subject Matter Eligibility Contentions, and accompanying document production on Plaintiff Advanced Memory Technologies, LLC ("AMT" or "Plaintiff"). Defendant contends that each of the claims asserted by AMT is invalid under at least 35 U.S.C. §§ 101, 102, 103, and/or 112.

I. GENERAL STATEMENT AND RESERVATION OF RIGHTS

A. General Reservation of Rights

These Contentions, along with the information and documents that Defendant produces herewith, are based on information currently available to Defendant and subject to further revision. Consistent with the Patent Rules, Defendant reserves the right to amend these Contentions should AMT: (1) provide any information that it failed to provide in its P. R. 3-1 and 3-2 disclosures or otherwise properly produce; (2) amend its P. R. 3-1 and 3-2 disclosures in any way; or (3) attempt to rely upon any information during claim construction proceedings, at trial, in a hearing, or during a deposition that it failed to provide in its P. R. 3-1 and 3-2 disclosures or otherwise properly produce. SK hynix further reserves the right to amend these contentions based on claim construction positions taken by AMT and/or construction of claim terms adopted by the Court. Moreover, Defendant further reserves the right to amend these contentions based on further discovery or Court rulings (or any other related reason). This includes, for instance, the issuance of subpoenas to third parties believed to have knowledge, documentation, and/or corroborating evidence concerning some of the prior art listed below and/or additional prior art. These third parties may include, without limitation, any relevant authors, inventors, developers, designers, corporate designees with knowledge, or assignees. SK hynix provides these Contentions, as well as the accompanying production of documents, for the sole purpose of complying with P. R. 3-3 and 3-4 and the Standing Order.

B. Asserted Claims

In this case, and based on AMT's P. R. 3-1 Disclosure of Asserted Claims and Infringement Contentions, served on April 2, 2025, AMT has asserted that SK hynix infringes the following claims ("Asserted Claims") of U.S. Patent Nos. 7,777,557 (the "'557 patent"), 7,920,018 (the "'018 patent"), 7,969,231 (the "'231 patent"), 8,593,888 (the "'888 patent"), and 8,400,835 (the "'835 patent") (collectively, the "Asserted Patents").

- '557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
- '018 patent: claims 1, 2, 4, 7, 9, and 10
- '231 patent: claims 1, 3, 4, 6, 7, and 8
- '888 patent: claims 1, 3, 5, 20, and 21
- '835 patent: claims 1, 2, 4 and 5

SK hynix's Invalidity and Subject Matter Eligibility Contentions address only those claims asserted in AMT's Infringement Contentions, and independent claims upon which these claims depend. To the extent that the Court or the Patent Rules permit AMT to assert additional claims against Defendant, Defendant reserves the right to disclose new or supplemental contentions regarding such claims.

C. AMT's P. R. 3-1 and 3-2 Disclosures

SK hynix provides these Contentions consistent with the schedule set forth in the Court's Second Amended Docket Control Order (Dkt. 27), but do so without waiving any right to receive from AMT full, complete and detailed infringement disclosures as required under P. R. 3-1 and 3-2. Defendant's compliance with the schedule currently in place should not be viewed as a waiver of its right to seek relief regarding the deficiencies in AMT's disclosures.

AMT's Infringement Contentions are deficient in numerous respects. AMT's Infringement Contentions lack the specificity required under P. R. 3-1 as would be necessary to fairly provide

Defendant notice of AMT's theories, including without limitation: (1) AMT fails to provide claim charts for each Accused Product; (2) AMT fails to support its assertions that there are no material differences between the Accused Products that affect its infringement theories for the uncharted products; (3) AMT fails to describe its claims with specificity or supporting documentary or declaratory evidence; (4) AMT accuses over 200 products but provides no more than nine total claim charts covering just four total products; and (2) AMT fails to identify where each element of each asserted claim is found within each Accused Product.

SK hynix further specifically reserves the right to modify, amend, or supplement its Contentions should AMT be permitted to further modify, amend, or supplement its P. R. 3-1 and 3-2 disclosures or produce documents responsive to SK hynix's discovery requests.

D. Priority Applications / Priority Date of Asserted Claims

SK hynix's Contentions, including but not limited to identification of prior art, rely in part on AMT's contention that the Asserted Patents are entitled to claim priority to the following applications:

- '557 patent: Japanese Patent Application No. 2007-007694, which has a priority date of January 17, 2007;
- '018 patent: claims Japanese Patent Application No. 2007-007694, which has a priority date of January 17, 2007;
- '231 patent: Japanese Patent Application No. 2008-179566, which has a priority date of July 9, 2008;
- '888 patent: Japanese Patent Application No. 2010-052722, which has a priority date of March 10, 2010;

- ’835 patent: Japanese Patent Application No. 2010-0521008-026211, which has a priority date of February 6, 2009.

SK hynix reserves the right to amend these Contentions to the extent that AMT is permitted to claim priority to an earlier application, assert an earlier conception or reduction to practice date than the priority application filing date, changes its alleged priority dates, or if the Court determines that any of the Asserted Patents are not entitled to claim priority to the earlier applications as asserted by AMT.

E. Claim Construction

Claim construction proceedings for this action have not yet occurred. Accordingly, SK hynix reserves the right to modify, amend, and/or supplement its Contentions in accordance with P. R. 3-6 following claim construction rulings from this Court, or to the extent permitted by this Court. SK hynix also reserves the right to modify, amend, and/or supplement its Contentions upon AMT’s alteration/clarification of any asserted claim constructions, including as adopted by AMT in its Infringement Contentions or any amendment thereto.

SK hynix’s Contentions are based in part on its present understanding of AMT’s Infringement Contentions. In some instances, AMT’s Infringement Contentions contradict the teachings of the Asserted Patents, contradict the meaning of the claim terms as would have been understood by a person of ordinary skill in the art, are internally inconsistent, and/or are vague and conclusory concerning how the claim limitations supposedly read on the Accused Products or activities. As a result, SK hynix is currently unable to fully discern AMT’s position regarding the construction of the patent claim limitations or terms. To the extent that AMT supplements or amends its Infringement Contentions, SK hynix reserves the right to modify, amend, and/or supplement these Contentions.

SK hynix's Contentions do not represent its agreement or view as to the meaning of any claim term contained therein. To the extent that SK hynix asserts that prior art is anticipatory or renders obvious claims based on the construction apparently applied by AMT to the Asserted Claims, SK hynix's Contentions are not—and should not be interpreted as—adoptions or admissions as to the accuracy of that scope or construction.

Nothing in SK hynix's Contentions should be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Nor should anything contained herein be understood or deemed to be an express or implied admission or contention with respect to the proper construction of any terms in any asserted claim, or with respect to the alleged infringement of that claim.

Unless otherwise stated herein, SK hynix takes no position on any matter of claim construction in these Contentions. SK hynix reserves the right to propose any claim construction it considers correct and to contest any claim construction it considers incorrect. SK hynix also reserves the right to argue that certain claim terms, phrases, and elements are indefinite, lack written description, are not enabled and/or are otherwise invalid under 35 U.S.C. § 112.

Because of the uncertainty of claim construction, SK hynix reserves the right to further supplement or modify the positions and information in these Contentions, including, without limitation, the prior art and grounds of invalidity set forth herein, after the Asserted Claims have been construed, in accordance with the Patent Rules and the Court's Orders.

F. Ongoing Discovery and Disclosures

Discovery in this case and SK hynix's investigation, including SK hynix's search for prior art, are ongoing. Some of the relevant prior art and other information is in the possession of third parties, and SK hynix is in the process of seeking discovery related to such prior art. For example, SK hynix intends to subpoena or otherwise seek discovery from third parties regarding at least the

Seiko Instruments Inc. S-24C02BMFN 2K EEPROM and prior art devices using Kilopass's technologies, in addition to other systems that may be related to the Asserted Patents and printed publication references disclosed in these contentions. SK hynix also intends to subpoena or otherwise seek discovery from Micron Technologies, Inc. concerning certain flash memory devices (including but not limited to MT28F008B3, MT28F800B3, and MT28F800B1WG-8B) that are prior art to the Asserted Patents. SK hynix expressly reserves the right to amend or modify these Contentions based on additional information obtained through continued formal discovery or other means pursuant to Fed. R. Civ. P. 26(e).

SK hynix further reserves the right to revise, amend, or supplement these Contentions, including by identifying, charting, and relying on additional information, references, systems, and devices, should SK hynix's further search and analysis yield additional information, references, systems, or devices, consistent with the Local Patent Rules and the Federal Rules of Civil Procedure. In addition, SK hynix reserves the right to supplement, amend, and/or alter the positions taken and information disclosed in these Contentions including, without limitation, the prior art and grounds of invalidity set forth herein under 35 U.S.C. §§ 101, 102, 103 or 112; to take into account information or defenses that may come to light as a result of SK hynix's discovery efforts; additional information obtained as to the priority date(s) of the asserted claim; testimony or documents produced by a party or non-party; and positions that AMT may take concerning infringement or invalidity issues. For example, SK hynix may seek further discovery from third parties believed to have knowledge, documentation, or corroborating evidence concerning prior art references, including prior art listed in the Exhibits hereto. Such third parties may include, without limitation, the authors, inventors, assignees, owners, or developers of the references and technologies listed in these disclosures. In particular, SK hynix reserves the right to assert

invalidity under pre-AIA 35 U.S.C § 102(c), (d), (f), or (g) for the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent to the extent that discovery or further investigation yields information forming the basis for such grounds for invalidity.

Defendant further reserve the right to rely upon prior art cited in the file histories of the Asserted Patents and related patent applications, including post-issuance proceedings, as invalidating references or to show the state of the art. Defendant further reserve the right to rely upon additional prior art to show the state of the art. Defendant further intend to rely on inventor admissions, and admissions by AMT and others providing testimony on behalf of AMT (*e.g.*, experts), concerning the scope of the prior art relevant to the Asserted Patents found in, *inter alia*: the patent prosecution history for the Asserted Patents and any related patents or patent applications, including post-issuance proceedings; any deposition testimony of the named inventors on the Asserted Patents; and the papers filed and any evidence submitted by AMT in connection with this litigation, prior litigations, and other proceedings involving the Asserted Patents. SK hynix incorporates by reference the relevant testimony of any fact witnesses who are deposed, provide declarations, or otherwise testify in this lawsuit. SK hynix also incorporate by references the reports and testimony of any expert witnesses regarding invalidity of the Asserted Patents, either here or at the Patent Trial and Appeals Board.

II. INVALIDITY CONTENTIONS

A. Invalidity Contentions Pursuant to P. R. 3-3(a)

Pursuant to P. R. 3-3(a), and as detailed below and in the attached Exhibits, SK hynix contends that the Asserted Claims of the Asserted Patents are invalid as anticipated and/or obvious, either expressly or inherently as understood by a person having ordinary skill in the art, under 35 U.S.C. §§ 102 and 103 over at least the following prior art. To the extent that any prior art listed herein is not identified as prior art that anticipates and/or renders obvious an Asserted Claim, SK

hynix intends to rely on the reference as background and as evidence of the state of the art at the time of AMT's alleged invention.

In addition to the references identified below, the prior art references and systems identified below, and the "References Cited" on the face of the Asserted Patents, may render obvious alone or in combination with any other reference cited herein the asserted claim of the Asserted Patents; provide background and context pertinent to the teachings and interpretation of the prior art referenced by the claim charts identified above; and may also be indicative of the relevant state of the art and/or the knowledge of one of ordinary skill in the art at the time of inventions of the Asserted Patents, such that it demonstrates, for example, the lack of invention between the asserted claim and the prior art as well as teachings, suggestions and motivations to combine. The prior art is exemplary only and is not in any way intended to limit the scope of what one of ordinary skill in the art would have understood at the time of the alleged invention.

Furthermore, along with the references disclosed in these contentions, the exhibits thereto, the Asserted Patents and their prosecution histories, and the common sense and understanding of those in the relevant field at the time of the alleged invention, invalidity may be demonstrated by the live testimony of relevant witnesses, who will be identified in accordance with the case schedule and as discovery in this matter proceeds. Such witnesses may be used, among other purposes, to discuss issues of prior art systems, prior art references, and the knowledge of one of ordinary skill in the art at the time of the alleged invention. As noted above, SK hynix intends to seek third-party discovery regarding certain prior art systems, in addition to other systems that may be related to the Asserted Patents and printed publication references disclosed in these contentions.

SK hynix reserves the right to rely upon additional prior art, information, testimony, and/or knowledge to demonstrate what one of ordinary skill in the art would have understood prior to the date of the alleged invention of the asserted claim of the Asserted Patents.

1. ’557 Patent Prior Art

Charted Prior Art Patents / Printed Publications				
Exhibit No. (Chart)	**Reference**	**Inventor Abbreviation**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
A-1	U.S. Pat. No. 6,501,325	Meng ’325	Jan. 18, 2001	Dec. 31, 2002
A-2	U.S. Pat. No. 7,382,177	Cordoba	Oct. 25, 2004	Apr. 27, 2006
A-3	U.S. Pat. No. 5,933,047	Zhu	Apr. 30, 1997	Aug. 3, 1999
A-4	U.S. Pat. No. 6,107,864	Fukushima	Feb. 1, 1999	Aug. 22, 2000
A-5	U.S. Pat. Pub. No. 2006/0061410	Chiu	Sep. 23, 2004	Mar. 23, 2006

Charted Prior Art Systems			
Exhibit No. (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
A-X1	The F90 Devices	2005	Hynix Semiconductor
A-X2	The F70 Devices	2006	Hynix Semiconductor

In addition, SK hynix reserves the right to rely upon at least the following additional prior art for obviousness combinations and/or to demonstrate the state of the art at the time of the alleged invention of the ’557 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. No. 6,100,557 (“Hung”)	Oct. 10, 1996	April 16, 1998
U.S. Pat. No. 6,952,129 (“Lin ’129”)	Jan. 12, 2004	Jul. 14, 2005
U.S. Pat. No. 6,121,821 (“Miki”)	Mar. 31, 1998	Sep. 19, 2000
U.S. Pat. No. 6,914,791 (“Park ’791”)	Nov. 6, 2002	Jul. 5, 2005
U.S. Pat. No. 6,175,264 (“Jinbo”)	Mar. 16, 1998	Jan. 16, 2001

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
VLSI-Design of Non-Volatile Memories (Campardo, Micheloni, Novosel) ("Campardo")	-	2005

2. '018 Patent Prior Art

Charted Prior Art Patents / Printed Publications				
Exhibit No. (Chart)	**Reference**	**Inventor Abbreviation**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
B-1	U.S. Pat. No. 6,501,325	Meng '325	Jan. 18, 2001	Dec. 31, 2002
B-2	U.S. Pat. No. 7,382,177	Cordoba	Oct. 25, 2004	Apr. 27, 2006
B-3	U.S. Pat. No. 5,933,047	Zhu	Apr. 30, 1997	Aug. 3, 1999
B-4	U.S. Pat. No. 6,107,864	Fukushima	Feb. 1, 1999	Aug. 22, 2000
B-5	U.S. Pat. Pub. No. 2006/0061410	Chiu	Sep. 23, 2004	Mar. 23, 2006

Charted Prior Art Systems			
Exhibit No. (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
B-X1	The F90 Devices	2005	Hynix Semiconductor
B-X2	The F70 Devices	2006	Hynix Semiconductor

In addition, SK hynix reserves the right to rely upon at least the following additional prior art for obviousness combinations and/or to demonstrate the state of the art at the time of the alleged invention of the '018 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. No. 6,100,557 ("Hung")	Oct. 10, 1996	April 16, 1998
U.S. Pat. No. 6,952,129 ("Lin '129")	Jan. 12, 2004	Jul. 14, 2005
U.S. Pat. No. 6,121,821 ("Miki")	Mar. 31, 1998	Sep. 19, 2000
U.S. Pat. No. 6,914,791 ("Park '791")	Nov. 6, 2002	Jul. 5, 2005
U.S. Pat. No. 6,175,264 ("Jinbo")	Mar. 16, 1998	Jan. 16, 2001

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
VLSI-Design of Non-Volatile Memories (Campardo, Micheloni, Novosel) ("Campardo")	-	2005

3. '231 Patent Prior Art

Charted Prior Art Patents / Printed Publications				
Exhibit No. (Chart)	**Reference**	**Inventor Abbreviation**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
C-1	U.S. Pat. No. 7,099,167	Fujise	Nov. 21, 2003	Aug. 29, 2006
C-2	U.S. Pat. No. 6,836,177	Ito-177	Jan. 13, 2003	Dec. 28, 2004
C-3	U.S. Pat. No. 6,473,321	Kishimoto	Jun. 19, 2001	Oct. 29, 2002
C-4	U.S. Pat. No. 5,941,990	Hiiragizawa	Oct. 29, 1996	Aug. 24, 1999
C-5	U.S. Pat. No. 8,102,157	Abe	May 16, 2008	Jan. 24, 2012
C-6	U.S. Pat. No. 6,230,280	Okasaka	Jan. 22, 1999	May 8, 2001
C-7	U.S. Pat. No. 6,080,205	Oshikawa	Dec. 22, 1997	Jun. 27, 2000
C-8	U.S. Pat. Appl. Pub. No. 2003/000823	Dohi	Nov. 16, 2001	Jan. 9, 2003
C-9	U.S. Pat. Appl. Pub. No. 2002/0006063	Sato	Jun. 19, 2001	Jan. 17, 2002
C-10	U.S. Pat. Appl. Pub. No. 2009/0174441	Gebara	Jan. 8, 2008	Jul. 9, 2009
C-11	U.S. Pat. Appl. Pub. No. 2001/0026187	Oku	Mar. 1, 2001	Oct. 4, 2001

Charted Prior Art Systems			
Exhibit No. (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
C-X1	SK hynix Nova	At least by 2006	SK hynix

In addition, SK hynix reserves the right to rely upon at least the following additional prior art for obviousness combinations and/or to demonstrate the state of the art at the time of the alleged invention of the '231 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. No. 5,179,535 (Nakayama)	Feb. 20, 1992	Jan. 12, 1993
U.S. Pat. No. 5,436,587 (Cernea)	Nov. 24, 1993	Jul. 25, 1995
U.S. Pat. No. 6,791,918 (Tanishima)	Nov. 22, 2000	Sep. 14, 2004
U.S. Pat. No. 5,365,121 (Morton)	Mar. 8, 1993	Nov. 15, 1994
U.S. Pat. No. 6,333,873 (Kumanoya)	Sep. 29, 1997	Dec. 25, 2001
U.S. Pat. No. 7,098,725 (Lee)	Jun. 24, 2004	Aug. 29, 2006
U.S. Pat. No. 6,249,455 (Kim)	Dec. 22, 1999	Jun. 19, 2001
U.S. Pat. No. 5,801,987 (Dinh)	Mar. 17, 1997	Sep. 1, 1998
U.S. Pat. Appl. Pub. No. 2007/0164811 (Crippa)	Jul. 27, 2006	Jul. 19, 2007
U.S. Pat. Appl. Pub. No. 2008/0123417 (Byeon)	Nov. 29, 2006	May 29, 2008
U.S. Pat. Appl. Pub. No. 2008/0205134 (Kato)	Feb. 1, 2008	Aug. 28, 2008
U.S. Pat. Appl. Pub. No. 2008/0018384 (Kim)	Jun. 27, 2007	Jan. 24, 2008
U.S. Pat. Appl. Pub. No. 2008/0136388 (Senda)	Oct. 31, 2007	Jun. 12, 2008
U.S. Pat. Appl. Pub. No. 2007/0133729 (Hsiao)	Feb. 28, 2006	Jun. 14, 2007
U.S. Pat. Appl. Pub. No. 2002/0008558 (Okuda)	Jul. 20, 2001	Jan. 24, 2002
U.S. Pat. Appl. Pub. No. 2008/0137428 (Nakai)	Nov. 14, 2007	Jun. 12, 2008
Chinese Pat. Appl. Pub. No. CN 101127479A (Wu)	Aug. 16, 2006	Feb. 20, 2008
Chinese Pat. Appl. Pub. No. CN 101154440A (Jiang)	Dec. 31, 2006	Apr. 2, 2008
Japanese Pat. Appl. Pub. No. JP 2008-112440A (Saito)	Oct. 1, 2007	May 15, 2008
Japanese Pat. Appl. Pub. No. JP 2003-219633A (Ito-633)	Jan. 17, 2002	Jul. 31, 2003
Japanese Pat. Appl. Pub. No. JP 2007-244164A (Shindo)	Mar. 13, 2006	Sep. 20, 2007
A programmable CMOS decimator for sigma-delta analog-to-digital converter and charge pump circuits (Anantha)	-	May 2005

4. ’888 Patent Prior Art

Charted Prior Art Patents / Printed Publications				
Exhibit No. (Chart)	**Reference**	**Inventor Abbreviation**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
D-1	JP Pat. Appl. Pub. No. 2008-217914A	Nakauchi	Mar. 6, 2007	Sep. 18, 2008
D-2	U.S. Pat. No. 5,907,505	Tomita	Sep. 29, 1997	May 25, 1999
D-3	U.S. Pat. No. 7,372,747	Nam	Jul. 7, 2006	May 13, 2008
D-4	CN Pat. Appl. Pub. No. CN 101303893A	Lin		Nov. 12, 2008
D-5	EP 2 302 635A1	Lo Giudice	Sep. 18, 2009	Mar. 30, 2011
D-6	A 5-V-Only One-Transistor 256K EEPROM with Page-Mode Erase	Nakayama	n/a	Aug. 1989

Charted Prior Art Systems			
Exhibit No. (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
D-X1	Seiko Devices (*e.g.*, S-24C02BMFN)	2003	Seiko Instruments
D-X2	XPM	2003	Kilopass
D-X3	Micron Technologies Flash Memory Devices (*e.g.*, MT28F008B3, MT28F800B3, and MT28F800B1WG-8B)	1998	Micron Technologies, Inc.

In addition, SK hynix reserves the right to rely upon at least the following additional prior art for obviousness combinations and/or to demonstrate the state of the art at the time of the alleged invention of the ’888 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. No. 6,842,383 (Shor)	Jan. 30, 2003	Jan. 11, 2005
U.S. Pat. No. 8,116,132 (Im)	Jan. 5, 2009	Feb. 14, 2012
U.S. Pat. No. 7,512,010 (Cho)	Jun. 11, 2007	Mar. 31, 2009
U.S. Pat. No. 5,812,445 (Yamauchi)	Mar. 27, 1997	Sep. 22, 1998
U.S. Pat. No. 6,128,242 (Banba)	Feb. 26, 1998	Oct. 3, 2000
U.S. Pat. Appl. Pub. No. US 2005/0219903 (Daga)	Feb. 18, 2005	Oct. 6, 2005
U.S. Pat. Appl. Pub. No. US 2006/0055452 (Tanzawa-452)	Nov. 9, 2005	Mar. 16, 2006
U.S. Pat. Appl. Pub. No. US 2003/0151945 (Tanzawa-945)	Dec. 26, 2002	Aug. 14, 2003
U.S. Pat. Appl. Pub. No. US 2002/0003724 (Tanzawa-724)	May 25, 2001	Jan. 10, 2002
U.S. Pat. Appl. Pub. No. US 2009/0296497 (Hirabayashi)	May 5, 2009	Dec. 3, 2009
U.S. Pat. Appl. Pub. No. US 2005/0232013 (Kawai)	Mar. 16, 2005	Oct. 20, 2005
U.S. Pat. Appl. Pub. No. US 2003/0145154 (Barnett)	Feb. 28, 2003	Jul. 31, 2003
U.S. Pat. Appl. Pub. No. US 2007/0201283 (O)	Jan. 12, 2007	Aug. 30, 2007
U.S. Pat. Appl. Pub. No. US2008/0237587 (Nierle)	Mar. 30, 2007	Oct. 2, 2008
JP Pat. Appl. Pub. No. JP 2006-172630A (Shibata)	Dec. 16, 2004	Jun. 29, 2006
Ultra-Low-Power Flash Memory in Standard 0.35 um CMOS for Passive Microwave RFID Transponders (De Vita)	-	2006
An EEPROM Programming Controller for Passive UHF RFID Transponders with Gated Clock Regulation Loop and Current Surge Control (Barnett-2007)	-	2007
An EEPROM Programming Controller for Passive UHF RFID Transponders with Gated Clock Regulation Loop and Current Surge Control (Barnett-2008)	-	2008

5. ’835 Patent Prior Art

Charted Prior Art Patents / Printed Publications				
Exhibit No. (Chart)	**Reference**	**Inventor Abbreviation**	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
E-1	JP Pat. Pub. No. JPH06150670A	Murakami	February 6, 1992	May 31, 1994
E-2	U.S. Pat. Pub. No. 2006/0133162A1	Wang ’162	December 22, 2004	June 22, 2006
E-3	U.S. Pat. Pub. No. 2008/0192545A1	Chen	February 13, 2007	August 14, 2008
E-4	U.S. Pat. Pub. No. 2004/0208055A1	Wang ’055	March 9, 2004	October 21, 2004
E-5	JP Pat. Pub. No. JPH0562484A	Kobayashi	September 6, 1991	March 12, 1993
E-6	U.S. Pat. Pub No. 2002/0122334A1	Lee	November 26, 2001	September 5, 2003
E-7	U.S. Pat. Pub. No. 2004/0008567A1	Furuyama	February 21, 2003	January 15, 2004
E-8	U.S. Pat. Pub. No. 2007/0058429A1	Umezawa	September 8, 2006	March 15, 2007

Charted Prior Art Systems			
Exhibit No. (Chart)	**Item Offered for Sale or Publicly Used or Known**	**Date of Offer or Use or Information Was Known**	**Identity of Person/Entity and Abbreviation**
E-X1	XPM	2003	Kilopass
E-X2	Micron Technologies Flash Memory Devices (*e.g.*, MT28F008B3, MT28F800B3, and MT28F800B1WG-8B)	1998	Micron Technologies, Inc.

In addition, SK hynix reserves the right to rely upon at least the following additional prior art for obviousness combinations and/or to demonstrate the state of the art at the time of the alleged invention of the ’835 patent.

Additional Prior Art		
Reference	**Filing Date**	**Date of Issuance or Publication or Public Use / Availability**
U.S. Pat. Pub. No. 2009/0116288A1 ("Varkony")	November 7, 2008	May 7, 2009
U.S. Pat. No. 5,430,674 ("Javanifard")	June 2, 1994	July 4, 1995
U.S. Pat. No. 5,751,637 ("Chen '637")	March 12, 1996	May 12, 1998
U.S. Pat. Pub. No. 2007/0263449A1 ("Yu")	May 15, 2006	November 15, 2006
U.S. Pat. No. 5,257,225 ("Lee '225")	March 12, 1992	October 26, 1993
U.S. Pat. No. 6,510,085 ("Fastow")	May 18, 2001	January 21, 2003
U.S. Pat. No. 5,230,058 ("Kumar")	May 8, 1990	July 20, 1993

B. Invalidity Contentions Pursuant To P. R. 3-3(b)-(c)

Subject to SK hynix's reservations of rights, and with respect to each asserted claim of AMT's Infringement Contentions, SK hynix provides the following information required by P. R. 3-3(b) and (c).

1. Claim Charts

As set forth in Exhibits A-1 through A-X; B-1 through B-X; C-1 through C-X; D-1 through D-X; and E-1 through E-X, and below, each of the charted references, and any products, devices, or processes used in the prior art that embody the subject matter disclosed in the references, invalidates one or more Asserted Claims of the Asserted Patents. To the extent any Exhibit concerns or refers to the operation, function, structure, or use of a product, system, or method, SK hynix's contentions are based on information and belief.

While SK hynix has identified at least one citation per element or limitation for each reference identified in the attached Exhibits, each and every disclosure of the same element or limitation in the same reference is not necessarily identified. In an effort to focus the issues, SK hynix cites exemplary relevant portions of identified references, even where a reference may contain additional disclosure for a particular claim element or limitation, and reserves all rights to rely on other portions of the identified references to support its claims and/or defenses. Any

reference to a figure in cited text incorporates by reference the figure itself, and any citation to a figure incorporates by reference any description of that figure in a reference. Similarly, any reference to a cited part or portion of a document encompasses all figures and text within the cited page or portion. Additionally, many of the prior art references are related to, or counterparts of, patent applications and issued patents that contain substantially the same subject matter (*e.g.*, published U.S. patent applications, issued U.S. patents, and foreign applications or issued patents). Any citation to or quotation from any of these patent applications or patents, therefore, should be understood as encompassing any parallel citation to the same subject matter in other related or corresponding applications or patents. Supporting citations in the Invalidity Charts are representative and do not necessarily represent every location where a particular claim element may be found in the prior art reference. SK hynix reserves the right to rely on additional, or different, portions of the prior art other than those specifically cited, and to supplement and/or amend these Invalidity Charts.

As noted above, these Invalidity Charts are based on SK hynix's understanding of the claim constructions applied by AMT, even though SK hynix does not necessarily agree with those constructions and reserves the right to dispute them. To the extent any limitation is deemed not to be met exactly by a prior art reference, SK hynix contends that the difference would have been obvious to a person of ordinary skill in the art and within the knowledge of one skilled in the art at the time of the alleged invention, so that the claimed invention would have been obvious both in light of the single reference alone and/or in light of combined references. SK hynix does not admit or concede that the element is not expressly or inherently disclosed by the reference at issue.

Much of the art identified in the attached Invalidity Charts reflects common knowledge and the state of the art at the time of the earliest filing date of the Asserted Patents. SK hynix may

rely on additional citations, references, expert testimony, fact testimony and other corroborating evidence, and other material to provide context and background illustrating the knowledge of a person of ordinary skill in the art at the time of the claimed inventions and/or to aid in understanding the cited portions of the references and/or cited features of the systems. SK hynix may also rely on expert testimony explaining relevant portions of references, relevant hardware or software products or systems, and other discovery regarding these subject matters. Additionally, SK hynix may rely on other portions of any prior art reference, whether or not identified in the Invalidity Charts, particularly those produced in SK hynix's accompanying production, for purposes of explaining the background, general technical subject area, and the knowledge of a person of ordinary skill in the art. In addition, SK hynix may rely on all portions of the prior art references that are identified in petitions for *inter partes* review or reexamination for the Asserted Patents and/or related patents, as well as any obviousness combinations identified in those documents.

2. Anticipation and Single Reference Obviousness

As set forth in the attached Exhibits and below, the following references anticipate one or more of the Asserted Claims of the Asserted Patents by expressly or inherently disclosing each and every limitation of that claim. To the extent AMT contends that any of these references do not expressly or inherently disclose any limitation of any claim, they nevertheless anticipate because a POSITA would at once envisage the claimed arrangement or combination of claim elements. To the extent that AMT contends that any of these references do not anticipate any asserted claim, SK hynix further contends each reference renders the asserted claim obvious either in view of the reference alone or in combination with other references and/or the knowledge of a person of ordinary skill in the art. A corresponding claim chart for each reference is attached hereto as indicated in the "Exhibit No." column.

Exhibit No.	Prior Art Reference[1]	Patents and Claims
A-1	Meng ’325	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-2	Cordoba	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-3	Zhu	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-4	Fukushima	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-5	Chiu	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-X1	F90 Devices	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
A-X2	F70 Devices	’557 patent: claims 1, 2, 4, 7, 9, 10, 11, 12, and 14
B-1	Meng ’325	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-2	Cordoba	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-3	Zhu	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-4	Fukushima	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-5	Chiu	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-X1	F90 Devices	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-X2	F70 Devices	’018 patent: claims 1, 2, 4, 7, 9, and 10
B-6	Chiu	’018 patent: claims 1, 2, 4, 7, 9, and 10
C-1	Fujise	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-2	Ito-177	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-3	Kishimoto	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-4	Hiiragizawa	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-5	Abe	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-6	Okasaka	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-7	Oshikawa	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-8	Dohi	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-9	Sato	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-10	Gebara	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-11	Oku	’231 patent: claims 1, 3, 4, 6, 7 and 8
C-X1	SK hynix Nova	’231 patent: claims 1, 3, 4, 6, 7 and 8
D-1	Nakauchi	’888 patent: claims 1, 3, 5, 20 and 21
D-2	Tomita	’888 patent: claims 1, 3, 5, 20 and 21
D-3	Nam	’888 patent: claims 1, 3, 5, 20 and 21
D-4	Lin	’888 patent: claims 1, 3, 5, 20 and 21
D-5	Lo Giudice	’888 patent: claims 1, 3, 5, 20 and 21
D-6	Nakayama	’888 patent: claims 1, 3, 5, 20 and 21
D-X1	Seiko	’888 patent: claims 1, 3, 5, 20 and 21
D-X2	Kilopass XPM Devices	’888 patent: claims 1, 3, 5, 20 and 21
D-X3	Micron Technology Flash Memory Devices	’888 patent: claims 1, 3, 5, 20 and 21
E-1	Murakami	’835 patent: claims 1, 2, 4 and 5
E-2	Wang ’162	’835 patent: claims 1, 2, 4 and 5
E-3	Chen	’835 patent: claims 1, 2, 4 and 5

[1] To the extent third-party discovery shows other prior art systems are anticipatory, SK hynix reserves the right to amend these contentions to specifically identify other anticipatory systems.

Exhibit No.	Prior Art Reference[1]	Patents and Claims
E-4	Wang ’055	’835 patent: claims 1, 2, 4 and 5
E-5	Kobayashi	’835 patent: claims 1, 2, 4 and 5
E-6	Lee	’835 patent: claims 1, 2, 4 and 5
E-7	Furuyama	’835 patent: claims 1, 2, 4 and 5
E-8	Umezawa	’835 patent: claims 1, 2, 4 and 5
E-X1	Kilopass XPM Devices	’835 patent: claims 1, 2, 4 and 5
E-X2	Micron Technology Flash Memory Devices	’835 patent: claims 1, 2, 4 and 5

3. Obviousness

As further set forth in the attached Exhibits and below, each of the charted references, and any products, devices, or processes used in the prior art that embody the subject matter disclosed in the references, anticipates and/or renders obvious one or more Asserted Claims of the Asserted Patents. Each of the combinations of prior art references described or identified in Claim Charts and below renders the Asserted Claims of the Asserted Patents invalid under 35 U.S.C. § 103 for obviousness. Each prior art reference may be combined with one or more other prior art references to render obvious the Asserted Claims, as explained in more detail below. The disclosures of these references also may be combined with information known to persons skilled in the art at the time of the alleged invention and understood and supplemented in view of the common sense of persons skilled in the art at the time of the alleged invention, including any statements in the intrinsic record of the Asserted Patents and related applications.

SK hynix expressly intends to combine one or more prior art references identified in the attached Exhibits with each other to address any further contentions from AMT that a particular prior art reference supposedly lacks one or more elements of an Asserted Claim. In other words, SK hynix contends that each charted prior art reference can be combined with each other charted prior art reference (individually or in combination) to the extent the prior art reference lacks or does not explicitly disclose an element or feature of an Asserted Claim. The obviousness

combinations described below are not to be construed to suggest that any reference included in the combinations is not anticipatory. Further, to the extent that AMT contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, SK hynix reserves the right to identify other prior art references that, when combined with the anticipatory prior art, would render the claims obvious despite an allegedly missing limitation.

To the extent not explicitly disclosed by the prior art, the Asserted Claims of the Asserted Patents are nothing more than a combination of standard, conventional elements already existing and well-known at the time of the purported invention, combined according to known methods to achieve predictable results.

All of the following rationales support a finding of obviousness here:

(a) Combining prior art elements according to known methods to yield predictable results;

(b) Simple substitution of one known element for another to obtain predictable results;

(c) Use of known technique to improve similar devices (methods, or products) in the same way;

(d) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(e) "Obvious to try"—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(f) Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and

(g) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

SK hynix further contends that certain prior art identified in these Contentions is evidence of simultaneous or near-simultaneous independent invention by others of the alleged invention as recited in one or more of the Asserted Claims. SK hynix reserves the right to rely on the

simultaneous or near-simultaneous independent invention by others as further evidence of the obviousness of the Asserted Claims.

Each limitation of the Asserted Claims was well known to those of ordinary skill in the art before the filing dates of the application to which the Asserted Patents claim priority, as detailed below and in the attached charts.

The elements recited in the Asserted Claims are mere combinations and modifications of these well-known elements. A person of ordinary skill in the art would be able, and motivated, to update the existing technology in the same or similar manner by combining or modifying the individual elements that were already known in the art to yield predictable results.

Additionally, Defendant notes that Plaintiff has neither provided any contention that secondary considerations of non-obviousness exist for any Asserted Patent nor provided any evidence of such secondary considerations. Defendant is not aware of any evidence supporting the existence of any such secondary considerations. This lack of evidence further renders the Asserted Claims obvious. Proving any such secondary considerations is Plaintiff's burden. *See, e.g.*, *ZUP, LLC v. Nach Mfg., Inc.*, 896 F.3d 1365, 1373 (Fed. Cir. 2018) ("[A] patentee bears the burden of production with respect to evidence of secondary considerations of nonobviousness."). To the extent Plaintiff is permitted to introduce contentions and/or evidence concerning secondary considerations in the future, Defendant reserves all rights to rebut those contentions if and when Plaintiff identifies them. In the meantime, Defendant notes the complete lack of any such evidence in the record. Moreover, Defendant further contends that, in any event, the evidence of obviousness for each Asserted Claim is so overwhelming that secondary considerations are necessarily insufficient to rebut Defendant's showing. *See, e.g., Ohio Willow Wood Co. v. Alps South, LLC*, 735 F.3d 1333, 1344 (Fed. Cir. 2013) ("[W]here a claimed invention represents no

more than the predictable use of prior art elements according to established functions, as here, evidence of secondary indicia are frequently deemed inadequate to establish non-obviousness.”).

a. The ’557 Patent

The following is a list of prior art references that, either alone or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below and in Exhibits A-1 through A-X, would have rendered obvious one or more Asserted Claims of the ’557 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits A-1 through A-X2, Defendant contends that all claims are rendered obvious by Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, and the F70 Devices, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exhibit No.	Primary Reference	In Combination With: [2]
A-1	Meng ’325	One or more of Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit A-OB.
A-2	Cordoba	One or more of Meng ’325, Zhu, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit A-OB.
A-3	Zhu	One or more of Meng ’325, Cordoba, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit A-OB.
A-4	Fukushima	One or more of Meng ’325, Cordoba, Zhu, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit A-OB.
A-5	Chiu	One or more of Meng ’325, Cordoba, Zhu, Fukushima, the F90 Devices, the F70 Devices, or any reference in Exhibit A-OB.
A-X1	F90 Devices	One or more of Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F70 Devices, or any reference in Exhibit A-OB.
A-X2	F70 Devices	One or more of Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, or any reference in Exhibit A-OB.

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’557 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’557 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits A-1 through A-X2 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits A-1 through A-X2, including for the reasons described below. A

[2] To the extent any reference is cited in Exhibits A-1 to A-X, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits A-1 to A-X2.

POSITA at the time of filing of the Asserted Patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’557 patent relates to a booster circuit comprising a triple-well structure and an analog comparison circuit outputting a well bias potential to the first well region of the switching elements of the boosting cells. The asserted claims recite elements that were conventional in DRAM and flash memory devices well before the priority date of the ’557 patent (January 17, 2007). Booster circuits utilizing a triple-well structure and analog comparison circuits to output a well bias to the switching elements were well-known prior to the ’557 patent. *See, e.g.*, ’557 patent at Fig. 25, 1:18-20, 1:21-41, 2:19-26. The prior art is replete with teachings that confirm the ’557 patent’s admission. *See, e.g.*, Meng ’325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 6:7-28, 6:47-52, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9. Indeed, SK hynix already used, in its products sold before the critical date of the ‘557 patent, a booster circuit with such a triple-well structure and an analog comparison circuit. *See* A-X1, A-X2.

Employing a circuit structure comprising two rows of boosting cell stages was also well-known prior to the ’557 patent. *See, e.g.*, ’557 patent at 1:18-20. The benefits of employing two rows of boosting cell stages were well known to a POSITA at the time of the ’557 patent. A two-row structure enabled a variety of advantages in the structure and function of charge pump circuits that utilize complementary clock cycles. Two-row structures exploit complementary clock cycles to be used in a single stage. This was known to reduce the complexity of charge pump circuits by enabling control signals and their complements to be used within a single stage. For example, this

structure was widely used to control switches placed in parallel with diode connected transistors in various charge pump circuits. In Meng ’325, for example, complementary clock signals in a two-row, single stage circuit are used to control switches (rather than diodes) to enable a reduction in the voltage drop that was experienced at each boosting cell stage. A traditional, single row charge pump with diode-connected transistors experiences a voltage drop at each boosting cell stage due to the threshold voltage associated with the switching element of that boosting cell stage. The threshold voltage reduces the voltage that was transferred across the switching element of a boosting cell stage. A two-row structure allowed for a switching element contained in one row to be driven by the complementary row such that the voltage transmission across the switching element did not experience as large of a voltage drop as it would have otherwise experienced due to the switching element’s threshold voltage. This so-called bootstrapping of the charge pump switching elements was well known in the prior art on or before the priority date of the ’557 patent. *See, e.g.*, Meng ’325, 3:63-4:9. The reduction in voltage drops experienced across the boosting cell stages increased the efficiency of a charge pump because a charge pump could yield a greater voltage boost for a given number of boosting cell stages or, alternatively, require fewer boosting cell stages to achieve a given voltage boost. This increased efficiency would have enabled a reduction in the die area required for housing the booster circuit. Similarly, the availability of a complementary control signal offers a reduction in circuit complexity when used in analog comparison circuits, well bias circuits, and various other applications in Cordoba, Meng ’325, and Fukushima. A POSITA would have been motivated to effectuate such a reduction in die area because it made more space available for the placement of memory cells, thereby increasing the memory storage capacity of a memory device. The prior art is replete with teachings that confirm the obviousness of booster circuits comprising two rows of boosting cell stages. *See, e.g.*, Meng

’325, Abstract, Figs. 2a, 2b, 3, 5, 7, 9a, 9b, 11a, 11b, 3:31-37, 4:10-17, 4:18-35, 6:29-38; Cordoba, Figs. 2, 3, 4, 7, 8, 5:15-23, 5:37-41; Fukushima, Abstract, Figs. 1A, 1C, 3A, 3B, 4, 1:11-25, 3:11-30, 4:47-51, 4:66-5:3, 5:4-12, 5:47-52, 6:54-63. Indeed, SK hynix already used a two-row boosting cell structure before the critical date of the ‘557 patent. *See* A-X1, A-X2.

The use of an “analog comparison circuit” in booster circuits was also well known prior to the ’557 patent. *See, e.g.*, Zhu, Figs. 4, 6, 5:1-9, 5:20-26. An analog comparison circuit was known before the priority date of the ’557 patent. Before the priority date of the ’557 patent, a comparison circuit was widely understood to be a circuit comprising two cross-coupled pass gates (*e.g.*, NMOS and/or PMOS transistors) that compared two voltages and outputted either the lower or the higher of the two voltage inputs. *See, e.g.*, Meng ’325, Figs. 5, 7, 9a, 9b, 11a, 11b, 8:16-25, 9:9-36; Fukushima, Fig. 1A, 5:58-64, 6:9-15, 6:39-53; Chiu, Figs. 1, 3A-3H, 5, [0031]. Such comparison circuits were used to select a particular potential and to apply that potential to a well region to prevent the forward biasing of that well region. *See, e.g.*, Meng ’325, Fig. 4, 7:31-47; Zhu, 4:43-57. In doing so, such comparison circuits helped increase the isolation of transistors and helped prevent current leakage between the transistor and the substrate, all of which contributed to increasing the efficiency of booster circuits. Such improved efficiency led to lower voltage losses and lower power consumption. *See, e.g.*, Meng ’325, 8:16-33, 9:9-36; Fukushima, 3:52-63, 7:28-38. The prior art is replete with teachings that confirm the obviousness of incorporating analog comparison circuits into the design of booster circuits. *See, e.g.*, Meng ’325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Indeed, SK hynix already used an analog comparison circuit in its products before the critical date of the ‘557 patent. *See* A-X1, A-X2.

Utilizing an analog comparison circuit to apply a well bias potential to a well region of a triple-well structure would also have been a trivial modification. More generally, applying a well bias potential to a different well region would have been a trivial matter. As discussed, analog comparison circuits were typically used to output a well bias potential to a well region. Choosing to apply an analog comparison circuit's well bias output to a well region in a triple-well structure was well within the scope of use cases. At the time of the '557 patent, it was well known that the additional well associated with a triple-well structure (*i.e.*, deep N-well) required the application of a bias potential to that well in order to prevent current leakage and improve isolation, in addition to preventing breakdown. As the voltage level was boosted at each stage of the charge pump, a POSITA would have been motivated to apply an output well bias potential to a deep N-well and the P-well in order to prevent breakdown between the P-well and deep N-well junction. A POSITA would have been motivated to apply an output well bias potential to the well regions of a triple-well structure in order to avoid the forward biasing of the diode formed at the junction between the deep N-well and the P-well. *See, e.g.*, Meng '325, Figs. 4, 5, 7:16-30, 8:16-33; Meng '494, Fig. 2b, 5:3-17, 15:14-16:5; Lin '129, Fig. 18, 9:26-39. The prior art is replete with teachings that confirm the obviousness of using an analog comparison circuit to apply a bias to a well region in a triple-well structure. *See, e.g.*, Meng '325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Indeed, SK hynix already used an analog comparison circuit to apply a well bias potential to a well region of a triple-well structure before the critical date of the '557 patent. *See* A-X1, A-X2.

Applying a well bias potential to the first well region (*i.e.*, the deep N-well) of the triple-well structure was also well-known prior to the '557 patent. *See, e.g.*, '557 patent at Fig. 25, 1:38-41, 2:22-23. The prior art is replete with teachings that confirm the '557 patent's admission. *See,*

e.g., Park, Figs. 5-7, 9, 11-13, 3:14-20, 4:6-16, 4:32-38, 5:52-58. Such a design was already utilized in SK hynix's devices before the critical date of the '557 patent. *See* A-X1, A-X2.

Utilizing a backflow preventing circuit in a booster circuit was also well-known prior to the '557 patent. *See, e.g.*, '557 patent at Fig. 25, 1:28-30, 1:55-61. Backflow preventing circuits were traditionally used in booster circuits so as to prevent current backflow of the boosted voltages that existed across the various stages of the booster circuit. A POSITA would have been aware of a backflow preventing circuit at the time of the '557 patent because a backflow preventing circuit was simply a diode. A POSITA would have been familiar with the idea of utilizing a diode to prevent the occurrence of backflow at any stage of the booster circuit. By preventing current backflow, backflow preventing circuits improved the efficiency of a booster circuit as it transferred boosted voltage levels across its boosting cell stages. This increased efficiency allowed for smaller input voltages, and also enabled a reduction in the number of boosting cell stages that was required by a booster circuit to reach a particular boosted voltage, which in turn reduced the die area of the booster circuit and enabled an increase in the memory capacity of the memory device. *See, e.g.*, Park '791, 6:13-27, 7:22-47. The prior art is replete with teachings that confirm the obviousness of incorporating backflow preventing circuits into the design of a booster circuit. *See, e.g.*, Park '791, Figs. 11, 7:36-47, 8:56-58, 9:65-67. Such a design was already utilized in SK hynix's devices before the critical date of the '557 patent. *See* A-X1, A-X2.

Utilizing an analog comparison circuit for each boosting cell stage of a booster circuit was also well-known prior to the '557 patent. *See, e.g.*, Meng '325, Fig. 5; Meng '494, 14:4-15. Including an analog comparison circuit for each boosting cell stage would also have been a trivial modification by the priority date of the '557 patent. Each boosting cell stage of a booster circuit would have required a well bias potential to avoid unwanted forward biasing, and as discussed

above, analog comparison circuits were widely used to both select and output an appropriate well bias potential so as to suppress the current leakage that occurs with forward biasing. Incorporating an analog comparison circuit for each boosting cell stage would have therefore been a trivial choice because the inclusion of an analog comparison circuit at each stage would have enabled more control over the well bias potential that was selected and applied to the well regions associated with each respective boosting cell stage. Each boosting cell stage operates at a different voltage level that is either at a higher or lower level than the previous boosting cell stage, and the well bias potential applied to the well regions of a particular boosting cell stage must be within an appropriate range in order to prevent current leakage and avoid breakdown. *See, e.g.*, Meng '494, 14. By including an analog comparison circuit at each stage, a POSITA would have been able to apply an appropriate well bias potential to the triple-well structure so as to avoid leakage, increase isolation, and avoid breakdown. This enhanced control over the amount of well bias potential applied at each boosting cell stage would have improved the overall efficiency of the booster circuit. A POSITA would have been motivated to implement such a trivial design modification in order to achieve the benefits that come with increased efficiency, such as reduced die area and lower power consumption. *See, e.g.*, Meng '325, 2:30-37; Park '791, 6:13-27. The prior art is replete with teachings that confirm the obviousness of utilizing an analog comparison circuit for each boosting cell stage. *See, e.g.*, Meng '325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Such a design was already utilized in SK hynix's devices before the critical date of the '557 patent. *See* A-X1, A-X2.

The presence of a diode at the junction of a terminal and a well region or at the junction between well regions was also well-known prior to the '557 patent. *See, e.g.*, '557 patent at 2:12-

18. The existence of a diode at the interface between a transistor terminal and a well region and at the interface between different well regions was a well-known physical phenomenon. A diode exists whenever a p-type material is adjacent to an n-type material, or more generally whenever two materials of different conductivity make contact. *See, e.g.*, Meng '325, 7:5-14. The prior art is replete with teachings that confirm the '557 patent's admission and that confirm how a POSITA would have understood the formation of a diode at such junctions. *See, e.g.*, Park, Figs. 5, 9, 2:60-3:5, 3:6-20, 3:21-32, 5:13-26, 8:9-16. Indeed, SK hynix already used such a diode before the critical date of the '557 patent. *See* A-X1, A-X2.

Positioning the switching elements of a boosting cell stage such that they share a common first well region of a triple-well structure was well-known prior to the '557 patent. Positioning the switching elements of a boosting cell stage such that they share a common first well region of a triple-well structure with the switching elements of an analog comparison circuit was also well-known prior to the '557 patent. A POSITA would have been motivated to implement an architecture comprising a shared common well region because the overlapping well regions would have reduced the overall die area used by a booster circuit because the multiple switching elements would be sharing the same space on the chip. *See, e.g.*, Hung Fig. 4; Park '791, 4:7-10; Jinbo, Figs. 8, 14, 15. More generally, a POSITA would not have tried to separate well regions that were at the same potential because there would have been no benefit to doing so. A POSITA would have instead been motivated to make efficient use of the chip area available to the booster circuit, and sharing well regions was a common way of making efficient use of limited chip space. *See, e.g.*, Hung Fig. 4; Park '791, 4:7-10; Jinbo, Figs. 8, 14, 15. Moreover, as previously mentioned, a reduced die area would have enabled the inclusion of additional memory cells and therefore increased the memory capacity of the memory device. *See, e.g.*, Meng '325, 2:30-37; Cordoba,

1:47-51. The prior art is replete with teachings that confirm the obviousness of employing shared well regions for the switching elements of a booster circuit. *See, e.g.*, Meng '325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47. Such a design was already utilized in SK hynix's devices before the critical date of the '557 patent. *See* A-X1, A-X2.

In sum, by the time the '557 patent was filed, it was well known to design a booster circuit as claimed at least because all the above was well known in the art, and a POSITA would have known that any and/or all the above techniques could be combined to design a booster circuit comprising two rows of boosting cell stages, a triple-well structure, an analog comparison circuit outputting a well bias potential to a first well region, and a backflow preventing circuit. This is especially true here because all of the references disclose various aspects of the booster circuit but may not disclose every aspect of the design to create a fully formed and functioning device. As such, a POSITA would have logically and predictably consulted multiple references together to design a complete booster circuit having a triple-well structure and both an analog comparison circuit and a backflow preventing circuit. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known booster circuit designs to create different booster circuits. Because all of these techniques were already known in the art for use in the design of a booster circuit, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try

to improve a booster circuit, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits A-1 through A-X2, a POSITA would have been motivated to combine any of the references identified as prior art to the ’557 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and in the accompanying invalidity claim charts teach similar booster circuit designs (and are within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Meng ’325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 4:10-17, 4:51-67, 5:18-20, 6:7-28, 6:47-52, 6:63-7:4, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67, 9:12-19; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, two rows of multiple boosting cell stages, triple-well structure, analog comparison circuit to output a well bias potential, and incorporation of a backflow preventing circuit to prevent backflow of the boosting voltage—to other references that relate to booster circuits generally because all references teach sufficiently a booster circuit designed to increase the magnitude of an input voltage, and it would have been a trivial exercise to consult the references that taught more specific booster circuit designs to fill in less specific disclosures in other references. *See, e.g.*, Meng ’325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 4:10-17, 4:51-67, 5:18-20, 6:7-28, 6:47-52, 6:63-7:4, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67, 9:12-19; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular booster circuit with the teachings regarding other materials, components, and configurations used in other booster circuits for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of booster circuit design exist. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: designing a booster circuit. This is thus a combination of prior art elements (*e.g.*, two row arrangement, switching transistors, triple-well structures, analog comparison circuits, and backflow preventing circuits) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these booster circuit components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of booster circuits were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that Meng '325 does not disclose the "outputting a well bias potential generated by an output potential" limitation, it would have been obvious to combine any

of these references with, *e.g.*, Cordoba or Fukushima, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for outputting a well bias potential generated by an output potential. *See, e.g.*, Cordoba, Figs. 3, 4, 7, 8, 8:41-54, 8:55-67, 9:12-21.

As another example, to the extent that Meng '325 does not disclose the "well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element" limitation, it would have been obvious to combine any of these references with, *e.g.*, Cordoba or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for applying a well bias potential to the first well region of a switching element. *See, e.g.*, Cordoba, Figs. 3, 4, 7, 8, 15, 7:9-19, 8:41-54, 8:55-67, 9:12-21.

As another example, to the extent that Cordoba does not disclose the "backflow preventing circuit" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for backflow preventing circuits. *See, e.g.*, Meng '325, Figs. 11a, 11b, 11:39-42, 11:43-56.

As another example, to the extent that Cordoba does not disclose the "well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one backflow preventing circuit" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325, Park, or Fukushima, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for applying a well bias potential

to the first well region of a switching element in a backflow preventing circuit. *See, e.g.*, Meng '325, Figs. 3-5, 11a, 11b, 7:5-15, 8:16-33, 11:39-42, 11:43-56.

As another example, to the extent that Cordoba does not disclose the "at least one switching elements … of the first and second boosting cell rows share a common first well region" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325 or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for having switching elements share a common first well region. *See, e.g.*, Meng '325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47.

As another example, to the extent that Cordoba does not disclose the "at least one switching elements … of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325 or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for having switching elements and analog comparison circuits share a common first well region. *See, e.g.*, Meng '325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47.

As another example, to the extent that Cordoba does not disclose the "at least one switching circuit of the boosting cell … of the first[/second] boosting cell row and a first[/second] element of the at least one analog comparison circuit share a common first well region" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325 or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for having switching elements

and an element of an analog comparison circuit of a boosting cell row share a common first well region. *See, e.g.*, Meng ’325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47.

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of AMT’s allegations with respect to the level of skill in the art and the qualifications of a POSITA. Defendant is also unaware of the extent, if any, to which AMT may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which AMT will contend that elements not disclosed in the Asserted Patent specifications would have been known to a POSITA. And Defendant does not yet know how the Court will construe terms in the asserted claim. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

b. The ’018 Patent

The following is a list of prior art references that, either alone, or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below, and in Exhibits B-1 through B-X would have rendered obvious one or more Asserted Claims of the ’018 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable

results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits B-1 through B-X2, Defendant contends that all claims are rendered obvious by Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, and the F70 Devices, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exhibit No.	**Primary Reference**	**In Combination With:** [3]
B-1	Meng ’325	One or more of Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit B-OB.
B-2	Cordoba	One or more of Meng ’325, Zhu, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit B-OB.
B-3	Zhu	One or more of Meng ’325, Cordoba, Fukushima, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit B-OB.
B-4	Fukushima	One or more of Meng ’325, Cordoba, Zhu, Chiu, the F90 Devices, the F70 Devices, or any reference in Exhibit B-OB.
B-5	Chiu	One or more of Meng ’325, Cordoba, Zhu, Fukushima, the F90 Devices, the F70 Devices, or any reference in Exhibit B-OB.
B-X1	F90 Devices	One or more of Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F70 Devices, or any reference in Exhibit B-OB.
B-X2	F70 Devices	One or more of Meng ’325, Cordoba, Zhu, Fukushima, Chiu, the F90 Devices, or any reference in Exhibit B-OB.

[3] To the extent any reference is cited in Exhibits B-1 to B-X, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits B-1 to B-X2.

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’018 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’018 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits B-1 through B-X2 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits B-1 through B-X2, including for the reasons described below. A POSITA at the time of filing of the Asserted Patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’018 patent relates to a booster circuit comprising a triple-well structure and an analog comparison circuit outputting a well bias potential to the first well region of the switching elements of the boosting cells. The asserted claims recite elements that were conventional in DRAM and flash memory devices well before the priority date of the ’018 patent (January 17, 2007). Booster circuits utilizing a triple-well structure and analog comparison circuits to output a well bias to the switching elements were well-known prior to the ’018 patent. *See, e.g.*, ’018 patent at Fig. 25, 1:28-30, 1:31-51, 2:29-36. The prior art is replete with teachings that confirm the ’018 patent’s admission. *See, e.g.*, Meng ’325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 6:7-28, 6:47-52, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9. Indeed, SK hynix already used, in its products sold before the critical date of the ‘018 patent,

a booster circuit with such a triple-well structure and an analog comparison circuit. *See* B-X1, B-X2.

Employing a circuit structure comprising two rows of boosting cell stages was also well-known prior to the ’018 patent. *See, e.g.,* ’018 patent at 1:28-30. The benefits of employing two rows of boosting cell stages were well known to a POSITA at the time of the ’557 patent. A two-row structure enabled a variety of advantages in the structure and function of charge pump circuits that utilize complementary clock cycles. Two-row structures exploit complementary clock cycles to be used in a single stage. This was known to reduce the complexity of charge pump circuits by enabling control signals and their complements to be used within a single stage. For example, this structure was widely used to control switches placed in parallel with diode connected transistors in various charge pump circuits. In Meng ’325, for example, complementary clock signals in a two-row, single stage circuit are used to control switches (rather than diodes) to enable a reduction in the voltage drop that was experienced at each boosting cell stage. A traditional, single row charge pump with diode-connected transistors experiences a voltage drop at each boosting cell stage due to the threshold voltage associated with the switching element of that boosting cell stage. The threshold voltage reduces the voltage that was transferred across the switching element of a boosting cell stage. A two-row structure allowed for a switching element contained in one row to be driven by the complementary row such that the voltage transmission across the switching element did not experience as large of a voltage drop as it would have otherwise experienced due to the switching element’s threshold voltage. This so-called bootstrapping of the charge pump switching elements was well known in the prior art on the priority date of the ’557 patent. *See, e.g.*, Meng ’325, 3:63-4:9. The reduction in voltage drops experienced across the boosting cell stages increased the efficiency of a charge pump since a charge pump could yield a greater voltage

boost for a given number of boosting cell stages or, alternatively, required fewer boosting cell stages to achieve a given voltage boost. This increased efficiency would have enabled a reduction in the die area required for housing the booster circuit. Similarly, the availability of a complementary control signal offers a reduction in circuit complexity when used in analog comparison circuits, well bias circuits, and various other applications in Cordoba, Meng ’325, and Fukushima. A POSITA would have been motivated to effectuate such a reduction in die area because it made more space available for the placement of memory cells, thereby increasing the memory storage capacity of a memory device. The prior art is replete with teachings that confirm the obviousness of booster circuits comprising two rows of boosting cell stages. *See, e.g.*, Meng ’325, Abstract, Figs. 2a, 2b, 3, 5, 7, 9a, 9b, 11a, 11b, 3:31-37, 4:10-17, 4:18-35, 6:29-38; Cordoba, Figs. 2, 3, 4, 7, 8, 5:15-23, 5:37-41; Fukushima, Abstract, Figs. 1A, 1C, 3A, 3B, 4, 1:11-25, 3:11-30, 4:47-51, 4:66-5:3, 5:4-12, 5:47-52, 6:54-63. Indeed, SK hynix already used a two-row boosting cell structure before the critical date of the ‘018 patent. *See* B-X1, B-X2.

The use of an “analog comparison circuit” in booster circuits was also well known prior to the ’018 patent. *See, e.g.*, Zhu, Figs. 4, 6, 5:1-9, 5:20-26. An analog comparison circuit was a device that was known before the priority date of the ’018 patent. Before the priority date of the ’018 patent, a comparison circuit was widely understood to be a circuit comprising two cross-coupled pass gates (*e.g.*, NMOS and/or PMOS transistors) that compared two voltages and outputted either the lower or the higher of the two voltage inputs. *See, e.g.*, Meng ’325, Figs. 5, 7, 9a, 9b, 11a, 11b, 8:16-25, 9:9-36; Fukushima, Fig. 1A, 5:58-64, 6:9-15, 6:39-53; Chiu, Figs. 1, 3A-3H, 5, [0031]. Such comparison circuits were used to select a particular potential and to apply that potential to a well region to prevent the forward biasing of that well region. *See, e.g.*, Meng ’325, Fig. 4, 7:31-47; Zhu, 4:43-57. In doing so, such comparison circuits helped increase the

isolation of transistors and helped prevent current leakage between the transistor and the substrate, all of which contributed to increasing the efficiency of booster circuits. Such improved efficiency led to lower voltage losses and lower power consumption. *See, e.g.*, Meng ’325, 8:16-33, 9:9-36; Fukushima, 3:52-63, 7:28-38. The prior art is replete with teachings that confirm the obviousness of incorporating analog comparison circuits into the design of booster circuits. *See, e.g.*, Meng ’325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Indeed, SK hynix already used an analog comparison circuit in its products before the critical date of the ‘018 patent. *See* B-X1, B-X2.

Utilizing an analog comparison circuit to apply a well bias potential to a well region of a triple-well structure would also have been a trivial modification. More generally, applying a well bias potential to a different well region would have been a trivial matter. As discussed, analog comparison circuits were typically used to output a well bias potential to a well region. Choosing to apply an analog comparison circuit’s well bias output to a well region in a triple-well structure was well within the scope of use cases. At the time of the ’557 patent, it was well known that the additional well associated with a triple-well structure (*i.e.*, deep N-well) required the application of a bias potential to that well in order to prevent current leakage and improve isolation, in addition to preventing breakdown. As the voltage level was boosted at each stage of the charge pump, a POSITA would be motivated to apply an output well bias potential to a deep N-well and the P-well in order to prevent breakdown between the P-well and deep N-well junction. A POSITA would have been motivated to apply an output well bias potential to the well regions of a triple-well structure in order to avoid the forward biasing of the diode formed at the junction between the deep N-well and the P-well. *See, e.g.*, Meng ’325, Figs. 4, 5, 7:16-30, 8:16-33; Meng ’494, Fig. 2b, 5:3-17, 15:14-16:5; Lin ’129, Fig. 18, 9:26-39. The prior art is replete with teachings that

confirm the obviousness of using an analog comparison circuit to apply a bias to a well region in a triple-well structure. *See, e.g.*, Meng '325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Indeed, SK hynix already used an analog comparison circuit to apply a well bias potential to a well region of a triple-well structure before the critical date of the '018 patent. *See* B-X1, B-X2.

Applying a well bias potential to the first well region (*i.e.*, the deep N-well) of the triple-well structure was also well-known prior to the '018 patent. *See, e.g.*, '018 patent at Fig. 25, 1:48-51, 2:32-33. The prior art is replete with teachings that confirm the '018 patent's admission. *See, e.g.*, Park, Figs. 5-7, 9, 11-13, 3:14-20, 4:6-16, 4:32-38, 5:52-58. Such a design was already utilized in SK hynix's devices before the critical date of the '018 patent. *See* B-X1, B-X2.

Utilizing a backflow preventing circuit in a booster circuit was also well-known prior to the '018 patent. *See, e.g.*, '018 patent at Fig. 25, 1:38-40, 1:65-2:4. Backflow preventing circuits were traditionally used in booster circuits so as to prevent current backflow of the boosted voltages that existed across the various stages of the booster circuit. A POSITA would have been aware of a backflow preventing circuit at the time of the '557 patent because a backflow preventing circuit was simply a diode. A POSITA would have been familiar with the idea of utilizing a diode to prevent the occurrence of backflow at any stage of the booster circuit. By preventing current backflow, backflow preventing circuits improved the efficiency of a booster circuit as it transferred boosted voltage levels across its boosting cell stages. This increased efficiency allowed for smaller input voltages, and also enabled a reduction in the number of boosting cell stages that was required by a booster circuit to reach a particular boosted voltage, which in turn reduced the die area of the booster circuit and enabled an increase in the memory capacity of the memory device. *See, e.g.*, Park '791, 6:13-27, 7:22-47. The prior art is replete with teachings that confirm the obviousness

of incorporating backflow preventing circuits into the design of a booster circuit. *See, e.g.*, Park ’791, Figs. 11, 7:36-47, 8:56-58, 9:65-67. Such a design was already utilized in SK hynix’s devices before the critical date of the ‘018 patent. *See* B-X1, B-X2.

Utilizing an analog comparison circuit for each boosting cell stage of a booster circuit was also well-known prior to the ’018 patent. *See, e.g.*, Meng ’325, Fig. 5; Meng ’494, 14:4-15. Including an analog comparison circuit for each boosting cell stage would also have been a trivial modification by the priority date of the ’018 patent. Each boosting cell stage of a booster circuit would have required a well bias potential to avoid unwanted forward biasing, and as discussed above, analog comparison circuits were widely used to both select and output an appropriate well bias potential so as to suppress the current leakage that occurs with forward biasing. Incorporating an analog comparison circuit for each boosting cell stage would have therefore been a trivial choice because the inclusion of an analog comparison circuit at each stage would have enabled more control over the well bias potential that was selected and applied to the well regions associated with each respective boosting cell stage. Each boosting cell stage operates at a different voltage level that is either at a higher or lower level than the previous boosting cell stage, and the well bias potential applied to the well regions of a particular boosting cell stage must be within an appropriate range in order to prevent current leakage and avoid breakdown. *See, e.g.*, Meng ’494, 14. By including an analog comparison circuit at each stage, a POSITA would have been able to apply an appropriate well bias potential to the triple-well structure so as to avoid leakage, increase isolation, and avoid breakdown. This enhanced control over the amount of well bias potential applied at each boosting cell stage would have improved the overall efficiency of the booster circuit. A POSITA would have been motivated to implement such a trivial design modification in order to achieve the benefits that come with increased efficiency, such as reduced die area and

lower power consumption. *See, e.g.*, Meng ’325, 2:30-37; Park ’791, 6:13-27. The prior art is replete with teachings that confirm the obviousness of utilizing an analog comparison circuit for each boosting cell stage. *See, e.g.*, Meng ’325, Abstract, Figs. 3, 5, 7, 9a, 9b, 11a, 11b, 6:12-14, 6:29-38, 8:16-22, 9:9-10; Cordoba, Figs. 3, 4, 7, 8, 8:24-39, 8:40-54, 8:55-67, 9:12-19. Such a design was already utilized in SK hynix’s devices before the critical date of the ‘018 patent. *See* B-X1, B-X2.

The presence of a diode at the junction of a terminal and a well region or at the junction between well regions was also well-known prior to the ’018 patent. *See, e.g.*, ’018 patent at 2:22-28. The existence of a diode at the interface between a transistor terminal and a well region and at the interface between different well regions was a well known physical phenomenon. A diode exists whenever a p-type material is adjacent to an n-type material, or more generally whenever two materials of different conductivity make contact. *See, e.g.*, Meng ’325, 7:5-14. The prior art is replete with teachings that confirm the ’018 patent’s admission and that confirm how a POSITA would have understood the formation of a diode at such junctions. *See, e.g.*, Park, Figs. 5, 9, 2:60-3:5, 3:6-20, 3:21-32, 5:13-26, 8:9-16. Indeed, SK hynix already used such a diode before the critical date of the ‘018 patent. *See* B-X1, B-X2.

Positioning the switching elements of a boosting cell stage such that they share a common first well region of a triple-well structure was well-known prior to the ’018 patent. Positioning the switching elements of a boosting cell stage such that they share a common first well region of a triple-well structure with the switching elements of an analog comparison circuit was also well-known prior to the ’018 patent. A POSITA would have been motivated to implement an architecture comprising a shared common well region because the overlapping well regions would have reduced the overall die area used by a booster circuit because the multiple switching elements

would be sharing the same space on the chip. *See, e.g.*, Hung Fig. 4; Park ’791, 4:7-10; Jinbo, Figs. 8, 14, 15. More generally, a POSITA would not have tried to separate well regions that were at the same potential because there would have been no benefit to doing so. A POSITA would have instead been motivated to make efficient use of the chip area available to the booster circuit, and sharing well regions was a common way of making efficient use of limited chip space. *See, e.g.*, Hung Fig. 4; Park ’791, 4:7-10; Jinbo, Figs. 8, 14, 15. Moreover, as previously mentioned, a reduced die area would have enabled the inclusion of additional memory cells and therefore increased the memory capacity of the memory device. *See, e.g.*, Meng ’325, 2:30-37; Cordoba, 1:47-51. The prior art is replete with teachings that confirm the obviousness of employing shared well regions for the switching elements of a booster circuit. *See, e.g.*, Meng ’325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47. Indeed, SK hynix already used such a diode before the critical date of the ‘018 patent. *See* B-X1, B-X2.

In sum, by the time the ’018 patent was filed, it was well known to design a booster circuit as claimed at least because all the above was well known in the art before the ’018 patent, and a POSITA would have known that any and/or all the above techniques could be combined to design a booster circuit comprising two rows of boosting cell stages, a triple-well structure, an analog comparison circuit outputting a well bias potential to a first well region, and a backflow preventing circuit. This is especially true here because all of the references disclose various aspects of the booster circuit but may not disclose every aspect of the design to create a fully formed and functioning device. As such, a POSITA would have logically and predictably consulted multiple references together to design a complete booster circuit having a triple-well structure and both an analog comparison circuit and a backflow preventing circuit. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number

of known booster circuit designs to create different booster circuits. Because all of these techniques were already known in the art for use in the design of a booster circuit, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a booster circuit, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits B-1 through B-X2, a POSITA would have been motivated to combine any of the references identified as prior art to the ’018 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and in the accompanying invalidity claim charts teach similar booster circuit designs (and are within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Meng ’325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 4:10-17, 4:51-67, 5:18-20, 6:7-28, 6:47-52, 6:63-7:4, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67, 9:12-19; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9.

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, two rows of multiple boosting cell stages, triple-well structure, analog comparison circuit to output a well bias potential, and incorporation of a backflow preventing circuit to prevent backflow of the boosting voltage—to other references that relate to

booster circuits generally because all references teach sufficiently a booster circuit designed to increase the magnitude of an input voltage, and it would have been a trivial exercise to consult the references that taught more specific booster circuit designs to fill in less specific disclosures in other references. *See, e.g.*, Meng '325, Abstract, Figs. 3-8, 1:13-24, 2:24-29, 3:31-37, 4:10-17, 4:51-67, 5:18-20, 6:7-28, 6:47-52, 6:63-7:4, 7:5-15, 7:23-29, 7:38-47, 7:57-61, 8:24-32, 8:51-65; Cordoba, Abstract, Figs. 3, 4, 6-8, 15, 1:6-8, 1:9-18, 8:14-23, 8:49-54, 8:62-67, 9:12-19; Park, Figs. 5-7, 9, 11-13, 2:67-3:5, 3:6-9.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference's exact set of materials, components, or configurations in a particular booster circuit with the teachings regarding other materials, components, and configurations used in other booster circuits for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of booster circuit design exist. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: designing a booster circuit. This is thus a combination of prior art elements (*e.g.*, two row arrangement, switching transistors, triple-well structures, analog comparison circuits, and backflow preventing circuits) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these booster circuit components, materials, and configurations were widely-used techniques.

Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of booster circuits were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that Meng '325 does not disclose the "outputting a well bias potential generated by an input potential" limitation, it would have been obvious to combine any of these references with, *e.g.*, Cordoba or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for outputting a well bias potential generated by an input potential. *See, e.g.*, Cordoba, Figs. 3, 4, 7, 8, 8:41-54, 8:55-67, 9:12-21.

As another example, to the extent that Meng '325 does not disclose the "well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element" limitation, it would have been obvious to combine any of these references with, *e.g.*, Cordoba or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for applying a well bias potential to the first well region of a switching element. *See, e.g.*, Cordoba, Figs. 3, 4, 7, 8, 15, 7:9-19, 8:41-54, 8:55-67, 9:12-21.

As another example, to the extent that Cordoba does not disclose the "backflow preventing circuit" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for backflow preventing circuits. *See, e.g.*, Meng '325, Figs. 11a, 11b, 11:39-42, 11:43-56.

As another example, to the extent that Cordoba does not disclose the "well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325, Park or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for applying a well bias potential to the first well region of a switching element in a backflow preventing circuit. *See, e.g.*, Meng '325, Figs. 3-5, 11a, 11b, 7:5-15, 8:16-33, 11:39-42, 11:43-56.

As another example, to the extent that Fukushima does not disclose the "the well bias potential is the lower potential out of the input potential of the boosting cell[s] on the i-th stage" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325 or Cordoba to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for selecting as the well bias potential the lower potential of the boosting cells on the i-th stage. *See, e.g.*, Meng '325, Figs. 5-8, 7:49-62, 8:16-33, 8:34-42, 8:43-48, 8:61-65, 9:9-36, 9:37-46.

As another example, to the extent that Cordoba does not disclose the "the at least one switching element of the boosting cell on the i-th stage of the first [/second] boosting cell row and a first[/second] element of the at least one analog comparison circuit share a common first well region" limitation, it would have been obvious to combine any of these references with, *e.g.*, Meng '325 or Fukushima to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for having switching elements and an element of an analog comparison circuit of a boosting cell row

share a common first well region. *See, e.g.*, Meng ’325, Figs. 3-5, 7, 4:36-50, 5:18-20, 6:39-62, 8:66-9:8; Fukushima, Figs. 1A, 3A, 3B, 4, 7:39-47.

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of AMT’s allegations with respect to the level of skill in the art and the qualifications of a POSITA. Defendant is also unaware of the extent, if any, to which AMT may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which AMT will contend that elements not disclosed in the Asserted Patent specifications would have been known to a POSITA. And Defendant does not yet know how the Court will construe terms in the asserted claim. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

c. The ’231 Patent

The following is a list of prior art references that, either alone or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below and in Exhibits C-1 through C-X would have rendered obvious one or more Asserted Claims of the ’231 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application

of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits C-1 through C-X, Defendant contends that all claims are rendered obvious by Fujise, Ito-177, Kishimoto, Hiiragizawa, Abe, Okasaka, Oshikawa, Dohi, Sato, Gebara, Oku, SK hynix Nova, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exhibit No.	**Primary Reference**	**In Combination With:** [4]
C-1	Fujise	One or more of Ito-177, Kishimoto, Abe, Okasaka, Dohi, Sato, SK hynix Nova, Nakayama, Cernea, Jiang, Saito, or any reference in Exhibit C-OB.
C-2	Ito-177	One or more of Fujise, Okasaka, Oshikawa, Gerbara, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-3	Kishimoto	One or more of Fujise, Ito-177, Okasaka, Oshikawa, Gerbara, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-4	Hiiragizawa	One or more of Ito-177, Kishimoto, Abe, Okasaka, Dohi, Sato, SK hynix Nova, Nakayama, Cernea, Jiang, Saito, or any reference in Exhibit C-OB.
C-5	Abe	One or more of Fujise, Ito-177, Kishimoto, Okasaka, Oshikawa, Gerbara, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-6	Okasaka	One or more of Fujise, Ito-177, Kishimoto, Abe, Oshikawa, Gerbara, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-7	Oshikawa	One or more of Fujise, Ito-177, Kishimoto, Hiiragizawa, Abe, Okasaka, Dohi, Sato, Gebara, Oku, SK hynix Nova, Nakayama, Cernea, Jiang, Saito, or any reference in Exhibit C-OB.

[4] To the extent any reference is cited in Exhibits C-1 to C-X, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits C-1 to C-X.

Primary Exhibit No.	Primary Reference	In Combination With: [4]
C-8	Dohi	One or more of Fujise, Ito-177, Hiiragizawa, Oshikawa, SK hynix Nova, Anantha, Shindo, or any reference in Exhibit C-OB.
C-9	Sato	One or more of Fujise, Ito-177, Hiiragizawa, Oshikawa, SK hynix Nova, Anantha, Shindo, or any reference in Exhibit C-OB.
C-10	Gebara	One or more of Fujise, Ito-177, Kishimoto, Abe, Oshikawa, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-11	Oku	One or more of Fujise, Ito-177, Kishimoto, Abe, Oshikawa, Gerbara, Oku, SK hynix Nova, Nakayama, Anantha, Nakai, Shindo, or any reference in Exhibit C-OB.
C-X1	SK hynix Nova	One or more of Fujise, Ito-177, Hiiragizawa, Abe, Okasaka, Oshikawa, Gebara, Oku, Nakayama, Cernea, Anantha, Jiang, Saito, Shindo, or any reference in Exhibit C-OB.

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’231 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’231 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits C-1 through C-X and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits C-1 through C-X, including for the reasons described below. A POSITA at the time of filing of the Asserted Patents would also have understood the references listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’231 patent relates to an internal voltage generating circuit comprising a first and a second boost circuit in serial connection, which are driven by different

clock signals output from a frequency dividing circuit and selected by a buffer circuit. The asserted claims recite elements that were conventional in DRAM and Flash memory devices well before the priority date of the ’231 patent (July 9, 2008). For example, the ’231 patent itself admits that an internal voltage generating circuit 900 comprising a first and a second boost circuit 901 and 902 was well-known in the art before the alleged invention. *See, e.g.*, ’231 patent at Fig. 9 and associated description. The prior art is replete with teachings that confirm the ’231 patent’s admission. *See, e.g.*, Fujise at Fig. 4; Ito-177 at Fig. 1; Kishimoto at Figs. 1-2 and 10; Abe at Fig. 1; Hiiragizawa at Fig. 4B; Okasaka at Fig. 6; Oshikawa at Fig. 14; Dohi at Fig. 2; Sato at Fig. 12, Gebara at Figs. 2 and 8; Oku at Figs. 5 and 12; Nakayama at Fig. 1; Cernea at Fig. 3; Nakai at Fig. 1; Jiang at Fig. 3; Saito at Fig. 6; Shindo at Fig. 3. Indeed, SK hynix already used, in its products sold before the critical date of the ‘231 patent, a first and second boost circuit driven by different clock signals from a frequency dividing circuit and a buffer circuit. *See* C-X1.

Connecting the first and the second boost circuit serially, rather than in parallel, was also well-known prior to the ’231 patent. It was widely recognized in the industry that a serially connected boost circuit could take advantage of the output of the preceding stage(s) to further step up the output voltage levels. This improves the efficiency of the internal voltage generating circuit and reduces the overall circuit area by eliminating duplicative step-up operations. A POSITA would have been motivated to effectuate such a change. The prior art is replete with teachings that confirm the obviousness of serially-connected boost circuit in an internal voltage generating circuit. As an example, in Kishimoto, the output of “Charge Pump A (CP10),” Va, is input to “Charge Pump B (CP20)” to generate the output voltage Vb. *See* Kishimoto at Fig. 10 and 15:63-16:53. As another example, in Ito-177, the output of the “1st step-up stage (21)” of the step-up circuit is input to the “2nd step-up stage (22),” which is then input to the “3rd step-up stage (23),”

which generates the output voltage Vou. *See* Ito-177 at Fig. 1 and 3:64-4:9. While Plaintiff's infringement contentions point to stages within a boost circuit as being the claimed serially connected first and second boost circuit, such teachings were also known long before the '231 patent. *See, e.g.*, Fujise at Figs. 1 and 4; Hiiragizawa at Fig. 4B. Further, although Plaintiff's infringement contentions also point to boost circuit connected in parallel as meeting the claimed requirements, such arrangements were also well known in the art long before the '231 patent. *See, e.g.*, Okasaka at Fig. 6.

Likewise, using a frequency dividing circuit and a buffer circuit to select different clock signals to supply to the boost circuit, including a serially-connected boost circuit, was also well-known prior to the '231 patent. In particular, because the two boost circuits are serially connected, different clock signals are required to drive them, which a POSITA would recognize to be commonly implemented via a frequency dividing circuit. Once the different clock signals are generated, a POSITA would further understand to select one of the multiple clock signals to supply to the first and the second boost circuit via a selection circuit, which the '231 patent calls the "buffer circuit." The prior art is replete with teachings that confirm the obviousness of using a frequency divider and a buffer to supply clock signals. As an example, Fujise implements a frequency divider (21) and a selection circuit (22) in Fig. 2; Ito-177 implements divider circuits (61, 62, and 63) and a selector circuit (70) in Fig. 5; Kishimoto implements a frequency divider (51) and a switching circuit (52) in Fig. 10; Abe implements a division circuit (24) and selector (23) in Fig. 1; and Hiiragizawa implements a frequency division circuit (6) and a switching circuit (7) in Fig. 6.

The relationship between the length of a period in which a clock signal is in a high state and the frequency of the clock signal was also well-known prior to the '231 patent. A POSITA

would have understood that the period and frequency of a clock signal exhibits an inverse relationship, such that a longer length of a period in which the clock signal is in a high state, the smaller its frequency. The prior art is replete with teachings that confirm the obviousness of this inverse relationship. *See, e.g.*, Fujise at Fig. 2 and 3:60-63; Ito-177 at Figs. 5-6; Kishimoto at Fig. 10; Abe at Fig. 1 and 7:10-24; Hiiragizawa at Figs. 2A, 2D.

In sum, by the time the ’231 patent was filed, it was well known to design an internal voltage generating circuit as claimed at least because all the above was well known in the art before the ’231 patent, and a POSITA would have known that any and/or all the above techniques could be combined to create an internal voltage generating circuit comprising a first and second boost circuit or charge pump circuit, a frequency dividing circuit, and a buffer circuit as claimed. This is especially true here because all of the references disclose various aspects of the foregoing internal voltage generating circuit but may not disclose every aspect of the design to create a fully formed and functioning device. As such, a POSITA would have logically and predictably consulted multiple references together to design a complete voltage generating circuit system. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known component designs to create a different internal voltage generating circuit. Because all of these techniques were already known in the art for use in fabrication of a an internal voltage generating circuit, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable

expectation of success in combining them, would have been obvious to try to improve a voltage generating circuit, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits C-1 through C-X, a POSITA would have been motivated to combine any of the references identified as prior art to the ’231 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and in the accompanying invalidity claim charts teach similar voltage generating circuit designs (and are within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Fujise at Figs. 1 and 4; Ito-177 at Figs. 1 and 5; Kishimoto at Fig. 10; Abe at Figs. 1 and 3; Hiiragizawa at Figs. 1, 4B, and 6;

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, generating and selecting clock signals using a frequency dividing circuit and a buffer circuit—to other references that relate to two serially-connected boost circuit (or charge pump circuit) generally because all references teach using these fundamental building blocks to design and implement an internal voltage generating circuit for memory devices, and it would have been a trivial exercise to consult the references that taught more specific clock generation designs to fill in less specific disclosures in other references. *See, e.g.*, Fujise at Figs. 1 and 4; Ito-177 at Figs. 1 and 5; Kishimoto at Fig. 10; Abe at Figs. 1 and 3; Hiiragizawa at Figs. 1, 4B, and 6;

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference’s exact set of materials, components, or configurations in a particular internal voltage generating circuit with the teachings regarding other materials, components, and configurations

used in other internal voltage generating circuit designs for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of internal voltage generating circuit design. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: to design an internal voltage generating circuit with reduced circuit area and improved efficiency. This is thus a combination of prior art elements (*e.g.*, boost circuit, charge pump circuit, frequency dividing circuit, buffer circuit) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that any prior art reference or system is found not to disclose a second boost circuit or a second charge pump circuit, it would have been obvious to do so for the reasons discussed here and in the corresponding charts, particularly in light of Plaintiff's infringement allegations. For example, Plaintiff alleges that different stages within a charge pump

correspond to the claimed "first charge pump circuit" and "second charge pump circuit." By the same logic, Fujise discloses that Q1, Q2, Q3, and/or Q4 are different stages of a charge pump which are connected serially. As another example, Plaintiff alleges that the charge pumps connected in parallel meet the claimed "first boost circuit" and "second boost circuit." By the same logic, Okasaka at Fig. 6 discloses charge pumps connected in parallel.

As another example, to the extent that any prior art reference or system is found not to disclose a frequency dividing circuit or a buffer circuit, it would have been obvious to combine any of these references with, *e.g.*, Fujise, Ito, Kishimoto, Abe, Hiiragizawa, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for generating clock signals of serially-connected boost circuit (or charge pump circuit).

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of AMT's allegations with respect to the level of skill in the art and the qualifications of a POSITA. Defendant is also unaware of the extent, if any, to which AMT may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which AMT will contend that elements not disclosed in the Asserted Patent specifications would have been known to a POSITA. And Defendant does not yet know how the Court will construe terms in the asserted claim. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

d. The ’888 Patent

The following is a list of prior art references that, either alone or in combination with the knowledge of a person of ordinary skill in the art, Applicant’s Admitted Prior Art, and/or the additional prior art references discussed below and in Exhibits D-1 through D-X, would have rendered obvious one or more Asserted Claims of the ’888 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits D-1 through D-X, Defendant contends that all claims are rendered obvious by Nakauchi, Tomita, Nam, Lin, Lo Giudice, Nakayama, Seiko, XPM, Micron Flash Memory Devices, or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exhibit No.	**Primary Reference**	**In Combination With:** [5]
D-1	Nakauchi	One or more of Tomita, Nam, Lo Giudice, Nakayama, Seiko, XPM, Micron, Im, Cho, Shor, or any reference in Exhibit D-OB.

[5] To the extent any reference is cited in Exhibits D-1 to D-X, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits D-1 to D-X.

Primary Exhibit No.	Primary Reference	In Combination With: [5]
D-2	Tomita	One or more of Nakauchi, Nam, Lo Giudice, Nakayama, Seiko, XPM, Micron, Im, Cho, Shor, or any reference in Exhibit D-OB.
D-3	Nam	One or more of Nakauchi, Tomita, Lo Giudice, Nakayama, Seiko, XPM, Micron, Cho, Shor, , or any reference in Exhibit D-OB.
D-4	Lin	One or more of Nakauchi, Tomita, Lo Giudice, Nakayama, Seiko, XPM, Micron, Cho, Shor, , or any reference in Exhibit D-OB.
D-5	Lo Giudice	One or more of Nakauchi, Tomita, Nam, Lin, Nakayama, Seiko, XPM, Micron, Hirabayashi, Cho, Shor, , or any reference in Exhibit D-OB.
D-6	Nakayama	One or more of Nakauchi, Tomita, Nam, Lin, Lo Giudice, Seiko, XPM, Micron, Hirabayashi, Cho, Shor, , or any reference in Exhibit D-OB.
D-X1	Seiko	One or more of Nakauchi, Tomita, Nam, Lin, Lo Giudice, Nakayama, XPM, Micron, Hirabayashi, Cho, Shor, , or any reference in Exhibit D-OB.
D-X2	XPM	One or more of Nakauchi, Tomita, Nam, Lin, Lo Giudice, Nakayama, Seiko, Micron, Hirabayashi, Cho, Shor, , or any reference in Exhibit D-OB.
D-X3	Micron	One or more of Nakauchi, Tomita, Nam, Lin, Lo Giudice, Nakayama, Seiko, XPM, Hirabayashi, Cho, Shor, , or any reference in Exhibit D-OB.

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’888 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’888 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits D-1 through D-X and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits D-1 through D-X, including for the reasons described below. A POSITA at the time of filing of the Asserted Patents would also have understood the references

listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’888 patent relates to a semiconductor memory device capable of erasing and writing memory contents including a memory cell, one regulator, multiple switches, and a voltage applying transistor. The asserted claims recite elements that were conventional in DRAM and EEPROM memory devices well before the priority date of the ’888 patent (March 10, 2010). For example, the ’888 patent itself admits that such a semiconductor memory device capable of erasing and writing memory contents including a memory cell, one regulator, and a voltage applying transistor was well known in the art. *See, e.g.*, ’888 patent at Background, citing Nakauchi at Fig. 9. The prior art is replete with teachings that confirm the ’888 patent’s admission. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7; Indeed, SK hynix already used, in its products sold before the critical date of the ‘888 patent, semiconductor memory devices capable of erasing and writing memory contents including a memory cell, one regulator, multiple switches, and a voltage applying transistor. *See* D-X2.

Using one regulator to power both the voltage applying transistor and the memory cell was also well-known prior to the ’888 patent. A POSITA would have understood at the relevant time the need to reduce circuit area and, as such, looked to combining the different regulators into one regulator. Indeed, even the Nakauchi prior art cited in the ’888 patent discloses such a motivation. *See, e.g.*, Nakauchi at paras. 60-61. The prior art is replete with teachings that confirm the ’888 patent’s admission. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7.

Employing one or more switches in connection with one regulator to power the voltage applying transistor and the memory cell was also well-known prior to the ’888 patent. A POSITA

would have appreciated at the relevant time that, by using a single regulator to provide different output voltages, different parts of the memory cell circuit can be served by selectively turning on and off one or more switches controlling the power supplied. The prior art is replete with teachings that confirm the ’888 patent’s admission. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7.

Operating the semiconductor memory device in one or more operation modes was also well-known prior to the ’888 patent. For example, at the relevant time period, a POSITA would have appreciated the need to program, read, and/or erase the memory cell contents, each requiring a different driving voltage. As stated before, when a single regulator is used to supply the different driving voltages, the memory cell operating in these different modes would require a plurality of switches to be turned on and off to support the different operation modes. As a POSITA would have recognized, doing so would reduce circuit area and improve the performance of the memory cell. The prior art is replete with teachings that confirm the ’888 patent’s admission. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7; Lo Giudice at Figs. 9-10; Nakayama at Figs. 5-7.

Likewise, using a booster circuit to create a voltage different from the output of the regulator was also well-known prior to the ’888 patent. Indeed, the ’231 patent, which predates the ’888 patent, relates to the use of boost circuit and/or charge pump circuit to supply different voltages to parts of a memory device. As another example, the Nakauchi reference cited in the ’888 patent also discloses the use of two different regulators to supply different voltages. A POSITA would have recognized at the relevant time period that by using a single regulator, it is sometimes necessary to introduce a booster circuit to create higher or lower voltages based on the output of the voltage regulator to supply other parts of the memory device. The prior art is replete

with teachings that confirm the ’888 patent’s admission. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7.

In sum, by the time the ’888 patent was filed, it was well known to design semiconductor memory devices as claimed at least because all the above was well known in the art before the ’888 patent, and a POSITA would have known that any and/or all the above techniques could be combined to design semiconductor memory devices. This is especially true here because all of the references disclose various aspects of the semiconductor memory devices but may not disclose every aspect of the design to create a fully formed and functioning device. As such, a POSITA would have logically and predictably consulted multiple references together to design a complete semiconductor memory device. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known semiconductor memory device designs to create different semiconductor memory devices. Because all of these techniques were already known in the art for use in fabrication of a semiconductor memory device, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a semiconductor memory device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits D-1 through D-X, a POSITA would have been motivated to

combine any of the references identified as prior art to the ’888 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar semiconductor memory device designs (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Tomita at Figs. 3-4 and 15; Nam at Figs. 1-2; Lo Giudice at Figs. 9-10; Nakayama at Figs. 2, 5-7;

Second, a POSITA would have been motivated and found it obvious to apply references teaching certain specific techniques—*e.g.*, one regulator with multiple switches—to other references that relate to power supply for voltage applying transistor and memory cell circuit generally because all references teach sufficiently the same memory circuit design principles, and it would have been a trivial exercise to consult the references that taught more specific regulator arrangements to fill in less specific disclosures in other references.

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference’s exact set of materials, components, or configurations in a particular semiconductor memory device with the teachings regarding other materials, components, and configurations used in other semiconductor memory devices for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that there were multiple techniques of semiconductor memory device design. The substitution of one component, material, or configuration for another would not have changed the principle of operation for either reference in any combination because the references all use similar mechanisms for a similar purpose: to power a voltage applying transistor and memory cell while occupying reduced circuit area. This is thus a combination of prior art elements (*e.g.*, regulator

with switches) according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references' teachings.

As one example, to the extent that a given prior art reference does not disclose the "one regulator" limitation, it would have been obvious to combine any of these references with, *e.g.*, Tomita, Nam, Lo Giudice, Nakayama, and Im, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for merging multiple regulators into a single regulator.

As another example, to the extent that a given prior art reference does not disclose the "output of the regulator is coupled to inputs of the first and second switches" limitation, it would have been obvious to combine any of these references with, *e.g.*, Tomita, Nam, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for implementing a single regulator with switches to power semiconductor memory devices.

As another example, to the extent that a given prior art reference does not disclose the "output of the first switch is coupled to a gate of the voltage applying transistor" limitation, it would have been obvious to combine any of these references with, *e.g.*, Tomita, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for controlling turning on and off the voltage applying transistor.

As another example, to the extent that a given prior art reference does not disclose the "voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell" limitation, it would have been obvious to combine any of these references with, *e.g.*, Nakauchi, Tomita, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for supplying a drain voltage to the memory cell.

As another example, to the extent that a given prior art reference does not disclose the "output of the second switch is coupled to a gate of the memory cell for application of a voltage" limitation, it would have been obvious to combine any of these references with, *e.g.*, Tomita, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for controlling turning on and off the memory cell.

As another example, to the extent that a given prior art reference does not disclose the "output of a fourth switch is coupled to the output of the second switch" limitation, it would have been obvious to combine any of these references with, *e.g.*, Nam, Im, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for supplying alternative

voltages to the gate terminal of the memory cell (e.g., in a programming mode, erase mode, or read mode).

As another example, to the extent that a given prior art reference does not disclose the "first operation mode" and "second operation mode" limitations, it would have been obvious to combine any of these references with, *e.g.*, Tomita, Lo Giudice, and Nakayama, to arrive at said limitation because those references disclose such limitation, and a POSITA would have been motivated to consult references that disclose known options for operating the memory cell in different modes (e.g., in a programming mode, erase mode, or read mode).

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of AMT's allegations with respect to the level of skill in the art and the qualifications of a POSITA. Defendant is also unaware of the extent, if any, to which AMT may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which AMT will contend that elements not disclosed in the Asserted Patent specifications would have been known to a POSITA. And Defendant does not yet know how the Court will construe terms in the asserted claim. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

e. The '835 Patent

The following is a list of prior art references that, either alone or in combination with the knowledge of a person of ordinary skill in the art, Applicant's Admitted Prior Art, and/or the additional prior art references discussed below and in Exhibits E-1 through E-X, would have

rendered obvious one or more Asserted Claims of the ’835 patent, including as indicated in the associated claim charts. A person of ordinary skill in the art would have been motivated and had a reasonable expectation of success to make these combinations because, for example, each would have been merely: (a) a combination of prior art elements according to known methods to yield predictable results; (b) a simple substitution of one known element for another to obtain predictable results; (c) a use of a known technique to improve similar devices in the same way; (d) application of a known technique to a known device ready for improvement to yield predictable results; (e) obvious to try; and/or (f) known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces since the variations are predictable to one of ordinary skill in the art.

As set forth with more detail in Exhibits E-1 through E-X, Defendant contends that all claims are rendered obvious by Murakami, Wang ’162, Chen, Wang ’055, Kobayashi, Lee, Furuyama, Umezawa, Kilpass XPM (“XPM Devices”), and Micron Technology Flash Memory Devices (“MTFM Devices”), or in combination with other references, including the references identified below and discussed in the attached exhibits.

Primary Exhibit No.	**Primary Reference**	**In Combination With:**[6]
E-1	Murakami	One or more of Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-2	Wang ’162	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-3	Chen	One or more of Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ’225, Fastow, or any reference in Exhibit E-OB.

[6] To the extent any reference is cited in Exhibits E-1 to E-X2, but not referenced here, any omission was unintentional and Defendant intends to rely on its identification of any such combinations in Exhibits E-1 to E-X2.

Primary Exhibit No.	Primary Reference	In Combination With:[6]
E-4	Wang ’055	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-5	Kobayashi	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-6	Lee	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-7	Furuyama	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-8	Umezawa	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-X1	Kilopass XPM	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.
E-X2	Micron Technology Flash Memory Devices	One or more of Murakami, Chen, Kumar, Varkony, Javanifard, Yu, Chen ’637, Lee ‘225, Fastow, or any reference in Exhibit E-OB.

To the extent that any of the anticipation references is found not to disclose a limitation recited in the asserted claim of the ’835 patent, it would have been obvious to a POSITA at the time of the alleged invention of the ’835 patent either (i) to modify the reference to include this limitation and any remaining limitations of this claim and/or (ii) to combine said reference with any other of the references in Exhibits E-1 through E-X2 and/or with a POSITA’s general knowledge. Generally, motivation to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. A POSITA would have been motivated to combine any of the references described in attached Exhibits E-1 through E-X2, including for the reasons described below. A POSITA at the time of filing of the Asserted Patents would also have understood the references

listed above, alone or in combination, to contain explicit and/or implicit teaching, suggestion, and/or rationales to combine them, including as further described below.

The alleged invention of the ’835 patent relates to a semiconductor memory for simultaneously writing a plurality of bit lines in non-volatile memory cells. The asserted claims recite elements that were conventional in dynamic random access memory technologies and non-volatile memory storage well before the priority date of the ’835 patent (February 6, 2009). Simultaneously writing a plurality of bit lines in semiconductor memory devices, including using switch circuits, switches, a voltage supply, and a voltage drain, was well-known prior to the ’835 patent. *See, e.g.*, ’835 patent at 1:16-2:39, Figure 9. Moreover, the prior art is replete with teachings that confirm the ’835 patent’s admissions regarding the state of the art at the time of the alleged invention. *See, e.g.*, Murakami at, *inter alia*, paragraphs [0008], [0013], [0044], Figures 1 & 2; Wang ’162 at, *inter alia*, paragraphs [0011]-[0019], Figures 1 & 2; Varkony at, *inter alia*, paragraphs [0041]-[0092] (“Memory Array Architecture, Generally”); Chen at paragraphs [0022]-[0030]; Wang ’055 at [0023], [0032], [0074]-[0076]; Javanifard at 1:18-2:45 (“History of the Prior Art”) 4:3-5:20, 5:39-64; Lee at paragraph [0007]-[0015]. In addition to themselves being prior art to the ’835 patent, each of the foregoing references goes to great lengths to summarize the well-known and well-understood state of the prior art concerning non-volatile flash memory and its components long before even those references’ priority dates. Moreover, commercial manufacturers of non-volatile flash memory cells—including Kilopass and Micron (*see* E-X1, E-X2)—incorporated all of the claimed elements of the ’835 patent into commercial flash products that were publicly disclosed, known, offered for sale, and/or sold into commerce prior to the critical date for the ’835 patent.

Simultaneously writing a plurality of memory cells in non-volatile memory was also well-known prior to the ’835 patent. *See, e.g.,* ’835 patent at 1:66-2:3 (“The write operation of the non-volatile semiconductor memory is typically performed on a group of memory cells basis, such as on a byte-by-byte basis, on a word-by-word basis, etc. The write voltage is simultaneously applied to memory cells in the group, whereby the write time is reduced.”); 2:30-39 (“In the conventional technique, however, a plurality of memory cells are simultaneously written under write conditions (a drain voltage and a drain voltage supply period) which are common to the memory cells.”). The prior art is replete with teachings that confirm the ’835 patent’s admission regarding this conventional technique. *See, e.g.,* Murakami at paragraph [0013]; Chen at paragraph [0008]; Kobayashi at abstract, paragraph [0033]. The notion of simultaneous programming in nonvolatile memory cells was well known and well understood in the prior art, in part because it results in predicable results (*e.g.*, the increase in programming speed and reduction in energy expenditure), and it therefore comprises a known solution that could readily be implemented in a memory device to achieve predictable results. For example, the simultaneous programming of nonvolatile memory cells is described using a plurality of switching transistors in Kumar, which discloses that the “primary object of the present invention” employing such technique is “to provide a simplified and faster initialization technique, and circuits for carrying it out.” Kumar at 1:48-61.

Implementing a drain voltage generation circuit to generate the source of a drain voltage for a plurality of non-volatile memory cells was also well-known prior to the ’835 patent, and such technique constituted a routine and conventional way to effectuate a “write” operation in memory cells. *See, e.g.,* ’835 patent at 1:38-65, 2:30-39, Figure 9. At its core, the disclosed drain voltage generation circuit is nothing more than a circuit that generates an output voltage that may be applied somewhere else in the construct of the IC, including to the memory cells. As disclosed in

the ’835 patent, the drain voltage generation circuit is nothing more than a routine and conventional circuit performing precisely as expected. Unsurprisingly, the prior art is replete with teachings that confirm the ’835 patent’s admission regarding the use of drain voltage and circuits for controlling the same in the construct of memory devices. *See, e.g.*, Murakami at paragraphs [0019], [0023], [0027], [0031]; Wang ’162 at paragraph [0013]; Chen at paragraphs [0006], [0024], [0028]; Furuyama at paragraphs [0009]-[0012]; Javanifard at 7:16-22, 8:19-38; Lee at paragraphs [0013], [0035].

Using one or more switch circuits to each control at least one switch at common terminal points was also well-known prior to the ’835 patent and constituted a predictable and easily-selectable structure for use in a programmable memory cell. The prior art is replete with teachings that confirm this well-known and predictable arrangement in the architecture of a memory cell, which at best constitutes a selection of arranged components from a finite list of options, yielding a predictable solution with expected results (as described further below). *See, e.g.*, Murakami at paragraphs [0029], [0030], [0040], Figures 1 & 3; Wang ’162 at paragraphs [0011]-[0014], Figure 1; Furuyama at paragraphs [0009], [0014]-[0016], Figure 2.

The use of switches (*i.e.*, transistors) in a parallel arrangement, while still being individually controllable by switch circuits in a programable memory cell, was well-known and commonplace to a person of ordinary skill in the art prior to the ’835 patent. A person of ordinary skill in the art would readily understand that each transistor in a memory cell may comprise a common field effect transistor, such as a MOSFET, that contains a gate terminal responsible for “switching” the transistor on/off and creating an electric field conductivity between the source and the drain. Thus, by nature of their operation, switches configured as transistors individually maintain their ability to be selectively controlled for precise applications of electricity.

Furthermore, a person of ordinary skill would know to vary the type of transistor used in such memory applications (e.g., choosing between P- and N-type transistors, among others), in addition to connecting such transistor or switch in parallel or in series with one or more other transistors or switches to achieve the desired output. For example, Murakami at Figure 3 discloses one such exemplary arrangement, which Murakami describes as "Variable resistance circuit VR consists of MOSFETs Q1 to Q4 in parallel form." Murakami at paragraph [0035]. *See also id.* at paragraph [0044] ("The effect is obtained that, assuming the memory array is divided in the direction of the data lines to create memory blocks, it is possible to generate control signals for a variable resistance circuit made up of MOSFETs in a parallel configuration by means of a simple configuration that decodes the X-system address signal to identify the position of the memory cell to be written.") In another example, Chen at Figure 3 discloses a parallel arrangement of transistors, and describes "[t]he data from data input DI is passed to the data latch 225 through a CMOS pass gates 227, which include PMOS and NMOS transistors coupled in parallel, with a first terminal of each coupled together to the data latch 227 and a second terminal of each coupled together to the data input line DI. The gate terminal of the NMOS receives signal DTL and the gate terminal of the PMOS is coupled to /DTL, via inverter 13. Collectively, the transistors of the CMOS pass gate 227 serve as a switch that passes signal DI when DTL is high." Chen at paragraph [0031]. Furthermore, Varkony clarifies that this structure a "common type[] of flash memory," where in "NOR" type flash memory arrangements, "cells are connected in parallel to the bit lines, allowing cells to be read and programmed individually. The parallel connection of cells resembles the parallel connection of transistors in a CMOS NOR gate." Varkony at paragraph [0150]. Thus a person of ordinary skill in the art would have appreciated that the selection of transistor-based

switches in a memory circuit could be controlled by any number of switch circuits or switch control circuits, via their gates, to achieve the ’835 patent claims’ requirements.

To the extent that any prior art reference or system is found not to disclose the specific integer-based numbers of data lines, bit lines, switch circuits, switch control circuits, and switches as set forth in the claims of the ’835 patent by the numbers M and N, it would have been obvious to modify any of the prior art to choose such number of data lines, bit lines, switch circuits, switch control circuits, and switches to arrive at the claimed invention. A person of ordinary skill in the art would readily appreciate that memory cell arrangements are highly modular and can be scaled up, scaled down, and modified by increasing/decreasing sub-features and sub-circuits with little effort and with highly predictable results. Indeed, as the exemplary prior art describes: “It should be understood that any number of bit lines and words lines, and thus any number of cells, may be included in a memory array.” Chen at paragraph [0028]. Wang ’055 similarly recognizes the fluidity of the design of memory cells and arrangements: “The memory 100 in practice is organized into bytes and pages and redundant rows or columns (not shown), which may be done in any desired manner. Many suitable memory organizations are well known in the art.” Wang ’055 at paragraph [0032]. Indeed, Varkony’s disclosure includes lengthy sections detailing such topics as “Memory Array Architecture, Generally,” “Operating Flash Memory,” and “More on Reading the State of The Memory Cells” that respectively detail the manner and arrangement of memory cells with varying numbers of bit lines, word lines, gates, processors, controls, and the application of threshold voltages to achieve memory read and write operations in such arrangements—all of which are “general” principals known by those of skill in the art prior to Varkony’s own invention disclosure. Varkony at paragraphs [0041]-[0092]. Pursuant to any of these exemplary disclosures, a person of ordinary skill in the art would have known that minor variation and alteration within

and among successively and modularly stacked memory cells could be performed to achieve the desired result for a given semiconductor or IC application. These modifications would have been well within the design choice of a person of ordinary skill, and the result of such modifications would have been predictable and expected.

In sum, by the time the ’835 patent was filed, it was well known to design semiconductor memory systems with the ability to simultaneously write a plurality of memory cells using a plurality of bit lines, using a controlled drain voltage supply, and specific, relative numbers of switch control circuits, switch circuits, switches, and data lines as claimed, at least because all the above was well known in the art before the ’835 patent, and a POSITA would have known that any and/or all the above techniques could be combined to achieve a semiconductor memory having such arrangement. This is especially true here because all of the references disclose various aspects of memory cells having common, substantially similar arrangements intended to improve efficiency of the circuits, improve write/read time, maximize longevity, and utilize the least amount of energy (among other goals) but they may not disclose every aspect of the design to create a fully formed and functioning device. As such, a POSITA would have logically and predictably consulted multiple references together, along with the solution-seeking approach of a skilled artisan, to design a complete semiconductor memory having the components arranged as in the ’835 patent claims. Furthermore, the general background knowledge described above and below would have provided the basis for combining any number of known non-volatile semiconductor memory designs to create different designs and arrangements. Because all of these techniques were already known in the art for use in fabrication of non-volatile memory devices and circuits, a POSITA would have understood that combining any/all of these techniques would have yielded predictable results, would have been a simple substitution of one known technique

for another to obtain predictable results, would have used known techniques to improve similar techniques in the same way, would have applied a known technique to a known method that was ready for improvement to yield predictable results, would have been obvious to try because the techniques were all known and there was reasonable expectation of success in combining them, would have been obvious to try to improve a semiconductor device, and would have been obvious because all techniques were already known and combined in various fashions before. With respect to the prior art references in Exhibits E-1 through E-X2, a POSITA would have been motivated to combine any of the references identified as prior art to the ’835 patent for these reasons provided above and the additional reasons provided below.

First, the prior art references identified above and the accompanying invalidity claim charts teach similar non-volatile memory designs (and within relevant timeframes), and thus the teachings of any one reference are applicable to other references in that same field. *See, e.g.*, Varkony at paragraphs [0041]-[0092] (detailing general principles of memory design).

A POSITA would have also been motivated and found it obvious to replace and/or combine a reference’s exact set of materials, components, or configurations in a particular non-volatile memory circuit with the teachings regarding other materials, components, and configurations used in other non-volatile memory circuits for all the reasons provided above and below. These modifications would have been a simple substitution of one known element for another, which would have obtained predictable results because it was already well known in the art that multiple techniques of non-volatile memory design were possible, given the modular, adaptable, and variable nature of design that could be employed on a granular circuit/component level. The substitution of one component, material, or configuration for another would not have changed the principle of operation for any reference in combination with such other reference because the

references all use similar mechanisms for a similar purpose: improved efficiency and decreased power requirements (among other things) to generally improve the quality and quantity of non-volatile memory storage. The non-volatile memory devices of the ’835 patent claims are thus merely a combination of prior art elements according to known methods (a POSITA would understand that these are all available design choices) to yield predictable results (a POSITA would understand the benefits and drawbacks of each design choice, and there are no unexpected results from any particular combination). A POSITA would have been motivated to combine these teachings, and to make these replacements, because all of these semiconductor device components, materials, and configurations were widely-used techniques. Accordingly, a POSITA would have had a reasonable expectation of success given considerations discussed above, the similarities in the teachings and systems, and given that the claimed components and configurations of semiconductor fabrication were all well-known at the time. Implementing the combination and any necessary modifications would have been routine and within the scope of the prior art references’ teachings.

As one example, to the extent that Murakami, Chen, Kobayashi, or Wang ’162 does not disclose the “on-state period” control limitation of claim 5, it would have been obvious to combine any of these references with, *e.g.*, Javanifard, Yu, Chen ’637, Lee ’225, or Fastow to arrive at said limitation because each of these references discloses such limitation (*e.g.*, “pulse width,” or similar nomenclature), and a POSITA would have been motivated to consult references that disclose known options for controlling the timing and on-state periods for switches and controls in memory circuits to improve write times and sequences for optimized memory storage. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1379-80 (Fed. Cir. 2023) (holding that a POSITA is “a person of ordinary creativity,” and can apply “universal” motivations “even absent any hint of

suggestion in the references themselves" and who can apply the "known technique rationale" for features having "established functions" that would "improve similar devices in the same way.") And "if there's a known technique to address a known problem using prior art elements according to their established functions, then there is a motivation to combine." *Id.* at 1380.

Additional obviousness combinations of the references identified here are possible, and Defendant may rely on such combination(s) in this litigation. In particular, Defendant is currently unaware of AMT's allegations with respect to the level of skill in the art and the qualifications of a POSITA. Defendant is also unaware of the extent, if any, to which AMT may contend that limitations of the claims at issue are not disclosed in the prior art identified by Defendant as anticipatory, and the extent to which AMT will contend that elements not disclosed in the Asserted Patent specifications would have been known to a POSITA. And Defendant does not yet know how the Court will construe terms in the asserted claim. Defendant is also continuing its investigation of the large universe of prior art to identify potential prior art systems, publications related to those systems, and third parties that may have information about those systems. Defendant reserves the right to amend and supplement these contentions to identify other prior art and combinations rendering the asserted claim obvious.

4. Secondary Considerations

Defendant is not aware of objective evidence or secondary considerations demonstrating non-obviousness of the asserted claims of the '557 patent, '018 patent, '231 patent, '888 patent, and '835 patent. As set forth below, the evidence confirms that the asserted claims would have been obvious to a person of ordinary skill in the art at the time of the alleged invention. Defendant reserves the right to supplement or modify these factors to address any evidence or arguments later identified by Plaintiff.

a. The Alleged Invention Did Not Satisfy a Long-Felt But Unresolved Need

Defendant is not aware of any evidence of a long-felt but unmet need that the asserted claims solve. On the contrary, the concepts and functions described in the asserted claims of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent were all well-known before the alleged invention date as evidenced by the patent itself, its file history and the references cited therein, and the prior art Defendant has identified in these contentions and accompanying Exhibits.

b. The Alleged Invention Did Not Face Unexpected Results, Skepticism, or Teaching Away by Experts

Defendant is not aware of any evidence of a failure of others to invent or use the claimed techniques before the alleged invention dates of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent. As discussed, the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent recites concepts that were already known in the prior art.

c. The Alleged Invention Was Not Subject to Industry Acceptance

Defendant is not aware of any evidence that Plaintiff’s alleged invention in the ’557 patent was subject to additional industry acceptance due to Plaintiff or the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent. This is at least because the subject matter of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent already existed in the industry and was used by many entities and individuals prior to the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent.

d. The Alleged Invention Has Not Been Subject to Industry Praise

Defendant is not aware of any evidence of industry praise for any of the alleged inventions of the ’557 patent. To the extent any industry praise is related to any functionality that Plaintiff alleges practices the ’557 patent, that praise is not due to the allegedly novel features of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent, but instead only to features present

in the prior art, which is not a sufficient nexus for purposes of obviousness. *See Muniauction, Inc. v. Thomson Corp.*, 532 F.3d 1318, 1328 (Fed. Cir. 2008).

e. The Alleged Invention Is Not Responsible for Commercial Success

Defendant is not aware of any evidence of alleged success of any products that is due to the alleged invention claimed in the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent. The patentee bears the burden of demonstrating that the relevant commercial success is attributable to the claimed invention “as opposed to other economic and commercial factors unrelated to the technical quality of the patented subject matter.” *Cable Elec. Prods, Inc. v. Genmark, Inc.*, 770 F. 2d 1015, 1027 (Fed. Cir. 1987). Here, Plaintiff has not shown (and cannot show) that any commercial success is due to the alleged invention of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent. *See Windsurfing Int’l Inc. v. AMF*, 782 F. 2d 995 (Fed. Cir. 1986) (considerations such as intervening, non-covered technological innovations, popularity of accessories, and advertising expense are all relevant to the nexus determination).

Moreover, to the extent any commercial success of any products is due to concepts discussed in any of the asserted patents, those concepts were already present in the prior art, as described above, and thus does not support any commercial success that is relevant to the question of obviousness. *Tokai Corp. v. Easton Enterprises, Inc.*, 632 F.3d 1358, 1369-70 (Fed. Cir. 2011) (“If commercial success is due to an element in the prior art, no nexus exists.”); *In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011) (“Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, there is no nexus to the merits of the claimed invention.”); *Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312 (Fed. Cir. 2006) (“[I]f the feature that creates the commercial success was known in the prior art, the success is not pertinent.”).

f. There Is No Evidence to Show Copying of the Alleged Invention

Defendant is not aware of any evidence of any aspect of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent that was copied by any entity or person, much less that any functionality that practices the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent was copied. *See Amazon.com, Inc. v. Barnesandnoble.com, Inc*., 239 F.3d 1343, 1366 (Fed. Cir. 2001) (allegedly copied feature must be an embodiment of the patented claims).

g. Simultaneous Development of the Alleged Invention Confirms that the Asserted Claims Were Obvious

As set forth above, many people and companies independently and simultaneously developed and invented the same technology within a comparatively short space of time of a few years, which further shows that the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent was the product only of ordinary engineering skill. Moreover, the fact that there was relatively simultaneous invention demonstrates that the subject matter of the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent was already well within the level of ordinary skill in the art.

h. There Is No Evidence of the Failure of Others

No evidence of any such failure is known. To the contrary, the prior art cited in the Exhibits demonstrates that numerous others had already succeeded at the same endeavor purportedly addressed by the ’557 patent, ’018 patent, ’231 patent, ’888 patent, and ’835 patent.

C. Invalidity Contentions Pursuant to P.R. 3-3(d)

Pursuant to P. R. 3-3(d), SK hynix contends that certain Asserted Claims of the Asserted Patents are invalid under 35 U.S.C. § 112 because: (1) the claims lack adequate written description; (2) the claims are not enabled, and/or (3) the claims are indefinite. The following contentions, made pursuant to P. R. 3-3(d), are subject to revision and amendment pursuant to Federal Rule of

Civil Procedure 26(e) and the Orders of record in this matter to the extent appropriate, *e.g.*, in light of further investigation and discovery regarding the defenses, the Court's construction of the claims at issue, and/or review and analysis of expert witnesses.

1. Enablement and Written Description

The asserted claims are invalid for failure to comply with the written description and enablement requirements because the Asserted Patents do not contain sufficient written description of the claimed invention and do not provide a sufficiently enabling disclosure. *See* 35 U.S.C. § 112. To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention at the time of filing the patent application. *See generally Ariad Pharm., Inc. v. Eli Lilly and Co.*, 598 F.3d 1336 (Fed. Cir. 2010) (en banc). "To be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." *MagSil Corp. v. Hitachi Global Storage Techs.*, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012) (citation omitted). The specifications of the Asserted Patents do not adequately describe or enable the claimed inventions recited in the Asserted Claims.

The "enablement requirement is satisfied when one skilled in the art, after reading the specification, could practice the claimed invention without undue experimentation." *Auto. Techs. Int'l, Inc. v. BMW of N. Am.*, 501 F.3d 1274, 1282 (Fed. Cir. 2007). A claimed invention may be invalid for lack of written description and non-enablement even if it was disclosed in the prior art: "It is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of an invention in order to constitute adequate enablement." *Genentech v. Novo Nordisk*, 108 F.3d 1361, 1366 (Fed. Cir. 1997). The patentee is "required to provide an adequate enabling disclosure in the specification; it cannot simply rely on the knowledge of a person of ordinary skill

to serve as a substitute for the missing information in the specification." *Alza Corp. v. Andrx Pharms., LLC*, 603 F.3d 935, 940-41 (Fed. Cir. 2010). "A patentee who chooses broad claim language must make sure the broad claims are fully enabled." *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999-1000 (Fed. Cir. 2008). As the Federal Circuit has explained:

> Enablement serves the dual function in the patent system of ensuring adequate disclosure of the claimed invention and of preventing claims broader than the disclosed invention. This important doctrine prevents both inadequate disclosure of an invention and overbroad claiming that might otherwise attempt to cover more than was actually invented. Thus, a patentee chooses broad claim language at the peril of losing any claim that cannot be enabled across its full scope of coverage.

Magsil Corp. and MIT v. Hitachi, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012). "The specification must contain sufficient disclosure to enable an ordinarily skilled artisan to make and use the entire scope of the claimed invention at the time of filing." *Id.* at 1381-82.

SK hynix contends that the patent specifications do not provide sufficient written description and enablement for each of the claim limitations identified below, which identify grounds of invalidity for lack of enablement and written description with respect to the asserted claims and the limitations of the asserted claims, pursuant to Patent Rule 3-3(d). Where SK hynix has identified a phrase as lacking written description and/or enablement, SK hynix also contends that the subparts of the phrase lack written description and/or enablement within the context recited in the claim.

The following discussion includes the identification and discussion of claim terms and limitations lacking § 112 written description and enablement support. A more detailed basis for Defendant's written description and enablement defenses may be set forth in any expert report(s) on invalidity to be served by Defendant in accordance with the Court's Second Amended Docket Control Order or any subsequent amendments ordered by the Court.

a. ’557 Patent

Asserted claims 1, 2, 4, 7, 9, 10, 11, 12, and 14 of the ’557 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’557 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AMT in its infringement contentions:

- “at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i-th stage (1≦i≦N) of the first boosting cell row and an output potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row” (claim 1)
- “the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows” (claim 1)
- “the well bias potential is the lower potential out of the output potential of the boosting cell on the i-th stage; (1≦i≦N) of the first-boosting cell row and the output potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row” (claim 4)
- “a diode element is provided between the first terminal and the first well region of the boosting cell” (claim 9)
- “the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region” (claim 10)
- “the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region” (claim 11)
- “the at least one switching circuit of the boosting cell on the i-th stage of the first[/second] boosting cell row and a first[/second] element of the at least one analog comparison circuit share a common first well region” (claim 12)
- “a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cel rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row” (claim 14)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’557 patent were in possession of the claimed subject matter, at least

to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '557 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '557 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

b. '018 Patent

Asserted claims 1, 2, 4, 7, 9, and 10 of the '018 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '018 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AMT in its infringement contentions:

- "at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i-th stage (1≦i≦N) of the first boosting cell row and an input potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row" (claim 1)
- "the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows" (claim 1)
- "the well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows" (claim 2)
- "the well bias potential is the lower potential out of the input potential of the boosting cell on the i-th stage (1≦i≦N) of the first boosting cell row and the input potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row" (claim 4)
- "a diode element is provided between the first terminal and the first well region of the boosting cell" (claim 9)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’018 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff’s infringement contentions, the ’018 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff’s infringement contentions, the ’018 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

c. ’231 Patent

Asserted claims 1, 3, 4, 6, 7 and 8 of the ’231 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’231 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AMT in its infringement contentions:

- “a first boost circuit provided between a first voltage and a first terminal” (claim 1)
- “a second boost circuit provided between the first terminal and a second terminal” (claim 1)
- “a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit” (claim 3)
- “wherein a frequency of a clock signal to be su shied to the second charge pump circuit is changed in accordance with a control signal” (claim 6)

- "the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency" (claim 6)
- "wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal" (claim 7)
- "wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency" (claim 8)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the '231 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff's infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff's infringement contentions, the '231 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '231 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

d. '888 Patent

Asserted claims 1, 3, 5, 20 and 21 of the '888 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the '888 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AMT in its infringement contentions:

- "A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal" (claim 1)
- "one regulator" (claim 1)

- “a voltage applying transistor for applying a voltage to the memory cell” (claim 1)
- “an output of the regulator is coupled to inputs of the first and second switches” (claim 1)
- “an output of the first switch is coupled to a gate of the voltage applying transistor” (claim 1)
- “a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell” (claim 1)
- “an output of the second switch is coupled to a gate of the memory cell for application of a voltage” (claim 1)
- “an output of a fourth switch is coupled to the output of the second switch” (claim 3)
- “a voltage different from the output of the regulator is applied to the gate of the memory cell” (claim 3)
- “allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell” (claim 5)
- “allowing the output voltage of the regulator to be applied to the gate of the memory cell” (claim 5)
- “the voltage different from the output of the regulator is an output voltage of a booster circuit” (claim 20)
- “an output of a booster circuit is coupled to a source terminal of the voltage applying transistor” (claim 21)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’888 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff’s infringement contentions, the ’888 patent fails to teach a person of ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff’s infringement contentions, the ’888

patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

e. ’835 Patent

Asserted claims 1, 2, 4 and 5 of the ’835 patent fail to satisfy the requirements of 35 U.S.C. § 112 at least because the ’835 patent fails to provide an adequate written description or enablement of the following limitations, at least as those limitations are applied by AMT in its infringement contentions:

- “M data lines connected to the plurality of bit lines based on a column address signal, where M is an integer of two or more and is smaller than the number of the bit lines” (claim 1)
- “each of the M switch circuits includes N switches, where N is an integer of one or more” (claim 1)
- “M switch circuits and M switch control circuits provided between the M data lines and the drain voltage supply line,” (claim 1)
- “each of the M×N switches includes a first and a second terminal, and the first terminals of the N switches of each of the M switch circuits are connected at a common point to a corresponding one of the M data lines, and the second terminals of the N switches of each of the M switch circuits are connected at a common point to the drain voltage supply line” (claim 1)
- “the M switch control circuits control combination of on and off states of the N switches connected to a corresponding one of the M data lines on a data line-by-data line basis” (claim 4)
- “the M switch control circuits control on-state periods of the N switches connected to a corresponding one of the M data lines on a data line-by-data line basis” (claim 5)

The foregoing phrases are not described in such a way that a person having ordinary skill in the art at the time of the alleged invention would have understood that the individuals named as the inventors on the face of the ’835 patent were in possession of the claimed subject matter, at least to the extent the claims are interpreted consistently with the positions taken in Plaintiff’s infringement contentions. Furthermore, to the extent the claims are interpreted consistently the positions taken in Plaintiff’s infringement contentions, the ’835 patent fails to teach a person of

ordinary skill in the art how to make and use the full scope of the claimed invention without undue experimentation with respect to foregoing phrases. To the extent the claims are construed or interpreted to be as broad as the positions taken in Plaintiff's infringement contentions, the '835 patent does not provide adequate written description or enable the full scope of the claim limitations listed above.

2. Indefiniteness

One or more terms of the Asserted Claims may suffer from defects that render them indefinite, as those claims are applied by AMT to the Accused Products in AMT's Infringement Contentions. A more detailed basis for SK hynix's indefiniteness defenses may be set forth in any expert report(s) on invalidity to be served by SK hynix in accordance with the Court's Second Amended Docket Control Order or any subsequent amendments ordered by the Court and/or at an appropriate later stage of this lawsuit, such as claim construction. To the extent that SK hynix has identified any instance of a term or limitation in a particular claim as rendering the claim invalid as indefinite, SK hynix contends that every instance of the challenged term or limitation in each Asserted Claim renders the claim invalid for the same reason.

a. '557 Patent

One or more Asserted Claims, and/or terms of the Asserted Claims, of the '557 patent may suffer from defects that render them indefinite, at least under interpretations and/or applications of the claim language that AMT appears to be asserting, including, for example:

- "at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i-th stage ($1 \leqq i \leqq N$) of the first boosting cell row and an output potential of the boosting cell on the i-th stage ($1 \leqq i \leqq M$) of the second boosting cell row" (claim 1)
- "the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows" (claim 1)

- “the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows” (claim 2)

- “the well bias potential is the lower potential out of the output potential of the boosting cell on the i-th stage; (1≦i≦N) of the first-boosting cell row and the output potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row” (claim 4)

- “a diode element is provided between the first terminal and the first well region of the boosting cell” (claim 9)

- “the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region” (claim 10)

- “the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region” (claim 11)

- “the at least one switching circuit of the boosting cell on the i-th stage of the first[/second] boosting cell row and a first[/second] element of the at least one analog comparison circuit share a common first well region” (claim 12)

- “a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cel rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row” (claim 14)

b. ’018 Patent

One or more Asserted Claims, and/or terms of the Asserted Claims, of the ’018 patent may suffer from defects that render them indefinite, at least under interpretations and/or applications of the claim language that AMT appears to be asserting, including, for example:

- “at least one analog comparison circuit for outputting a well bias potential generated by an input potential of the boosting cell on the i-th stage (1≦i≦N) of the first boosting cell row and an input potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row” (claim 1)

- “the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows” (claim 1)

- “the well bias potential of the at least one analog comparison circuit is applied to a first well region of a switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows” (claim 2)

- "the well bias potential is the lower potential out of the input potential of the boosting cell on the i-th stage (1≦i≦N) of the first boosting cell row and the input potential of the boosting cell on the i-th stage (1≦i≦M) of the second boosting cell row" (claim 4)

- "a diode element is provided between the first terminal and the first well region of the boosting cell" (claim 9)

c. '231 Patent

One or more Asserted Claims, and/or terms of the Asserted Claims, of the '231 patent may suffer from defects that render them indefinite, at least under interpretations and/or applications of the claim language that AMT appears to be asserting, including, for example:

- "a first boost circuit provided between a first voltage and a first terminal" (claim 1)

- "a second boost circuit provided between the first terminal and a second terminal" (claim 1)

- "a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit" (claim 3)

- "wherein a frequency of a clock signal to be su shied to the second charge pump circuit is changed in accordance with a control signal" (claim 6)

- "the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency" (claim 6)

- "wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal" (claim 7)

- "wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency" (claim 8)

d. '888 Patent

One or more terms of the Asserted Claim of the '888 patent may suffer from defects that render the Asserted Claim indefinite, at least under interpretations and/or applications of the claim language that AMT appears to be asserting, including, for example:

- "A semiconductor memory device capable of erasing and writing memory contents in a memory cell using an electric signal" (claim 1)

- “one regulator” (claim 1)
- “a voltage applying transistor for applying a voltage to the memory cell” (claim 1)
- “an output of the regulator is coupled to inputs of the first and second switches” (claim 1)
- “an output of the first switch is coupled to a gate of the voltage applying transistor” (claim 1)
- “a voltage is applied from a drain terminal of the voltage applying transistor to a drain terminal of the memory cell” (claim 1)
- “an output of the second switch is coupled to a gate of the memory cell for application of a voltage” (claim 1)
- “an output of a fourth switch is coupled to the output of the second switch” (claim 3)
- “a voltage different from the output of the regulator is applied to the gate of the memory cell” (claim 3)
- “allowing the output voltage of the regulator to be applied to the drain terminal of the memory cell” (claim 5)
- “allowing the output voltage of the regulator to be applied to the gate of the memory cell” (claim 5)
- “the voltage different from the output of the regulator is an output voltage of a booster circuit” (claim 20)
- “an output of a booster circuit is coupled to a source terminal of the voltage applying transistor” (claim 21)

e. ’835 Patent

One or more terms of the Asserted Claim of the ’835 patent may suffer from defects that render the Asserted Claim indefinite, at least under interpretations and/or applications of the claim language that AMT appears to be asserting, including, for example:

- “M data lines connected to the plurality of bit lines based on a column address signal, where M is an integer of two or more and is smaller than the number of the bit lines” (claim 1)
- “each of the M switch circuits includes N switches, where N is an integer of one or more” (claim 1)

- "each of the M×N switches includes a first and a second terminal, and the first terminals of the N switches of each of the M switch circuits are connected at a common point to a corresponding one of the M data lines, and the second terminals of the N switches of each of the M switch circuits are connected at a common point to the drain voltage supply line" (claim 1)

- "the M switch control circuits control combination of on and off states of the N switches connected to a corresponding one of the M data lines on a data line-by-data line basis" (claim 4)

- "the M switch control circuits control on-state periods of the N switches connected to a corresponding one of the M data lines on a data line-by-data line basis" (claim 5)

D. Document Production Pursuant to P.R. 3-4

1. Documents Related to Accused Instrumentalities Under P.R. 3-4(a)

Based on Defendant's investigations to date, Defendant has collected and is ready to produce materials pursuant to Patent Rule 3-4(a). Specifically, Defendant has collected documents sufficient to show the operation of the accused instrumentality identified by AMT in its P.R. 3-1(c) charts. But as Defendant has previously informed Plaintiff, SK hynix's technical information underlying the accused instrumentality is classified as national core technology (NCT) by the South Korean Ministry of Trade, Industry, and Energy (MOTIE), and thus approval from the MOTIE is necessary for SK hynix to produce the technical information in this case. *See* K. Jang's April 21, 2025 and May 28, 2025 Emails. Upon approval of the MOTIE applications (which were submitted on March 11, 2025 and May 23, 2025), SK hynix will produce the documents containing NCT, including by making the materials designated RESTRICTED CONFIDENTIAL SOURCE CODE available for review on a source code computer at Quinn Emanuel's offices located in 555 Twin Dolphin Dr 5th Floor, Redwood City, CA 94065.

2. Documents Related to Prior Art Under P.R. 3-4(b)

Based on Defendant's investigations to date, pursuant to P.R. 3-4(b), Defendant has produced or is producing documents currently in its possession, custody, or control that are the

prior art references identified above and/or in the attached charts in connection with Defendant's P.R. 3-3 disclosure. Such documents include those produced (or will be produced) at SKH_00008844 to SKH_00014741. Further, Defendant has made prior art materials designated RESTRICTED CONFIDENTIAL SOURCE CODE (*e.g.*, at SKH_SC_00000001 to SKH_SC_00002068) available for inspection at Quinn Emanuel's offices located in 555 Twin Dolphin Dr 5th Floor, Redwood City, CA 94065, consistent with the Protective Order and Discovery Order in this case. The native source files will also be made available for inspection under SK hynix's network in the Republic of Korea.

Defendant expects to supplement these productions based on documents produced by third parties pursuant to one or more subpoenas or Letter Rogatory served or will be served in this case.

Dated: June 25, 2025

Respectfully submitted,

/s/ Kevin Jang

Sean Pak (CA Bar No. 219032)
seanpak@quinnemanuel.com
Andrew M. Holmes (CA Bar No. 260475)
drewholmes@quinnemanuel.com
Kevin (Gyushik) Jang (CA Bar No. 337747)
kevinjang@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
50 California Street, 22nd Floor
San Francisco, California 94111-4788
Tel: (415) 875-6600
Fax: (415) 875-6700

D. James Pak (CA Bar No. 194331)
djamespak@quinnemanuel.com
Zhaoxin John Yin (CA Bar No. 325589)
johnyin@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
865 S. Figueroa St, 10th Floor

Los Angeles, CA 90017
Tel: (213) 443-3000
Fax: (213) 443-3100

Richard Erwine (NY Bar No. 2753929)
richarderwine@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
295 5th Avenue, 9th Floor
New York, New York 10016
Tel: (212) 849-7000
Fax: (212) 849-7100

Brian L. Saunders (DC Bar No. 1615227)
briansaunders@quinnemanuel.com
QUINN EMANUEL URQUHART & SULLIVAN, LLP
1300 I St N.W., Suite 900
Washington, DC 20005
Tel.: (202) 538-8000
Fax: (202) 538-8100

Deron R. Dacus
Texas Bar No. 00790553
THE DACUS FIRM, P.C.
821 ESE Loop 323, Suite 430
Tyler, Texas 75701
903-705-1117
E-mail: ddacus@dacusfirm.com

Counsel for Defendant SK hynix Inc.

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above and foregoing document has been served on June 25, 2025 to all counsel of record by e-mail message addressed as follows:

Justin A. Nelson
Texas State Bar No. 24034766
SUSMAN GODFREY LLP
1000 Louisiana Street, Suite 5100
Houston, Texas 77002
Telephone: (713) 651-9366
Facsimile: (713) 654-6666
jnelson@susmangodfrey.com

Kalpana Srinivasan
California State Bar No. 237460
SUSMAN GODFREY LLP
1900 Avenue of the Stars, Suite 1400
Los Angeles, CA 90067
Telephone: (310) 789-3100
Facsimile: (310) 789-3150
ksrinivasan@susmangodfrey.com

Ian Gore
Washington State Bar No. 54519
Kemper Diehl
Washington State Bar No. 53212
Bianca Rey
Washington State Bar No. 62422
SUSMAN GODFREY LLP
401 Union Street, Suite 3000
Seattle, Washington 98101
Telephone: (206) 516-3880
Facsimile: (206) 516-3883
igore@susmangodfrey.com
kdiehl@susmangodfrey.com
brey@susmangodfrey.com

Ravi Bhalla
New York State Bar No. 5748223
Andrew Nassar
New York State Bar No. 6162226
SUSMAN GODFREY LLP

One Manhattan West, 50th Floor
New York, NY 10001
Telephone: (212) 336-8330
Facsimile: (212) 336-8340
rbhalla@susmangodfrey.com
anassar@susmangodfrey.com

Of Counsel:
Claire Abernathy Henry
Texas State Bar No. 24053063
Andrea Fair
Texas State Bar No. 24078488
MILLER FAIR HENRY PLLC
1507 Bill Owens Parkway
Longview, TX 75604
Telephone: (903) 757-6400
Fax: (903) 757-2323
claire@millerfairhenry.com
andrea@millerfairhenry.com

Counsel for Plaintiff Advanced Memory Technologies, LLC

/s/ John Yin
John Yin