Carl Sechen

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Research Interests

My research interests center primarily on the design and computer-aided design of digital and analog integrated circuits. Ongoing projects include the design of secure ICs that cannot be reverse engineered. We are continuing the development of the TRAP (TRAnsistor-level Programmable) fabric that implements 10X more logic in the same area compared to lookup-table based FPGAs and eFPGAs, making it the first practical approach to secure hardware via IC redaction.

Education

Ph.D., Electrical Engineering, University of California, Berkeley, 1986
Thesis: *Placement and Global Routing of Integrated Circuits Using Simulated Annealing*
Advisor: Prof. Alberto Sangiovanni-Vincentelli
M.S., Electrical Engineering, Massachusetts Institute of Technology, 1977
Advisor: Prof. Stephen Senturia
B.E.E., Electrical Engineering, University of Minnesota, 1975

Employment history

Professor, University of Texas at Dallas August 15, 2005 – present
Professor, University of Washington July 1999 – August 14, 2005
Associate Professor, University of Washington July 1992 – June 1999
Associate Professor, Yale University July 1990 – June 1992
Assistant Professor, Yale University July 1986 – June 1990

University Administrative Positions

Director of ECS Tech Support Services, UTD, June 2012 – February 2014

Honors and Awards

- *Best Paper Award* at the 2017 IEEE PhD Research in Microelectronics and Electronics Conference (PRIME), for the paper "Improved Lagrangian Relaxation-based Gate Size and VT Assignment for Very Large Circuits", Bariloche, Argentina, February 2017.
- Nominated for a *Best Paper Award* for: "A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration", *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 27-31, 2017, Lausanne, Switzerland.
- Nominated for UTD's President's Teaching Excellence Award for Graduate/Professional Instruction, 2020.
- Received the *Graduate Teaching Excellence Award* from the ECE Department at UT Dallas, May 2024.
- Received the *Distinguished Teaching Award* for the Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2014.
- Received the *Distinguished Teacher of the Year* Award, Dept. of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2008.
- Elected *IEEE Life Fellow* in 2002

- Elected a Fellow of Asia-Pacific Artificial Intelligence Association (AAIA)
- Received the *Outstanding Research Advisor* Award, Department of Electrical Engineering, University of Washington, 2002.
- Received the *Best Project Award*, NSF Center for the Design of Digital and Analog ICs (CDADIC), July 2002.
- Received the Semiconductor Research Corporation's 2001 *SRC Inventor's Recognition Award*
- Received the Semiconductor Research Corporation's 1994 *SRC Technical Excellence Award*
- Received the Semiconductor Research Corporation's 1988 *SRC Inventor's Recognition Award*

Graduated Ph.D. Students

1. Kai-Win Lee (Yale May 1990) "Global Routing of Row-Based Integrated Circuits".
2. Dahe Chen (Yale May 1992) "Mickey: A Graph-Based Macro-Cell Global Router".
3. Mark Chiang (Yale May 1992) "A Perturbation Approach to the Symbolic Analysis of Analog Circuits".
4. William Swartz (Yale May 1993) "Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits".
5. Ted Stanion (Yale May 1994) "Boolean Algorithms for Combinational Synthesis and Test Generation".
6. Kalapi Roy (University of Washington June 1994) "A Timing-Driven Multi-Way Partitioning System for Integrated Circuits and Multi-Chip Systems".
7. Jer-Jaw Hsu (University of Washington December 1994) "Fully Symbolic Analysis of Large Analog Integrated Circuits".
8. Wern-Jieh Sun (University of Washington December 1994) "Effective and Efficient Placement for Very Large Integrated Circuits".
9. Qicheng Yu (University of Washington March 1995) "Approximate Symbolic Analysis of Large Analog Integrated Circuits".
10. Bingzhong David Guan (University of Washington August 1996) "Automatic Layout Generation of Static CMOS Combinational Cells and Blocks".
11. Eugene Liu (University of Washington, December 1997) "Global Routing and Pin Assignment for Multi-layer Chip-level Layout".
12. Hsiao-Ping Tseng (University of Washington, December 1997) "Detailed Routing Algorithms for VLSI Circuits".
13. Gin Yee (University of Washington, June 1999) "Dynamic Logic Design and Synthesis Using Clock-Delayed Domino".
14. Tyler Thorp (University of Washington, December 1999), "Design and Synthesis of Dynamic Circuits".
15. Tatjana Serdar (University of Washington, December 2000), "Automatic Datapath Tile Placement and Routing".
16. Jovanka Ciric (University of Washington, August 2001), "Boolean Matching and Level-Based Technology Mapping".
17. Yi Han (University of Washington, December 2004), "A High-Performance CMOS Programmable Logic Core for System-on-Chip Applications".
18. Hiran Tennakoon (University of Washington, August 2005), "Efficient and Accurate Gate Sizing With Piecewise Convex Delay Models".
19. Miodrag Vujkovic (University of Washington, March 2006), "Efficient Fully-Automated, Refinement-Based Power-Delay Optimization Design Flow for Standard Cell Designs".
20. Kian Hour (Alfred) Chong (University of Washington, June 2006), "Self-Calibrating Differential Output Prediction Logic".
21. Xinyu (Sunny) Guo (University of Washington, June 2006), " A High-Throughput Divider Based on Output Prediction Logic".
22. Sheng Sun (University of Washington, August 2006), "High Performance and Energy Efficient Adder Design".
23. Mohammad Rahman (UT-Dallas, December 2011), "Power and Leakage Minimization for Digital ICs".
24. Chiu-Wei Pan (UT-Dallas, August 2012), "High Speed and Power Efficient Compression of Partial Products".
25. Zhao Wang (UT-Dallas, October 2012), "Accurate Wire Endpoint Delay Estimation".

26. Akshay Sridharan (UT-Dallas, October 2015), “STARK: Synchronous to Asynchronous Redesign Kit”.
27. Anitha Yella (UT-Dallas, January 2016), “Power Optimization in ICs”.
28. Meisam Roshan (UT-Dallas, September 2016), “A MEMS-Assisted Dual-Resonator Temperature-to-Digital Converter”.
29. Huihua (Helen) Huang (UT-Dallas, May 2018), “A 0.1ps Resolution Coarse-Fine Time-to-Digital Converter with 2.21ps Single-Shot Precision”.
30. Jingxiang (Amelie) Tian (UT-Dallas, December 2019), “Transistor-level Programmable Fabric”.
31. Bo Hu (UT-Dallas, March 2021), “Thermal-Aware Placement and High Level Synthesis For Hardware Security”.
32. Lubaba Nahar, (UT-Dallas, July 2022), “CAD Tools for PCB Reverse Engineering and IC Interconnect”.
33. Qiongdan (Olivia) Huang, (UT-Dallas, July 2022), “Toward Accurate Timing Analysis of Transistor-Level Programmable Fabric”.
34. Xiangyu Xu, (UT-Dallas, December 2022), “Routing Methods for Transistor-level Programmable Fabrics”.
35. Vibhav Kumarswami Salimath, (UT-Dallas, December 2023), “Standard Cell Library Composition Optimization for Advanced Process Nodes”.
36. Apurva Jain, (UT-Dallas, January 2024), “Addressing Testing and Verification Challenges in a Transistor-level Programmable Fabric”.
37. Thomas Broadfoot (UT-Dallas, December 2025), “Transistor-level Programmable Fabrics for Cost-Effective IC Redaction”.

Current Ph.D. Students

1. Jinkun Feng, Ph.D. expected 06/27
2. Nazia Bushra, Ph.D. expected 06/28

Teaching Activities

Yr	*Qtr*	*Course*	*Brief Title, Credits, #students*	*Stud. Opin. Survey*
1992	Aut	EE538	Auto Layout, 4 credits, 20 students	4.38/4.08
1993	Win	EE356	Analog ICs, 4 credits, 55 students	3.21/3.00
1993	Spr	EE535	VLSI Design, 4 credits, 25 students	4.27/4.47
1993	Sum	EE332	Analog ICs, 5 credits, 35 students	3.57/3.48
1993	Aut	EE538	Auto Layout, 4 credits, 15 students	3.60/3.50
1993	Aut	EE332	Analog ICs, 5 credits, 40 students	3.93/3.90
1994	Win	EE433	Analog MOS ICs, 4 credits, 65 students	3.96/4.08
1994	Spr	EE476	Digital ICs, 5 credits, 55 students	3.89/3.89
1994	Aut	EE538	Auto Layout, 4 credits, 15 students	3.63/3.63
1994	Aut	EE433	Analog MOS ICs, 4 credits, 55 students	4.32/4.30
1995	Win	EE476	Digital ICs, 5 credits, 85 students	3.75/3.85

1995	Spr	EE473	Adv. Analog MOS, 5 credits, 45 students	3.53/3.59
1995	Aut	EE476	Digital ICs, 5 credits, 85 students	4.40/4.20
1996	Win	EE535	VLSI Design, 4 credits, 55 students	4.10/4.00
1996	Spr	EE538	Auto Layout, 4 credits, 15 students	4.30/4.50
1996	Aut	EE476	Digital ICs, 5 credits, 125 students	3.40/3.40
1997	Win	EE477	Custom Dig ICs, 4 credits, 45 students	4.30/4.10
1997	Win	EE541	Auto Layout, 4 credits, 20 students	4.70/4.70
1997	Spr	EE535	VLSI Design, 4 credits, 20 students	3.83/4.00
1997	Aut	EE476	Digital ICs, 5 credits, 60 students	3.88/3.89
1998	Win	EE477	Custom Dig ICs, 4 credits, 60 students	3.66/3.61
1998	Spr	EE476	Digital ICs, 5 credits, 60 students	3.39/3.50
1998	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.57/3.94
1998	Aut	EE476	Digital ICs, 5 credits, 35 students	4.15/4.50
1999	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.00/3.94
1999	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.79/4.13
1999	Aut	EE476	Digital ICs, 5 credits, 50 students	4.70/4.70
2000	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.53/4.27
2000	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	4.35/4.44
2000	Aut	EE476	Digital ICs, 5 credits, 125 students	4.20/4.19
2001	Win	EE477	VLSI II, 5 credits, 75 students	4.30/4.37
2001	Win	EE525	VLSI II, 5 credits, 25 students	4.25/4.50
2001	Spr	EE526	VLSI III, 4 credits, 50 students	4.35/4.50
2001	Aut	EE476	VLSI I, 5 credits, 150 students	4.1/4.2
2002	Win	EE477	VLSI II, 5 credits, 75 students	4.1/4.1
2002	Win	EE525	VLSI II, 5 credits, 25 students	4.1/4.1
2002	Spr	EE526	VLSI III, 4 credits, 50 students	3.6/3.3
2002	Aut	EE476	VLSI I, 5 credits, 150 students	3.7/3.6
2003	Win	EE477	VLSI II, 5 credits, 55 students	3.4/3.8
2003	Win	EE525	VLSI II, 5 credits, 25 students	3.6/3.3
2003	Spr	EE526	VLSI III, 4 credits, 32 students	3.3/3.5
2003	Aut	EE476	VLSI I, 5 credits, 30 students	4.5/4.6
2004	Win	EE477	VLSI II, 5 credits, 12 students	3.2/3.7
2004	Win	EE525	VLSI II, 5 credits, 7 students	2.2/2.2
2004	Spr	EE526	VLSI III, 4 credits, 12 students	3.2/3.2
2004	Aut	EE476	VLSI I, 5 credits, 65 students	3.8/3.9
2005	Fall	EE6325	VLSI Design, 3 units, 42 students	4.4/4.6
2006	Spr	EE7325	Advanced VLSI Design, 3 units, 20 students	4.5/4.3
2006	Fall	EE6325	VLSI Design, 3 units, 66 students	4.4/4.2
2007	Spr	EE7325	Advanced VLSI Design, 3 units, 15 students	4.5/4.2
2007	Fall	EE6325	VLSI Design, 3 units, 40 students	4.8/4.6
2008	Spr	EE4325	Introduction to VLSI Design, 40 students	3.5/3.4
2008	Spr	EE7325	Advanced VLSI Design, 3 units, 19 students	4.6/4.4
2008	Sum	EE6325	VLSI Design, 3 units, 36 students	4.0/3.7
2008	Fall	EE6325	VLSI Design, 3 units, 40 students	4.1/4.1
2009	Spr	EE4325	Introduction to VLSI Design, 22 students	4.2/3.9
2009	Spr	EE7325	Advanced VLSI Design, 3 units, 37 students	3.7/3.6
2009	Sum	EE6325	VLSI Design, 3 units, 17 students	4.1/4.0
2009	Fall	EE6325	VLSI Design, 3 units, 67 students	4.3/4.0
2010	Spr	EE4325	Introduction to VLSI Design, 25 students	4.6/4.5
2010	Spr	EE7325	Advanced VLSI Design, 3 units, 35 students	4.4/4.4
2010	Sum	EE6325	VLSI Design, 3 units, 17 students	4.7/4.5

2010	Sum	EE3320	Digital Circuits, 3 units, 17 students	4.1/3.8
2010	Fall	EE6325	VLSI Design, 3 units, 77 students	4.4/4.2
2011	Spr	EE4325	Introduction to VLSI Design, 37 students	4.0/4.1
2011	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.2/4.2
2011	Sum	EE6325	VLSI Design, 3 units, 16 students	4.14
2011	Sum	EE3320	Digital Circuits, 3 units, 26 students	4.13
2011	Fall	EE6325	VLSI Design, 3 units, 91 students	4.73
2012	Spr	EE4325	Introduction to VLSI Design, 27 students	4.25
2012	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.90
2012	Sum	EE6325	VLSI Design, 3 units, 35 students	4.46
2012	Sum	EE3311	Electronic Circuits, 3 units, 22 students	3.62
2012	Fall	EE6325	VLSI Design, 3 units, 144 students	4.76
2013	Spr	EE6325	VLSI Design, 3 units, 41 students	4.85
2013	Spr	EE4325	Introduction to VLSI Design, 7 students	4.75
2013	Sum	EE7325	Advanced VLSI Design, 3 units, 67 students	4.38
2013	Sum	EE3311	Electronic Circuits, 3 units, 46 students	4.58
2013	Fall	EE6325	VLSI Design, 3 units, 129 students	4.64
2014	Spr	EE4325	Introduction to VLSI Design, 25 students	4.69
2014	Sum	EE7325	Advanced VLSI Design, 3 units, 74 students	4.53
2014	Sum	EE3311	Electronic Circuits, 3 units, 40 students	4.75
2014	Fall	EE6325	VLSI Design, 3 units, 139 students	4.79
2015	Spr	EE4325	Introduction to VLSI Design, 25 students	4.72
2015	Sum	EE7325	Advanced VLSI Design, 3 units, 49 students	4.25
2015	Sum	EE3311	Electronic Circuits, 3 units, 25 students	4.80
2015	Fall	EE6325	VLSI Design, 3 units, 142 students	4.73
2016	Spr	EE4325	Introduction to VLSI Design, 25 students	3.67
2016	Sum	EE7325	Advanced VLSI Design, 3 units, 70 students	4.77
2016	Sum	EE3311	Electronic Circuits, 3 units, 35 students	4.88
2016	Fall	EE6325	VLSI Design, 3 units, 140 students	4.79
2017	Spr	EE4325	Introduction to VLSI Design, 32 students	4.10
2017	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2017	Sum	EE3311	Electronic Circuits, 3 units, 32 students	4.50
2017	Fall	EE6325	VLSI Design, 3 units, 80 students	4.82
2018	Spr	EE4325	Introduction to VLSI Design, 32 students	4.63
2018	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2018	Fall	EE6325	VLSI Design, 3 units, 80 students	4.88
2019	Spr	EE4325	Introduction to VLSI Design, 43 students	4.33
2019	Sum	EE3311	Electronic Circuits, 3 units, 61 students	4.23
2019	Fall	EE6325	VLSI Design, 3 units, 60 students	4.84
2020	Spr	EE4325	Introduction to VLSI Design, 33 students	4.75
2020	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.30
2020	Fall	EE6325	VLSI Design, 3 units, 43 students	4.65
2020	Fall	EE7325	Advanced VLSI Design, 3 units, 16 students	4.17
2021	Spr	EE4325	Introduction to VLSI Design, 41 students	3.40
2021	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.20
2021	Fall	EE6325	VLSI Design, 3 units, 72 students	4.75
2022	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.17
2022	Spr	EE4325	Introduction to VLSI Design, 46 students	4.13
2022	Sum	EE3311	Electronic Circuits, 3 units, 29 students	-----
2022	Fall	EE6325	VLSI Design, 3 units, 111 students	4.20
2023	Spr	EE4325	Introduction to VLSI Design, 48 students	4.00

2023	Fall	EE6325	VLSI Design, 3 units, 76 students	4.00
2024	Fall	EE6325	VLSI Design, 3 units, 42 students	4.75

Course Development

U. of Washington: EE 541 Automatic Layout of Integrated Circuits (first offering: Fall 1992)
U. of Washington: EE 477 Custom Digital CMOS Circuit Design (first offering: Win 1997)
U. of Washington: EE 476 Digital Integrated Circuit Design (first offering: Spr 1994)

Yale University: EE 880 Automatic Layout of Integrated Circuits.
Yale University: EE 877 Introduction to VLSI CAD Tools
Yale University: EE 878 Introduction to VLSI Synthesis
Yale University: EE 988 Analog Integrated Circuits II

Journal Publications

1. A. Fowler, S. Mohammed, M. Shihab, T. Broadfoot, P. Beerel, C. Sechen, and Y. Makris, "A TRAP for SAT: On the Imperviousness of a Transistor-Level Programmable Fabric to Satisfiability Attacks", *Transactions on Cryptographic Hardware and Embedded Systems* 2025, Issue 2.
2. A. Jain, T. Broadfoot, Y. Makris and C. Sechen, "Modeling Bidirectional Switches for Enabling Logic Equivalence Checking in a Transistor-Level Programmable Fabric," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2025, Vol. 44, No. 1, pp. 385-389.
3. Roshan, C. Sechen, *et al*., "A MEMS-Assisted Temperature Sensor with 20μK Resolution, Conversion Rate of 200S/s and FOM of 0.04pJK", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 185-197, January 2017.
4. Z. Wang, X. He, and C. Sechen, "A New Approach for Gate-Level Delay-Insensitive Asynchronous Logic", *Journal of Circuits, Systems & Signal Processing*, October 2014.
5. Z. Wang, C. Pan, Y. Song, and C. Sechen, "High-Throughput Digital IIR Filter Design", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 2, pp. 15-27, April 2014.
6. C. Pan, Z. Wang and C. Sechen, "High Speed and Power Efficient Compression of Partial Products and Vectors," *Journal of Algorithms and Optimization (JAO)*, Vol. 1, No. 1, pp. 39-54, October 2013.
7. Z. Wang and C. Sechen, "A New Algorithm for Accurate Wire Endpoint Delay Estimation", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 1, pp. 30-43, Jan. 2014.
8. M. Rahman, H. Tennakoon, and C. Sechen, "Library-Based Cell-Size Selection using Extended Logical Effort", *IEEE Trans. on Computer-Aided Design*, July 2013.
9. H. Tennakoon and C. Sechen, "Non-convex Gate Delay Modeling and Delay Optimization," *IEEE Trans. on Computer-Aided Design*, Vol. 27, No. 9, September 2008, pp. 1583-1594.
10. Don Bouldin, Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees, Carl Sechen, and Wayne Dai, "Automated Design of Digital Signal Processing ASICs," *IEEE Circuits and Devices*, vol. 20, n. 4, pp. 17-21, July 2004.

11. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *IEEE Trans. on Computer-Aided Design*, Vol. 22, No. 5, May 2003, pp. 535-544.
12. T. Thorp and C. Sechen, "Design and Synthesis of Dynamic Circuits," *IEEE Transactions on VLSI Systems*, Vol. 11, No. 1, February 2003, pp. 141-149.
13. G. Hoyer, G. Yee and C. Sechen, "Locally-Clocked Pipelines and Dynamic Logic," *IEEE Transactions on VLSI Systems*, Vol. 10, No. 1, February 2002, pp. 58-62.
14. H. P. Tseng, L. Scheffer and C. Sechen, "Timing- and Crosstalk-Driven Area Routing," *IEEE Transactions on Computer Aided Design*, vol. 20, no. 4, pp. 528-544, April 2001.
15. G. Yee and C. Sechen, "Clock-Delayed Domino for Dynamic Circuit Design," *IEEE Transactions on VLSI Systems*, Vol. 8, No. 4, August 2000, pp. 425-431.
16. L. Liu and C. Sechen, "Multi-layer Chip-level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
17. L. Liu and C. Sechen, "Multi-layer Pin Assignment for Macro Cell Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
18. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Router for Standard Cell Circuits using CTM Cells," *IEEE Transactions on Computer Aided Design*, Vol. 18, No. 10, October 1999.
19. W. Sun and C. Sechen, "A Parallel Standard Cell Placement Algorithm," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 11, November 1997, pp. 1342-1357.
20. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 10, October 1997, pp. 1073-1081.
21. Q. Yu and C. Sechen, "Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis," *Int. Journal of Circuit Theory and Applications*, Vol. 24, No. 5, pp. 597-603, 1996.
22. Q. Yu and C. Sechen, "A Unified Approach to the Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 8, pp. 656-669, August 1996.
23. K. Roy and C. Sechen, "A Timing-Driven Partitioning System for Multiple FPGAs," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 309-328, 1996.
24. K. Roy, D. Guan and C. Sechen, "A Sea-of-Gates Style FPGA Placement Algorithm," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 293-307, 1996.
25. T. Stanion, D. Bhattacharya, and C. Sechen, "An Efficient Method for Generating Exhaustive Test Sets," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 12, December 1995.
26. W. Sun and C. Sechen, "Efficient and Effective Placement for Very Large Circuits," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 3, pp. 349-359, March 1995.
27. J. J. Hsu and C. Sechen, "DC Small Signal Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I*, Vol. 41, No. 12, pp. 817-828, December 1994.
28. T. Stanion and C. Sechen, "Boolean Division and Factorization Using Binary Decision Diagrams," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, September 1994, pp. 1179-1184.
29. C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro Cell Integrated Circuits Using Simulated Annealing," *Int. J. Computer-Aided VLSI Design*, vol. 2, no. 2, 1990, pp. 127-158.

30. C. Sechen, D. Braun, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *IEEE J. of Solid State Circuits*, vol. 23, n. 2, pp. 410- 420, April 1988.
31. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *IEEE J. of Solid State Circuits*, vol. 20, n. 2, April 1985, pp. 510-522.
32. C. Sechen, "An Improved Lock Layer Transistor," *Solid State Electronics*, Vol. 21, No. 6, June 1978, pp. 911-913.
33. S. Senturia and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Transactions on Electron Devices*, vol.24, no.9, p.1207, September 1977.
34. S. Senturia, C. Sechen, and J. Wishneusky, "The Charge-Flow Transistor: A New MOS Device," *Applied Physics Letters*, Vol. 30, No. 2, Jan. 1977, p. 106-108.

Fully Refereed Conference Proceedings

1. A. Fowler, C. Sechen and Y. Makris, "An SMT-Based Method for Identifying State-Holding Elements in Extracted Netlists", International Test Conference (ITC), Sept. 21-26, 2025, San Diego, CA.
2. S. Chaitaligajanan, A. Fowler, B. Schaefer, Y. Makris, C. Sechen, M. Zaman, and R. Narumi, "Trusted, Assured and Cyber-secure Microelectronics", Proc. GOMACTech-25 (Government Microcircuit Applications & Critical Technology Conference), March 17-20, 2025, Pasadena, CA.
3. T. Broadfoot, Y. Makris, and C. Sechen, "TRAPv4: A Transistor-Level Programmable Fabric for "Blacked-Out" ASIC Redaction", Proc. GOMACTech-25 (Government Microcircuit Applications & Critical Technology Conference), March 17-20, 2025, Pasadena, CA.
4. A. Jain, T. Broadfoot, Y. Makris, and C. Sechen, "Testing a Transistor-Level Programmable Fabric: Challenges and Solutions", *Proc. IEEE VLSI Test Symposium (VTS)*, Tempe, AZ, April 22-24, 2024.
5. A. Jain, T. Broadfoot, Y. Makris, and C. Sechen, "Quo Vadis Signal? Automated Directionality Extraction for Post-Programming Verification of a Transistor-Level Programmable Fabric", *Proc. Design Automation and Test in Europe (DATE) Conference*, Antwerp, Belgium, April 17-19, 2023.
6. V. Salimath and C. Sechen, "Essential Standard Cell Library Composition", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
7. L. Nahar, J. Rajendran, Y. Makris and C. Sechen, "MTBoM: Metal Trace to Bill of Materials Generation for PCB Reverse Engineering", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
8. Q. Huang, J. Tian, T. Broadfoot, X. Xu, B. Hu, M. Shihab, A. Jain, V. Salimath, Y. Makris and C. Sechen, "Toward Accurate Timing Analysis for Transistor-Level Programmable Fabrics", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
9. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.

10. V. Salimath and C. Sechen, "Optimal Standard Cell Library Composition for 7nm", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.
11. M. Shihab, B. Ramanidharan, S. Tellakula, G. Reddy, J. Tian, C. Sechen, and Y. Makris, "ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric", *Proc. 8th IEEE VLSI Test Symposium (VTS'20)*, April 5-8, 2020, San Diego, CA.
12. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "A Transistor-Level Fabric for Design Obfuscation", *Proc. Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, March 16-19, 2020, San Diego, CA.
13. B. Hu, M. Shihab, Y. Makris, B. Schaefer and C. Sechen, "An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs", *Proc. Design Automation in Europe Conference (DATE)*, March 9-13, 2020, Grenoble, France.
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26. H. Huang and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS", *2014 Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.
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141. C. Sechen and D. Chen, "An Improved Objective Function for Mincut Circuit Partitioning," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 7-10, 1988, Santa Clara, CA, pp. 502-505.
142. C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro/Custom Cell Circuits Using Simulated Annealing," *Proc. of the 25th Design Automation Conference (DAC)*, June 1988, Anaheim, CA, pp. 73-80.
143. C. Sechen and K. W. Lee, "An Improved Simulated Annealing Algorithm for Row-Based Placement," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 478-481.
144. C. Sechen, "Average Interconnection Length Estimation for Random and Optimized Placements," *Proc. of Int. Conf. on Computer-Aided Des. (ICCAD)*, Nov. 9-13, 1987, Santa Clara, CA, pp. 190-193.
145. J. Burns, A. Casotto, M. Igusa, F. Marron, F. Romeo, A. Sangiovanni-Vincentelli, C. Sechen, H. Shin, G. Srinath, and H. Yaghutiel, "Mosaico: An Integrated Macro-Cell Layout System," in C. Sequin, editor, *Proc. of VLSI '87*, Vancouver, Canada, August, 1987.
146. C. Sechen and A. Sangiovanni-Vincentelli, "TimberWolf3.2: A New Standard Cell Placement and Global Routing Package," *Proc. 23rd Design Automation Conference (DAC)*, June 29-July 2, 1986, Las Vegas, NV, pp. 432-439.
147. D Braun, C. Sechen, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1986, Rochester, NY.
148. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Simulated Annealing Research at Berkeley," *Proc. Int. Conf. on Computer Design (ICCD)*, October 1984, Rye Brook, NY.
149. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, May 1984, Rochester, NY.
150. M. Huberman, S. Senturia, and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Device Research Conference (DRC)*, Cornell University, June 1977.
151. S. Senturia and C. Sechen, "The Charge-Flow Transistor," *IEEE Int. Electron Devices Meeting (IEDM)*, Washington DC, Dec. 1976.
152. L. Liu and C. Sechen, "A Multi-Layer Chip-Level Global Router," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
153. L. Liu and C. Sechen, "Multi-Layer Pin Assignment for Macro Cell Circuits," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.

154. G. Yee and C. Sechen, "Clock-Delayed Domino for Adder and Combinatorial Logic Design," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
155. B. Guan and C. Sechen, "Efficient Standard Cell Generation When Diffusion Strapping is Required," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
156. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Channel Router Based on a Combined Constraint Graph and Tile Expansion Approach," *Proc. of the Fifth ACM/SIGDA Physical Design Workshop*, April 15-17, 1996, Reston, Virginia.
157. J. J. Hsu and C. Sechen, "The Sifting Approach to Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 211-230.
158. Q. Yu and C. Sechen, "Approximate Symbolic Analysis of Large Analog Integrated Circuits," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 241-259.
159. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *Proc. of the Third International Workshop on Symbolic Methods and Applications to Circuit Design (SMACD)*, Sevilla, Spain, October 6-7, 1994, pp. 261-277.
160. T. Stanion and C. Sechen, "Maximum Projections of Don't Care Conditions in a Boolean Network," *Proc. of the International Workshop on Logic Synthesis*, Lake Tahoe, CA, May 23-26, 1993.
161. W. Sun, K. Roy, and C. Sechen, "Fast, High-Quality Placement for Large Circuits," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.
162. K. Roy, D. Guan and C. Sechen, "FPGA MCM Partitioning and Placement," *Proc. of the 4th ACM/SIGDA Physical Design Workshop*, Lake Arrowhead, CA, April 19-21, 1993.
163. T. Stanion and C. Sechen, "Incremental and Simultaneous Computation of Satisfiability and Observability Don't Cares," *Proc. IEEE/ACM Winter VLSI Workshop*, Jan. 25-27, 1993, Asilomar, CA.
164. R. Weier and C. Sechen, "TimberWolfAR: An Arbitrary Design Rule Multi-Layer Area Router," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.
165. W. Swartz and C. Sechen, "A Generalized Row-Based Global Router for FPGAs," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.
166. K. Roy and C. Sechen, "A Timing Driven N-Way Chip Partitioner," *Int. Workshop on Layout Synthesis*, May 18-21, 1992, MCNC, Research Triangle Park, NC.
167. K. W. Lee and C. Sechen, "A Global Router for Sea-of-Gates Circuits," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
168. D. Chen and C. Sechen, "Mickey: A New Macro Cell Global Router", *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
169. W. Swartz and C. Sechen, "New Algorithms for the Placement and Routing of Macro Cells," *Proc. Int. Workshop on Layout Synthesis*, Research Triangle Park, NC, May 8-11, 1990.
170. C. Sechen, "TimberWolfSG: A Sea-of-Gates Layout Package," *Proc. of SRC Workshop on Sea-of-Gates Design*, Sept. 22-23, 1988, Berkeley, CA.
171. C. Sechen, "A Global Router for the Sea-of-Gates Environment," *Proc. IFIP Workshop on Physical Design of Sea-of-Gates VLSI*, August 11-12, 1988, Lenggries, Germany.
172. J. Lam, J. M. Delosme, and C. Sechen, "A New Simulated Annealing Schedule for Row-Based Placement," *Proc. IEEE International Workshop on Placement and Routing*, May 10-13, 1988, Research Triangle Park, NC.

173. F. Romeo, C. Sechen, and A. Sangiovanni-Vincentelli, "Some Theoretical Results on Simulated Annealing and TimberWolf: A Placement and Routing Package for the Layout of Integrated Circuits," *Proc. Workshop on Statistical Physics in Engineering and Biology*, IBM T.J. Watson Research Center, Yorktown Heights, NY, April 1984.

Books Authored

Carl Sechen, **Placement and Global Routing of Integrated Circuits Using Simulated Annealing**, 278 pages, Kluwer Academic Publishers, Boston, MA, 1988.

Patents

C. Sechen, Y. Makris, T. Broadfoot, "Field Programmable Transistor Arrays", US Patent 11,362,662 issued June 14, 2022. (New patent relative to the below two.)

C. Sechen, Y. Makris, G. Reddy, J. Tian, "Field Programmable Transistor Arrays", US Patent 10,855,285 B2, issued 1 December 2020. (New patent relative to the 2019 one.)

C. Sechen, Y. Makris, G. Reddy, J. Tian, "Field Programmable Transistor Arrays", US Patent No. 10,511,308, issued December 17, 2019.

C. Sechen, L. McMurchie, G. Yee and T. Thorp, "Method of High Performance CMOS Design", US Patent No. 6,549,038 issued April 15, 2003.

Research Funding

- "Cost-Effective IC Redaction through a CMOS/MRAM Transistor-Level Programmable Fabric", PI: C. Sechen, Co-PIs: J. Friedman, Y. Makris. NSF CHEST I/UCRC. June 1, 2024 – August 31, 2025. $125,000.

- "Cost-Effective IC Redaction through a CMOS/MRAM Transistor-Level Programmable Fabric", PI: C. Sechen, Co-PIs: J. Friedman, Y. Makris. NSF CHEST I/UCRC. June 1, 2023 – May 31, 2024. $100,000.

- NSF Proposal: SaTC: TTP: Medium: Hardware Intellectual Property Protection through Hybrid ASIC/TRAP Integrated Circuit Design, 8/15/22-7/31/26, $900,000 (PI: Y. Makris, co-PI: C. Sechen).

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer,

ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $150,000. NSF CHEST I/UCRC. March 1, 2022 – February 28, 2023.

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, Dr. William Swartz Jr., ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $150,000. NSF CHEST I/UCRC. March 1, 2021 – February 28, 2022.

- IBM / NSWC CW3085860, "Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP)," 10/8/20-3/20/21, $143,576 (PI: Y. Makris, co-PI: C. Sechen)

- "DEFENSEWERX-Advanced Microelectronics Design & Prototype Challenge", Benjamin Carrion Schaefer, Yiorgos Makris, Carl Sechen, William Swartz Jr., InertialWave/Defensewerks/Air Force, August 1, 2020 – November 30, 2020, $200,000.

- "CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)", Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, Dr. William Swartz Jr., ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, $100,000. NSF CHEST I/UCRC. March 1, 2020 – February 28, 2021.

- "TRAP-based Circuit Obfuscation Development and Evaluation", PIs: Y. Makris, B. Schaefer, W. Swartz and C. Sechen, The Boeing Company, $149,914, February 1, 2020 – August 31, 2020.

- "DEFENSEWERX-Advanced Microelectronics Design & Prototype Challenge", Benjamin Carrion Schaefer, Yiorgos Makris, Carl Sechen, William Swartz Jr., InertialWave/Defensewerks/Air Force, Nov. 15, 2019 – Mar. 15, 2020, $87,980.

- "OpenROAD: Foundations and Realizations of Open, Accessible Design", co-PIs Carl Sechen and William Swartz, Defense Advanced Research Products Agency (DARPA) IDEA Program, May 1, 2018 through April 30, 2019, $287,341.

- CSR: "Small: Host-Assisted Software-Defined Solid-State Disk", PI: Carl Sechen, October 1, 2014 – September 30, 2019, $265,067.

- TerraSwarms Research Center, DARPA/SRC FCRP research center based at UC Berkeley, Jan. 15, 2013 – Jan. 14, 2014, co-PI: Carl Sechen portion: $100,000.

- "Optimal Gate Size and Vt Selector, and Innovative Approach to Path-Based Timing Analysis", PI: Carl Sechen, Texas Instruments, Jan. – Dec., 2012, $50,000. Current status: completed.

- "Optimal Gate Size and Vt Selection", Texas Instruments, Wireless Division, Jan. – Dec., 2011, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2011, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2010, $75,000, PI: Carl Sechen.

- "Low Power HD Video Decoder Research", Texas Instruments, Wireless Division, Jan. – Dec., 2010, $50,000, PI: Carl Sechen.

- "Power Minimization Research", Texas Instruments, ASIC Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Low Power HD Video Decoder Research", Texas Instruments, Wireless Division, Jan. – Dec., 2009, $50,000, PI: Carl Sechen.

- "Power Optimization and Circuit Hardening", MARCO Focus Center Research Program (C2S2), $155,000, September 2005 – August 2008.

- "Ultra High Performance Digital Circuit Design and Synthesis", National Science Foundation (NSF), $80,000, (Jan. 2006 – Dec., 2008).

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $80,000, Jan. – Dec., 2008.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2008.

- "Power Minimization and Yield Optimization in Digital IC's", Carl Sechen, Semiconductor Research Corporation TxACE, $150,000, August 2007 – July 2010.

- "Analog-to-Digital Converter based on Time-to-Digital Conversion", Carl Sechen, Texas Instruments, $40,000, Sep. 2007 – Aug. 2008.

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $45,000, Jan. – Dec., 2007.

- "Three-Transistor Memory Cell Research", Carl Sechen, Texas Instruments, $35,000, Jan. – Dec., 2007.

- "Power Minimization Research", Carl Sechen, Texas Instruments, ASIC Division, $37,000, Jan. – Dec., 2007.

- "Low Power HD Video Decoder Research", Carl Sechen, Texas Instruments, Wireless Division, $30,000, Sept. – Dec., 2006.

- "DRAM-Density SRAM", Carl Sechen, Honeywell, $105,000, January 2006 – April 2007.

- "RADHARD by Design," DARPA/Boeing, Phase I, $45,000 (co-PI, my portion), November 2004 – August 2005).

- "CLASS: Clockless Logic, Analysis, Synthesis, and Systems," DARPA/Boeing, Phase II/III, $709,000 (co-PI, my portion), (Sept. 2004 – August 2006).

- "MSP Phase 2: Digital IC Optimization Techniques," DARPA/Boeing, $285,000 (co-PI, my portion), (September 2004 – August 2006).

- "Power Optimization and Circuit Hardening," MARCO FCRP C2S2 Center, $100,000, PI (Oct. 04 – Sep. 05).

- "High Speed and Low Power Digital IC Design," NSF ITR, $350,000 (my portion) co-PI, (Sept. 00 – Aug. 05).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $110,000, PI (Sep 04 – Aug 05).

- "High Speed & Low Power Digital Circuit Synthesis and Design," MARCO FCRP C2S2 Center, $100,000, PI (Oct. 03 – Sep. 04), full indirect.

- "CLASS: Clockless Logic, Analysis, Synthesis, and Systems," DARPA/Boeing, Phase I, $135,000 (co-PI, my portion), (Oct. 2003 – May 2004).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $105,000, PI (Sep 03 – Aug 04), full indirect.

- "Low Power Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 03 – Aug 04), no indirect.

- "Reconfigurable RF, Analog and Digital Array for Radiation-Hardened Wireless Communication Circuits," DARPA/SPAWAR, $150,000, PI (April 03 – May 04), full indirect.

- "Development of Pulse-Based Logic," DARPA, $100,000, PI (March 03 – May 04), full indirect.

- "High Performance and Power Efficient Digital IC Optimization Techniques," MSP Phase 1: Boeing/DARPA, $400,000, PI (April 02 – August 03), full indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (May 03 – April 04).

- "High Performance Digital IC Design," MARCO/DARPA C2S2 Center, $170,000, PI (Jan. 01 – Aug. 03), full indirect.

- "Ultra High Performance Digital Circuit Design and Synthesis," National Science Foundation, $180,000, PI, (Sep 02 – Aug 05).

- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, $95,000, PI (Sep 02 – Aug 03), full indirect.

- "PLL Design, Clock Generation and High-Speed/Low-Power DSP-block Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000, PI (Sep 02 – Aug 03), no indirect.

- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 02 – Feb 03), no indirect.

- "High Performance Digital IC Design," Semiconductor Research Corporation (SRC), June 1, 2000 – May 31, 2003, $525,000 (full indirect).

- "High Performance Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), $60,000 (no indirect), PI (Sep. 00 - Aug. 01).
- Unrestricted grant, Intel Corporation, $60,000, PI (Mar 01 – Feb 02).
- Unrestricted grant, Sun Microsystems, $30,000, PI (Feb 00 – Mar 01).
- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 99 – Sep. 00).
- Unrestricted grant, Cadabra, Inc., $20,000, PI (Feb. 00 – Mar 01).
- "Ultra High Speed Digital Circuit Synthesis and Layout NSF Center for the Design of Analog and Digital ICs (CDADIC), $55,000 (no indirect), PI (Sep. 99-Aug. 00).
- "Ultra High Speed Digital Circuit Synthesis and Layout", National Science Foundation, $255,000 (full indirect), PI (Sep 99 – Aug 02).
- "Ultra High Speed Digital Circuit Synthesis and Layout", Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).
- "Ultra High Speed Digital Circuit Synthesis and Layout", , Semiconductor Research Corporation, $154,000 (full indirect), PI (Mar 99-Mar 00).
- "Synthesis of Ultra High Speed Random Logic Blocks", Semiconductor Research Corporation, $132,000, PI (Mar 98-Feb 99).
- "Ultra High Speed Digital Circuit Synthesis and Layout", NSF Center for the Design of Analog and Digital ICs (CDADIC), $65,000, PI (Sep. 98-Aug. 99).
- "Radiation-hard High Speed Digital Circuit Synthesis", Boeing, $35,000, PI (Sep. 98-Aug. 99).
- "Datapath Cell Layout", Compaq/Digital Equipment, $25,000, PI (Sep. 98 – Aug. 99).
- Unrestricted grant, Sun Microsystems, $8,000, PI (June 99 – May 00).
- Unrestricted grant, Compaq Computer Corp., $25,000, PI (Oct. 98 – Sep. 99).
- Unrestricted grant, Sun Microsystems, $30,000, PI (Jan. 99 – Dec. 99).
- Unrestricted grant, TimberWolf Systems, Inc., $20,000, PI (Apr. 98 – Mar. 99).
- Unrestricted grant, Sun Microsystems, Inc., $8,000, PI (June 98 – May 99).
- Various industrial gifts, $65,000, PI (Sep 97-Aug 98).
- "High Speed Digital Circuit Design", NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 97-Aug. 98).

- “Automatic Layout Research”, Semiconductor Research Corporation, $132,000, PI (Mar 97-Feb 98).
- Various industrial gifts, $112,000, PI (Sep 96-Aug 97).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $50,000, PI (Sep. 96-Aug. 97).
- “Symbolic Analysis of Large Analog Circuits”, National Science Foundation, $90,000, PI (Sep 94-Aug 97).
- “Automatic Layout Research”, Semiconductor Research Corporation, $132,000, PI (Mar 96-Feb 97).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 95-Aug. 96).
- Various industrial gifts, $117,000, PI (Sep 95-Aug 96).
- “Automatic Layout Research”, Semiconductor Research Corporation, $132,000, PI (Mar 95-Feb 96).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 94-Aug. 95).
- Various industrial gifts, $208,000, PI (Sep 94-Aug 95).
- “Automatic Layout Research”, Semiconductor Research Corporation, $144,000, PI (Mar 94-Feb 95).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 93-Aug. 94).
- Various industrial gifts, $343,000, PI (Sep 93-Aug 94).
- “Automatic Layout Research”, Semiconductor Research Corporation, $140,000, PI (Mar 93-Feb 94).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), $45,000, PI (Sep. 92-Aug. 93).
- Various industrial gifts, $312,000, PI (Sep 92-Aug 93).
- “Automatic Layout Research”, Semiconductor Research Corporation, $140,000, PI (Mar 92-Feb 93).
- Various industrial gifts, $306,000, PI (Sep 91-Aug 92).
- Yale University, Various Industrial Gifts, $1.65 million, PI (1986-1992).

Conference Service Activities

- Session Chairman for the Design Automation and Test in Europe Conference, 2012-2014.
- Session Chairman for the IEEE Design Automation Conference, 1987, 1990, 1991, 1997.
- Session Chairman for the International Symposium on Physical Design, 1997, 1998.
- Session Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1988, 89, 90, 91, 92.
- Session Chairman for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989, 1990, 1991, 1992, 1993, 1998.
- Elected Chairman for the Placement and Floorplanning sub-committee for the 2004 Design Automation Conference (DAC), 2004.
- Elected to the Placement and Floorplanning sub-committee for the 2003 Design Automation Conference (DAC), 2003.
- Elected Program Chair for the 2000 ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU).
- Elected chairman of the placement and floorplanning committee of the 2001 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 2000 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and routing committee of the 1999 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 1998 Int. Conf. On Computer Aided Design (ICCAD).
- Elected Program Chairman of the ACM Physical Design Workshop, Lake Arrowhead, CA, April 1993.
- Elected Chairman of the 1992 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- Elected Chairman of the 1990 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- CAD Track Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1991.

Service as a Referee

- Technical Program Committee for the Design Automation Conference, 2014, 2015.
- Technical Program Committee for the Design Automation and Test in Europe Conference, 2012-2014.
- Technical Program Committee for the IEEE Int. Symposium on VLSI Design, 2010-2011.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989-93, 98.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Design (ICCD), 1987-97.
- Technical Program Committee for the European Design and Test Conference (EDTC), 1995, 96, 97, 98.
- Technical Program Committee for the Design Automation and Test in Europe (DATE) Conference, 1998, 99, 00, 01, 02, 03.
- Technical Program Committee for ACM International Physical Design Workshop, 1996.
- Technical Program committee for the International Symposium on Physical Design, 1997, 98.
- Technical Program Committee for the International Workshop on Layout Synthesis, 1988, 90, 92.
- IEEE/ACM Design Automation Conference, 1986-1998.
- National Science Foundation, 1986-present.

- IEEE Transactions on Computer Aided Design, 1986-present.
- IEEE Transactions on VLSI Systems, 1992-present.
- ACM Transactions on Design Automation of Electronic Systems, 1995-present.

University Service

UTD

Academic Affairs Committee 2022-2024
Director of ECS Tech Support Services, June 2012 – February 2014
Information Technology Planning and Policy Committee, Sept. 1, 2016 – August 31, 2019

UW

Faculty Council on Research, 1994-1997
Faculty Senate, 2002-2004

Department Service

UTD

Chair of the TA Assignment Committee, Spring 2024-2025, and ongoing
Chair of Adhoc Committee for a possible promotion to Associate Professor with Tenure (Prof. Kanad Basu), 2024.
Chair of the Computer Resources Committee, ECE Dept., 2007-2021
Advisory Committee to TxACE (SRC Texas Analog Center of Excellence) 2008-2009
Chair of the Analog Search Sub-Committee, EE Dept., 2007-2008
Faculty Search Committee (computer engineering) 2010-11
Teaching Assistant (TA) Selection Committee, 2021-23

UW

Faculty Search Committee, 2005-2006
Group Chair, VLSI and Digital Systems Group, 1997-2005
Faculty Search Committee, 98-99.
Graduate Studies and Research Committee, 1992-93, 96-97, 97-98.
Group Chair, Electronics, 94-95.
Graduate Admissions Committee, Electrical Engineering Dept., 1992-93.
Qualifying Examination Subcommittee, 1992-93.
Computer Resources Committee, 1992-93.

Outside University Service

Selected by the NSF to serve as a panelist for (invited) full proposals submitted to the CISE Expeditions in Computing (Expeditions) program, NSF 08-568, April 6-7, 2010.

Selected by the NSF to serve on the 2008 proposal review panel (April 14-15, 2008) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2009 funding.

Selected by the NSF to serve on the 2007 proposal review panel (January 8-9, 2007) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2008 funding.

Selected by the NSF to serve on the 2005 proposal review panel (October 20-21, 2005) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2006 funding.

Selected by the NSF to serve on the 2004 proposal review panel (May 5-6, 2004) to review a number of proposals that have been submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2004 funding.

Selected by the NSF to serve on the 2002 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Selected by the NSF to serve on the 1999 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Co-Director of the NSF Center for the Design of Analog and Digital ICs (CDADIC), 1997-2005; this center provides about $450,000 annually to the University of Washington.

Professional Society Memberships

Eta Kappa Nu
Tau Beta Pi
Sigma Xi
IEEE Fellow
ACM