

ABSTRACT OF THE DISCLOSURE

An output terminal of a first boost circuit is connected to a second boost circuit. After the second boost circuit is started up, a boost clock frequency of the second boost circuit is reduced. A time required to start up the second boost circuit is reduced, and in addition, a current supply capability of the first boost circuit is increased after the second boost circuit is started up. When the second boost circuit is driven, output voltages of the first and second boost circuits are stably supplied without instantaneously changing the output voltage of the first boost circuit.

**UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)**

Mail Stop New Utility Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing is the patent application of:

**INVENTOR: Seiji YAMAHIRA
FOR: INTERNAL VOLTAGE GENERATING CIRCUIT**

Enclosed are:

- ☒ 19 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed of Japanese Patent Application No. **JP 2008-179566** filed July 9, 2008.
- ☒ 8 sheets of formal drawing.
- ☒ Information Disclosure Statement, Form PTO-1449 and references.

The filing fee has been calculated as shown below:

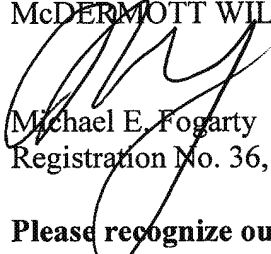
	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	7	-20	0	\$52.00	\$0.00
Independent Claims	3	-3	0	\$220.00	\$0.00
Multiple Dependent Claim(s)					\$0.00
Sheets of specification and drawing (\$260.00 for each 50 sheets in excess of 100)					\$0.00
Basic Filing Fee					\$330.00
Patent Search Fee					\$540.00
Patent Examination Fee					\$220.00
Late Filing Fee(Declaration)					\$0.00
Total of Above Calculations					\$1,090.00
Less ½ for Small Entity					\$0.00
English Translation Surcharge					\$0.00
Assignment & Recording Fee					\$0.00
Total Fee					\$1,090.00

Case Docket Number: 079195-0937

- ☒ Please charge my Deposit Account No. 500417 in the amount of **\$1,090.00**. A duplicate copy of this sheet is enclosed.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417 . A duplicate copy is enclosed.
- ☒ Any additional filing fees required under 37 CFR 1.16.
- ☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.
- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

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Date: July 2, 2009

WHAT IS CLAIMED IS:

1. An internal voltage generating circuit comprising:

a first boost circuit provided between a first voltage and a first terminal;

5 a second boost circuit provided between the first terminal and a second terminal;

a frequency dividing circuit configured to divide a first clock signal to be supplied
to the first boost circuit to generate a second clock signal; and

a buffer circuit configured to select and supply the first clock signal or the second
clock signal to the second boost circuit.

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2. The internal voltage generating circuit of claim 1, further comprising:

a clock comparing circuit configured to compare the first clock signal and the
second clock signal to output a control signal to the buffer circuit.

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3. An internal voltage generating circuit comprising:

a first charge pump circuit configured to generate a second voltage from a first
voltage;

a second charge pump circuit configured to generate a third voltage from the
second voltage;

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a frequency dividing circuit configured to divide a first clock signal to generate a
second clock signal; and

a buffer circuit configured to select the first clock signal or the second clock signal
and generate a third clock signal,

wherein the third clock signal is supplied to the second charge pump circuit.

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4. The internal voltage generating circuit of claim 3, wherein

a clock signal having substantially the same frequency as that of the first clock

signal is supplied to the first charge pump circuit.

5. The internal voltage generating circuit of claim 3, further comprising:

a comparison circuit configured to output a first control signal in accordance with

5 on the first clock signal and the second clock signal,

wherein the buffer circuit is controlled in accordance with the first control signal.

6. An internal voltage generating circuit comprising:

a first charge pump circuit configured to generate a second voltage from a first

10 voltage; and

a second charge pump circuit configured to generate a third voltage from the second voltage,

wherein a frequency of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal.

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7. The internal voltage generating circuit of claim 6, wherein

the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.

FIG. 1

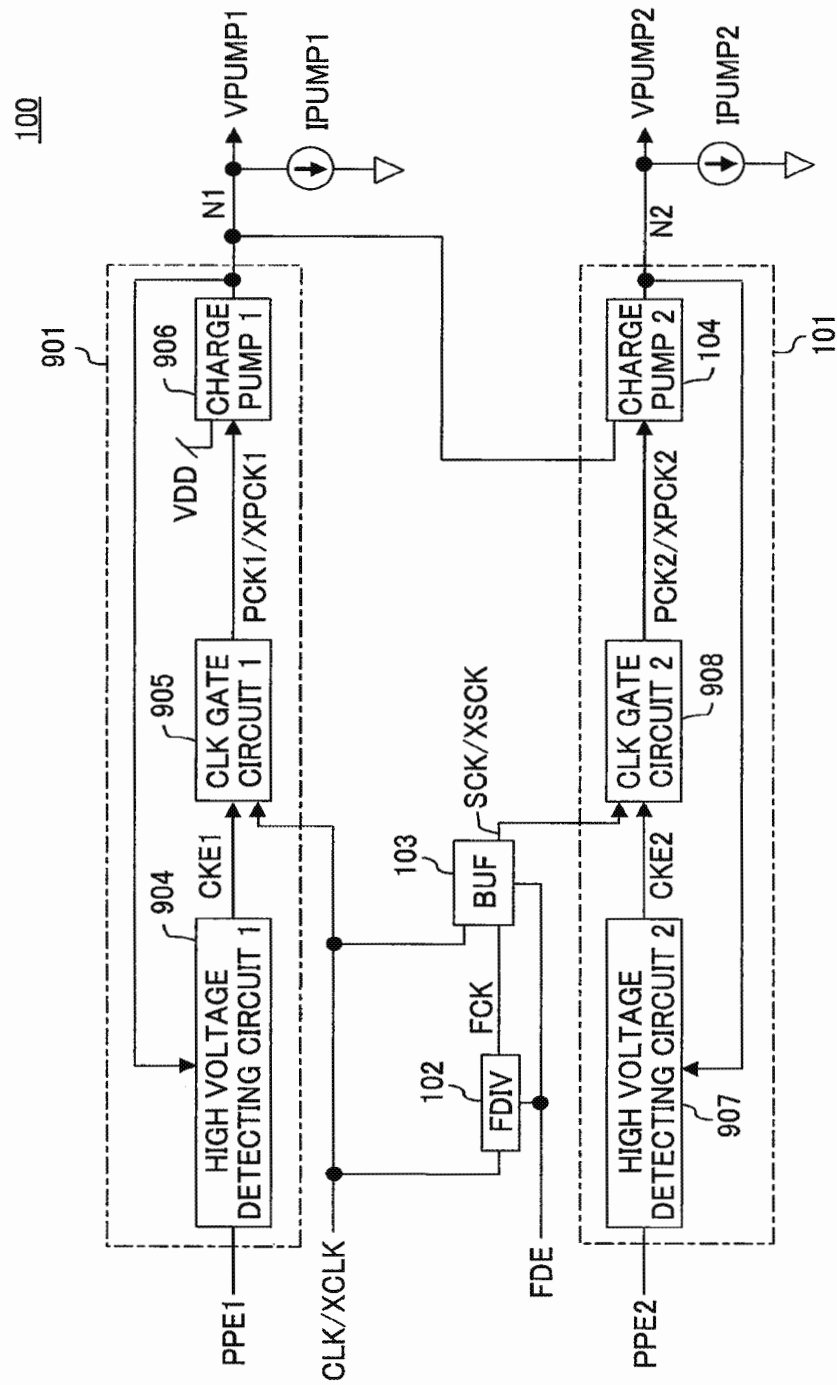


FIG. 2

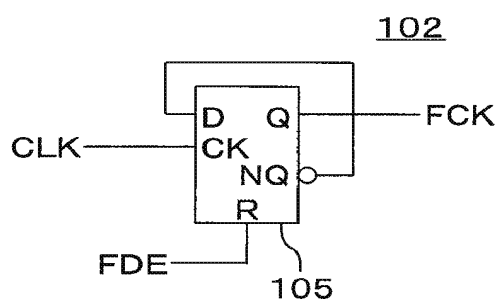


FIG. 7

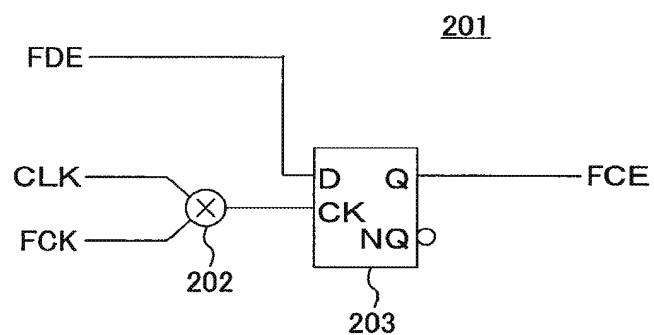


FIG. 3

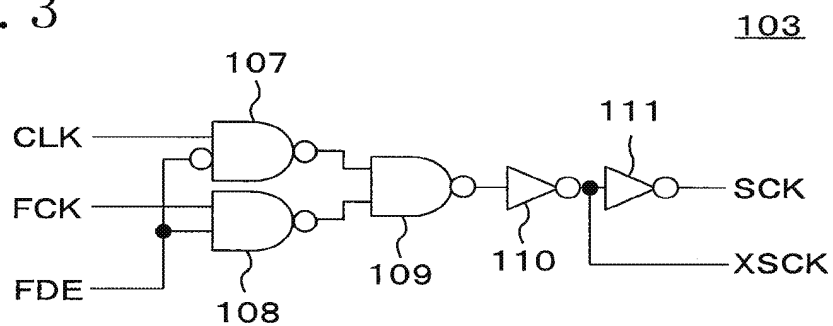


FIG. 4

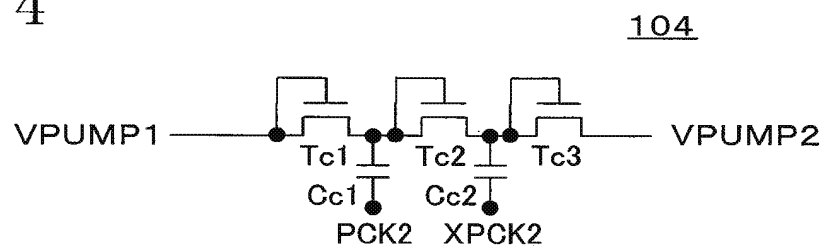


FIG. 5

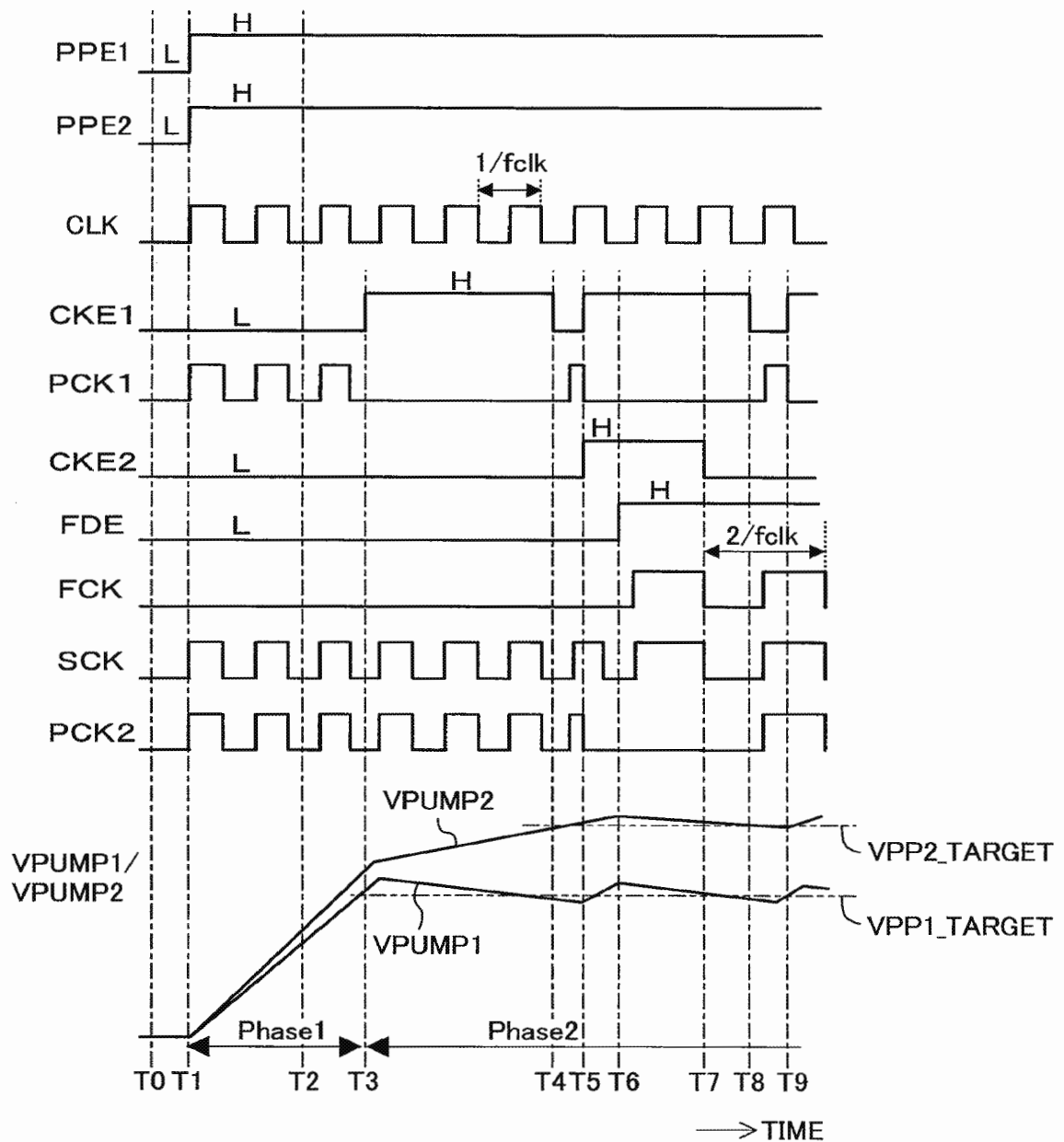


FIG. 6

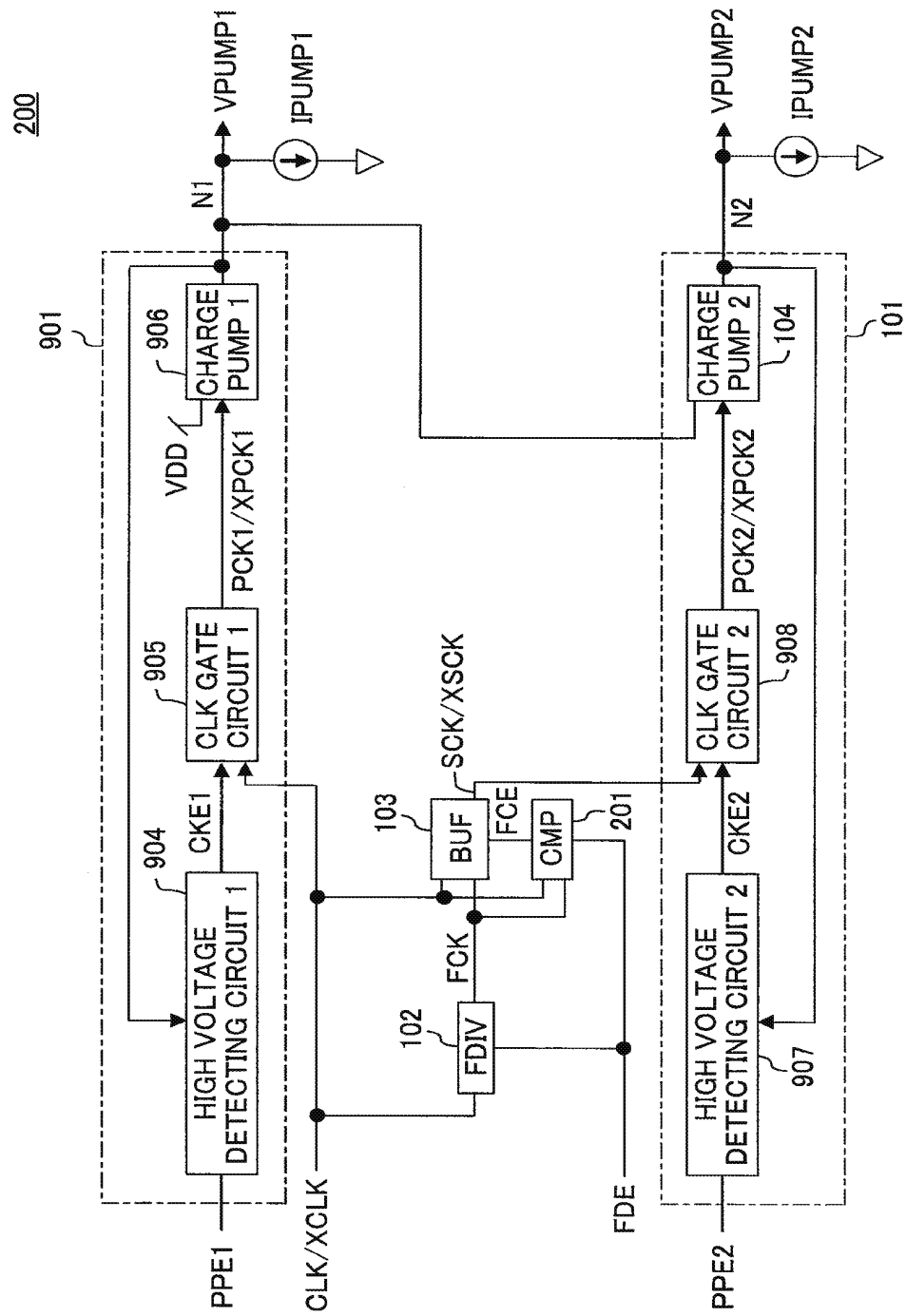


FIG. 8

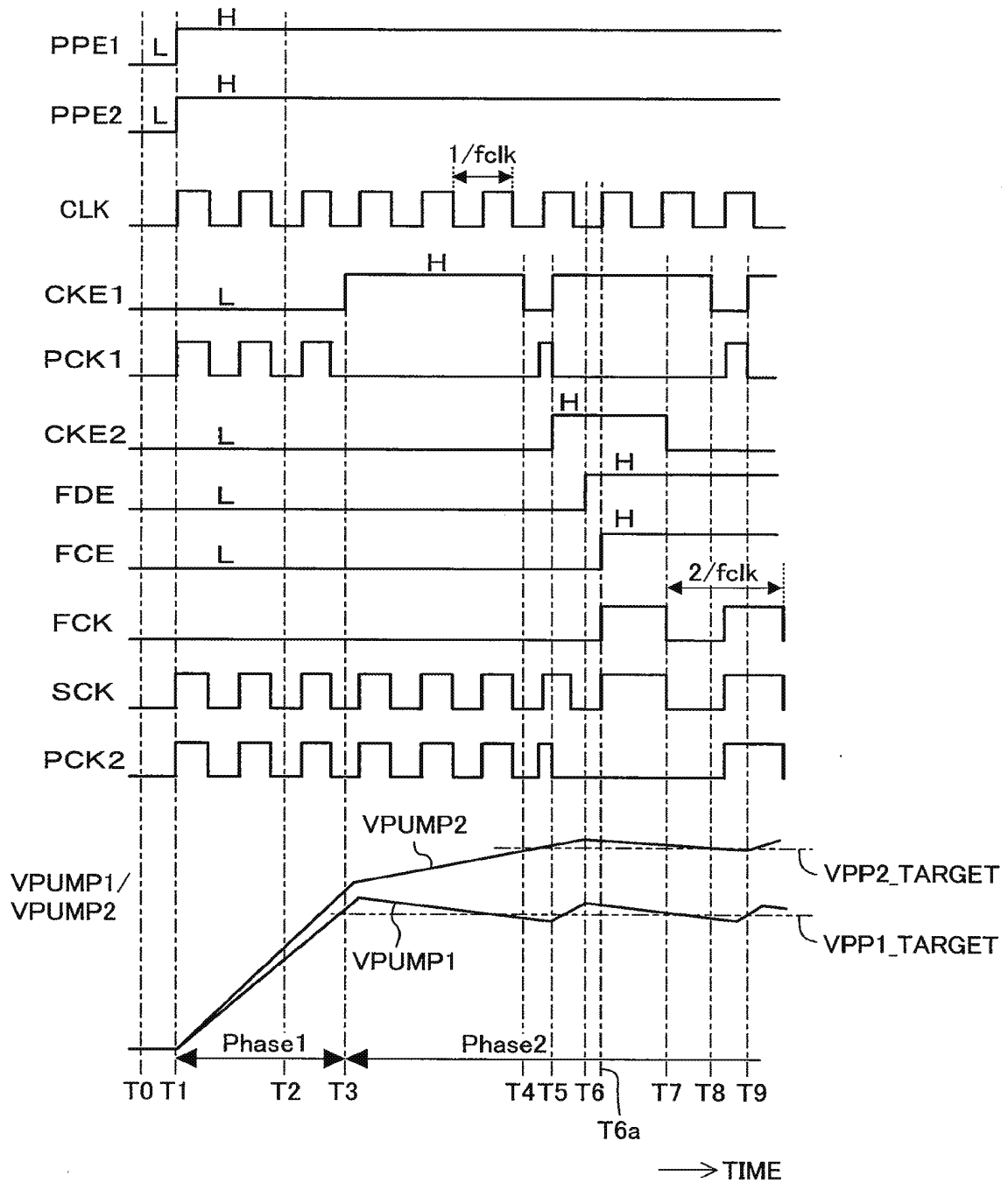


FIG. 9
PRIOR ART

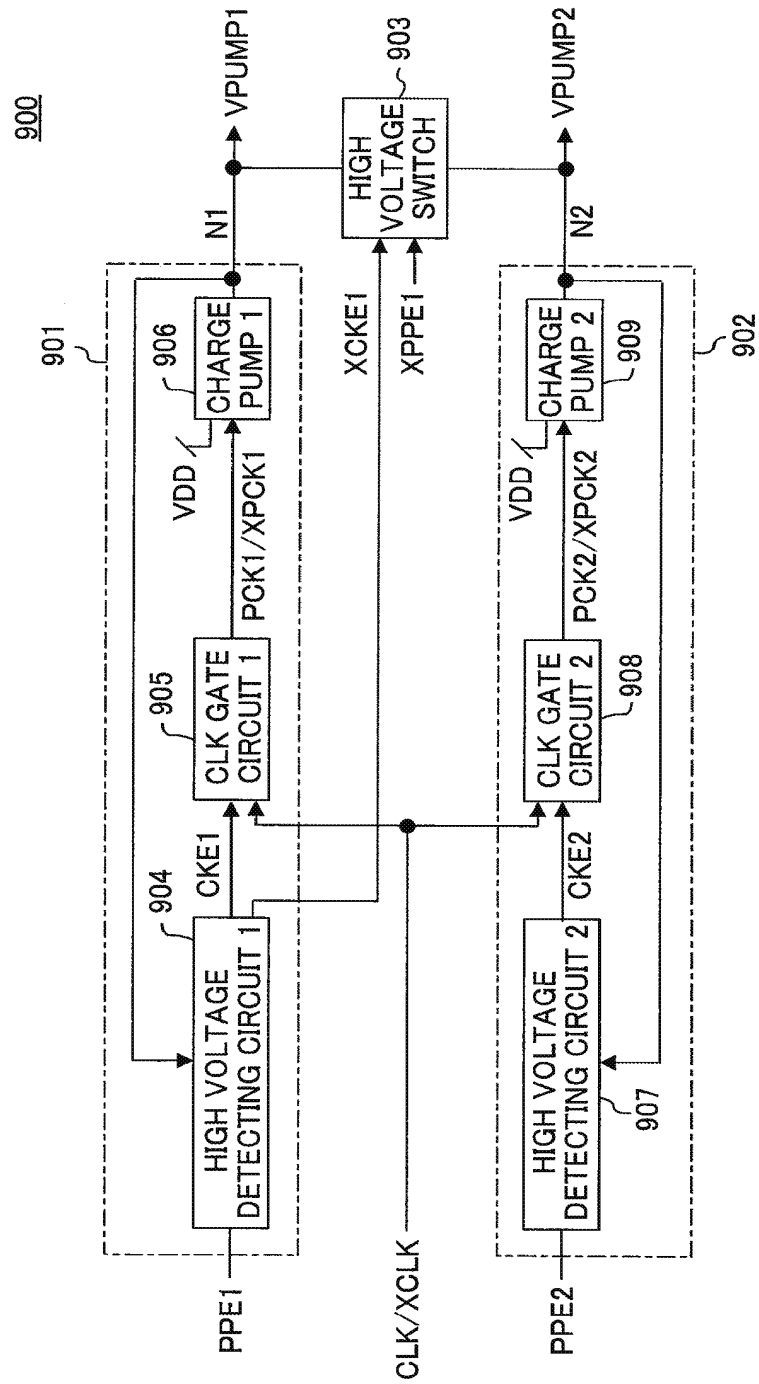


FIG. 10
PRIOR ART

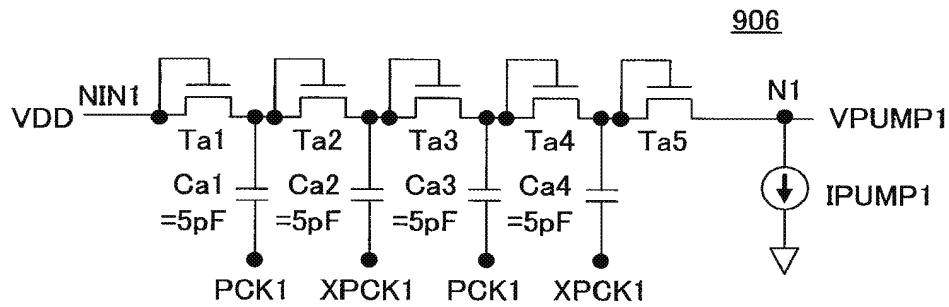


FIG. 11
PRIOR ART

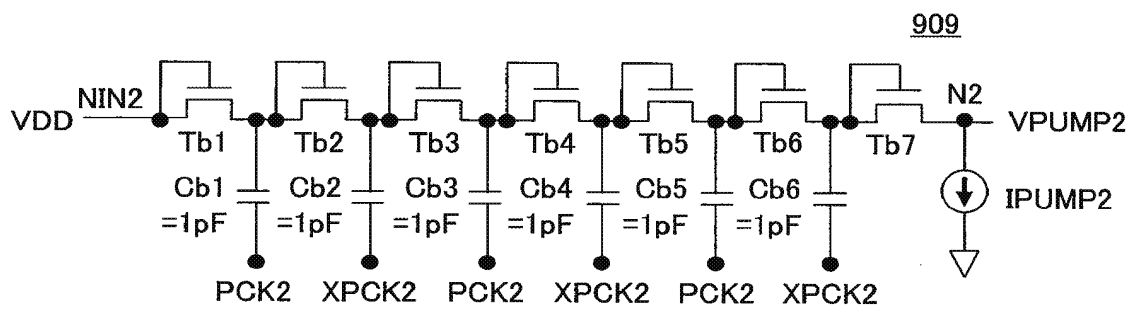
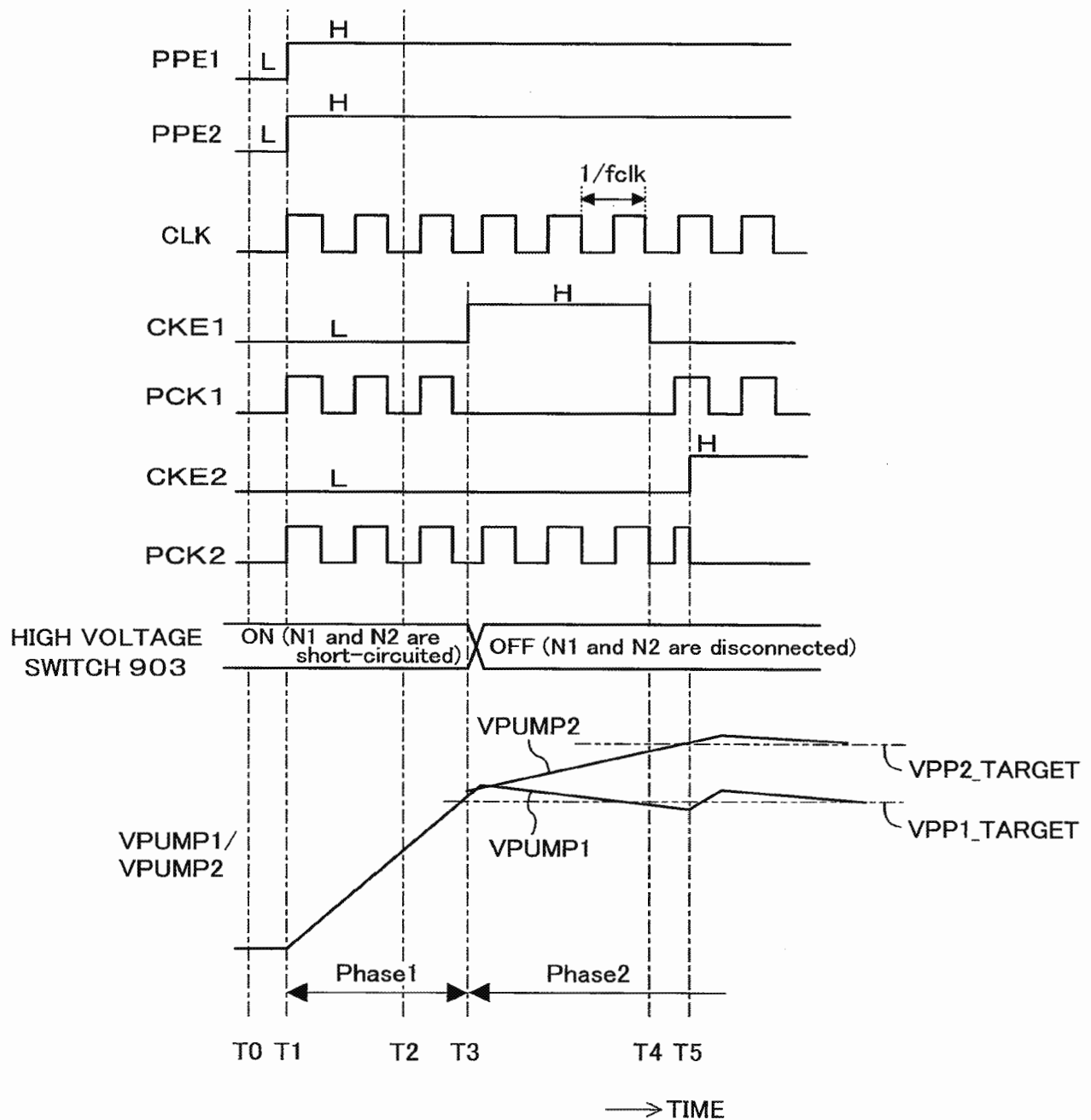


FIG. 12
PRIOR ART



Electronic Acknowledgement Receipt

EFS ID:	5636564
Application Number:	12497090
International Application Number:	
Confirmation Number:	5747
Title of Invention:	INTERNAL VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Seiji YAMAHIRA
Customer Number:	53080
Filer:	Michael E. Fogarty/Margaret Barham
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	079195-0937
Receipt Date:	02-JUL-2009
Filing Date:	
Time Stamp:	15:14:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1090
RAM confirmation Number	1587
Deposit Account	500417
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	P05300501_DEC_079195-0937.pdf	129201	no	2
			16e373dc2a215cbba05129e55a7a46c3f31918b3		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	P05300501_DRW_079195-0937.pdf	118642	no	8
			a207449b2363218de6ac49d6ee730bc079975a1b		
Warnings:					
Information:					
3	Transmittal Letter	P05300501_IDS_079195-0937.pdf	81958	no	3
			18a2d33b6720c2c2b02ac9b6b6802e13e366b6af		
Warnings:					
Information:					
4		P05300501_SPEC_CLAIMS_ABS T_079195-0937.pdf	817694	yes	19
			9b33b4e95d12c0408509bbe2f138a0f149a29567		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	16	
	Claims		17	18	
	Abstract		19	19	
Warnings:					
Information:					
5	Transmittal of New Application	P05300501_TRN_079195-0937.pdf	60654	no	2
			341ec5fc77fef2737ea4d93aab2a2b4e4def7b30		
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	32857	no	2
			c8f260b0615b48291d79e114cb86786d0807e177		
Warnings:					
Information:					
Total Files Size (in bytes):			1241006		

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		INTERNAL VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Seiji YAMAHIRA		
Filer:		Michael E. Fogarty/Margaret Barham		
Attorney Docket Number:		079195-0937		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Filing Date: 07/02/09

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/497,090	
APPLICATION AS FILED – PART I					OTHER THAN SMALL ENTITY	
(Column 1)		(Column 2)		SMALL ENTITY		OR
FOR	NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A		N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A		N/A		N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A		N/A
TOTAL CLAIMS (37 CFR 1.16(i))	7	minus 20 =		x\$26		x\$52
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *		x\$110		x\$220
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						
* If the difference in column 1 is less than zero, enter "0" in column 2.				195		390
				TOTAL		TOTAL
				1090		
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus	**		X	=
Independent (37 CFR 1.16(h))	*	Minus	***		X	=
Application Size Fee (37 CFR 1.16(s))						
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL		TOTAL
				ADD'T FEE		
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)
Total (37 CFR 1.16(i))	*	Minus	**		X	=
Independent (37 CFR 1.16(h))	*	Minus	***		X	=
Application Size Fee (37 CFR 1.16(s))						
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL		TOTAL
				ADD'T FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".						
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 079195-0937		SERIAL NO. Not Yet Assigned	
				APPLICANT Seiji YAMAHIRA			
				FILING DATE July 02, 2009		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 5,940,284	08-17-1999	TROUTMAN			
		US 5,999,475	12-07-1999	FUTATSUYA et al.			
		US 6,249,445 B1	06-19-2001	SUGASAWA			
		US 2004/0095806 A1	05-20-2004	OSAWA et al.			
		US 2007/0222498 A1	09-27-2007	CHOY et al.			
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Panasonic Ref*: P053005-01
 (* must be filled)
 Japan Firm Name: MAEDA PATENT OFFICE
 US Firm Name: MWE

Application Serial No. _____
 Japan Firm Ref: M09-P-216US1
 US Firm Ref: _____

DECLARATION AND POWER OF ATTORNEY FOR U.S. PATENT APPLICATION

(a) ☒ Original (b) ☐ Supplemental (c) ☐ Substitute (d) ☐ PCT (e) ☐ Design

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; and I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Title of Invention: INTERNAL VOLTAGE GENERATING CIRCUIT
--

which is described and claimed in (if the following box is not checked, the specification of which is attached hereto):

1. For use when submitting this Declaration prior to U.S. application filing date			
(f) ☒ the attached specification, or			
2. For use when submitting this Declaration after U.S. application filing date			
(g) ☐ the specification in the U.S. Application:	Application No. (if available)	filed on: (must be filled)	
	and with amendments (if applicable):	filed on	, or
3. For PCT-US national entry under 35 U.S.C. 371 (for use when filing this Declaration before and after the U.S. national entry date)			
(h) ☐ the specification in the International Application:	PCT Application No.	filed on: (PCT filing date)	
(Check here only for US national entry under 35 U.S.C. 371.)	and with amendments (if applicable):	filed on:	,

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above.

I acknowledge my duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a-d), §172, or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below, and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

(Foreign Priority Information)

COUNTRY	APPLICATION NO.	DATE OF FILING	PRIORITY CLAIMED
JAPAN	2008- 179566	July 9, 2008	YES

☐ Additional foreign or international application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States Provisional application(s) listed below.

(US Provisional Application Information)

APPLICATION NO.	U.S. PROVISIONAL APPLICATION FILING DATE

☐ Additional U.S. provisional application numbers are listed on a supplemental priority sheet attached hereto.

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(C) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Domestic Priority Information)

APPLICATION NO.	U.S. FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

☐ Additional U.S. or international application numbers are listed on a supplemental priority sheet attached hereto.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the attorneys and agents associated with the U.S. Patent and Trademark Office Customer Number identified below to prosecute this application including divisions, continuations and reissues thereof in the United States and to transact all business in the U.S. Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that customer number.

I hereby authorize the U.S. attorneys and agents associated with the customer number to accept and follow instructions from Panasonic Corporation and any affiliated or subsidiary company thereof, received via their corporate representatives and/or their foreign patent attorneys or agents, if any, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the U.S. attorneys or agents and myself.

Power of Attorney given to practitioners associated with, and direct Correspondence to:

CUSTOMER NUMBER 53080

I further declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

INVENTOR (s)

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Residence & Citizenship	CITY, STATE or COUNTRY Kyoto, Japan			CITIZENSHIP Japan
Post office address	ADDRESS c/o Panasonic Corporation, 1006, Oaza Kadoma, Kadoma-shi, Osaka, Japan 571-8501			

Full Name of Second Inventor	FIRST NAME	LAST NAME	SIGNATURE	DATE OF SIGNATURE
Residence & Citizenship	CITY, STATE or COUNTRY			CITIZENSHIP
Post office address	ADDRESS CITY STATE OR COUNTRY ZIP CODE			

Total of 2 pages are submitted.

INTERNAL VOLTAGE GENERATING CIRCUIT

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U.S.C. §119(a) on Patent Application No.
5 2008-179566 filed in Japan on July 9, 2008, the entire contents of which are hereby
incorporated by reference.

BACKGROUND

The present disclosure relates to an internal voltage generating circuit employing a
10 boost circuit.

In recent years, flash memories, which are non-volatile semiconductor memory
devices, require data read operation and data write operation which are performed using a
single power source voltage or a low power source voltage. To achieve this, a boost
circuit for supplying a boosted voltage or a negative boosted voltage during each operation
15 is required on a chip. Also, in CMOS processes, a voltage generated by a boost circuit is
used as a power source to improve characteristics of an analog circuit.

FIG. 9 shows a configuration of an internal voltage generating circuit 900 which is
disclosed in US Patent No. 5,999,475. The internal voltage generating circuit 900
includes a first boost circuit 901 which performs boost operation in synchronization with a
20 clock signal CLK and a complementary clock signal XCLK to output a first boosted
voltage VPUMP1 through a first output node N1, a second boost circuit 902 which
similarly performs boost operation in synchronization with the clock signals CLK and
XCLK to output a second boosted voltage VPUMP2 through a second output node N2, and
a high voltage switch circuit 903 which causes a path between the first output node N1 and
25 the second output node N2 to be in the conductive or non-conductive state.

The first boost circuit 901 includes a first high voltage detecting circuit 904 which,
when a first control signal PPE1 is activated, detects a voltage level of the first boosted

voltage VPUMP1 and sets a first sense signal CKE1 to be in the active or inactive state, a first CLK gate circuit 905 which outputs the clock signals CLK and XCLK as first boost clock signals PCK1 and XPCK1 in response to the first sense signal CKE1, and a first charge pump circuit 906 which performs boost operation in synchronization with the first boost clock signals PCK1 and XPCK1 to output the first boosted voltage VPUMP1 through the first output node N1.

The second boost circuit 902 includes a second high voltage detecting circuit 907 which, when a second control signal PPE2 is activated, detects a voltage level of the second boosted voltage VPUMP2 and sets a second sense signal CKE2 to be in the active or inactive state, a second CLK gate circuit 908 which outputs the clock signals CLK and XCLK as second boost clock signals PCK2 and XPCK2 in response to the second sense signal CKE2, and a second charge pump circuit 909 which performs boost operation in synchronization with the second boost clock signals PCK2 and XPCK2 to output the second boosted voltage VPUMP2 through the second output node N2.

The high voltage switch circuit 903 is controlled in accordance with a control signal XPPE1 complementary to the first control signal PPE1 and a sense signal XCKE1 complementary to the first sense signal CKE1. When the operation of the internal voltage generating circuit 900 is started, the high voltage switch circuit 903 causes a path between the first output node N1 and the second output node N2 to be in the conductive state. After a voltage level of the first output node N1 becomes at a predetermined voltage level, the high voltage switch circuit 903 causes the path between the first output node N1 and the second output node N2 to be in the non-conductive state.

FIG. 10 shows details of the first charge pump circuit 906. The first charge pump circuit 906 includes boost capacitances Ca1 to Ca4 which are boosted in synchronization with the first boost clock signals PCK1 and XPCK1, charge transfer transistors Ta1 to Ta4 which transfer boosted charge from the previous stage to the next stage, and a backflow preventing circuit Ta5 which prevents backflow of charge of the first output node N1

(four-stages-one-parallel arrangement).

FIG. 11 shows details of the second charge pump circuit 909. The second charge pump circuit 909 includes boost capacitances Cb1 to Cb6 which are boosted in synchronization with the second boost clock signals PCK2 and XPCK2, charge transfer transistors Tb1 to Tb6 which transfer boosted charge from the previous stage to the next stage, and a backflow preventing circuit Tb7 which prevents backflow of charge of the second output node N2 (six-stages-one-parallel arrangement).

Here, the first and second charge pump circuits 906 and 909 receive a power source voltage VDD through first and second input terminals NIN1 and NIN2 and generate the first and second boosted voltages VPUMP1 and VPUMP2, respectively. Output voltages and output currents of the first and second charge pump circuits 906 and 909 are assumed to have the following relationships. Specifically, it is assumed that the boosted voltage VPUMP1 of the first charge pump circuit 906 is lower than the boosted voltage VPUMP2 of the second charge pump circuit 909, and a current supply capability IPUMP1 of the first charge pump circuit 906 is larger than a current supply capability IPUMP2 of the second charge pump circuit 909. Moreover, for example, it is assumed that the boost capacitances Ca1 to Ca4 of the first charge pump circuit 906 each have a capacitance value of 5 pF, and the boost capacitances Cb1 to Cb6 of the second charge pump circuit 909 each have a capacitance value of 1 pF.

FIG. 12 shows operational waveforms in FIGS. 9 to 11. The boost operation will be briefly described with reference to FIG. 12.

(Time T0)

An initial state of the circuit is shown. Both the first control signal PPE1 and the second control signal PPE2 are at “L.”

(Time T1)

At time T1, the first control signal PPE1 transitions from “L” to “H.” In this case, the first boosted voltage VPUMP1 at the first output node N1 has not reached a first target

voltage VPP1_TARGET, and therefore, the first high voltage detecting circuit 904 outputs “L” as the first sense signal CKE1. As a result, the first CLK gate circuit 905 outputs the clock signals CLK and XCLK as the first boost clock signals PCK1 and XPCK1, and the first charge pump circuit 906 starts the boost operation in synchronization with the first boost clock signals PCK1 and XPCK1.

Similarly, the second control signal PPE2 transitions from “L” to “H.” In this case, the second boosted voltage VPUMP2 at the second output node N2 also has not reached a second target voltage VPP2_TARGET, and therefore, the second high voltage detecting circuit 907 outputs “L” as the second sense signal CKE2. As a result, the second CLK gate circuit 908 outputs the clock signals CLK and XCLK as the second boost clock signals PCK2 and XPCK2, and the second charge pump circuit 909 starts the boost operation in synchronization with the second boost clock signals PCK2 and XPCK2.

Thus, since the first sense signal CKE1 is at “L,” the sense signal XCKE1 complementary to this is at “H,” and therefore, the high voltage switch circuit 903 is in the conductive state. As a result, charging of the first output node N1 and the second output node N2 is started by the first charge pump circuit 906 and the second charge pump circuit 909.

(Time T2)

At time T2, while the high voltage switch circuit 903 remains in the conductive state, the first output node N1 and the second output node N2 are charged at the same rate by the first charge pump circuit 906 and the second charge pump circuit 909.

(Time T3)

At time T3, when the first boosted voltage VPUMP1 has reached the first target voltage VPP1_TARGET, the first sense signal CKE1 of the first high voltage detecting circuit 904 transitions from “L” to “H,” and the first CLK gate circuit 905 fixes the first boost clock signal PCK1 to “L” and its complementary signal XPCK1 to “H.” As a result, the boost operation of the first charge pump circuit 906 is stopped, and at the same time,

the high voltage switch circuit 903 transitions from the conductive state to the non-conductive state, so that the first output node N1 and the second output node N2 are disconnected.

During a “Phase1” period from time T1 to time T3 that the high voltage switch circuit 903 is in the conductive state, the second output node N2 of the second charge pump circuit 909 having the low current supply capability IPUMP2 is rapidly charged to the first target voltage VPP1_TARGET by the first charge pump circuit 906 having the high current supply capability IPUMP1. At time T3, the internal voltage generating circuit 900 transitions from the “Phase 1” period to a “Phase2” period during which the high voltage switch circuit 903 is in the non-conductive state, and the first charge pump circuit 906 and the second charge pump circuit 909 operate independently of each other. Thereafter, Phase 2 continues.

(Time T4)

At time T4, the second output node N2 is charged using only the second charge pump circuit 909 which has the boost capacitances Cb1 to Cb6 (=1 pF) which are 1/5 of the first boost capacitances Ca1 to Ca4 (=5 pF) of the first charge pump circuit 906. At time T5, the second output node N2 reaches the second target voltage VPP2_TARGET. During Phase2 that the second output node N2 is charged using only the second charge pump circuit 909 having the low current supply capability IPUMP2, a change in voltage per unit time at the second output node N2 is smaller than that during Phase1.

Thereafter, the logic of the first sense signal CKE1 is inverted, depending on the voltage level of the first output node N1, and the logic of the second sense signal CKE2 is inverted, depending on the voltage level of the second output node N2. Thus, the first charge pump circuit 906 and the second charge pump circuit 909 repeatedly perform intermittent operation to hold the respective voltage levels.

As described above, the first output node N1 of the first charge pump circuit 906 having the high current supply capability IPUMP1 and the second output node N2 of the

second charge pump circuit 909 having the low current supply capability IPUMP2 are controlled into the conductive/non-conductive state by the high voltage switch circuit 903. As a result, a voltage setup time for the second output node N2 of the second charge pump circuit 909 having the low current supply capability IPUMP2 can be reduced while preventing an increase in area of the internal voltage generating circuit 900.

SUMMARY

In the conventional internal voltage generating circuit 900, the second boost capacitances Cb1 to Cb6 of FIG. 11 may be increased only for the purpose of reducing the setup time of the second charge pump circuit 909 during Phase2, which disadvantageously increasing the number of circuits having poor use efficiency. Moreover, when the second boost capacitances Cb1 to Cb6 are increased so as to reduce the setup time, a smoothing capacitance is required at the second output node N2 of the second charge pump circuit 909 so as to prevent a ripple at the second output node N2, which disadvantageously increases the circuit area.

An overview of representative embodiments of the present disclosure will be briefly described as follows.

According to an aspect of the present disclosure, an internal voltage generating circuit includes a first boost circuit provided between a first voltage and a first terminal, a second boost circuit provided between the first terminal and a second terminal, a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal, and a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.

According to another aspect of the present disclosure, an internal voltage generating circuit includes a first charge pump circuit configured to generate a second voltage from a first voltage, a second charge pump circuit configured to generate a third voltage from the second voltage, a frequency dividing circuit configured to divide a first

clock signal to generate a second clock signal, and a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal. The third clock signal is supplied to the second charge pump circuit.

According to still another aspect, an internal voltage generating circuit includes a first charge pump circuit configured to generate a second voltage from a first voltage, and a second charge pump circuit configured to generate a third voltage from the second voltage. A frequency of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal.

According to the internal voltage generating circuit of the present disclosure, a boosted voltage of the first charge pump circuit in the first boost circuit is used as an input voltage to the second charge pump circuit having a low current supply capability in the second boost circuit. Each charge pump circuit is controlled by a high voltage detecting circuit. Moreover, by dividing a boost clock signal to be supplied to the second charge pump circuit, the setup time of the second charge pump circuit can be reduced. After the second charge pump circuit is set up, current supply can be concentrated into the output load of the first charge pump circuit, whereby a more stable boosted voltage and a more stable boosted current can be supplied.

Moreover, if a clock comparing circuit is further provided which compares the first clock signal and the second clock signal to control a timing of the output selection of the buffer circuit, the cycle of the boost clock signal is prevented from being temporarily reduced, by switching between the clock signal and the frequency-divided clock signal when both of them is at "H" or "L," whereby an increase in fluctuation of the output voltage can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a configuration of an internal voltage generating circuit according to a first embodiment of the present disclosure.

FIG. 2 is a circuit diagram showing a detailed example configuration of a frequency dividing circuit of FIG. 1.

FIG. 3 is a circuit diagram showing a detailed example configuration of a buffer circuit of FIG. 1.

5 FIG. 4 is a circuit diagram showing a detailed example configuration of a second charge pump circuit of FIG. 1.

FIG. 5 is a timing diagram showing operation of the internal voltage generating circuit of FIG. 1.

10 FIG. 6 is a block diagram showing a configuration of an internal voltage generating circuit according to a second embodiment of the present disclosure.

FIG. 7 is a circuit diagram showing a detailed example configuration of a clock comparing circuit of FIG. 6.

FIG. 8 is a timing diagram showing operation of the internal voltage generating circuit of FIG. 6.

15 FIG. 9 is a block diagram showing a configuration of an example conventional internal voltage generating circuit.

FIG. 10 is a circuit diagram showing a detailed example configuration of a first charge pump circuit of FIG. 9.

20 FIG. 11 is a circuit diagram showing a detailed example configuration of a second charge pump circuit of FIG. 9.

FIG. 12 is a timing diagram showing operation of the internal voltage generating circuit of FIG. 9.

DETAILED DESCRIPTION

25 Hereinafter, embodiments of the present disclosure will be described with reference to the accompanying drawings. Like parts are indicated by like reference symbols and will not be repeatedly described.

(First Embodiment)

<Configuration>

FIG. 1 shows a configuration of an internal voltage generating circuit 100 according to a first embodiment of the present disclosure. The internal voltage generating circuit 100 includes a first boost circuit 901 which is driven in accordance with a first control signal PPE1, and a second boost circuit 101 which is driven in accordance with a second control signal PPE2. The internal voltage generating circuit 100 outputs a first boosted voltage VPUMP1 through a first output node N1 of the first boost circuit 901, and outputs a second boosted voltage VPUMP2 through a second output node N2 of the second boost circuit 101. Reference symbol 102 indicates a frequency dividing circuit (FDIV) which receives a clock signal CLK having a frequency and generates a frequency-divided clock signal FCK having a frequency which is $1/N$ of that of the clock signal CLK (N is a natural number of two or more) in accordance with a control signal FDE. Reference symbol 103 indicates a buffer circuit (BUF) which outputs the clock signal CLK or the frequency-divided clock signal FCK as a clock signal SCK, and at the same time, outputs a clock signal XSCK complementary to the clock signal SCK, in accordance with the control signal FDE. Reference symbol 104 indicates a second charge pump circuit which receives the first boosted voltage VPUMP1 of the first boost circuit 901 as an input voltage and generates the second boosted voltage VPUMP2.

FIG. 2 shows an example configuration of the frequency dividing circuit 102. Reference symbol 105 indicates a flip-flop circuit which transitions to the reset state and outputs "L" through a terminal Q when the control signal FDE is at "L." On the other hand, a terminal NQ is a signal terminal complementary to the terminal Q. The flip-flop 105 outputs "H" through the terminal NQ when it is in the reset state. When the control signal FDE is at "H," the flip-flop 105 inverts the logic of the terminal Q, which is triggered by a rising edge of the clock signal CLK. As a result, the flip-flop 105 outputs the frequency-divided clock signal FCK whose frequency is a half of that of the clock

signal CLK. Specifically, when the frequency of the clock signal CLK is f_{clk} , the frequency of the frequency-divided clock signal FCK is $f_{clk}/2$.

FIG. 3 shows an example configuration of the buffer circuit 103. Reference symbols 107 to 111 are logic elements. When FDE is at “L,” the logic element 107 (one of two input logic elements) is effective, so that the clock signal CLK is selected and output as the clock signal SCK, and at the same time, the clock signal XSCK complementary to the clock signal SCK is output. When FDE is at “H,” the logic element 108 (the other input logic element) is effective, so that the frequency-divided clock signal FCK is selected and output as the clock signal SCK, and at the same time, the clock signal XSCK complementary to the clock signal SCK is output.

FIG. 4 shows an example configuration of the second charge pump circuit 104 (two-stages-one-parallel arrangement). Reference symbols Cc1 and Cc2 indicate boost capacitances which are boosted in accordance with second boost clock signals PCK2 and XPCK2, respectively. Reference symbols Tc1 and Tc2 indicate charge transfer transistors which have a diode-connection and transfer charge from the previous stage to the next stage. Reference symbol Tc3 indicates a backflow preventing circuit which prevents backflow of the boosted voltage VPUMP2. Here, the second charge pump circuit 104 receives the first boosted voltage VPUMP1 of a first charge pump circuit 906 as an input voltage and generates the second boosted voltage VPUMP2 which has a higher voltage level than that of the first boosted voltage VPUMP1. Specifically, the boosted voltage VPUMP2 of the second charge pump circuit 104 is represented by

$$VPUMP2 = VPUMP1 + V\alpha$$

where $V\alpha$ represents an increase in voltage of the second charge pump circuit 104.

Note that the present disclosure is not limited to the frequency dividing circuit 102 of FIG. 2. Any circuit having a similar function may be employed. Moreover, the frequency dividing circuit 102 is not limited to 1/2 frequency division and may be 1/N frequency division (N: a natural number of two or more). A complementary clock signal

may be generated by the frequency dividing circuit 102.

Moreover, the numbers of elements connected in parallel and elements connected in series in the charge pump circuits 906 and 104 are only for illustrative purposes. The present disclosure is not limited to this. Any configuration having a similar function may be employed. Moreover, although a pair of the first boost circuit 901 and the second boost circuit 101 is provided, the second boost circuit 101 may include a plurality of charge pump circuits, each of which is connected to the first output node N1. In this case, the frequency dividing circuit 102 and the buffer circuit 103 may be shared or a plurality of frequency dividing circuits 102 and a plurality of buffer circuits 103 may be provided, resulting in a similar effect.

Next, operation of the internal voltage generating circuit 100 shown in FIGS. 1 to 4 will be described with reference to FIG. 5. Here, the output voltages and output currents of the first and second charge pump circuits 906 and 104 are assumed to have the following relationships. The first boosted voltage VPUMP1 of the first charge pump circuit 906 is lower than the second boosted voltage VPUMP2 of the second charge pump circuit 104, and the current supply capability IPUMP1 of the first charge pump circuit 906 is larger than the current supply capability IPUMP2 of the second charge pump circuit 104.

(Time T0)

The circuit is in the initial state, where the first control signal PPE1 and the second control signal PPE2 are both at “L.”

(Time T1)

At time T1, the first control signal PPE1 transitions from “L” to “H.” In this case, the first boosted voltage VPUMP1 of the first output node N1 has not reached a first target voltage VPP1_TARGET, and therefore, a first high voltage detecting circuit 904 outputs “L” as a first sense signal CKE1. As a result, a first CLK gate circuit 905 outputs the clock signals CLK and XCLK as first boost clock signals PCK1 and XPCK1, and the first charge pump circuit 906 starts boost operation in synchronization with the first boost clock

signals PCK1 and XPCK1.

Similarly, the second control signal PPE2 transitions from “L” to “H.” In this case, the second boosted voltage VPUMP2 of the second output node N2 also has not reached a second target voltage VPP2_TARGET, and therefore, a second high voltage
5 detecting circuit 907 outputs “L” as a second sense signal CKE2. Also, since the control signal FDE is at “L,” the frequency dividing circuit 102 fixes the frequency-divided clock signal FCK to “L,” and the buffer circuit 103 outputs the clock signal CLK as the clock signal SCK to a second CLK gate circuit 908.

As a result, the second CLK gate circuit 908 outputs the clock signals SCK and
10 XSCK as the second boost clock signals PCK2 and XPCK2, and the second charge pump circuit 104 starts boost operation in synchronization with the second boost clock signals PCK2 and XPCK2.

(Time T2)

At time T2, the first charge pump circuit 906 receives the first boost clock signals
15 PCK1 and XPCK1 and outputs the first boosted voltage VPUMP1 through the first output node N1, and the second charge pump circuit 104 receives the second boost clock signals PCK2 and XPCK2 and outputs the second boosted voltage VPUMP2 ($=VPUMP1+V_{\alpha}$) through the second output node N2. A setup time until this time is substantially the same for the second boosted voltage VPUMP2 and the first boosted voltage VPUMP1.

20 (Time T3)

At time T3, when the first boosted voltage VPUMP1 of the first output node N1 has reached the first target voltage VPP1_TARGET, the first sense signal CKE1 of the first high voltage detecting circuit 904 transitions from “L” to “H.” As a result, the first CLK gate circuit 905 fixes the first boost clock signal PCK1 to “L” and its complementary
25 signal XPCK1 to “H,” so that the boost operation of the first charge pump circuit 906 is stopped. On the other hand, since the second boosted voltage VPUMP2 of the second output node N2 has not reached the second target voltage VPP2_TARGET, the boost

operation is continued. As a result, the first charge pump circuit 906 no longer contribute to an increase in the second boosted voltage VPUMP2, i.e., the increase is attributed only to the current supply capability of the second charge pump circuit 104, resulting in a decrease in voltage increasing rate. In other words, as is similar to the conventional example, "Phase1" during which the voltage is increased without the contribution of the charge pump circuit 906 continues until time T3, and "Phase1" is transitioned to "Phase2" during which there is no contribution of the charge pump circuit 906 at time T3, and thereafter, Phase 2 continues.

(Time T4)

At time T4, the second boosted voltage VPUMP2 of the second output node N2 reaches the second target voltage VPP2_TARGET. As a result, the boost operation of the second charge pump circuit 104 is stopped. Note that the second boosted voltage VPUMP2 increases until the first target voltage VPP1_TARGET of the first boosted voltage VPUMP1 at substantially the same rate as that of the first boosted voltage VPUMP1, resulting in a reduction in setup time. Also, obviously, during the time that the second charge pump circuit 104 is stopped, the second charge pump circuit 104 does not consume charge of the first boosted voltage VPUMP1 of the first charge pump circuit 906, and therefore, charge which would otherwise be supplied to the second charge pump circuit 104 can be supplied to an output load of the first charge pump circuit 906, whereby the use efficiency of the first boost circuit 901 can be improved.

(Time T5)

At time T5, when the first boosted voltage VPUMP1 becomes lower than the first target voltage VPP1_TARGET, the first sense signal CKE1 transitions from "L" to "H," so that the boost operation of the first charge pump circuit 906 is resumed.

(Time T6)

At time T6, when the control signal FDE has transitioned from "L" to "H," the frequency dividing circuit 102 is driven to output the frequency-divided clock signal FCK

whose frequency is 1/2 of that of the clock signal CLK. At the same time, the buffer circuit 103 switches the clock signal SCK to be supplied to the second CLK gate circuit 908 from the clock signal CLK to the frequency-divided clock signal FCK and starts outputting the clock signal SCK. As a result, the clock signals SCK and XSCK based on the frequency-divided clock signal FCK are supplied as the second boost clock signals PCK2 and XPCK2 of the second charge pump circuit 104. Therefore, after the second charge pump circuit 104 starts the boost operation, charge at the first output node N1 is no longer rapidly used. As a result, even when the boost capacitances Cc1 and Cc2 of the second charge pump circuit 104 are increased so as to reduce the setup time of the second output node N2, the potential stability of the first output node N1 can be held. Moreover, it is possible to allow the current supply capability IPUMP1 of the first charge pump circuit 906 to stably supply charge.

Thereafter, the first charge pump circuit 906 performs an intermittent operation, depending on the voltage level of the first boosted voltage VPUMP1 of the first output node N1. Similarly, the second charge pump circuit 104 performs intermittent operation, depending on the voltage level of the second boosted voltage VPUMP2 of the second output node N2. During this period of time, the second sense signal CKE2 falls at time T7, the first sense signal CKE1 falls at time T8, and the first sense signal CKE1 rises at time T9.

Note that current consumption can be reduced by synchronizing both or either of the frequency dividing circuit 102 and the buffer circuit 103 with the second sense signal CKE2 of the second high voltage detecting circuit 907.

<Effect>

As described above, the first boosted voltage VPUMP1 of the first charge pump circuit 906 is used as an input voltage to the second charge pump circuit 104 having a small current supply capability, and the charge pump circuits 906 and 104 are controlled using the separate high voltage detecting circuits 904 and 907, respectively, and moreover,

the boost clock signal to be supplied to the second charge pump circuit 104 is divided, whereby the setup time of the second charge pump circuit 104 can be reduced. In addition, after setting up, current supply can be concentrated into the output load of the first charge pump circuit 906, and even when the second charge pump circuit 104 is operated, the frequency of the boost clock signal is set to be low. Therefore, the fluctuation of the output voltage of the first charge pump circuit 906 can be suppressed, resulting in a more stable boosted voltage and a more stable supply of a boost current.

(Second Embodiment)

FIG. 6 shows an internal voltage generating circuit 200 according to a second embodiment which is different from the internal voltage generating circuit 100 of the first embodiment of FIG. 1 in that the buffer circuit 103 is controlled by a clock comparing circuit (CMP) 201 which compares the clock signal CLK and the frequency-divided clock signal FCK and generates a new control signal FCE. Referring to FIG. 7, in the clock comparing circuit 201, when the clock signal CLK and the frequency-divided clock signal FCK are both at “H,” the output of the operational circuit 202 is at “H” and is input to a clock terminal of a latch circuit 203, which in turn outputs the control signal FDE (=“H”) received as a data signal as the new control signal FCE through a terminal Q. As a result, the buffer circuit 103 switches the clock signal SCK between the clock signal CLK and the frequency-divided clock signal FCK.

FIG. 8 is a timing diagram which is obtained by adding time T6a to FIG. 5. At time T6, although the logic of the control signal FDE transitions, since the clock signal CLK and the frequency-divided clock signal FCK are both at “L,” the new control signal FCE remains at “L.” At time T6a, both the clock signal CLK and the frequency-divided clock signal FCK transition to “H,” so that the control signal FDE (=“H”) becomes effective and the logic of the new control signal FCE transitions, and the buffer circuit 103 outputs the clock signals SCK and XSCK to the second CLK gate circuit 908 based on the frequency-divided clock signal FCK.

Note that if all or any of the frequency dividing circuit 102, the buffer circuit 103 and the clock comparing circuit 201 are operated in synchronization with the second sense signal CKE2 of the second high voltage detecting circuit 907, current consumption can be reduced.

5 Thus, by switching between the clock signal CLK and the frequency-divided clock signal FCK when both of them are at “H” or “L,” it is possible to prevent the cycle of the clock signals SCK and XSCK to the second CLK gate circuit 908 from being temporarily decreased, whereby an increase in fluctuation of the output voltage can be prevented.

 Although it has been assumed in the embodiments above that the single-phase
10 clock signals CLK and XCLK are employed, it is clear that if a plurality of first and second charge pump circuits 906 and 104 are arranged in parallel, then when a multi-phase clock signal is supplied to the respective corresponding charge pump circuits, a similar function and effect can be obtained.

 The internal voltage generating circuit of the present disclosure is useful as, for
15 example, a power source generating circuit for a non-volatile semiconductor memory device. The internal voltage generating circuit of the present disclosure can also be used in applications, such as power source circuits for a volatile semiconductor memory device (e.g., a DRAM, etc.), a liquid crystal device, a mobile device and the like.

 Although the preferable embodiments of the present disclosure have been
20 described above, the present disclosure is not limited to those. Various changes and modifications can be made.

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In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: Not Yet Assigned
	:	
Application No.: Not Yet Assigned	:	Group Art Unit: Not Yet Assigned
	:	
Filed: July 02, 2009	:	Examiner: Not Yet Assigned
	:	
For: INTERNAL VOLTAGE GENERATING CIRCUIT		

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In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

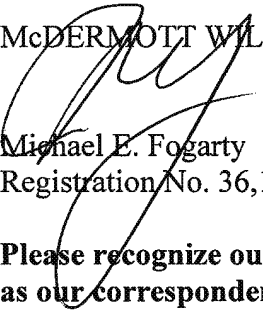
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The relevance of the reference **US 5,999,475** is discussed in the present specification.

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Respectfully submitted,

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Date: July 2, 2009

**UTILITY PATENT APPLICATION
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Transmitted herewith for filing is the patent application of:

**INVENTOR: Seiji YAMAHIRA
FOR: INTERNAL VOLTAGE GENERATING CIRCUIT**

Enclosed are:

- ☒ 19 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed of Japanese Patent Application No. **JP 2008-179566** filed July 9, 2008.
- ☒ 8 sheets of formal drawing.
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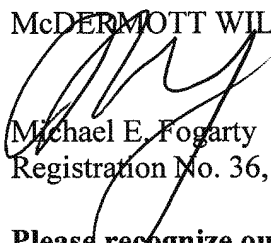
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Respectfully submitted,

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/497,090	07/02/2009	2838	1090	079195-0937	7	3

CONFIRMATION NO. 5747

FILING RECEIPT



OC000000036924272

Date Mailed: 07/20/2009

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Domestic Priority data as claimed by applicant

Foreign Applications

JAPAN 2008-179566 07/09/2008

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Projected Publication Date: 01/14/2010

Non-Publication Request: No

Early Publication Request: No

Title

INTERNAL VOLTAGE GENERATING CIRCUIT

Preliminary Class

363

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This is to certify that the annexed is a true copy of the following application as filed with this Office.

出 願 年 月 日
Date of Application: 2008年 7月 9日

出 願 番 号
Application Number: 特願2008-179566

パリ条約による外国への出願
に用いる優先権の主張の基礎
となる出願の国コードと出願
番号
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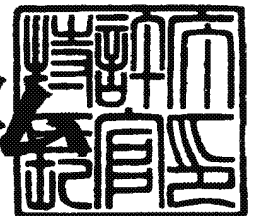
J P 2008-179566

出 願 人
Applicant(s): パナソニック株式会社

2009年 8月 4日

特許庁長官
Commissioner,
Japan Patent Office

細野 哲子



【書類名】	特許願
【整理番号】	5037600007
【提出日】	平成20年 7月 9日
【あて先】	特許庁長官殿
【国際特許分類】	H02M 3/07
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【手数料の表示】
【予納台帳番号】 014409
【納付金額】 15,000円
【提出物件の目録】
【物件名】 特許請求の範囲 1
【物件名】 明細書 1
【物件名】 図面 1
【物件名】 要約書 1
【包括委任状番号】 0505962

【書類名】 特許請求の範囲

【請求項 1】

第 1 の電圧と第 1 の端子との間に備えられた第 1 の昇圧回路と、
前記第 1 の端子と第 2 の端子との間に備えられた第 2 の昇圧回路と、
前記第 1 の昇圧回路に供給される第 1 のクロック信号を分周して第 2 のクロック信号を生成する分周回路と、
前記第 1 のクロック信号又は前記第 2 のクロック信号のいずれかを選択して前記第 2 の昇圧回路に供給するバッファ回路とを有することを特徴とする内部電圧発生回路。

【請求項 2】

請求項 1 記載の内部電圧発生回路において、
前記第 1 のクロック信号と前記第 2 のクロック信号とを比較して前記バッファ回路の出力選択タイミングを制御するクロック比較回路を更に有することを特徴とする内部電圧発生回路。

【書類名】明細書

【発明の名称】内部電圧発生回路

【技術分野】

【0001】

本発明は、昇圧回路を用いた内部電圧発生回路に関するものである。

【背景技術】

【0002】

近年、不揮発性半導体記憶装置であるフラッシュメモリにおいては、単一電源電圧あるいは低い電源電圧でのデータの読み出し、データの書き換えが要求されており、各動作を実施する際にオンチップで昇圧電圧、あるいは負昇圧電圧を供給する昇圧回路が必要とされている。また、CMOSプロセスにおいても昇圧回路で発生された電圧が電源としてアナログ回路の特性改善に用いられている。

【0003】

図9は、特許文献1に記載の内部電圧発生回路900の構成を示す。内部電圧発生回路900は、クロック信号CLK及び相補クロック信号XCLKに同期して昇圧動作を行って第1の出力ノードN1に第1の昇圧電圧VPUMP1を出力する第1の昇圧回路901と、同様にクロック信号CLK及びXCLKに同期して昇圧動作を行って第2の出力ノードN2に第2の昇圧電圧VPUMP2を出力する第2の昇圧回路902と、第1の出力ノードN1と第2の出力ノードN2との間を導通状態又は非導通状態とする高電圧スイッチ回路903とを備える。

【0004】

第1の昇圧回路901は、第1の制御信号PPE1が活性化されると、第1の昇圧電圧VPUMP1の電圧レベルを検出して第1の検知信号CKE1を活性状態又は不活性状態のいずれかに設定する第1の高電圧検出回路904と、第1の検知信号CKE1に応じてクロック信号CLK及びXCLKを第1の昇圧クロック信号PCK1及びXPCK1として出力する第1のCLKゲート回路905と、第1の昇圧クロック信号PCK1及びXPCK1に同期して昇圧動作を行って第1の出力ノードN1に第1の昇圧電圧VPUMP1を出力する第1のチャージポンプ回路906とを備える。

【0005】

第2の昇圧回路902は、第2の制御信号PPE2が活性化されると、第2の昇圧電圧VPUMP2の電圧レベルを検出して第2の検知信号CKE2を活性状態又は不活性状態のいずれかに設定する第2の高電圧検出回路907と、第2の検知信号CKE2に応じてクロック信号CLK及びXCLKを第2の昇圧クロック信号PCK2及びXPCK2として出力する第2のCLKゲート回路908と、第2の昇圧クロック信号PCK2及びXPCK2に同期して昇圧動作を行って第2の出力ノードN2に第2の昇圧電圧VPUMP2を出力する第2のチャージポンプ回路909とを備える。

【0006】

高電圧スイッチ回路903は、第1の制御信号PPE1に対して相補的な制御信号XPPE1と、第1の検知信号CKE1に対して相補的な検知信号XCKE1とに応じて制御され、内部電圧発生回路900の動作開始時には、第1の出力ノードN1と第2の出力ノードN2との間を導通状態にし、第1の出力ノードN1の電圧レベルが所定の電圧レベルになった後、第1の出力ノードN1と第2の出力ノードN2との間を遮断状態とする。

【0007】

図10は第1のチャージポンプ回路906の詳細であり、第1の昇圧クロック信号PCK1及びXPCK1に同期して昇圧される昇圧容量Ca1～Ca4と、昇圧された電荷を前段から後段へ転送する電荷転送トランジスタTa1～Ta4と、第1の出力ノードN1の電荷の逆流を防止する逆流防止回路Ta5とを備えた4段1並列から構成される。

【0008】

図11は第2のチャージポンプ回路909の詳細であり、第2の昇圧クロック信号PCK2及びXPCK2に同期して昇圧される昇圧容量Cb1～Cb6と、昇圧された電荷を

前段から後段へ転送する電荷転送トランジスタT b 1～T b 6と、第2の出力ノードN 2の電荷の逆流を防止する逆流防止回路T b 7とを備えた6段1並列から構成される。

【0009】

ここで、第1及び第2のチャージポンプ回路906、909はともに第1及び第2の入力端子NIN1、NIN2に電源電圧VDDが供給されて、第1及び第2の昇圧電圧VPUMP1、VPUMP2を発生する。これら第1及び第2のチャージポンプ回路906、909の出力電圧、出力電流の関係は、次のとおりとする。すなわち、第1のチャージポンプ回路906の昇圧電圧VPUMP1は、第2のチャージポンプ回路909の昇圧電圧VPUMP2より低く、かつ、第1のチャージポンプ回路906の電流供給能力IPUMP1は、第2のチャージポンプ回路909の電流供給能力IPUMP2より大きいものとする。更に例えば、第1のチャージポンプ回路906の昇圧容量Ca1～Ca4の容量値は5pF、第2のチャージポンプ回路909の昇圧容量Cb1～Cb6の容量値は1pFとする。

【0010】

図12は図9～図11の動作波形であり、図12を用いて昇圧動作を簡単に説明する。

【0011】

〔時刻T0〕

回路の初期状態を示し、第1の制御信号PPE1及び第2の制御信号PPE2がいずれも“L”である。

【0012】

〔時刻T1〕

時刻T1において、第1の制御信号PPE1が“L”から“H”に遷移する。このとき、第1の出力ノードN1の第1の昇圧電圧VPUMP1は、第1の目標電圧VPP1__TARGETに達しておらず、第1の高電圧検出回路904は第1の検知信号CKE1として“L”を出力する。これにより、第1のCLKゲート回路905は、第1の昇圧クロック信号PCK1及びXPCK1としてクロック信号CLK及びXCLKを出力し、第1のチャージポンプ回路906は第1の昇圧クロック信号PCK1及びXPCK1に同期して昇圧動作を開始する。

【0013】

同様に第2の制御信号PPE2が“L”から“H”に遷移する。このとき、第2の出力ノードN2の第2の昇圧電圧VPUMP2も、第2の目標電圧VPP2__TARGETに達しておらず、第2の高電圧検出回路907は第2の検知信号CKE2として“L”を出力する。これにより、第2のCLKゲート回路908は、第2の昇圧クロック信号PCK2及びXPCK2としてクロック信号CLK及びXCLKを出力し、第2のチャージポンプ回路909は第2の昇圧クロック信号PCK2及びXPCK2に同期して昇圧動作を開始する。

【0014】

上記より、第1の検知信号CKE1が“L”であるため、これに対して相補的な検知信号XCKE1が“H”となり、高電圧スイッチ回路903が導通状態となる。これにより、第1のチャージポンプ回路906と第2のチャージポンプ回路909との双方によって、第1の出力ノードN1と第2の出力ノードN2との充電が開始される。

【0015】

〔時刻T2〕

時刻T2では、高電圧スイッチ回路903が導通状態のまま、第1のチャージポンプ回路906と第2のチャージポンプ回路909とによって、第1の出力ノードN1と第2の出力ノードN2が同じ速度で充電される。

【0016】

〔時刻T3〕

時刻T3となり、第1の昇圧電圧VPUMP1が第1の目標電圧VPP1__TARGETに到達すると、第1の高電圧検出回路904の第1の検知信号CKE1が“L”から“

H”に遷移し、第1のCLKゲート回路905は第1の昇圧クロック信号PCK1を“L”に、その相補信号XPCK1を“H”にそれぞれ固定する。これによって、第1のチャージポンプ回路905の昇圧動作が停止されると同時に、高電圧スイッチ回路903が導通状態から非導通状態へと遷移し、第1の出力ノードN1と第2の出力ノードN2とが遮断される。

【0017】

時刻T1から時刻T3までの高電圧スイッチ回路903が導通状態である「Phase 1」の間、電流供給能力の低い第2のチャージポンプ回路909の第2の出力ノードN2は、電流供給能力の高い第1のチャージポンプ回路906によって第1の目標電圧VPP1_TARGETまで急速に充電される。時刻T3以降、高電圧スイッチ回路903が非導通状態となって第1のチャージポンプ回路906と第2のチャージポンプ回路909とが別々に動作する「Phase 2」に遷移する。

【0018】

〔時刻T4〕

時刻T4となり、第1の昇圧容量Ca1～Ca4 (= 5 pF) を持つ第1のチャージポンプ回路906に対して、1/5の昇圧容量Cb1～Cb6 (= 1 pF) を持つ第2のチャージポンプ回路909のみで第2の出力ノードN2を充電し、時刻T5にて第2の目標電圧VPP2_TARGETに到達する。電流供給能力の低い第2のチャージポンプ回路909のみを用いて第2の出力ノードN2の充電を行うPhase 2では、第2の出力ノードN2の時間当たりの電圧変化は、Phase 1に比べて急激に小さくなる。

【0019】

これ以降、第1の出力ノードN1の電圧レベルに応じて第1の検知信号CKE1が、第2の出力ノードN2の電圧レベルに応じて第2の検知信号CKE2がそれぞれ論理反転し、第1のチャージポンプ回路906と第2のチャージポンプ回路909との間欠動作が繰り返されて各々の電圧レベルが保持される。

【0020】

以上のように、電流供給能力が高い第1のチャージポンプ回路906の第1の出力ノードN1と、電流供給能力が低い第2のチャージポンプ回路909の第2の出力ノードN2とを高電圧スイッチ回路903によって導通/非導通状態に制御することで、内部電圧発生回路900の面積増大を抑制した上で、電流供給能力が低い第2のチャージポンプ回路909の第2の出力ノードN2の電圧セットアップ時間を早くすることが可能となる。

【特許文献1】特開平11-134892号公報

【発明の開示】

【発明が解決しようとする課題】

【0021】

しかしながら、上記従来例の内部電圧発生回路900では、Phase 2における第2のチャージポンプ回路909のセットアップ時間短縮を図る際、セットアップ時間短縮のためだけに、図11に示す第2の昇圧容量Cb1～Cb6を大きくする場合が発生し、利用効率の悪い回路を増加させる課題があった。また、上記セットアップ時間短縮のために第2の昇圧容量Cb1～Cb6を増加した場合、第2の出力ノードN2のリップル抑制用に第2のチャージポンプ回路909の当該第2の出力ノードN2に平滑容量が必要となり、回路面積が大きくなる課題があった。

【課題を解決するための手段】

【0022】

本発明の1つの局面に従うと、第1の電圧と第1の端子との間に備えられた第1の昇圧回路と、前記第1の端子と第2の端子との間に備えられた第2の昇圧回路と、前記第1の昇圧回路に供給される第1のクロック信号を分周して第2のクロック信号を生成する分周回路と、前記第1のクロック信号又は前記第2のクロック信号のいずれかを選択して前記第2の昇圧回路に供給するバッファ回路とを有する内部電圧発生回路の構成が採用される。

【発明の効果】

【0023】

請求項1の発明によれば、第2の昇圧回路における電流供給能力の小さい第2のチャージポンプ回路の入力電圧として、第1の昇圧回路における第1のチャージポンプ回路の昇圧電圧を利用し、それぞれのチャージポンプ回路を高電圧検出回路により制御し、更に第2のチャージポンプ回路に供給する昇圧クロック信号を分周することで、第2のチャージポンプ回路のセットアップ時間を短縮でき、セットアップ終了後は、第1のチャージポンプ回路の出力負荷に電流供給を集中でき、更に安定した昇圧電圧と安定した昇圧電流の供給が可能である。

【0024】

請求項2の発明によれば、クロック信号と分周クロック信号との切り換えを“H”又は“L”の時に行うことで、昇圧クロック信号の周期が一時的に短くなることを防止でき、出力電圧変動の増加を抑制できる。

【発明を実施するための最良の形態】

【0025】

以下、本発明の実施の形態を図面を参照して詳しく説明する。なお、図中同一又は相当部分には同一の符号を付しその説明は繰り返さない。

【0026】

(第1の実施形態)

<構成>

図1は、本発明の第1の実施形態による内部電圧発生回路100の構成を示す。この内部電圧発生回路100は、第1の制御信号PPE1に応じて駆動する第1の昇圧回路901と、第2の制御信号PPE2に応じて駆動する第2の昇圧回路101とを備え、第1の昇圧回路901の第1の出力ノードN1に第1の昇圧電圧VPUMP1を出力し、第2の昇圧回路101の第2の出力ノードN2に第2の昇圧電圧VPUMP2を出力する。102は、制御信号FDEに応じてクロック信号CLKをN分周（Nは2以上の自然数）し、分周クロック信号FCKを出力する分周回路（FDIV）、103は制御信号FDEに応じて、クロック信号CLKあるいは分周クロック信号FCKのいずれか一方をクロック信号SCKとして出力し、同時にこのクロック信号SCKに対して相補的なクロック信号XSCKを出力するバッファ回路（BUF）である。104は、第1の昇圧回路901の第1の昇圧電圧VPUMP1を入力電圧として第2の昇圧電圧VPUMP2を発生する第2のチャージポンプ回路である。

【0027】

図2は、分周回路102の構成例である。105はフリップフロップ回路であり、制御信号FDEが“L”の時、リセット状態となって端子Qより“L”が出力される。一方、端子NQは端子Qに対して相補的な信号端子であり、リセット状態で端子NQより“H”が出力される。制御信号FDEが“H”の時、クロック信号CLKの立ち上がりエッジをトリガとして、端子Qを論理反転させる。これにより、クロック信号CLKに対して周波数が半分である分周クロック信号FCKを出力する。

【0028】

図3は、バッファ回路103の構成例である。107～111は論理素子であり、FDEが“L”の時、一方の入力論理素子107が有効となってクロック信号CLKが選択されてクロック信号SCKとして出力され、同時にクロック信号SCKに対して相補的なクロック信号XSCKが出力される。FDEが“H”の時、他方の入力論理素子108が有効となって分周クロック信号FCKが選択されてクロック信号SCKとして出力され、同時にクロック信号SCKに対して相補的なクロック信号XSCKが出力される。

【0029】

図4は、2段1並列の第2のチャージポンプ回路104の構成例である。Cc1～Cc2は、第2の昇圧クロック信号PCK2及びXPCK2によって昇圧される昇圧容量、Tc1～Tc2はダイオード接続されて、電荷を前段より後段に転送する電荷転送トランジ

スタ、 $Tc3$ は昇圧電圧VPUMP 2の逆流を防止する逆流防止回路である。ここで第2のチャージポンプ回路104は第1のチャージポンプ回路906の第1の昇圧電圧VPUMP 1を入力電圧として、第1の昇圧電圧VPUMP 1より高い電圧レベルである第2の昇圧電圧VPUMP 2を発生する。つまり、第2のチャージポンプ回路回路104の昇圧電圧VPUMP 2は、

$$VPUMP\ 2 = VPUMP\ 1 + V\alpha$$

となる。ここに、 $V\alpha$ は第2のチャージポンプ回路104における電圧上昇分である。

【0030】

なお、図2の分周回路102はこれに限らず、同様の機能を果たすものであればよく、更に1/2分周でなくともよく、1/N分周（N：2以上の自然数）であってもよい。相補的なクロック信号を分周回路102で生成してもよい。

【0031】

また、チャージポンプ回路906、104の並列数、段数は一例であり、これに限らなくてよく、更に構成においても同様の機能を果たすものであればよい。また、一例として第1の昇圧回路901と第2の昇圧回路101とを1対として設けているが、第2の昇圧回路101のチャージポンプ回路を複数個備え、それぞれのチャージポンプ回路を第1の出力ノードN1に接続して構成することも可能である。そのとき、分周回路102及びバッファ回路103を共通にすることも、あるいは複数個備えて構成しても同様の効果が得られる。

【0032】

次に、図5を参照しつつ、図1から図4に示した内部電圧発生回路100の動作について説明する。ここに、第1及び第2のチャージポンプ回路906、104の出力電圧、出力電流の関係として、第1のチャージポンプ回路906の第1の昇圧電圧VPUMP 1は、第2のチャージポンプ回路104の第2の昇圧電圧VPUMP 2より低く、かつ、第1のチャージポンプ回路906の電流供給能力IPUMP 1は、第2のチャージポンプ回路104の電流供給能力IPUMP 2より大きいものとする。

【0033】

〔時刻T0〕

回路の初期状態を示し、第1の制御信号PPE 1及び第2の制御信号PPE 2がいずれも“L”である。

【0034】

〔時刻T1〕

時間T1において、第1の制御信号PPE 1が“L”から“H”に遷移する。このとき、第1の出力ノードN1の第1の昇圧電圧VPUMP 1は、第1の目標電圧VPP1__TARGETに達しておらず、第1の高電圧検出回路904は第1の検知信号CKE 1として“L”を出力する。これにより、第1のCLKゲート回路905は、第1の昇圧クロック信号PCK 1及びXPCK 1としてクロック信号CLK及びXCLKを出力し、第1のチャージポンプ回路906は第1の昇圧クロック信号PCK 1及びXPCK 1に同期して昇圧動作を開始する。

【0035】

同様に第2の制御信号PPE 2が“L”から“H”に遷移する。このとき、第2の出力ノードN2の第2の昇圧電圧VPUMP 2も、第2の目標電圧VPP2__TARGETに達しておらず、第2の高電圧検出回路907は第2の検知信号CKE 2として“L”を出力する。また、制御信号FDEが“L”であるため、分周回路102は分周クロックFCCKを“L”に固定し、バッファ回路103は第2のCLKゲート回路908へのクロック信号SCKとしてクロック信号CLKを出力する。

【0036】

これにより、第2のCLKゲート回路908は、第2の昇圧クロック信号PCK 2及びXPCK 2としてクロック信号SCK及びXSCKを出力し、第2のチャージポンプ回路104は第2の昇圧クロック信号PCK 2及びXPCK 2に同期して昇圧動作を開始する。

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【0037】

〔時刻T2〕

時刻T2において、第1のチャージポンプ回路906は、第1の昇圧クロック信号PCK1及びXPCK1が供給されて第1の出力ノードN1に第1の昇圧電圧VPUMP1を出力し、第2のチャージポンプ回路104は、第2の昇圧クロック信号PCK2及びXPCK2が供給されて第2の出力ノードN2に第2の昇圧電圧VPUMP2(=VPUMP1+V α)を出力する。ここまで、第2の昇圧電圧VPUMP2と第1の昇圧電圧VPUMP1とのセットアップ時間は、ほぼ同等となる。

【0038】

〔時刻T3〕

時刻T3において、第1の出力ノードN1の第1の昇圧電圧VPUMP1が第1の目標電圧VPP1__TARGETに達成すると、第1の高電圧検出回路904の第1の検知信号CKE1が“L”から“H”に遷移する。これによって、第1のCLKゲート回路905によって第1の昇圧クロック信号PCK1が“L”に、その相補信号XPCK1が“H”にそれぞれ固定され、第1のチャージポンプ回路906の昇圧動作が停止される。一方、第2の出力ノードN2の第2の昇圧電圧VPUMP2は第2の目標電圧VPP2__TARGETに達成していないため、昇圧動作が続けられる。これより第2の昇圧電圧VPUMP2の電圧上昇において、第1のチャージポンプ回路906による上昇はなくなり、第2のチャージポンプ回路104のみの電流供給能力となるため、電圧上昇速度が低下する。つまり、時刻T3までは従来例同様、他のチャージポンプ回路906からの補助を受けて電圧上昇を行う「Phase1」であり、時刻T3以降、他のチャージポンプ回路906からの補助がなくなる「Phase2」へと遷移する。

【0039】

〔時刻T4〕

時刻T4において、第2の出力ノードN2の第2の昇圧電圧VPUMP2が第2の目標電圧VPP2__TARGETに達成する。これによって第2のチャージポンプ回路104の昇圧動作が停止される。ただし、第2の昇圧電圧VPUMP2は、第1の昇圧電圧VPUMP1の第1の目標電圧VPP1__TARGETまで、第1の昇圧電圧VPUMP1とほぼ同じ速度で電圧上昇し、セットアップ時間が短縮される。また、当然ながら、第2のチャージポンプ回路104が停止している間、第2のチャージポンプ回路104による第1のチャージポンプ回路906の第1の昇圧電圧VPUMP1の電荷消費はなくなるため、第2のチャージポンプ回路104に供給していた電荷を第1のチャージポンプ回路906の出力負荷に供給することができ、第1の昇圧回路901の利用効率を向上させることが可能である。

【0040】

〔時刻T5〕

時刻T5において、第1の昇圧電圧VPUMP1が第1の目標電圧VPP1__TARGETを下回ると第1の検知信号CKE1が“L”から“H”へと遷移し、第1のチャージポンプ回路906の昇圧動作が再開される。

【0041】

〔時刻T6〕

時刻T6において、制御信号FDEが“L”から“H”へと遷移すると、分周回路102が駆動してクロック信号CLKが2分周された分周クロック信号FCKが出力される。同時に、バッファ回路103は、第2のCLKゲート回路908へのクロック信号SCKとして、クロック信号CLKから分周クロック信号FCKに切り換えて出力を開始する。これにより、第2のチャージポンプ回路104の第2の昇圧クロック信号PCK2及びXPCK2として、分周クロック信号FCKに基づくクロック信号SCK及びXSCKが供給される。したがって、第2のチャージポンプ回路104が昇圧動作を開始した場合において、第1の出力ノードN1の電荷を急激に使用することがなくなるため、第2の出力ノ

ードN2のセットアップ時間短縮のために第2のチャージポンプ回路104の昇圧容量Cc1, Cc2を増やした場合においても、第1の出力ノードN1の電位の安定性を保持でき、更に第1のチャージポンプ回路906の電流供給能力IPUMP1による安定的な電荷供給が可能となる。

【0042】

以降、第1の出力ノードN1の第1の昇圧電圧VPUMP1の電圧レベルに応じて第1のチャージポンプ回路906は間欠動作を行い、同様に第2の出力ノードN2の第2の昇圧電圧VPUMP2の電圧レベルに応じて第2のチャージポンプ回路104は間欠動作を行う。この間、時刻T7にて第2の検知信号CKE2が立ち下がり、時刻T8にて第1の検知信号CKE1が立ち下がり、時刻T9にて第1の検知信号CKE1が立ち上がる。

【0043】

なお、分周回路102、バッファ回路103の両方、又は一方を第2の高電圧検出回路907の第2の検知信号CKE2に同期させることで消費電流を削減することが可能である。

【0044】

<効果>

以上のように、電流供給能力の小さい第2のチャージポンプ回路104の入力電圧として、第1のチャージポンプ回路906の第1の昇圧電圧VPUMP1を利用し、それぞれのチャージポンプ回路906, 104を別々の高電圧検出回路904, 907により制御し、更に第2のチャージポンプ回路104に供給する昇圧クロック信号を分周することで、第2のチャージポンプ回路104のセットアップ時間を短縮できる。また、セットアップ終了後は、第1のチャージポンプ回路906の出力負荷に電流供給を集中でき、かつ、第2のチャージポンプ回路104が動作した場合にも昇圧クロック信号の周波数を低くしているため、第1のチャージポンプ回路906の出力電圧の変動を抑制でき、更に安定した昇圧電圧と安定した昇圧電流の供給が可能となる。

【0045】

(第2の実施形態)

図6に示す内部電圧発生回路200は第2の実施形態であり、第1の実施の形態で示した図1に対して、クロック信号CLKと分周クロック信号FCKとを比較して新たな制御信号FCEを出力するクロック比較回路(CMP)201によってバッファ回路103を制御する点が異なる。クロック比較回路201は図7に示すとおりであり、クロック信号CLKと分周クロック信号FCKとがともに“H”の時に演算回路202の出力が“H”となってラッチ回路203のクロック端子に入力され、データ信号として与えられた制御信号FDE(=“H”)を出力する。この結果、バッファ回路103によってクロック信号CLKと分周クロック信号FCKとが切り換えられる。

【0046】

図8はタイミング図であり、図5に対して時刻T6aが追加されている。時刻T6において、制御信号FDEが論理遷移しているが、クロック信号CLK及び分周クロック信号FCKがともに“L”であるため、新たな制御信号FCEは“L”を出力したままとなる。時刻T6aとなって、クロック信号CLK及び分周クロック信号FCKがともに“H”となることで、制御信号FDE(=“H”)が有効となり、新たな制御信号FCEが論理遷移してバッファ回路103より、分周クロック信号FCKに基づく第2のCLKゲート回路908へのクロック信号SCK及びXSCKとして出力される。

【0047】

なお、分周回路102、バッファ回路103、クロック比較回路201の全て、又はいずれかを第2の高電圧検出回路907の第2の検知信号CKE2に同期させることで消費電流を削減することが可能である。

【0048】

以上によって、クロック信号CLKと分周クロック信号FCKとの切り換えを“H”又は“L”の時に行うことで、第2のCLKゲート回路908へのクロック信号SCK及び

X S C Kの周期が一時的に短くなることを防止でき、出力電圧変動の増加を抑制できる。

【0049】

なお、単相のクロック信号C L K及びX C L Kを用いた実施形態の説明を行ったが、第1及び第2のチャージポンプ回路906, 104が多並列構成になった場合には、多相クロック信号を対応するチャージポンプ回路に供給することで、同様の機能と効果が得られることは明確である。

【産業上の利用可能性】

【0050】

本発明に係る内部電圧発生回路は、不揮発性半導体記憶装置の電源発生回路等として有用である。また、D R A M等の揮発性半導体記憶装置や、液晶装置、携帯機器の電源回路等の用途にも応用できる。

【図面の簡単な説明】

【0051】

【図1】本発明の第1の実施形態による内部電圧発生回路の構成を示すブロック図である。

【図2】図1中の分周回路の詳細構成例を示す回路図である。

【図3】図1中のバッファ回路の詳細構成例を示す回路図である。

【図4】図1中の第2のチャージポンプ回路の詳細構成例を示す回路図である。

【図5】図1の内部電圧発生回路の動作を示すタイミング図である。

【図6】本発明の第2の実施形態による内部電圧発生回路の構成を示すブロック図である。

【図7】図6中のクロック比較回路の詳細構成例を示す回路図である。

【図8】図6の内部電圧発生回路の動作を示すタイミング図である。

【図9】内部電圧発生回路の従来例の構成を示すブロック図である。

【図10】図9中の第1のチャージポンプ回路の詳細構成例を示す回路図である。

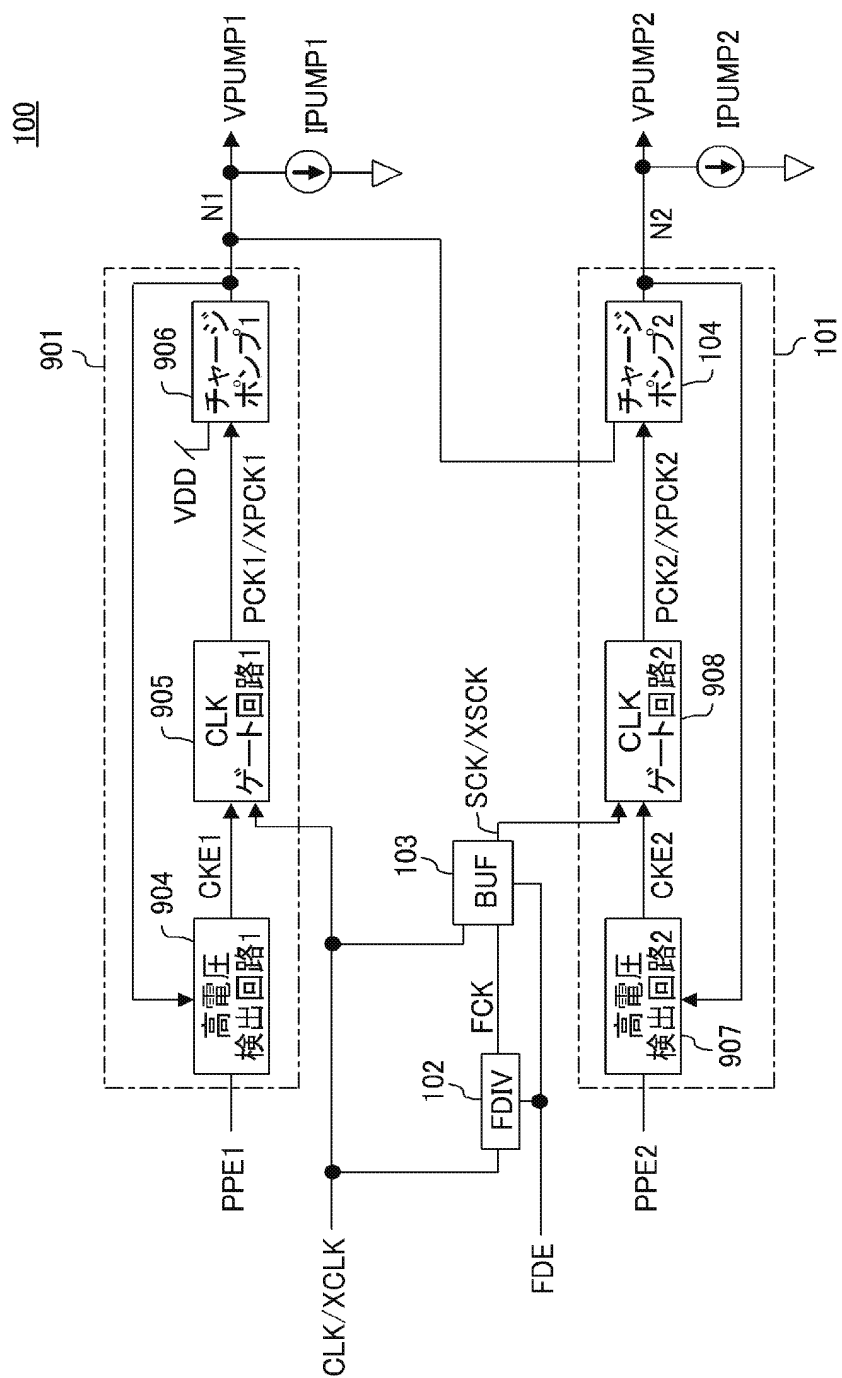
【図11】図9中の第2のチャージポンプ回路の詳細構成例を示す回路図である。

【図12】図9の内部電圧発生回路の動作を示すタイミング図である。

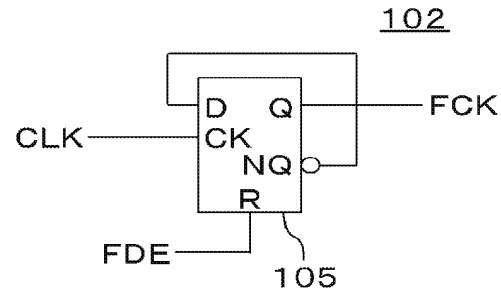
【符号の説明】

【0052】

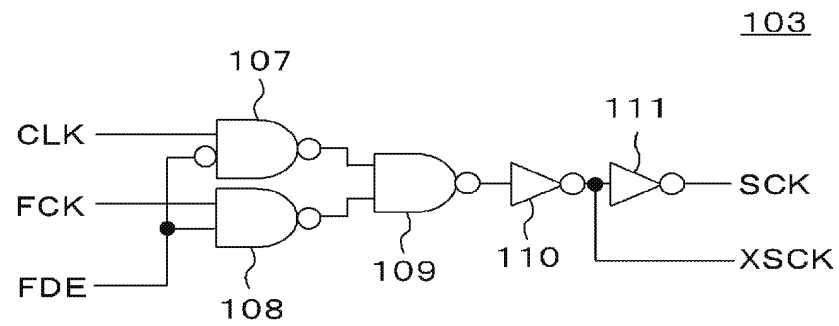
- 100 内部電圧発生回路
- 101 第2の昇圧回路
- 102 分周回路
- 103 バッファ回路
- 104 第2のチャージポンプ回路
- 200 内部電圧発生回路
- 201 クロック比較回路
- 900 内部電圧発生回路
- 901 第1の昇圧回路
- 902 第2の昇圧回路
- 903 高電圧スイッチ回路
- 904 第1の高電圧検出回路
- 905 第1のC L Kゲート回路
- 906 第1のチャージポンプ回路
- 907 第2の高電圧検出回路
- 908 第2のC L Kゲート回路
- 909 第2のチャージポンプ回路



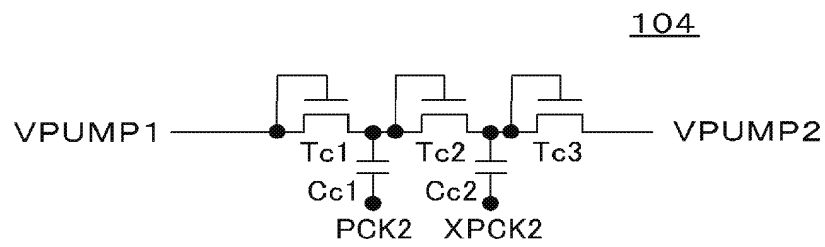
【図2】



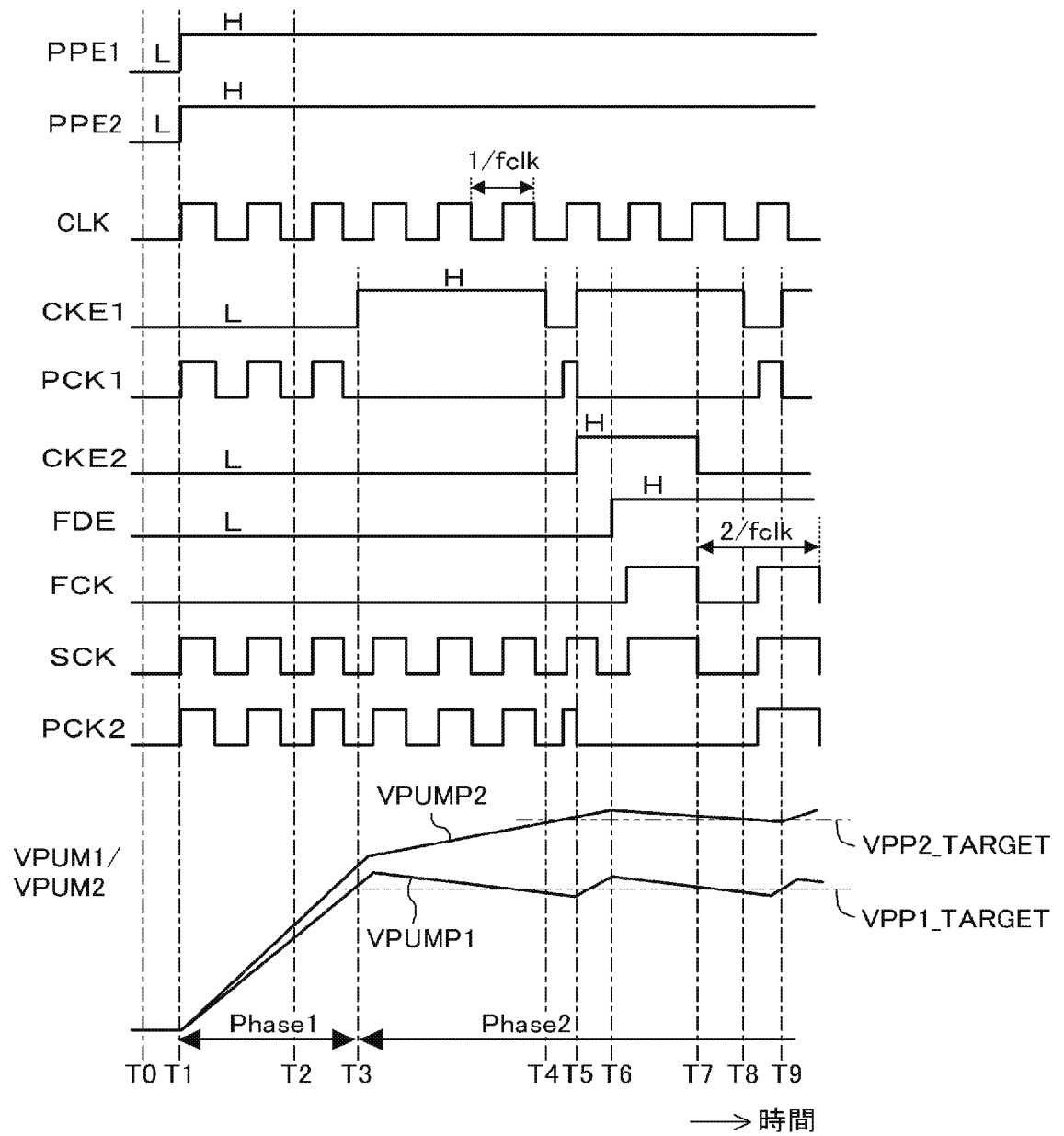
【図3】



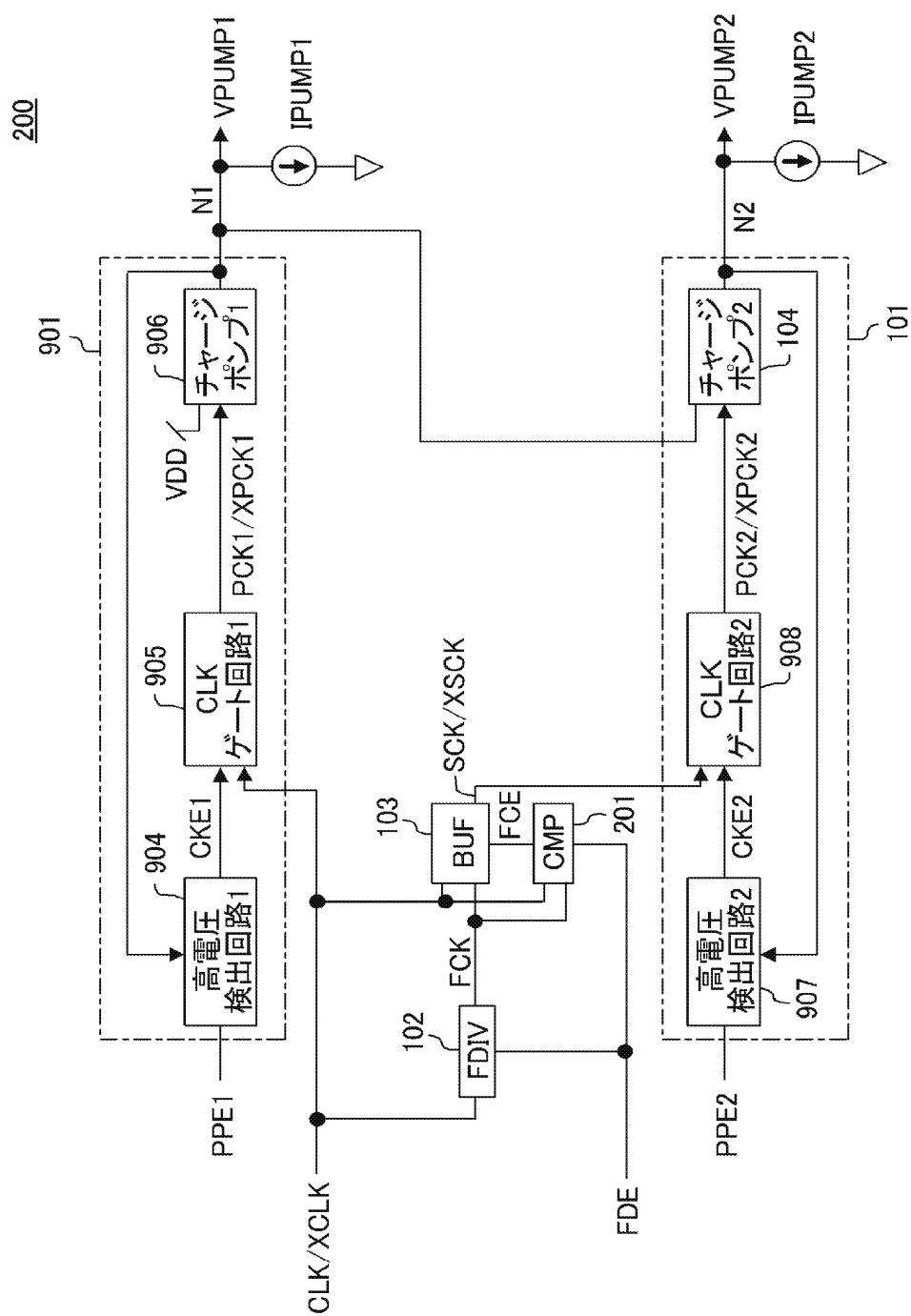
【図4】



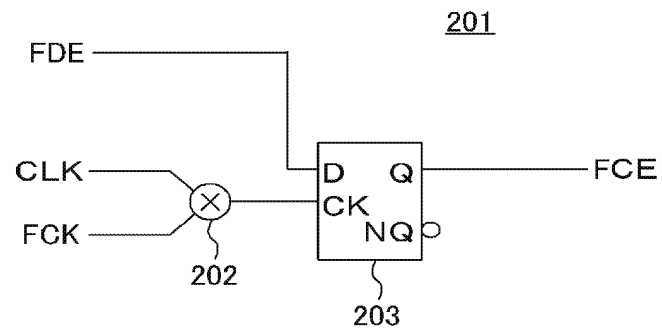
【図 5】



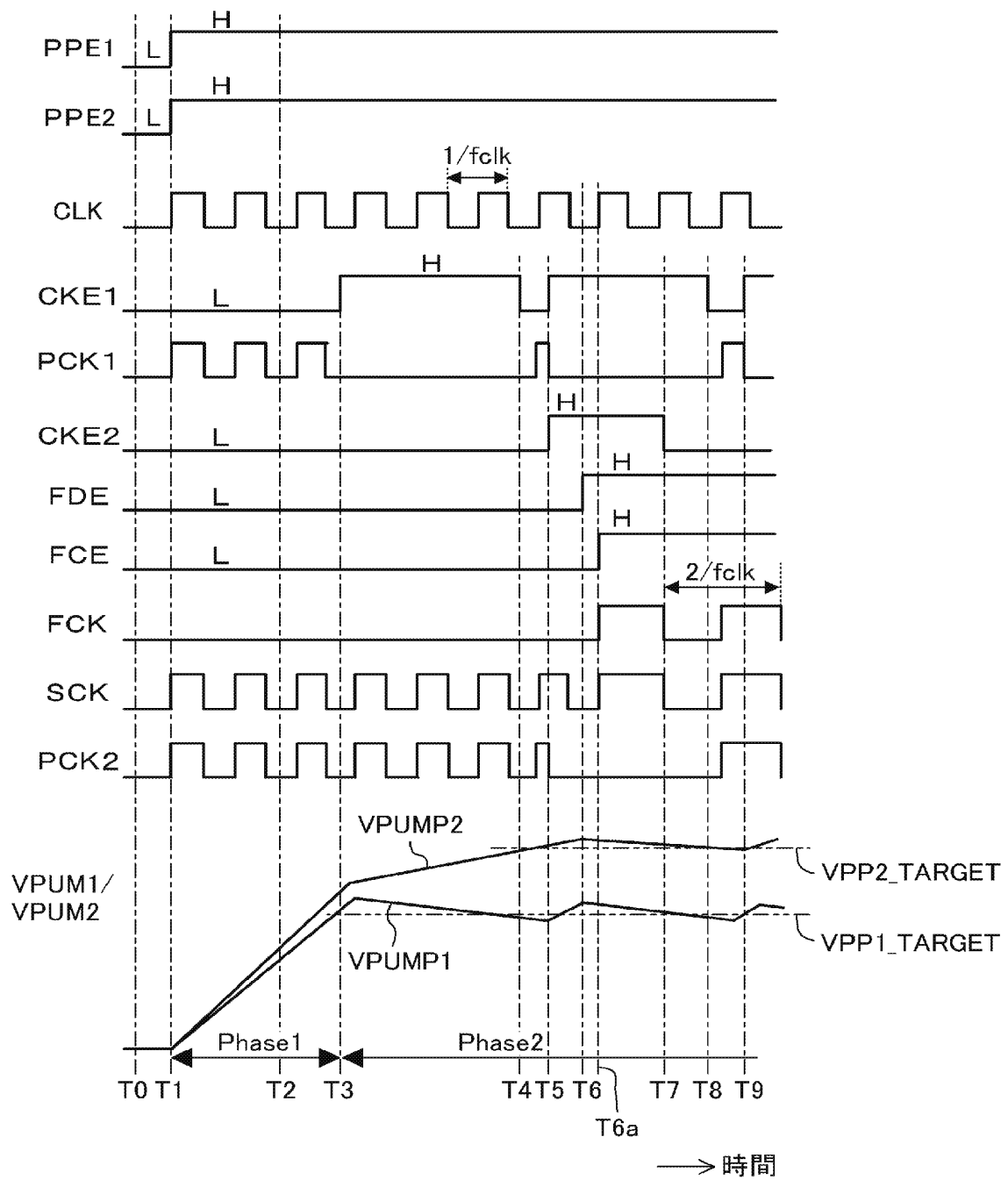
【図6】



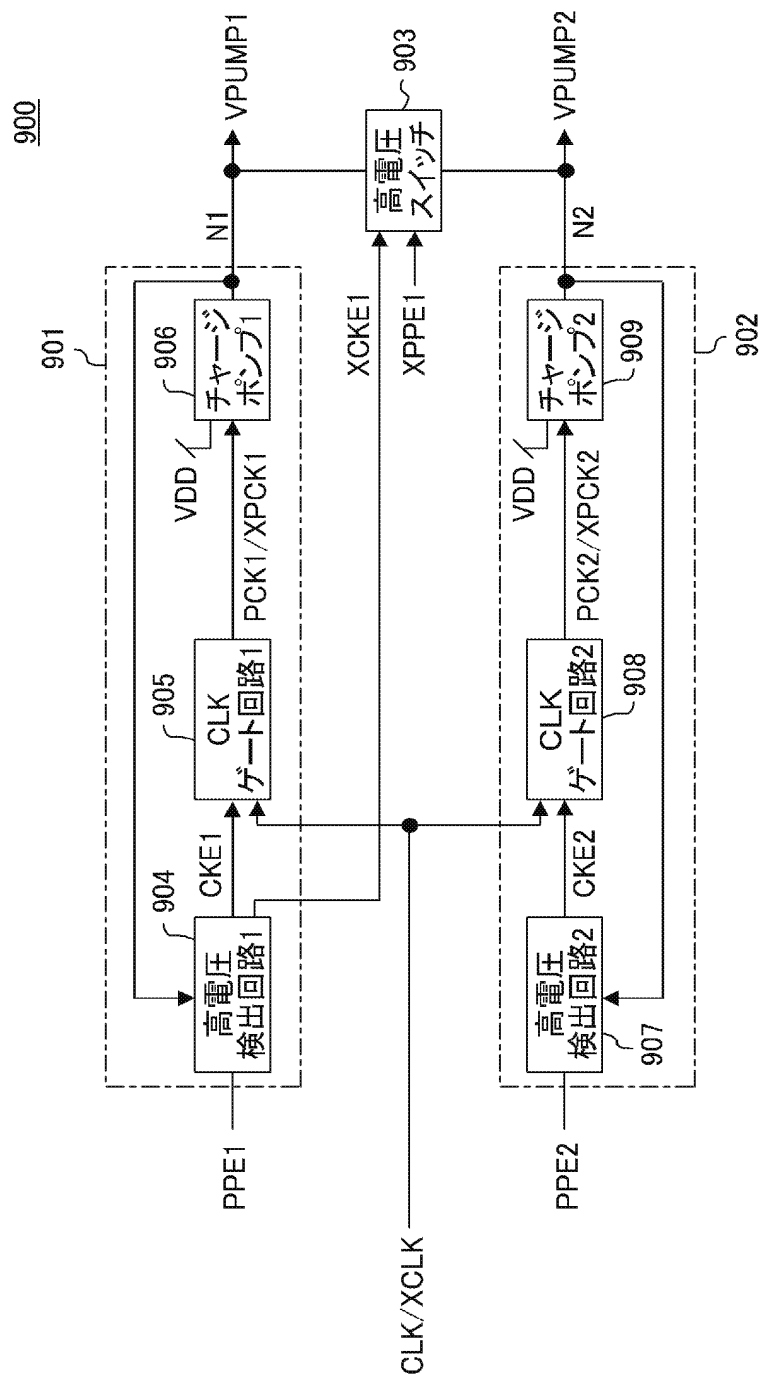
【図 7】



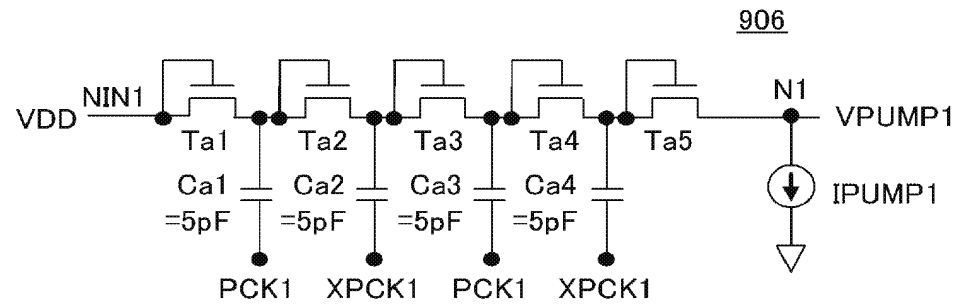
【図 8】



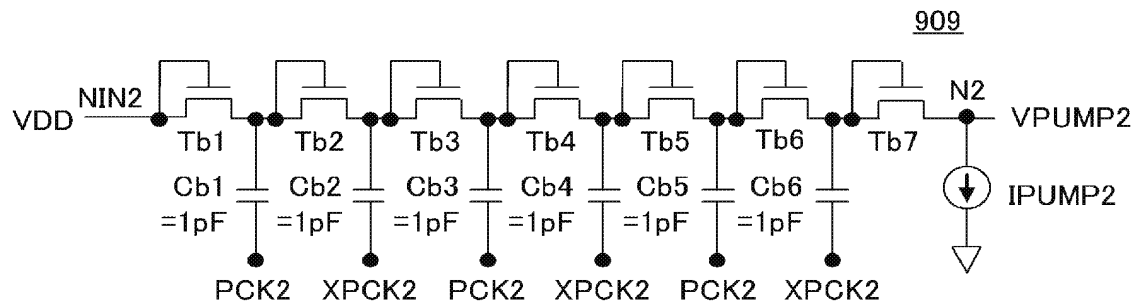
【図9】



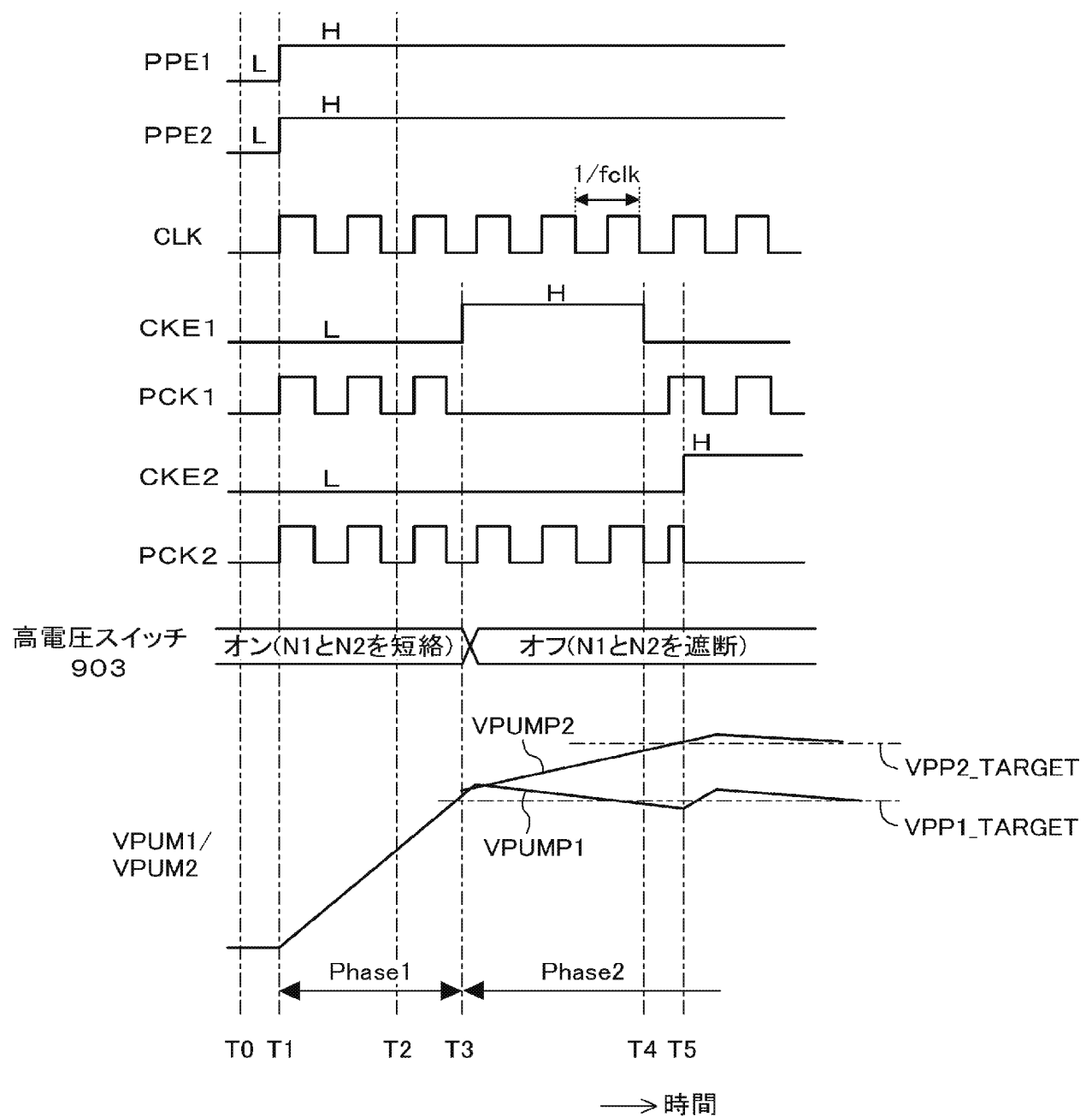
【図 1 0】



【図 1 1】



【図 1 2】



【書類名】 要約書

【要約】

【課題】 出力負荷に対して、第 1、第 2 の昇圧回路の電流供給能力を適切に設定可能な内部電圧発生回路を提供する。

【解決手段】 第 2 の昇圧回路 101 を第 1 の昇圧回路 901 の出力端子に接続し、更に起動後は、第 2 の昇圧回路 101 の昇圧クロック周波数を低くできるように構成する。これによって、第 2 の昇圧回路 101 の起動時間を早くするだけでなく、起動後は、第 1 の昇圧回路 901 の電流供給能力を増大できる。更に、第 2 の昇圧回路 101 が駆動する際、瞬時的に第 1 の昇圧回路 901 の出力電圧を変動させることもなく、第 1 及び第 2 の昇圧回路 901, 101 の出力電圧を安定して供給することができる。

【選択図】 図 1

出願人履歴

000005821

19900828

新規登録

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名称変更

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パナソニック株式会社



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/497,090	07/02/2009	Seiji Yamahira	079195-0937

CONFIRMATION NO. 5747

53080
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

PUBLICATION NOTICE



Title:INTERNAL VOLTAGE GENERATING CIRCUIT

Publication No.US-2010-0007408-A1

Publication Date:01/14/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

SHEET 1 OF 1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Substitute for form 1449/PTO)				ATTY. DOCKET NO. 079195-0937		SERIAL NO. Not Yet Assigned	
				APPLICANT Seiji YAMAHIRA			
				FILING DATE July 02, 2009		GROUP Not Yet Assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
		US 5,940,284	08-17-1999	TROUTMAN			
		US 5,999,475	12-07-1999	FUTATSUYA et al.			
		US 6,249,445 B1	06-19-2001	SUGASAWA			
		US 2004/0095806 A1	05-20-2004	OSAWA et al.			
		US 2007/0222498 A1	09-27-2007	CHOY et al.			
		US					
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
EXAMINER /Jeffery Zweizig/				DATE CONSIDERED 09/22/2010			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 12/497,090		Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI	
	Examiner Jeffrey S. Zweizig		Art Unit 2816	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,782,120	08-2010	Kim et al.	327/535
*	B	US-7,605,639	10-2009	Gou, Ja-Seung	327/536
*	C	US-7,592,856	09-2009	Ito et al.	327/536
*	D	US-7,579,902	08-2009	Frulio et al.	327/536
*	E	US-6,980,045	12-2005	Liu, Ping-Chen	327/536
*	F	US-6,278,317	08-2001	Hsu et al.	327/536
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747
53080 7590 09/24/2010 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			EXAMINER ZWEIZIG, JEFFERY SHAWN	
			ART UNIT 2816	PAPER NUMBER
			MAIL DATE 09/24/2010	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/497,090	Applicant(s) YAMAHIRA, SEIJI	
	Examiner Jeffrey S. Zweizig	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 July 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-5 is/are allowed.
- 6) ☒ Claim(s) 6 is/are rejected.
- 7) ☒ Claim(s) 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>7/2/09</u> . | 6) ☐ Other: _____ |

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Frulio et al. (7,579,902).

Fig. 7 shows a first charge pump 1 to m and a second charge pump m+1 to n as recited in claim 6. The frequency of the clock to the second charge pump is changed according to control signal STOP2 (clock frequency changes between active and zero).

Conclusion

Claims 1-5 appear to be allowable over the Prior Art of record. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Frulio et al. does not appear to show the divider recited in claims 1, 3 and 7.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571)

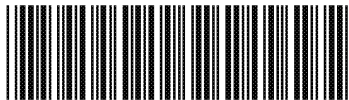
272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

536f1
/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

Search Notes 	Application/Control No. 12497090	Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI
	Examiner Jeffrey S Zweizig	Art Unit 2816

SEARCHED			
Class	Subclass	Date	Examiner
327	535, 536, 537	9/21/10	/JZ/

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 53080
 :
 Seiji YAMAHIRA : Confirmation Number: 5747
 :
 Application No.: 12/497,090 : Group Art Unit: 2816
 :
 Filed: July 02, 2009 : Examiner: Jeffery Shawn ZWEIZIG
 :
 For: INTERNAL VOLTAGE GENERATING CIRCUIT

Mail Stop Amendment
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

- ☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	7	20	0	\$52.00 =	\$0.00
Independent Claims	3	3	0	\$220.00 =	\$0.00
Multiple dependent claims newly presented					\$0.00
Fee for extension of time					\$0.00
Total of Above Calculations					\$0.00

- ☐ Please charge my Deposit Account No. 500417 in the amount of \$0.00. An additional copy of this transmittal sheet is submitted herewith.
- ☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
 Registration No. 36,139

Please recognize our Customer No. 53080 as our
 correspondence address.

600 13th Street, N.W.
 Washington, DC 20005-3096
 Phone: 202.756.8000 MEF:rp
 Facsimile: 202.756.8087
 Date: December 22, 2010

Docket No.: 079195-0937

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: 5747
	:	
Application No.: 12/497,090	:	Group Art Unit: 2816
	:	
Filed: July 02, 2009	:	Examiner: Jeffery Shawn ZWEIZIG
	:	
For: INTERNAL VOLTAGE GENERATING CIRCUIT	:	

AMENDMENT UNDER 37 C.F.R. § 1.111

Mail Stop - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Office Action dated September 24, 2010, having a three-month shortened statutory period for response set to expire on December 24, 2010, please amend the above-identified application as follows:

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 6 so as to more specifically recite the intended subject matter of the present disclosure. No new matter has been added.

Applicants note with appreciation the indication of allowance of claims 1-5 and the indication that claim 7 recites patentable subject matter.

For at least the reasons set forth below, it is respectfully submitted that all pending claims are now in condition for allowance.

II. The Rejection Of Claim 6 Under 35 U.S.C. §102

Claim 6 was rejected under 35 U.S.C. § 102 as being anticipated by USP No. 7,579,902 to Frulio. For at least the following reasons, it is respectfully submitted that claim 6, as amended, is not anticipated by Frulio.

Claim 6 relates to an internal voltage generating circuit which includes a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage. As amended, claim 6 further recites that a pulse width of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal.

For example, as explained in paragraph [0070] of Applicants' published application, if the control signal FDE transitions from low to high, the pulse width of the frequency-divided clock signal FCK is twice the pulse width of the clock signal CLK, and the pulse width of the second boost clock signal PCK2 is charged to twice the pulse width of the clock signal CLK.

Thus, in accordance with the claimed circuit recited by amended claim 6, the length of the period in which the clock signal is in a high state (i.e., the pulse width) is changed.

Turning to the pending rejection and the cited prior art reference, Frulio discloses a charge pump circuit which inhibits the clock signal supplied to the second charge pump circuit by the control signal STOP2. In other words, Frulio discloses changing the length of a period in which the clock signal is in a low state. However, Frulio fails to teach or suggest the feature that the length of a period in which the clock signal is in a high state is changed.

Thus, at a minimum, Frulio fails to disclose or suggest the feature of amended claim 6 which recites “a pulse width of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal.”

As it is well known that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art, *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994), and Frulio fails to do so for at least the foregoing reasons, it is clear that Frulio does not anticipate amended claim 6.

III. Summary

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

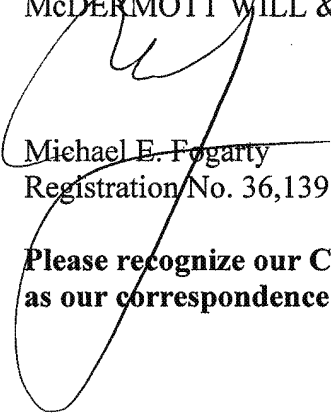
To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

Application No.: 12/497,090

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:rp
Facsimile: 202.756.8087
Date: December 22, 2010

**Please recognize our Customer No. 53080
as our correspondence address.**

WDC99 1956618-1.079195.0937

IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) An internal voltage generating circuit comprising:
a first boost circuit provided between a first voltage and a first terminal;
a second boost circuit provided between the first terminal and a second terminal;
a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and
a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.
2. (Original) The internal voltage generating circuit of claim 1, further comprising:
a clock comparing circuit configured to compare the first clock signal and the second clock signal to output a control signal to the buffer circuit.
3. (Original) An internal voltage generating circuit comprising:
a first charge pump circuit configured to generate a second voltage from a first voltage;
a second charge pump circuit configured to generate a third voltage from the second voltage;
a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and
a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal,
wherein the third clock signal is supplied to the second charge pump circuit.
4. (Original) The internal voltage generating circuit of claim 3, wherein

a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.

5. (Original) The internal voltage generating circuit of claim 3, further comprising:

a comparison circuit configured to output a first control signal in accordance with on the first clock signal and the second clock signal,

wherein the buffer circuit is controlled in accordance with the first control signal.

6. (Currently amended) An internal voltage generating circuit comprising:

a first charge pump circuit configured to generate a second voltage from a first voltage;
and

a second charge pump circuit configured to generate a third voltage from the second voltage,

wherein a ~~frequency~~ pulse width of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal.

7. (Original) The internal voltage generating circuit of claim 6, wherein

the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.

Electronic Acknowledgement Receipt

EFS ID:	9104063
Application Number:	12497090
International Application Number:	
Confirmation Number:	5747
Title of Invention:	INTERNAL VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Seiji Yamahira
Customer Number:	53080
Filer:	Michael E. Fogarty/Rosanna Pase
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	079195-0937
Receipt Date:	22-DEC-2010
Filing Date:	02-JUL-2009
Time Stamp:	20:51:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		079195_0937.pdf	224141 6bbc4a9f5260196011b837881c245a7a54b02aeb	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	2
	Claims	3	4
	Applicant Arguments/Remarks Made in an Amendment	5	7
Warnings:			
Information:			
Total Files Size (in bytes):		224141	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/497,090		Filing Date 07/02/2009		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY		
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A				N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				N/A		
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR		X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =				X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL				TOTAL		
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT	12/22/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0	X \$ =		OR	X \$52=	0	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$ =		OR	X \$220=	0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										Legal Instrument Examiner: /ANNIE c. SINGLETON/	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747

53080 7590 01/11/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

ZWEIZIG, JEFFERY SHAWN

ART UNIT	PAPER NUMBER
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2816

MAIL DATE	DELIVERY MODE
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01/11/2011

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 12/497,090	Applicant(s) YAMAHIRA, SEIJI	
	Examiner Jeffrey S. Zweizig	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 December 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-5 is/are allowed.
- 6) ☒ Claim(s) 6 and 7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 July 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Original claim 7 is rendered indefinite by the amendment to base claim 6. In claim 7 line 2 there is no longer any antecedent basis for "the frequency".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Amended claim 6 remains rejected under 35 U.S.C. 102(e) as being anticipated by Frulio et al. (7,579,902).

Fig. 7 shows a first charge pump 1 to m and a second charge pump m+1 to n as recited in claim 6. The frequency or pulse width of the clock to the second charge pump is changed according to control signal STOP2.

Response to Amendments and Arguments

The amendment to claim 6 is not seen to materially alter the scope of the claim. Like frequency, pulse width is an inherent characteristic of the clock, which is changed according to the control signal STOP2.

Conclusion

Claims 1-5 appear to be allowable over the Prior Art of record. Claim 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Frulio et al. does not appear to show the divider recited in claims 1, 3 and 7.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

536f1
/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 53080
	:	
Seiji YAMAHIRA	:	Confirmation Number: 5747
	:	
Application No.: 12/497,090	:	Group Art Unit: 2816
	:	
Filed: July 02, 2009	:	Examiner: Jeffery Shawn ZWEIZIG
	:	
For: INTERNAL VOLTAGE GENERATING CIRCUIT		

AMENDMENT UNDER 37 C.F.R. § 1.116

Mail Stop - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

In response to the Final Office Action dated January 11, 2011, having a three-month shortened statutory period for response set to expire on April 11, 2011, please amend the above-identified application as follows:

REMARKS

In response to the pending Office Action, Applicants have cancelled claim 6, without prejudice, and have rewritten claim 7 into independent format. Claim 7 has also been amended to address the rejection thereof under 35 U.S.C. § 112, second paragraph. As claim 7 was indicated to recite patentable subject matter, it is respectfully submitted that, as amended, claim 7 is in condition for allowance.

In addition for the foregoing, new claims 8 and 9 have been added. New claim 8 relates to an internal voltage generating circuit, and recites, *inter alia*, a length of a period in which a clock signal to be supplied to the second charge pump circuit is **in a high state** is changed in accordance with a control signal. Thus, new claim 8 expressly states that a length of a period in which the clock signal **is in a high state** is changed.

As noted in the Applicants' previous response, for example, as explained in paragraph [0070] of Applicants' published application, if the control signal FDE transitions from low to high, the pulse width of the frequency-divided clock signal FCK is twice the pulse width of the clock signal CLK, and the pulse width of the second boost clock signal PCK2 is changed to twice the pulse width of the clock signal CLK. Thus, in accordance with the claimed circuit, the length of the period in which the clock signal, to be supplied to the second charge pump circuit, is **in a high state** is changed.

Turning to the cited prior art reference, as also previously noted, Frulio discloses a charge pump circuit which inhibits the clock signal supplied to the second charge pump circuit by the control signal STOP2. As expressly noted in col. 4, line 65 – col. 5, line 1, when the STOP2 signal is "HIGH", the second clock generator does not output a clock signal (*i.e.*, the clock signal is inhibited). In other words, the clock signal is turned off. Thus, at best, Frulio discloses

changing the length of a period in which the clock signal is in a low state. Clearly, however, Frulio DOES NOT disclose or suggest a device in which the length of a period in which the clock signal is **in a high state** is changed.

Accordingly, at a minimum, Frulio fails to disclose or suggest the feature of claim 8 which recites **a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.**

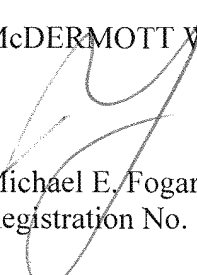
As it is well known that the factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art, *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994), and Frulio fails to do so for at least the foregoing reasons, it is clear that Frulio does not anticipate claim 8, or claim 9, which is dependent thereon.

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP


Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF:
Facsimile: 202.756.8087
Date: April 6, 2011

**Please recognize our Customer No. 53080
as our correspondence address.**

IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) An internal voltage generating circuit comprising:
a first boost circuit provided between a first voltage and a first terminal;
a second boost circuit provided between the first terminal and a second terminal;
a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and
a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.
2. (Original) The internal voltage generating circuit of claim 1, further comprising:
a clock comparing circuit configured to compare the first clock signal and the second clock signal to output a control signal to the buffer circuit.
3. (Original) An internal voltage generating circuit comprising:
a first charge pump circuit configured to generate a second voltage from a first voltage;
a second charge pump circuit configured to generate a third voltage from the second voltage;
a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and
a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal,
wherein the third clock signal is supplied to the second charge pump circuit.
4. (Original) The internal voltage generating circuit of claim 3, wherein

a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.

5. (Original) The internal voltage generating circuit of claim 3, further comprising:

a comparison circuit configured to output a first control signal in accordance with on the first clock signal and the second clock signal,

wherein the buffer circuit is controlled in accordance with the first control signal.

6. (Cancelled)

7. (Currently amended) ~~The internal voltage generating circuit of claim 6, wherein~~

An internal voltage generating circuit comprising:

a first charge pump circuit configured to generate a second voltage from a first voltage;

and

a second charge pump circuit configured to generate a third voltage from the second voltage,

wherein a frequency of a clock signal to be supplied to the second charge pump circuit is changed in accordance with a control signal, and

the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.

8. (New) An internal voltage generating circuit comprising:

a first charge pump circuit configured to generate a second voltage from a first voltage;

and

a second charge pump circuit configured to generate a third voltage from the second voltage,

wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.

9. (New) The internal voltage generating circuit of claim 8, wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.

Electronic Acknowledgement Receipt

EFS ID:	9826763
Application Number:	12497090
International Application Number:	
Confirmation Number:	5747
Title of Invention:	INTERNAL VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Seiji Yamahira
Customer Number:	53080
Filer:	Michael E. Fogarty/3328/Matilda Mason
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	079195-0937
Receipt Date:	06-APR-2011
Filing Date:	02-JUL-2009
Time Stamp:	22:18:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$810
RAM confirmation Number	6453
Deposit Account	500417
Authorized User	

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		079195-0937RCE.pdf	116541 3acd65a05d1c0e85f07a3724c4a637df1f73af0	yes	8
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Request for Continued Examination (RCE)		1	1	
	Amendment Submitted/Entered with Filing of CPA/RCE		2	8	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30265 a70fdc9b21a8dd307c41615767dc79ef35a6b3d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			146806		
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Electronic Patent Application Fee Transmittal				
Application Number:		12497090		
Filing Date:		02-Jul-2009		
Title of Invention:		INTERNAL VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Seiji Yamahira		
Filer:		Michael E. Fogarty/3328/Matilda Mason		
Attorney Docket Number:		079195-0937		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for continued examination	1801	1	810	810
Total in USD (\$)				810

Document code: WFEE

United States Patent and Trademark Office
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/497,090		Filing Date 07/02/2009		☐ To be Mailed
APPLICATION AS FILED – PART I									
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY	
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =			X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =			X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.									
APPLICATION AS AMENDED – PART II									
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	04/06/2011	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 8	Minus	** 20	= 0	X \$ =		OR X \$52=	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***3	= 1	X \$ =		OR X \$220=	220
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		OR TOTAL ADD'L FEE	220
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		OR TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.									
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".									
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Request for Continued Examination (RCE) Transmittal Address to: Mail Stop RCE Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number	12/497,090
	Filing Date	July 02, 2009
	First Named Inventor	Seiji YAMAHIRA
	Art Unit	2816
	Examiner Name	Jeffery Shawn ZWEIZIG
	Attorney Docket Number	079195-0937

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
 Request for Continued Education (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

- Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

ii. ☐ Other _____

b. ☐ Enclosed

i. ☐ Amendment/Reply

iii. ☐ Information Disclosure Statement (IDS)

ii. ☐ Affidavit(s)/Declaration(s)

iv. ☐ Other _____
- Miscellaneous**

a. ☐ Suspension of action of the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

b. ☐ Other _____
- Fees** The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 500417. I have enclosed a duplicate copy of this sheet.

i. ☒ RCE fee required under 37 CFR 1.17(e) \$810.00

ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)

iii. ☐ Other _____

b. ☐ Check in the amount of \$ _____ enclosed

c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	Date	April 6, 2011
Name (Print/Type) Michael E. Fogarty	Registration No.	36,139

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.		
Signature	Date	
Name(Print/Type)	Date	

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5747

SERIAL NUMBER 12/497,090	FILING or 371(c) DATE 07/02/2009 RULE	CLASS 327	GROUP ART UNIT 2816	ATTORNEY DOCKET NO. 079195-0937		
APPLICANTS Seiji Yamahira, Kyoto, JAPAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** /JZ/ JAPAN 2008-179566 07/09/2008 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/14/2009						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /JEFFREY SHAWN ZWEIZIG/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 8	TOTAL CLAIMS 7	INDEPENDENT CLAIMS 3
ADDRESS MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096 UNITED STATES						
TITLE INTERNAL VOLTAGE GENERATING CIRCUIT						
FILING FEE RECEIVED 1310	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
				☐ Credit		



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P.O. Box 1450
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

53080 7590 04/20/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER

ZWEIZIG, JEFFERY SHAWN

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 04/20/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747

TITLE OF INVENTION: INTERNAL VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	07/20/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747

TITLE OF INVENTION: INTERNAL VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	07/20/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZWEIG, JEFFERY SHAWN	2816	327-541000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747
53080 7590 04/20/2011 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096			EXAMINER ZWEIZIG, JEFFERY SHAWN	
			ART UNIT 2816	PAPER NUMBER
DATE MAILED: 04/20/2011				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 22 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 22 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/497,090	YAMAHIRA, SEIJI	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 4/6/11.
2. ☒ The allowed claim(s) is/are 1-5 and 7-9.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

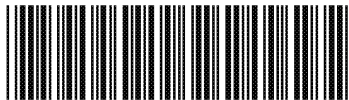
4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____. |
|---|---|

/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

Search Notes 	Application/Control No. 12497090	Applicant(s)/Patent Under Reexamination YAMAHIRA, SEIJI
	Examiner Jeffrey S Zweizig	Art Unit 2816

SEARCHED			
Class	Subclass	Date	Examiner
327	535, 536, 537	9/21/10	/JZ/
update	above	4/12/11	/JZ/

SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
327	536	4/12/11	/JZ/

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Electronic Acknowledgement Receipt

EFS ID:	10150370
Application Number:	12497090
International Application Number:	
Confirmation Number:	5747
Title of Invention:	INTERNAL VOLTAGE GENERATING CIRCUIT
First Named Inventor/Applicant Name:	Seiji Yamahira
Customer Number:	53080
Filer:	Michael E. Fogarty/stephanie sharrett
Filer Authorized By:	Michael E. Fogarty
Attorney Docket Number:	079195-0937
Receipt Date:	23-MAY-2011
Filing Date:	02-JUL-2009
Time Stamp:	17:07:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1822
RAM confirmation Number	4381
Deposit Account	500417
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Issue Fee Payment (PTO-85B)	IF.PDF	103345 63eab0266c99b645f7432336fb95832cd0a6a23a	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	33528 af260b727b4d33f39adff95e74887ae3b4786681	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			136873		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Electronic Patent Application Fee Transmittal				
Application Number:		12497090		
Filing Date:		02-Jul-2009		
Title of Invention:		INTERNAL VOLTAGE GENERATING CIRCUIT		
First Named Inventor/Applicant Name:		Seiji Yamahira		
Filer:		Michael E. Fogarty/stephanie sharrett		
Attorney Docket Number:		079195-0937		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				1822

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

53080 7590 04/20/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Customer No: 53080

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	07/02/2009	Seiji Yamahira	079195-0937	5747

TITLE OF INVENTION: INTERNAL VOLTAGE GENERATING CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	07/20/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZWEIZIG, JEFFERY SHAWN	2816	327-541000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

MCDERMOTT WILL & EMERY LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PANASONIC CORPORATION**Osaka, Japan**Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies **Four (4)**

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number **500417** (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Date **May 23, 2011**

Typed or printed name

Michael E. FogartyRegistration No. **36,139**

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/497,090	06/28/2011	7969231	079195-0937	5747

53080 7590 06/08/2011
MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 22 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Seiji Yamahira, Kyoto, JAPAN;

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: ADVANCED MEMORY TECHNOLOGIES LLCApplication No./Patent No.: 7969231Filed/Issue Date: June 28, 2011Titled: INTERNAL VOLTAGE GENERATING CIRCUITADVANCED MEMORY TECHNOLOGIES LLC, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: the inventor(s) To: PANASONIC CORPORATIONThe document was recorded in the United States Patent and Trademark Office at
Reel 023266, Frame 0680, or for which a copy thereof is attached.2. From: PANASONIC CORPORATION To: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD.The document was recorded in the United States Patent and Trademark Office at
Reel 053570, Frame 0429, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)3. From: PANASONIC SEMICONDUCTOR SOLUTIONS CO., LTD. To: NUVOTON TECHNOLOGY CORPORATION JAPAN

The document was recorded in the United States Patent and Trademark Office at
 Reel 066849, Frame 0802, or for which a copy thereof is attached.

4. From: NUVOTON TECHNOLOGY CORPORATION JAPAN To: ADVANCED MEMORY TECHNOLOGIES LLC

The document was recorded in the United States Patent and Trademark Office at
 Reel 067184, Frame 0869, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Szymon M. Gurda/

Signature

Szymon M. Gurda

Printed or Typed Name

December 30, 2024

Date

58451

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION # 12/497,090	RECEIPT DATE / TIME 12/30/2024 10:27:16 PM Z ET	ATTORNEY DOCKET # 079195-0937
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Title of Invention

INTERNAL VOLTAGE GENERATING CIRCUIT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	7969231
CONFIRMATION #	5747	FILED BY	Yi Lu
PATENT CENTER #	68561166	FILING DATE	07/02/2009
CUSTOMER #	53080	FIRST NAMED INVENTOR	Seiji Yamahira
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Szymon Gurda

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA.pdf	2	Power of Attorney	1152 KB
aia0096.pdf	3	Assignee showing of ownership per 37 CFR 3.73	120 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA.pdf	CE8FC9263F7403322CCA44DA7726192D87096587E6419A3999 4B0877BD463083EE8DB3084DB5BBDDC65F643F56791A8DE7 2E66959D86B47C5B12481E96AD6B05
aia0096.pdf	C2BEF4829ECF608E92B6C89D2CBE34E7AB05EDDFC2F41663 FE0E5BE5F952068976EFD01D3E18D1846FB57956EF30B4826

93184B458D2D0D88ECBACC497D6613B

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	7969231
	Issue Date	June 28, 2011
	First Named Inventor	Saiji YAMAHIRA
	Title	INTERNAL VOLTAGE GENERATING CIRCUIT
	Attorney Docket No.	0870-04135 US

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

27197

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

SIGNATURE of Applicant or Patent Owner

Signature

Date

December 28, 2024

Name

Saiji Yamahira

Telephone

Title and Company

Authorized Signatory, ADVANCED MEMORY TECHNOLOGIES LLC

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/497,090	07/02/2009	Seiji Yamahira	079195-0937

CONFIRMATION NO. 5747

53080

Rimon PC - Panasonic Corporation
8300 Greensboro Dr.
Suite 500
McLean, VA 22102

POWER OF ATTORNEY NOTICE



OC000000082992074

Date Mailed: 01/14/2025

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/497,090	07/02/2009	Seiji Yamahira	079195-0937

CONFIRMATION NO. 5747

27197
MICHAEL J. CHERSKOV
SZYMON M. GURDA
903 COMMERCE DR
SUITE 310
OAK BROOK, IL 60523

POA ACCEPTANCE LETTER



OC000000082992108

Date Mailed: 01/14/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/30/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/s/torres/