IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SK HYNIX, INC.,

Petitioner,

v.

ADVANCED MEMORY TECHNOLOGIES, LLC,

Patent Owner.

_____

Case No. IPR2025-01451

U.S. Patent No. 7,969,231

_____

DECLARATION OF CARL SECHEN, PH.D.

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D. Claim 1 29

(i) 1[pre]: *An internal voltage generating circuit comprising:* 29

(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;* 29

(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;* 32

(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and* 32

(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.* 33

E. Claim 3 45

(i) 3[pre]: *An internal voltage generating circuit comprising:* 45

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;* 45

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and* 46

(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.* 47

F. Claim 4 48

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein* 48

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.* 49

G. Claim 6 49

(i) 6[pre]: *An internal voltage generating circuit comprising:* 49

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,* 50

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and* 50

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.* 50

H. Claim 7 51

(i) 7[pre]: *An internal voltage generating circuit comprising:* 51

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,* 52

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.* 52

I. Claim 8 54

(i) 8[pre]: *The internal voltage generating circuit of claim 7,* 54

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.* 54

X. GROUND 2: ABE 57

A. Overview of Abe 57

B. Claim 1 57

(i) 1[pre]: *An internal voltage generating circuit comprising:* 57

(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;* 58

(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;* 59

(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and* 61

(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.* 66

C. Claim 3 69

(i) 3[pre]: *An internal voltage generating circuit comprising:* 69

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;* 70

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and* 71

(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.* 72

D. Claim 4 74

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein* 74

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.* 74

E. Claim 6 76

(i) 6[pre]: *An internal voltage generating circuit comprising:* 76

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,* 77

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and* 77

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.* 78

F. Claim 7 78

(i) 7[pre]: *An internal voltage generating circuit comprising:* 78

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,* 78

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.* 79

G. Claim 8 79

(i) 8[pre]: *The internal voltage generating circuit of claim 7,* 79

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.* 79

XI. GROUND 3: HIIRAGIZAWA 80

A. Overview of Hiiragizawa 80

B. Claim 3 81

(i) 3[pre]: *An internal voltage generating circuit comprising:* 81

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;* 82

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and* 85

(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.* 86

C. Claim 4 88

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein* 88

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.* 88

D. Claim 6 89

(i) 6[pre]: *An internal voltage generating circuit comprising:* 89

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,* 89

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and* 89

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.* 91

E. Claim 7 92

(i) 7[pre]: *An internal voltage generating circuit comprising:* 92

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,* 92

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.* 93

F. Claim 8 94

(i) 8[pre]: *The internal voltage generating circuit of claim 7,* 94

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.* 94

XII. GROUND 4: ITO 96

A. Overview of Ito 96

B. Claim 1 98

(i) 1[pre]: *An internal voltage generating circuit comprising:* 98

(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;* 99

(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;* 102

(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and* 104

(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.* 106

C. Claim 3 108

(i) 3[pre]: *An internal voltage generating circuit comprising:* 108

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;* 108

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and* 110

(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.* 111

D. Claim 4 114

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein* 114

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.* 114

E. Claim 6 119

(i) 6[pre]: *An internal voltage generating circuit comprising:* 119

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,* 119

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and* 119

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.*....122

F. Claim 7....122

(i) 7[pre]: *An internal voltage generating circuit comprising:*....122

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,*....123

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.*....123

G. Claim 8....124

(i) 8[pre]: *The internal voltage generating circuit of claim 7,*....124

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.*....124

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EXHIBIT LIST

Exhibit No.	Description
EX1001	U.S. Patent No. 7,969,231 ("'231 Patent")
EX1002	Declaration of Carl Sechen, Ph.D.
EX1003	[reserved]
EX1004	Curriculum Vitae of Dr. Carl Sechen
EX1005	Prosecution History for U.S. Pat. No. 7,969,231
EX1006	Patent Owner's District Court Infringement Chart for '231 Patent
EX1007	U.S. Pat. No. 7,099,167 ("Fujise")
EX1008	U.S. Pat. No. 6,836,177 ("Ito")
EX1009	U.S. Pat. No. 6,473,321 ("Kishimoto")
EX1010	U.S. Pat. No. 5,941,990 ("Hiiragizawa")
EX1011	U.S. Pat. No. 8,102,157 ("Abe")
EX1012	U.S. Pat. No. 5,999,475 ("Futatsuya")
EX1013	U.S. Pat. No. 7,579,902 ("Frulio")
EX1014	U.S. Pat. No. 6,080,205 ("Oshikawa")

DECLARATION OF CARL SECHEN, PH. D

I, Carl Sechen, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained on behalf of SK hynix, Inc. ("SK hynix" or "Petitioner") to testify as an expert in this *Inter Partes* Review ("IPR") proceeding. I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I have prepared this declaration in connection with SK hynix's related petition for IPR of U.S. Patent No. 7,969,231 ("the '231 Patent"), which I am informed is being filed concurrently with this declaration. I have been asked to provide certain opinions relating to the patentability of the '231 Patent. Specifically, I have been asked to provide my opinion regarding whether claims 1, 3, 4, 6, 7, and 8 of the '231 Patent ("the Challenged Claims") are invalid as obvious in view of certain prior art.

3. I receive compensation at an hourly rate of $500 per hour for my time working on this matter, plus expenses. I have no financial interest in SK hynix or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The conclusions I present are due to my own judgment.

II. BACKGROUND AND QUALIFICATIONS

4. My qualifications and credentials are set forth herein as further evidenced by my curriculum vitae (addendum hereto).

5. I earned a B.E.E. in Electrical Engineering from the University of Minnesota in 1975, followed by an M.S. in Electrical Engineering from the Massachusetts Institute of Technology in 1977. I earned a Ph.D. in Electrical Engineering from the University of California, Berkeley in 1986.

6. I have been a Professor of Electrical Engineering for 30 years. Since August 15, 2005, I have been a Professor of Electrical and Computer Engineering at the University of Texas at Dallas. From July 1992 to August 14, 2005, I served as a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I served as an Assistant Professor and then Associate Professor of Electrical Engineering at Yale University.

7. Over these years, my research has focused on the design and computer-aided design of digital integrated circuits, including the design of dynamic random-access memory ("DRAM") and static random-access memory ("SRAM") modules. I have also designed several chips that included various types of embedded DRAM (eDRAM). In this research work, I have designed multiple sense amplifier circuits for the various DRAMs, embedded DRAMs, and SRAMs. I have authored or

coauthored over 200 papers and one book, the majority of which concern digital integrated circuit design and memory design.

8. As a professor, I have developed and taught numerous courses, including several courses that teach digital integrated circuit design and memory design, including extensive coverage of flash memory design. I have taught these courses continuously for the past 30 years. I have taught digital integrated circuit design and memory design, including flash memory design, to undergraduate and graduate students at the University of Washington and at the University of Texas at Dallas. DRAM and embedded DRAM design is covered in these courses, as is the design of sense amplifier circuits for various types of memory. NAND-Flash memory design is taught in detail, including both SLC (single-level cell) and MLC (multi-level cell) variants.

9. I was elected a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE") in 2002 for contributions to placement and routing of ASICs. IEEE is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of "Fellow" to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

10. I received several research and teaching awards during my career. I received the Semiconductor Research Corporation's Inventor's Recognition Award in 1988 and in 2001. I also received the Technical Excellence Award from the Semiconductor Research Corporation in 1994. While serving as Professor at the University of Washington, I received the Outstanding Research Advisor award from the Department of Electrical Engineering in 2002. In 2008, I received the Distinguished Teacher of the Year Award from the Department of Electrical and Computer Engineering (ECE) at the University of Texas at Dallas. I also received the Distinguished Teaching Award for the Erik Johnson School of Engineering and Computer Science in 2014. In addition, I received the Graduate Teaching Excellence Award from the ECE Department at UT Dallas, May 2024.

11. Over the years, I have also received funding to conduct research in computer circuits and memory designs, including area-efficient and reliable embedded DRAM and SRAM design. Together with my graduate students, I have designed and fabricated various types of computational VLSI chips.

12. I am a co-inventor on four issued patents directed to transistor and computational logic technologies. Three of the patents concern transistor-level programmable logic.

13. Additional details about my employment history, fields of expertise, courses taught, and publications are further included in my CV attached as EX1004.

14. In summary, I am an expert in the field of circuit design generally and as applied within the context of the '231 Patent, including the design of flash memory and other non-volatile memories ("NVM"). As set forth above, my experience includes practical product development, including performance considerations and design choices involving the memory technology state of the art before the earliest, July 9, 2008, priority date applicable to the challenged claims.

15. As an expert, I am qualified to evaluate, interpret and rely on reports, patents, scholarly papers and professional opinions of others, within my areas of expertise, as to authenticity and accuracy. Moreover, I am qualified to provide an opinion as to what a person of ordinary skill in the art (POSITA) would have understood, known and concluded before July 9, 2008, including the context in which a POSITA would understand and construe teachings and terminology in written publications.

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

16. In preparing this Declaration, I have reviewed the '231 Patent and have considered each of the documents cited herein upon which I specifically rely. In formulating my opinions, I have relied upon my experience, education, and

knowledge in the relevant art, including other background documents. I have also considered the viewpoint of a person of ordinary skill in the art of computer memories at the time of the alleged invention of the '231 Patent, that is, close to, but earlier than July 9, 2008.

17. This Declaration is limited to my opinions on invalidity with respect to the Challenged Claims 1, 3, 4, 6, 7, and 8 of the '231 Patent. Those opinions, as set forth in detail in this Declaration, are summarized below:

A. All Challenged Claims are obvious over U.S. Patent No. 6,473,321 ("**Kishimoto**," KISHIMOTO), including incorporated references, in view of U.S. Patent No. 8,102,157 ("**Abe**," ABE) and the knowledge of a POSITA of the extensive background technology.

B. All Challenged Claims are obvious over **Abe** in view of the knowledge of a POSITA of the extensive background technology.

C. The Challenged Claims 3, 4, 6, 7, and 8 are anticipated by U.S. Patent No. 5,941,990 ("**Hiiragizawa**," HIIRAGIZAWA) in view of the knowledge of a POSITA of the extensive background technology.

D. All Challenged Claims are obvious over U.S. Patent No. 6,836,177 ("**Ito**," ITO) in view of the knowledge of a POSITA of the extensive background technology.

18. While Kishimoto, Abe, Hiiragizawa, Ito, and other references cited below as background technology form the primary bases for my opinion, I note that there are many other relevant references which further support a finding of invalidity as discussed herein. I reserve the possibility of amending or supplementing this Declaration should additional information arise which may affect my opinions.

IV. LEGAL UNDERSTANDING

19. I am not an attorney. However, as outlined in my curriculum vitae addended hereto, I have formed and presented opinions according to my technology expertise and the legal standards which are relevant to my analysis and opinions. I summarize here the understandings relevant for this declaration, noting that greater detail may be provided upon any cross-examination, and others may be provided for any amendment or supplementation reserved above.

20. **What Constitutes Prior Art that May Invalidate a Patent.** I understand that former 35 U.S.C. § 102 (*i.e.*, Pre-AIA § 102) listed conditions that may invalidate a patent, including what is considered "prior art" to a patent such as the '231 patent. I understand the most pertinent conditions are:

> (i) under § 102(a), if the invention was known or used by others in this country, or was patented or described in a printed publication in this or

a foreign country, before the date of the invention of the asserted patent; or

(ii) under § 102(b), if the invention was patented or described in a printed publication in this or a foreign country, or in public use or on sale in this country, more than one year before the effective filing date of the asserted patent; or

(iii) under § 102(e), if the invention was described in (a) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (b) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent.

21. I understand that one or more of the above conditions apply to the art relied upon here for my invalidity analysis.

22. **How the Prior Art Is Applied in the Invalidity Analysis: Anticipation.** I understand that a patent claim may be found to be invalid as "anticipated" under a subsection of Pre-AIA 35 U.S.C. § 102 if a single prior art reference (including any other prior art incorporated by reference in the prior art document) under that subsection describes every element of the claim explicitly or

inherently (*i.e.*, necessarily present) as understood by a POSITA to allow making and using the claimed invention.

23. **How the Prior Art Is Applied in the Invalidity Analysis: Obviousness.** I understand that a patent claim may be invalid as "obvious" under Pre-AIA 35 U.S.C. § 103 if the differences between the claimed invention and the prior art (including any other prior art incorporated by reference in the prior art document) are such that the claimed invention, as a whole, would have been obvious to a POSITA before the effective filing date of the claimed invention. The analysis calls for consideration of (a) level of ordinary skill in the pertinent art; (b) the scope and content of the prior art; (c) the differences between the prior art as a whole and the claim at issue; and (d) as appropriate, objective indicia of non-obviousness. The objective indicia, appropriate if there is a nexus with the claimed invention, include: (1) commercial success attributable to the invention; (2) long-felt but unsolved need for the invention; (3) failure of others; (4) skepticism by experts; (5) praise by others; (6) teaching away by others; (7) recognition of a problem which the claimed invention addresses; (8) copying by others; and (9) unexpected results.

24. I understand that obviousness may be found on a single reference (and any of its incorporated references) considered in view of the knowledge of the POSITA, and that a patent that incorporates another document by reference includes

the disclosure of the incorporated document as if it was explicitly contained in the patent. Where multiple references are proffered, I understand that while there is no requirement of an explicit teaching, suggestion or motivation to combine, generally there needs to be put forth some reason why a POSITA (if only by common sense or ordinary creativity) would have made the particular combination and that there is a reasonable expectation of success of the combination.

V. BACKGROUND OF THE RELEVANT TECHNOLOGY

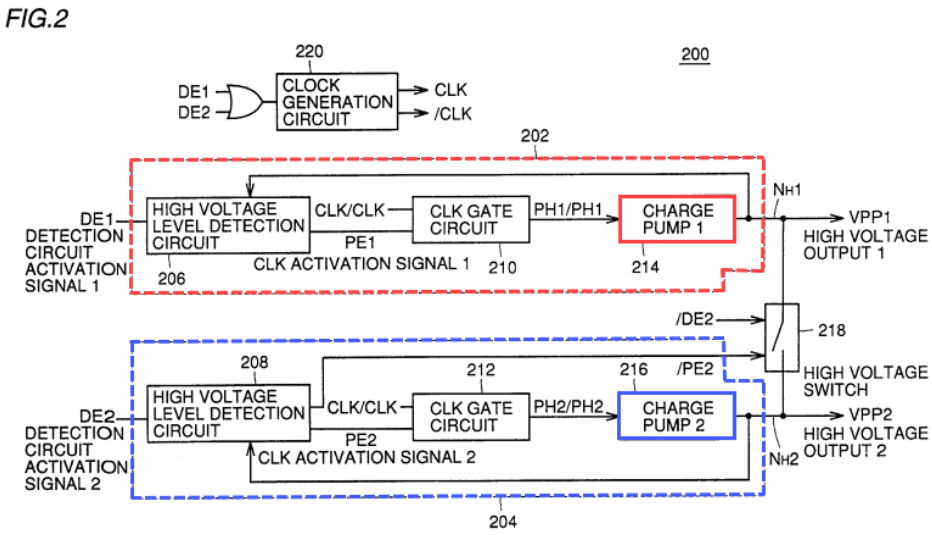
A. Boost Circuit / Charge Pump

25. Boost circuits (*i.e.*, charge pumps) are circuits that take a supply voltage and increase, or "boost," the supply voltage to output a higher voltage. *See* '231 Patent at 1:19-24. Long before the July 9, 2008 priority date of the '231 patent, boost circuits were widely used in memory devices such as a flash memory because the higher voltage output of a boost circuit was used for writing and erasing programmable elements. *See* '231 Patent at 1:16-24.

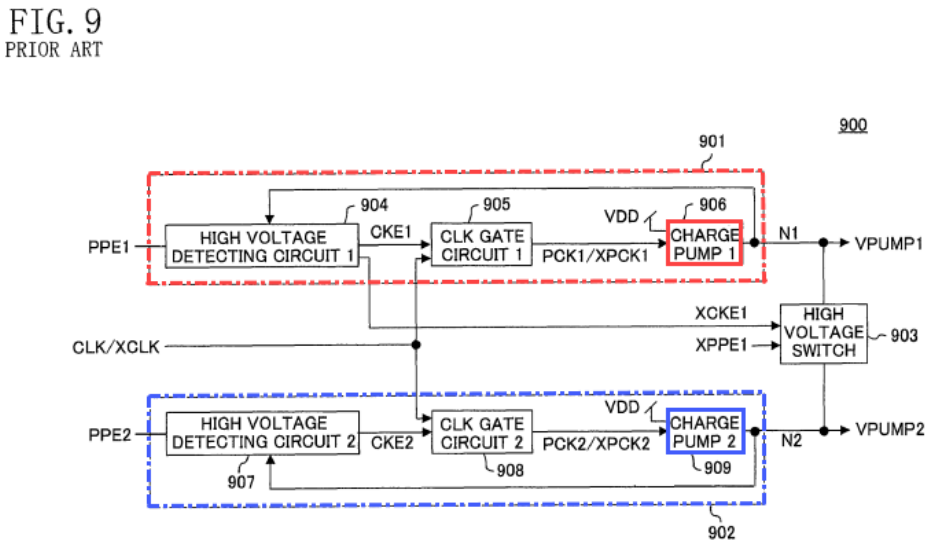
26. The '231 Patent itself admits that boost circuits were known in the art ***for at least a decade*** before the July 9, 2008 priority date. *See* '231 Patent at 1:25-27 (referencing prior art U.S. Pat. No. 5,999,475, *i.e.*, Futatsuya, which was filed in 1998). Futatsuya discloses in Fig. 2 a "high voltage generation circuit" including "**a first boosting circuit 202**" and "**a second boosting circuit 204**" for semiconductor

memory devices. *See* Futatsuya at 9:4-13. The first and second boosting circuits in Futatsuya also include **charge pump circuits 214** and **216**, respectively. *See* Futatsuya at 9:21-43.

Futatsuya Fig. 2



'231 Patent Fig. 9



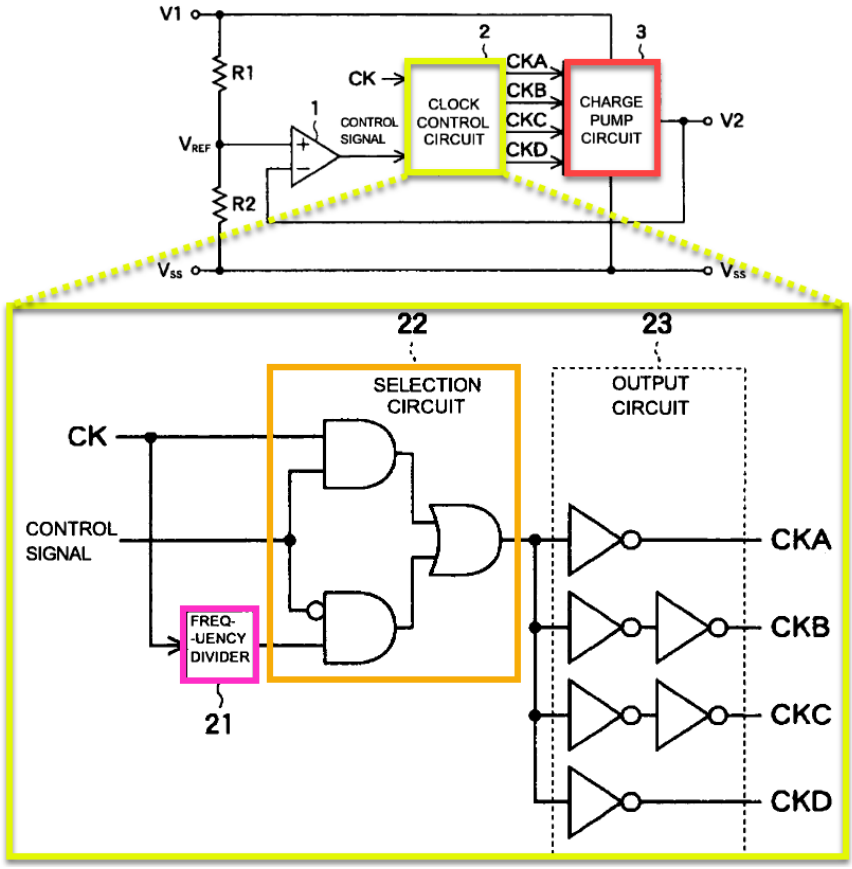
B. Frequency Divider and Buffer (Selection)

27. It was known long before the July 8, 2008 priority date that boost circuits in a voltage generating circuit were driven by clock signals. *See, e.g.*, Futatsuya at 9:21-31. Many techniques had been developed in the art before then to provide such driving clock signals to boost circuits and charge pumps.

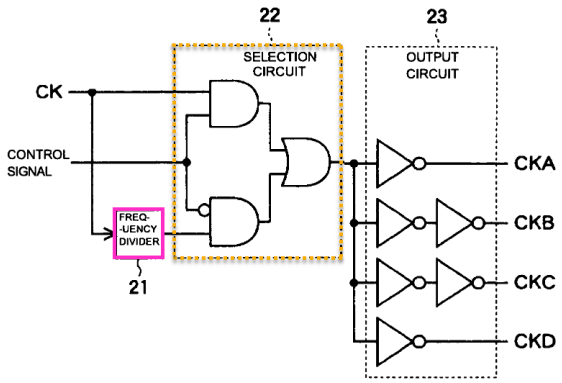
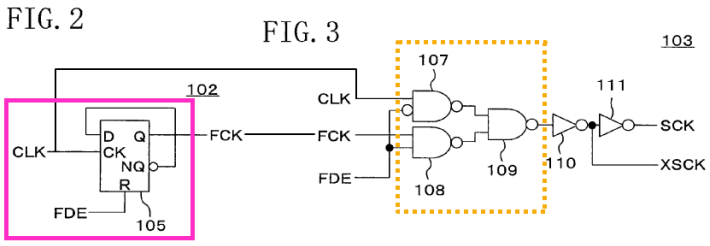
(i) Fujise

28. For example, in Fujise, a "clock control circuit 2" generates four clock signals (CKA through CKD) to drive "charge pump circuit 3." Fujise at 3:38-47.

Fujise Fig. 1 and Fig. 2



29. Figure 2 of Fujise shows the internal structure of "clock control circuit 2," which, among other components, includes a "**frequency divider 21** which divides an input clock signal CK" and a "**selection circuit 22** which ***selects***, based on the control signal provided by the comparator, either the input clock signal CK or a clock signal divided by the frequency divider 21." Fujise at 3:57-63. Fujise's selection circuit 22 is similar to the '231 patent's "buffer circuit," shown in Fig. 3, which is configured to "***select*** the first clock signal [CLK] or the second clock signal [FCK] and generate a third clock signal." *See* '231 patent at 4:21-23, 4:30-32. In fact, Fujise's selection circuit 22 is logically the same as the "buffer circuit" disclosed in the '231 Patent, and are referred to as two-to-one multiplexers in the art:

Fujise Fig. 2	**'231 Patent Figs. 2-3**
	

(ii) Hiiragizawa

30. As another example, Hiiragizawa, published in 1999 before the July 9, 2008 priority date of the '231 Patent, discloses another "charge pump circuit and the circuit portion related to its clock input" in Figure 6. *See* Hiiragizawa at 6:49-51.

Hiiragizawa Fig. 6

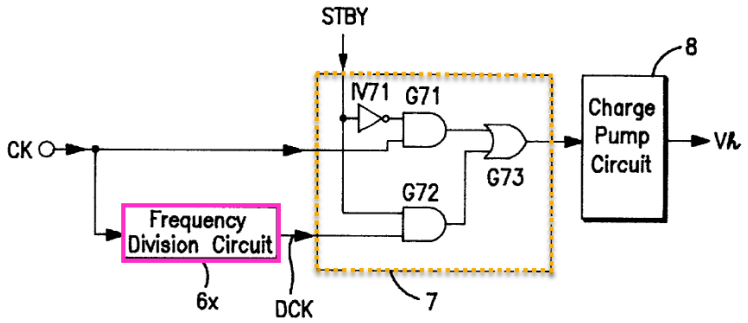
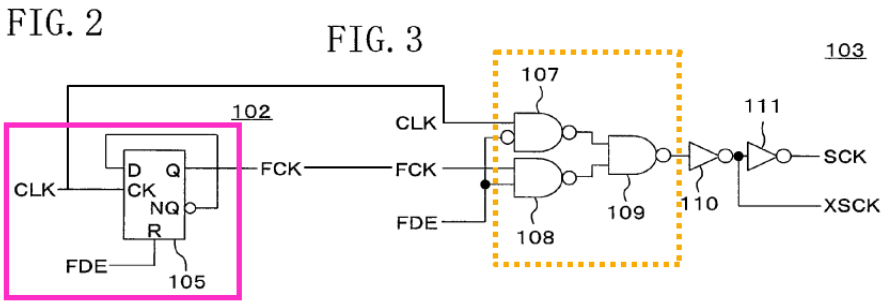


FIG. 6
PRIOR ART

'231 Patent Fig. 3



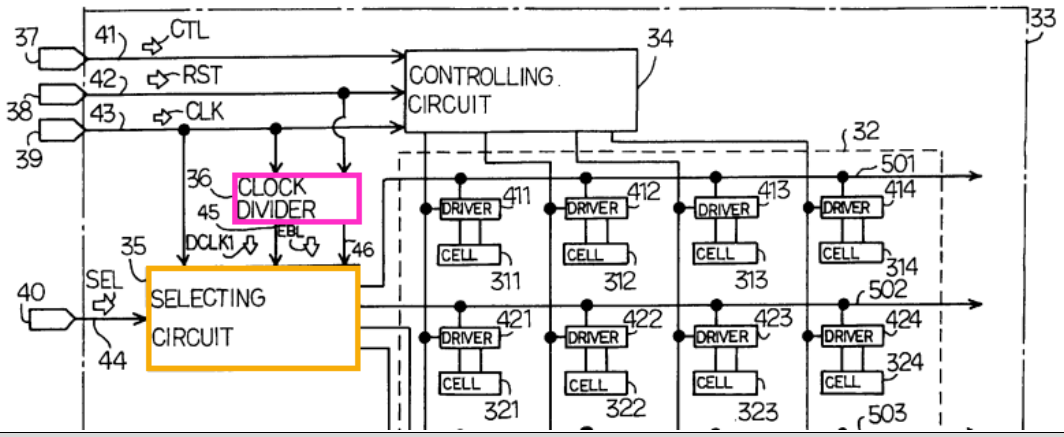
31. Hiiragizawa shows "a **frequency division circuit 6x** which divides the frequency of a clock signal CK from the outside into a specified frequency, and a **switching circuit** which … supplies the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x to the charge pump circuit 8

when the standby signal STBY is at the active level, and supplies the clock signal CK from the outside without change to the charge pump circuit 8 when the signal STBY is at the inactive level." *See* Hiiragizawa at 6:52-62.

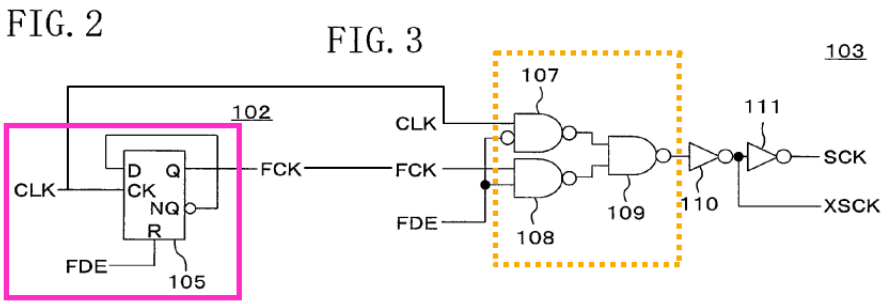
(iii) Oshikawa

32. As yet another example, Oshikawa, published in 2000 before the July 9, 2008 priority date, discloses a "clock divider 36" and a "selecting circuit 35" that supply clock signals to a plurality of "additional current drivers 411 to 444." Oshikawa at 4:17-20.

OSHIKAWA (Oshikawa) Fig. 7



'231 PATENT ('231 Patent) Fig. 3



33. Oshikawa's "**clock divider 36** is connected through signal lines 45 and 46 to the **selecting circuit 35**, and supplies a divided clock signal DCLK1 and an enable signal EBL through the signal lines 45/46 to the selecting circuit 35. The divided clock signal DCLK1 has a pulse interval twice as long as the pulse interval of the clock signal CLK." Oshikawa at 4:33-39.

34. Therefore, it is my opinion that the use of a frequency divider and a buffer (selection) circuit to generate a set of different clock signals for a boost circuit / charge pump was a well-known technique long before the July 9, 2008 priority date of the '231 Patent, as demonstrated by at least Fujise, Hiiragizawa, and Oshikawa shown above.

VI. PERSON OF ORDINARY SKILL IN THE ART (POSITA)

35. I am informed by counsel that "a person of ordinary skill in the art at the time of the inventions" ("POSITA") is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the invention. I have further been informed that this hypothetical POSITA would also be a person of ordinary creativity, capable of understanding the scientific principles applicable to the relevant field, and not an automaton.

36. In view of this instruction, my experience with the issues, and the '231 Patent, in my opinion, a POSITA for the '231 Patent had at least a master's degree

in electrical engineering, computer engineering, physics, or a related field, with at least two years of experience in the field of integrated circuits and/or memory devices. Less work experience may be compensated by a higher level of education or vice versa. I exceeded this level by July 9, 2008.

VII. THE '231 PATENT

37. Having read many patents, I am of the opinion that the '231 Patent does not claim anything that might be considered new. The claims of the '231 Patent cover well-known and, in some instances, decades-old building blocks of voltage supply circuitry for memory devices, such as boost circuits, charge pumps, frequency dividers, and buffer (selection) circuits implemented as a multiplexer.

A. The Challenged Claims

38. I understand the following claims of the '231 Patent are being challenged by SK hynix (the "Challenged Claims") and I have been asked to opine on them specifically. I reserve the right to opine on other claims of the '231 Patent if I am asked to do so.

Cl. #	Claim Limitation
1[pre]	An internal voltage generating circuit comprising:
1[a]	a first boost circuit provided between a first voltage and a first terminal;

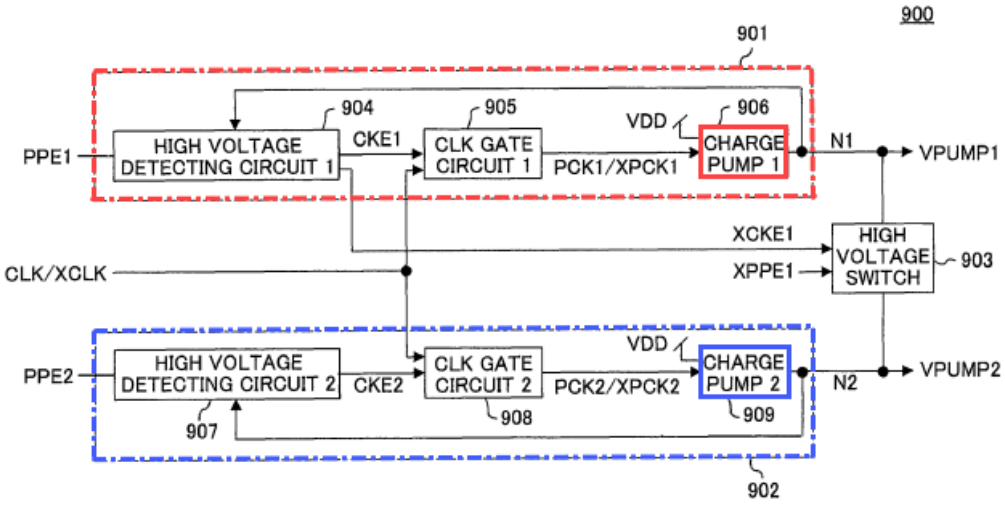
Cl. #	Claim Limitation
1[b]	a second boost circuit provided between the first terminal and a second terminal;
1[c]	a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and
1[d]	a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.
3[pre]	An internal voltage generating circuit comprising:
3[a]	a first charge pump circuit configured to generate a second voltage from a first voltage;
3[b]	a second charge pump circuit configured to generate a third voltage from the second voltage;
3[c]	a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and
3[d]	a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal,
3[e]	wherein the third clock signal is supplied to the second charge pump circuit.
4[pre]	The internal voltage generating circuit of claim 3, wherein
4[a]	a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.
6[pre]	An internal voltage generating circuit comprising:
6[a]	a first charge pump circuit configured to generate a second voltage from a first voltage; and

Cl. #	Claim Limitation
6[b]	a second charge pump circuit configured to generate a third voltage from the second voltage,
6[c]	wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and
6[d]	the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.
7[pre]	An internal voltage generating circuit comprising:
7[a]	a first charge pump circuit configured to generate a second voltage from a first voltage; and
7[b]	a second charge pump circuit configured to generate a third voltage from the second voltage,
7[c]	wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.
8[pre]	The internal voltage generating circuit of claim 7,
8[a]	wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.

B. The ’231 Patent Specification

39. The ’231 patent specification admits that an internal voltage generating circuit having a first boost circuit and a second boost circuit had long been known in the art, shown in Figure 9. *See* ’231 Patent at 1:25-37 (noting Fig. 9’s origin in the Futatsuya prior art).

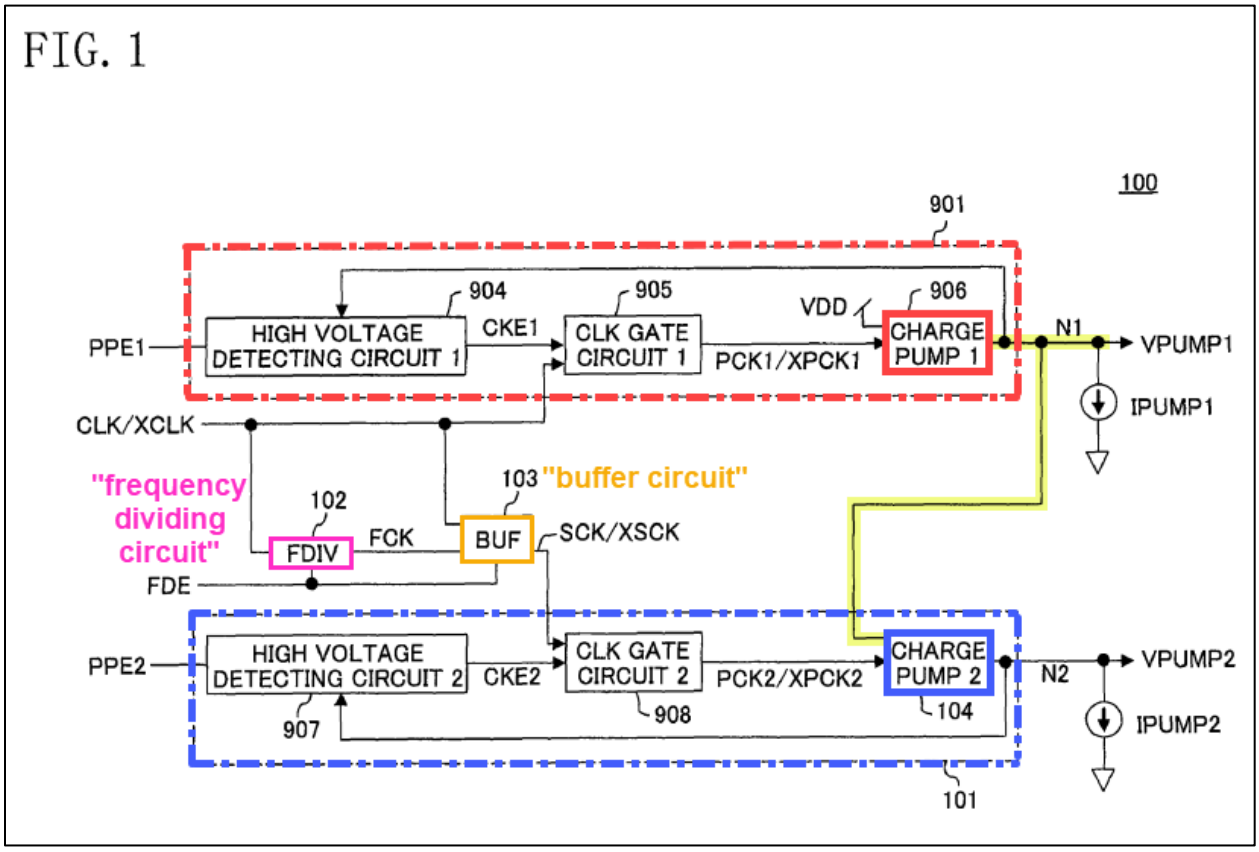
FIG. 9
PRIOR ART



40. In the prior art internal voltage generating circuit above, the first and second boost circuits are supplied by a first clock signal and a second clock signal, respectively. *See* '231 Patent at 1:38-48 ("first boost clock signals PCK1 and XPCK1") and 1:49-60 ("second boost clock signals PCK2 and XPCK2").

41. While the **first boost circuit 901** and **second boost circuit 902** in Figure 9 above are arranged in parallel (*i.e.*, their respective outputs, VPUMP1 and VPUMP2, are connected by high voltage switch 903), the '231 Patent proposes connecting the two boost circuits ***serially***, and driving the second boost circuit with a ***divided*** clock signal generated by a **frequency dividing circuit** and a **buffer circuit**. The serial connection, in which the output N1 of the first boost circuit 901 is input to the second boost circuit 101, is traced in yellow in Figure 1 below.

FIG. 1



42. The '231 Patent does not purport to have invented frequency dividing circuits or buffer (selection) circuits themselves, which were widely-used components of analog circuitry long before the July 9, 2008 priority date, as I explained above in § V.B.

C. Prosecution History Of The '231 Patent

43. I have reviewed the prosecution history of the '231 Patent in EX1005. In the first office action, the Examiner rejected original claim 6 as being anticipated by Frulio but found original claims 1-5 allowable. *See* '231 Patent Prosecution History at p. 74. Compared to original independent claim 3, original independent

claim 6 omitted limitations directed to "a frequency dividing circuit" and "a buffer circuit," both of which also appeared in original claims 1-5 that were found to be allowable. *See id.* at pp. 4-5. In the same office action, the Examiner also objected to original claim 7 as being dependent upon an original independent claim 6 but stated it would be allowable if rewritten in independent form. *See id.* at p. 74. Original claim 7 recited similar subject matter as the "frequency dividing circuit" and "buffer circuit" in allowable claims 1-5. *See id.* at p. 5.

44. Subsequently, the applicant attempted to overcome the Examiner's rejections by amending original claim 6 to introduce additional matter, but failed to persuade the Examiner with that addition. *See* '231 Patent Prosecution History at pp. 78-81 (attempted amendment and argument from the applicant) and pp. 87-92 (the Examiner noting that "[t]he amendment to claim 6 is not seen to materially alter the scope of the claim.").

45. Therefore, in the next turn, the applicant cancelled original claim 6, rewrote original claim 7 in independent form, and introduced new claims 8-9 directed to similar subject matter as original claim 7. *See* '231 Patent Prosecution History at pp, 98-99. With this amendment, all pending claims were allowed. *See id.* at p. 113. Accordingly, it is my understanding as a POSITA that the basis of the

Examiner's decision to grant the '231 Patent was the subject matter in the "frequency dividing circuit" and "buffer circuit" limitations.

VIII. CLAIM CONSTRUCTION

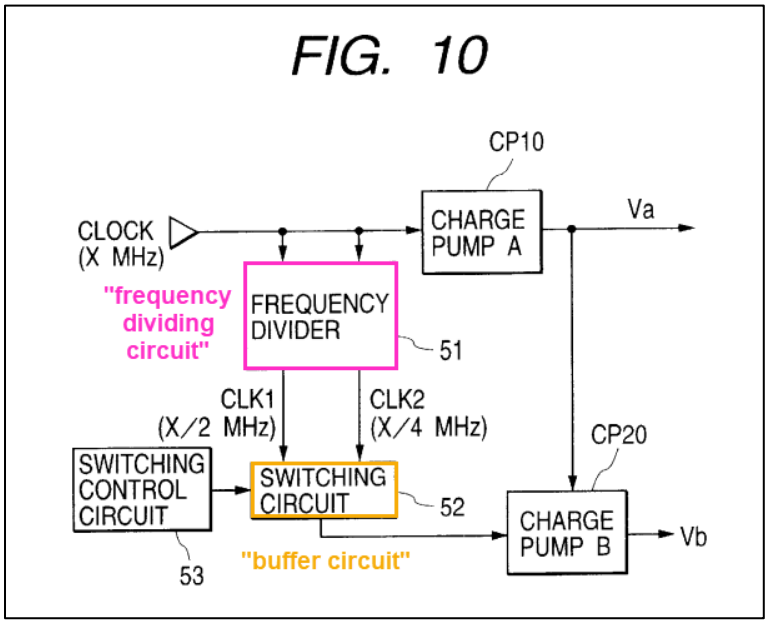
46. I have been informed that patent claims terms should be understood in accordance with their plain and ordinary meanings to a POSITA. In my opinion, it is not necessary to construe any of the claim terms of the '231 Patent in order to determine that the Challenged Claims are invalid. To the extent relevant, I have applied the plain meaning of certain terms in my analysis of Grounds 1-4 below.

IX. GROUND 1: KISHIMOTO IN VIEW OF ABE

A. Overview of Kishimoto and State of the Art

47. Kishimoto is prior art under at least pre-AIA 35 U.S.C. §§ 102(a)-(b) because it was patented on Oct. 29, 2002, before the July 9, 2008 priority date of the '231 Patent. Based on my review of the '231 Patent Prosecution History, I understand that Kishimoto was not considered by the Examiner during prosecution.

48. Kishimoto discloses an internal voltage generating circuit in Fig. 10, which provides two serially connected charge pumps (*e.g.*, CP10 and CP20), "a frequency divider 51," and "a switching circuit 52 or a selector." Kishimoto at 15:66-16:12. Kishimoto supplies clock signal CLK0 to charge pump CP10 and either clock signals CLK1 or CLK2 to charge pump CP20, as shown in Figure 10.

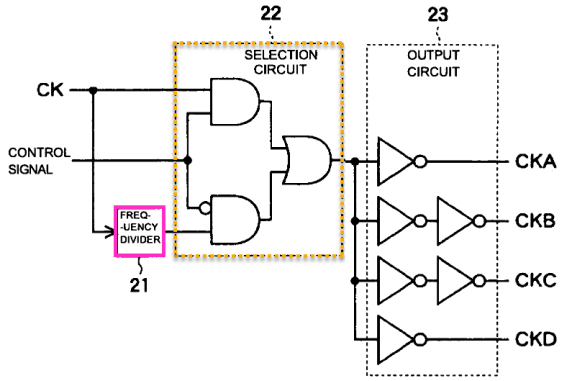


49. Kishimoto's switching circuit 52 differs slightly from the "buffer circuit" of the '231 Patent. In particular, Kishimoto's switching circuit 52 selects one of "the [divided] clocks CLK1 and CLK2" (Kishimoto at 16:2-4) to supply to the second charge pump CP20, rather than selecting either the original clock (CLK0) or the divided clocks (CLK1 or CLK2) as the "buffer circuit" of the '231 Patent does. But a POSITA reviewing Kishimoto at the time just before July 9, 2008 would have readily understood that such a difference is very trivial. Indeed, numerous prior art before the priority date of the '231 Patent had already disclosed such a concept.

50. For example, as discussed in § V.B, Fujise, Hiiragizawa, and Oshikawa each disclosed a similar buffer circuit that selects not only the divided clock(s), but also the original clock, to supply to a boost circuit / charge pump. *See, e.g.*, Fujise at 3:57-63; Hiiragizawa at 6:49-62; and Oshikawa at 4:17-39.

51. These disclosures are illustrated below. Further, as I will explain further below, Abe also discloses the same concept.

Fujise Fig. 2



Hiiragizawa Fig. 6

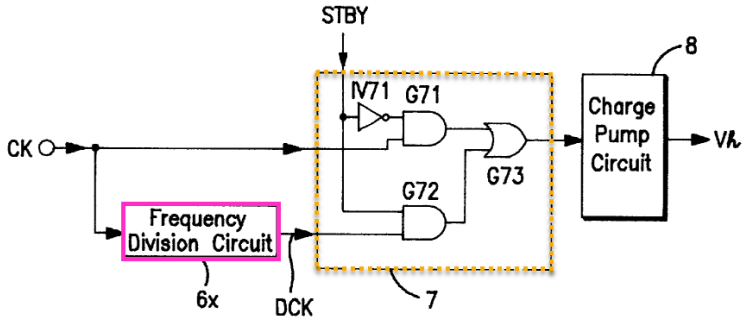
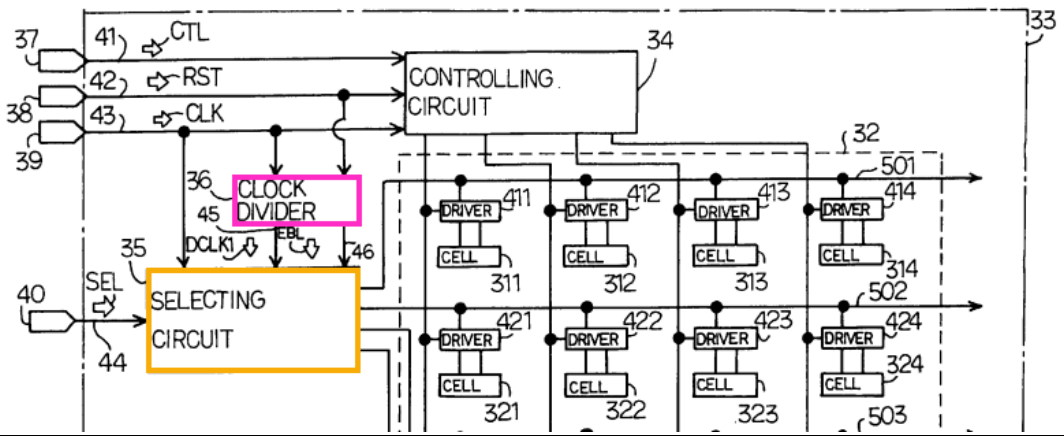


FIG. 6
PRIOR ART

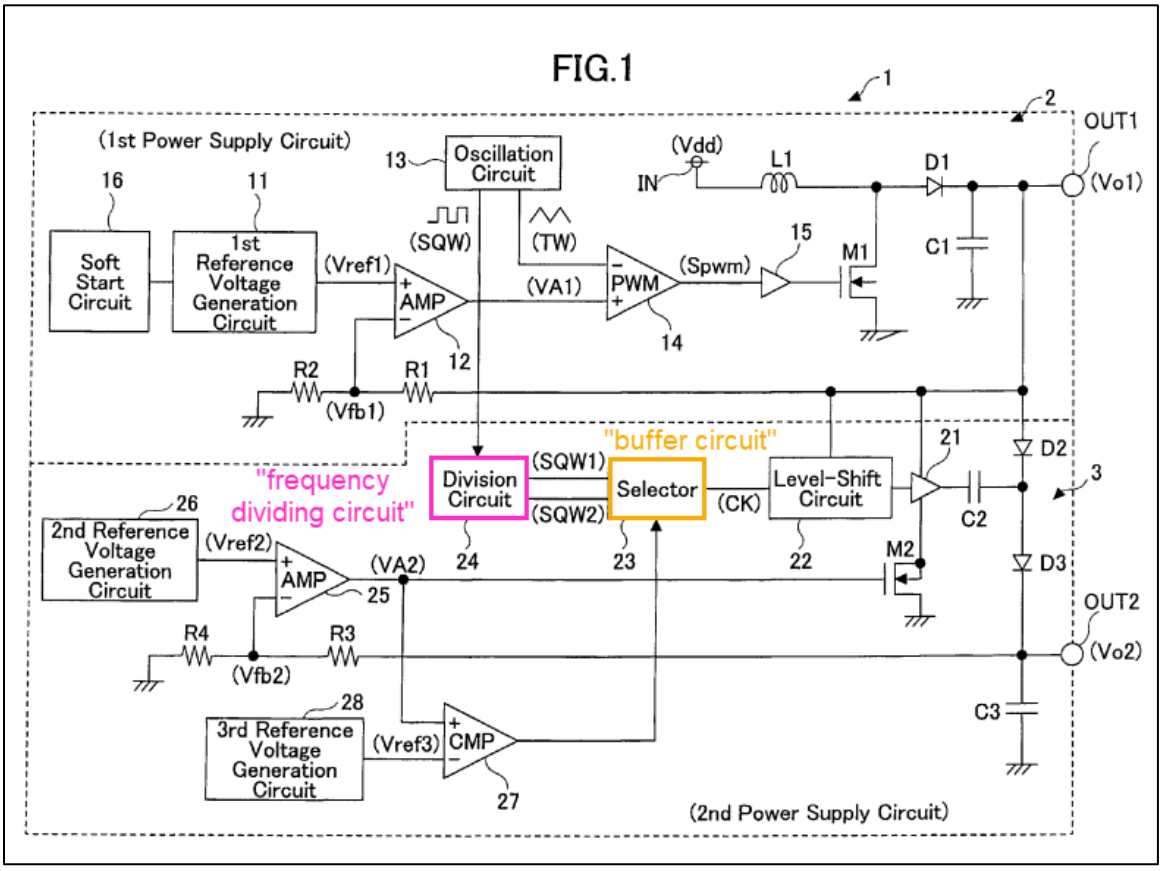
Oshikawa Fig. 7



B. Overview of Abe

52. Abe is prior art under at least pre-AIA 35 U.S.C. § 102(e) because it was filed as a PCT application on May 16, 2008, before the July 9, 2008 priority date of the '231 Patent, and because Abe designated the United States and was published in the English language (by Sep. 23, 2010). Based on my review of the '231 Patent Prosecution History, I understand that Abe was not considered by the Examiner during prosecution.

53. Similar to Kishimoto, Abe teaches an internal voltage generating circuit in Figure 1, as shown below. *See* Abe at 4:65-67.



54. Although Abe's Figure 1 shows an embodiment in which selector 23 selects one of the divided clock signals SQW1 or SQW2 to supply to the second power supply circuit 3, Abe expressly states that its disclosure is not limited to such an embodiment. *See* Abe at 8:51-52. In particular, Abe discloses that "instead of the rectangular signal SQW1 and the rectangular signal SQW2, the rectangular signal SQW may be used." *Id.* at 8:52-54. Further, Abe teaches that "the number of signals input to the selector 23 may be three or more," accounting for the fact that SQW, SQW1, and SQW2 may all be inputs to selector 23. *See id.* at 8:54-56.

C. Combining Kishimoto and Abe

55. Both Kishimoto and Abe are directed to the field of internal voltage generating circuits. *See, e.g.*, Kishimoto at Fig. 10; Abe at Fig. 1. Moreover, both Kishimoto and Abe disclose two serially-connected power supply circuits (such as charge pumps) driven by different clock signals. *See id.* Further, Kishimoto and Abe each implements a frequency dividing circuit (*e.g.*, Kishimoto's frequency divider 51 and Abe's division circuit 24) and a buffer (*e.g.*, Kishimoto's switching circuit 52 and Abe's selector 23) to provide the different clock signals to charge pumps.

56. While Kishimoto and Abe differ slightly in their implementations of the frequency dividing circuit and buffer, it is my opinion that a POSITA would have

understood these different implementations to be mere design choices that were well known in the art before the July 9, 2008 priority date of the '231 Patent. Specifically, Kishimoto's switching circuit 52 selects amongst the divided clock signals whereas Abe's selector 23 selects amongst both the original clock signal and the divided clock signals.

57. In my opinion, a POSITA would have been motivated to use Kishimoto's switching circuit 52 with Abe's selector 23, or vice versa, depending on the design needs at hand, *i.e.*, whether the original clock signal should also be selectable to drive a charge pump circuit. Such a configuration would have been made with a reasonable expectation of success because the use of a frequency dividing circuit and a buffer to supply clock signals in *either* of the foregoing mechanisms had been well-known in the field for a decade before the priority date of the '231 Patent.

58. My additional opinions regarding the motivation to combine Kishimoto and Abe and a POSITA's reasonable expectation of success for doing so are further discussed below with respect to limitation 1[d].

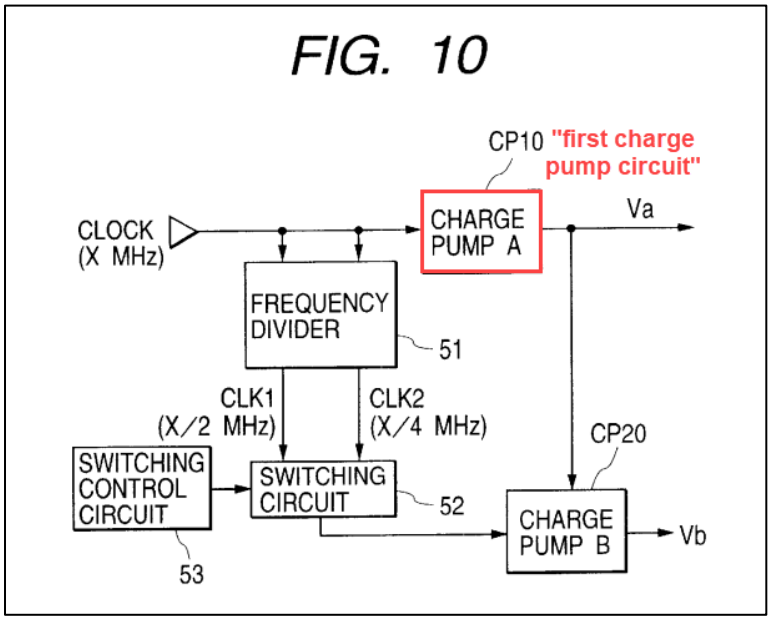
D. Claim 1

(i) 1[pre]: *An internal voltage generating circuit comprising:*

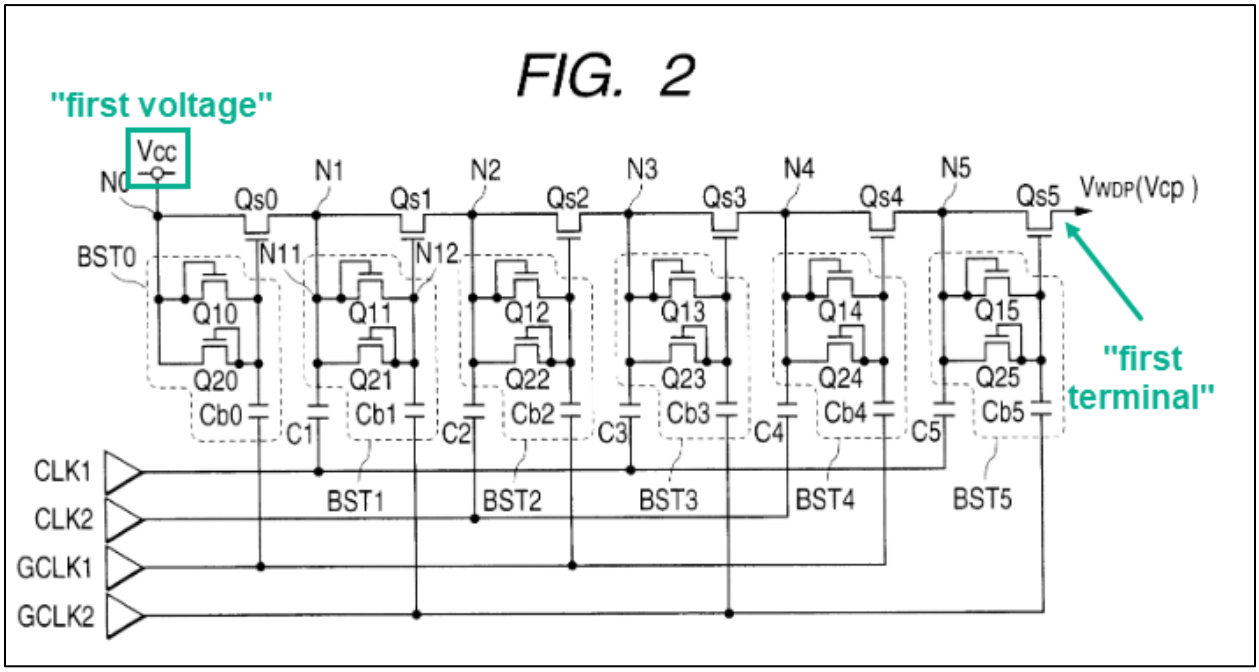
59. If the preamble is deemed to be limiting, it is my opinion that Kishimoto discloses an internal voltage generating circuit. Kishimoto describes "a semiconductor integrated circuit having an internal booster circuit." Kishimoto at Abstract. For example, in Figure 10, Kishimoto shows an embodiment that achieves "voltage boosting by 10 times or more." Kishimoto at 16:13-18.

(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;*

60. In my opinion, Kishimoto meets claim limitation 1[a]. Kishimoto discloses a first boost circuit in "**charge pump CP10**," as shown in the annotated Figure 10 below. *See* Kishimoto at 15:63-16:8. In my opinion, Kishimoto's charge pumps are a "boost circuit" because they are circuitry for "carrying out first stage ***voltage boosting*** on the basis of a source voltage." Kishimoto at Abstract.

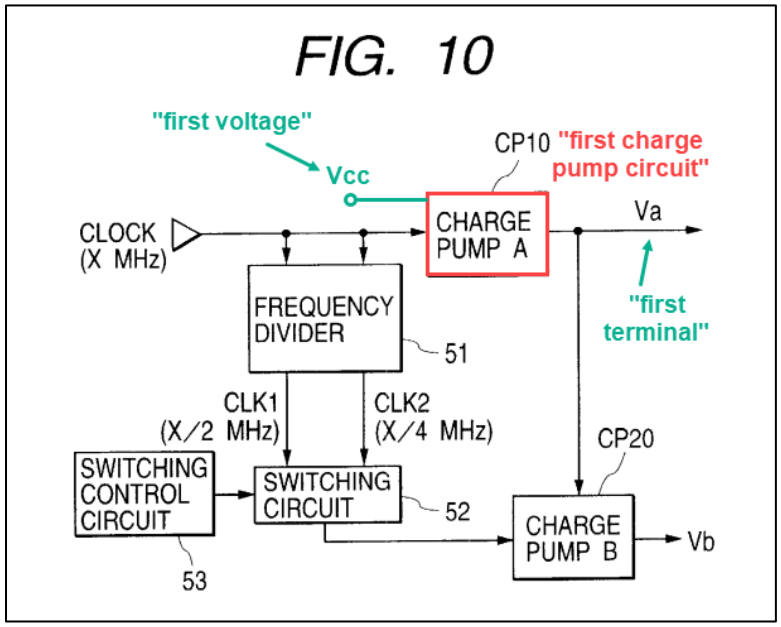


61. In my opinion, the first boost circuit (*i.e.*, CP10) in Kishimoto is "a parallel capacity type unit," shown in annotated Figure 2 below. *See* Kishimoto at 16:13-16, 5:24-26.



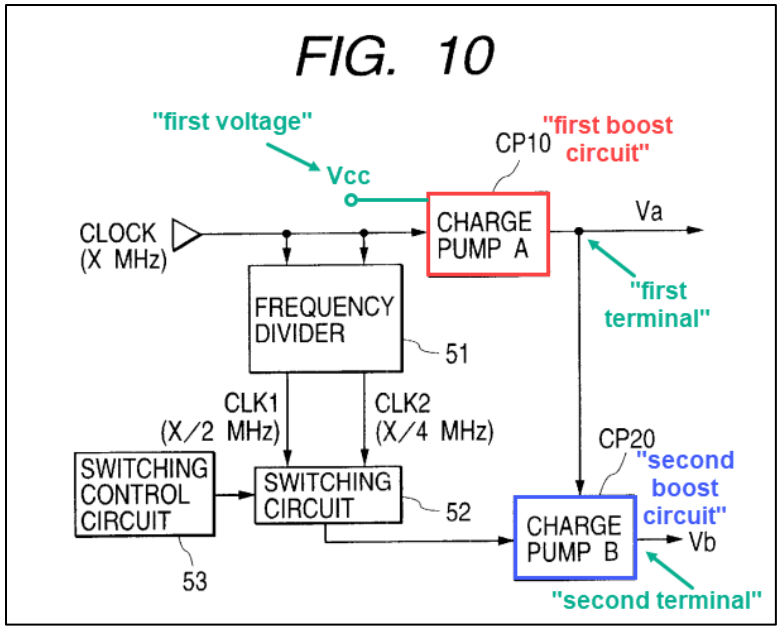
62. CP10 as shown in Figure 2 receives "external source voltage Vcc" to generate and transmit "voltage VWDP (VCP) … to circuits on the voltage supply receiving side." Kishimoto at 8:3-12. Therefore, in my opinion, Kishimoto's charge pump CP10 is provided between a first voltage (Vcc) and a first terminal (the output terminal of Qs5 leading to the voltage supply receiving side).

63. This structure of CP10 is also reflected in the internal voltage generating circuit of Figure 10, which I have modified below to call attention to the well-understood supply of Vcc to CP10.



(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;*

64. In my opinion, Kishimoto meets claim limitation 1[b]. Kishimoto discloses a second boost circuit in "**charge pump CP20**," as shown in the annotated Fig. 10 below. *See* Kishimoto at 15:63-16:8.

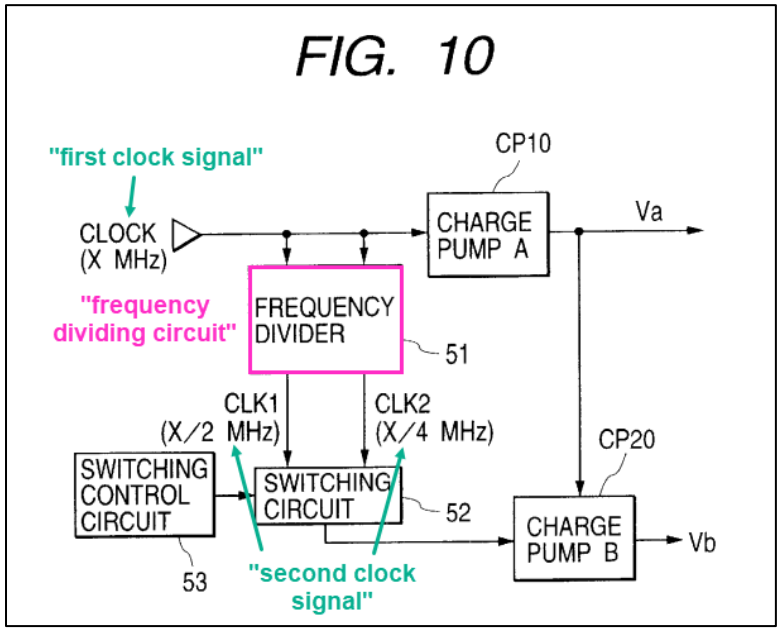


65. Therefore, in my opinion, the second boost circuit of Kishimoto (CP20) is provided between the first terminal (the output terminal of CP10) and the second terminal (the output terminal of CP20).

(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and*

66. In my opinion, Kishimoto meets claim limitation 1[c]. Kishimoto discloses "a **frequency divider 51** for dividing the frequency of a clock signal CLK0

for operating a charge pump CP10." Kishimoto at 15:66-16:1. Further, Kishimoto's "clocks CLK1 and CLK2 hav[e] undergone frequency division by the frequency divider 51." *Id.* at 16:3-4.

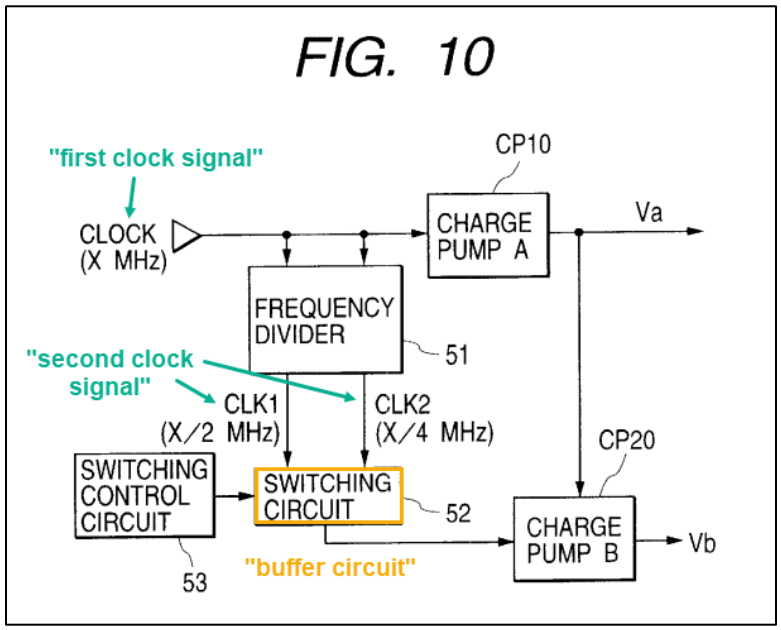


67. Accordingly, in my opinion, Kishimoto discloses a frequency dividing circuit (frequency divider 51) configured to divide a first clock signal (CLK0) to be supplied to the first boost circuit (CP10) to generate a second clock signal (either CLK1 or CLK2).

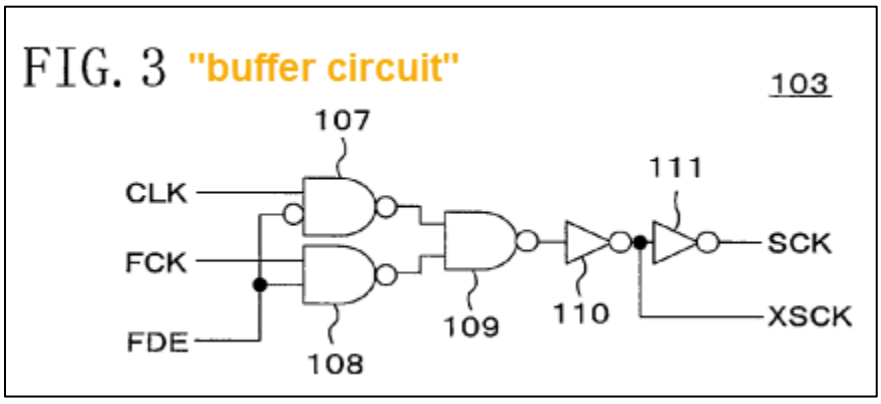
(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.*

68. In my opinion, Kishimoto meets claim limitation 1[d]. Kishimoto discloses "a **switching circuit 52** or a selector for switching the clocks CLK1 and

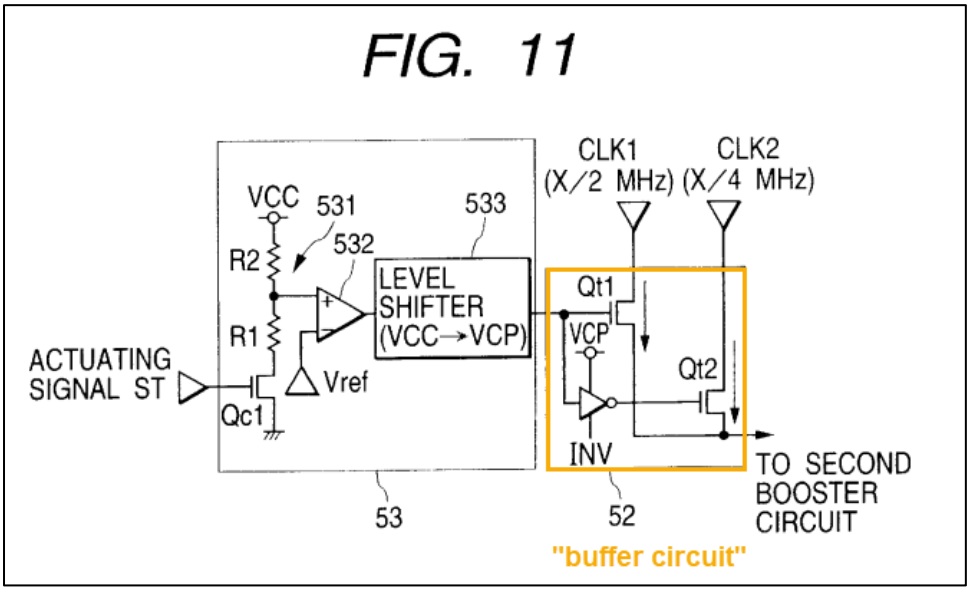
CLK2 … to operate the charge pump CP20 for carrying out the second stage of voltage boosting," as shown in annotations below. Kishimoto at 16:2-7.



69. In my opinion, at the time just before July 9, 2008, a POSITA would have understood the claimed "buffer circuit" in the '231 Patent to be a multiplexer. *See* '231 Patent at 6:7-17, Fig. 3. As a multiplexer, the '231 Patent's buffer circuit selects either CLK or FCK to output as SCK based on the control signal FDE.



70. Similarly, in my opinion, a POSITA would also have understood at the time that Kishimoto's switching circuit 52 is a multiplexer. An example of Kishimoto's switching circuit 52 is shown in Figure 11 shown below.



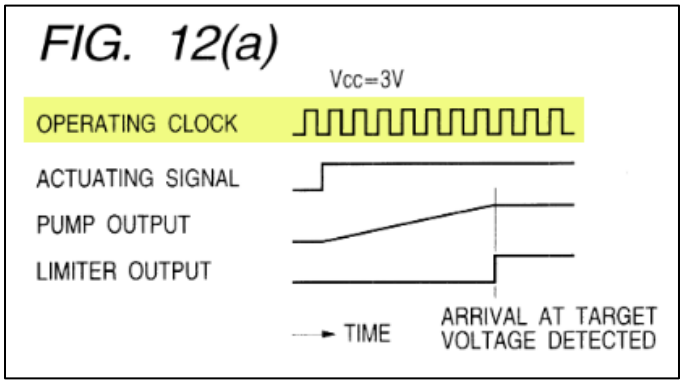
71. Similar to the claimed "buffer circuit" of the '231 Patent as a multiplexer, Kishimoto's switching circuit 52 selects either CLK1 or CLK2 to output to CP20 based on a control signal from the switching control circuit 53. Therefore, Kishimoto's switching circuit 52 can be mapped to the claimed "buffer circuit" of the '231 Patent.

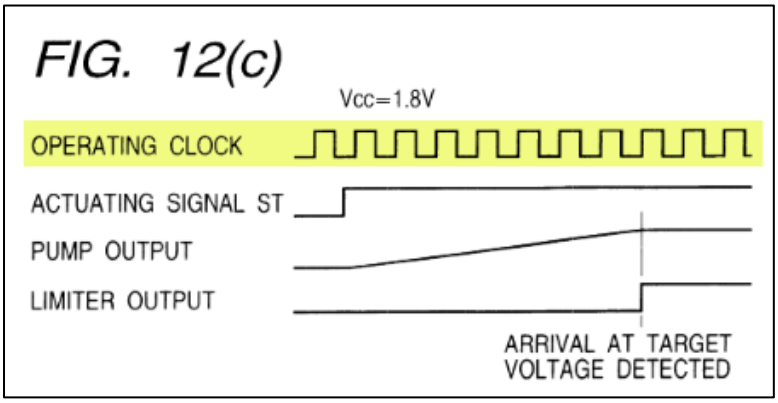
72. As such, it is my opinion that a POSITA would have understood Kishimoto discloses a buffer circuit (switching circuit 52) configured to select and supply the second clock signal (CLK1 or CLK2) to the second boost circuit (charge pump CP20).

73. I understand the Patent Owner may argue that claim limitation 1[d] requires ***both*** the first clock signal ***and*** the second clock signal be supplied by the buffer circuit, rather than either one ***or*** the other. If so, it is my opinion that a POSITA at the time of the '231 Patent would have found it obvious to modify Kishimoto's switching circuit 52 to select one of three clock signals (CLK0, CLK1, and CLK2) for charge pump CP20, rather than merely selecting one of the two clock signals expressly identified in Fig. 10 (CLK1 and CLK2).

74. *First*, Kishimoto itself provides a clear motivation for doing so. For example, the purpose behind selecting one of multiple clock signals to the second charge pump CP20 is to allow flexibility in varying the clock frequency that drives CP20. *See* Kishimoto at 16:2-8 ("a switching circuit 52 or a selector for switching the clocks CLK1 and CLK2 … ***so that the frequency of the clock signal PCLK to operate the charge pump CP20*** for carrying out the second stage of voltage boosting ***varies*** in accordance with a control signal from a switching control circuit 53").

75. Kishimoto even provides specific examples of driving the second charge pump CP20 with high and low clock frequencies. For example, Kishimoto's Figures 12a-12c are "timing chart showing the operating timing of the circuit of FIG.11," which is the "switching control circuit in FIG. 10." Kishimoto at 5:51-54.

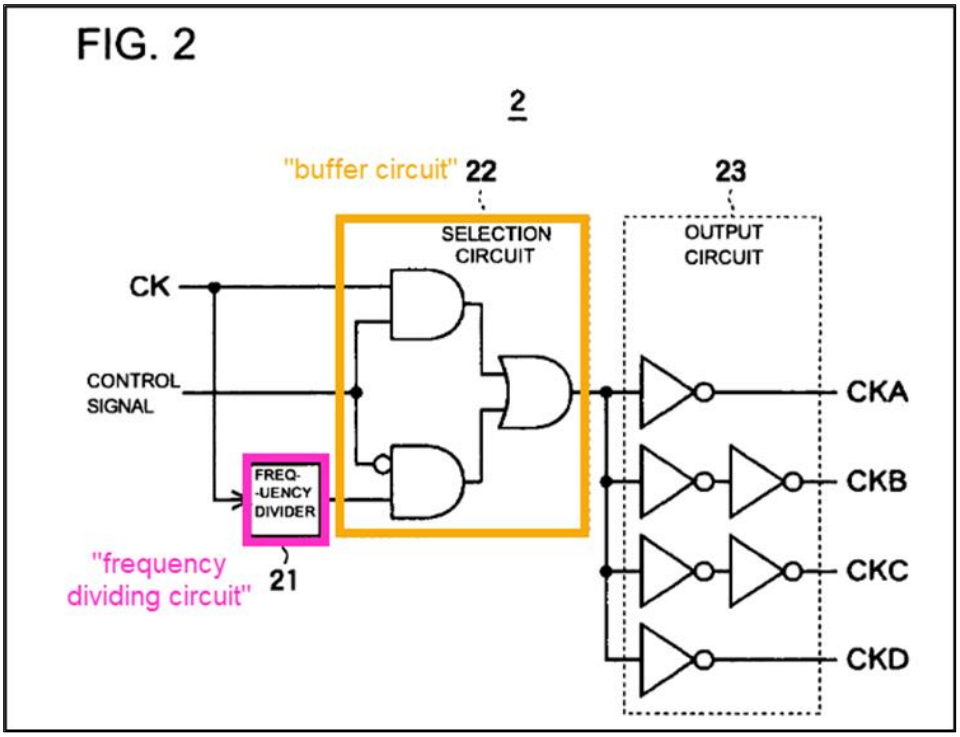




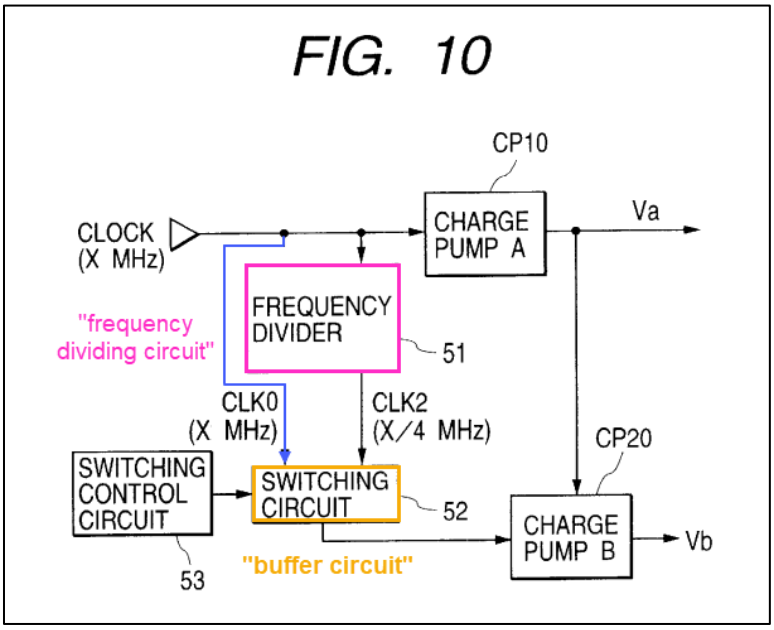
76. Specifically, CP20 "reached the target voltage" when "the clock frequency was ***high*** as shown in FIG. 12(a)," annotated above; and when the clock frequency is ***lowered*** "as shown in FIG. 12(c), the output of the charge pump CP20 … can eventually attain the target voltage even though it takes a longer time." Kishimoto at 17:16-25.

77. *Second*, it had been known long before the July 9, 2008 priority date of the '231 Patent to use a frequency divider and selection circuit to allow selection of ***both*** the original clock signal ***and*** the divided clock signal(s) to drive a charge pump. I have provided several prior art illustrating this in § V.B above.

78. For example, Fujise disclosed a "frequency divider 21 which divides an input clock signal CK" and a "selection circuit 22 which selects, based on the control signal provided by the comparator, ***either the input clock signal CK*** or ***a clock signal divided by the frequency divider 21***." Fujise at 3:57-63, Fig. 2.

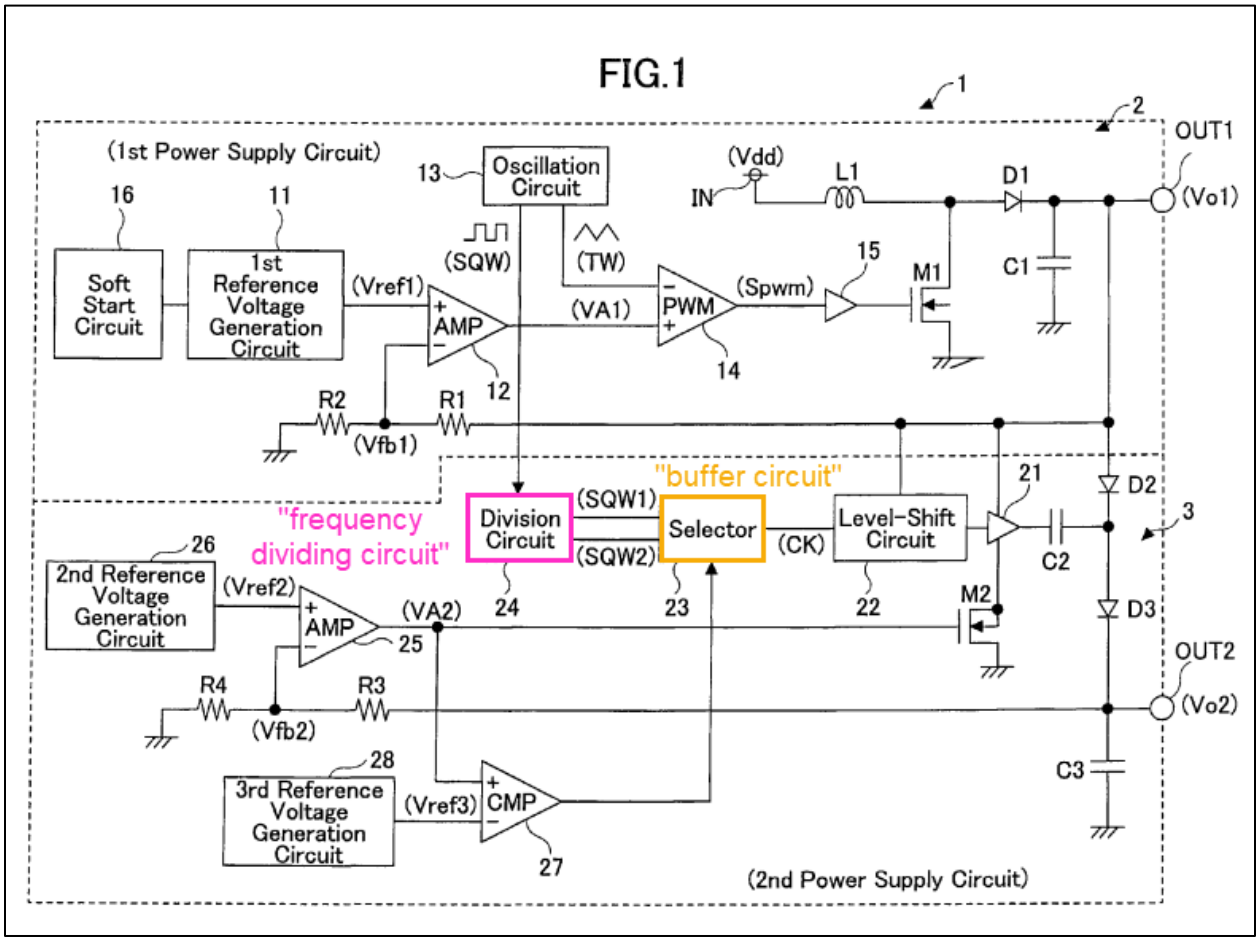


79. Modifying Kishimoto's switching circuit 52 to select either the original clock signal (CLK0) or a divided clock signal (CLK1 or CLK2) is trivial to implement and consistent with the above teachings to provide flexibility in driving CP20 with varying frequencies. Doing so would simply involve replacing one of the inputs to Kishimoto's switching circuit 52 with CLK0, as shown in blue annotation below.



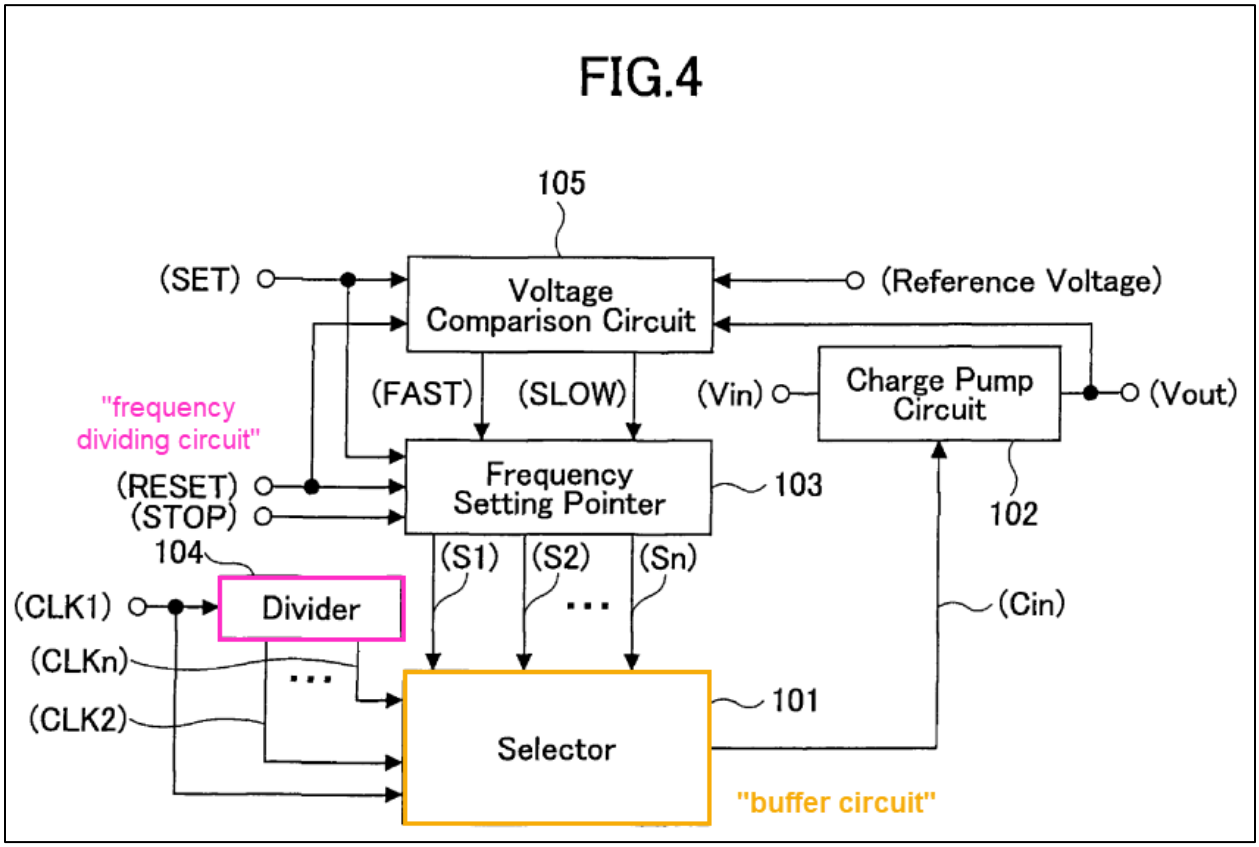
80. Further, in my opinion, a POSITA would have had a reasonable expectation of success by the July 9, 2008 priority date to carry out such a modification to further the stated objective of the switching circuit disclosed in Kishimoto's Fig. 10.

81. *Third*, before the priority date of the '231 Patent, a POSITA would also have been motivated to combine Kishimoto with Abe, which teaches an analogous buffer circuit that selects one of three inputs to supply to the second booster circuit. While the details of Abe are described in connection with Ground 2, which I explain below, Abe in pertinent part discloses a "multi-output power supply device 1" in Fig. 1, which includes, *inter alia*, "division circuit 24" and "selector 23," shown below. Abe at 5:20-22, 8:43-51.



82. Although Figure 1 of Abe illustrates one embodiment in which division circuit 24 divides the original clock signal "SQW" into SQW1 and SQW2 and selector 23 selects either SQW1 or SQW2, Abe is not limited to such an embodiment. Abe at 8:46-52. In particular, Abe discloses that, "instead of the rectangular signal SQW1 and the rectangular signal SQW2, ***the rectangular signal SQW may be used***." *Id.* at 8:52-54. Further, "the number of signals input to the selector 23 may be three or more." *Id.* at 8:54-56. In my opinion, this is the exact same modification to the switching circuit 52 in Kishimoto, where the original clock

CLK0 is also provided as an input to the switching circuit (*i.e.*, a "buffer circuit") and may be selected and supplied to the second charge pump CP20. As a matter of fact, Abe illustrates such a selector circuit in Figure 4, shown below.



83. Abe's "clock signal CLK1, ***and*** clock signals CLK2 through CLKn, which are signals obtained by dividing the clock signal CLK1 with a divider 104, are ***also input to the selector 101***" and supplied to charge pump circuit 102. Abe at 1:38-41.

84. In my opinion, it would have been obvious at the time of the July 9, 2008 priority date for a POSITA to combine the teachings of Kishimoto and Abe

with respect to the subject matter of claim limitation 1[d]. Kishimoto and Abe are analogous art in the same field of endeavor as the '231 Patent, *i.e.*, internal voltage generating circuitry. Abe is one concrete example in the prior art that demonstrates the proposed modification to Kishimoto's switching circuit 52—selecting and supplying both the original clock CLK0 and the divided clock CLK1 or CLK2 to the second charge pump CP20—which is already envisioned in Kishimoto and consistent with Kishimoto's stated objective, namely, to allow clocks of varying frequencies to drive CP20.

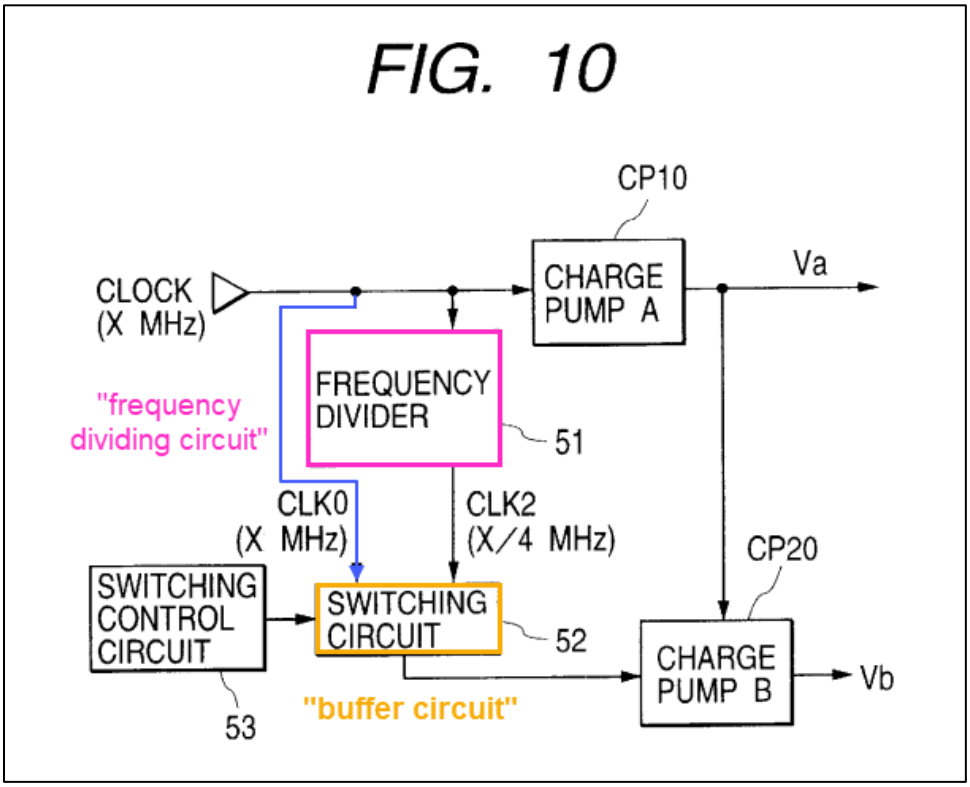
85. Both Kishimoto and Abe acknowledge that allowing clocks of varying frequencies to drive the second charge pump is highly desirable in the art.

86. For example, Kishimoto notes that "switching the frequency of operating clocks" allows the second charge pump to "reliably generate a boosted voltage of a desired level even if the source voltage is low." Kishimoto at 4:37-42, 7:17-21 ("to save power consumption by switching the frequency of operating clocks").

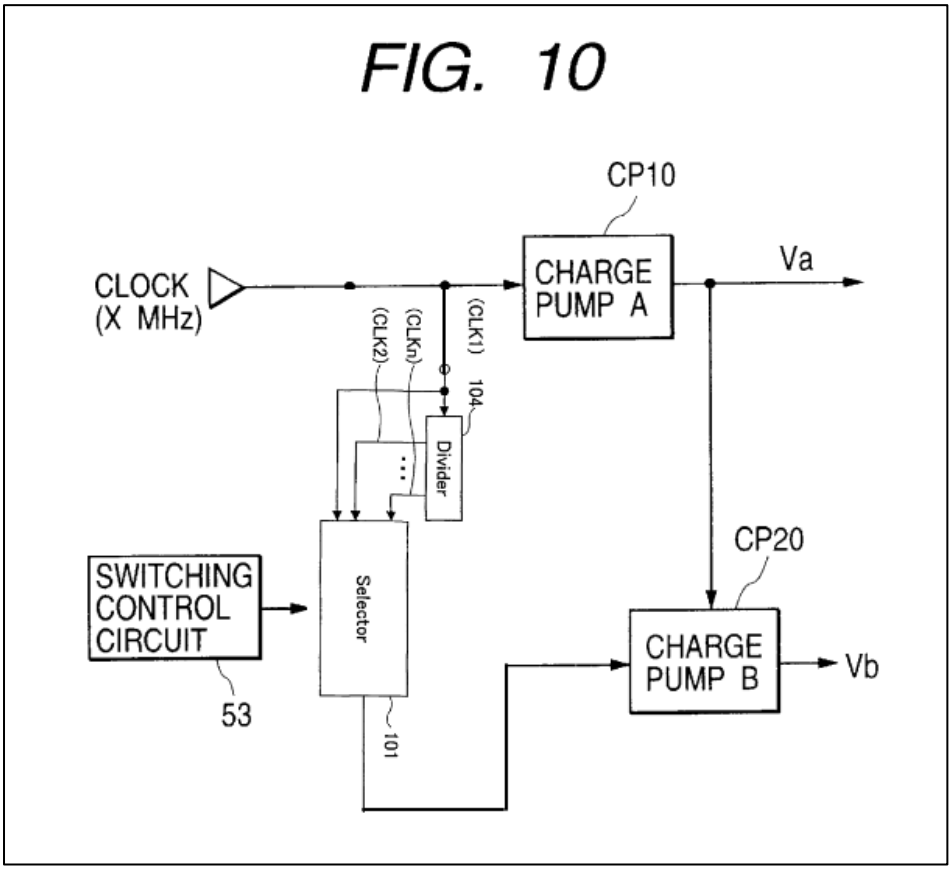
87. Moreover, Abe explains that "appropriately chang[ing] the frequency of the clock signal CK" supplied to the "second power supply circuit 3" makes it possible to "reduce spike noise compared to the case in which the same clock signal is used for the charge pump circuits," which "results in low noise." Abe at 9:1-10.

As such, it is my opinion that a POSITA attempting to improve the reliability of a boosted voltage, as motivated by Kishimoto, would have looked to the teachings of Abe for additional implementation details on variable clock frequencies.

88. Further, a POSITA would have had a reasonable expectation of success in modifying Kishimoto's switching circuit 52 to receive and select the original clock signal as its output, as disclosed by Abe. Such a modification would have been well within the expertise of a POSITA. For example, one possible modification simply entails replacing CLK1 with CLK0 as an input to Kishimoto's switching circuit 52, as shown in modified Fig. 10 below.



89. In my opinion, another possible modification would be to simply replace Kishimoto's frequency divider 51 and switching circuit 52 with Abe's divider 104 and selector 101, as shown below.



90. In fact, as Abe noted, one merely needs to "accordingly increase the number of control signal input terminals of the selector 23" when three or more inputs are fed into Abe's selector 23. Abe at 8:54-59. In my opinion, a POSITA is well-equipped to follow the guidance from Abe and modify Kishimoto accordingly.

91. Therefore, it is my opinion that claim limitation 1[d] is rendered obvious by Kishimoto as modified by the express disclosures in Abe.

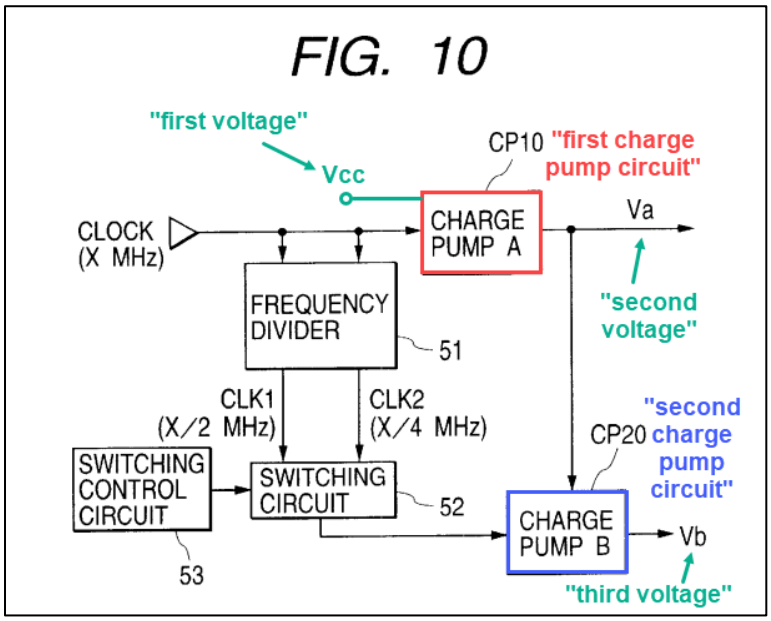
E. Claim 3

(i) 3[pre]: *An internal voltage generating circuit comprising:*

92. In my opinion, Kishimoto discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § IX.D.(i) above.

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;*

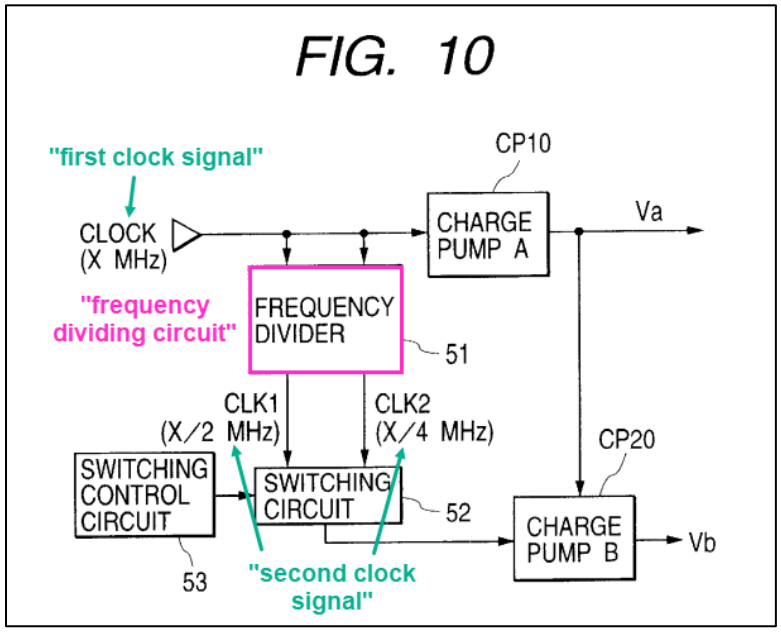
93. In my opinion, Kishimoto meets claim limitations 3[a] and 3[b]. As I explain above for claim limitations 1[a] and 1[b], Kishimoto discloses a first charge pump circuit in "charge pump A" (CP10) and a second charge pump circuit in "charge pump B" (CP20). *See* § IX.D.(ii) and § IX.D.(iii) above.



94. As shown in the annotated Figure 10 above, Kishimoto's charge pump A (CP10) is configured to generate a second voltage (Va) from a first voltage (Vcc), and its charge pump B (CP20) is configured to generate a third voltage (Vb) from the second voltage (Va).

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and*

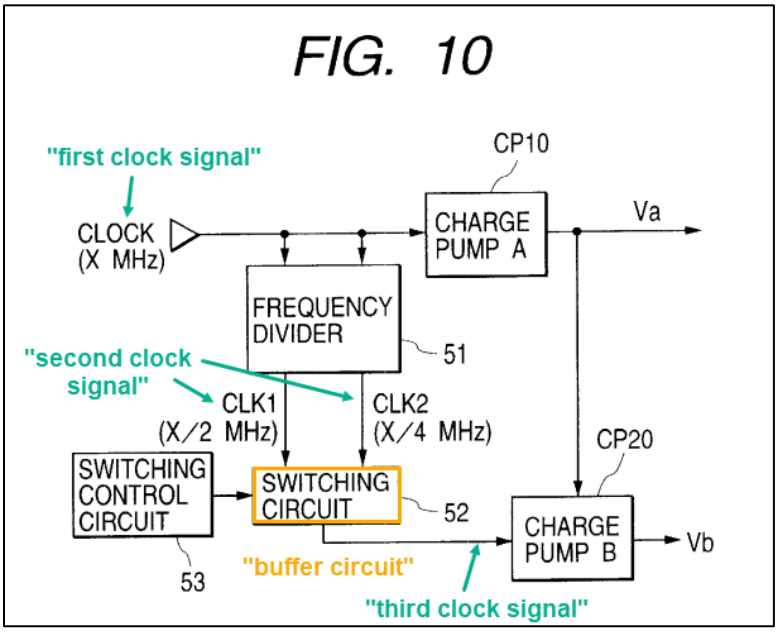
95. In my opinion, there is no additional requirement in claim limitation 3[c] than what is set forth in 1[c]. As I explained above in connection with claim limitation 1[c], Kishimoto discloses frequency divider 51 configured to divide CLK0 to generate CLK1 and CLK2. *See* § IX.D.(iv) above.



(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.*

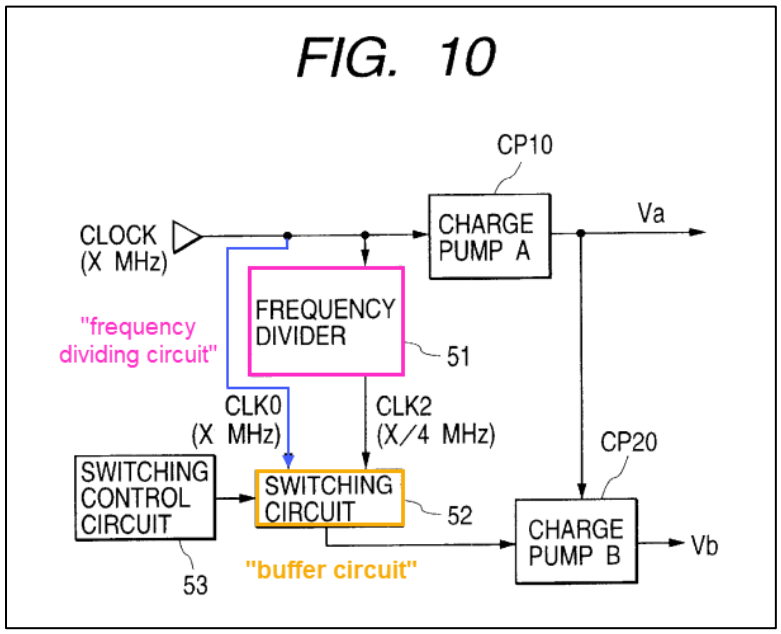
96. In my opinion, the only additional requirement of claim limitations 3[d]-3[e] beyond claim limitation 1[d] is to "generate a third clock signal." But this additional requirement is also taught in Kishimoto.

97. As I set forth above regarding claim limitation 1[d], Kishimoto discloses the generation of "clock signal PCLK to operate the charge pump CP20" by selecting either CLK1 or CLK2. Kishimoto at 16:2-6. Therefore, it is my opinion that Kishimoto discloses claim limitations 3[d] and 3[e].



98. I understand that Patent Owner may argue claim limitations 3[d] and 3[e] require Kishimoto's switching circuit to select ***both*** the original clock signal

CLK0 ***and*** one of the divided clock signals CLK1 or CLK2. In my opinion, Kishimoto and Abe render these claim limitations obvious. As discussed in § IX.C and § IV.D.(v), *supra*, a POSITA would have been motivated to modify Kishimoto in view of Abe to replace the CLK1 input to switching circuit 52 with CLK0 in Kishimoto such that CLK0 or CLK2 is supplied to charge pump B (CP20) as the third clock signal. As I explained in the sections above, such a modification would have had a reasonable expectation of success. *See id.*



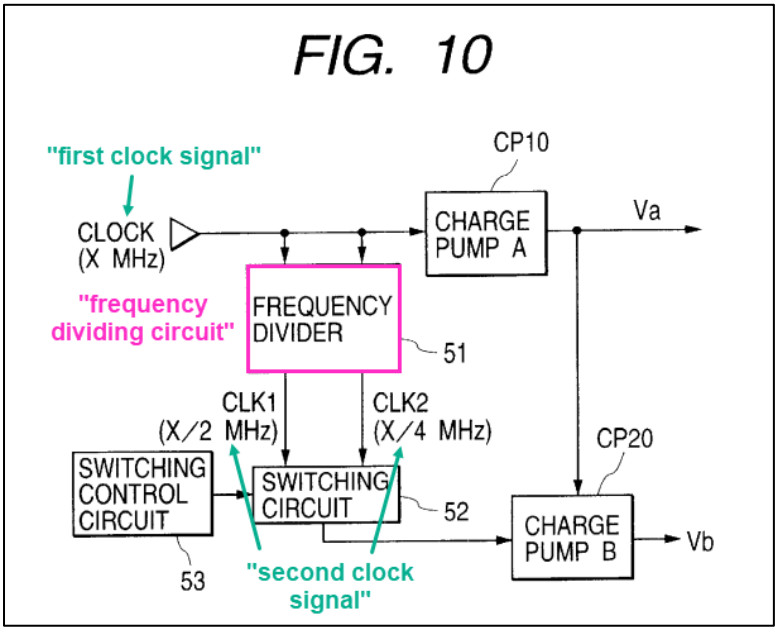
F. Claim 4

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein*

99. In my opinion, Kishimoto discloses an internal voltage generating circuit, as I discussed in 1[pre] above. *See* § IX.D.(i).

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.*

100. In my opinion, Kishimoto discloses claim limitation 4[a]. As I explained above regarding claim limitation 1[c], Kishimoto discloses "a frequency divider 51 for dividing the frequency of ***a clock signal CLK0 for operating a charge pump CP10***." Kishimoto at 15:66-16:1.



G. Claim 6

(i) 6[pre]: *An internal voltage generating circuit comprising:*

101. In my opinion, Kishimoto discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § IX.D.(i).

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,*

102. In my opinion, Kishimoto discloses claim limitations 6[a]-[b], as discussed in 3[a]-[b]. *See* § IX.D.(ii)-(iii).

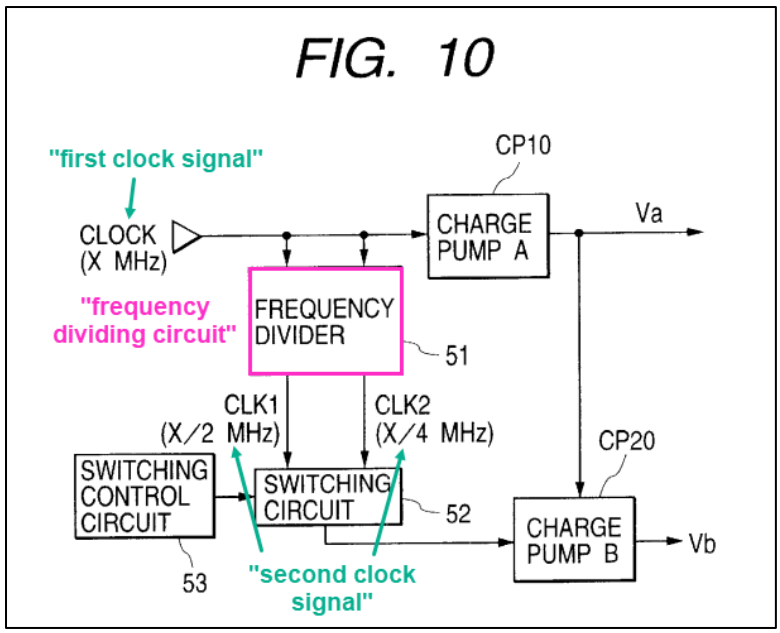
(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and*

103. In my opinion, Kishimoto discloses claim limitation 6[c]. As set forth above in claim limitation 1[d], Kishimoto discloses "a switching circuit 52 or a selector for switching the clocks CLK1 and CLK2 … ***so that the frequency of the clock signal PCLK to operate the charge pump CP20*** for carrying out the second stage of voltage boosting ***varies in accordance with a control signal*** from a switching control circuit 53." Kishimoto at 16:2-8. Therefore, in my opinion, the frequency of the clock signal (PCLK) to be supplied to the second charge pump circuit (CP20) is changed in accordance with a control signal. Kishimoto therefore discloses claim limitation 6[c].

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.*

104. In my opinion, Kishimoto discloses claim limitation 6[d]. As I explained above in claim limitation 1[c], Kishimoto discloses "clocks CLK1 and

CLK2"—which are supplied to the second charge pump CP20—have "undergone frequency division by the frequency divider 51," as shown in annotations below. See Kishimoto at 16:3-4.) Accordingly, it is my opinion that Kishimoto discloses claim limitation 6[d].



H. Claim 7

(i) 7[pre]: *An internal voltage generating circuit comprising:*

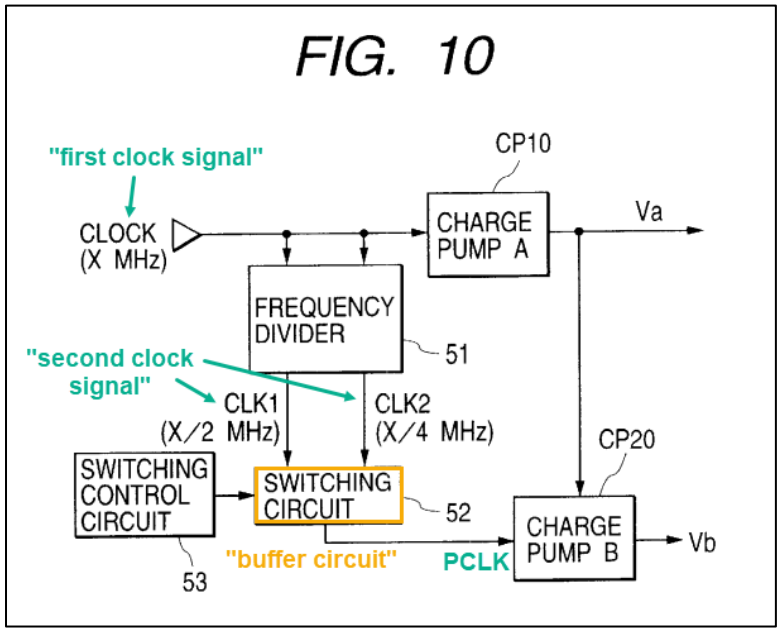
105. In my opinion, Kishimoto discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § IX.D.(i).

(ii) 7[a]-[b]: ***a first charge pump circuit configured to generate a second voltage from a first voltage; and*** **7[b]:** ***a second charge pump circuit configured to generate a third voltage from the second voltage,***

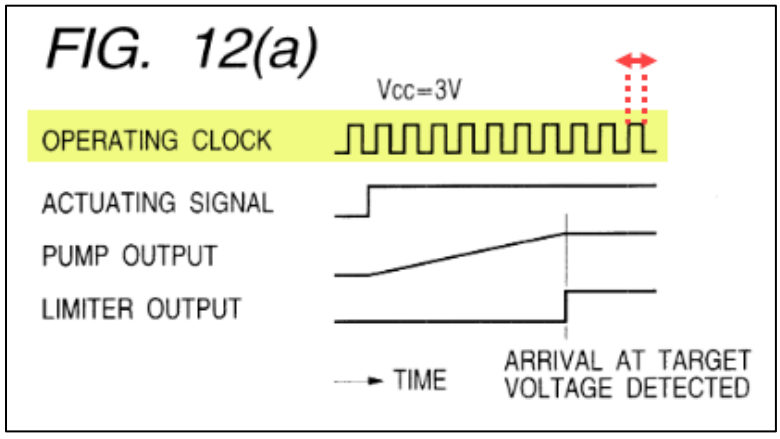
106. In my opinion, Kishimoto discloses claim limitation 7[a]-[b], as discussed in 3[a]-[b]. *See* § IX.E.(ii).

(iii) 7[c]: ***wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.***

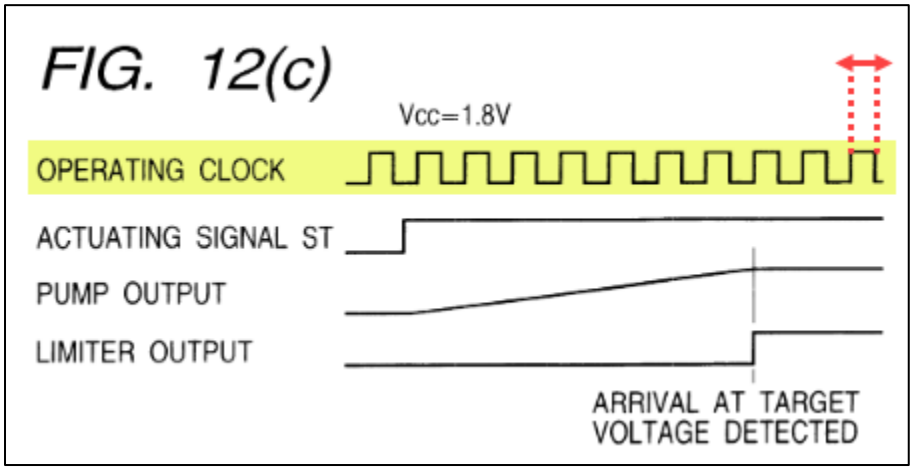
107. In my opinion, Kishimoto discloses claim limitation 7[c]. As I explained above in claim limitation 1[d], Kishimoto discloses "a switching circuit 52 or a selector for switching the clocks CLK1 and CLK2 … ***so that the frequency of the clock signal PCLK to operate the charge pump CP20*** for carrying out the second stage of voltage boosting ***varies in accordance with a control signal*** from a switching control circuit 53." Kishimoto at 16:2-8.



108. In addition, when the clock signal PCLK that drives charge pump CP20 changes from CLK1 to CLK2, it is my opinion that Figure 12 of Kishimoto discloses the length of a period in which the clock signal is in a high state is changed. Specifically, when the higher frequency CLK1 signal is applied to drive CP20, the length of a period in which the clock is in a high state is shorter (illustrated in red below):



109. However, when the lower frequency CLK2 signal is applied to drive CP20, the length of a period in which the clock is in a high state is longer (illustrated in red below):



110. Accordingly, it is my opinion that Kishimoto discloses claim limitation 7[c].

I. Claim 8

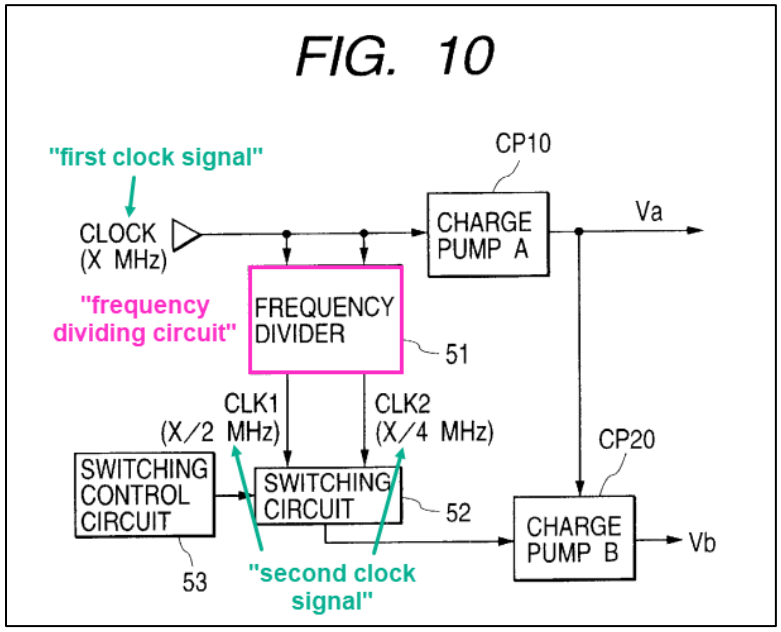
(i) 8[pre]: *The internal voltage generating circuit of claim 7,*

111. In my opinion, Kishimoto discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § IX.D.(i).

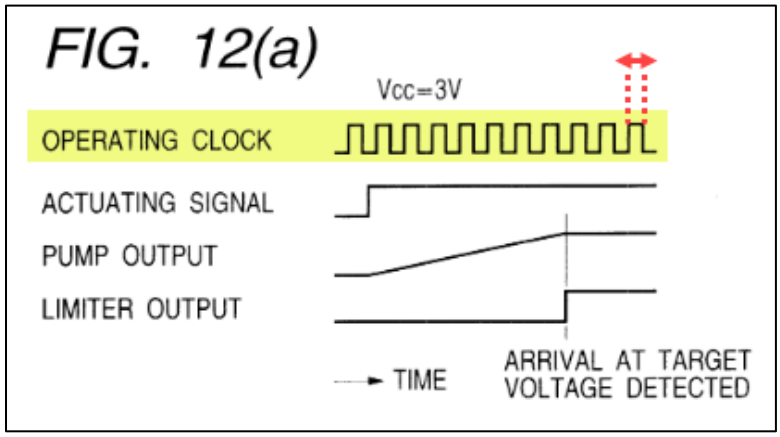
(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.*

112. In my opinion, Kishimoto discloses claim limitation 8[a]. As I explained above in 1[c], Kishimoto discloses "clocks CLK1 and CLK2"—which are

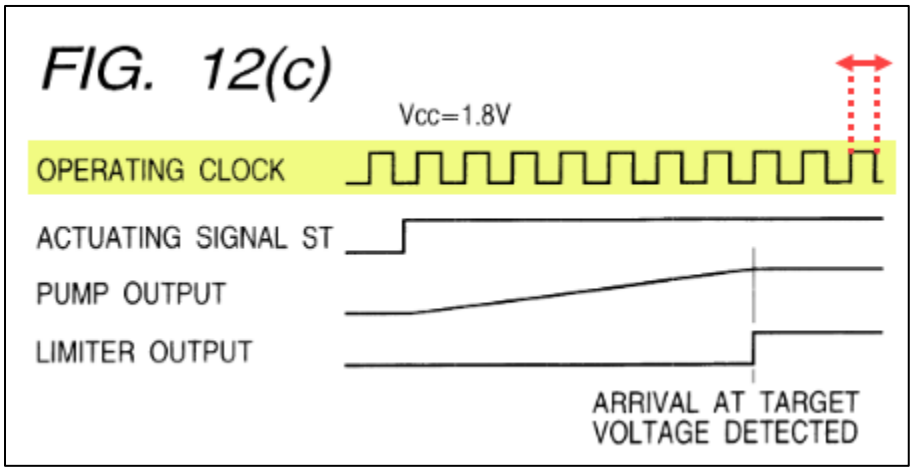
supplied to the second charge pump CP20—have "undergone frequency division by the frequency divider 51" upon the original clock, CLK0, as shown in annotations below. *See* Kishimoto at 16:3-4.



113. In other words, the length of a period in which the clock signal to be supplied to the second charge pump circuit (*e.g.*, CP20) is in a high state, as I have shown in annotated Figs. 12(a) and 12(c) below, is changed depending on whether CLK1 or CLK2 is selected. A POSITA would have understood that if CLK1 is selected, the clock frequency is one half of the original clock frequency CLK0 and the length of a period in a high state is twice as long compared to CLK0.



114. On the other hand, if CLK2 is selected, the clock frequency is changed to one quarter of the original clock frequency CLK0 and the length of a period in a high state is longer than CLK0, namely, four times as long. Accordingly, it is my opinion that Kishimoto discloses claim limitation 8[a].



X. GROUND 2: ABE

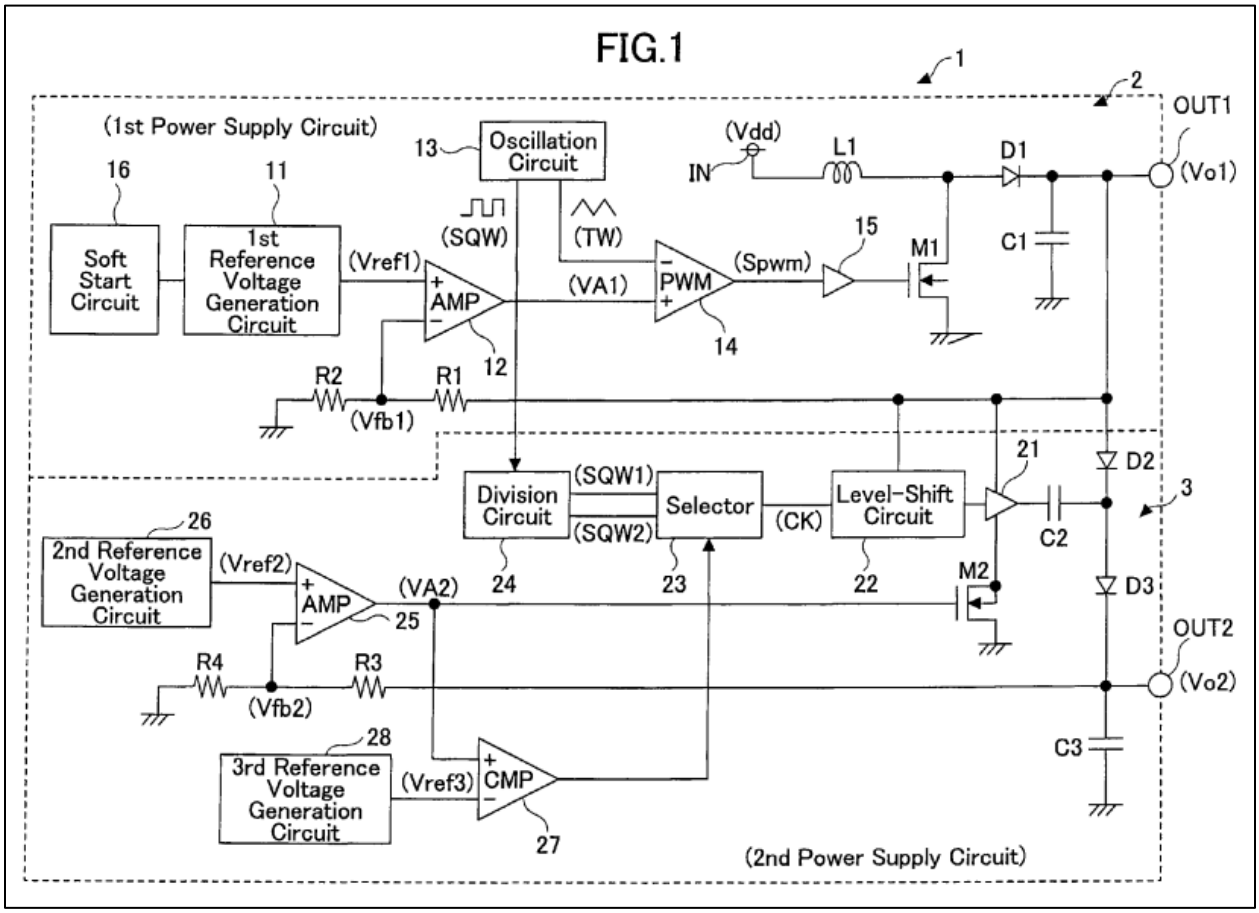
A. Overview of Abe

115. As I explained in § IX.B. above, Abe is prior art under at least pre-AIA 35 U.S.C. § 102(e). In my opinion, Abe discloses or renders obvious all challenged claim limitations of the '231 Patent.

B. Claim 1

(i) 1[pre]: *An internal voltage generating circuit comprising:*

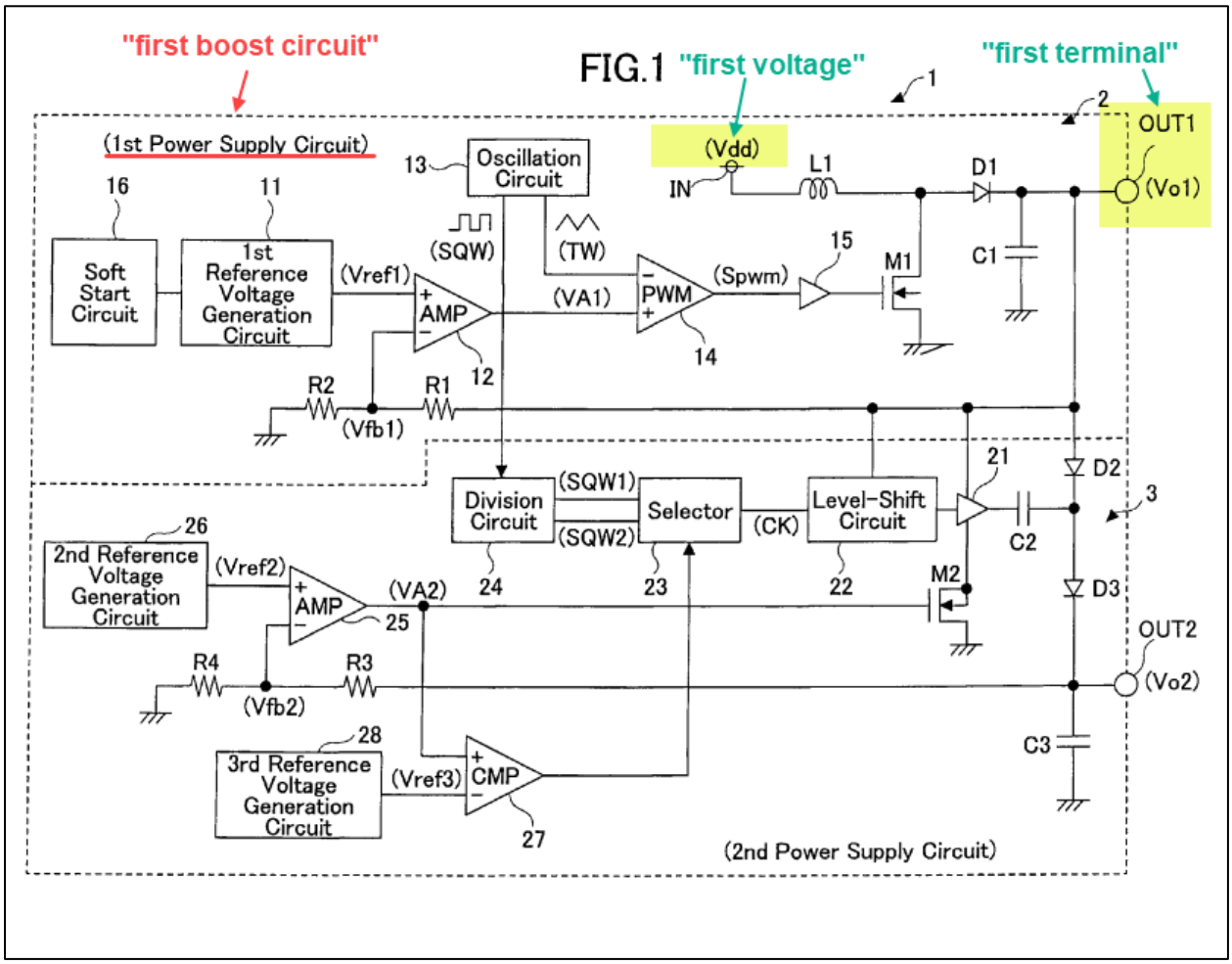
116. If the preamble is deemed limiting, it is my opinion that Abe discloses this preamble. For example, Abe discloses a "multi-output power supply device 1" in Fig. 1, which "boosts an input voltage Vdd, which is input from an input terminal IN, to plural voltages having specified different values, and outputs the voltages from corresponding output terminals OUT1 and OUT2, respectively." Abe at 5:23-27. In my opinion, because Abe's multi-output power supply device 1 generates internal voltages (Vo1 and Vo2) based on an input voltage, it is an "internal voltage generating circuit."



(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;*

117. In my opinion, Abe also meets claim limitation 1[a]. "The multi-output power supply device 1" in Abe's Fig. 1 "includes a first power supply circuit 2, which serves as a step-up switching regulator for generating and outputting the output voltage Vo1." Abe at 5:30-33. In my opinion, Abe's **first power supply circuit 2** is a "first boost circuit" because it is a "step-up" regulator, which generates boosted output voltage Vo1 from the input voltage Vdd. Abe at 5:23-27. It is also

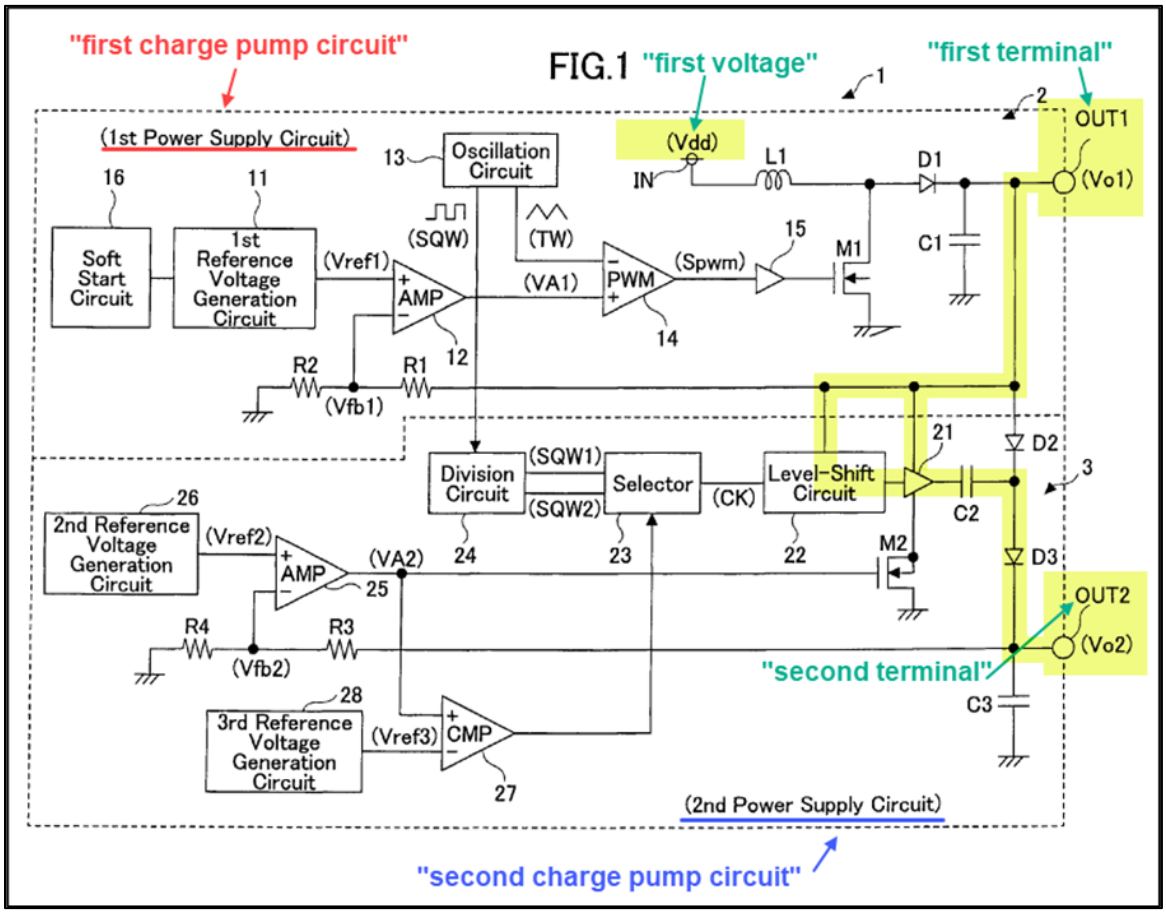
my opinion that Abe's first power supply circuit 2 is provided between a "first voltage" (Vdd) and a "first terminal" (OUT1).



(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;*

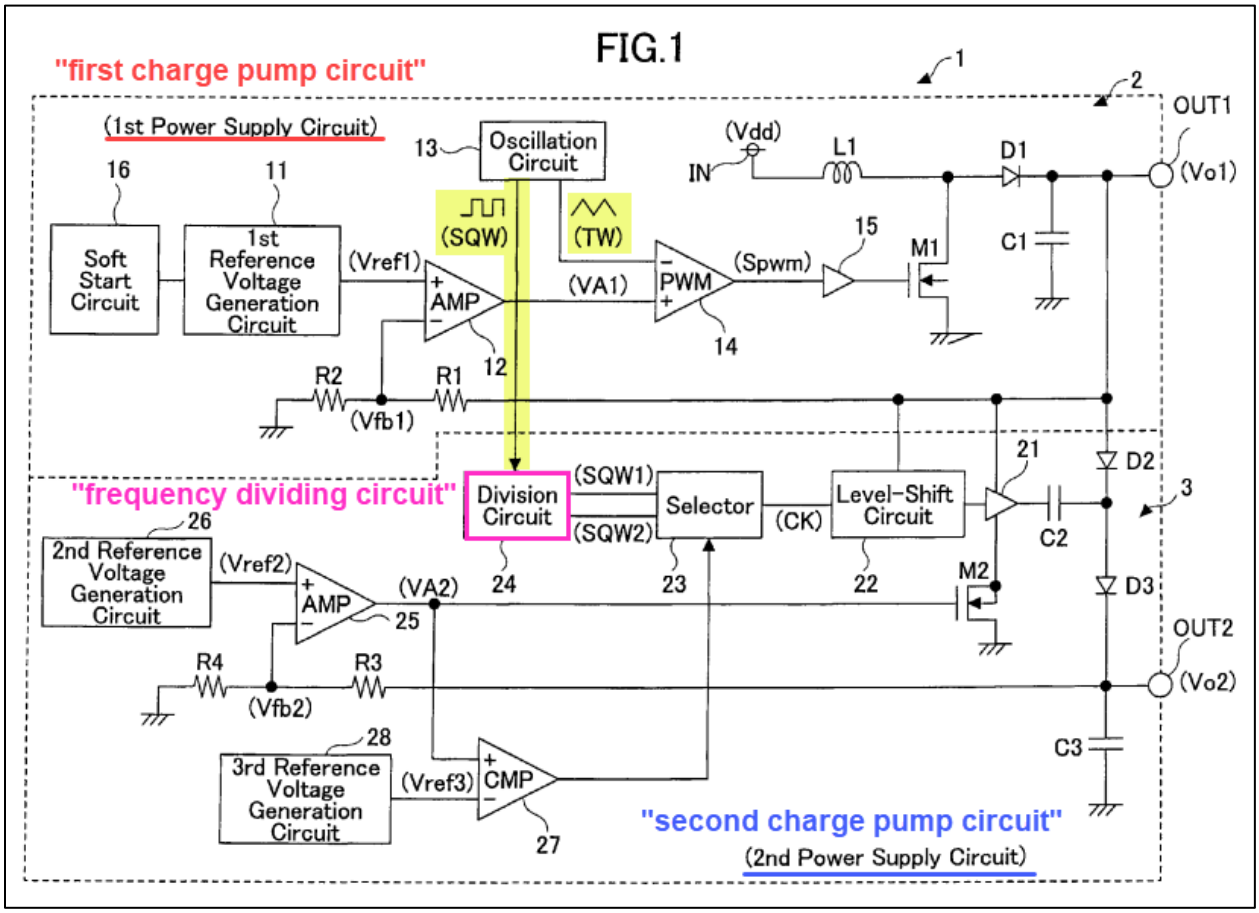
118. In my opinion, Abe meets claim limitation 1[b]. "The multi-output power supply device 1" in Abe's Fig. 1 also includes "a second power supply circuit 3, which serves as a step-up charge pump circuit for generating and outputting the output voltage Vo2 with the output voltage Vo1 of the first power supply circuit 2

as an input voltage." Abe at 5:30-36. In my opinion, Abe's **second power supply circuit 3** is a "second boost circuit" because it is a "step-up charge pump" that generates output voltage Vo2 from input voltage Vo1. It is also my opinion that Abe's second power supply circuit 3 is provided between the first terminal (OUT1) and a second terminal (OUT2).



(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and*

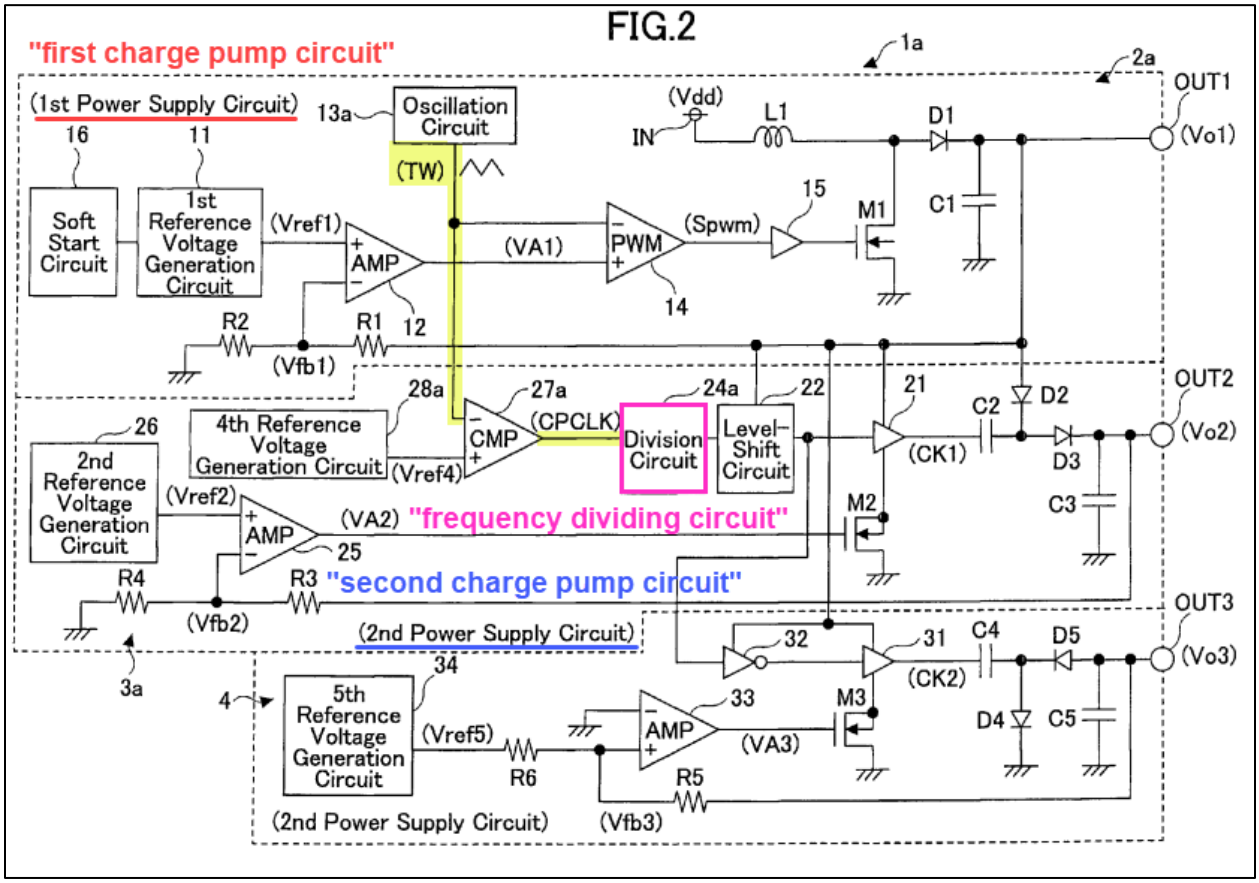
119. It is my opinion that Abe renders obvious claim limitation 1[c]. Specifically, Abe's triangular signal TW is supplied to the first charge pump circuit (*i.e.*, the claimed "first boost circuit"). Further, "[t]he rectangular signal SQW from the oscillation circuit 13 is input to the **division circuit 24**" which "divides the frequency of the rectangular signal SQW by two, thus obtaining a rectangular signal SQW1, and divides the frequency of the rectangular signal SQW by four, thus obtaining a rectangular signal SQW2." Abe at 7:10-15.



120. In my opinion, because Abe's division circuit 24 divides the frequency of the input signal and outputs a signal (SQW1 or SQW2) with ***divided*** frequencies, it is a "frequency dividing circuit." It is further my opinion that SQW1 and SQW2, generated by the frequency dividing circuit, are each a "second clock signal."

121. In my opinion, it would have been obvious to a POSITA to modify Abe's Figure 1 such that, instead of rectangular signal SQW, the triangular signal TW (a "first clock signal") is supplied as an input to the division circuit 24. In fact, Abe itself provides the motivation by disclosing an embodiment, as shown in

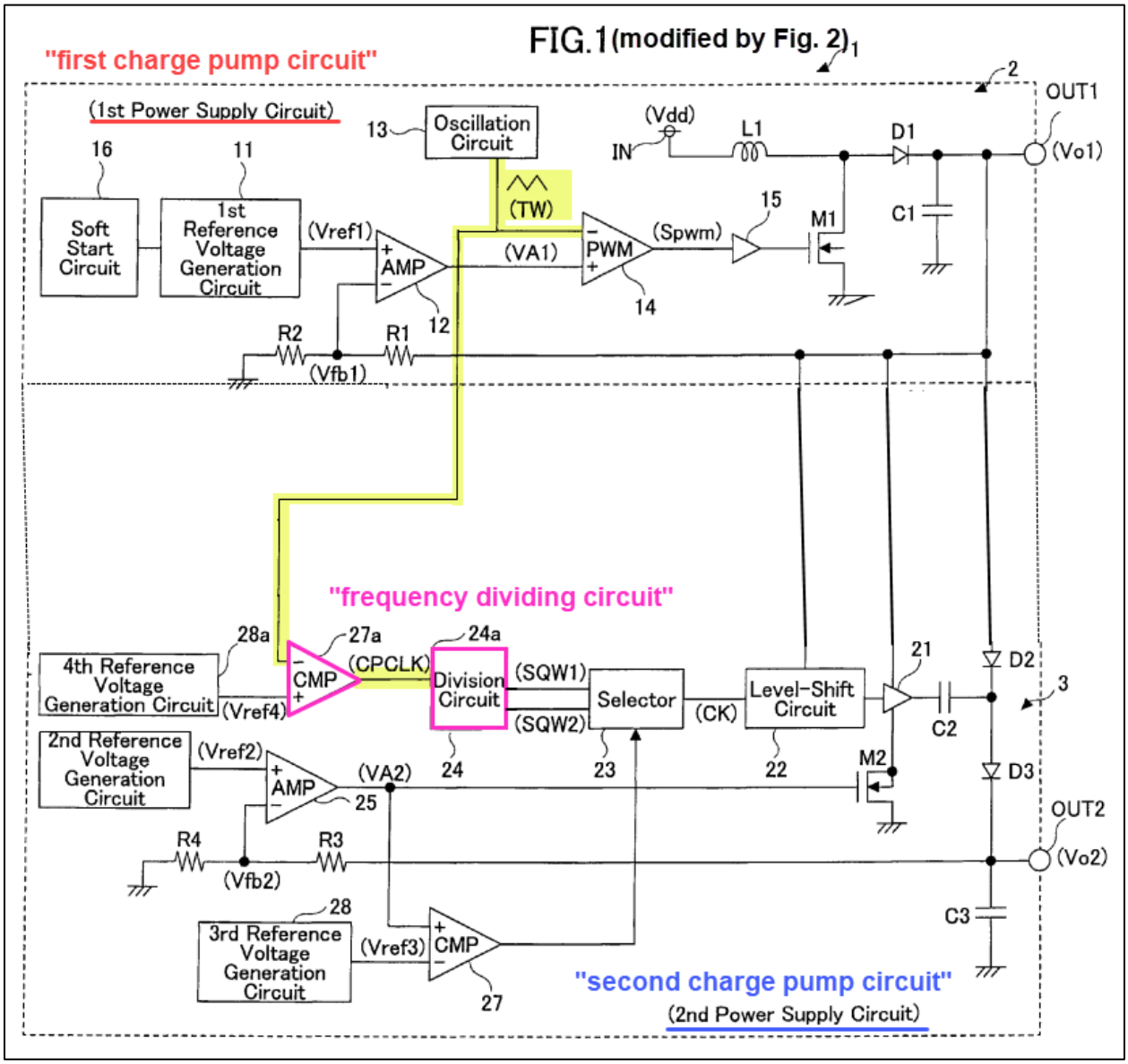
Figure 2 below, where "the oscillation circuit 13a generates and outputs ***only the triangular signal TW***" and "the division circuit 24a divides the frequency of the input signal with only one division ratio." Abe at 9:39-41.



122. In my opinion, a POSITA would have been motivated to improve the flexibility of clock frequencies in Abe's Figure 1 embodiment by using the "triangular signal TW"-only design as disclosed in Abe's Figure 2, thus obviating the need for a separate rectangular signal SQW. In fact, because the triangular signal TW and the rectangular signal SQW in Abe's Fig. 1 have the ***same frequency*** and are generated ***by the same oscillation circuit 13*** (Abe at 7:25-27), it is my opinion

that a POSITA would have found it obvious to generate "***only the triangular signal TW***," as taught in Abe's Figure 2, to further simplify the circuitry.

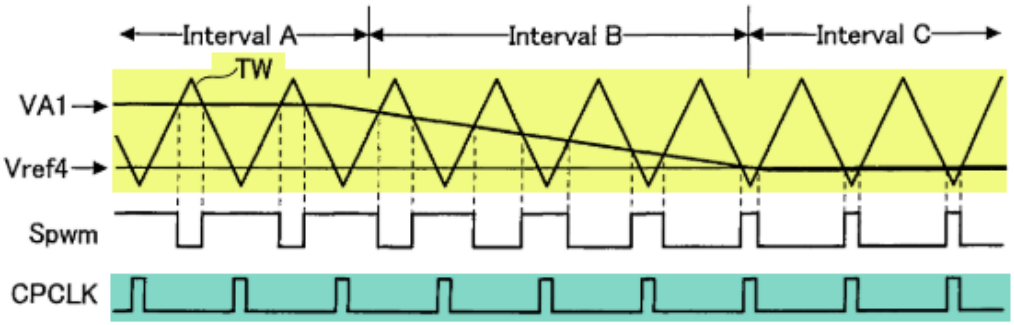
123. It is further my opinion that a POSITA would have had a reasonable expectation of success in modifying Abe's Figure 1 embodiment to use the triangular signal TW as the ***only*** input to division circuit 24. For example, one possible modification is to replace the ***division circuit 24*** of Abe's Figure 1 with both ***comparator 27a*** and ***division circuit 24a*** from Abe's Figure 2, as shown below.



124. In this modified embodiment, consistent with the disclosure of Abe's Figure 2, "the triangular signal TW is input to an inverted input terminal of the comparator 27a" and "[t]he output signal CPCLK from the comparator 27a is input to the division circuit 24a," which "divides the frequency of the output signal CPCLK by the present division ratio." Abe at 11:59-64. In fact, Figure 3 of Abe

even shows how the output of the comparator 27a, CPCLK (highlighted in green), is a rectangular signal having the same frequency as the input triangular signal TW (highlighted in yellow), and thus the same frequency as the original rectangular signal SQW.

FIG.3



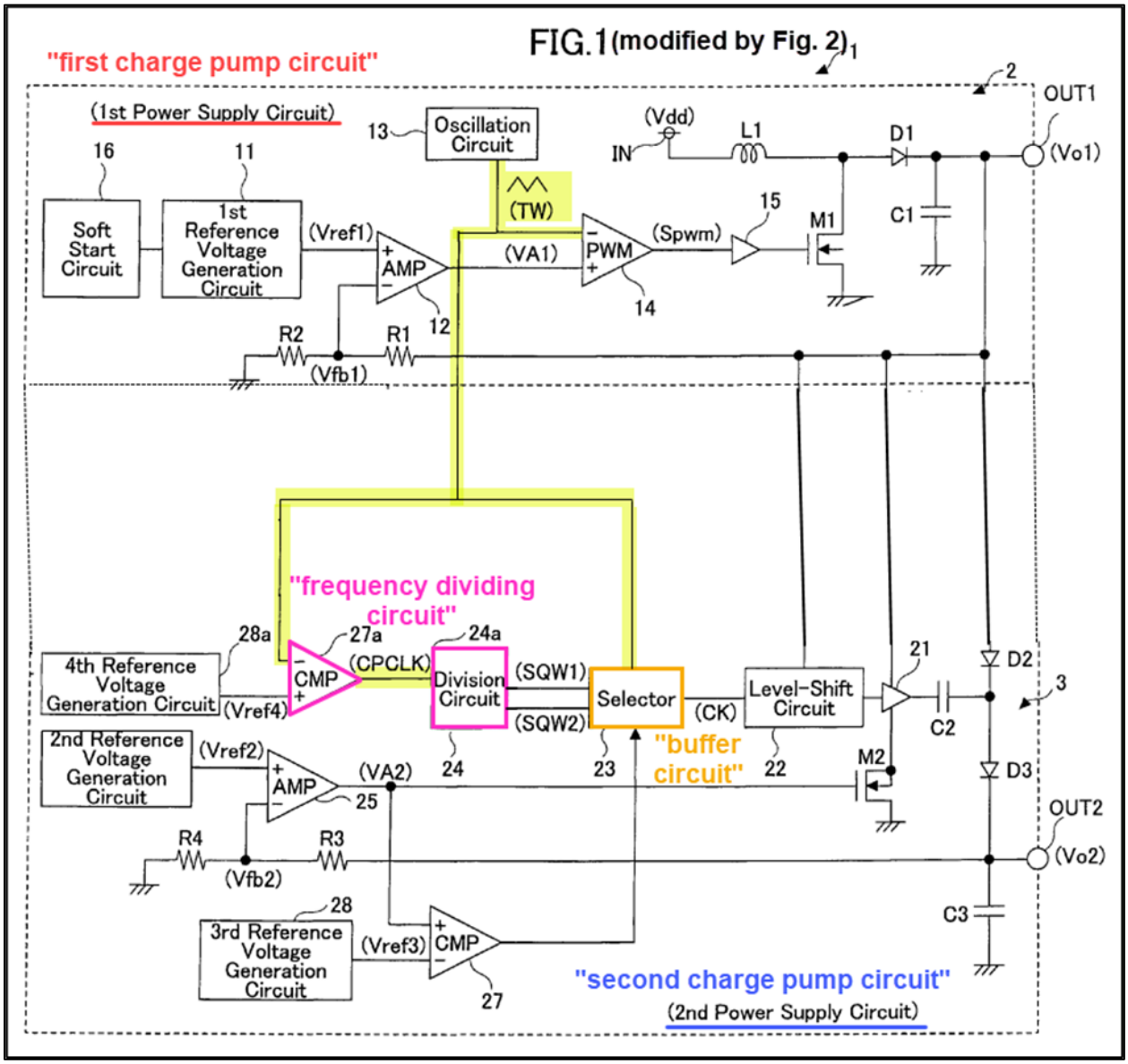
125. Accordingly, it is my opinion that Abe renders obvious a frequency dividing circuit (division circuit 24) configured to divide a first clock signal (TW) to be supplied to the first boost circuit (first power supply circuit 2) to generate a second clock signal (SQW1 or SQW2).

(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.*

126. In my opinion, Abe meets claim limitation 1[d]. Abe's **selector 23** is a "buffer circuit" because it "selects one of the rectangular signal SQW1 and the rectangular signal SQW2 according to the signal from the signal from the

comparator 27, and outputs the selected signal to the level-shift circuit 22 as a clock signal CK." Abe at 7:18-22. Abe's selector 23 is a multiplexer, similar to the "buffer circuit" of the '231 Patent. *See* '231 Patent at Fig. 3.

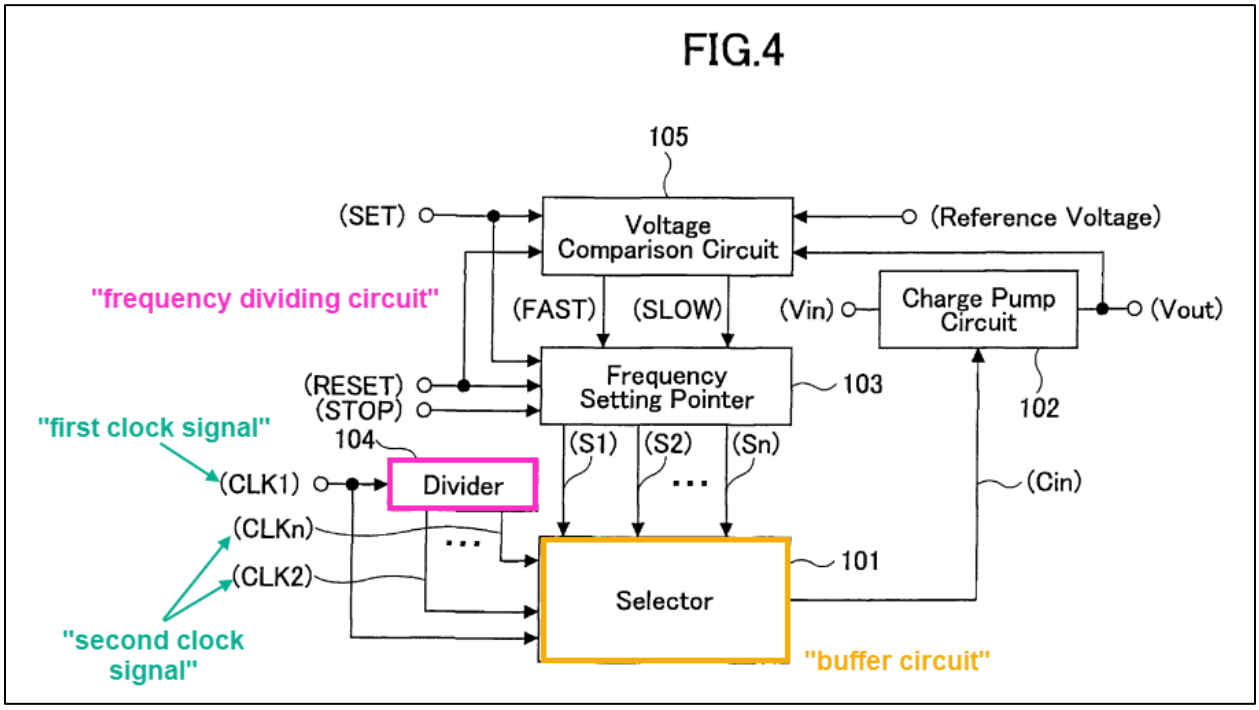
127. In my opinion, Abe's selector 23 is "configured to select and supply the first clock signal" (TW by itself) or "the second clock signal" (SQW1 or SQW2) to the second boost circuit. Abe discloses that selector 23 is not limited to receiving either SQW1 or SQW2 as input. Abe at 8:46-54. In my opinion, in the proposed modification where the triangular signal TW is the ***only input*** into division circuit 24, TW would also have been one of the signals input to the selector 23.



128. As such, it is my opinion that the buffer circuit is configured to select and supply the first clock signal" (TW by itself) or "the second clock signal" (SQW1 or SQW2) to the "second boost circuit."

129. As discussed above in connection with Ground 1, Abe discloses such a selector in Figure 4, where the original clock signal CLK1 and the divided clock

signals CLK2 to CLKn are all inputs to the selector circuit. In my opinion, the original clock signal CLK1 is TW alone, and the divided clock signals are the divided clocks SQW1 and SQW2.



130. Accordingly, even if Abe is found to not anticipate claim limitation 1[d], it is my opinion that a POSITA would have found 1[d] obvious in view of Abe.

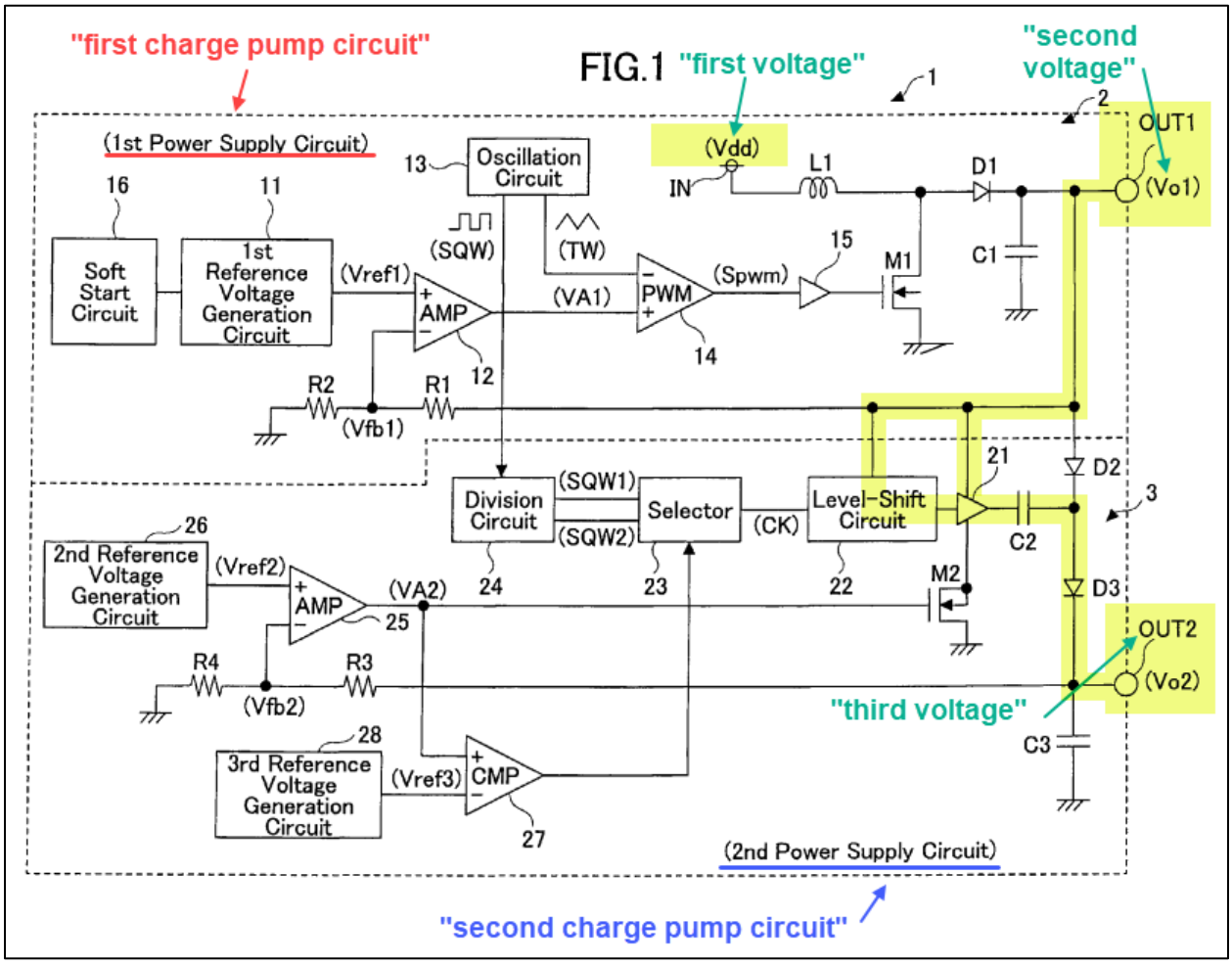
C. Claim 3

(i) 3[pre]: *An internal voltage generating circuit comprising:*

131. Abe discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § X.B.(i), *supra*.

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;*

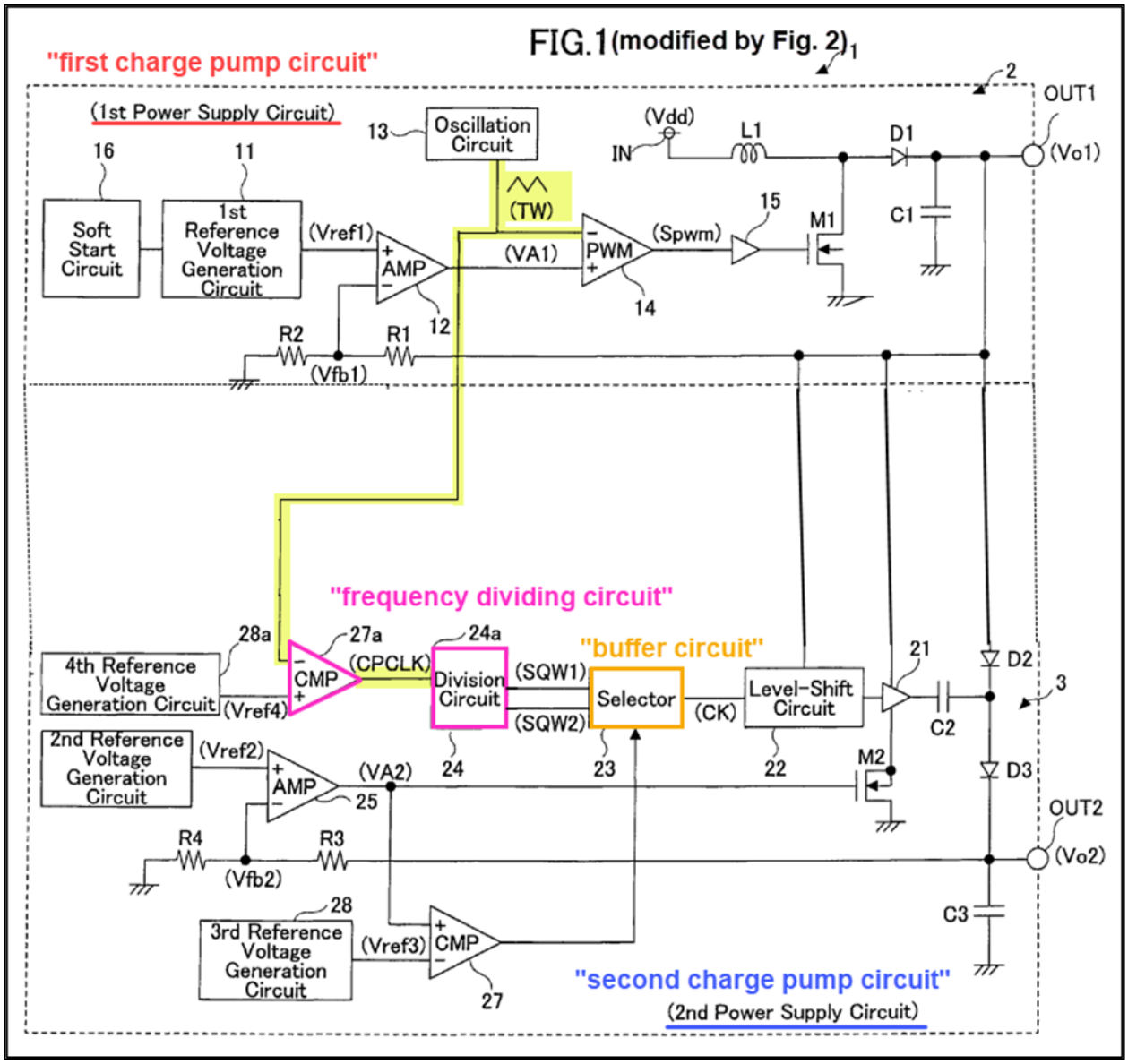
132. In my opinion, Abe meets claim limitations 3[a]-3[b]. As discussed above, Abe discloses first power supply circuit 2 and second power supply circuit 3. In Abe, the first charge pump circuit (first power supply circuit 2) is configured to generate a second voltage (Vo1) from a first voltage (Vdd). Abe at 5:23-27, Fig. 1.



133. Similarly, in my opinion, the second charge pump circuit in Abe (second power supply circuit 3) is configured to generate a third voltage (Vo2) from the second voltage (Vo1). See Abe at 5:30-36.

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and*

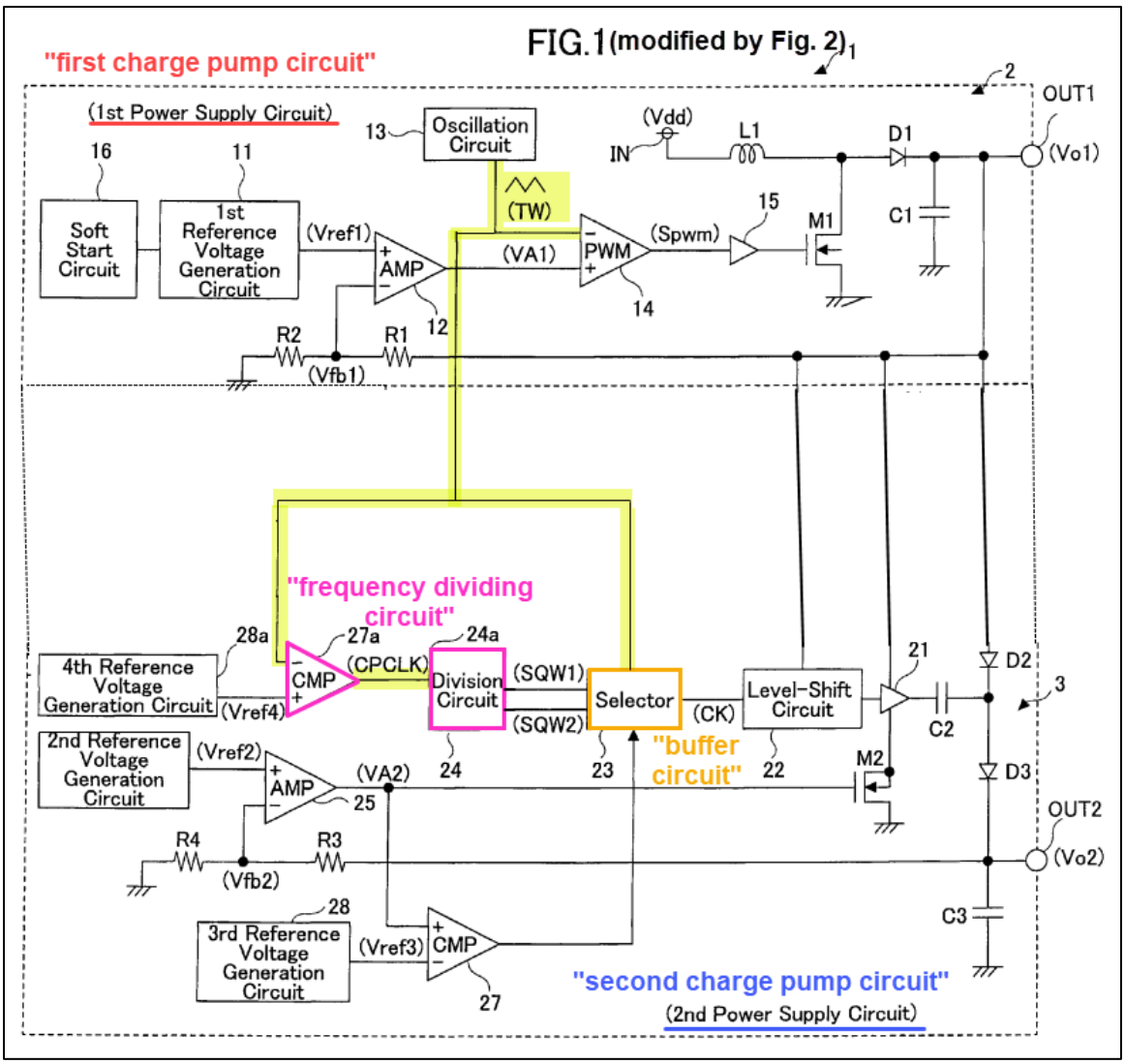
134. As I explained above in § X.B.(iv), it is my opinion that Abe renders claim limitation 3[c] obvious because Abe discloses **division circuit 24** as "a frequency dividing circuit." As further discussed in that section, it is my opinion that it would have been obvious to modify Abe such that division circuit 24a is configured to divide a first clock signal (triangular signal TW) to generate a second clock signal (divided clock signal, SQW1 or SQW2). See Abe at 7:10-15.



(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.*

135. It is my opinion that Abe renders claim limitations 3[d]-[e] obvious. As set forth above regarding limitation 1[d], it would have been obvious to modify Abe's system such that the division circuit 24 receives ***only*** TW as an input signal.

In my opinion, in that modification, **selector 23** (the "buffer circuit") is configured to select either TW ("the first clock signal") or one of SQW1 and SQW2 ("the second clock signal") and generate clock signal CK ("a third clock signal.") See Abe at 7:18-22.



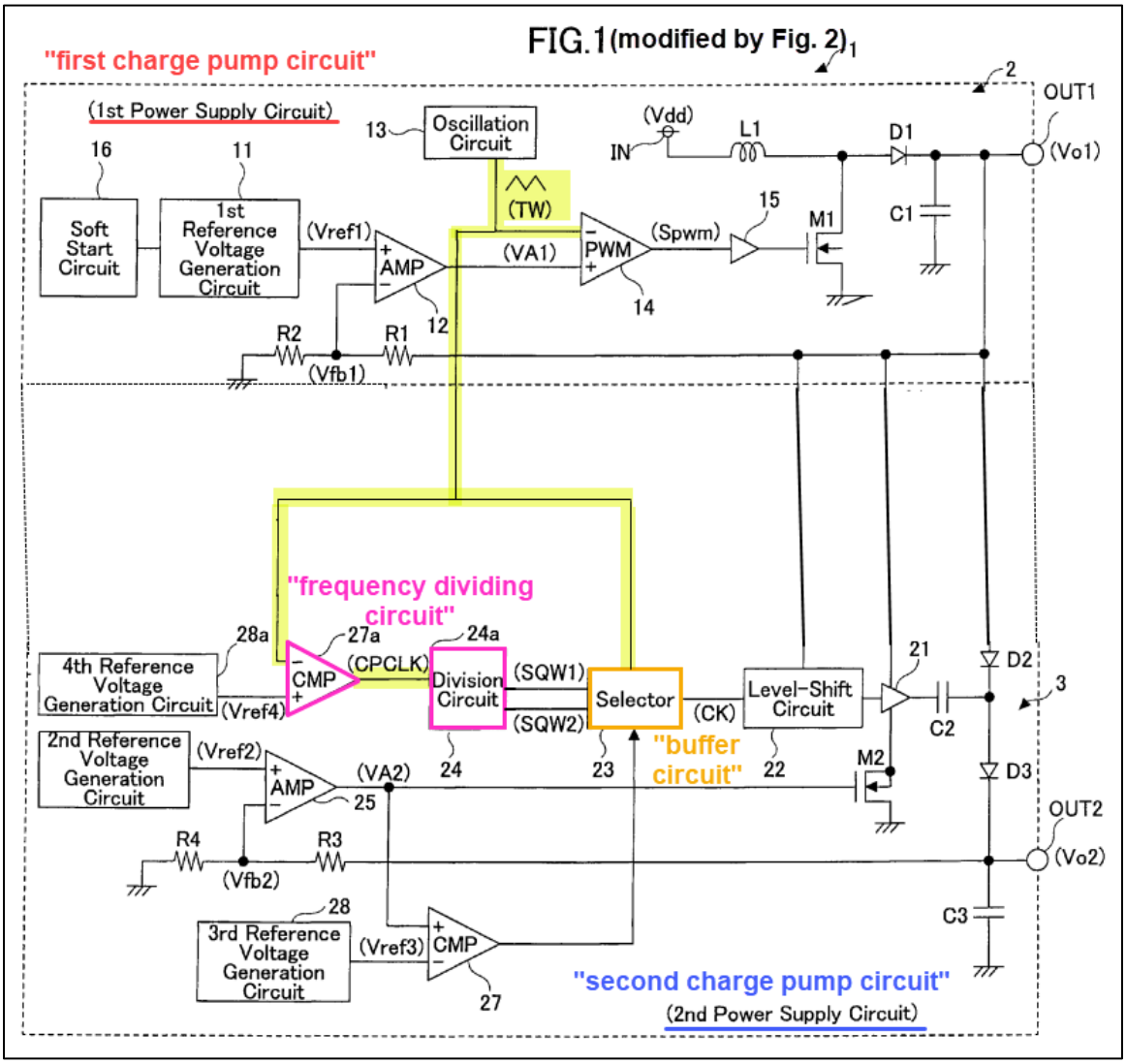
D. Claim 4

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein*

136. In my opinion, Abe meets 4[pre] as I explained in connection with 1[pre]. *See* § X.B.(i), *supra*.

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.*

137. As I explained in connection with claim limitation 1[c] in § X.B.(iv), Abe's triangular signal TW alone is the claimed "first clock signal" in the modified circuit shown below, because TW can generate CPCLK, which generates the two divided clock signals SQW1 and SQW2.

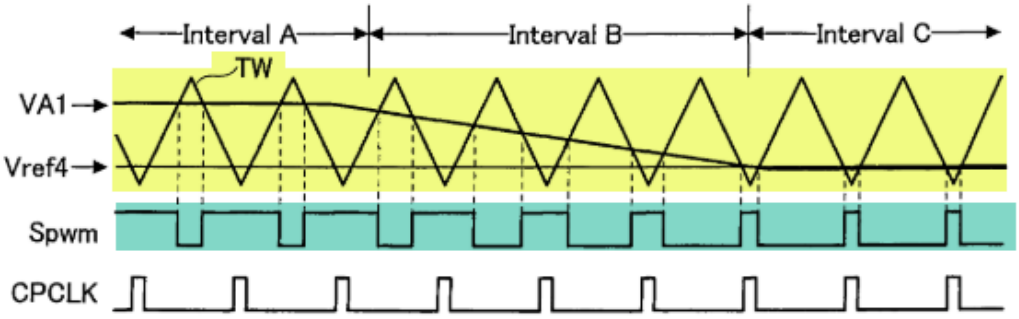


138. Therefore, it is my opinion that Abe renders obvious a clock signal (TW) having substantially the same frequency as that of the first clock signal (TW) is supplied to the first charge pump circuit ("first power supply circuit 2").

139. Alternatively, "the triangular signal TW is input to an inverted input terminal" of PWM comparator 14, which "outputs a pulse signal Spwm." Abe at 6:33-40. "The pulse signal Spwm is input to the gate of the switching transistor M1

through the buffer 15." Abe at 6:33-40. As shown in Fig. 3, the frequency of Spwm has substantially the same frequency as that of the triangular signal TW.

FIG.3



140. Therefore, in the modified embodiment where the triangular signal TW, in addition to the square signal SQW, is input into the division circuit 24, as I discussed for claim limitation 1[c] in § X.B.(iv) above, a clock signal (Spwm) having substantially the same frequency as that of the first clock signal (TW) is supplied to the first charge pump circuit (first power supply circuit 2).

E. Claim 6

(i) 6[pre]: *An internal voltage generating circuit comprising:*

141. In my opinion, Abe discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § X.B.(i) above.

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,*

142. As I explained for claim limitations 3[a]-[b], it is my opinion that Abe meets claim limitations 6[a]-[b]. *See* § X.C.(ii) above.

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and*

143. In my opinion, Abe meets claim limitation 6[c]. Abe discloses that "the output signal from the comparator 27 is input to the selector 23." Abe at 7:7-9. "The selector 23 exclusively selects one of the rectangular signal SQW1 and the rectangular signal SQW2 ***according to the signal from the comparator 27***, and outputs the selected signal to the level-shift circuit 22 as a clock signal CK." Abe at 7:18-22, 7:10-16 (showing SQW1 and SQW2 having different frequencies). Further, as I explained in connection with claim limitations 3[d]-[e], the clock signal CK is supplied to the second power supply circuit 3. *See* Abe at 8:9-11 ("it is desirable that the second power supply circuit 3 ***operate with the clock signal CK*** of a frequency as low as possible").

144. Accordingly, it is my opinion that in Abe, a frequency of a clock signal (CK) to be supplied to the second charge pump (second power supply circuit 3) is changed in accordance with a control signal (output of comparator 27).

(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.*

145. In my opinion, Abe meets claim limitation 6[d]. As I discussed above, the clock signal CK is selected from either SQW1 or SQW2, which are obtained by dividing the frequency of the rectangular signal SQW by two or four, respectively. *See* Abe at 7:10-16. Accordingly, it is my opinion that Abe discloses the frequency of the clock signal (CK) to be supplied to the second charge pump circuit (second power supply circuit 3) is changed to a frequency which is obtained by dividing an original frequency (frequency of SQW).

F. Claim 7

(i) 7[pre]: *An internal voltage generating circuit comprising:*

146. In my opinion, Abe discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § X.B.(i) above.

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,*

147. In my opinion, Kishimoto meets claim limitations 7[a]-[b], as I discussed above in connection with claim limitations 3[a]-[b]. *See* § X.C.(ii) above.

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.*

148. In my opinion, Abe meets claim limitation 7[c]. As I explained in connection with claim limitations 6[c]-[d], the ***frequency*** of the clock signal (CK) to be supplied to the second charge pump circuit (second power supply circuit 3) is changed in accordance with a control signal (output of comparator 27). In my opinion, a POSITA would have understood that Abe's SQW1 and SQW2 are rectangular signals having the same duty cycle (percentage of time the signal is high) but different frequencies. Therefore, selecting one of SQW1 or SQW2 as the clock signal CK would result in different lengths of a period (in other words, different clock period) in which the clock signal is in a high state.

G. Claim 8

(i) 8[pre]: *The internal voltage generating circuit of claim 7,*

149. In my opinion, Abe discloses an internal voltage generating circuit, as I discussed above in 1[pre]. *See* § X.B.(i) above.

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.*

150. In my opinion, Abe meets claim limitation 8[a]. As I explained in connection with claim limitation 7[c], the length of a period in which the clock signal

(CK) to be supplied to the second charge pump circuit (second power supply circuit 3) is in a high state is changed to that of either SQW1 or SQW2, both of which are obtained by dividing an original frequency (SQW). Accordingly, it is my opinion that Abe meets claim limitation 8[a].

XI. GROUND 3: HIIRAGIZAWA

A. Overview of Hiiragizawa

151. Hiiragizawa is prior art under at least pre-AIA 35 U.S.C. §§ 102(a)-(b) because it was patented on Aug. 24, 1999 and thus before July 9, 2008 priority date of the ’231 Patent. I further understand that Hiiragizawa was not considered by the Examiner during prosecution of the ’231 Patent.

152. In my opinion, Hiiragizawa discloses an internal voltage generating circuit in Fig. 6, which includes charge pump circuit 8, “a frequency division circuit 6x” and “a switching circuit.” Hiiragizawa at 6:52-56. An example of charge pump circuit 8 is shown in Fig. 4B, where “charge pump circuit 23 is constituted of an N-channel transistor T23a” and “an N-channel transistor T23b.” Hiiragizawa at 4:8-12, Fig. 4B.

153. In my opinion, Hiiragizawa discloses claims 3, 4, 6, 7, and 8 of the ’231 Patent at least under Patent Owner’s apparent interpretation of the claim limitations. In particular, I understand that in the infringement contentions, Patent Owner

pointed to individual stages within a typical charge pump circuit to contend the claimed first and second charge pump circuits are met. As I explained below, under this interpretation, it is my opinion that Hiiragizawa anticipates the foregoing claims of the '231 Patent.

B. Claim 3

(i) 3[pre]: *An internal voltage generating circuit comprising:*

154. If the preamble is deemed to be limiting, it is my opinion that Hiiragizawa discloses this preamble. For example, Hiiragizawa discloses a "charge pump circuit and the circuit portion related to its clock input" in Fig. 6. Hiiragizawa at 6:49-51. In particular, "charge pump circuit 8 [] supplies a high voltage Vh with a potential higher than the power supply voltage Vdd." Hiiragizawa at 5:31-33. In my opinion, a POSITA would have understood a charge pump circuit is an internal voltage generating circuit.

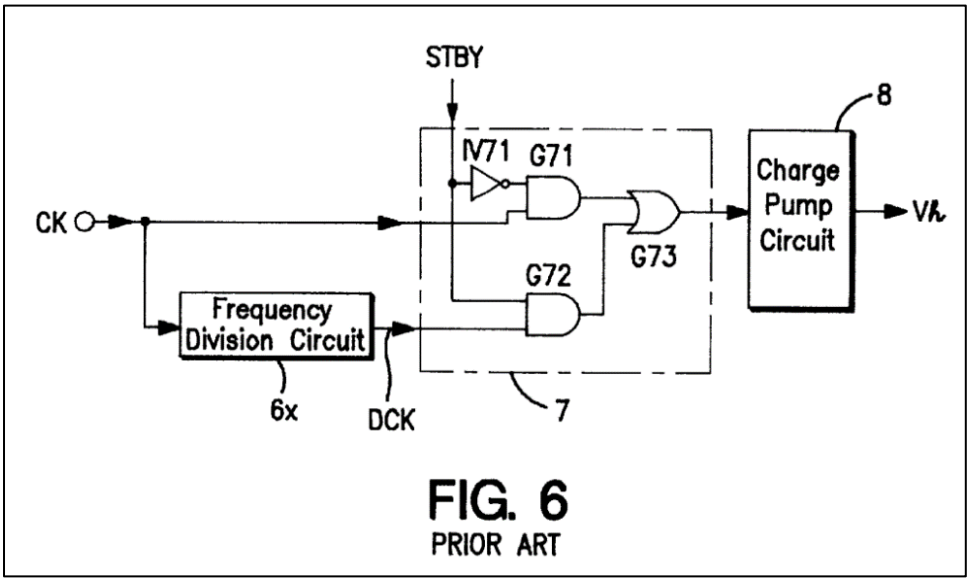


FIG. 6
PRIOR ART

155. In a related example in which a "circuit diagram of a charge pump circuit 23" is shown in Fig. 4B, Hiiragizawa's charge pump generates voltage for an UV-erasable PROM (EPROM) memory device. *See* Hiiragizawa at 4:5-7, 2:37-40.

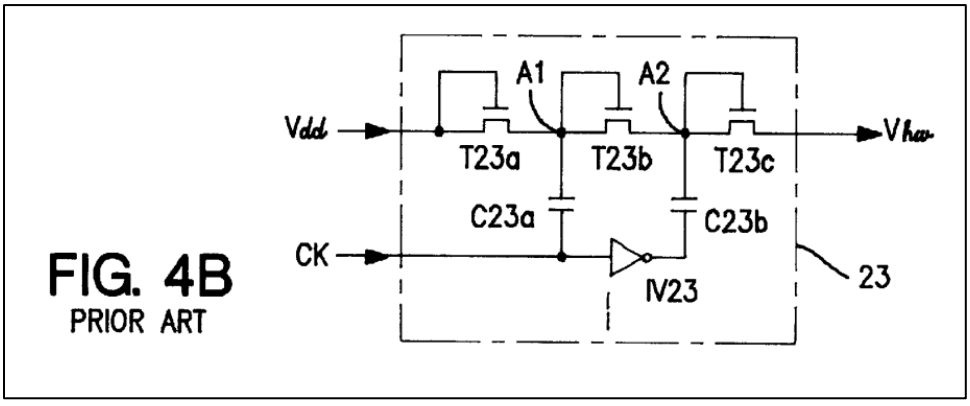


FIG. 4B
PRIOR ART

(ii) 3[a]-[b]: ***a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;***

156. In my opinion, Hiiragizawa meets claim limitations 3[a]-3[b]. Hiiragizawa discloses an "N-channel transistor T23a which receives the power

supply voltage Vdd to the source and the gate," "an **N-channel transistor T23b** whose source and the gate are connected (at node A1) to the drain of the transistor T23a," and "an **N-channel transistor T23c** whose source and the gate are connected (at node A2) to the drain of the transistor T23b and has its drain as an output terminal of the high voltage Vhw." Hiiragizawa at 4:8-15.

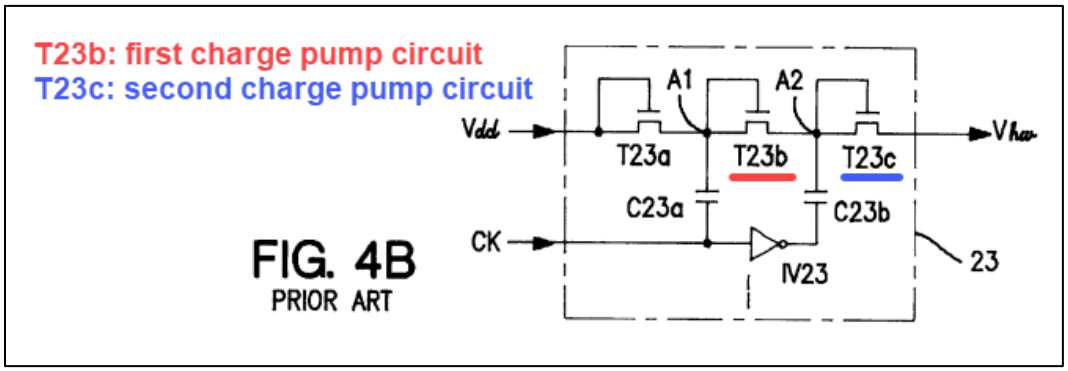


FIG. 4B
PRIOR ART

157. As a POSITA would have understood, transistor T23b (and capacitor C23a) generates a voltage at node A2 (the claimed "second voltage") from the input voltage at node A1 (the claimed "first voltage"); and transistor T23c (and capacitor C23b) generates the high voltage Vhw (the claimed "third voltage") from the input voltage at node A2.

158. Although transistors T23b and T23c (along with respective capacitors C23a and C23b) are two stages of a single charge pump circuit (i.e., charge pump circuit 23) rather than two separate charge pump circuits that are serially connected, mapping them as such is at least consistent with how Patent Owner interpreted claim limitations 3[a]-3[b]. In particular, in the infringement contentions in the related

district court litigation, the Patent Owner mapped the claimed "first charge pump circuit" to one stage of a charge pump ("[redacted]"), as shown below. (EX1006, p. 5.)



159. Likewise, Patent Owner mapped the claimed "second charge pump circuit" to the next stage of the *same* charge pump ("[redacted]"), as shown below. (EX1006, p. 6.)



160. Accordingly, based on at least the Patent Owner's apparent interpretation, it is my opinion that Hiiragizawa discloses the claimed first and second charge pump circuits.

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and*

161. In my opinion, Hiiragizawa discloses claim limitation 3[c]. For example, Hiiragizawa discloses a "charge pump circuit and the circuit portion related to its clock input" in Fig. 6, shown below. Hiiragizawa at 6:49-51.

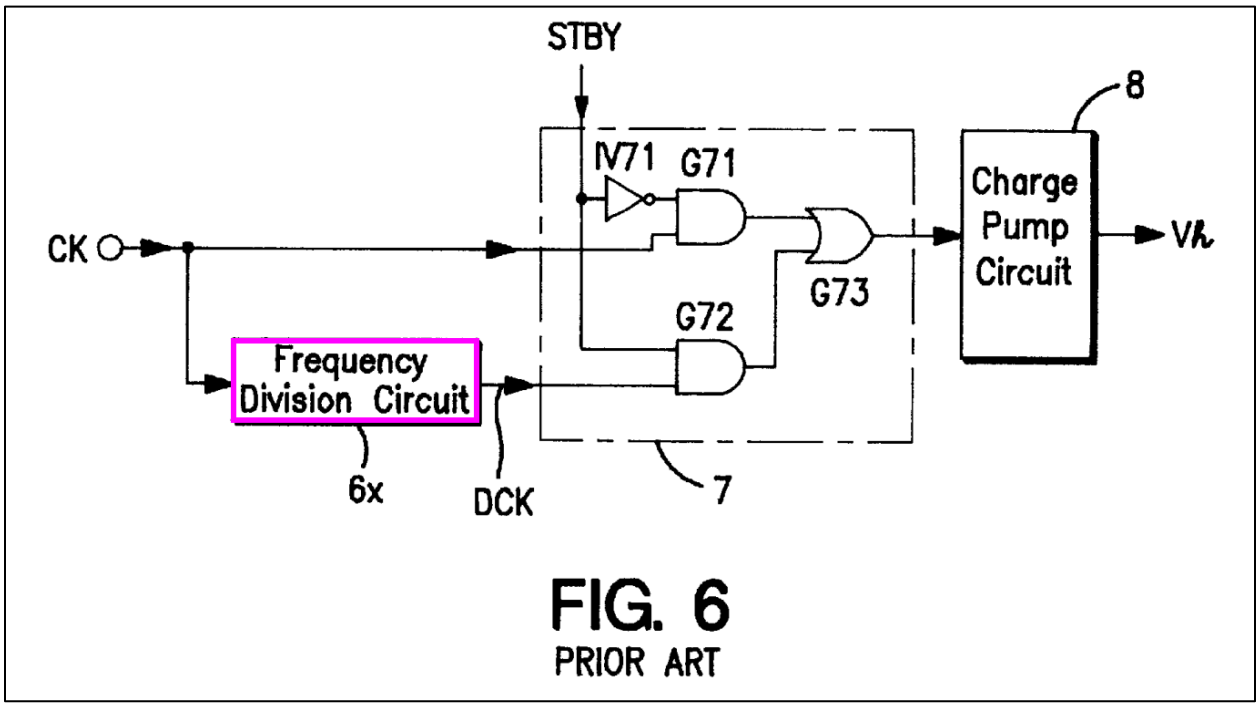


FIG. 6
PRIOR ART

162. In particular, it is my opinion that Hiiragizawa discloses a "**frequency division circuit 6x** which divides the frequency of a clock signal CK from the outside into a specified frequency," DCK. Hiiragizawa at 6:52-58.

163. Accordingly, it is my opinion that Hiiragizawa discloses a frequency division circuit 6x (the claimed "frequency dividing circuit") configured to divide a clock signal CK (the claimed "first clock signal") to generate a divided clock signal DCK (the claimed "second clock signal").

(iv) 3[d]-[e]: *a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.*

164. In my opinion, Hiiragizawa discloses claim limitations 3[d]-[e]. For example, as shown below, Hiiragizawa discloses a "**switching circuit 7**" which "supplies the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x to the charge pump circuit 8 when the standby signal STBY is at the active level, and supplies the clock signal CK from the outside without change to the charge pump circuit 8 when the signal STBY is at the inactive level." Hiiragizawa at 6:56-62.

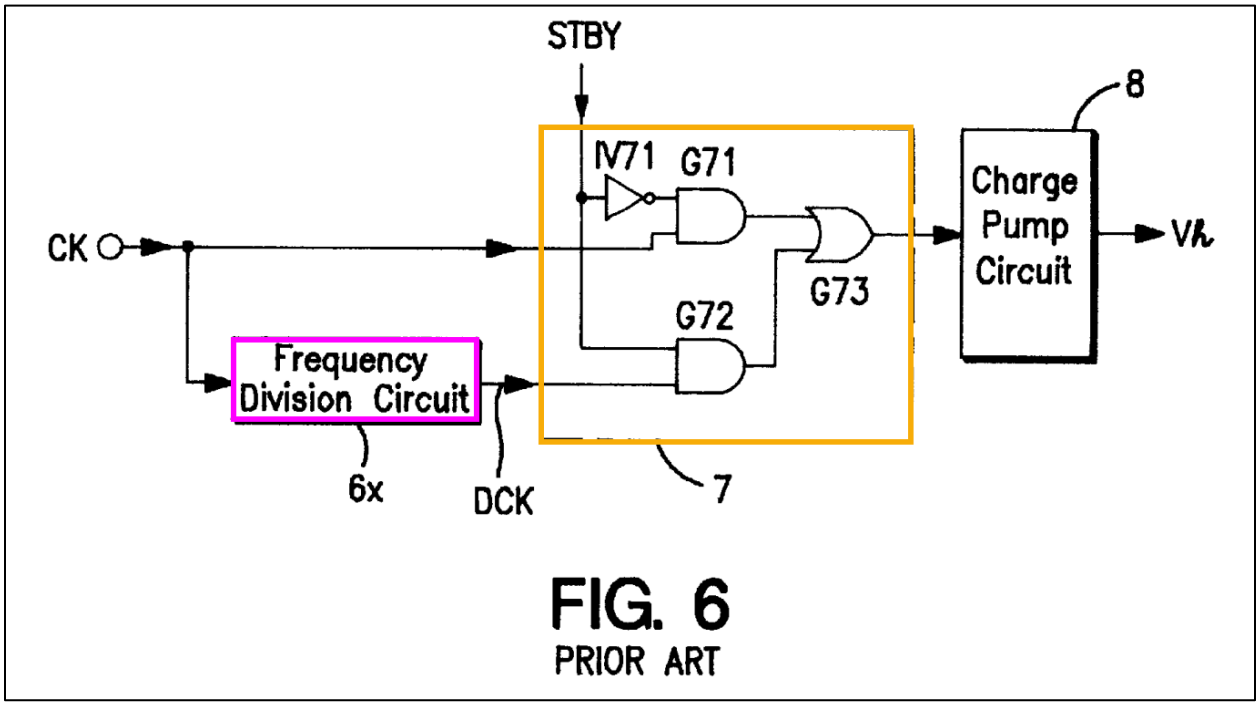


FIG. 6
PRIOR ART

165. Therefore, it is my opinion that the output of Hiiragizawa's switching circuit 7 supplies a clock signal (*i.e.*, either the clock signal CK or the divided clock signal DCK) to the charge pump circuit 8 as the claimed "third clock signal."

166. Further, Hiiragizawa discloses that the "third clock signal" is "supplied to the second charge pump," under Patent Owner's interpretation of a "second charge pump" as described in § XI.B.(ii) above. In particular, in Figure 4B, which shows the internal structure of a charge pump circuit similar to Figure 6's charge pump circuit 8, the input clock signal (the "third clock signal") is supplied to the **N-channel transistor T23c** (the "second charge pump circuit" under the Patent Owner's interpretation).

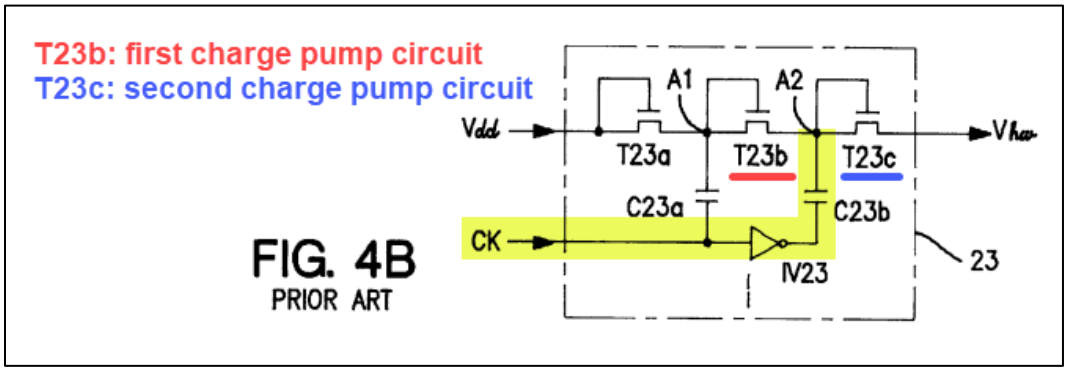


FIG. 4B
PRIOR ART

C. Claim 4

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein*

167. In my opinion, Hiiragizawa discloses an internal voltage generating circuit, as discussed in connection with 3[pre]. *See* § XI.B.(i) above.

(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.*

168. The clock signal supplied to **transistor T23b** (the claimed "first charge pump circuit") is clock signal CK (the claimed "first clock signal"). Hiiragizawa at 4:27-43. Therefore, in my opinion, Hiiragizawa teaches claim limitation 4[a].

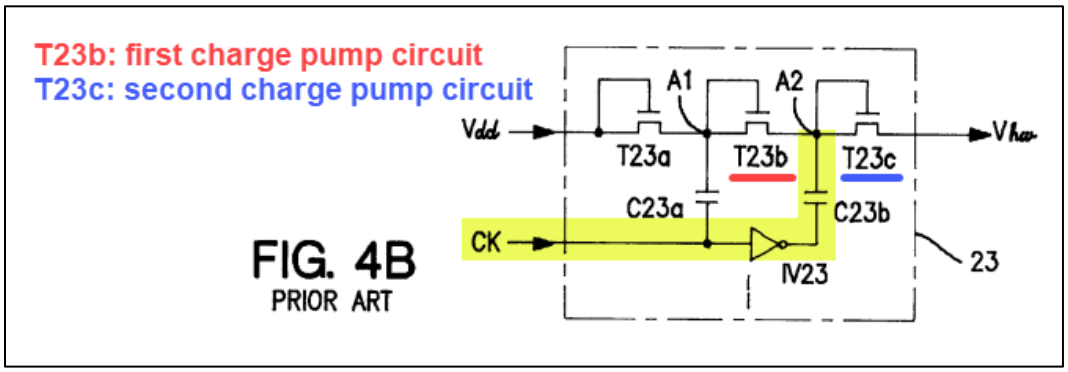


FIG. 4B
PRIOR ART

D. Claim 6

(i) 6[pre]: *An internal voltage generating circuit comprising:*

169. In my opinion, Hiiragizawa discloses an internal voltage generating circuit, as discussed in 3[pre]. *See* § XI.B.(i) above.

(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,*

170. In my opinion, Hiiragizawa discloses claim limitations 6[a]-[b] for the same reasons as I discussed in connection with claim limitations 3[a]-[b]. *See* § XI.B.(ii) above.

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and*

171. In my opinion, Hiiragizawa discloses claim limitation 6[c]. For example, as shown below, Hiiragizawa discloses that "**switching circuit 7**" which "supplies the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x to the charge pump circuit 8 when the standby signal STBY is at the active level, and supplies the clock signal CK from the outside without change to the charge pump circuit 8 when the signal STBY is at the inactive level." Hiiragizawa at 6:56-62.

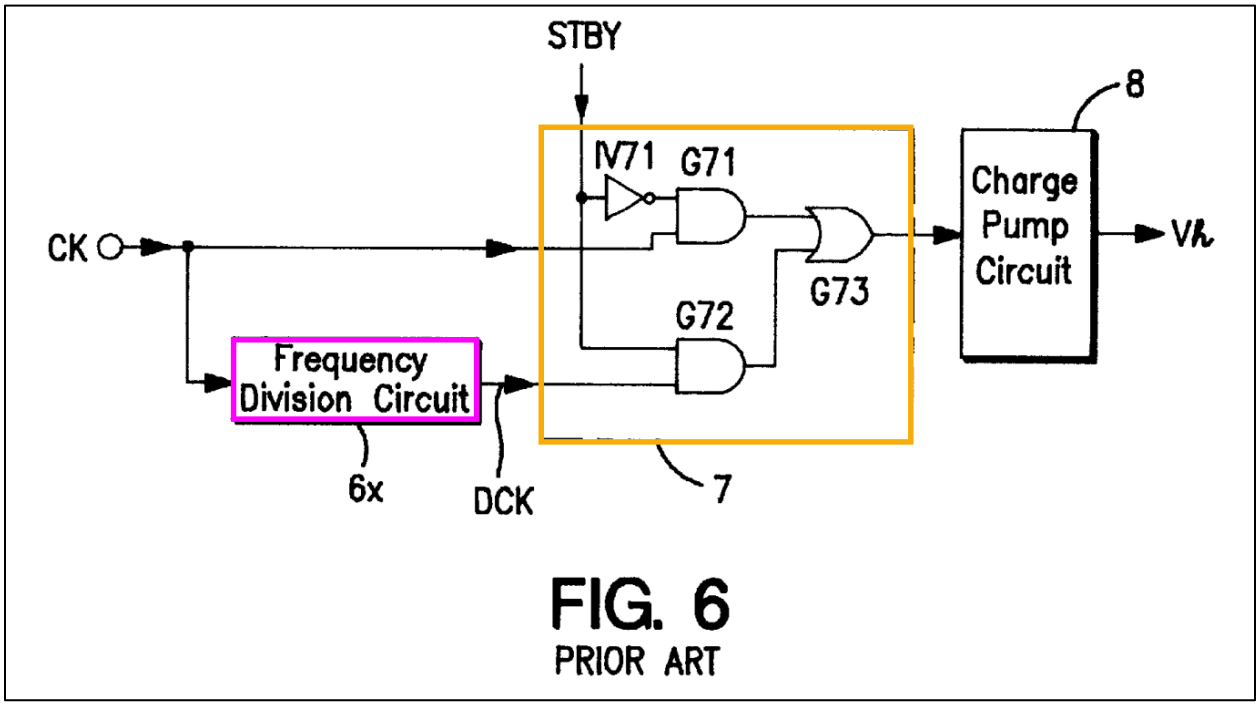
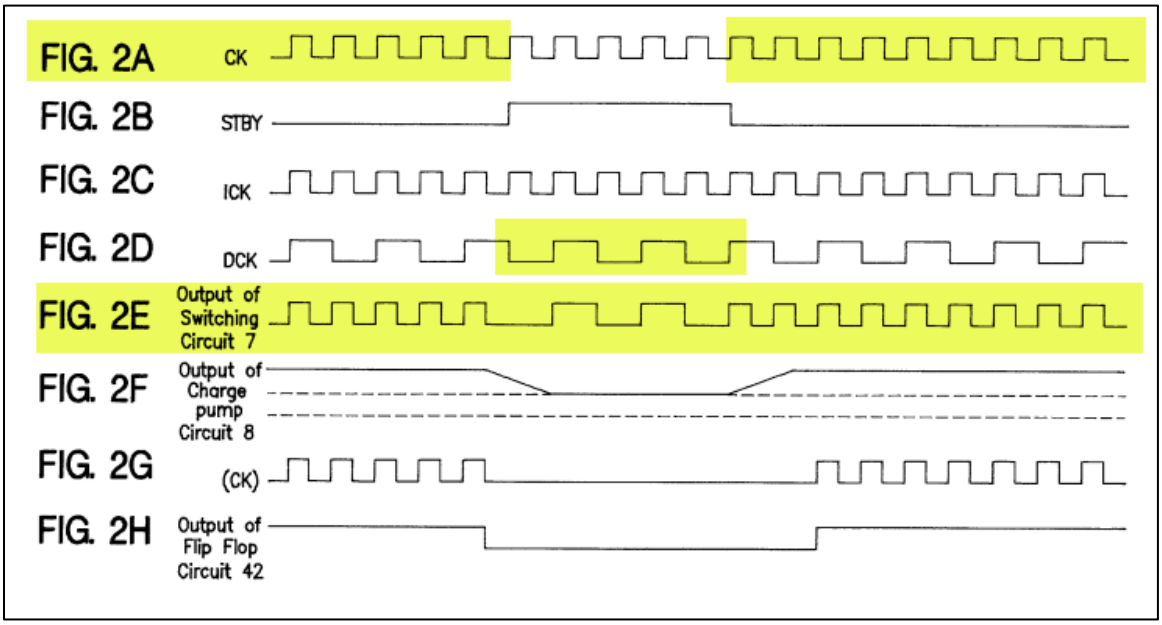


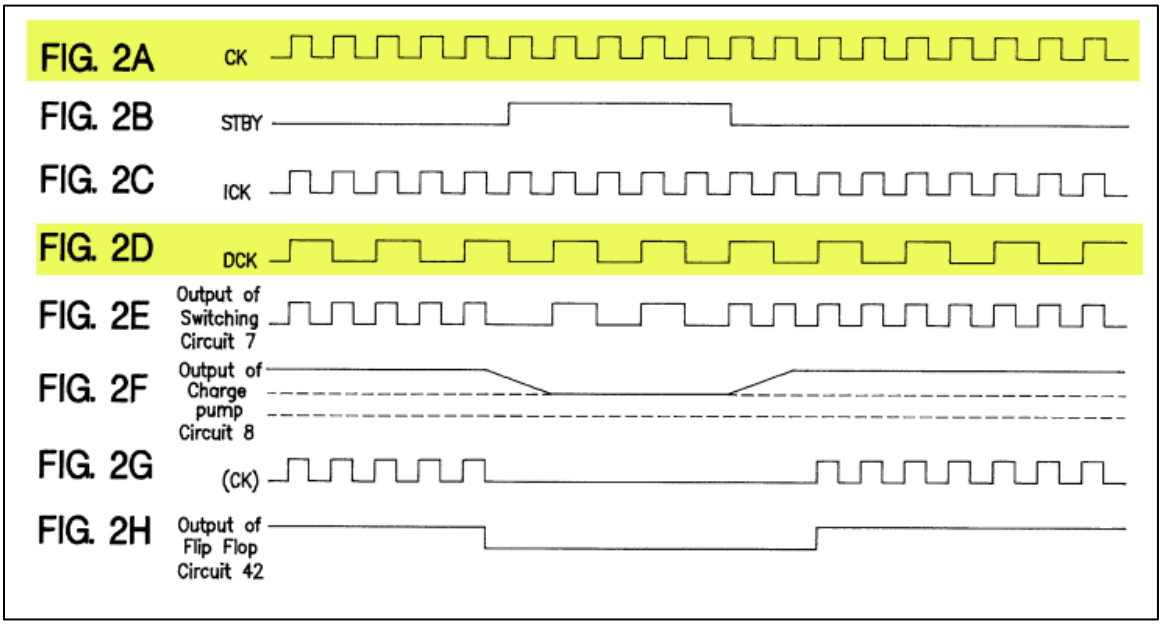
FIG. 6
PRIOR ART

172. Therefore, it is my opinion that the clock signal supplied to transistor T23c is the "output of switching circuit 7," as shown below. This clock signal is changed to either CK or DCK in accordance with the signal STBY (the claimed "control signal").



(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.*

173. In my opinion, Hiiragizawa discloses claim limitation 6[d]. As I discussed above in connection with claim limitation 6[c], the frequency of the clock signal to be supplied to transistor T23c (the claimed "second charge pump circuit") is changed to DCK when the signal STBY is at the active level, where "the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x." Hiiragizawa at 6:56-62. In my opinion, Hiiragizawa's Figure 2 further shows that the frequency of the divided clock signal DCK is obtained by dividing the clock signal CK.



E. Claim 7

(i) 7[pre]: *An internal voltage generating circuit comprising:*

174. In my opinion, Hiiragizawa discloses an internal voltage generating circuit, as discussed in 3[pre]. *See* § XI.B.(i) above.

(ii) 7[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and* 7[b]: *a second charge pump circuit configured to generate a third voltage from the second voltage,*

175. In my opinion, Hiiragizawa discloses claim limitations 7[a]-[b], as I discussed in connection with claim limitations 3[a]-[b]. *See* § XI.B.(ii) above.

(iii) 7[c]: *wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.*

176. In my opinion, Hiiragizawa discloses claim limitation 7[c]. For example, as shown below, Hiiragizawa discloses that "**switching circuit 7**" "supplies the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x to the charge pump circuit 8 when the standby signal STBY is at the active level, and supplies the clock signal CK from the outside without change to the charge pump circuit 8 when the signal STBY is at the inactive level." Hiiragizawa at 6:56-62.

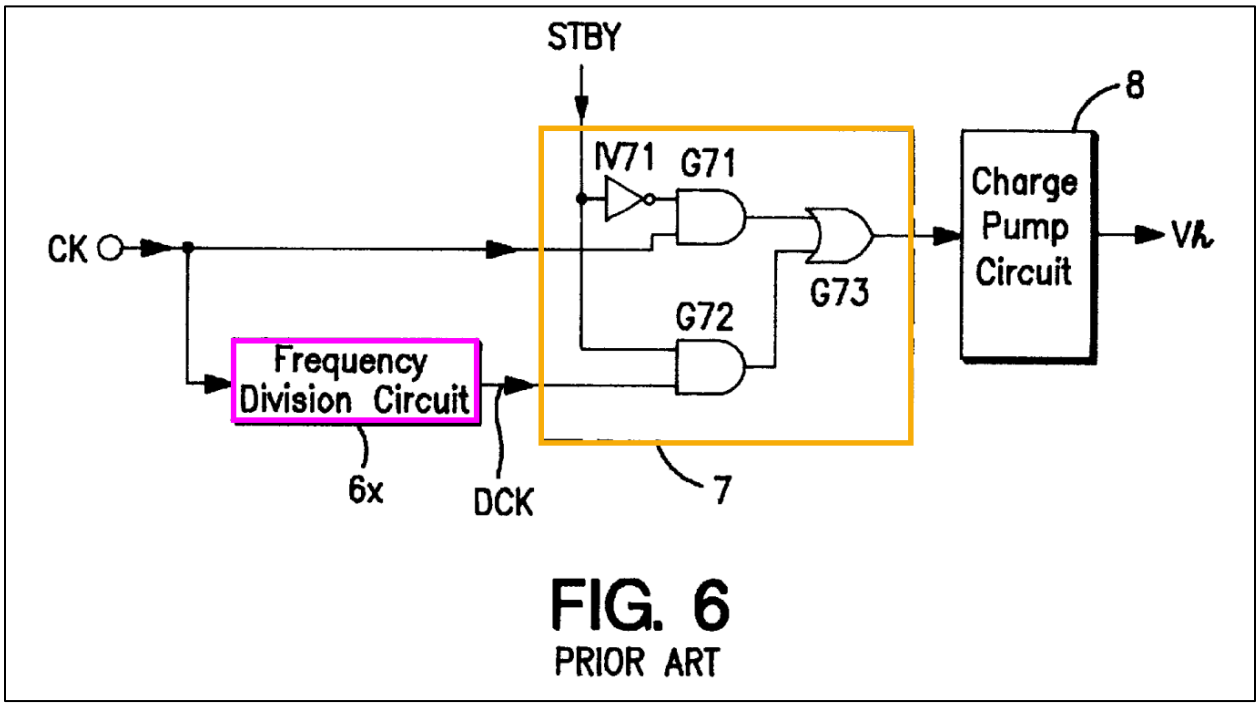
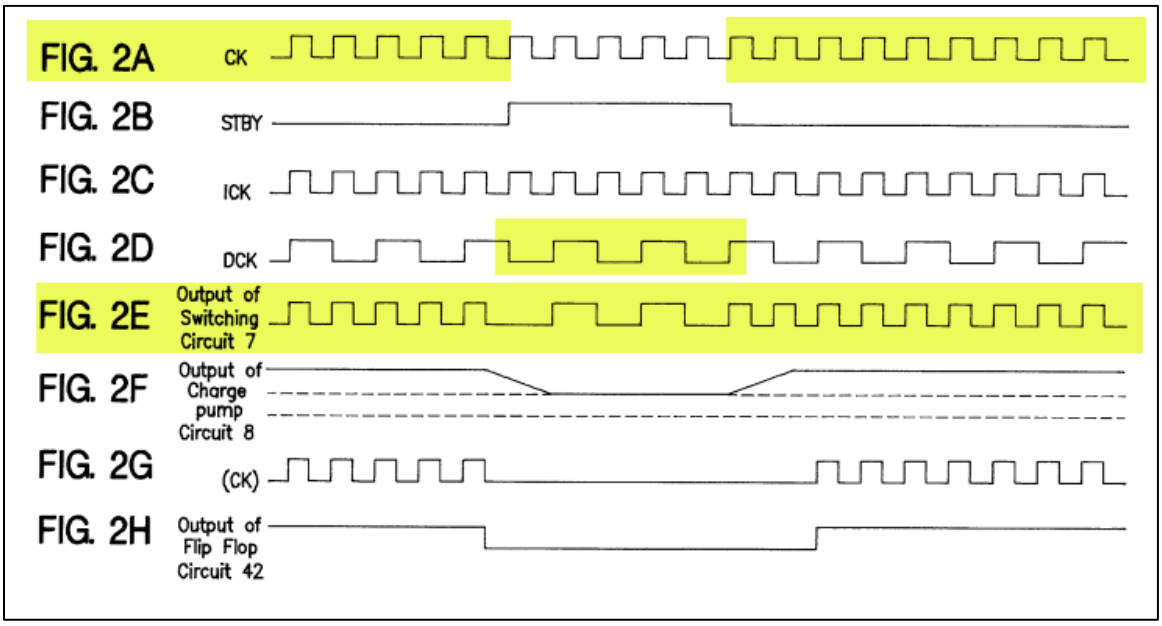


FIG. 6
PRIOR ART

177. Therefore, it is my opinion that the output of switch circuit 7 is a "clock signal to be supplied to the second charge pump circuit" (transistor T23c).

178. Further, in my opinion, a length of a period in which the clock signal, namely the "output of switching circuit 7," is in a high state is demonstrated in Figure 2E below. The length of a period is changed to that of either CK (shorter period, Fig. 2A) or DCK (longer period, Fig. 2D) in accordance with the signal STBY (*i.e.*, the "control signal", Fig. 2B).



F. Claim 8

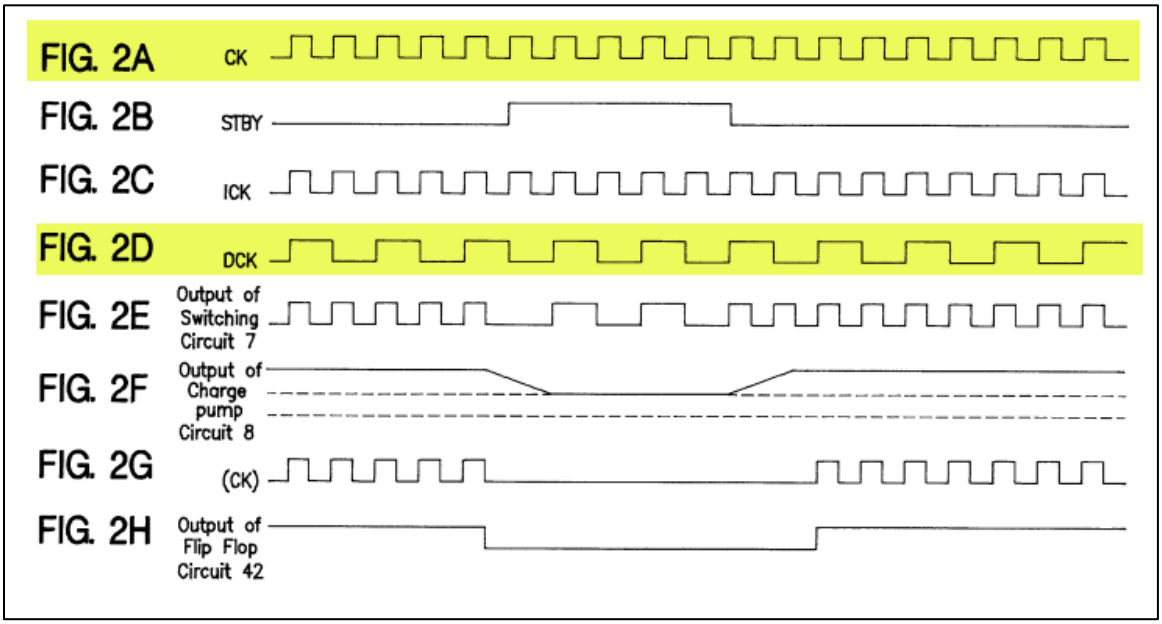
(i) 8[pre]: *The internal voltage generating circuit of claim 7,*

179. In my opinion, Hiiragizawa discloses an internal voltage generating circuit, as I discussed in connection with 3[pre]. *See* § XI.B.(i) above.

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high*

state is changed to a frequency which is obtained by dividing an original frequency.

180. In my opinion, Hiiragizawa discloses claim limitation 8[a]. As discussed above in connection with claim limitation 6[c] and claim 7, "the length of a period in which the clock signal to be supplied to the second charge pump circuit" (e.g., transistor T23c) is changed to DCK when the signal STBY is at the active level, where "the divided clock signal DCK obtained by frequency division in the frequency division circuit 6x." Hiiragizawa at 6:56-62. In my opinion, Hiiragizawa's Figure 2 further shows that the length of a period of the divided clock signal DCK is "obtained by dividing an original frequency" of the clock signal CK.



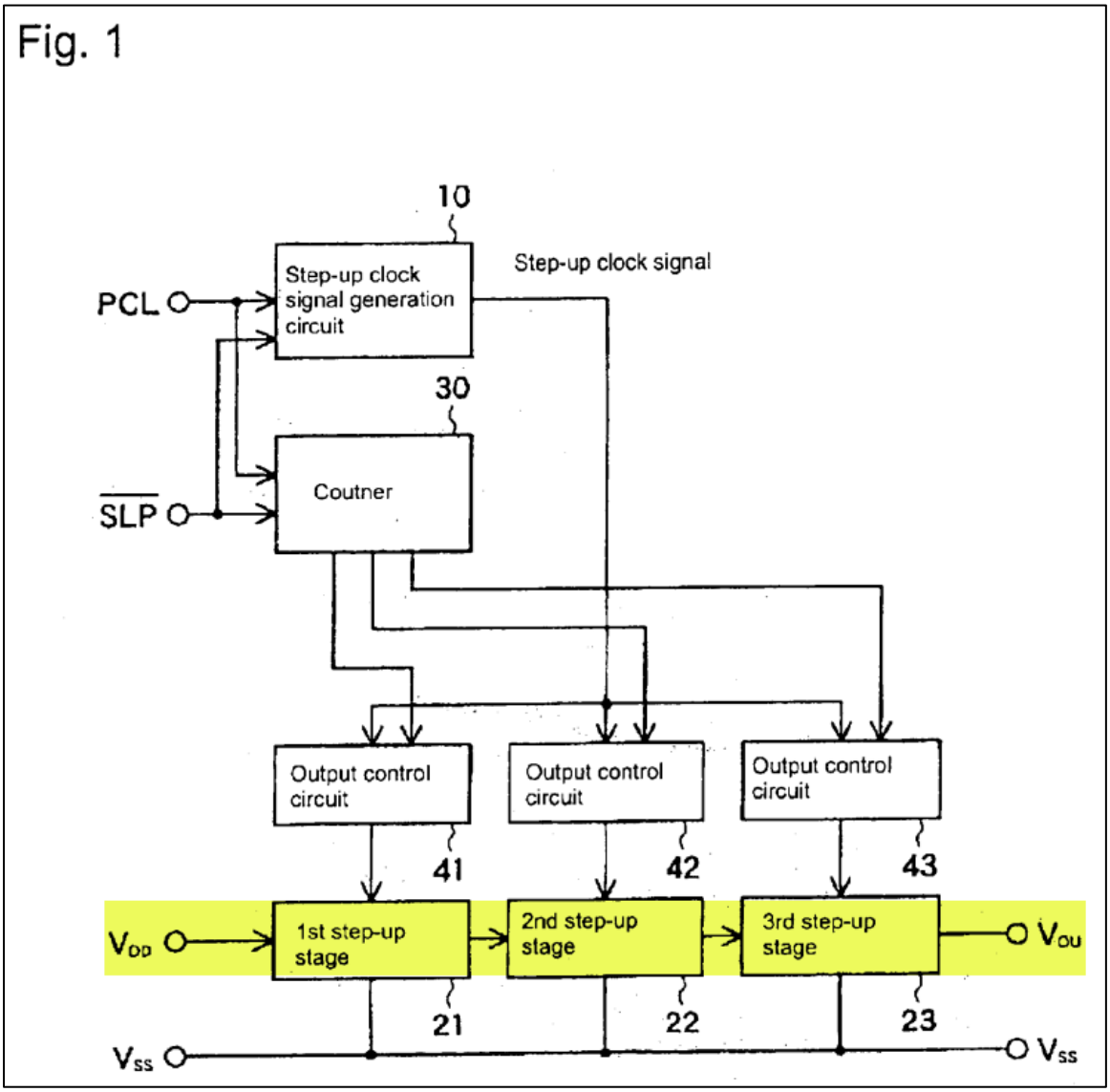
XII. GROUND 4: ITO

A. Overview of Ito

181. Ito is prior art under at least pre-AIA 35 U.S.C. §§ 102(a)-(b). I understand that Ito was patented on Dec. 28, 2004 and thus before July 9, 2008 priority date of the '231 Patent. I further understand that Ito was not considered by the Examiner during prosecution of the '231 Patent.

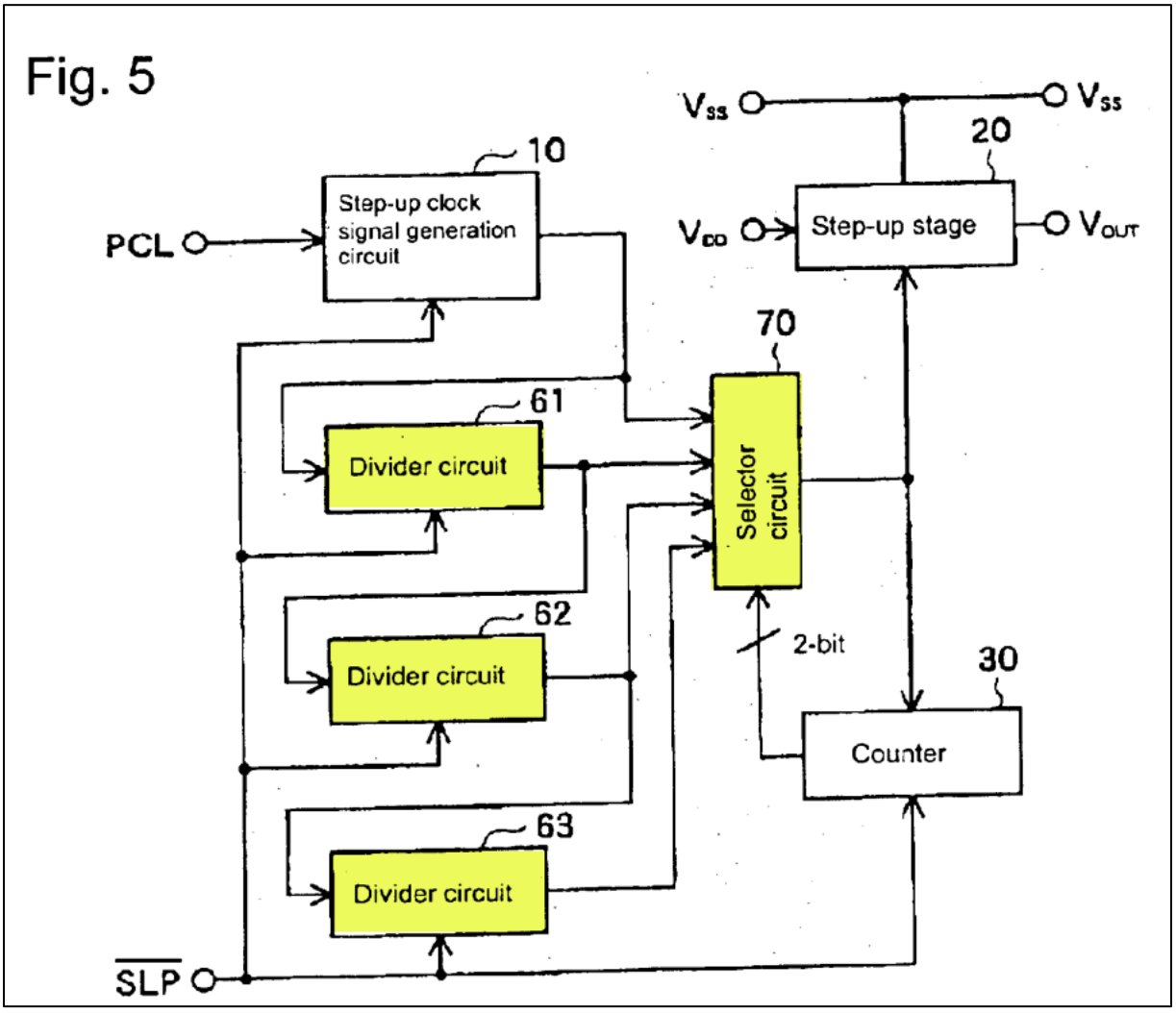
182. In my opinion, Ito discloses "step-up circuits that perform a charge pump operation." Ito at 1:5-7. Specifically, in a first embodiment, Ito discloses a step-up circuit with "**a plurality of step-up stages** (which indicate first-third step-up stages 21-23 in FIG. 1) that successively step up voltages between a first power supply voltage V_{DD} and a second power supply voltage V_{SS} (which is a ground potential in the present embodiment) based on the step-up clock signal generated by the step-up clock signal generation circuit 19 and output an output potential V_{OUT}." Ito at 3:64-4:9, Fig. 1.

Fig. 1



183. In another embodiment, the step-up circuit in Ito's Fig. 5 includes "***at least one step-up stage 20***," which a POSITA would have understood to be in reference to the plurality of step-up stages described in Ito's Fig. 1. Ito at 5:58. In my opinion, Ito's Figure 5 also "includes a step-up clock signal generation circuit 10 that generates a step-up clock signal based on a power clock signal PCL supplied, a plurality of **frequency-divider circuits 61-63** that individually frequency-divide

the step-up clock signal and output plural frequency-divided clock signals, and a **selector circuit 70** that selects one of the clock signals among the step-up clock signal and the plural frequency-divided clock signals." Ito at 5:46-55, Fig. 5.



B. Claim 1

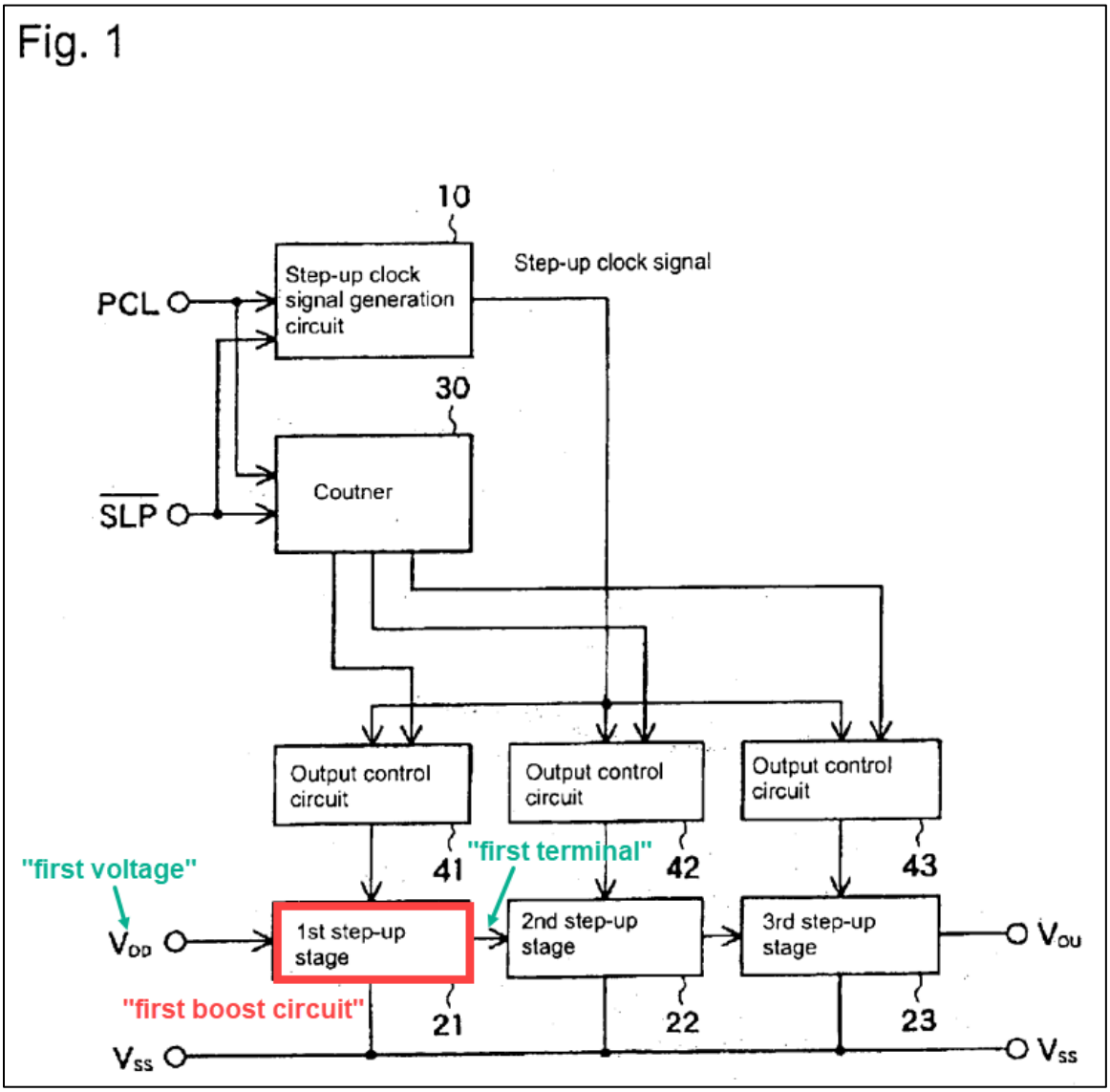
(i) 1[pre]: *An internal voltage generating circuit comprising:*

184. If the preamble is deemed to be limiting, it is my opinion that Ito meets this preamble. For example, Figure 1 of Ito discloses "a plurality of step-up stages

… that successively **step up voltages**" to generate a power supply voltage. Ito at 4:2-4. Likewise, it is my opinion that Ito's Figure 5 discloses a step-up circuit that includes "at least one step-up stage 20 that **steps up**, based on the clock signal selected by the selector circuit 70, a voltage … and outputs an output potential V_{OUT}." Ito at 5:56-63. In my opinion, the step-up circuit generates a power supply voltage, therefore Ito discloses "an internal voltage generating circuit."

(ii) 1[a]: *a first boost circuit provided between a first voltage and a first terminal;*

185. In my opinion, Ito discloses claim limitation 1[a]. For example, Figure 1 of Ito discloses a plurality of step-up stages, including "**1st step-up stage 21**," provided between V_{DD} (the claimed "first voltage") and a terminal at the output of 1st step-up stage 21 (the claimed "first terminal"). Ito at 4:2-9. In my opinion, Ito's "1st step-up stage 21" is a first boost circuit because it steps up the input voltage VDD to a higher voltage at its output.



186. Although Ito's "1st step-up stage 21" is the first stage of the step up circuit, mapping them as such is at least consistent with how the Patent Owner interpreted claim limitations 3[a]-3[b]. In particular, in the infringement contentions in the related district court litigation, the Patent Owner mapped the claimed "first charge pump circuit" to one stage of a charge pump ("[redacted]"), as shown below. (EX1006, p. 5.)

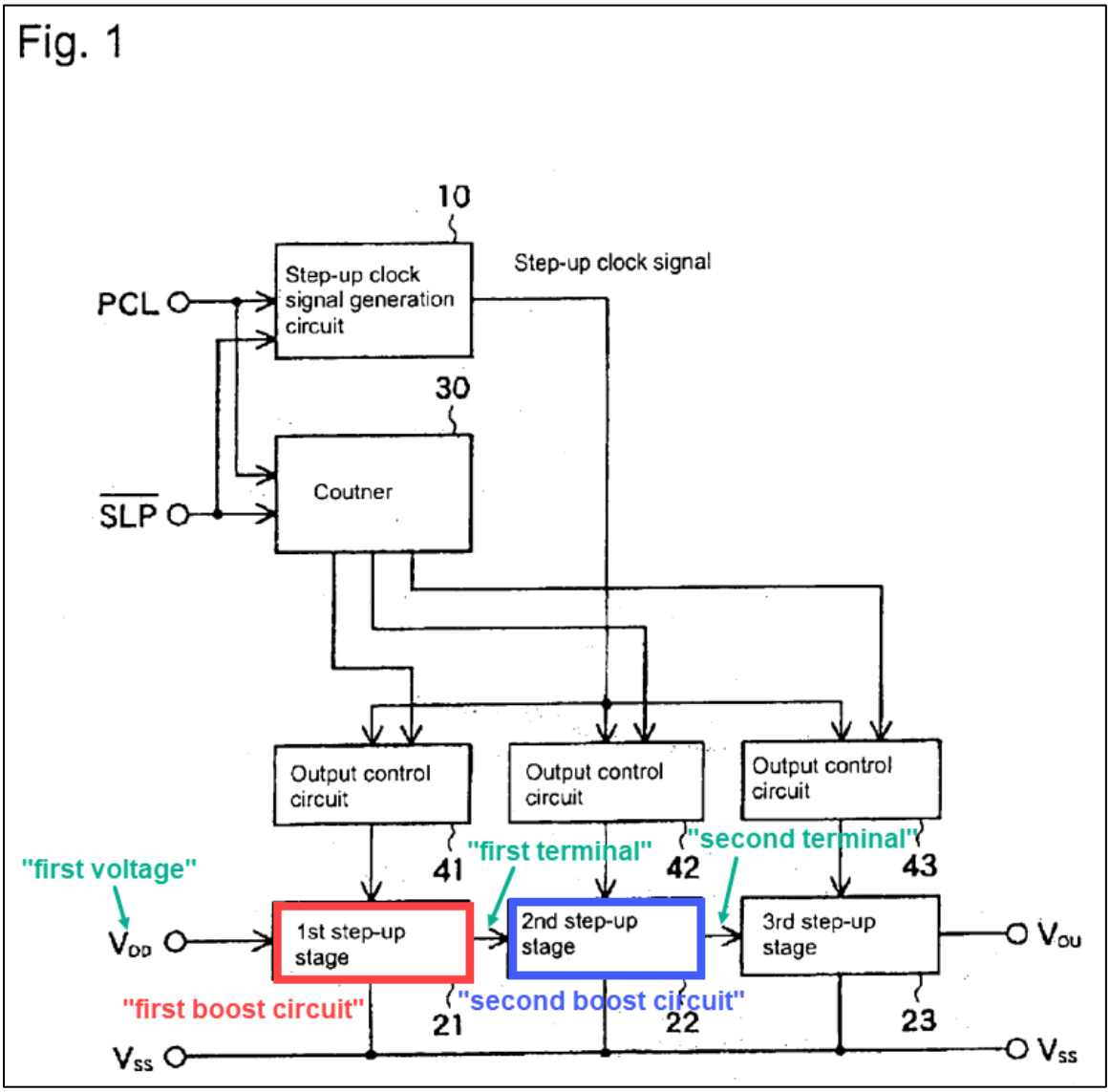


187. Likewise, in my opinion, Figure 5 of Ito discloses that its step-up circuit includes "**at least one step-up stage 20** that steps up, based on the clock signal selected by the selector circuit 70, a voltage … and outputs an output potential V_{OUT}." Ito at 5:56-63. As discussed above, it is my opinion that a POSITA would have understood the "***at least one*** step-up stage 20" in Ito's Figure 5 to include more than one stage, such as the "plurality of step up stages" 21-23 shown in Ito's Figure 1. In my opinion, each such step-up stage in Ito's Figure 5 is a "boost circuit" because it **steps up** a voltage, at least under Patent Owner's interpretation of claim 1. Accordingly, based on at least the Patent Owner's apparent interpretation, Figure 1 and Figure 5 of Ito each discloses a "first boost circuit."

(iii) 1[b]: *a second boost circuit provided between the first terminal and a second terminal;*

188. In my opinion, Ito discloses claim limitation 1[b]. Ito's Figure 1 discloses "**2nd step-up stage 22**," provided between the output terminal of the 1st step-up stage 21 (the claimed "first terminal") and the voltage at the output terminal of the 2nd step-up stage 22 (the claimed "second terminal"). Ito at 4:2-9. In my opinion, a POSITA would have understood Ito's "2nd step-up stage 21" is a second boost circuit because it steps up an input voltage to a higher voltage at its output.

Fig. 1

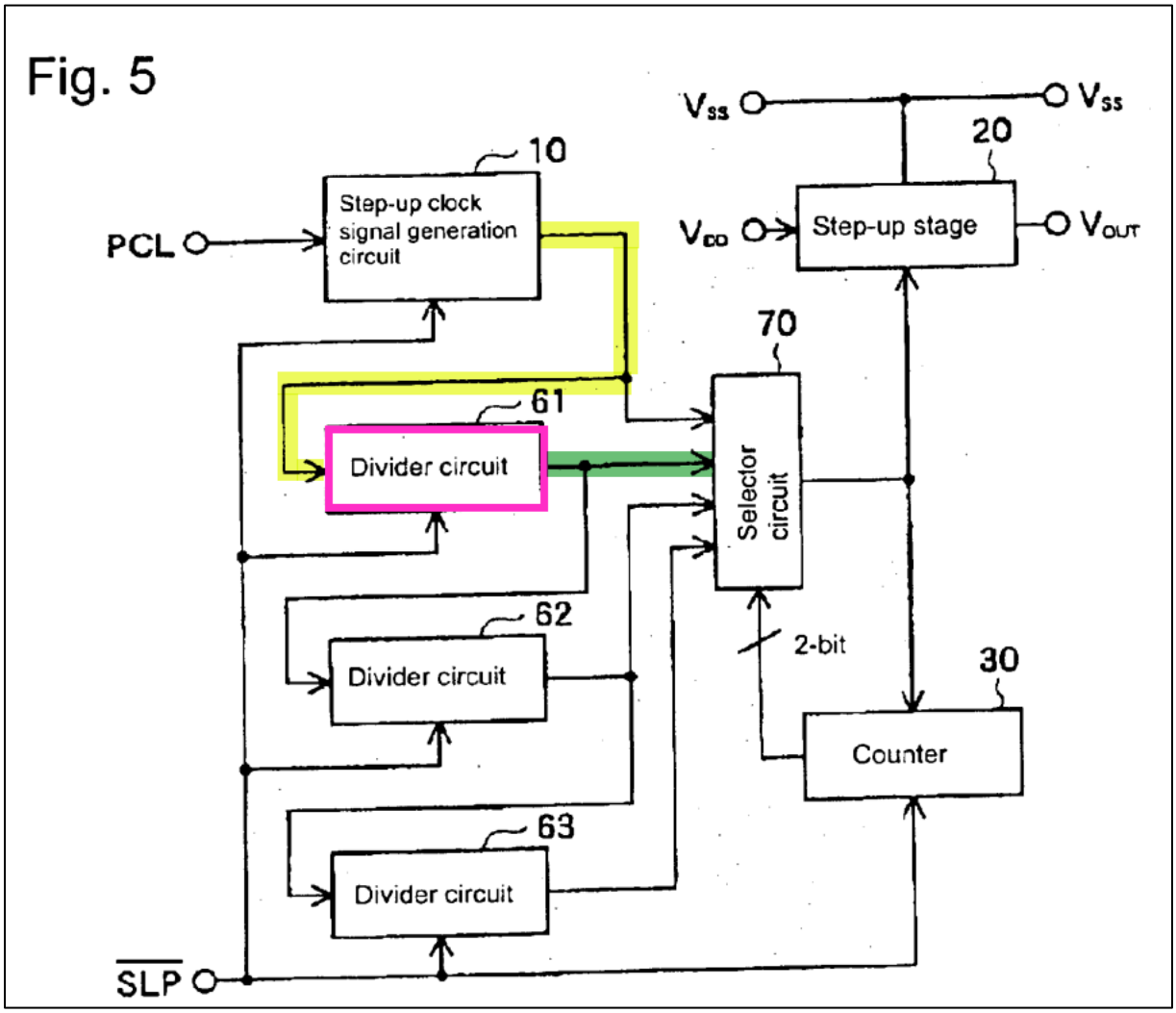


189. Likewise, Figure 5 of Ito discloses that its step-up circuit includes "**at least one step-up stage 20** that steps up, based on the clock signal selected by the selector circuit 70, a voltage … and outputs an output potential V_{OUT}." Ito at 5:56-63. In my opinion, the "step-up stage 20" in Figure 5 can include more than one stage, such as the three-stage configuration shown in Ito's Figure 1. Each such step-up stage in Ito's Figure 5 would have been a boost circuit because it **steps up** a

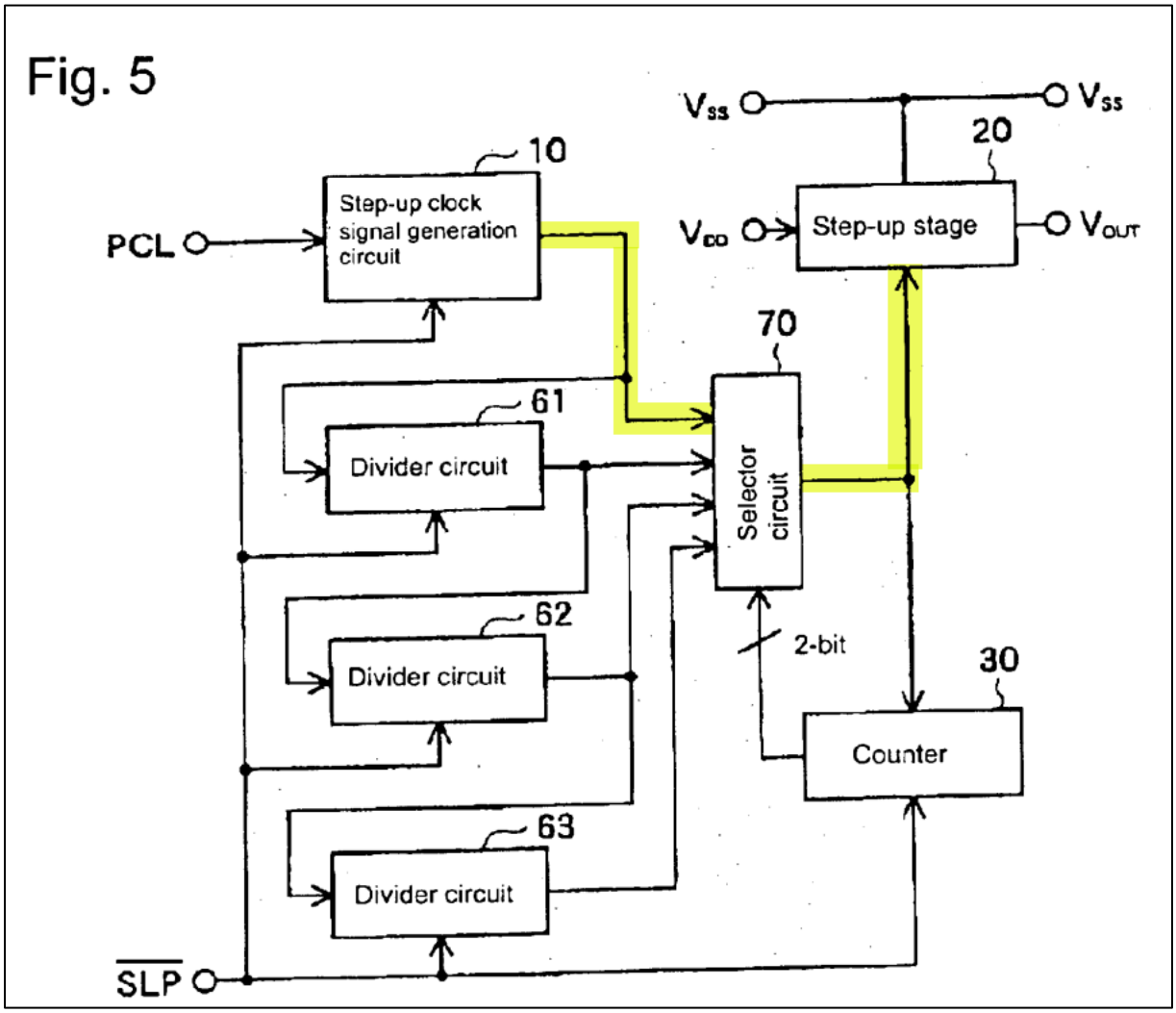
voltage, at least under Patent Owner's interpretation of claim 1. Therefore, based on at least the Patent Owner's apparent interpretation, it is my opinion that Figure 1 and Figure 5 of Ito each discloses the claimed "second boost circuit."

(iv) 1[c]: *a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and*

190. In my opinion, Ito discloses claim limitation 1[c]. For example, Ito discloses "a plurality of **frequency-divider circuits 61-63** that individually frequency-divide the step-up clock signal and output plural frequency-divided clock signals." Ito at 5:51-53. As shown in Figure 5 below, the frequency-divider circuit 61 receives the "step-up clock signal" (the claimed "first clock signal," shown in yellow highlighting) from step-up clock signal generation circuit 10 and outputs a "frequency-divided clock signal" (the claimed "second clock signal," shown in green highlighting). Ito at 5:48-53.



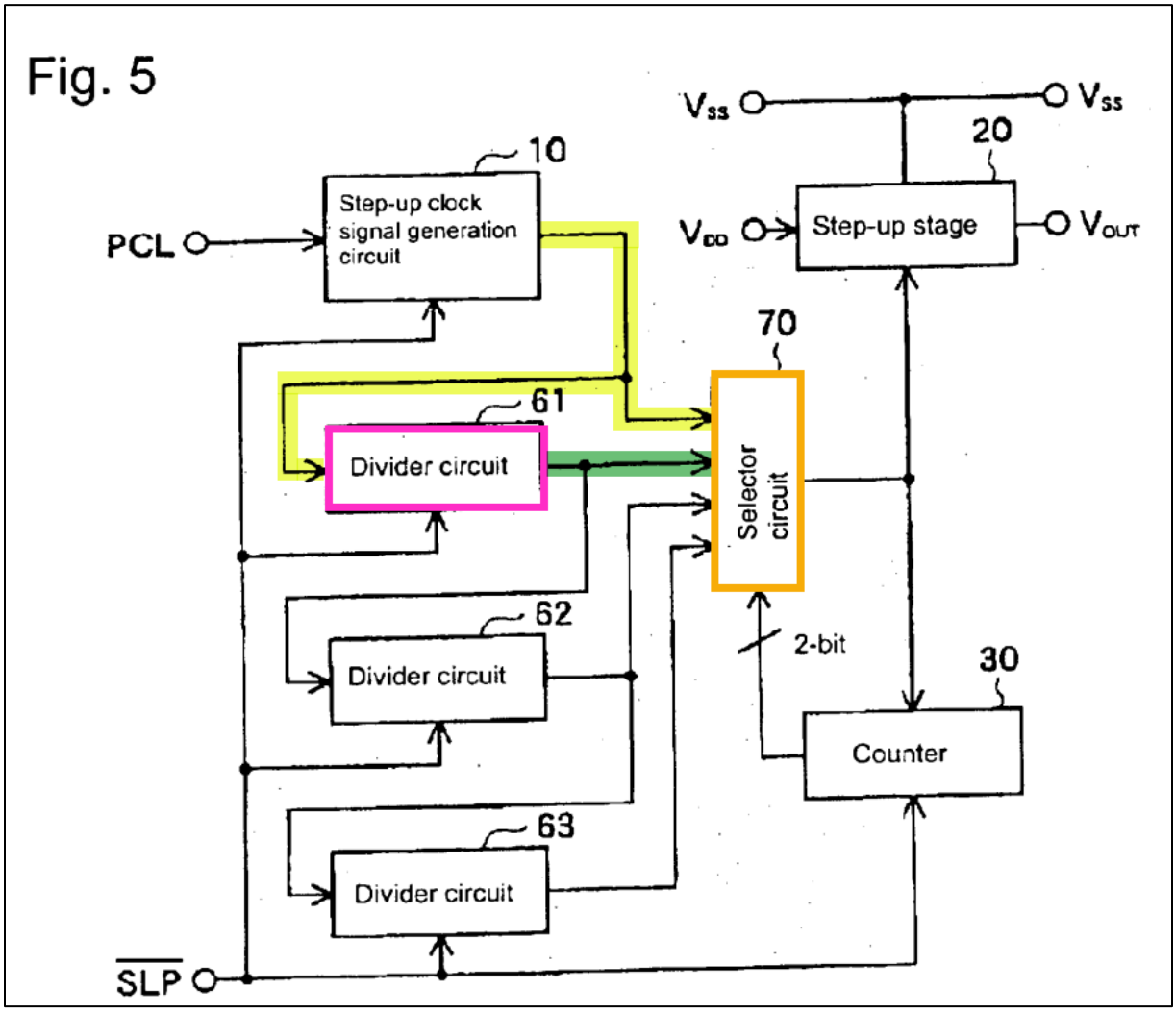
191. Further, as shown below, it is my opinion that the original "step-up clock signal" is supplied to at least one of the step-up stages 20. Accordingly, Ito discloses the frequency dividing circuit of claim limitation 1[c].



(v) 1[d]: *a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.*

192. In my opinion, Ito discloses claim limitation 1[d]. For example, Ito discloses "a **selector circuit 70** that selects one of the clock signals among the step-up clock signal and the plural frequency-divided clock signals." Ito at 5:53-55. In my opinion, Ito's selector circuit 70 is a buffer circuit because it is a multiplexer that accepts multiple inputs (clock signals), selects one such clock signal, and outputs it

to the at least one step-up stage 20. The '231 patent identifies multiplexer/selector circuits as exemplary embodiments of a buffer circuit. *See* '231 Patent at Figs. 3 and 7 (element 202); Ito at 5:56-58.



193. Therefore, it is my opinion that Ito discloses a selection circuit 70 ("a buffer circuit") configured to select and supply the step-up clock signal ("the first clock signal") or the plural frequency-divided clock signals ("the second clock signal") to one of the at least one step-up stage 20 ("the second boost circuit").

C. Claim 3

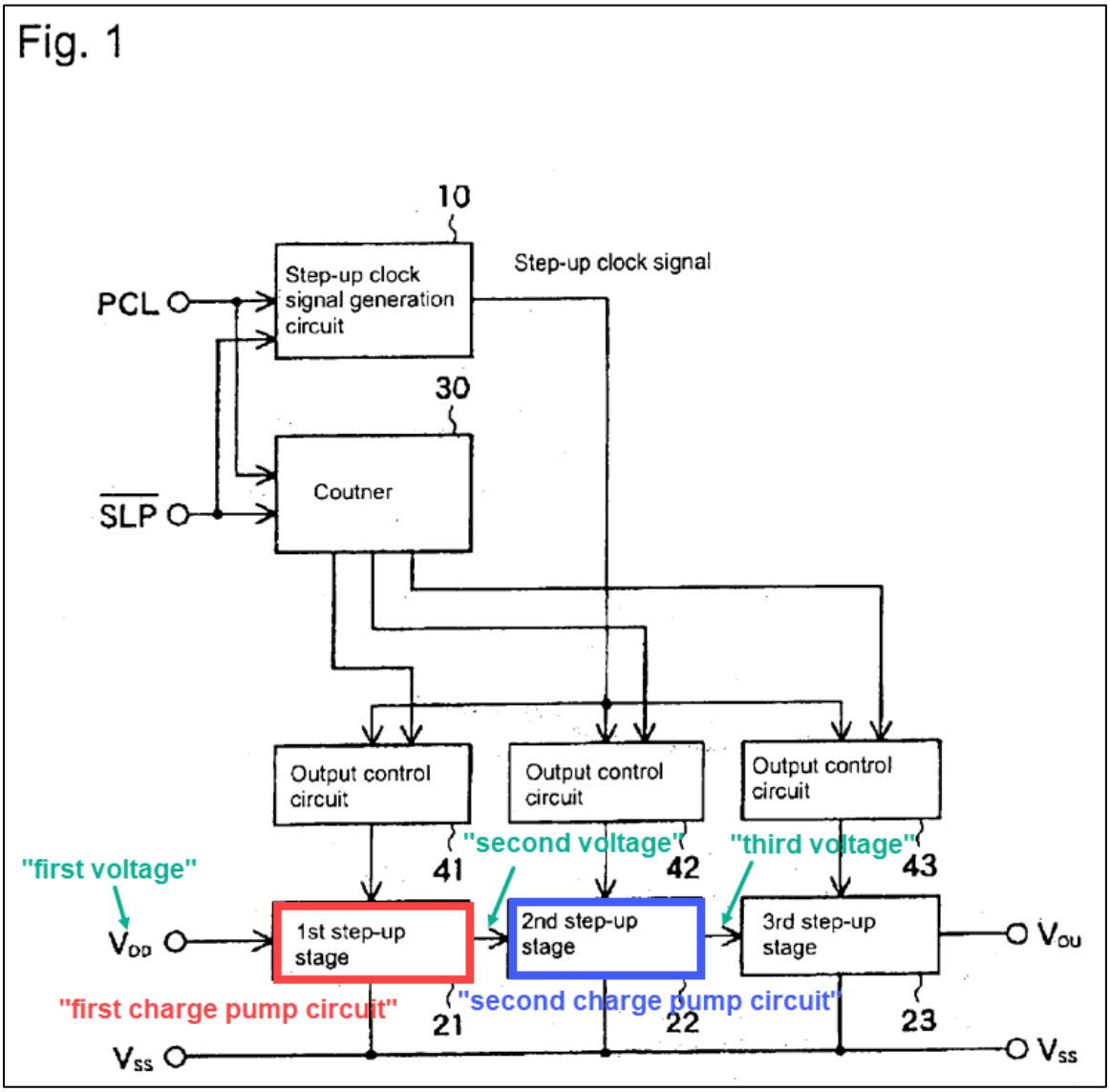
(i) 3[pre]: *An internal voltage generating circuit comprising:*

194. In my opinion, Ito discloses an internal voltage generating circuit, as I discussed for 1[pre]. *See* § XII.B.(i) above.

(ii) 3[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; a second charge pump circuit configured to generate a third voltage from the second voltage;*

195. In my opinion, Ito discloses claim limitations 3[a]-3[b]. As discussed in claim limitation 1[a], it is my opinion that Figure 1 of Ito discloses a 1st step-up stage 21 ("a first charge pump circuit") configured to generate a voltage at its output terminal ("the second voltage") from V_{DD} ("the first voltage"). Likewise, as discussed in claim limitation 1[b], it is my opinion that Figure 1 also discloses a 2nd step-up stage 22 ("a second charge pump circuit") configured to generate a voltage at its output ("a third voltage") from the output of the 1st step-up stage 21.

Fig. 1



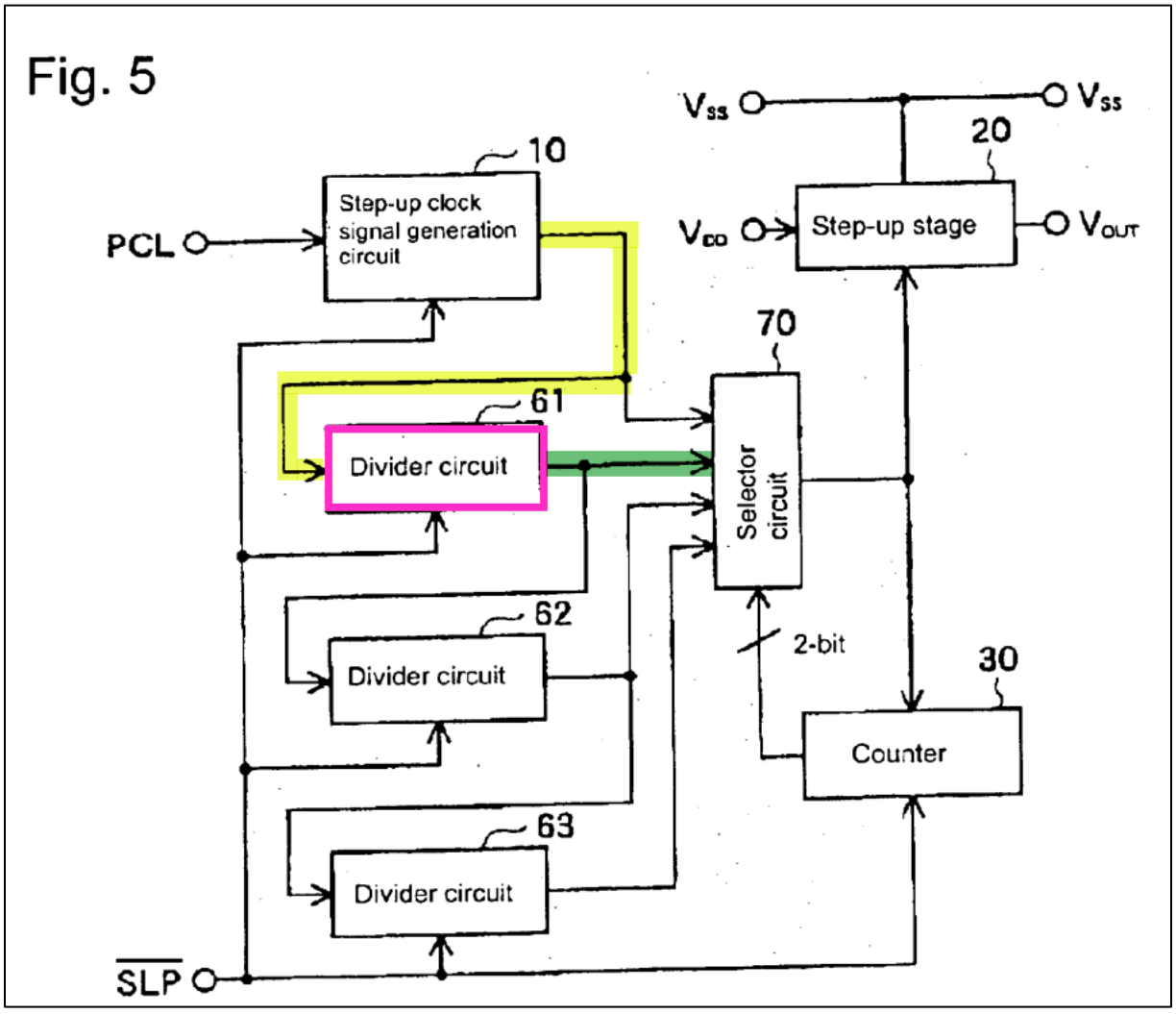
196. Likewise, in my opinion, Figure 5 of Ito discloses that its step-up circuit includes "**at least one step-up stage 20** that steps up, based on the clock signal selected by the selector circuit 70, a voltage … and outputs an output potential V_{OUT}." Ito at 5:56-63. For example, it is my opinion that the "step-up stage 20" in Figure 5 can include more than one stage, such as the three-stage configuration

shown in Ito's Fig. 1. Each such step-up stage in Ito's Fig. 5 is a "charge pump circuit" because it **steps up** a voltage.

197. Therefore, even if the step-up stages in Ito are stages within a single charge pump circuit, it is my opinion that they are the claimed first and second charge pump circuits at least according to how the Patent Owner interpreted claim limitations 3[a]-3[b].

(iii) 3[c]: *a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and*

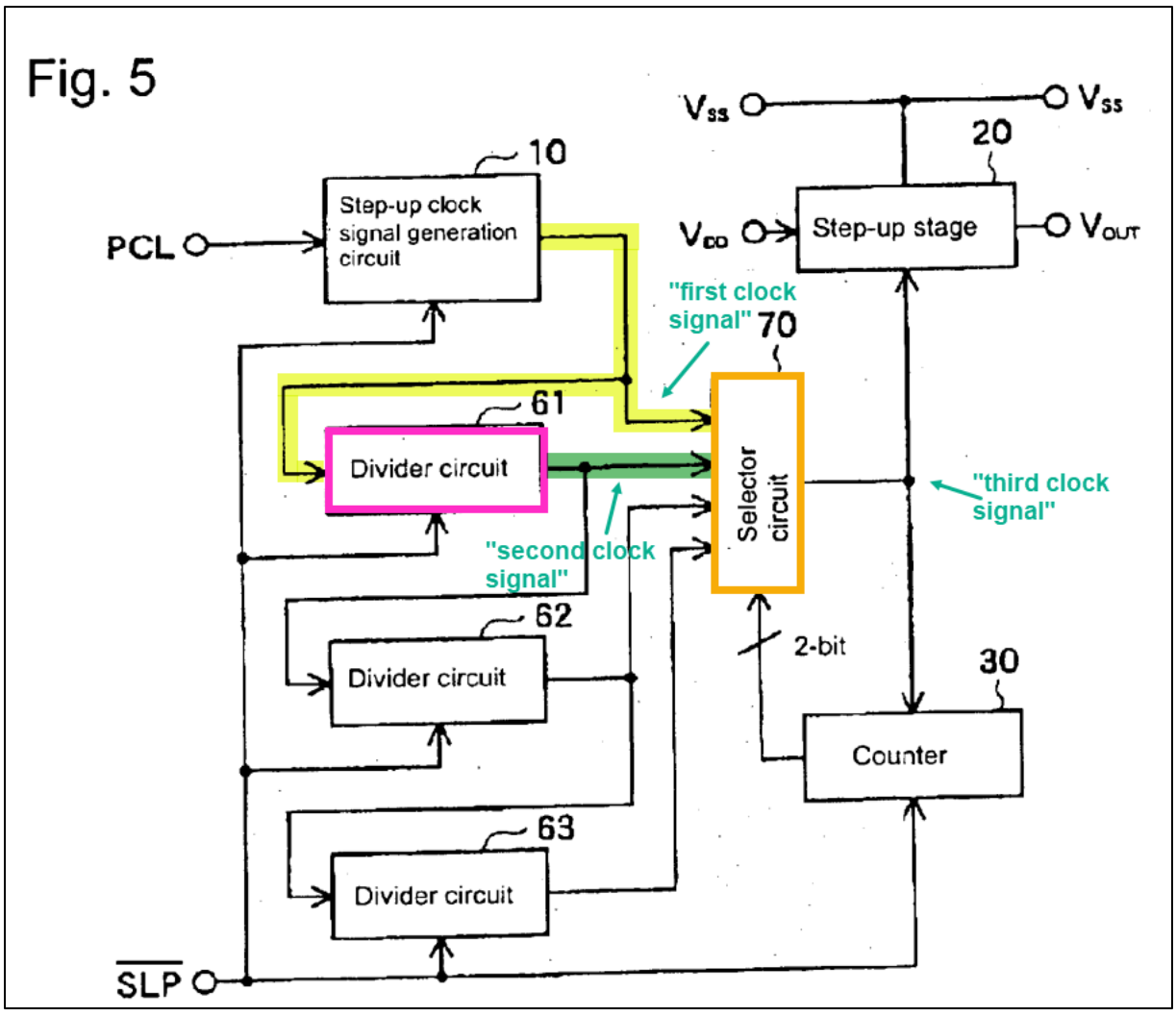
198. As discussed above in connection with claim limitation 1[c], it is my opinion that Ito discloses "a plurality of **frequency-divider circuits 61-63**" that individually frequency-divide the step-up clock signal (the claimed "first clock signal") and output plural frequency-divided clock signals (each a claimed "second clock signal"). Ito at 5:51-53.



(iv) 3[d]-[e]: ***a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal, wherein the third clock signal is supplied to the second charge pump circuit.***

199. As I discussed for claim limitation 1[d], it is my opinion that Ito discloses "a **selector circuit 70** that selects one of the clock signals among the step-up clock signal and the plural frequency-divided clock signals." Ito at 5:53-55. In my opinion, Ito's selector circuit 70 is a buffer circuit because it is a multiplexer that

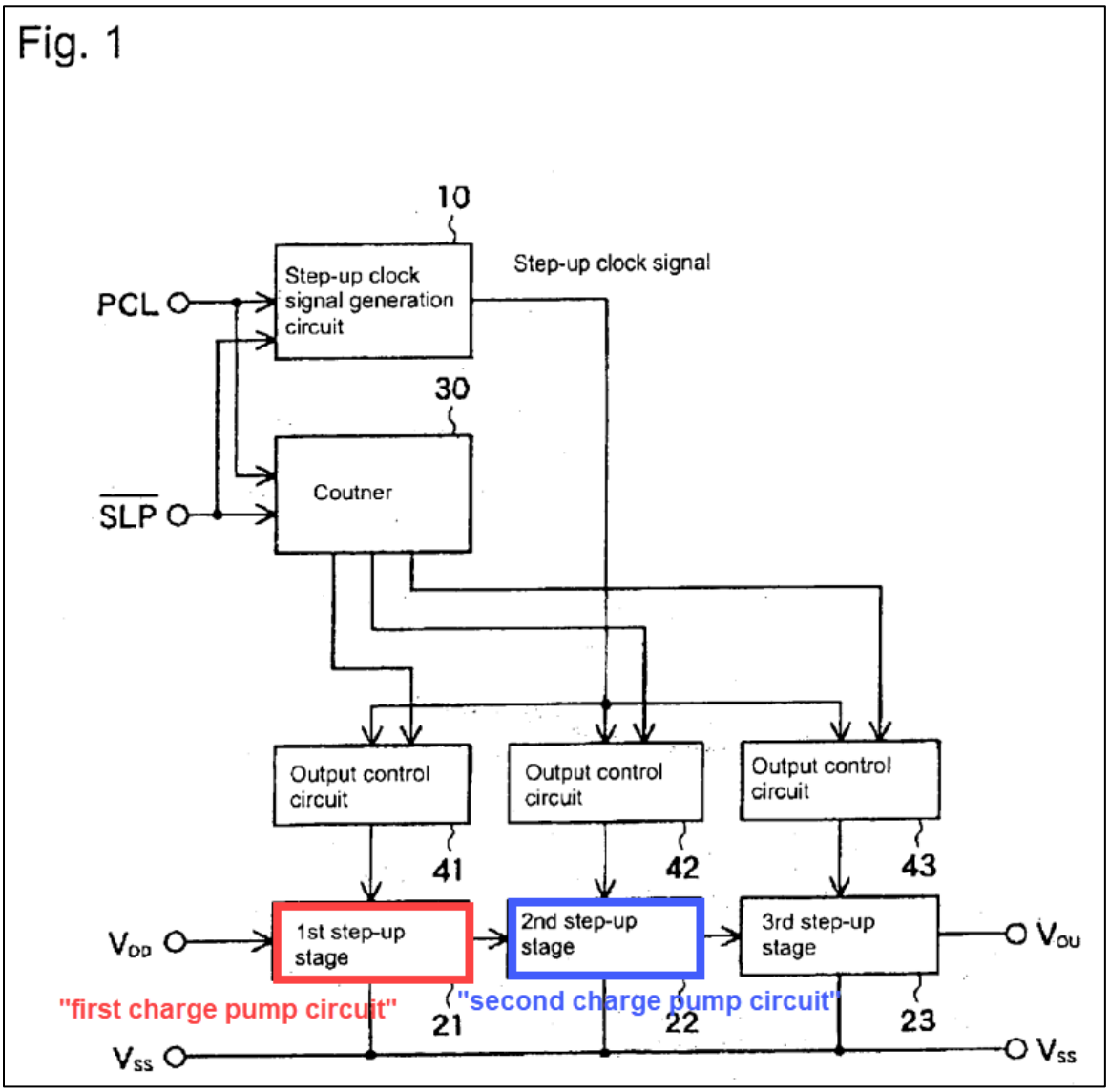
accepts multiple inputs (clock signals), selects one such clock signal, and outputs it to the at least one step-up stage 20. The ’231 patent identifies multiplexer/selector circuits as exemplary embodiments of a buffer circuit. *See* ’231 Patent at Figs. 3 and 7 (element 202); Ito at 5:56-58.



200. Further, Ito discloses that “**at least one step-up stage 20** [] steps up, **based on the clock signal selected by the selector circuit 70**, a voltage.” Ito at

5:58-59. In my opinion, the "at least one step-up stage 20" in Ito's Fig. 5 can include the three-stage configuration disclosed in Fig. 1, shown below.

Fig. 1



201. Therefore, under at least Patent Owner's apparent interpretation of claim 1, it is my opinion that the clock signal selected by the selector circuit 70 (the claimed "buffer circuit") can be supplied to the 2nd step-up stage 22 shown in Ito's Figure 1 (the claimed "second charge pump circuit").

202. In the event that Ito is found to not expressly disclose this limitation, in my opinion, it would have been obvious to modify Ito's embodiment in Figure 5 with the three-stage step-up circuit design from Ito's Figure 1. Doing so would involve no more than a routine combination of known circuit elements, particularly when Ito's Figure 5 already provides the motivation by disclosing that the step-up stage therein is "at least one step-up stage 20," implying that multiple stages—such as the three-stage configuration of Fig. 1—have been contemplated. For the foregoing reasons, Ito at least renders obvious claim limitations 3[d]-3[e].

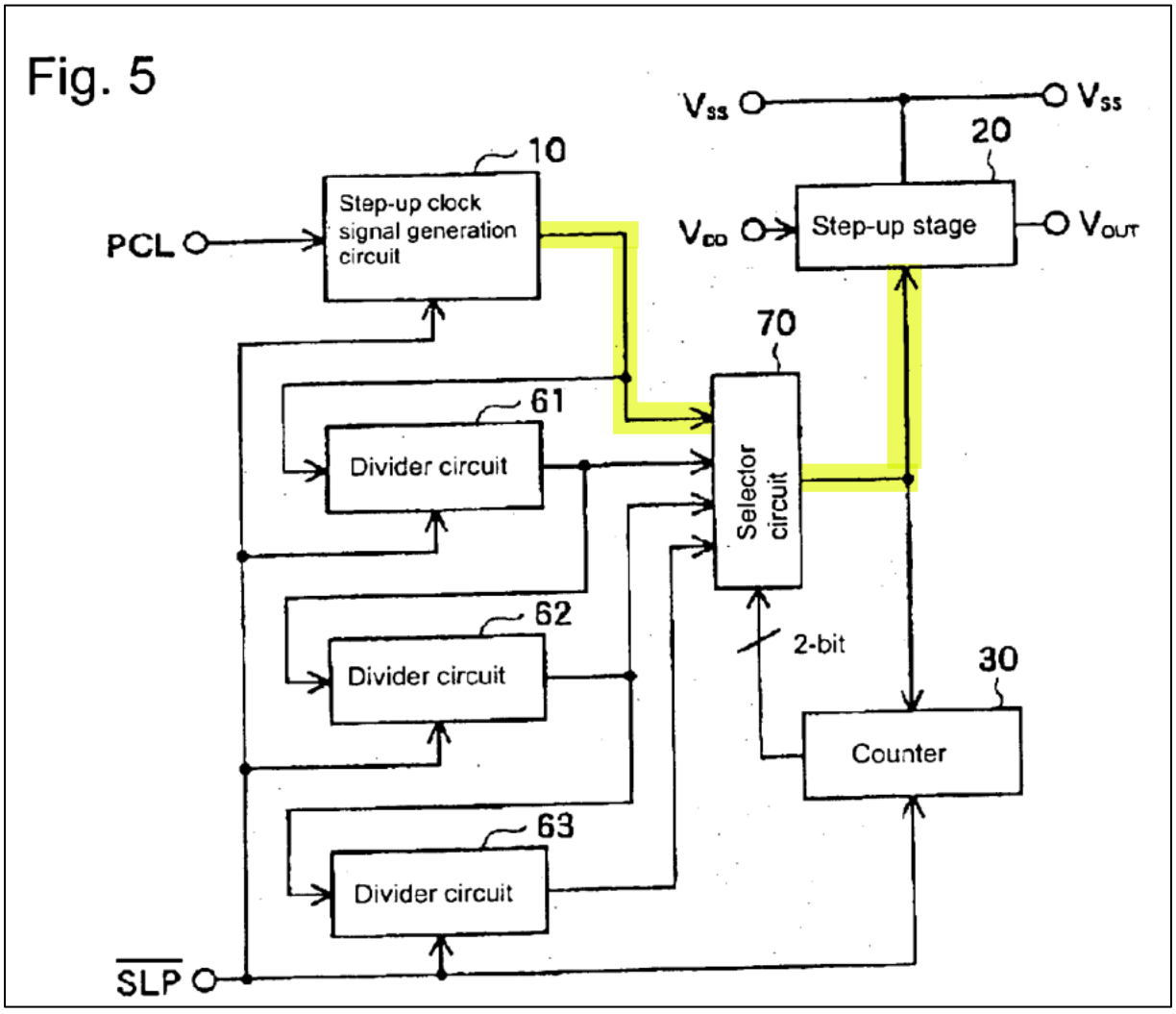
D. Claim 4

(i) 4[pre]: *The internal voltage generating circuit of claim 3, wherein*

203. In my opinion, Ito discloses an internal voltage generating circuit, as I discussed in 1[pre]. *See* § XII.B.(i) above.

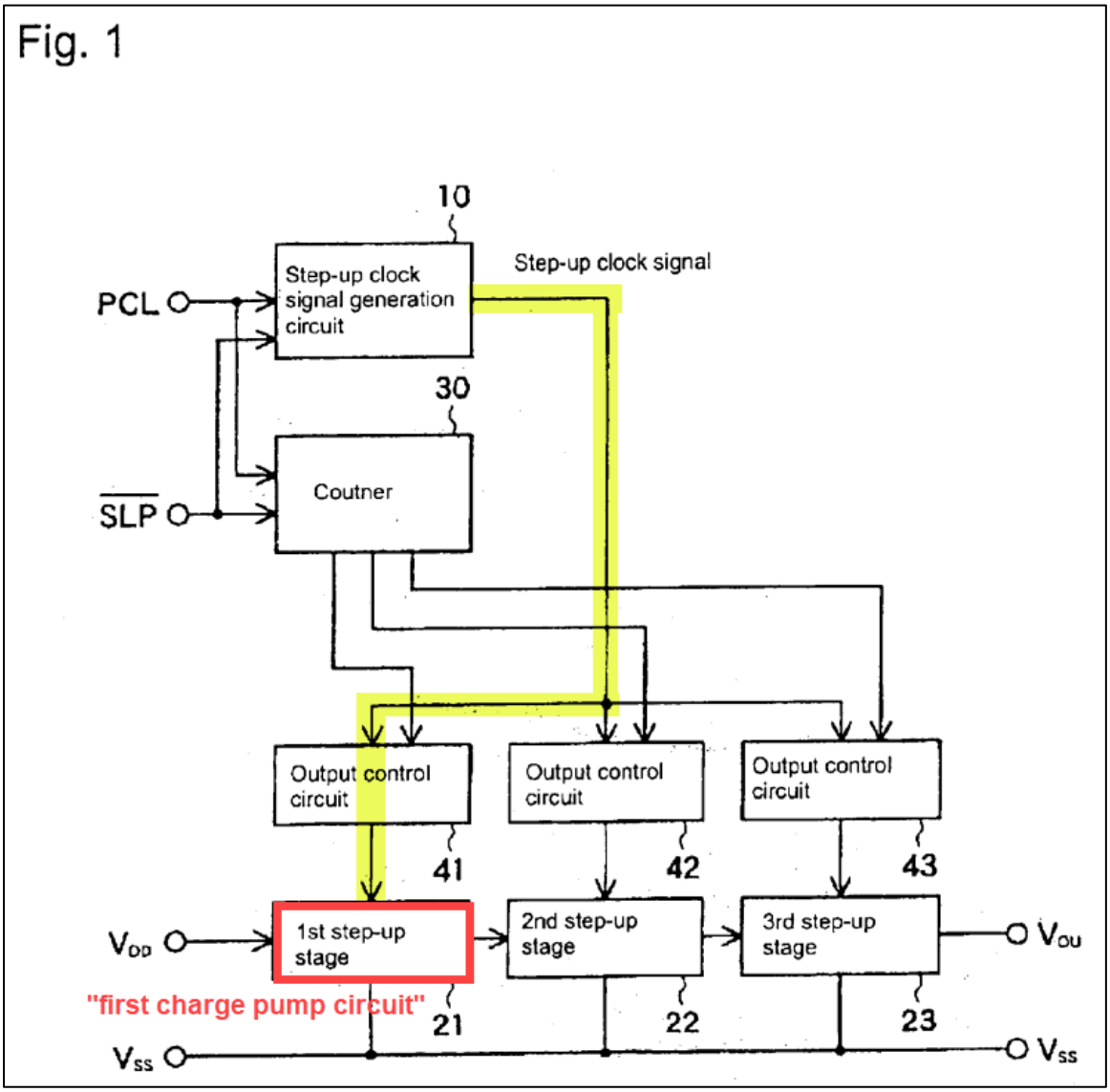
(ii) 4[a]: *a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.*

204. In my opinion, Ito renders claim limitation 4[a] obvious. Figure 5 of Ito shows that the original step-up clock signal (the claimed "first clock signal") can be supplied to the "at least one step-up stage 20," which includes the claimed "first charge pump circuit." Ito at 5:53-55.



205. In a similar way, Figure 1 of Ito shows the original step-up clock signal (the claimed "first clock signal") is supplied to the 1st step-up stage 21 (the claimed "first charge pump circuit"), as shown by the yellow-highlighted pathway below.

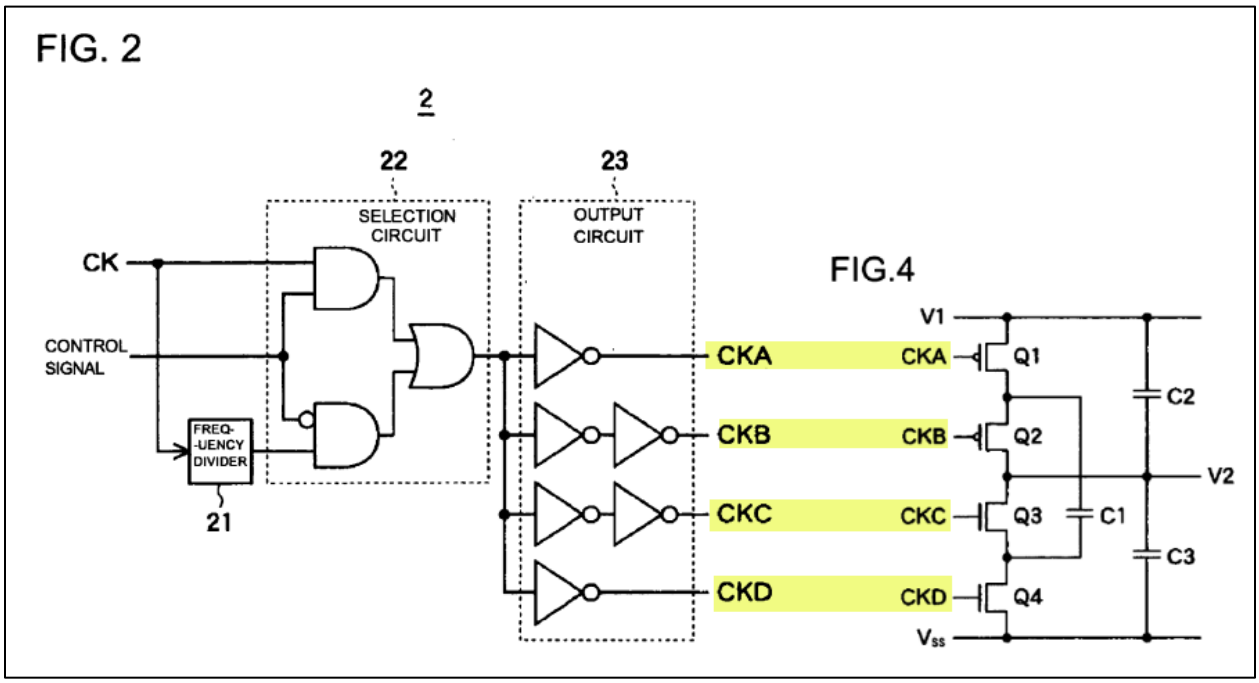
Fig. 1



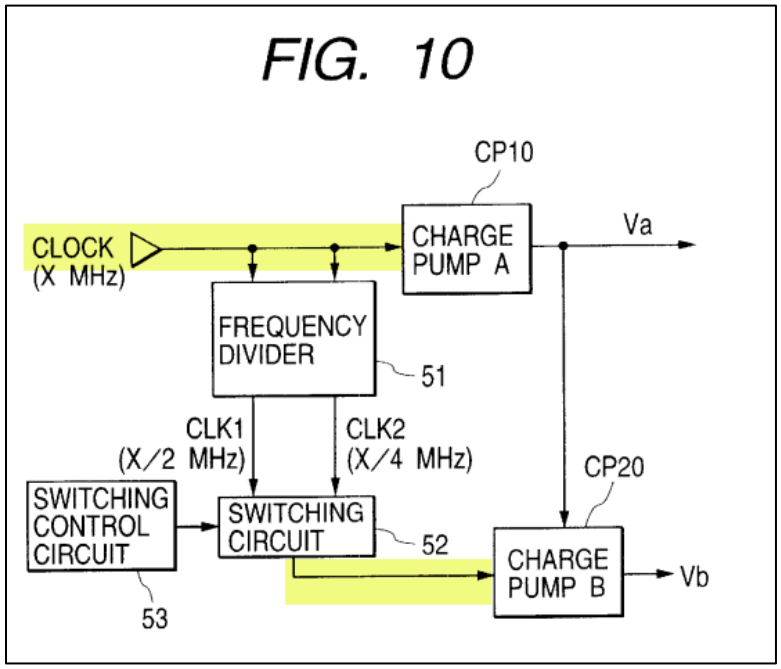
206. In my opinion, a POSITA would have been motivated to combine the step-up stages 21, 22, and 23 of Ito's Figure 1 with the disclosure of multiple clock signals in Ito's Figure 5. As I explained above, Ito itself supplies the motivation because the "step-up stage 20" of Figure 5 is disclosed as being "***at least one***" stage. *See* Ito at 5:56-63. In other words, a POSITA would have understood the "step up stage 20" in Ito's Fig. 5 to refer to the step-up stages 21, 22, and 23 in Ito's Fig. 1.

207. In my opinion, a POSITA would have been further motivated to supply individual clock signals to the step-up stages 21, 22, and 23 (as part of modified Fig. 5, as discussed above) in order to provide flexible control of individual charge pumps. In fact, many prior art did just so.

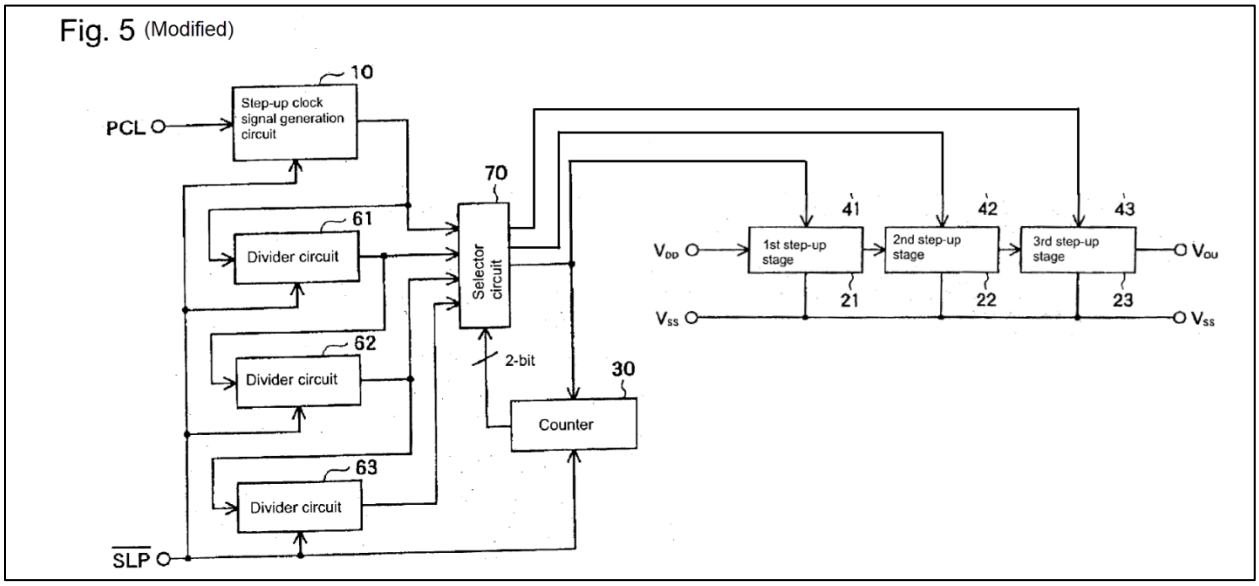
208. For example, as I explained above, in Fujise, four different clock signals (CKA, CKB, CKC, and CKD) are supplied to individual stages within a charge pump circuit, as shown below. *See* Fujise at [0004]-[0005] and [0027].



209. As another example, as I explained above, Kishimoto taught that different clock signals are supplied to charge pump A (CP10) and charge pump B (CP20), respectively.



210. A POSITA would have had a reasonable expectation of success to modify Ito's Fig. 1 and Fig. 5 because it was well-known in the art at the time of the July 9, 2008 priority date of the '231 Patent to supply different clock signals to different charge pump circuits (or to different stages within a charge pump). For example, a POSITA would have been motivated to, and succeed in creating, the modified Ito design below.



E. Claim 6

(i) 6[pre]: *An internal voltage generating circuit comprising:*

211. In my opinion, Ito discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § XII.B.(i) above.

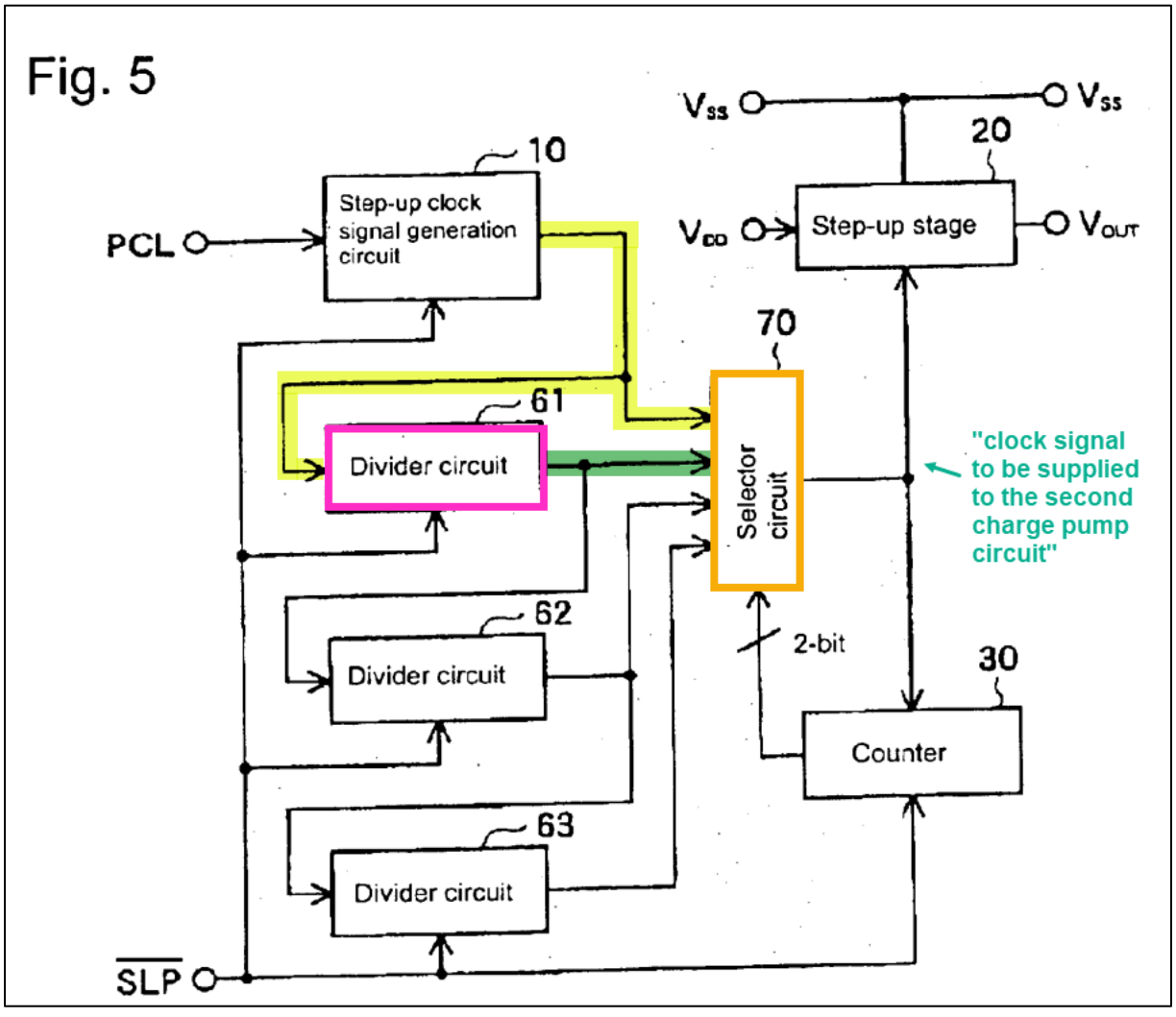
(ii) 6[a]-[b]: *a first charge pump circuit configured to generate a second voltage from a first voltage; and a second charge pump circuit configured to generate a third voltage from the second voltage,*

212. In my opinion, Ito discloses claim limitations 6[a]-[b], as I discussed in connection with claim limitations 3[a]-[b]. *See* § XII.C.(ii) above.

(iii) 6[c]: *wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and*

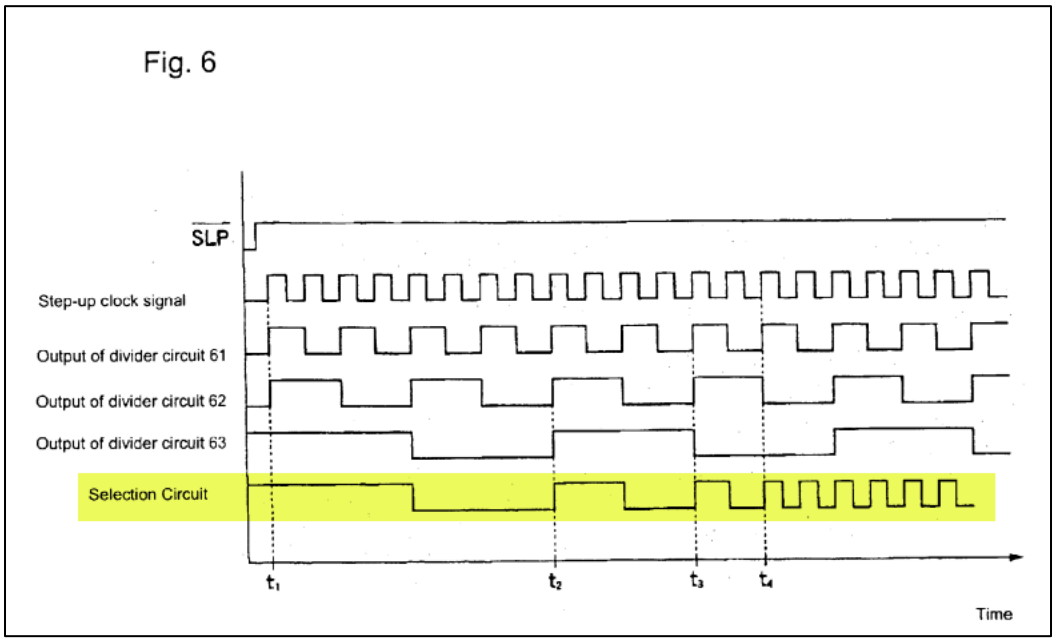
213. In my oinion, Ito discloses claim limitation 6[c]. For example, Ito discloses "a plurality of **frequency-divider circuits 61-63**" that individually

frequency-divide the step-up clock signal (the claimed "first clock signal") and output plural frequency-divided clock signals (each a claimed "second clock signal"). Ito at 5:51-53. Ito also discloses "a **selector circuit 70** [] selects one of the clock signals among the step-up clock signal (highlighted in yellow) and the plural frequency divided clock signals (one of which is highlighted in green)." Ito at 5:53-55.



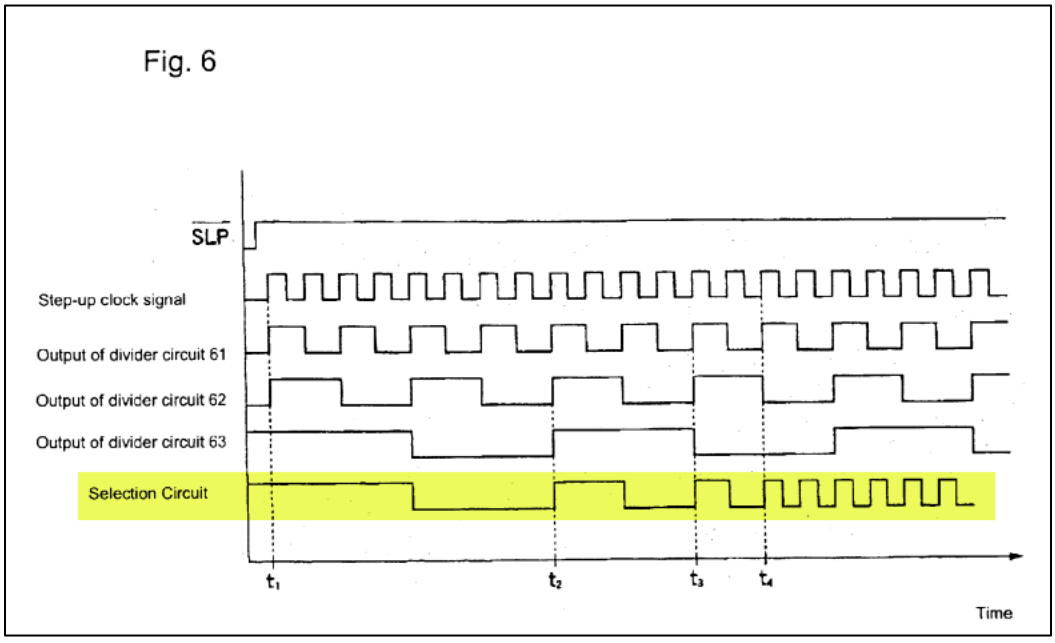
214. As indicated above in green text, it is my opinion that the "clock signal to be supplied to the second charge pump circuit" changes its frequency from the original step-up clock signal to one of the plural frequency-divided clock signals.

215. "Further, the step-up circuit includes a counter 30 that counts the clock signal selected by the **selector circuit 70** and at least one step-up stage 20 that steps up, based on the clock signal selected by the selector circuit 70, a voltage." Ito at 56-59. In my opinion, a POSITA would have understood Ito's counter to provide a 2-bit signal, as shown above, that controls the frequency of the output of selection circuit 70, which is the clock signal to be supplied to the second charge pump circuit. Indeed, Ito's Figure 6 shows how this output clock frequency may change.



(iv) 6[d]: *the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.*

216. In my opinion, Ito discloses claim limitation 6[d]. For example, the frequency of the output of the **selector circuit 70** (*i.e.*, the claimed "clock signal to be supplied to the second charge pump circuit") is changed to a frequency of the divider circuit 61 at time t3, shown below. The frequency of divider circuit 61 is obtained by dividing the original frequency of the step-up clock signal, shown below.



F. Claim 7

(i) 7[pre]: *An internal voltage generating circuit comprising:*

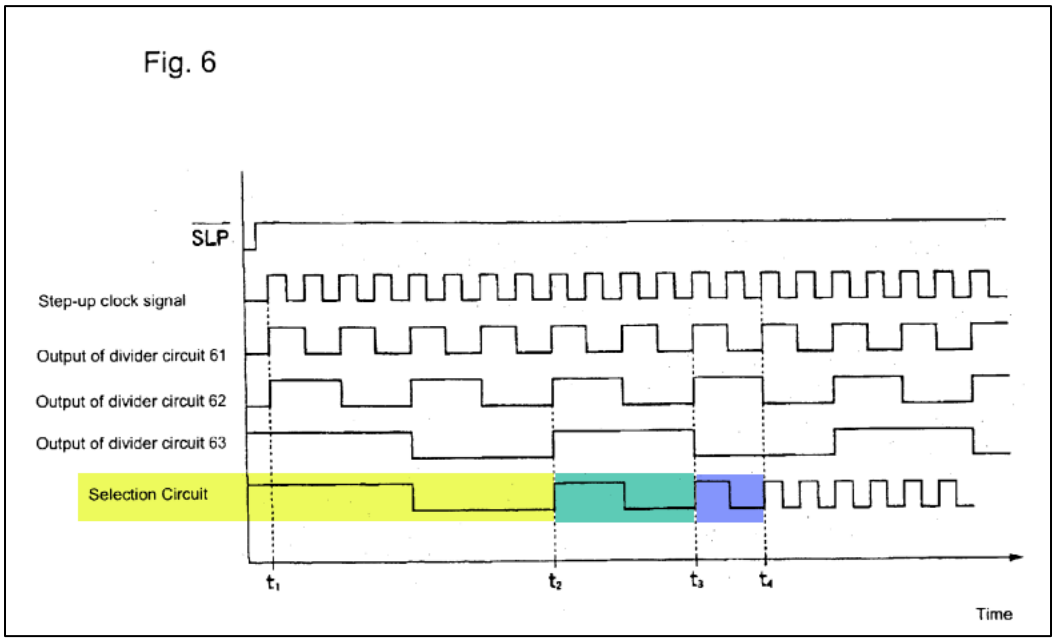
217. In my opinion, Ito discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § XII.B.(i) above.

(ii) 7[a]-[b]: ***a first charge pump circuit configured to generate a second voltage from a first voltage; and*** **7[b]:** ***a second charge pump circuit configured to generate a third voltage from the second voltage,***

218. In my opinion, Ito discloses claim limitations 7[a]-[b], as discussed in connection with claim limitations 3[a]-[b]. *See* § XII.C.(ii) above.

(iii) 7[c]: ***wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.***

219. In my opinion, Ito discloses claim limitation 7[c]. For example, Ito discloses that a length of a period in which the output of the **selector circuit 70** (the claimed "clock signal to be supplied to the second charge pump circuit") is in a high state is changed at times t2, t3, and t4, based on a two-bit control signal from counter 30, as shown in Figure 5 below.



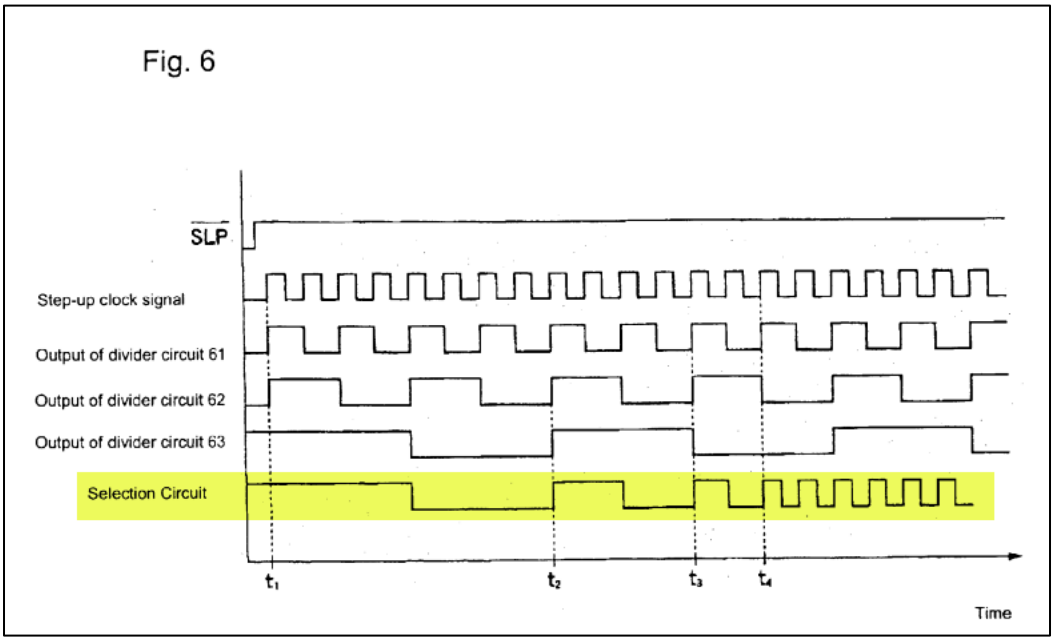
G. Claim 8

(i) 8[pre]: *The internal voltage generating circuit of claim 7,*

220. In my opinion, Ito discloses an internal voltage generating circuit, as discussed in 1[pre]. *See* § XII.B.(i) above.

(ii) 8[a]: *wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.*

221. In my opinion, Ito discloses claim limitation 8[a]. For example, Ito discloses that the length of a period in which the output clock signal of the **selector circuit 70** (the claimed "clock signal to be supplied to the second charge pump circuit") is in a high state is changed to a frequency of the divider circuit 61 at time t3, shown below. In my opinion, the frequency of divider circuit 61 is obtained by dividing the original frequency of the step-up clock signal, as shown below.



XIII. CONCLUSION

222. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Respectfully submitted,

Date: 26 August 2025 By: Carl Sechen
Carl Sechen, Ph.D.