Exhibit C-OB: Omnibus Obviousness Chart

The following chart demonstrates that asserted claims 1, 3, 4, 6, 7, and 8 of U.S. Patent No. 7,969,231 (the '231 patent") are obvious in view of the references discussed in Exhibits C-1 – C-X1 alone, or in combination with one or more of the following references (collectively the "Omnibus References"), consistent with the obviousness combinations and rationale set forth in the cover pleading hereto:

- Fujise
- Ito-177
- Kishimoto
- Hiiragizawa
- Abe
- Okasaka
- Oshikawa
- Dohi
- Sato
- Gebara
- Oku
- SK hynix Nova
- Nakayama
- Cernea
- Tanishima
- Morton
- Kumanoya
- Lee
- Kim
- Dinh
- Crippa
- Byeon
- Kato
- Kim
- Senda
- Hsiao
- Okuda
- Nakai
- Wu
- Jiang
- Saito
- Ito-633
- Shindo
- Anantha

As set out below, each limitation was well known in the art and would have been obvious to a person of ordinary skill in the art as it was part of the general knowledge of one of ordinary skill in the art, as shown by the teachings of at least one of the prior art references set forth above. A person of ordinary skill in the art would have been motivated to combine any of these references with at least one or more of the foregoing prior art references for at least the reasons set forth in the cover document of SK hynix's invalidity contentions and/or as further set out in Exhibits C-1 – C-X1.

This chart incorporates by reference—for each respective claim and claim limitation of the '231 patent—the exemplary prior art disclosures identified in SK hynix's charts Exhibits C-1 through C-X1. Those disclosures are each incorporated into this chart in this Exhibit C-OB as if fully set forth, but which for brevity are not repeated verbatim below. This chart therefore sets out the additional disclosures from the remaining references described above which, together with such other references incorporated or noted in this chart, render obvious each and every claim limitation of the '231 patent, to the extent such limitation(s) are not anticipated.

The analysis in this chart is based on the apparent claim constructions and interpretations that AMT has advanced to allege infringement of the asserted claims of the '231 patent, as set forth in AMT's infringement contentions served April 2, 2025. Nothing in this chart should be interpreted as SK hynix conceding that AMT's apparent claim constructions and interpretations are correct or supported by intrinsic or extrinsic evidence.

The analysis in this chart is preliminary, and SK hynix's investigation into the invalidity of the asserted claims of the '231 patent is ongoing. SK hynix reserves the right to provide additional theories under which the cited prior art anticipates or renders obvious the asserted claims of the '231 Patent, including in response to the receipt of third party discovery currently ongoing and to be produced in this litigation. The citations to specific disclosure of the prior art references in this chart are exemplary, and SK hynix reserves the right to rely on additional disclosures to the same references. SK hynix also reserves the right to offer expert testimony and opinions explaining how a person of skill in the art would understand the disclosures of the cited prior art references.

Exemplary Disclosures
1[a] An internal voltage generating circuit comprising:
To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious an internal voltage generating circuit . *See, e.g.*: Cernea at Abstract: A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases,

respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

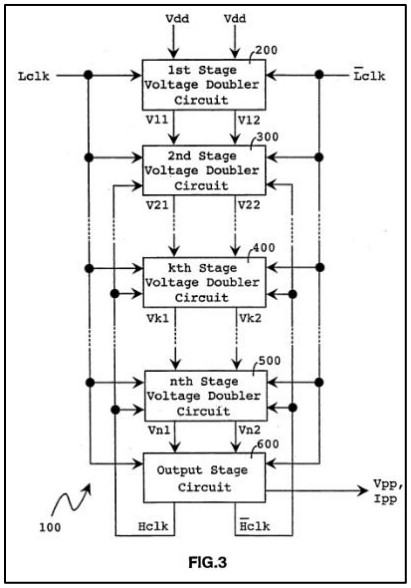


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second

phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

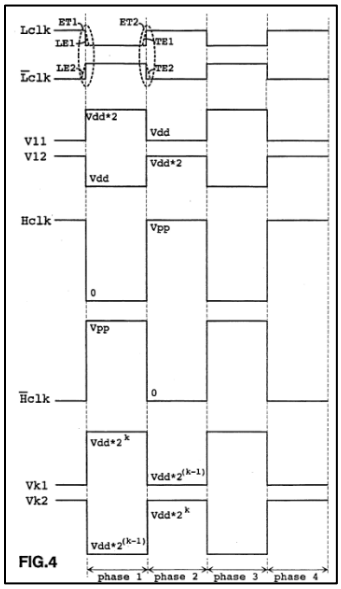


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter

(ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be

applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

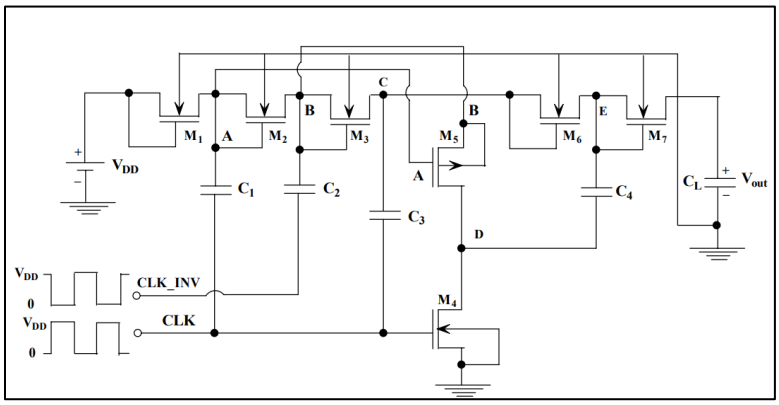
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 μs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 μs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

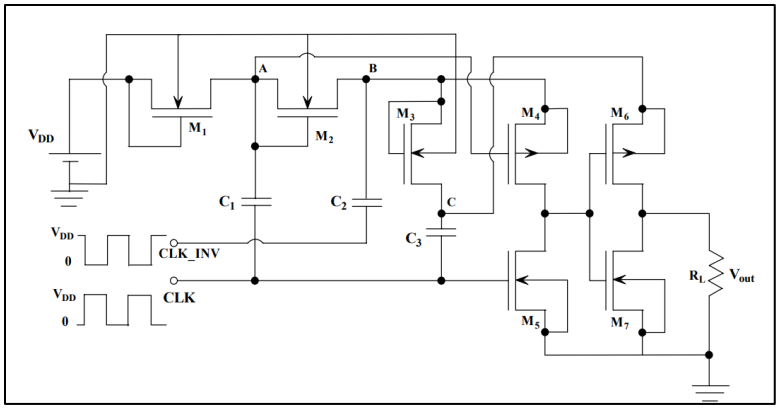
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

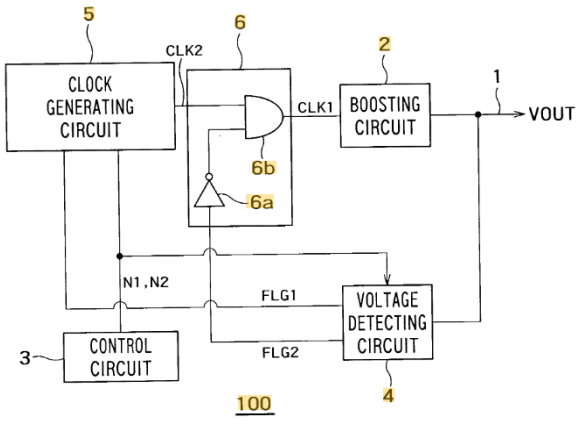


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating

circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

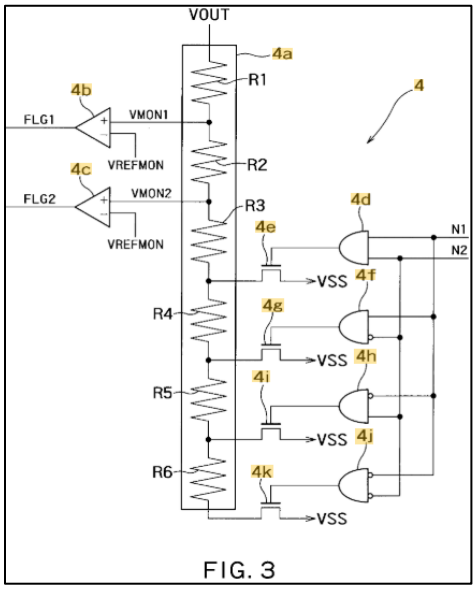


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5

includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

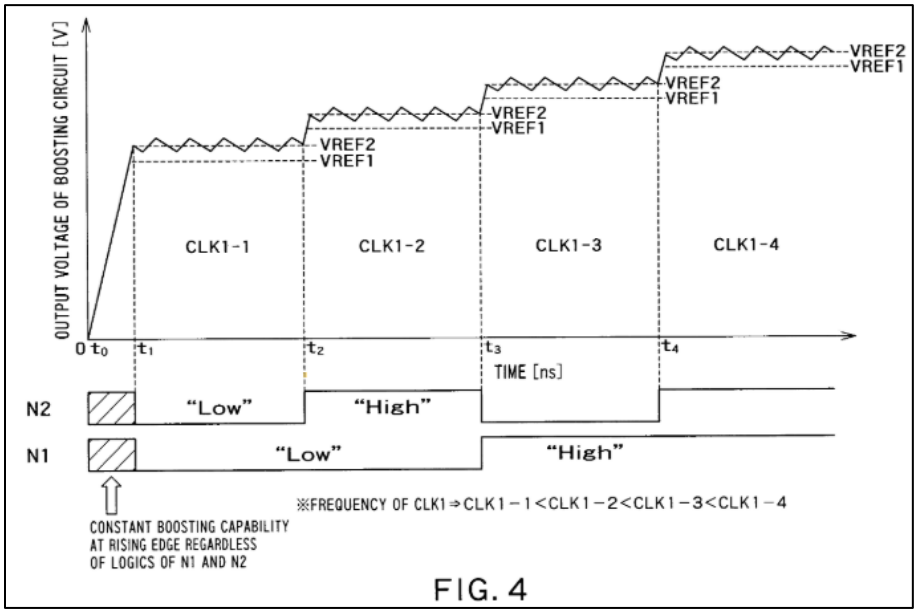


FIG. 4

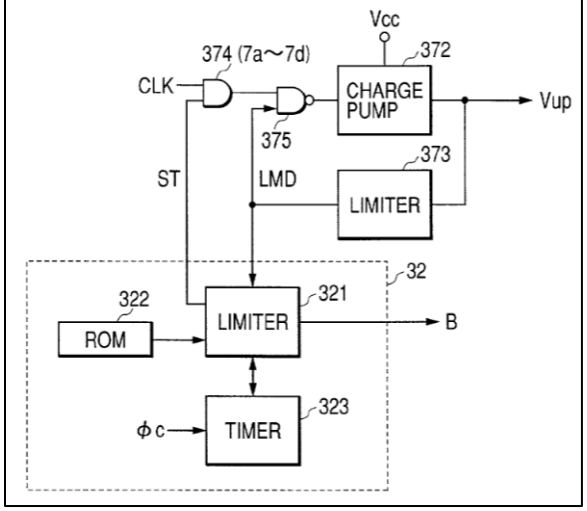
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4

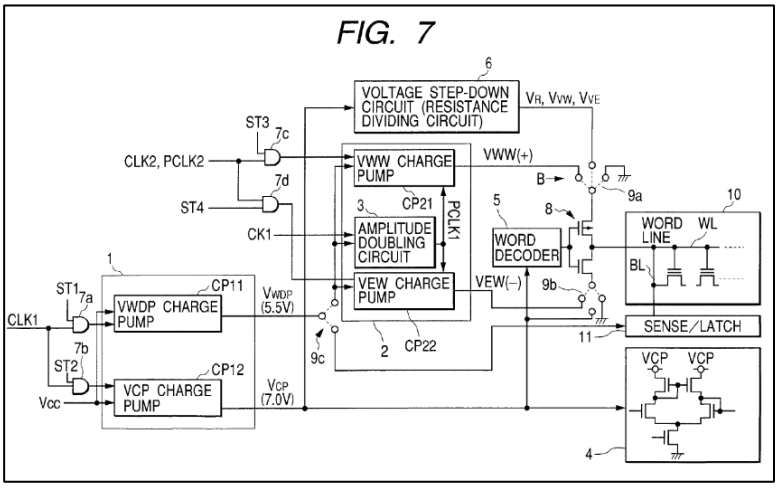


Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory

having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted,

the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2 goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

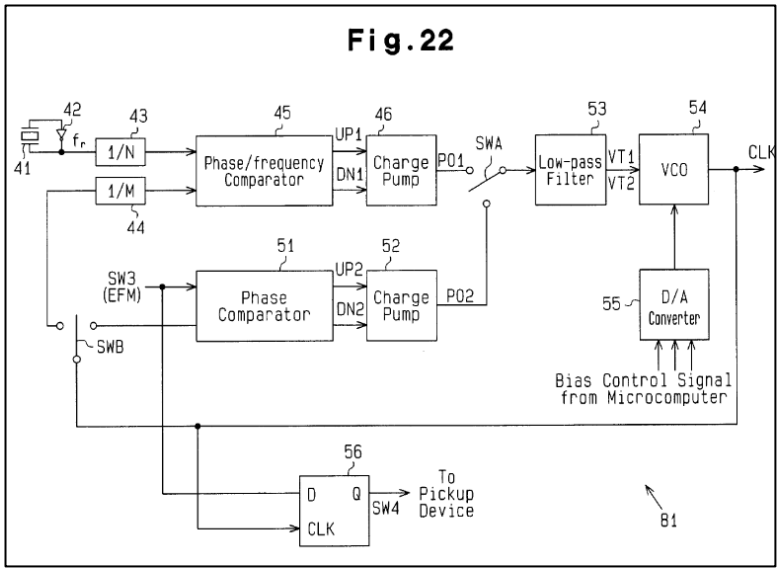
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

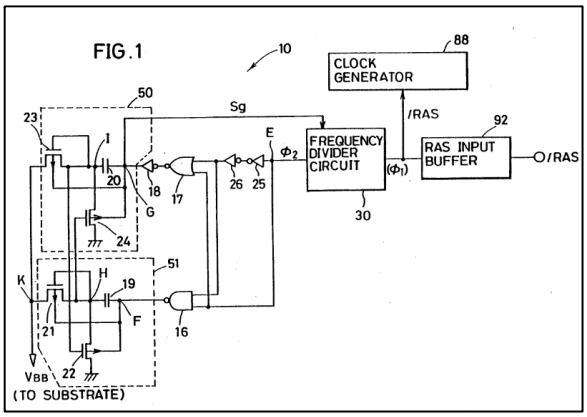


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

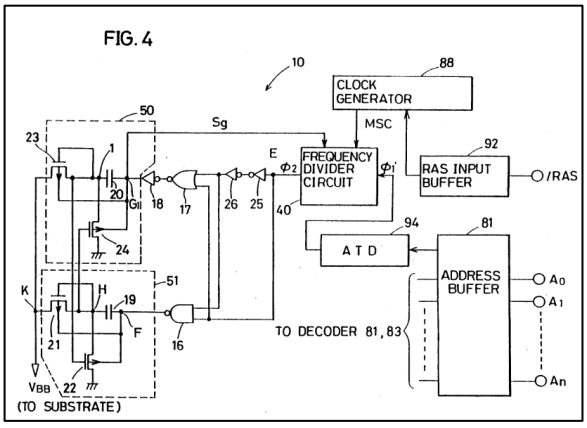
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

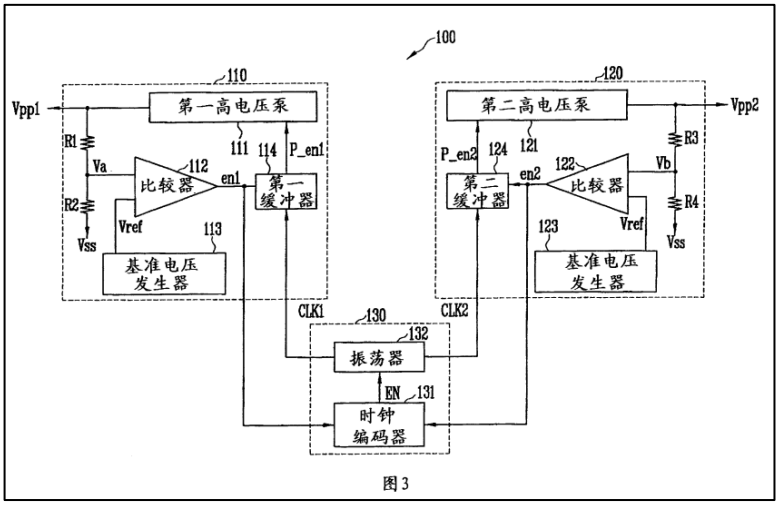


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

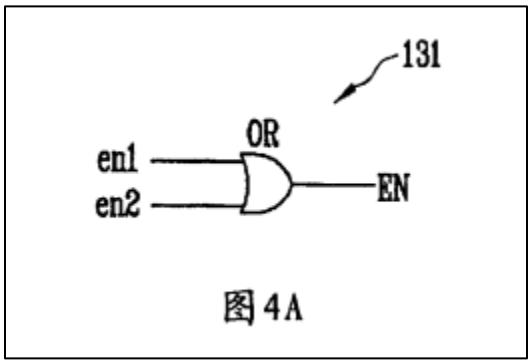


图 4A

Jiang at Fig. 6:

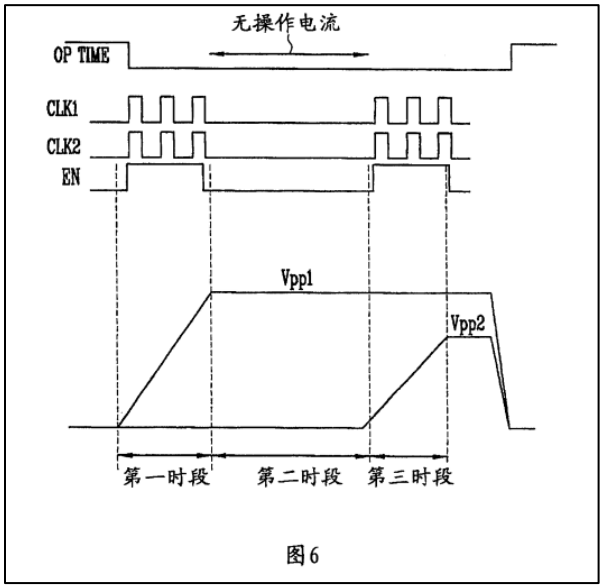
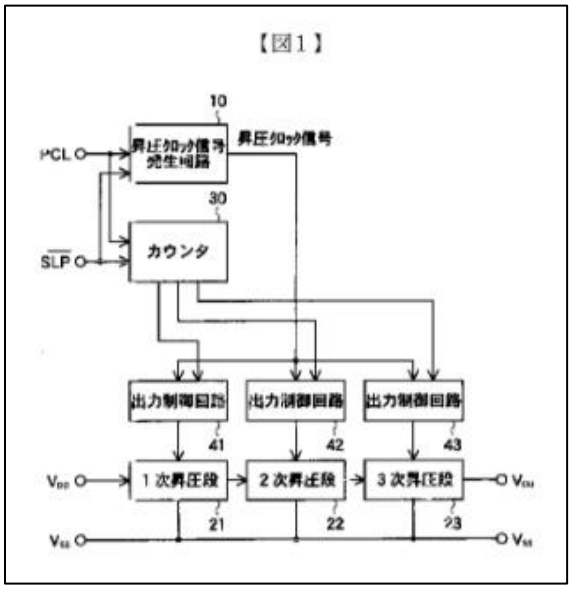


图6

Ito-633 at [0018] and Fig. 1:

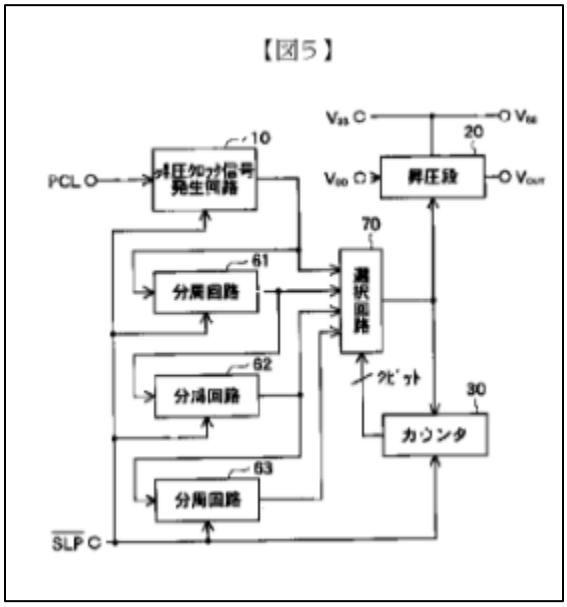
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as “boost clock signal”) based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

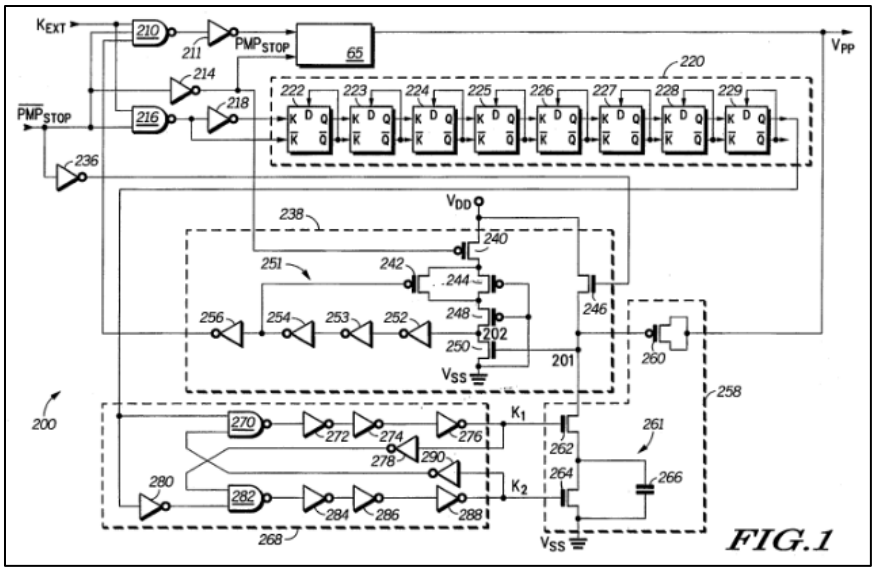


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

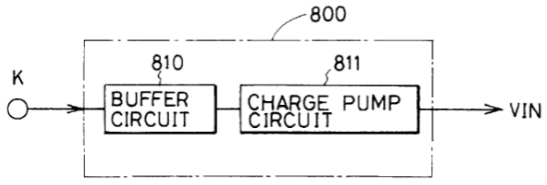


FIG.57

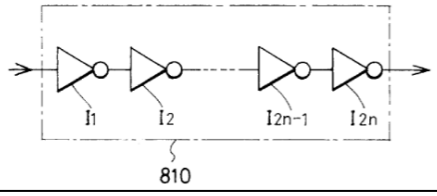


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

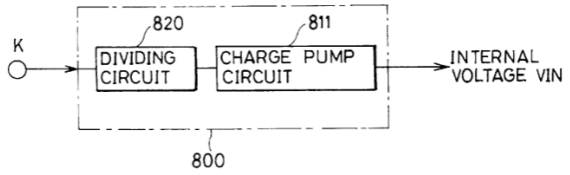
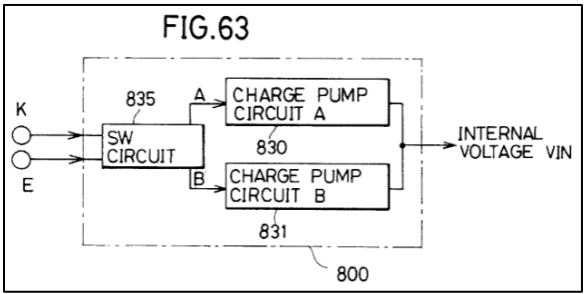


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



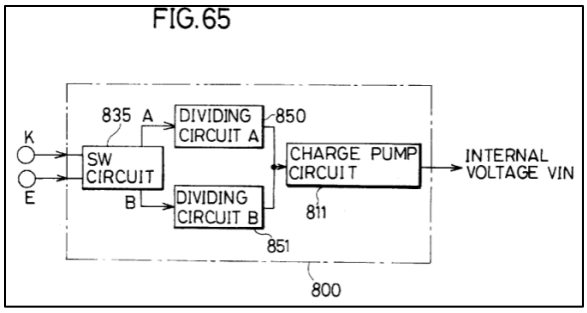
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

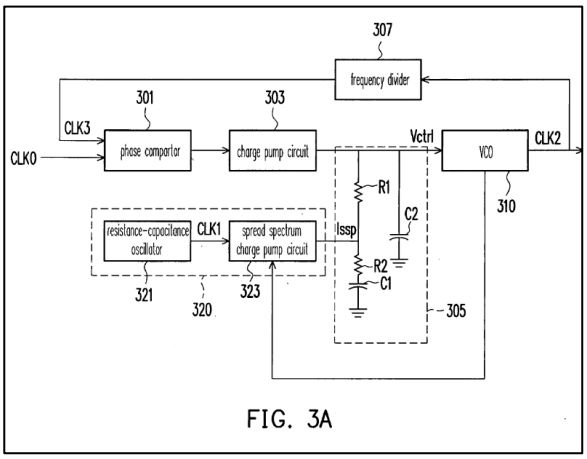


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

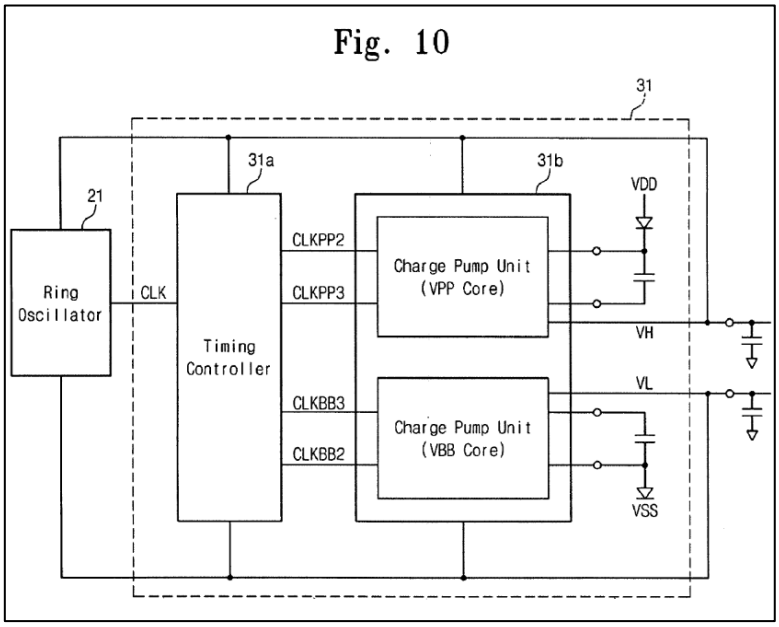


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

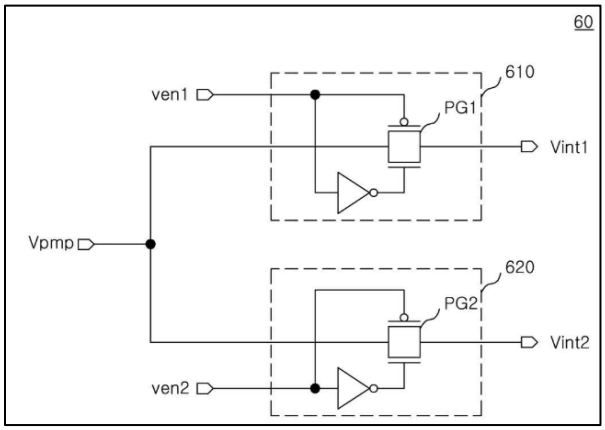
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

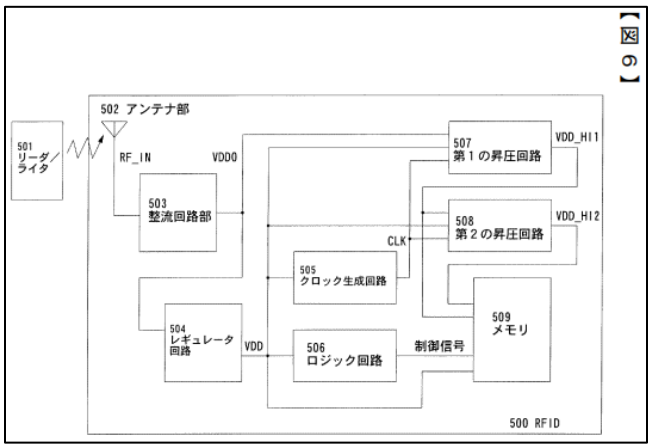
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

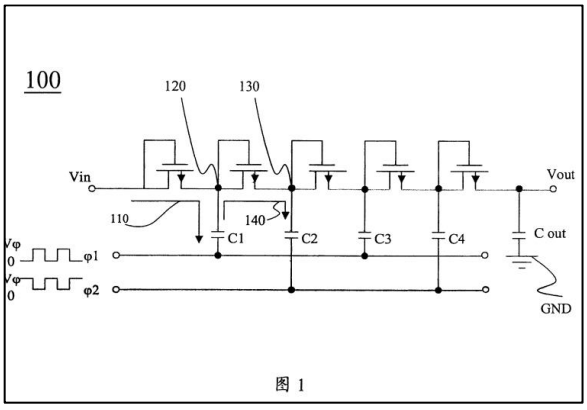
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

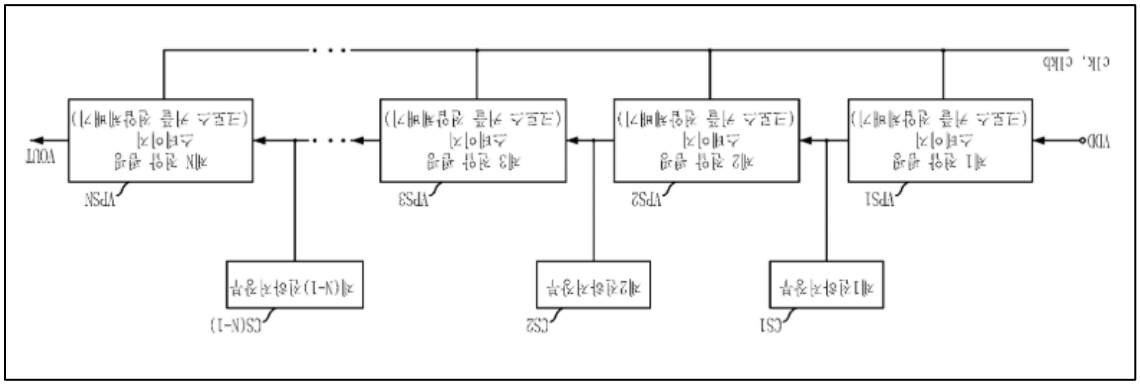
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

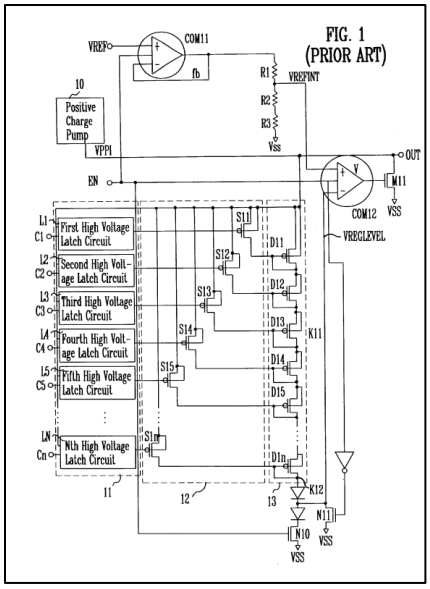
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



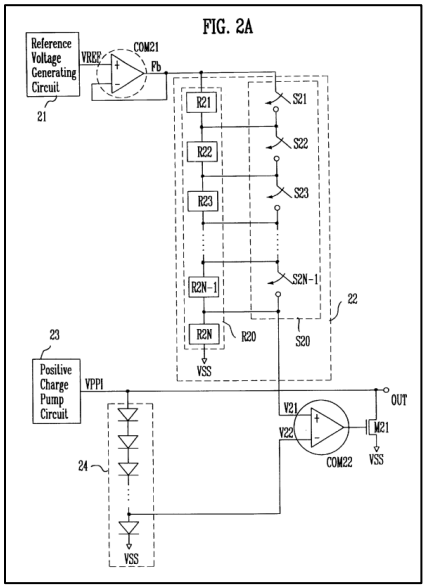
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

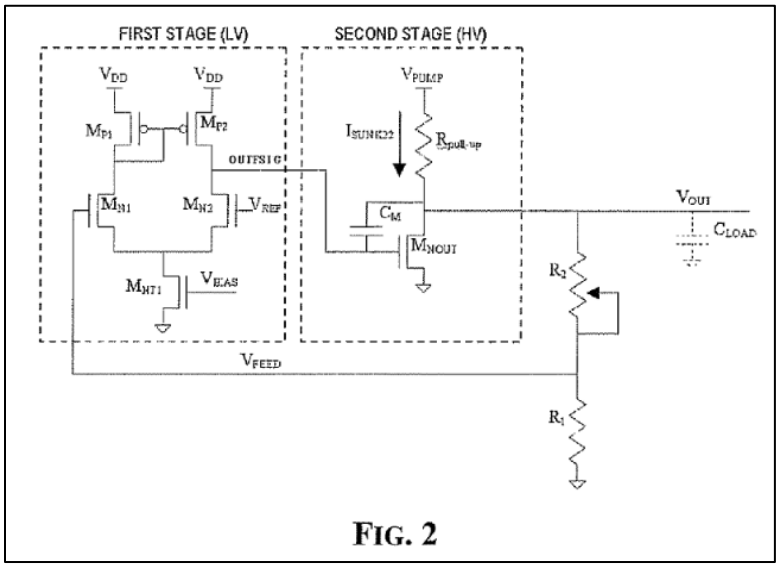


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

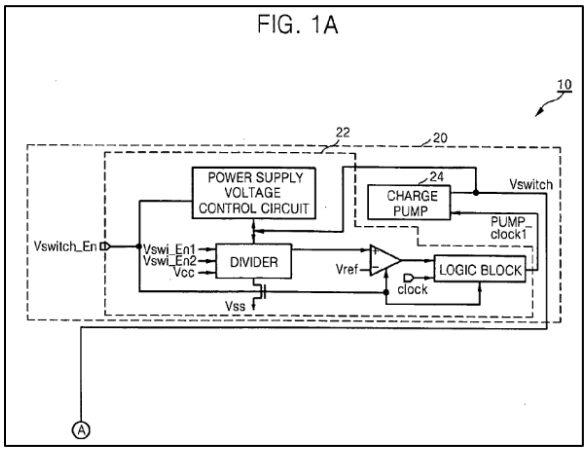
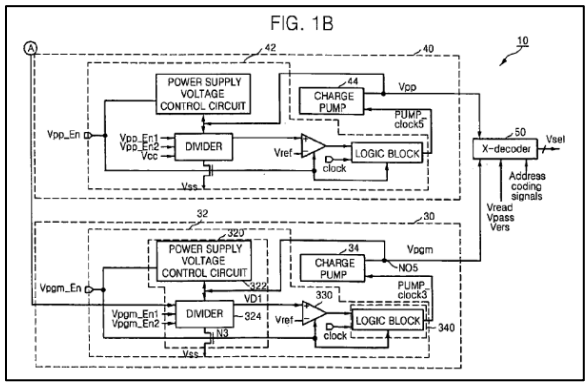
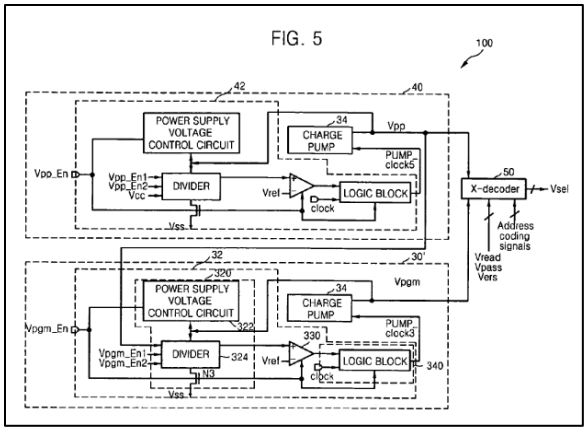


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

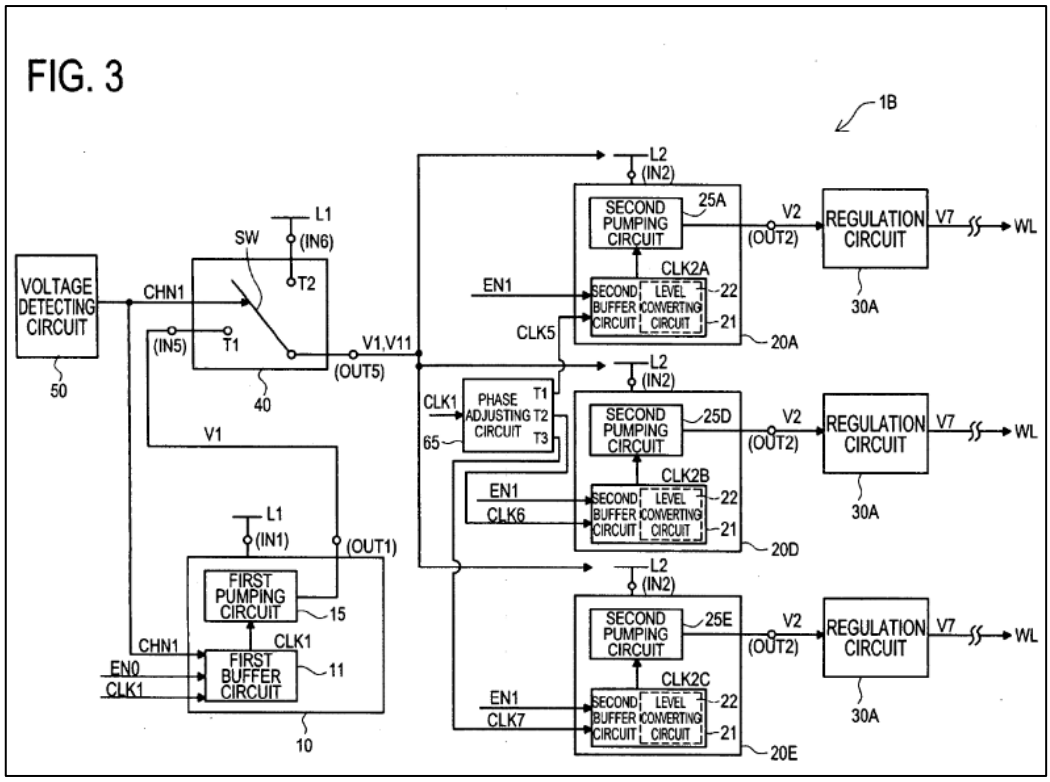
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

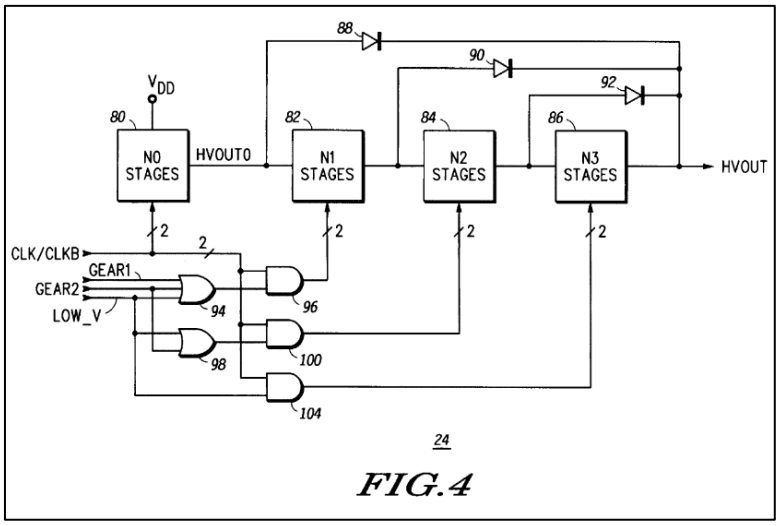


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

1[b] a first boost circuit provided between a first voltage and a first terminal;

The Omnibus References disclose and/or render obvious a first boost circuit provided between a

first voltage and a first terminal.

See, e.g.:

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

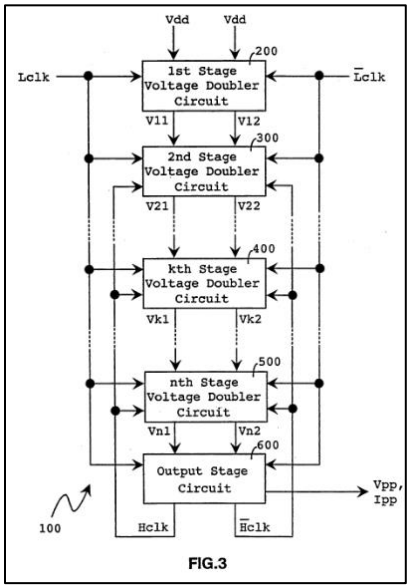


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal

to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

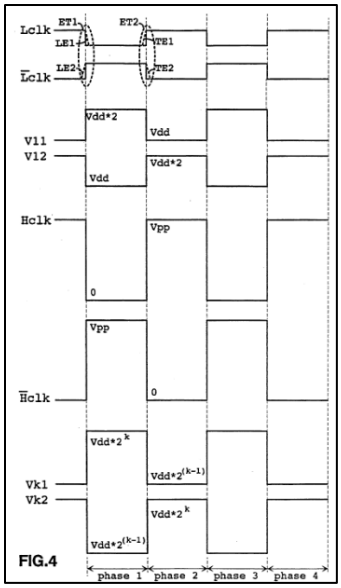


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

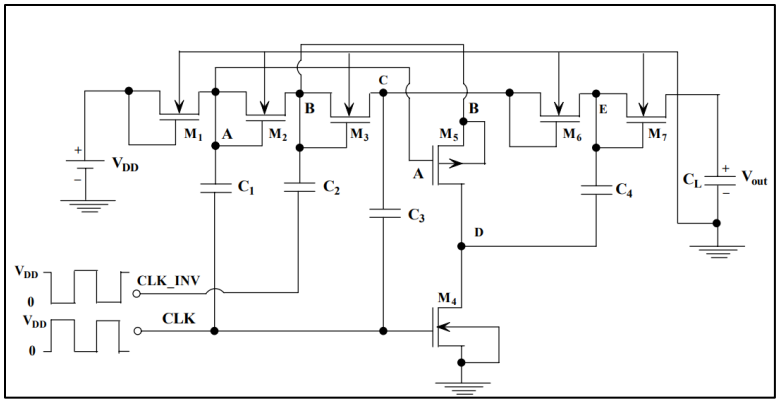
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

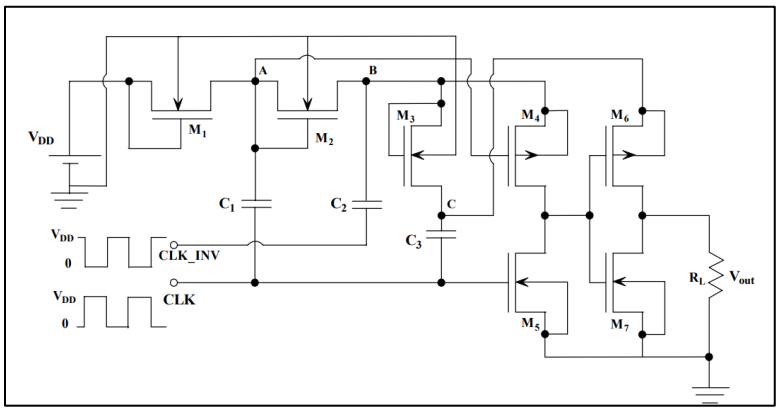
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

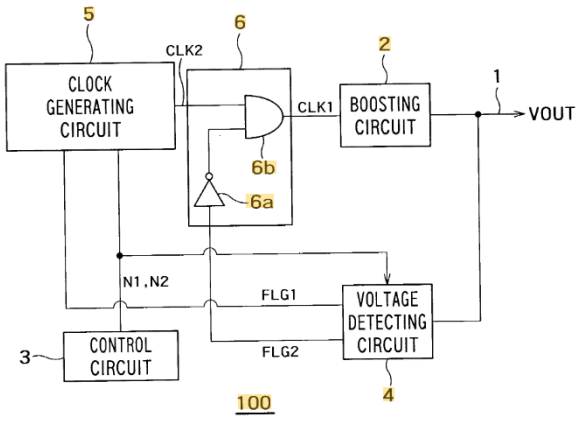


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

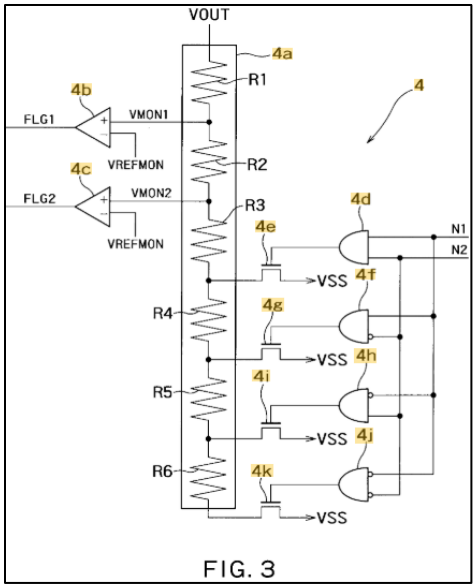


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

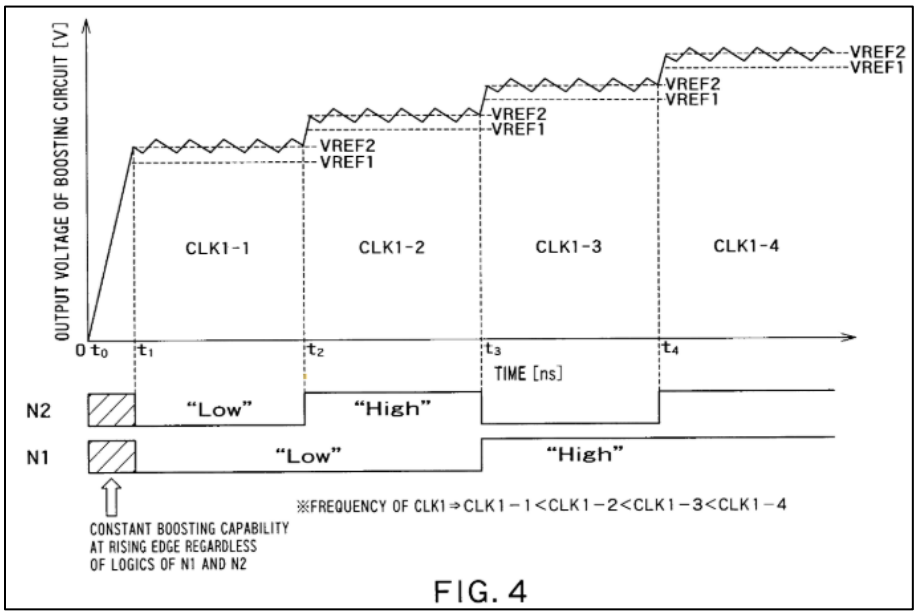


FIG. 4

Sato at [0051]:

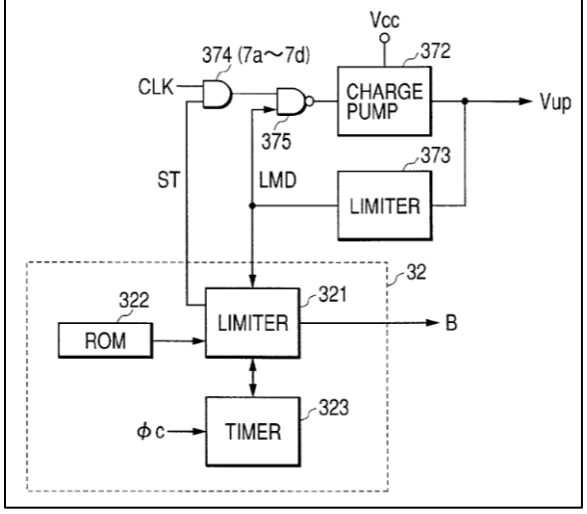
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

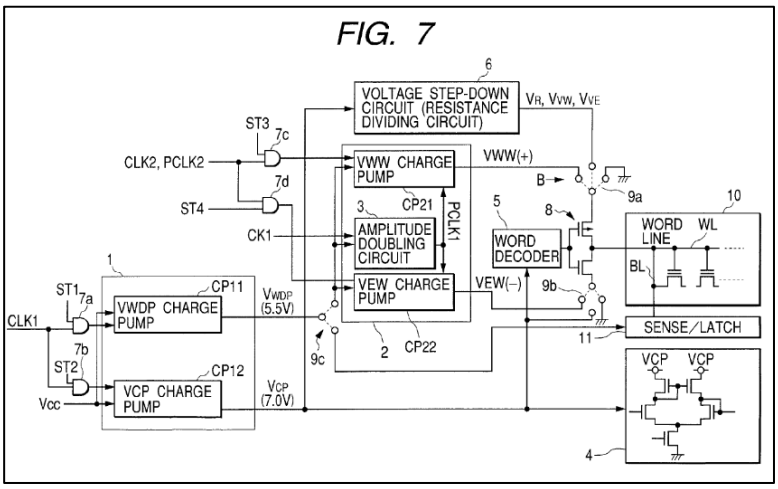
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

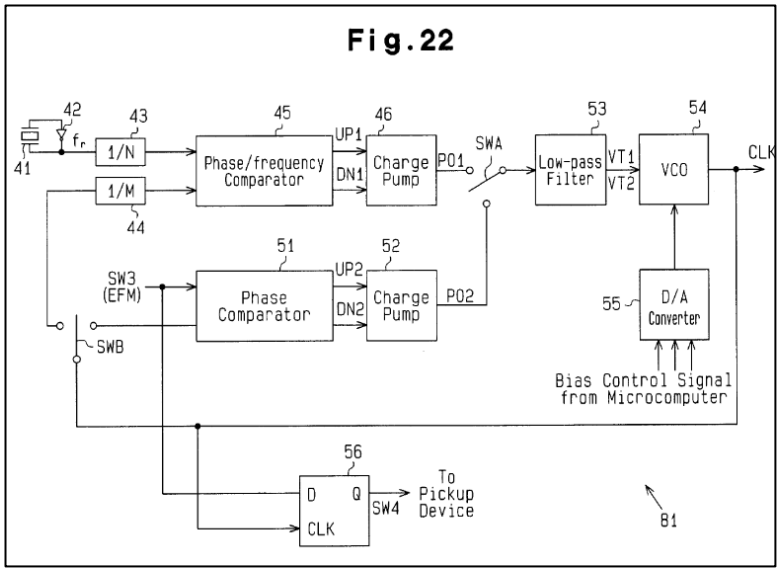
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

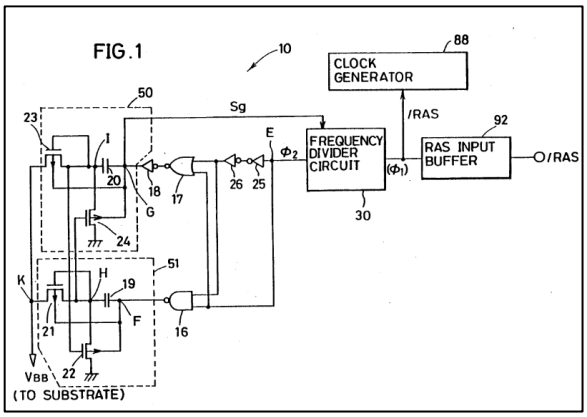


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

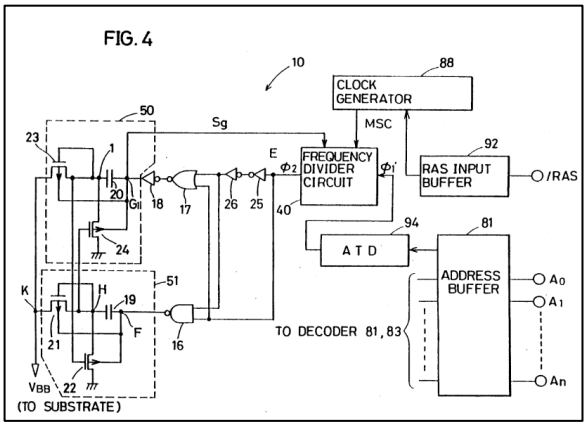
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

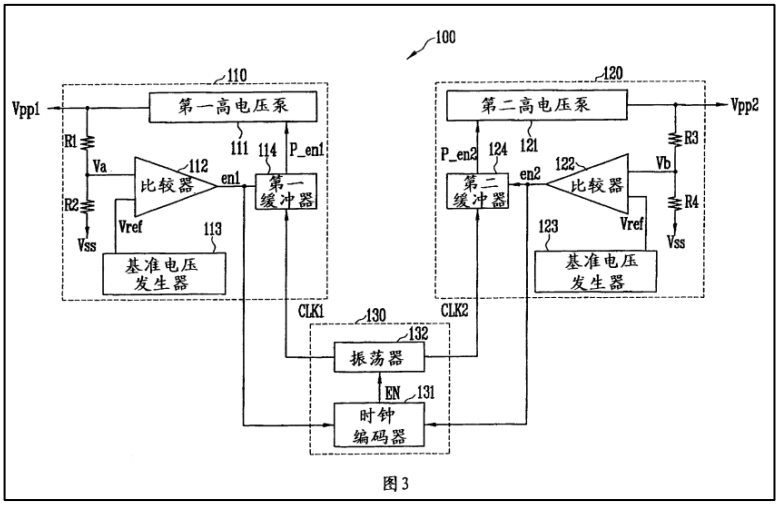


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

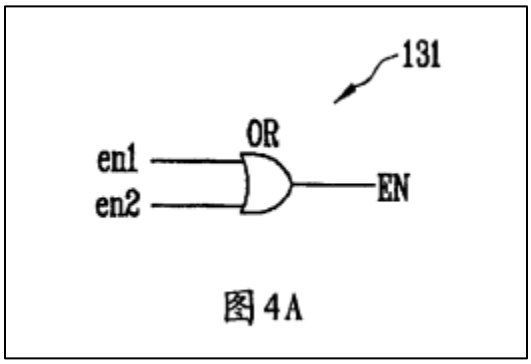


图 4A

Jiang at Fig. 6:

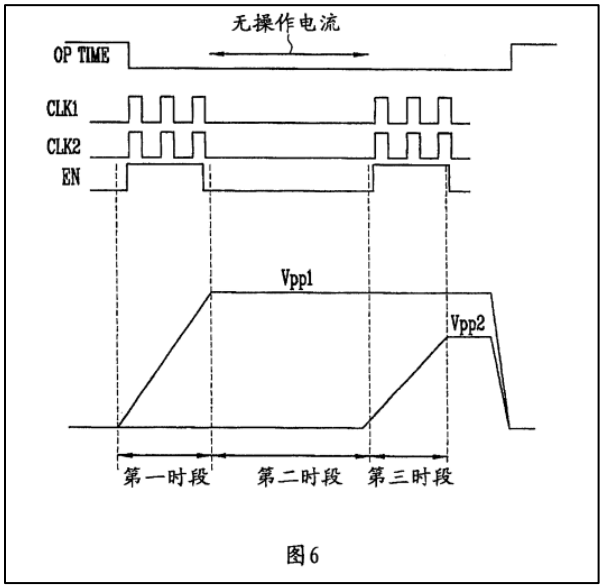
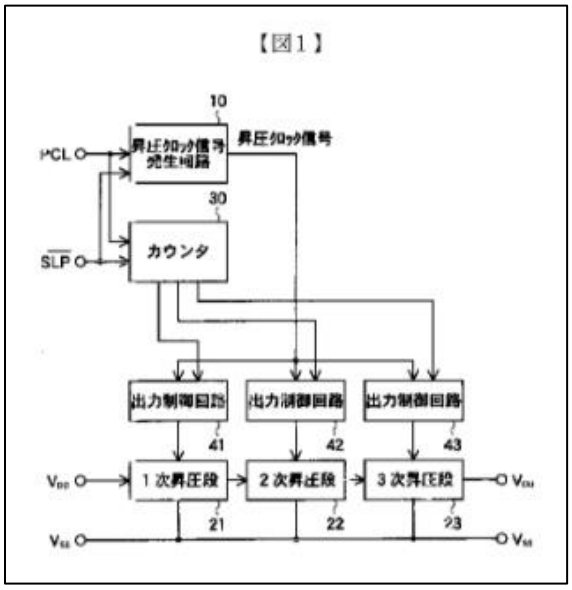


图 6

Ito-633 at [0018] and Fig. 1:

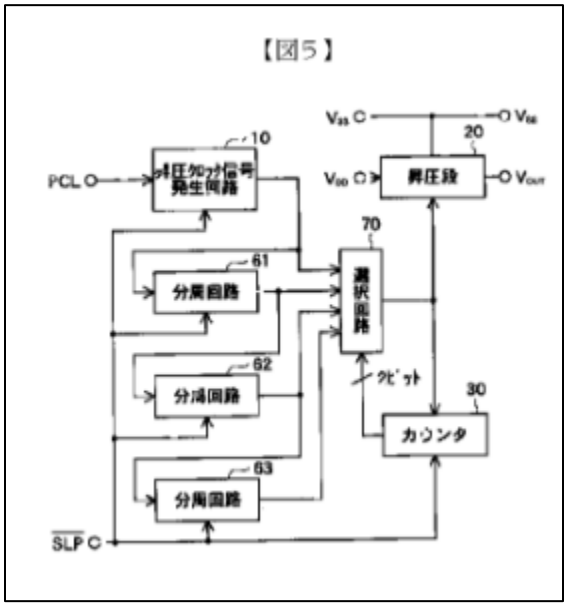
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

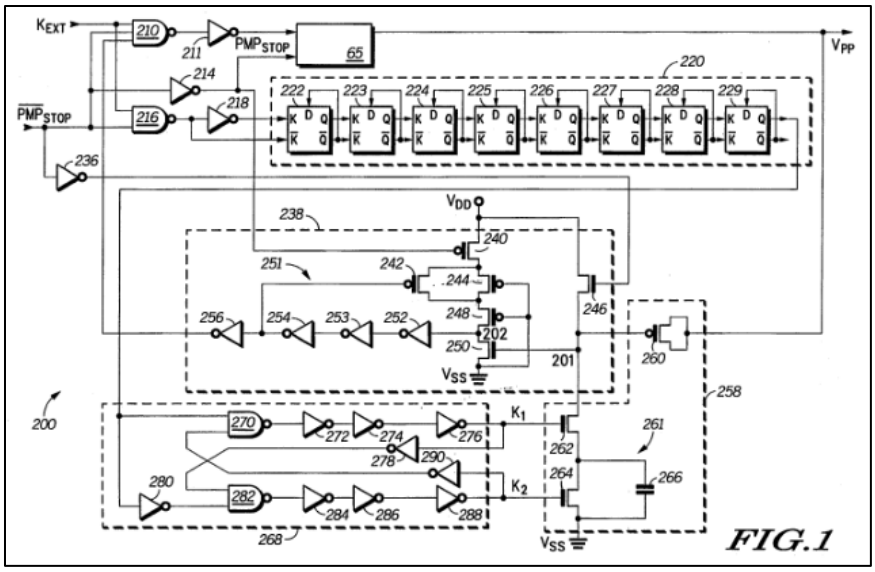


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

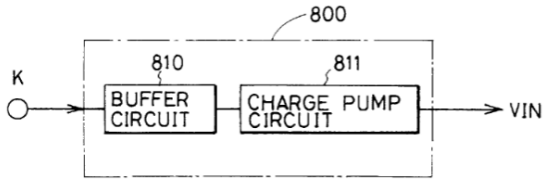


FIG.57

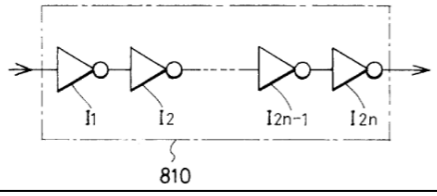
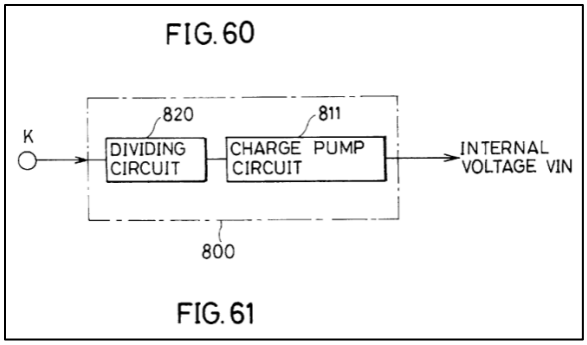


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

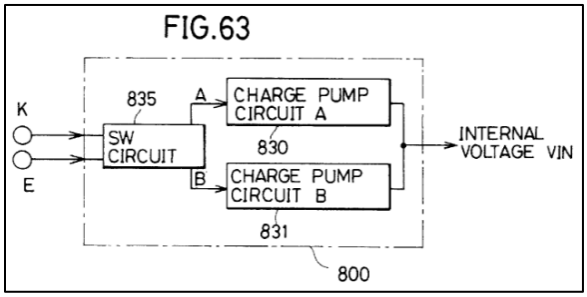
Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.



Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.



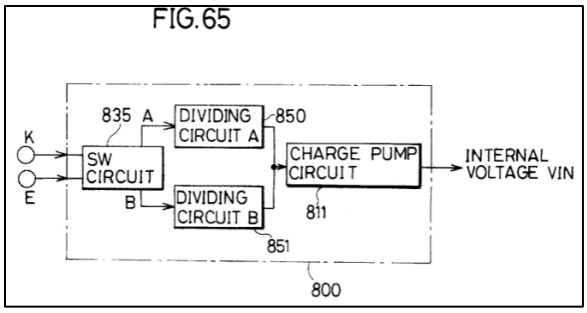
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

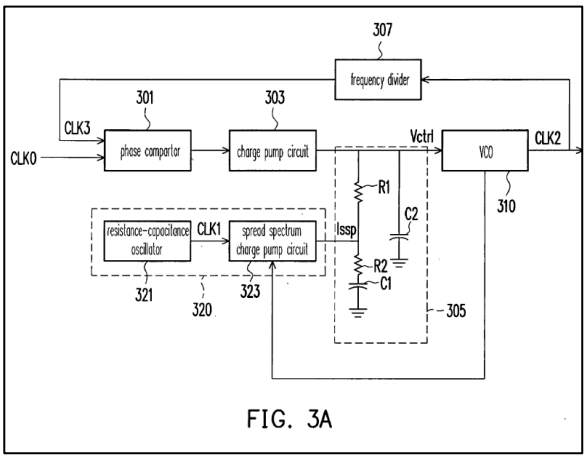


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

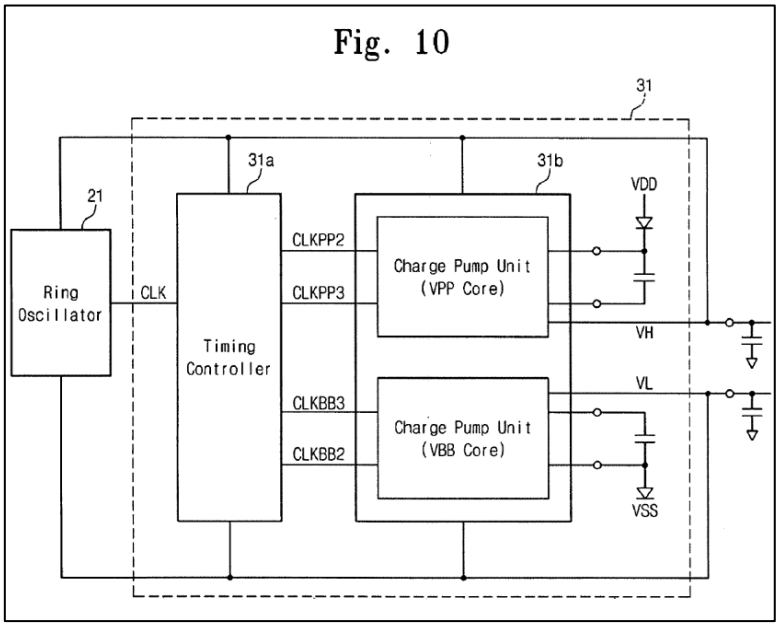


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

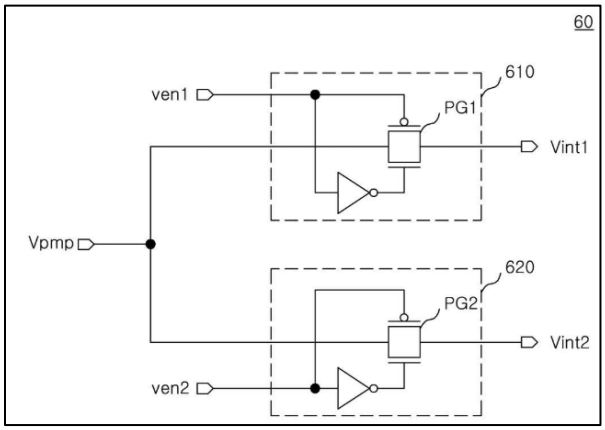
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

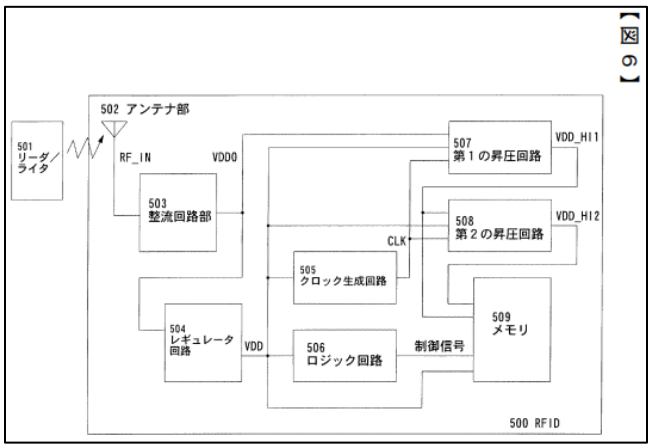
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

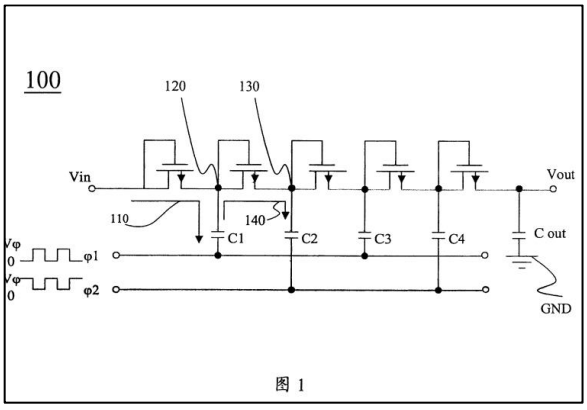
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

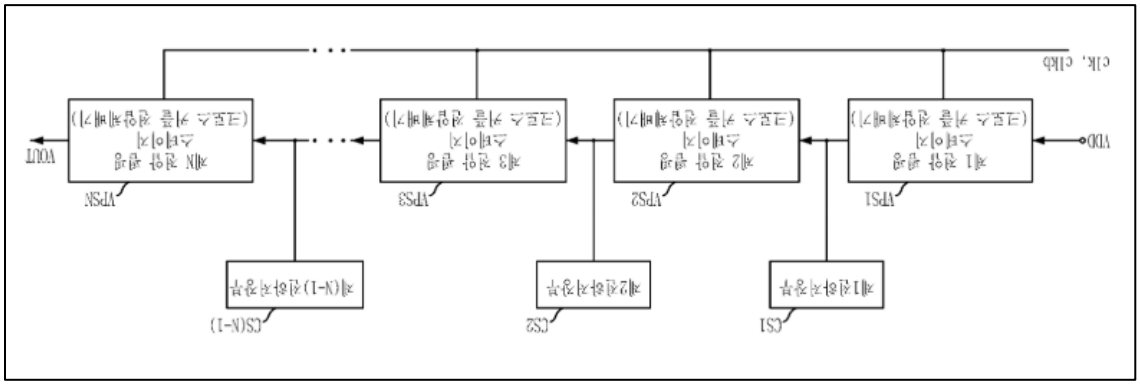
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

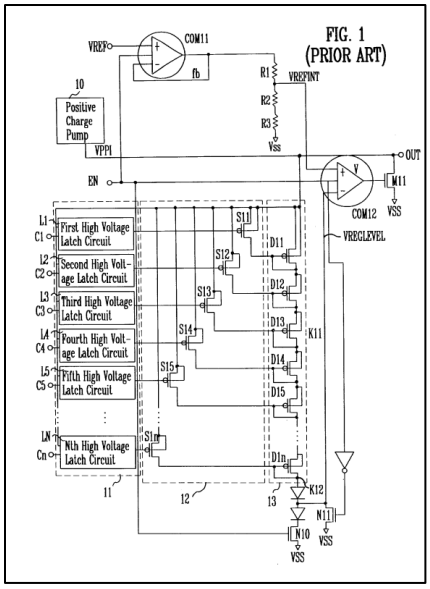
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



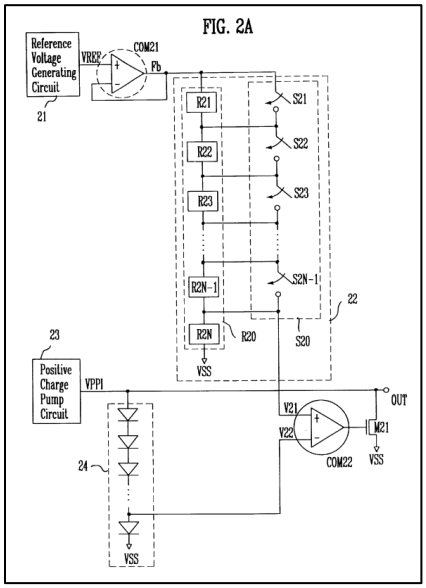
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

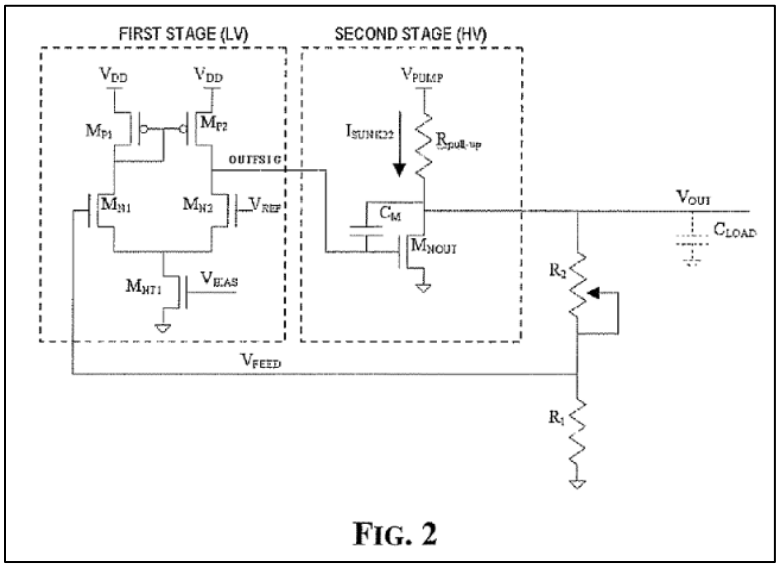


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

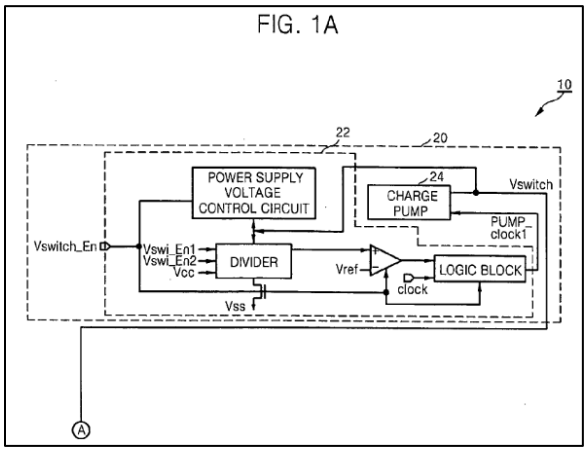
Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

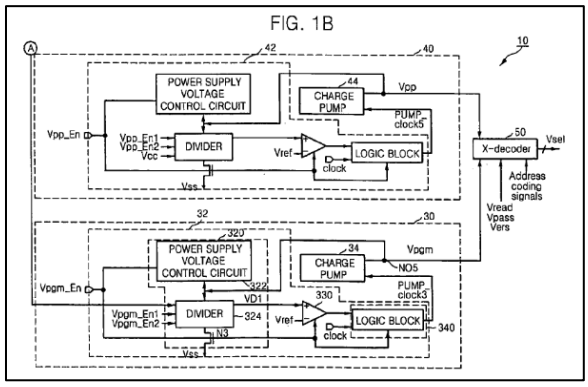
FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

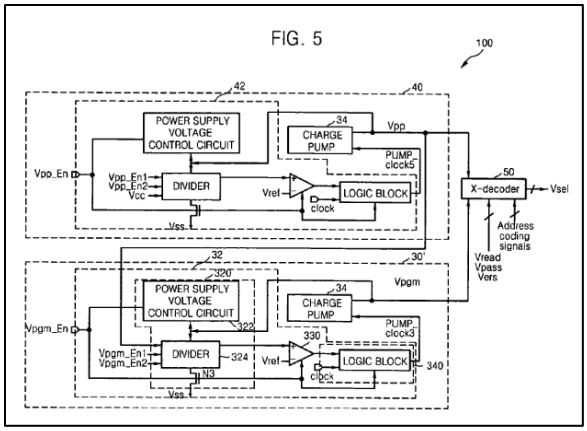
The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.





Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

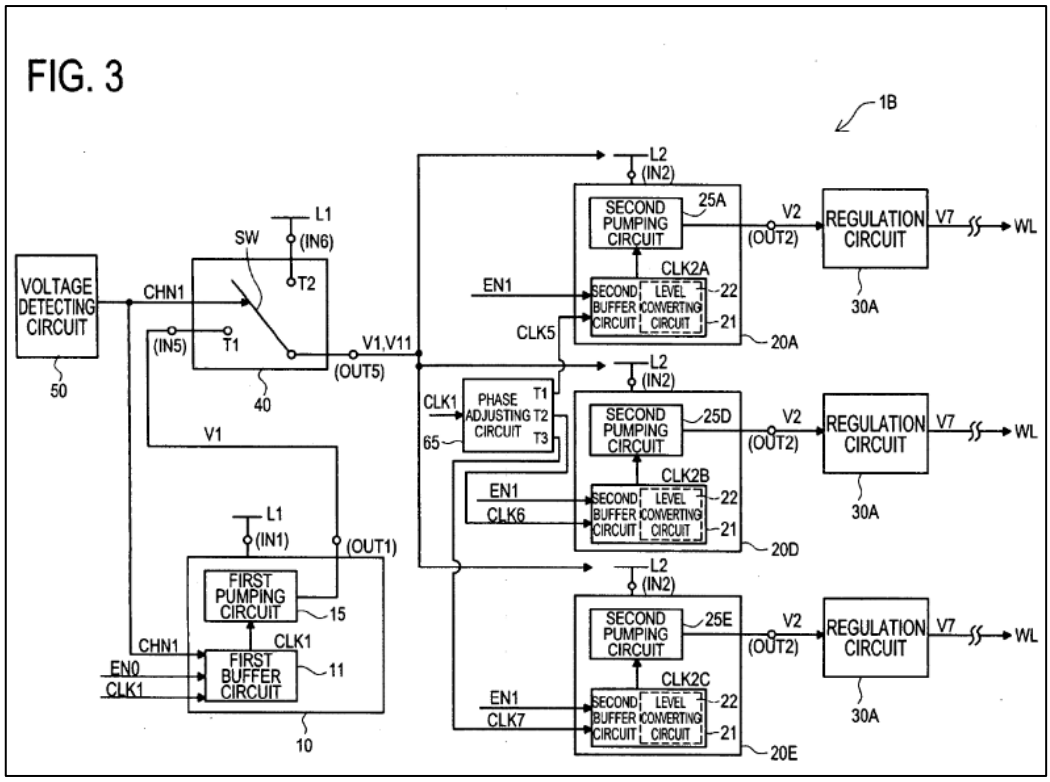
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

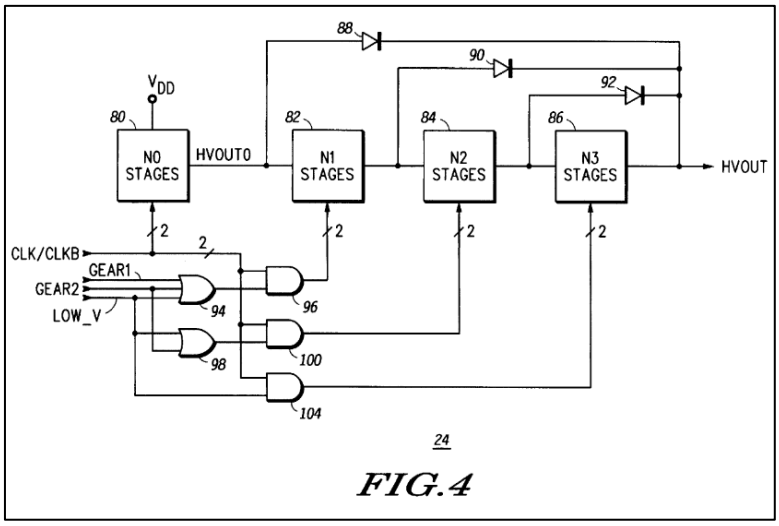


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

1[c] a second boost circuit provided between the first terminal and a second terminal;

The Omnibus References disclose and/or render obvious a second boost circuit provided between

the first terminal and a second terminal.

See, e.g.:

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

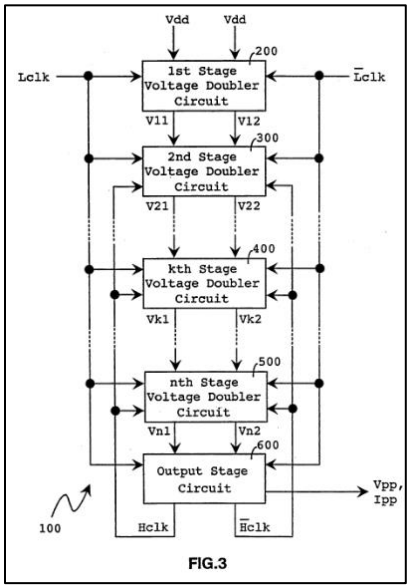


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal

to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

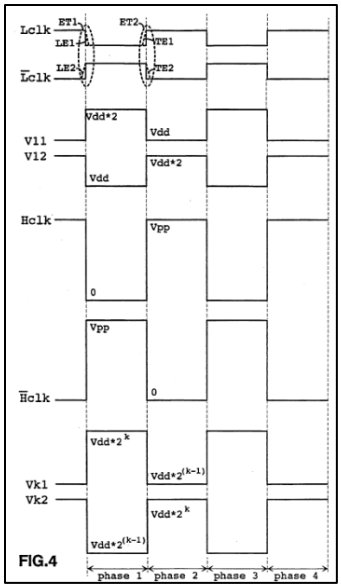


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

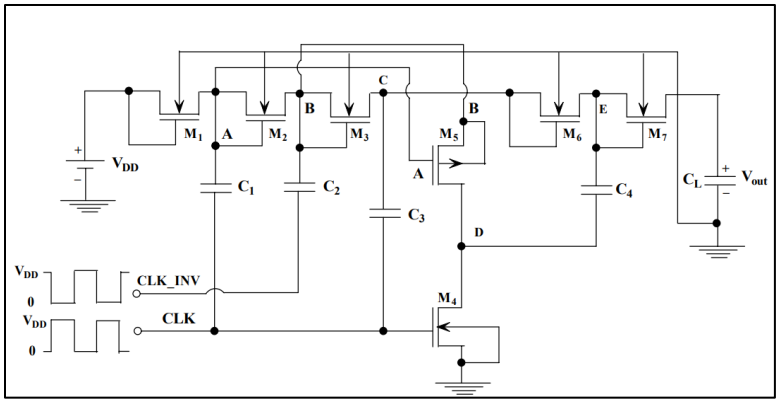
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

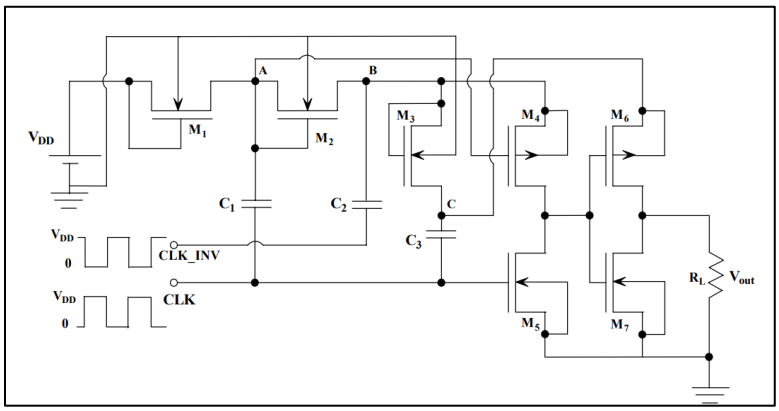
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

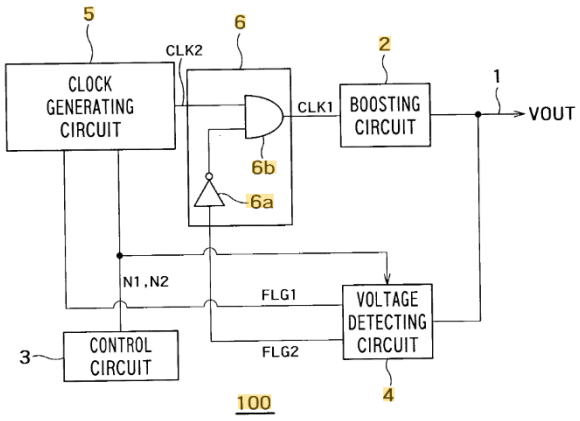


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

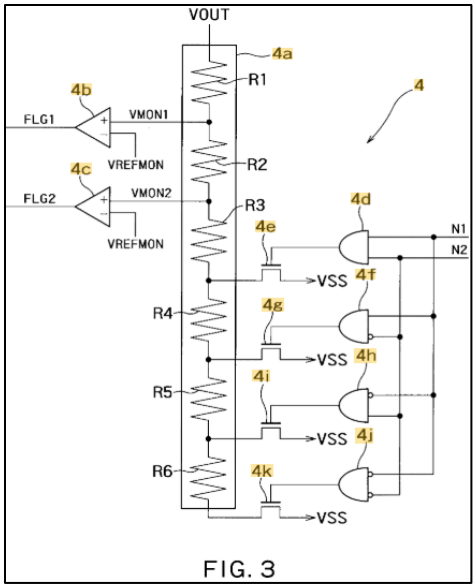


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

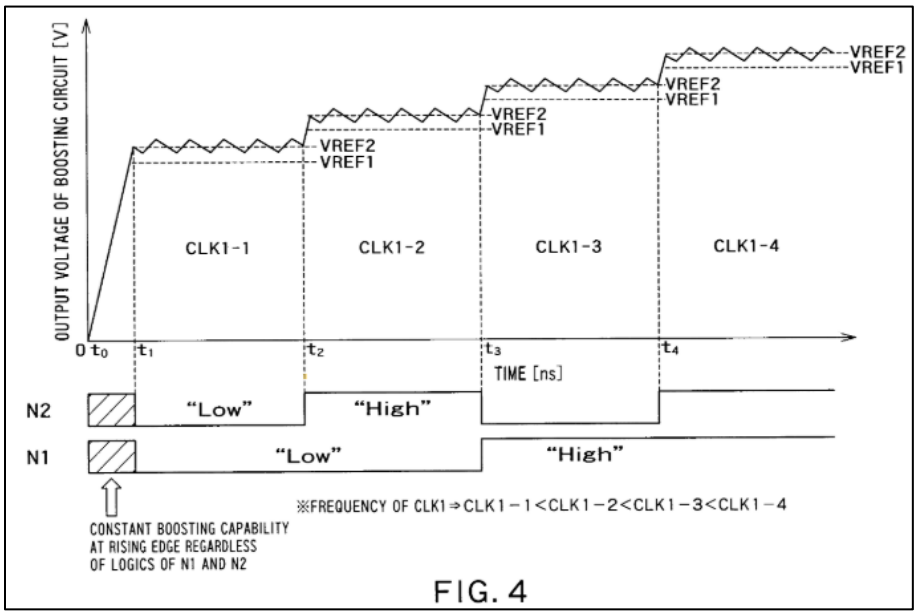


FIG. 4

Sato at [0051]:

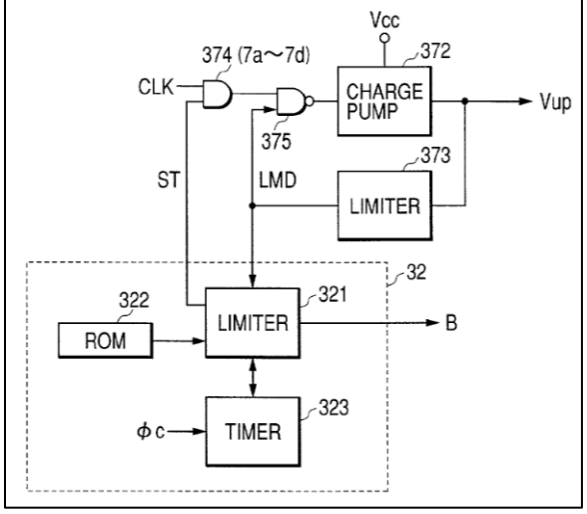
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

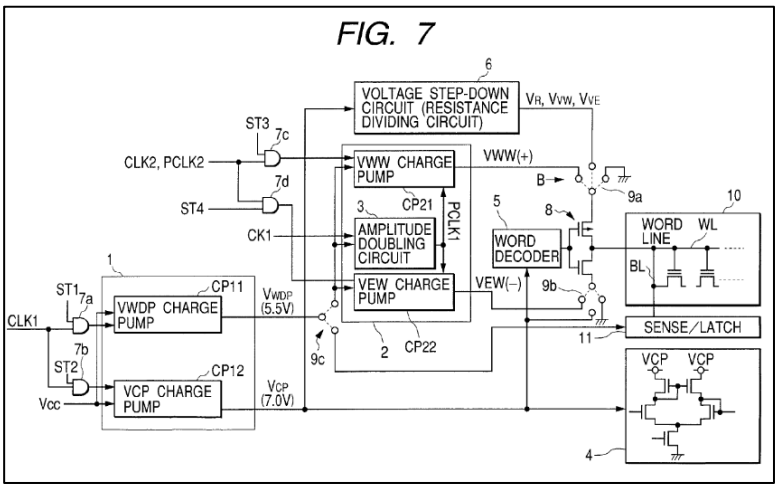
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

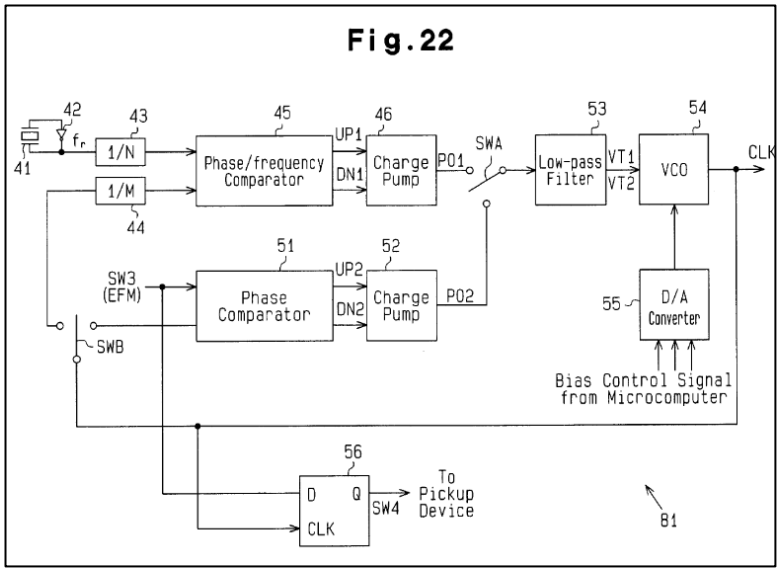
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

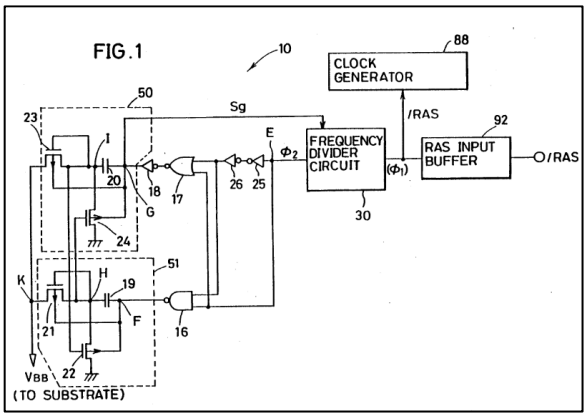


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

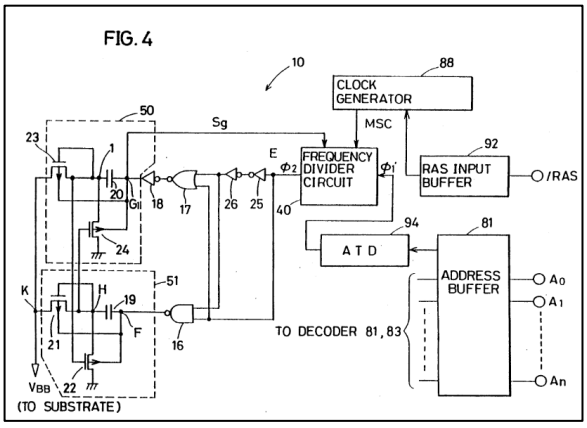
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

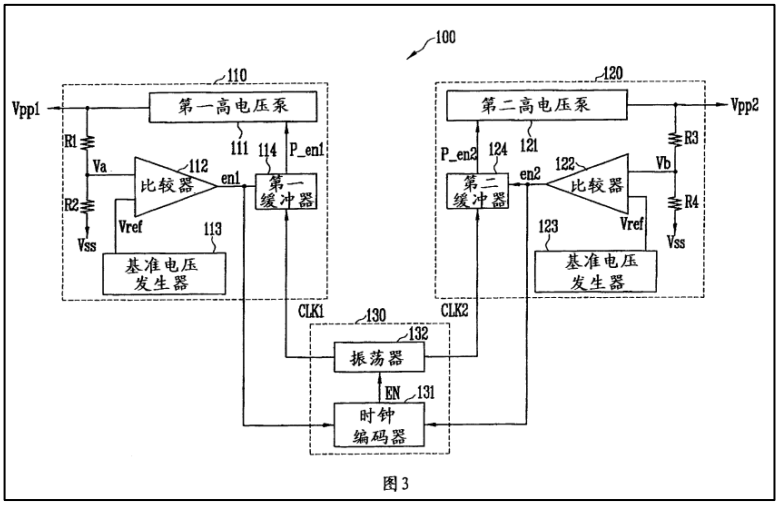


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

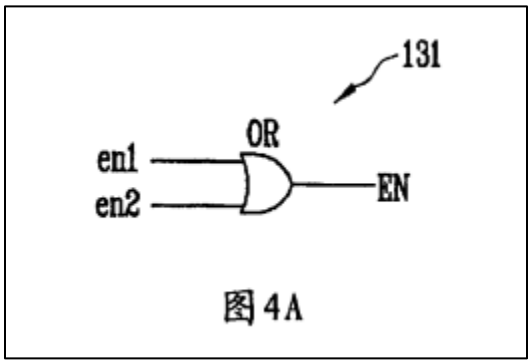


图 4A

Jiang at Fig. 6:

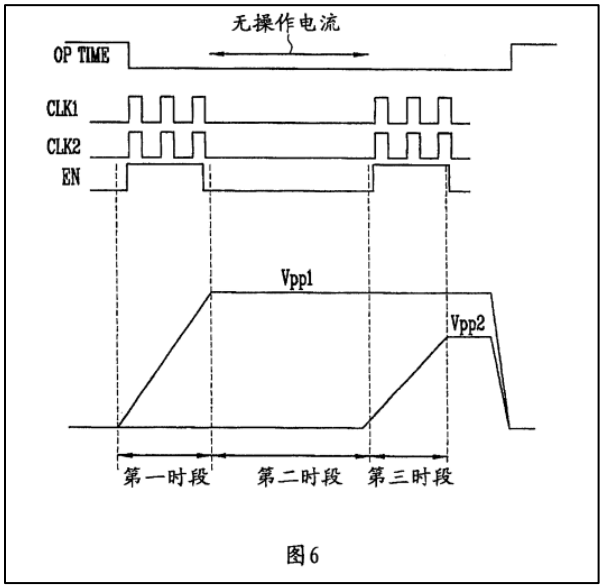
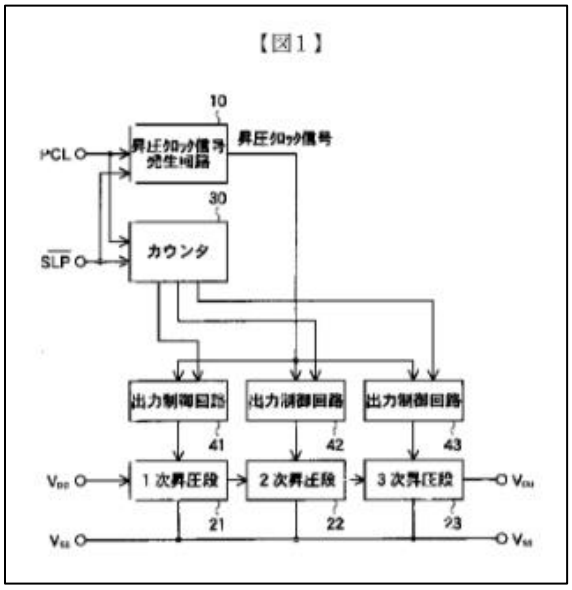


图6

Ito-633 at [0018] and Fig. 1:

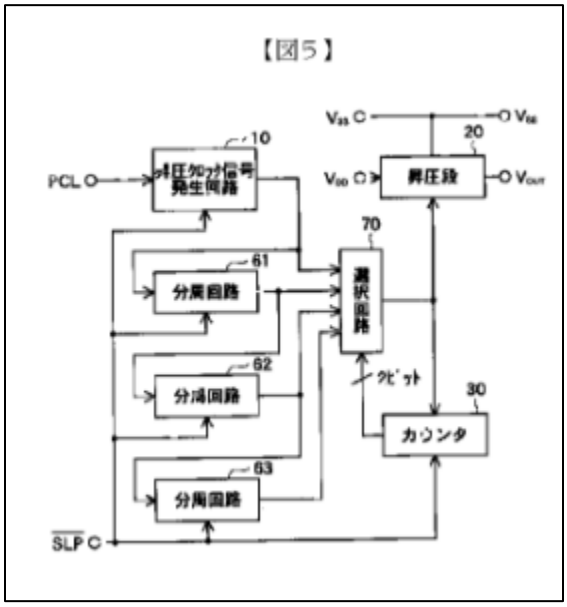
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

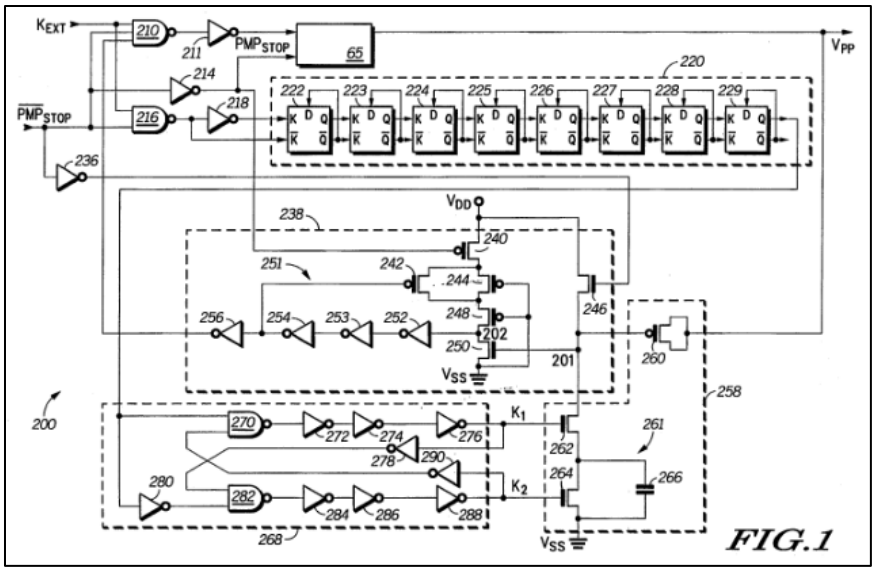


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

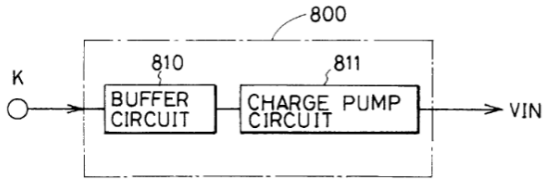


FIG.57

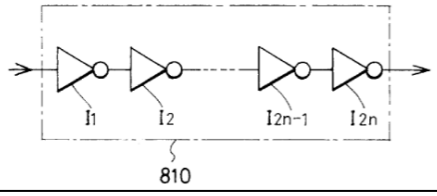


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

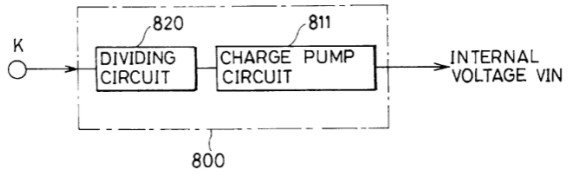
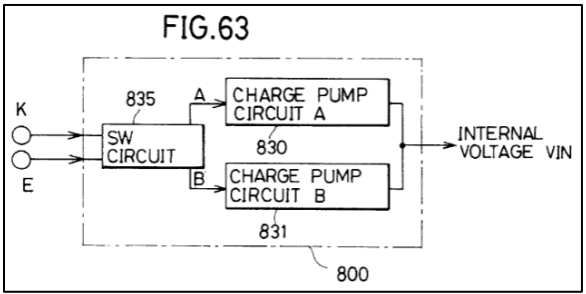


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



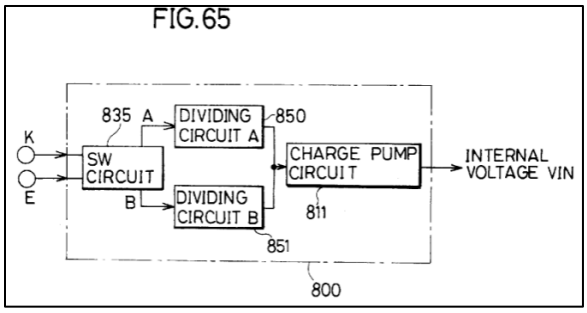
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

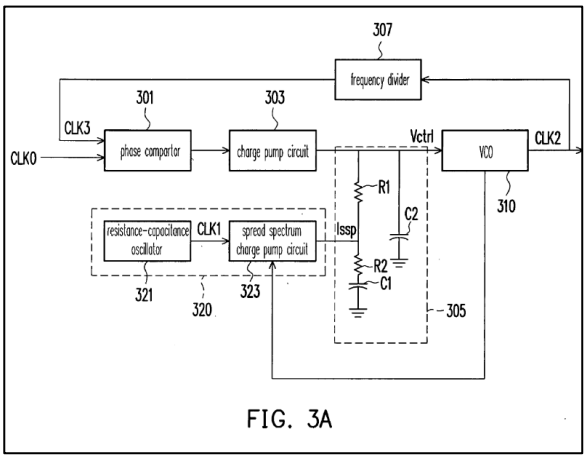


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

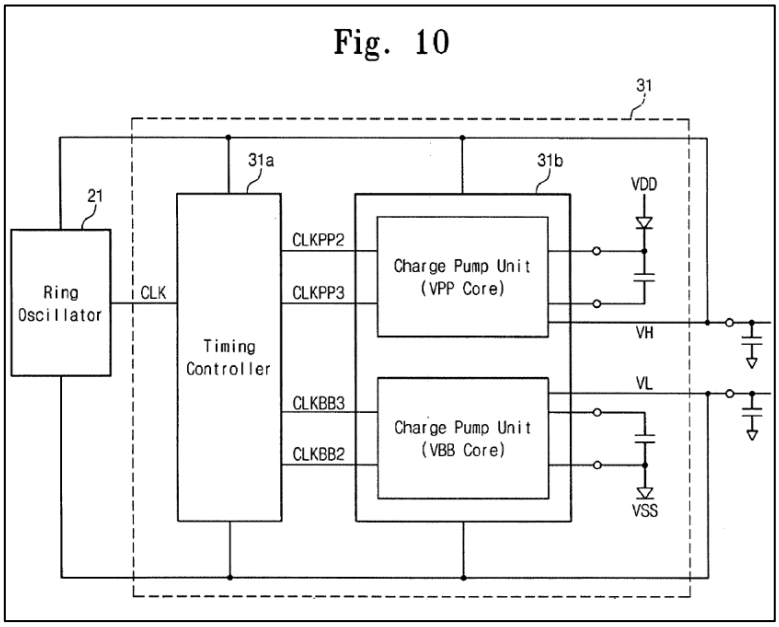


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

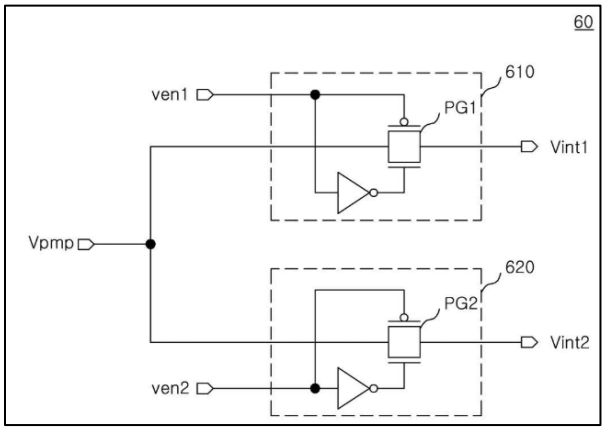
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

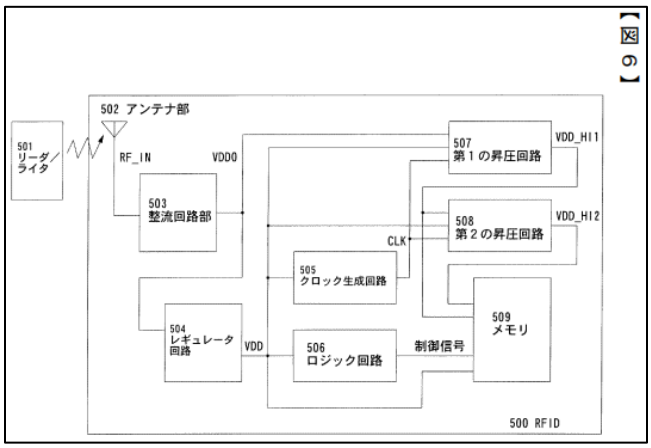
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

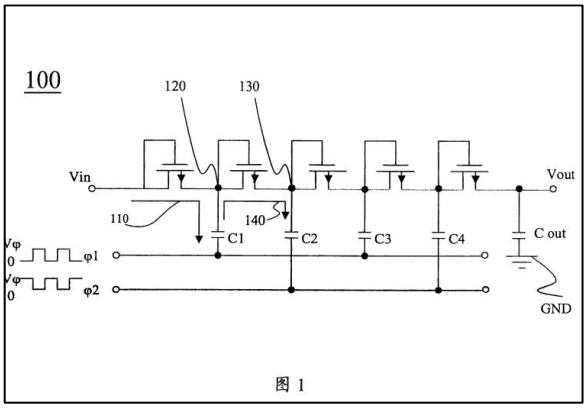
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

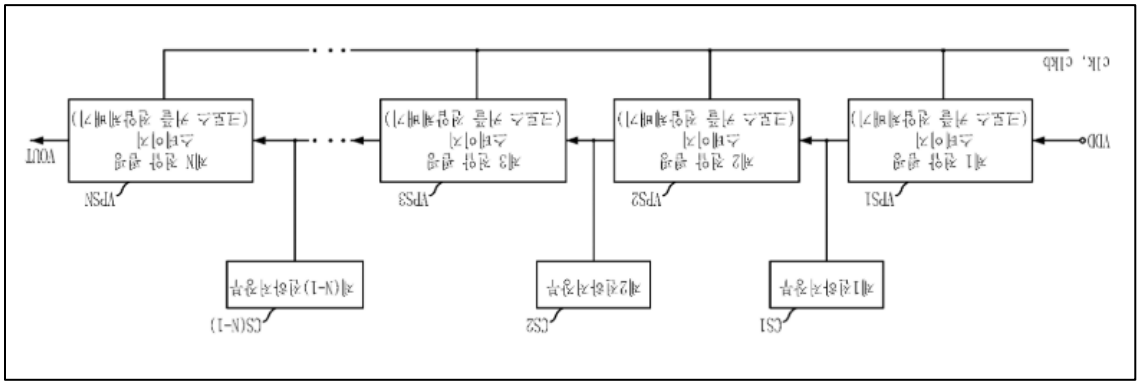
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

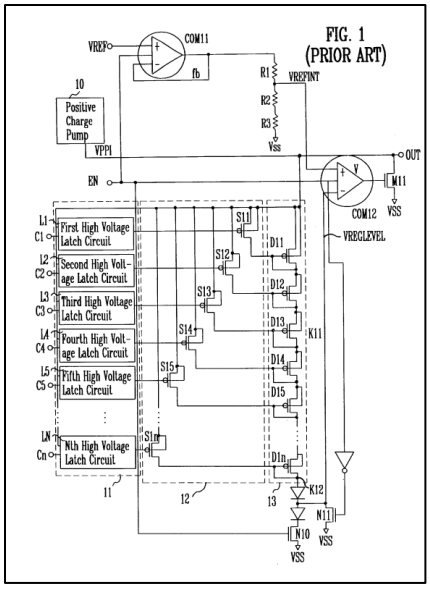
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



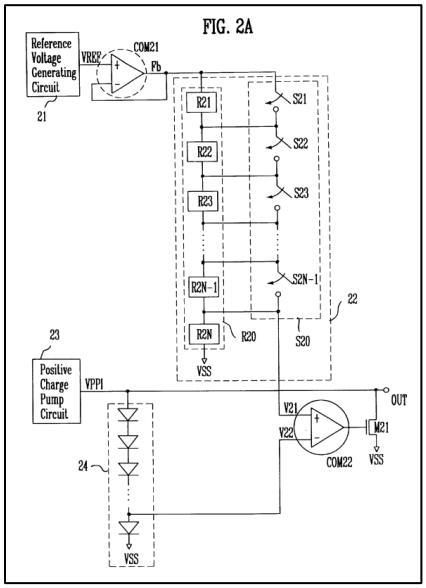
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

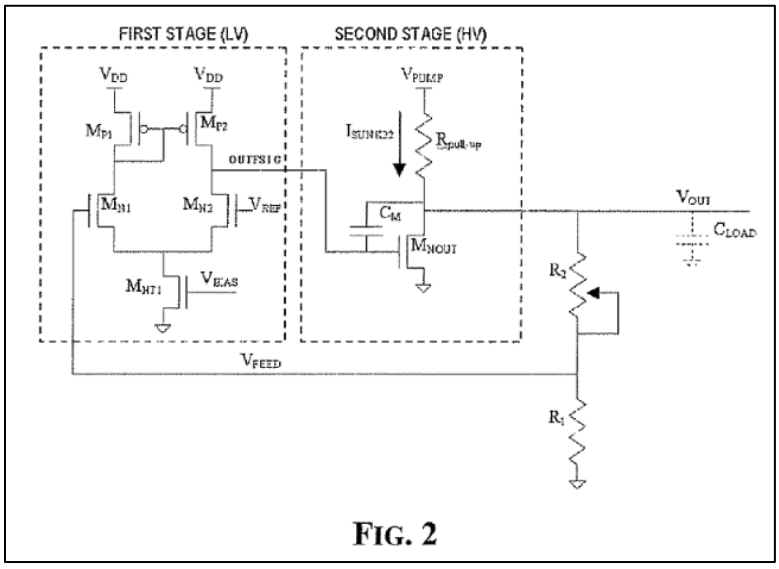


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

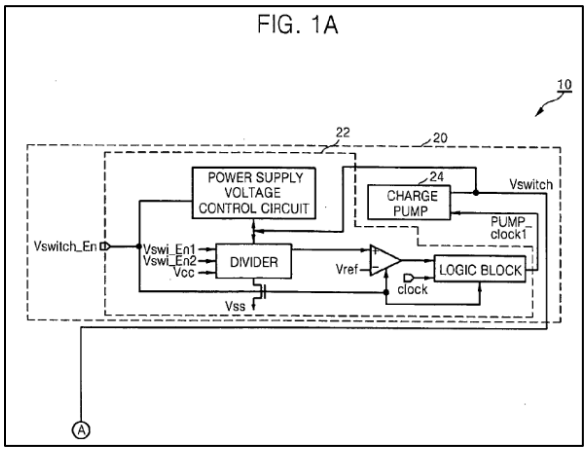
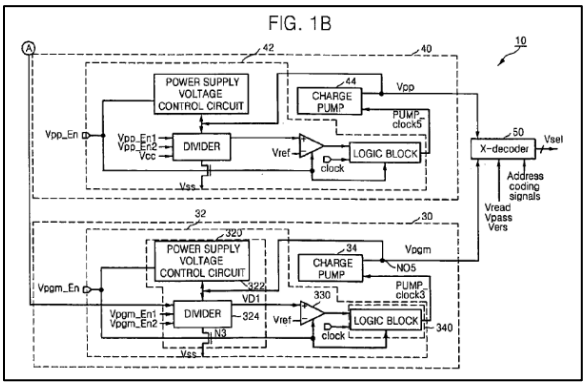
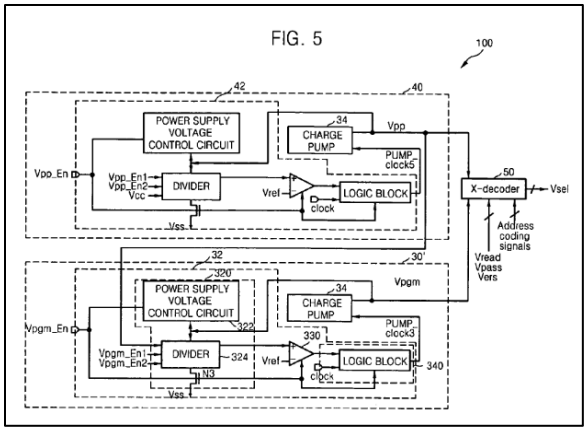


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

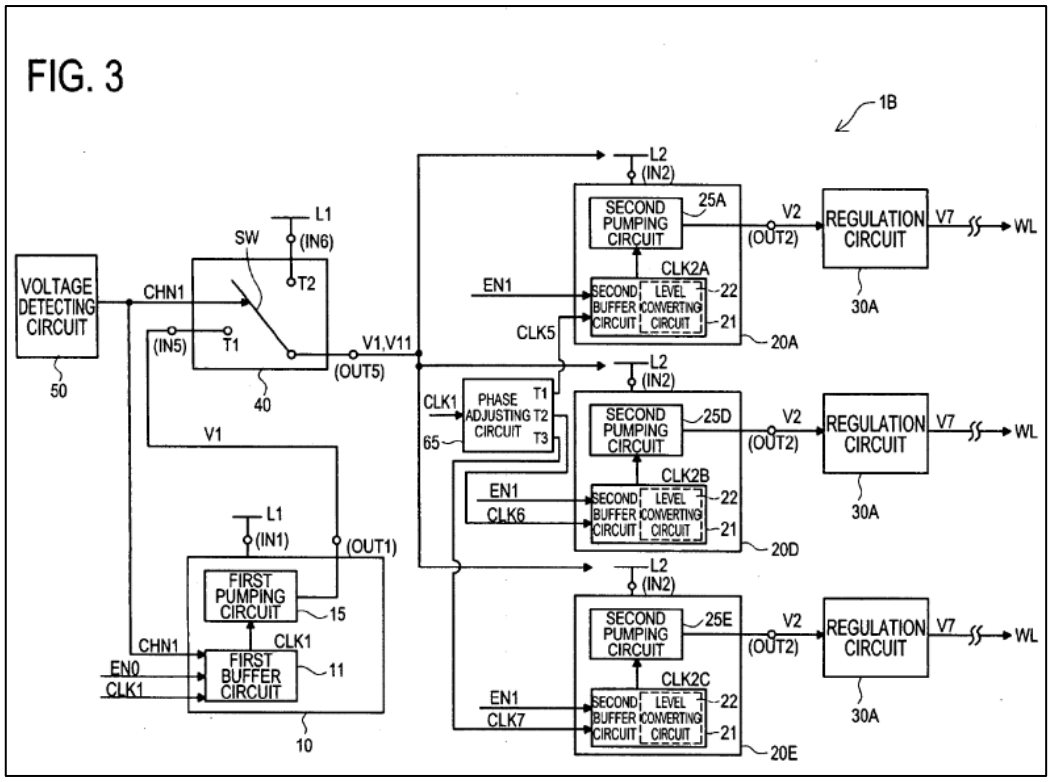
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

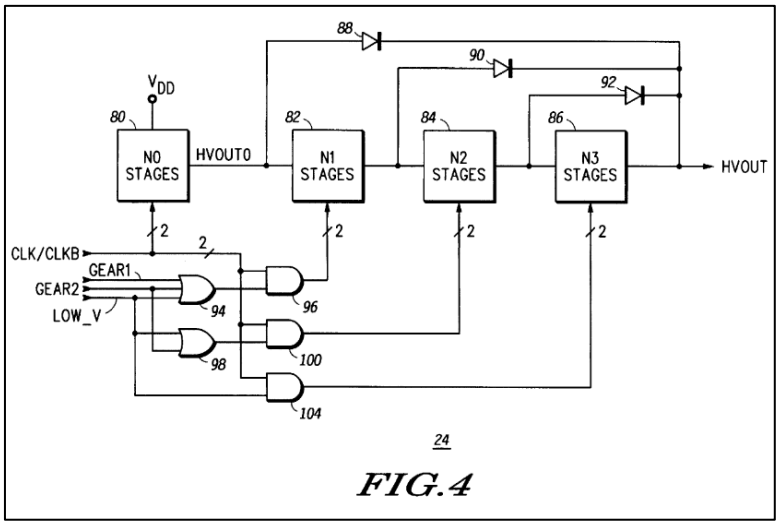


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading

1[d] a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and

The Omnibus References disclose and/or render obvious a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal.

See, e.g.,

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

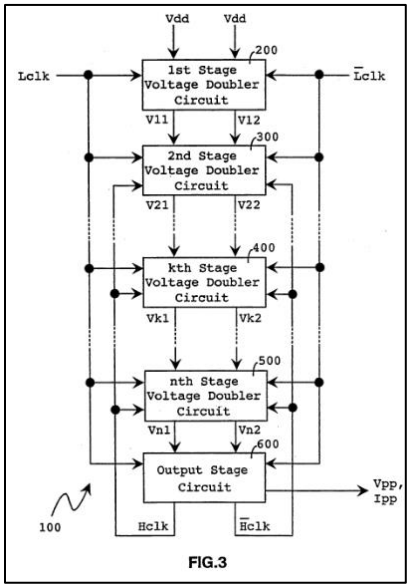


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

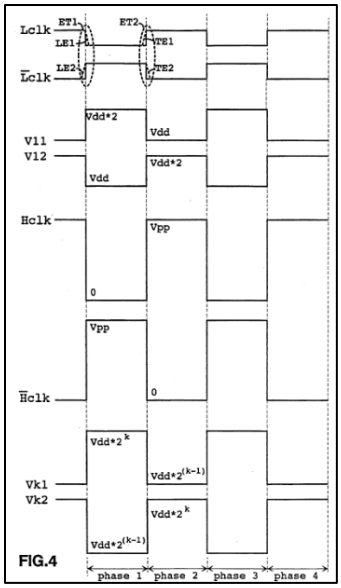


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

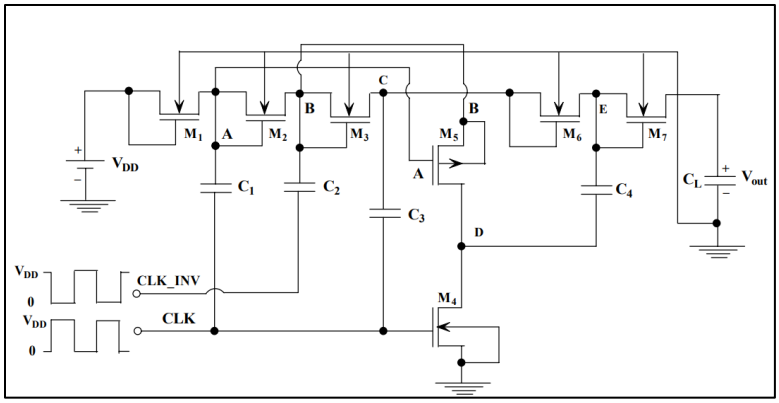
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

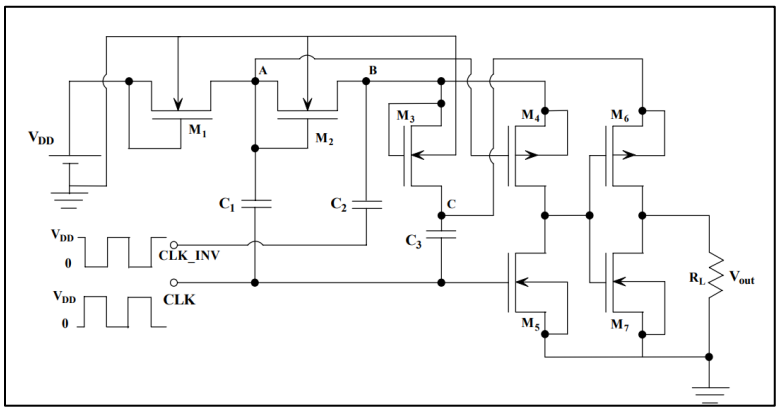
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

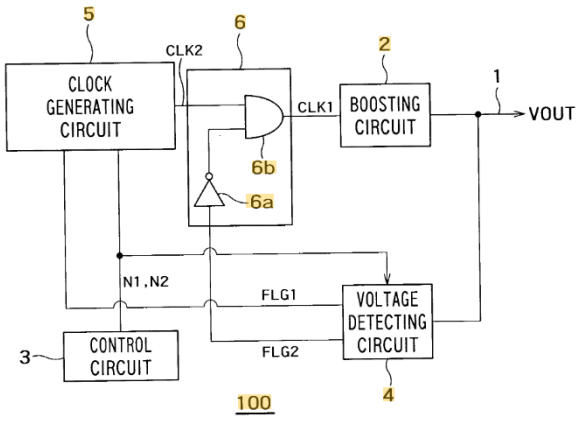


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

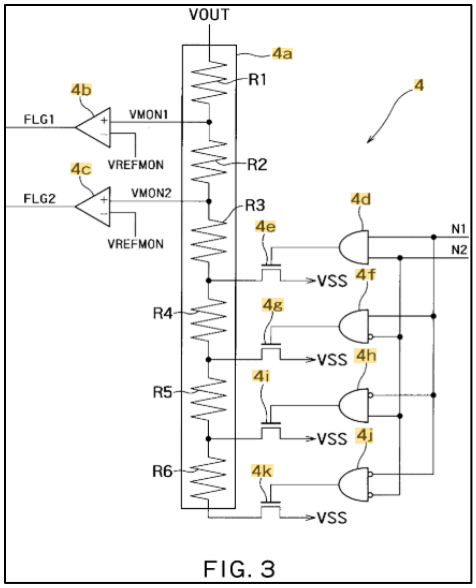


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

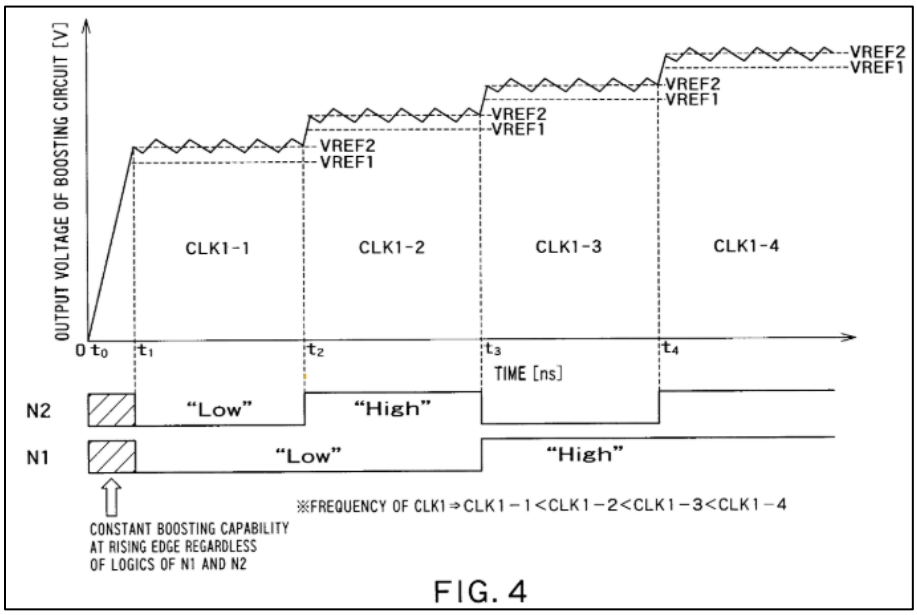


FIG. 4

Sato at [0051]:

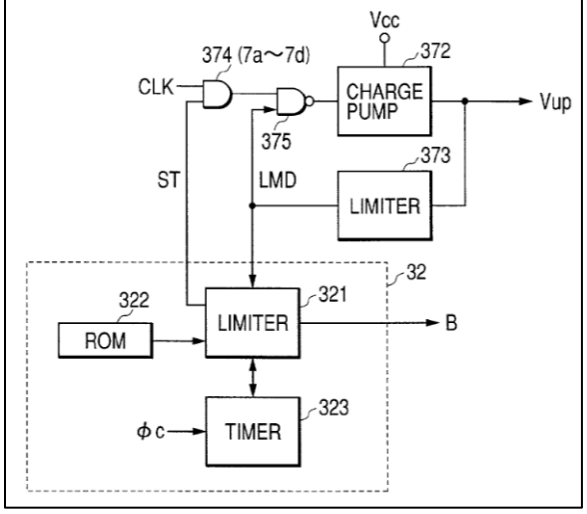
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

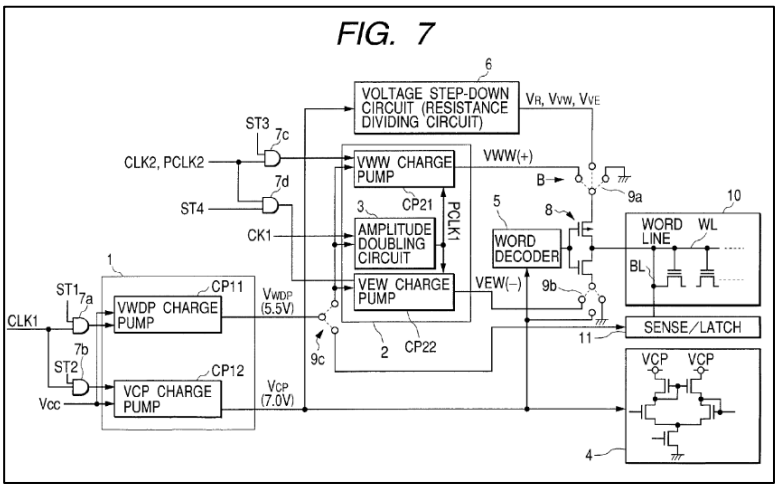
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

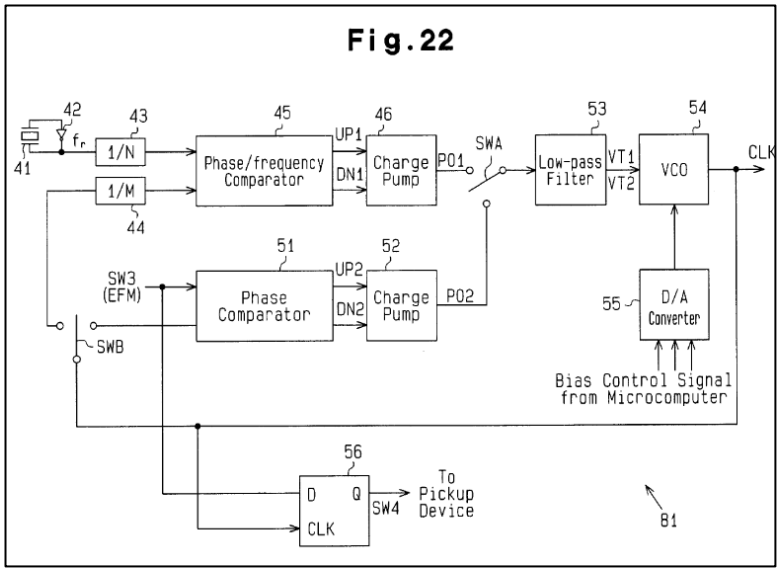
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

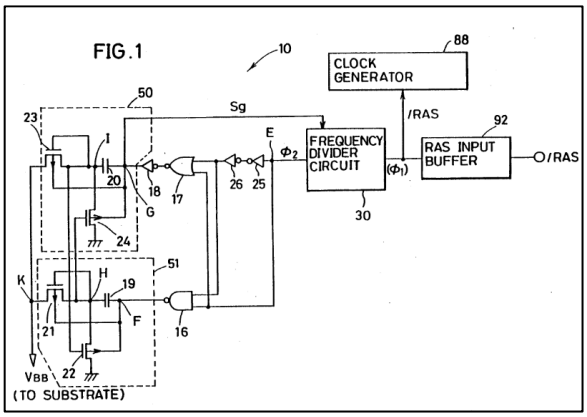


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

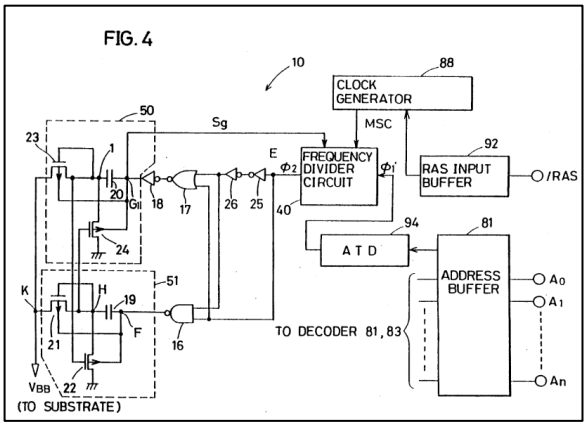
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

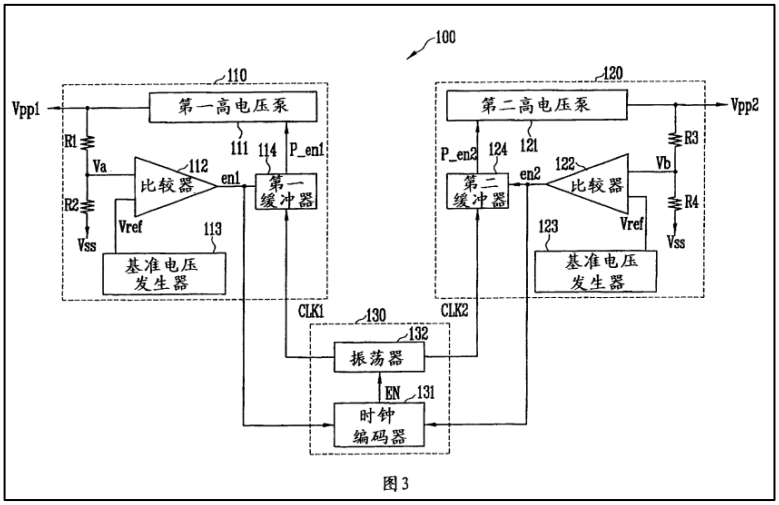


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

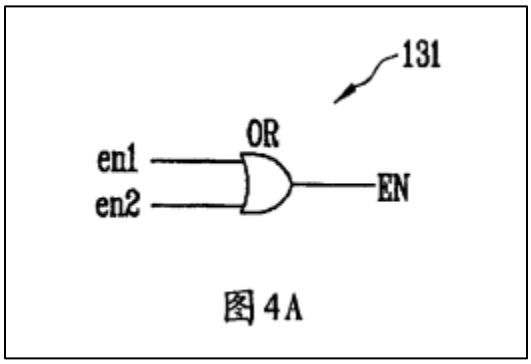


图 4A

Jiang at Fig. 6:

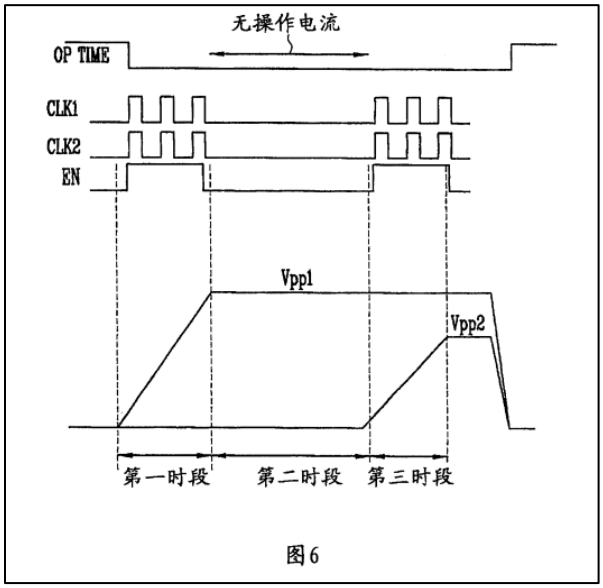
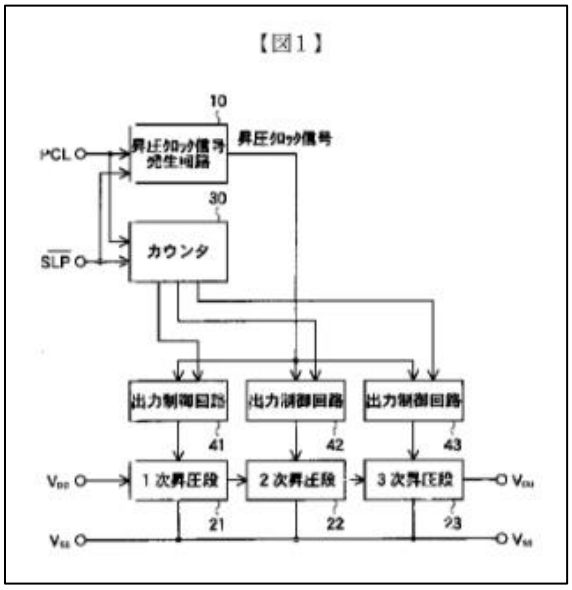


图 6

Ito-633 at [0018] and Fig. 1:

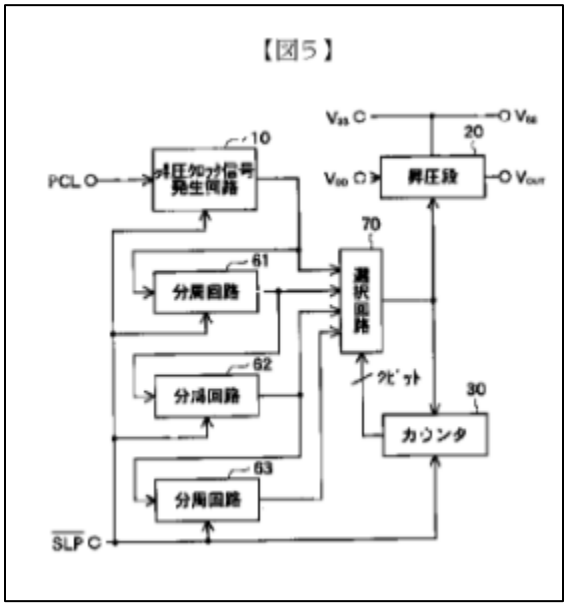
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

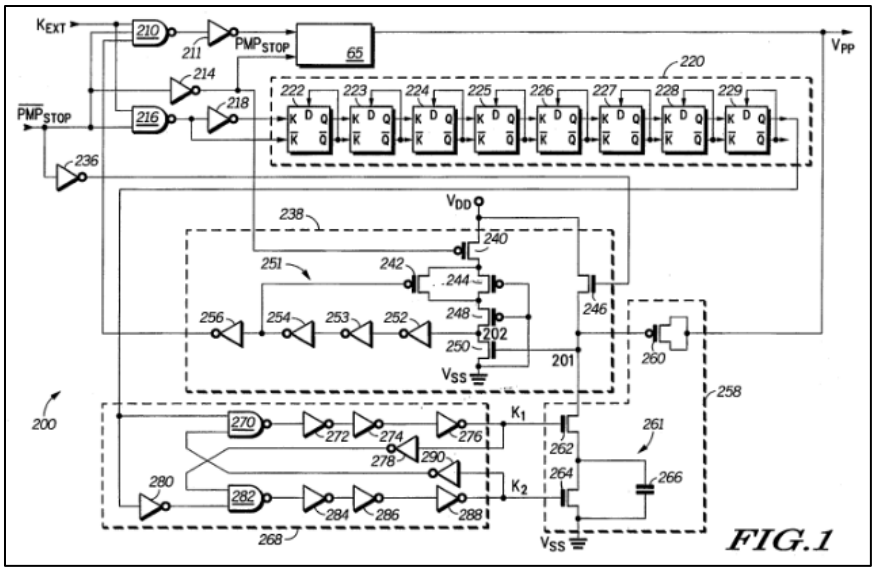


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

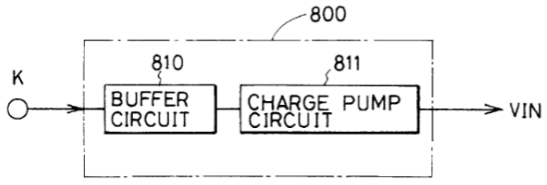


FIG.57

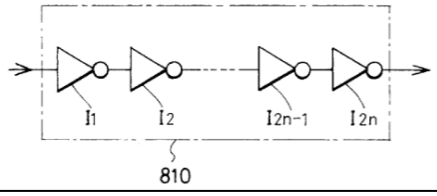


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

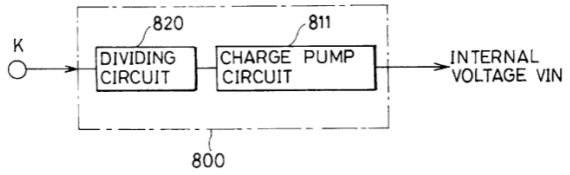
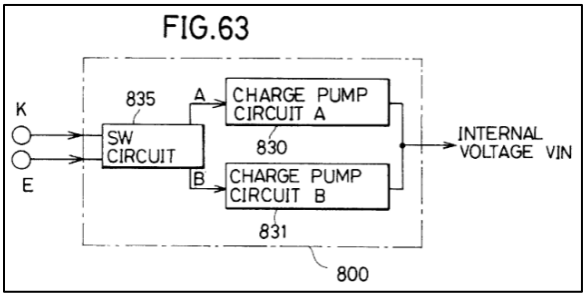


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



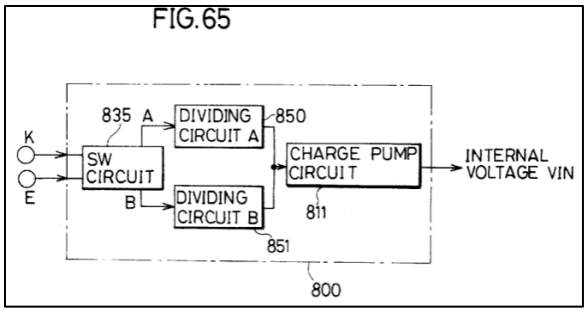
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

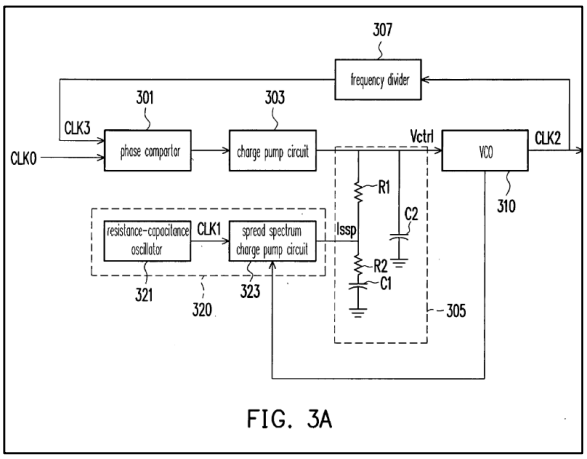


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

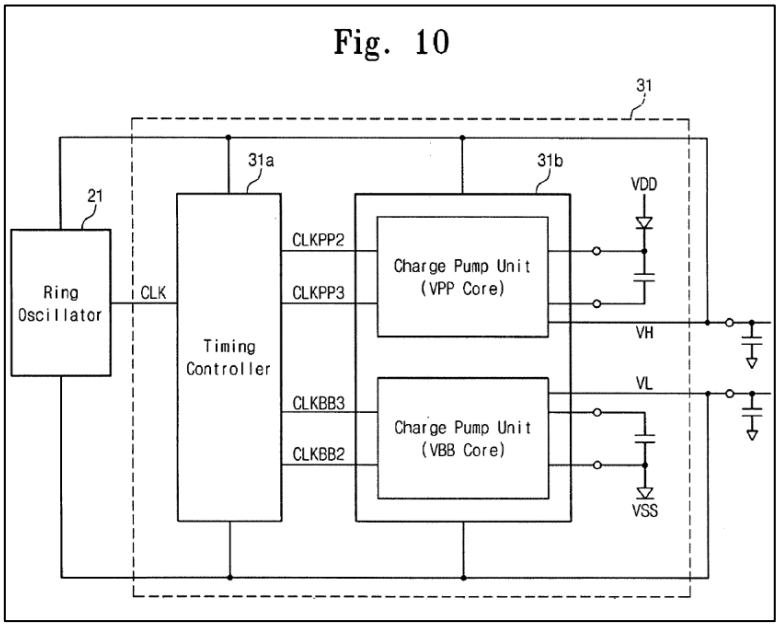


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

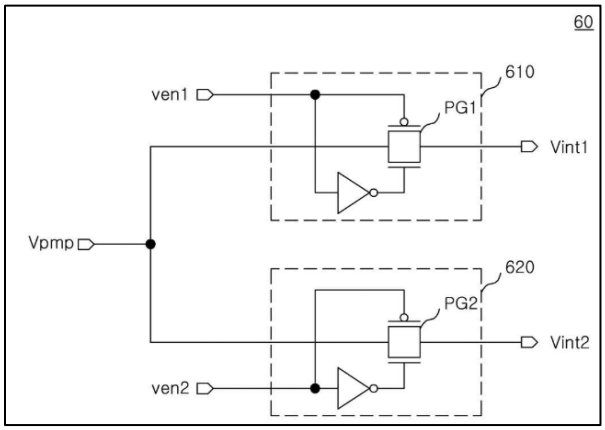
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

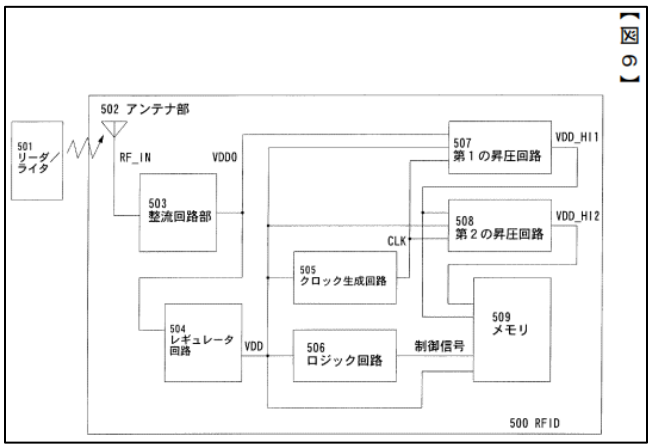
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

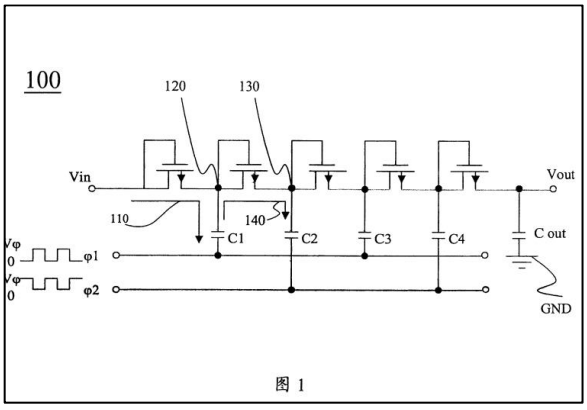
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

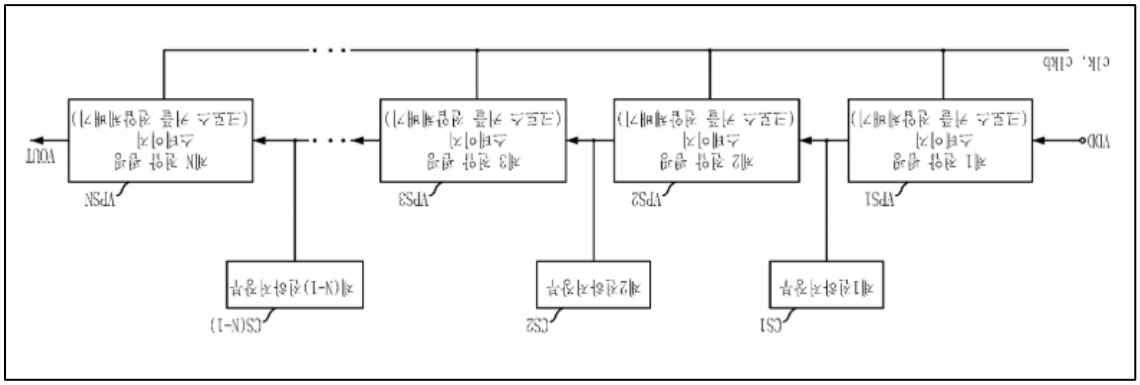
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

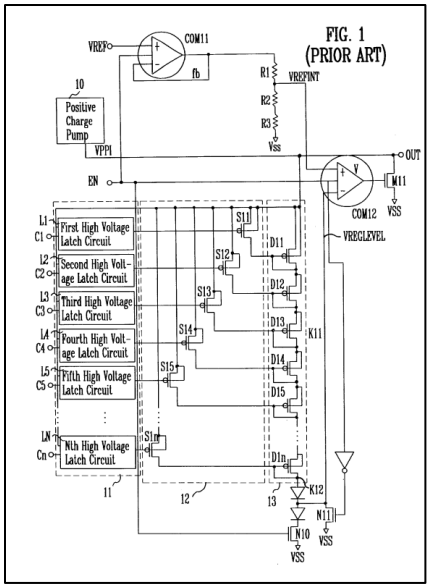
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



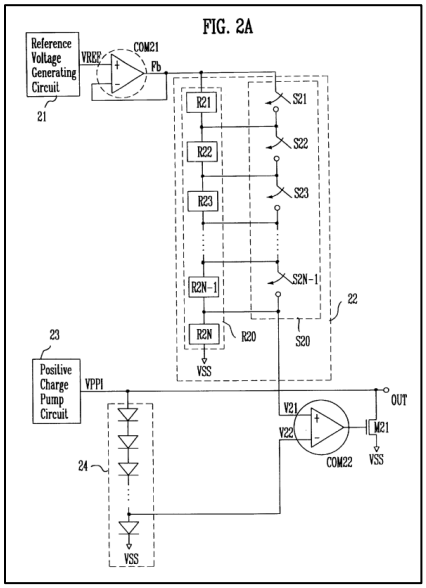
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

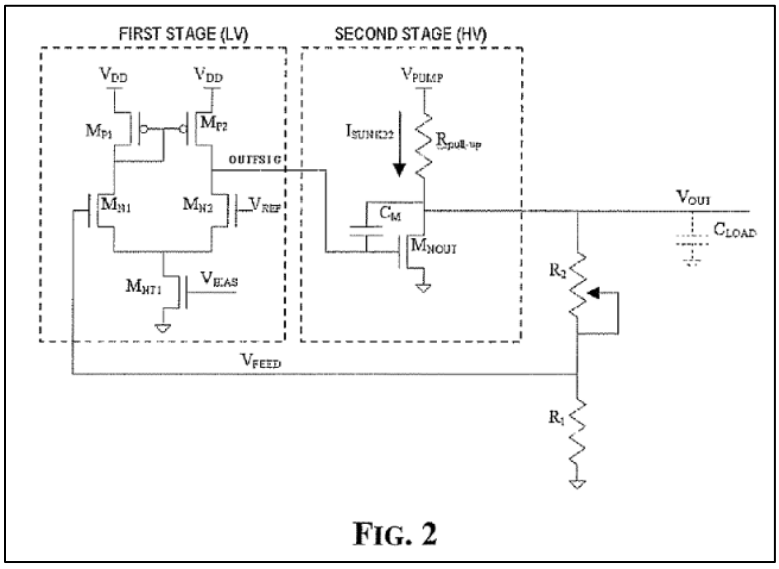


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

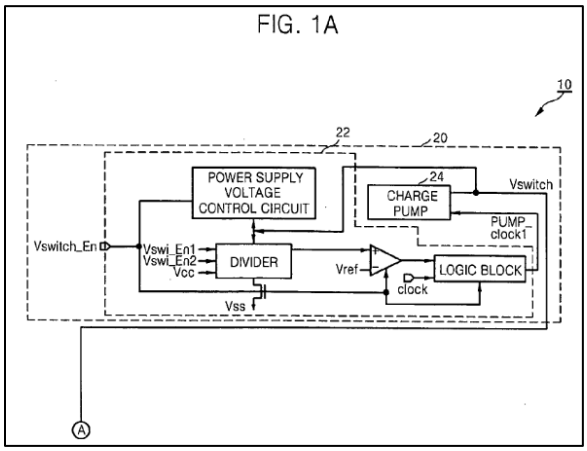
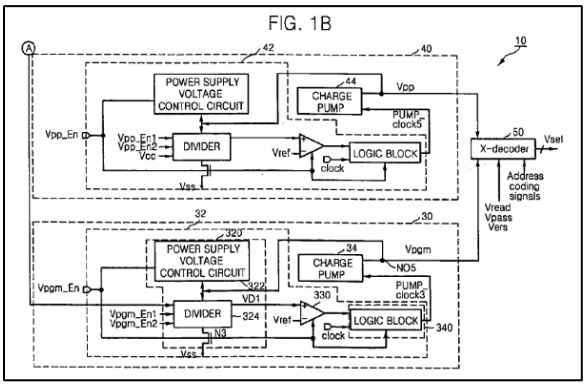
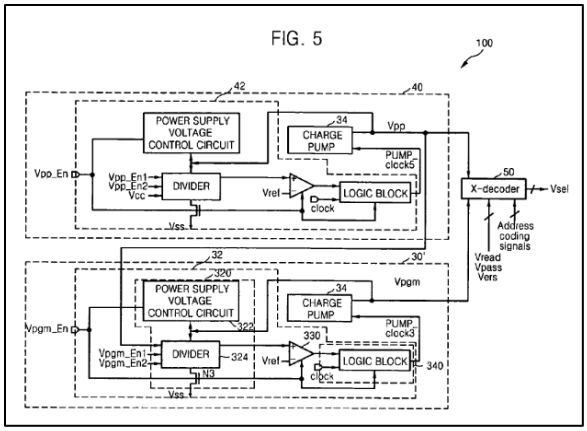


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

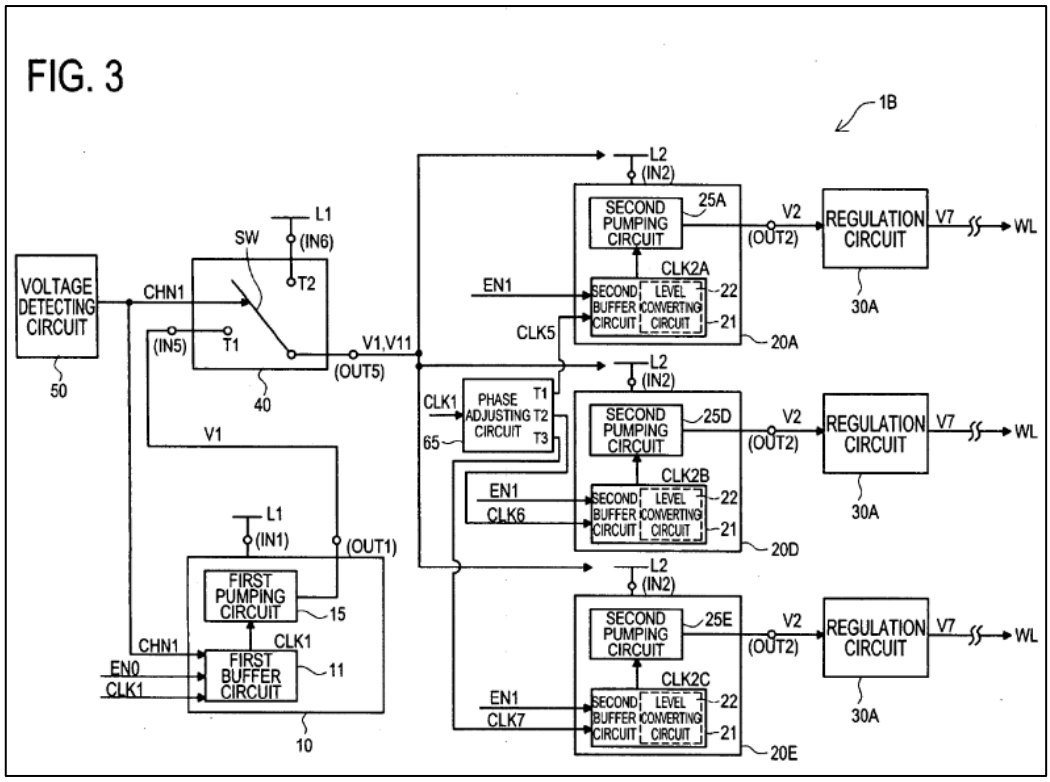
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

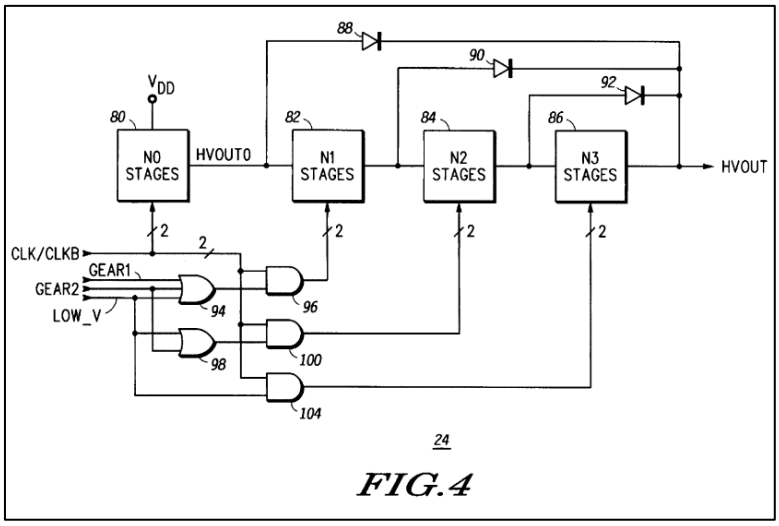


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

1[e] a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.

The Omnibus References disclose and/or render obvious a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.

See, e.g.:

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

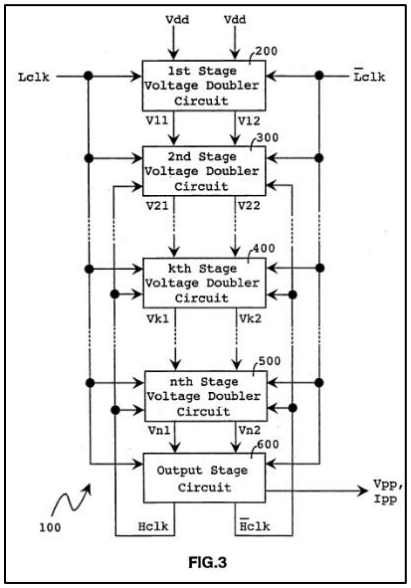


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

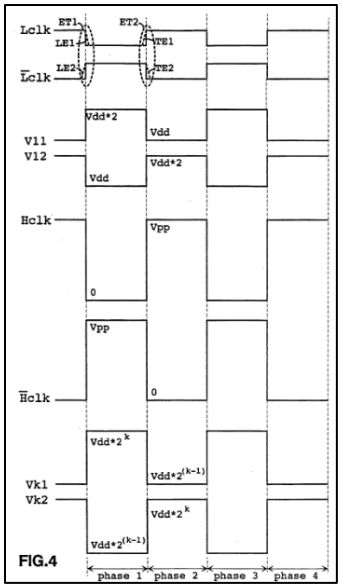


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

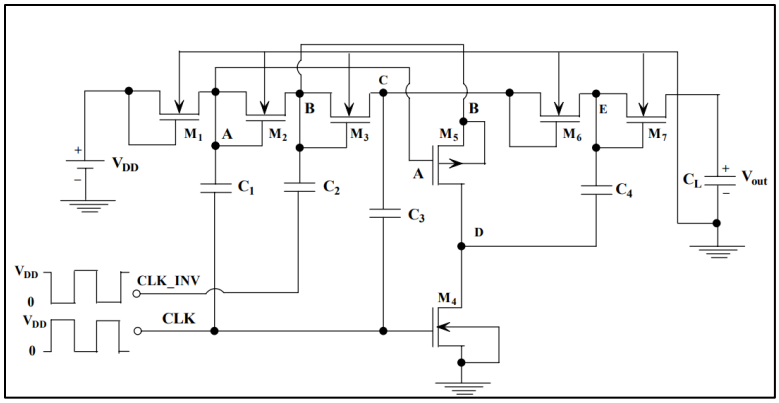
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

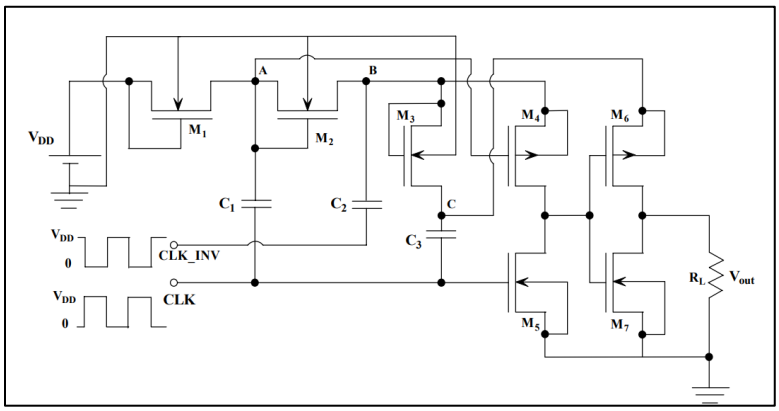
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

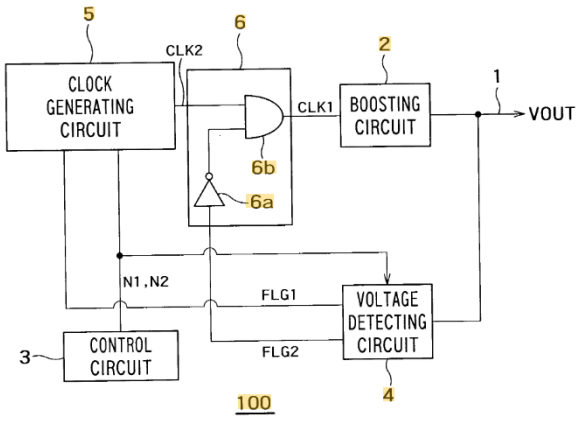


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

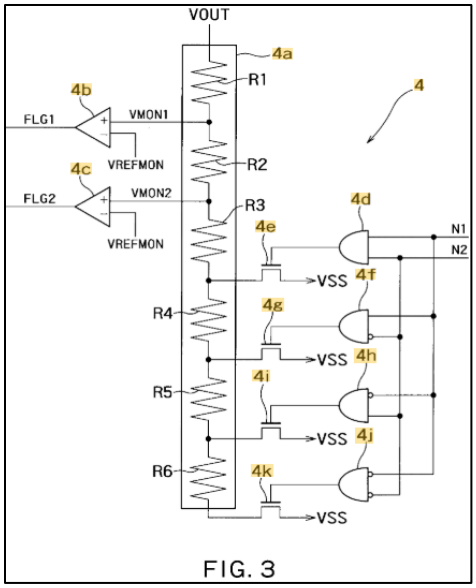


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

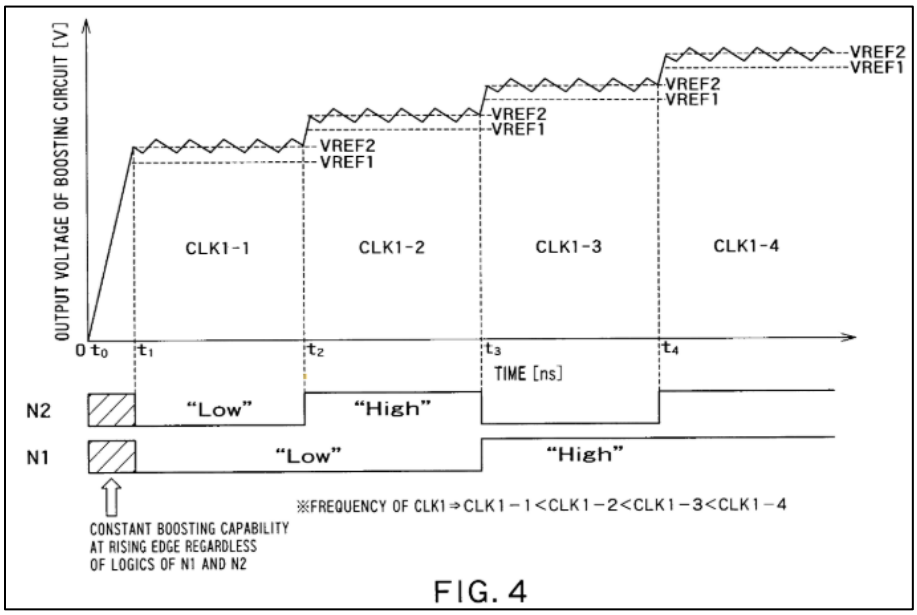


FIG. 4

Sato at [0051]:

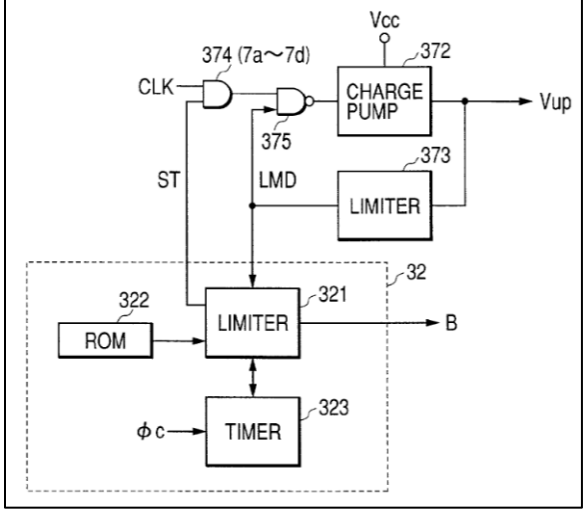
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

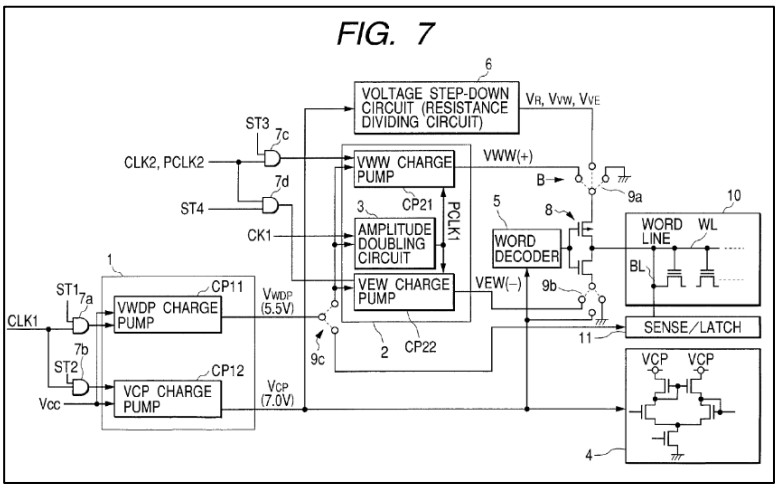
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

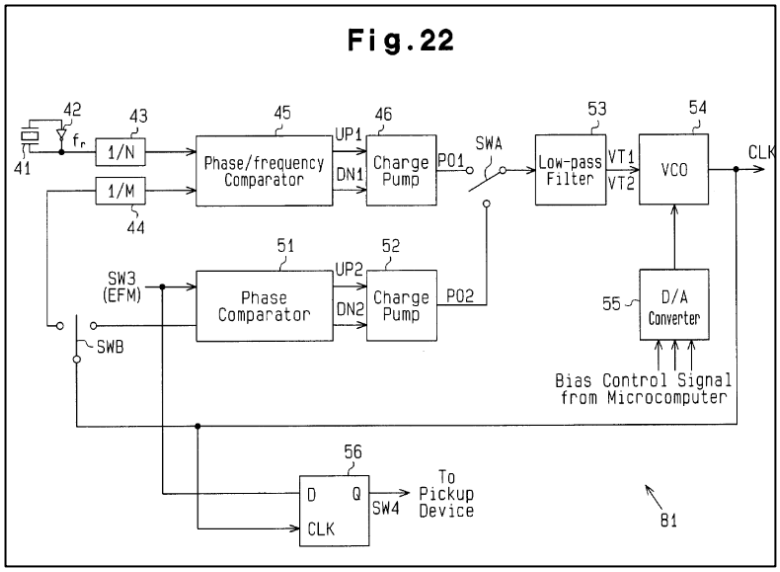
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

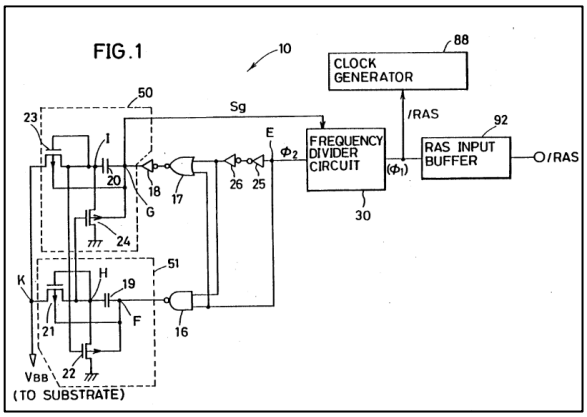


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

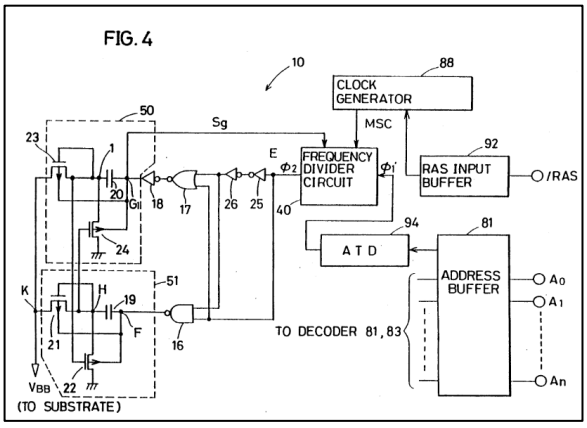
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

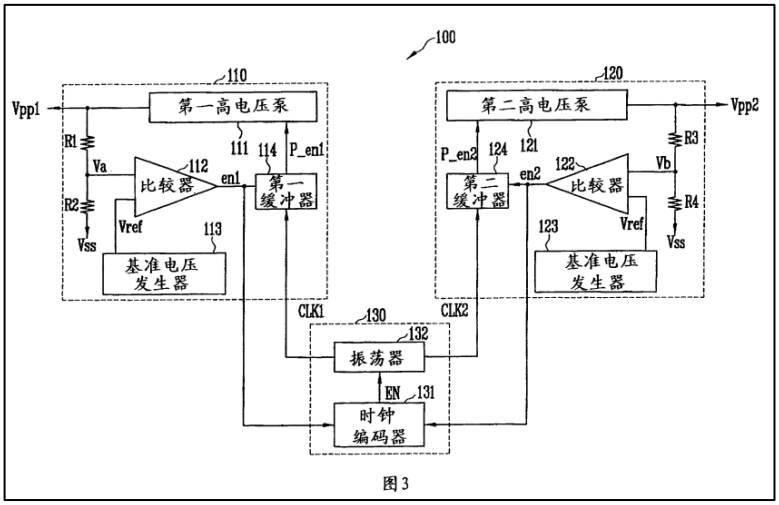


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

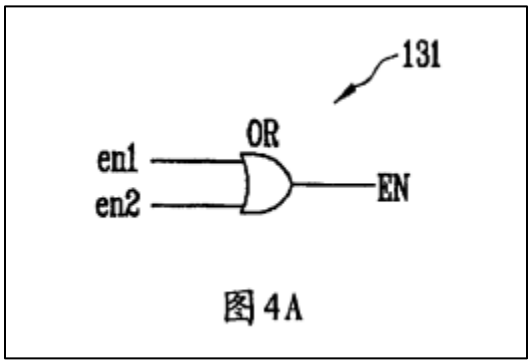


图 4A

Jiang at Fig. 6:

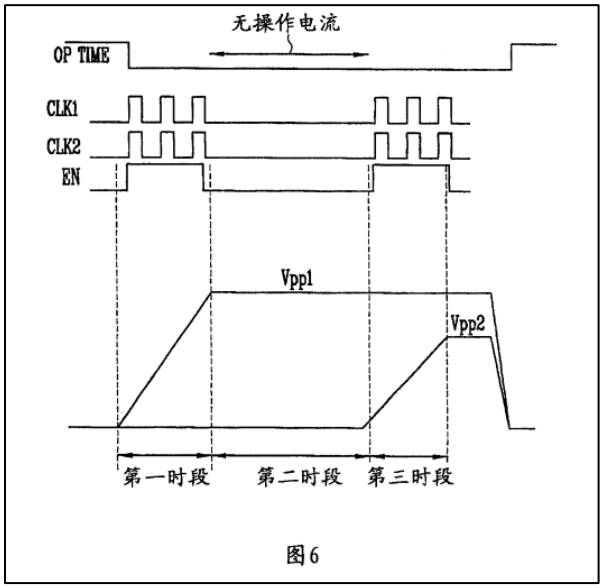
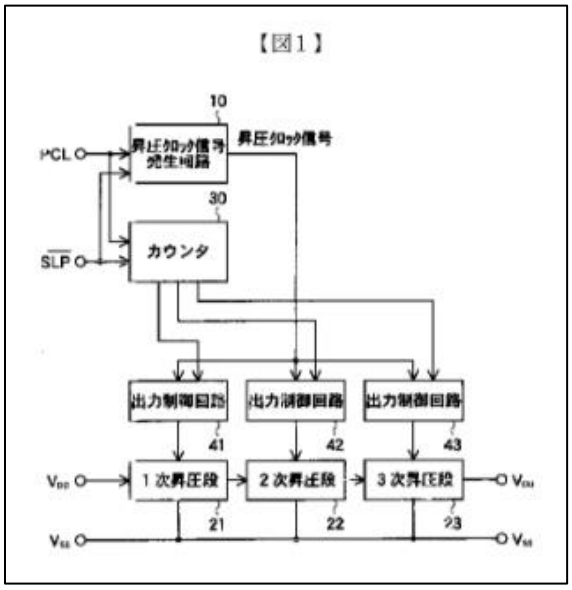


图6

Ito-633 at [0018] and Fig. 1:

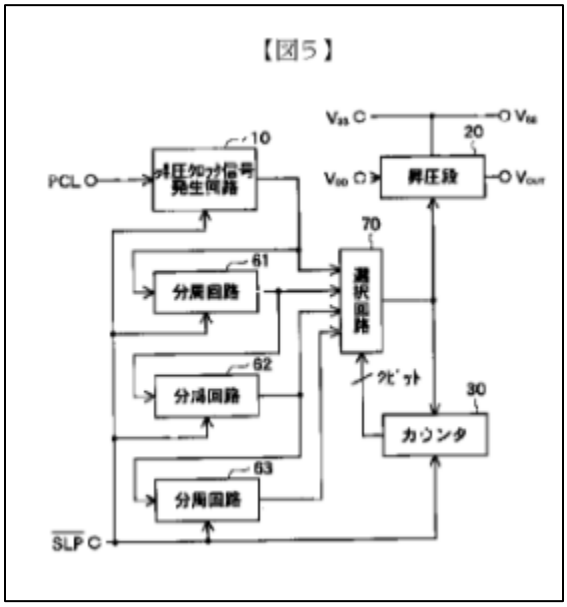
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

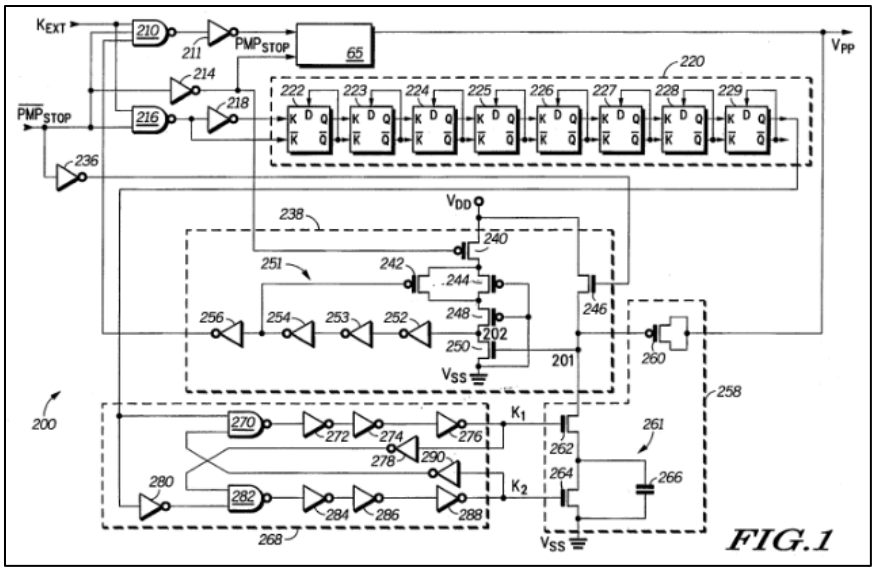


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

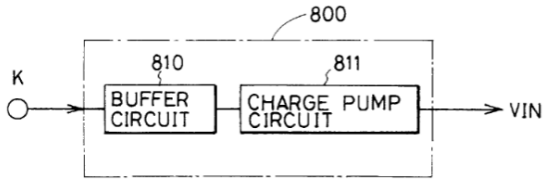


FIG.57

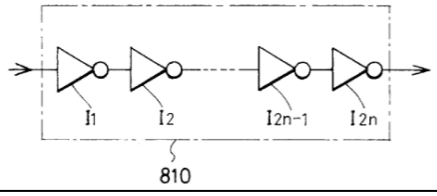


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

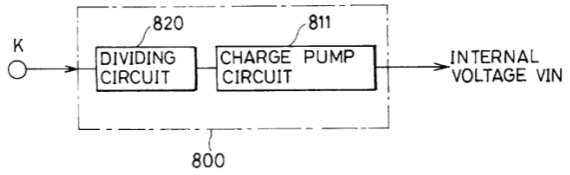
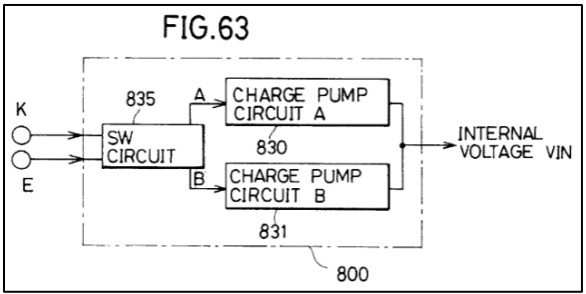


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

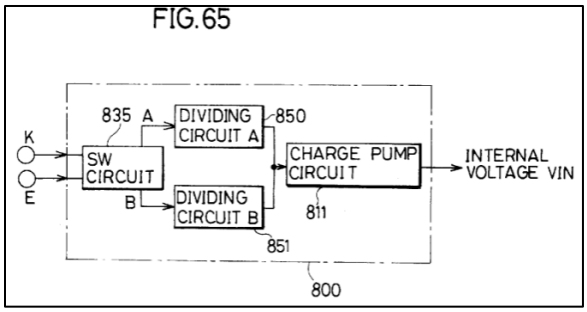
Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.

FIG.65



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

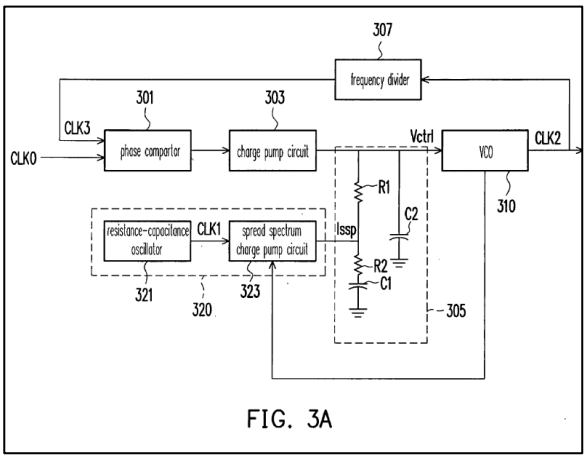


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

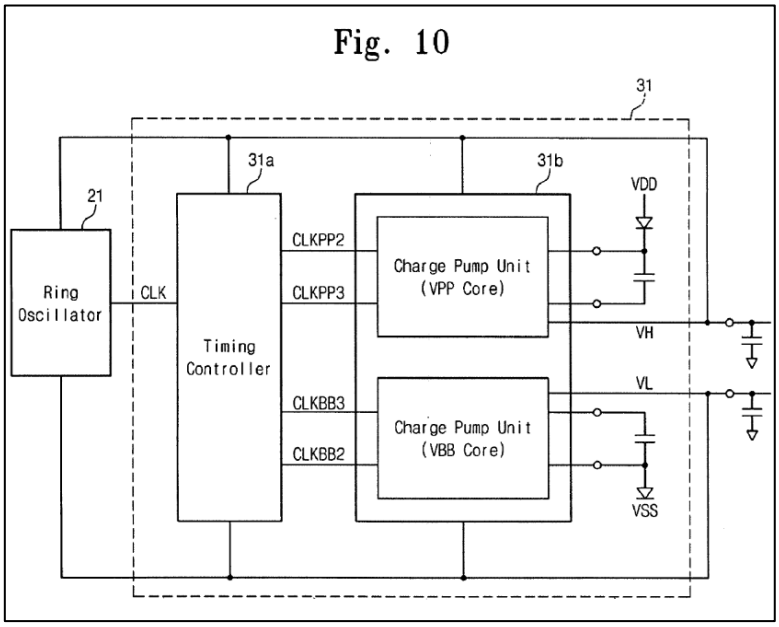


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

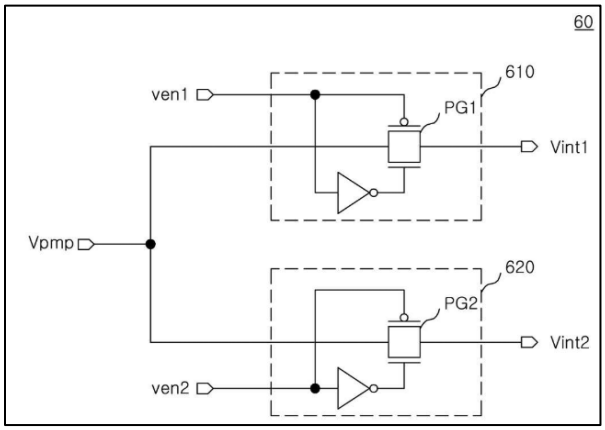
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

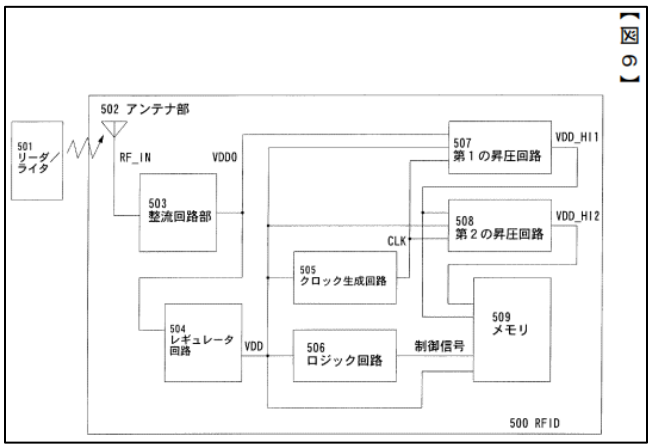
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

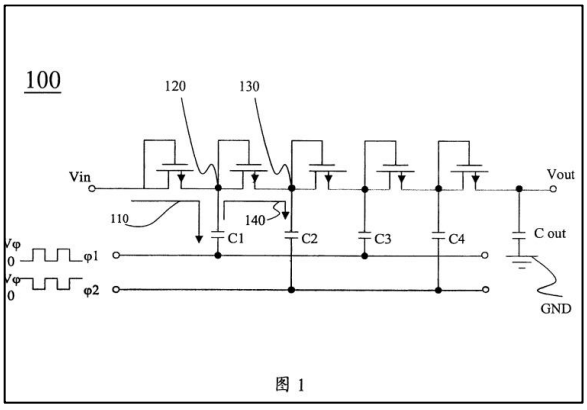
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

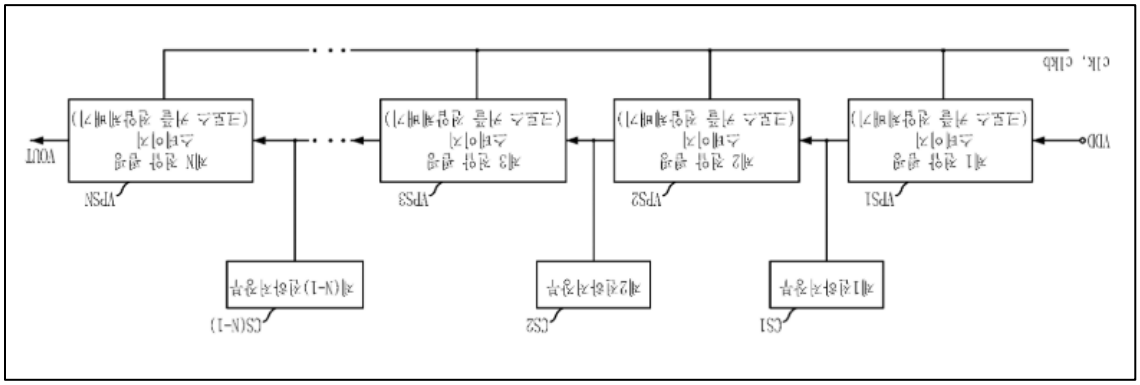
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

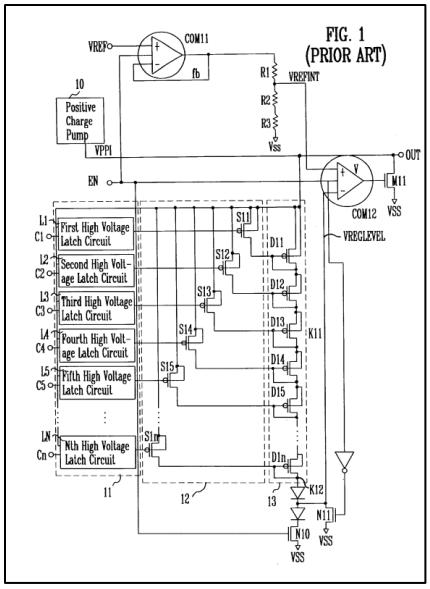
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



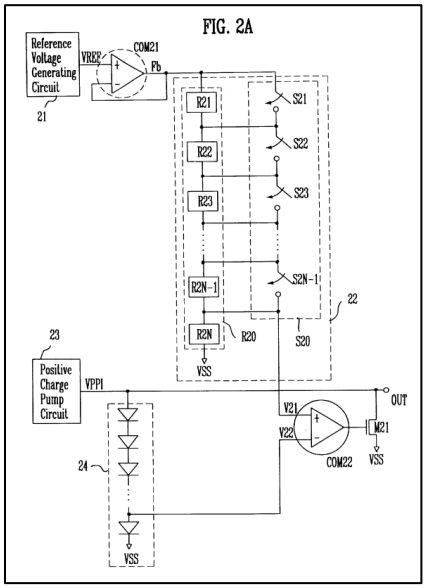
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R**2**N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

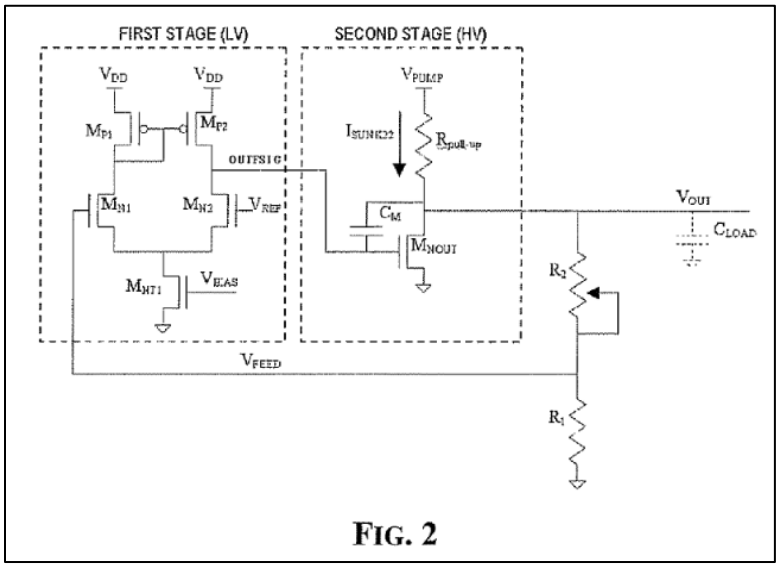


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

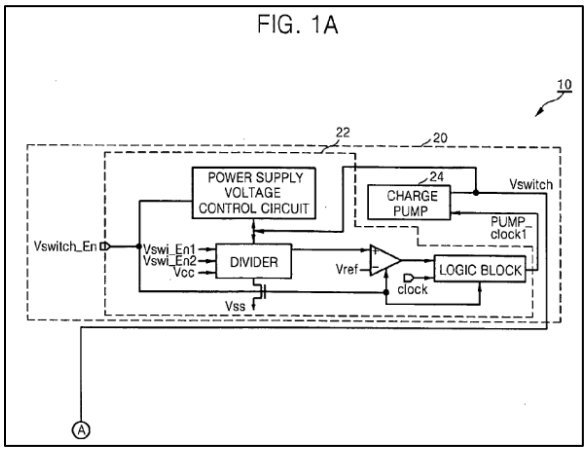
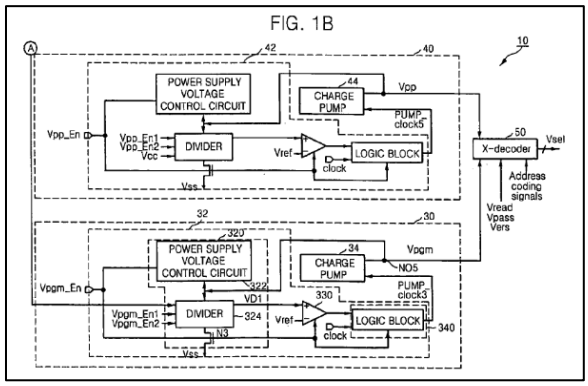
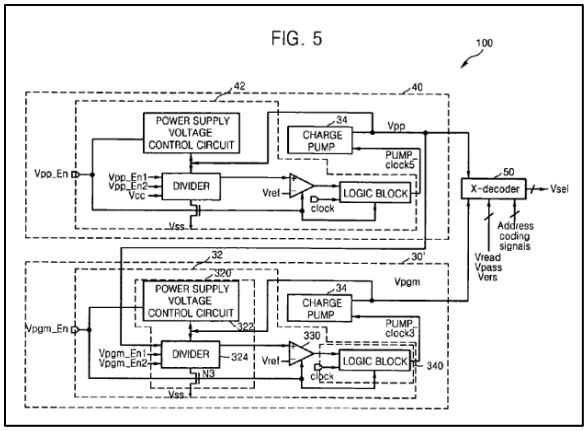


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

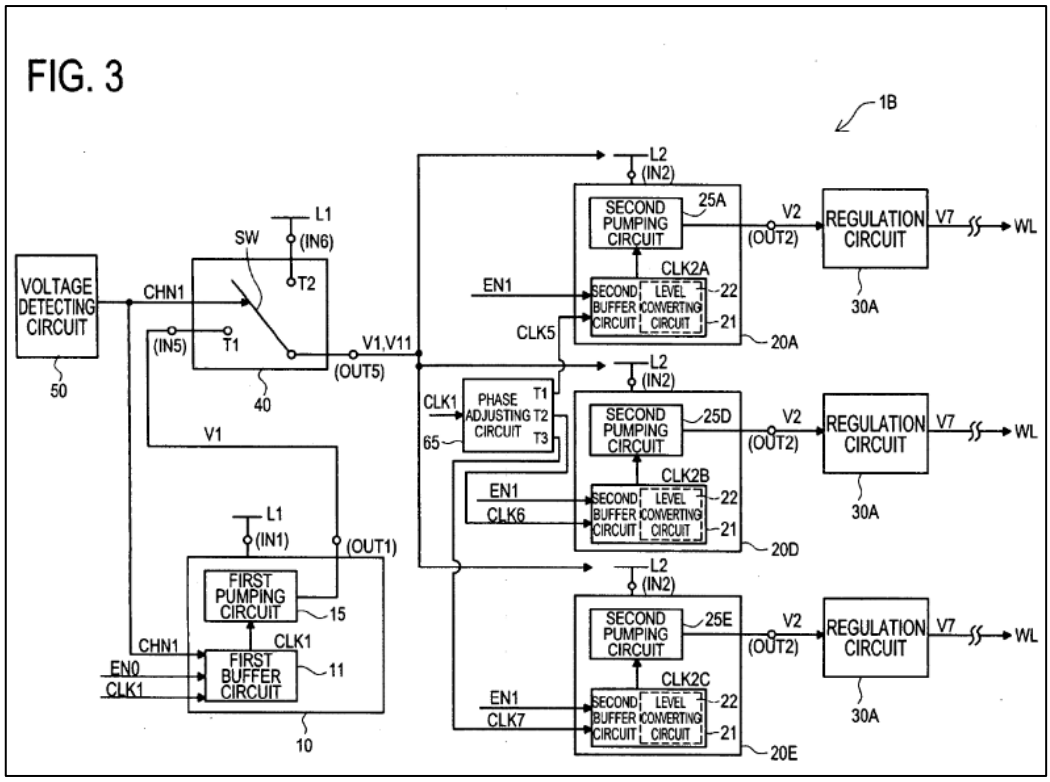
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

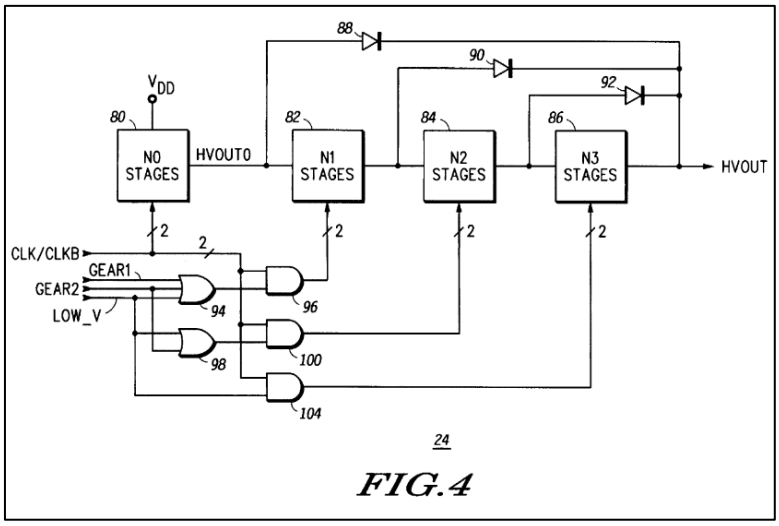


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[a] An internal voltage generating circuit comprising:

The Omnibus References disclose and/or render obvious an internal voltage generating circuit.

See, e.g.: claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[b] a first charge pump circuit configured to generate a second voltage from a first voltage;

The Omnibus References disclose and/or render obvious a first charge pump circuit configured to generate a second voltage from a first voltage.

See, e.g.: claim limitation 1[b], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

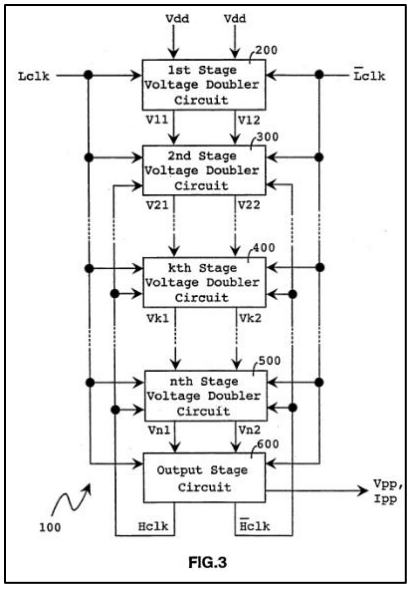


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second

voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

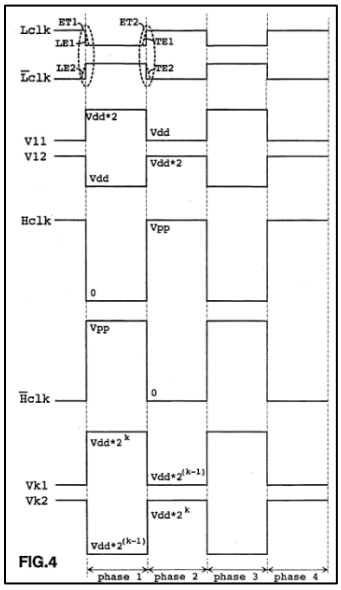


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation

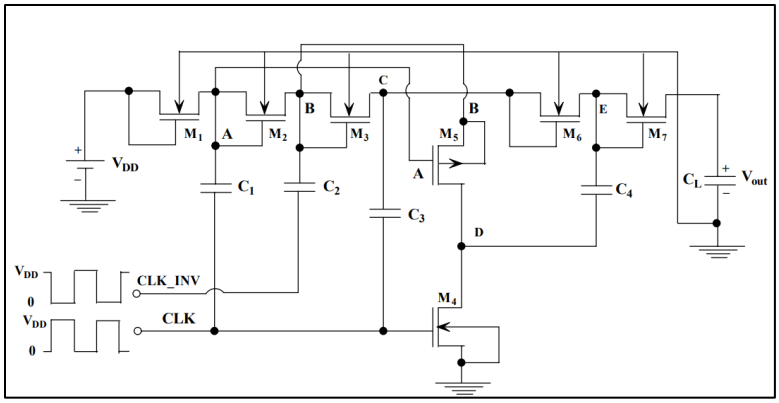
filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

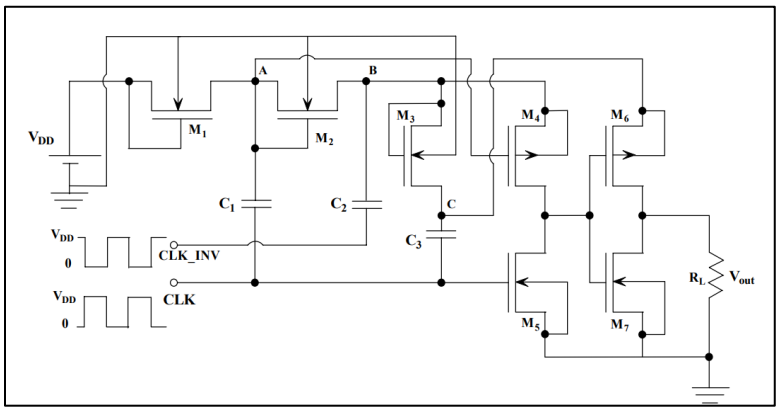
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

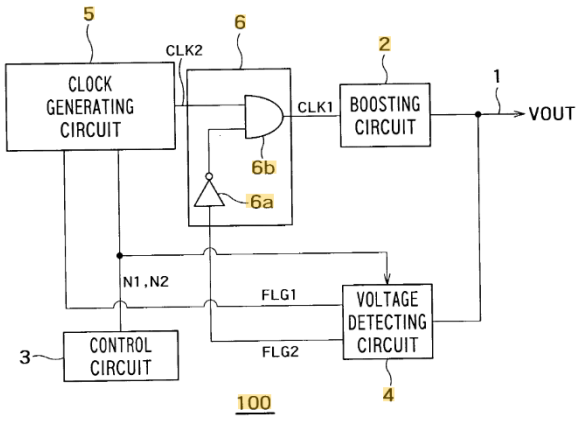


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

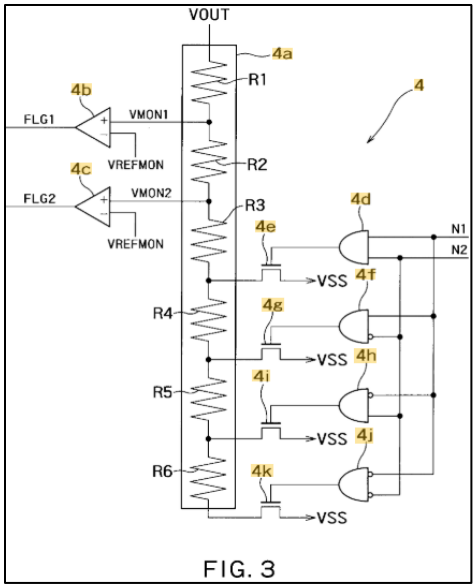


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

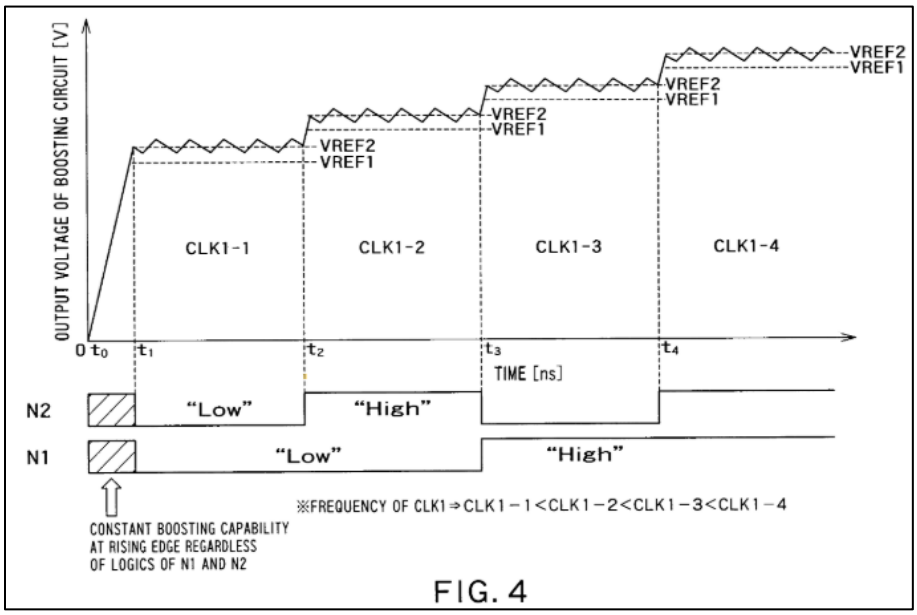


FIG. 4

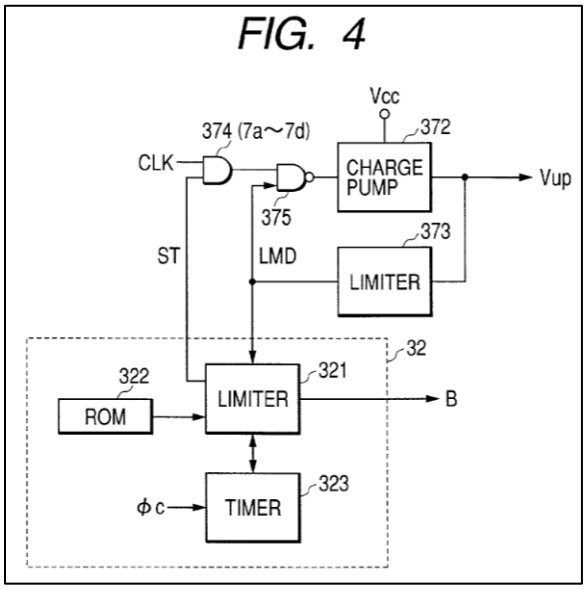
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

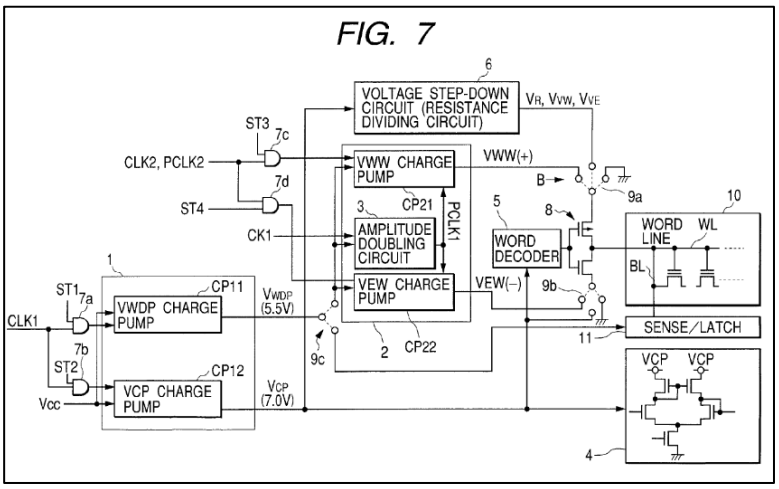
Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

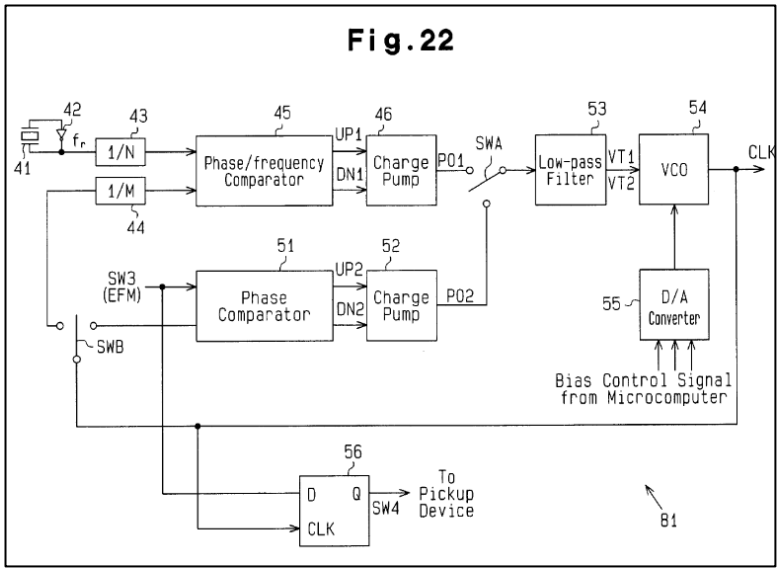
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

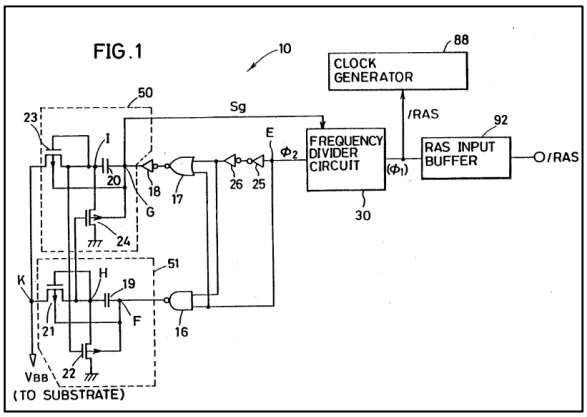


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

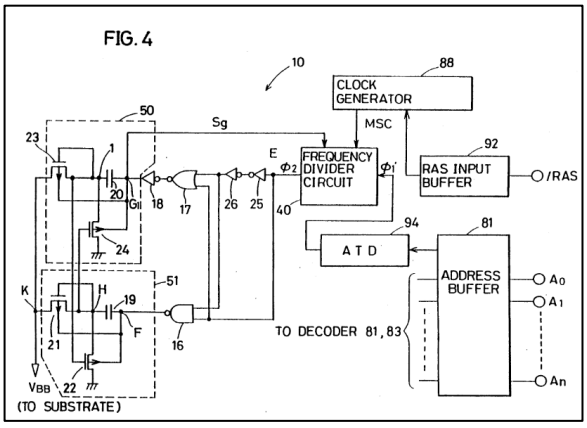
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

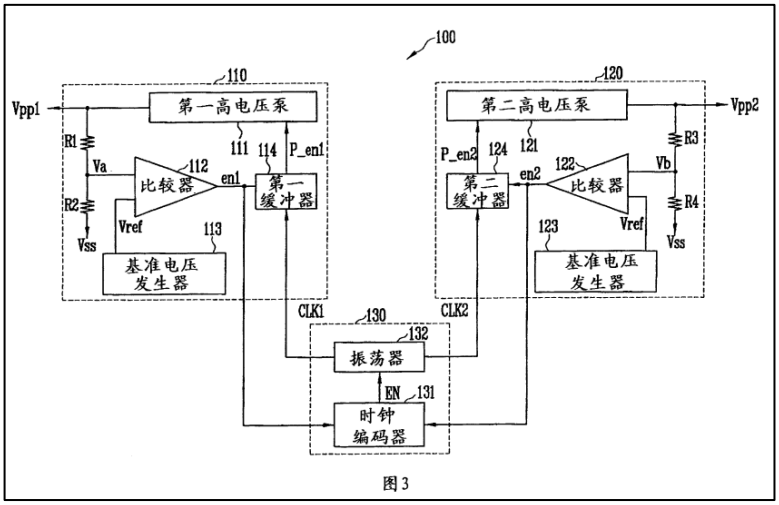


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

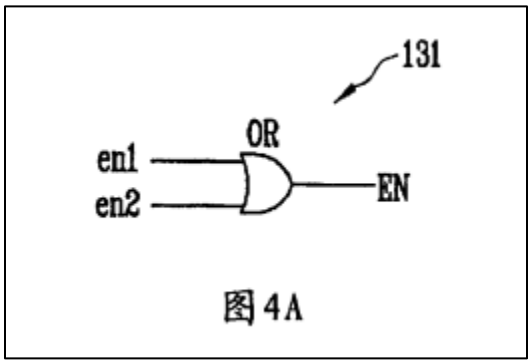


图 4A

Jiang at Fig. 6:

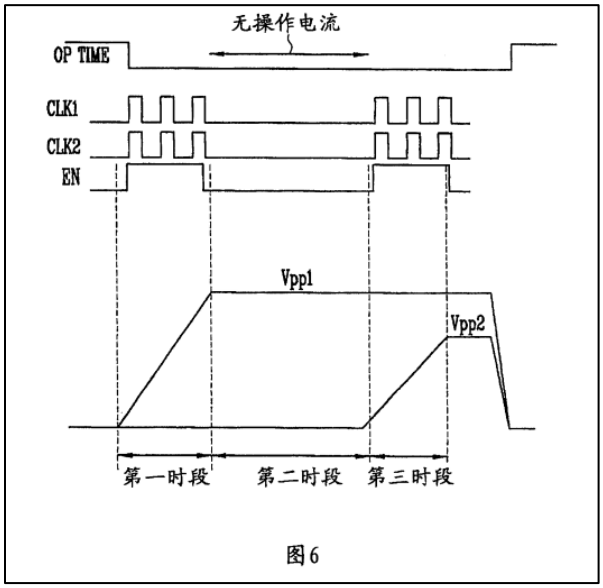
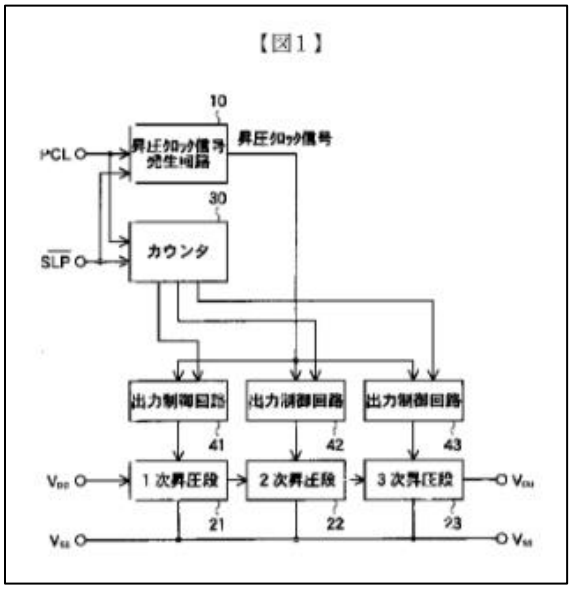


图6

Ito-633 at [0018] and Fig. 1:

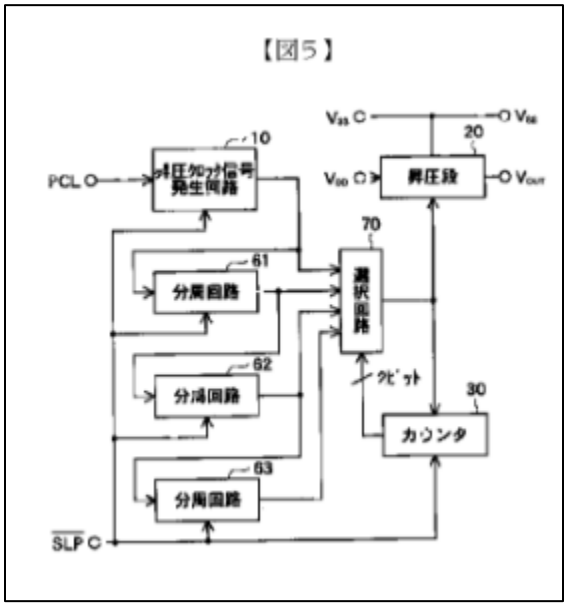
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

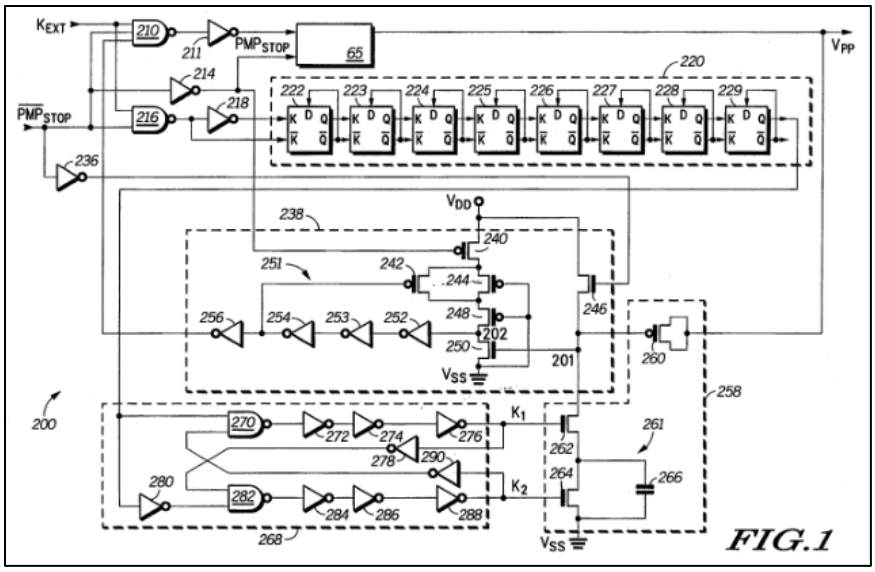


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

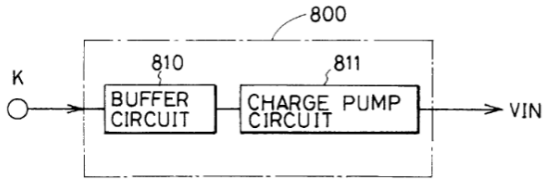


FIG.57

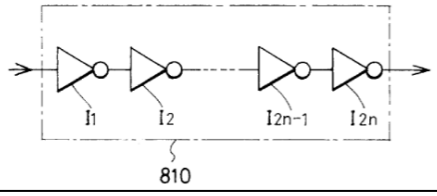


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

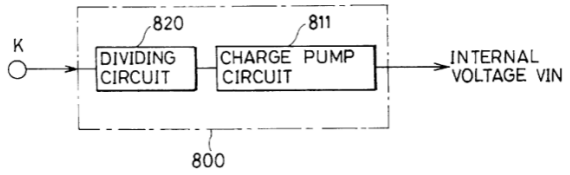
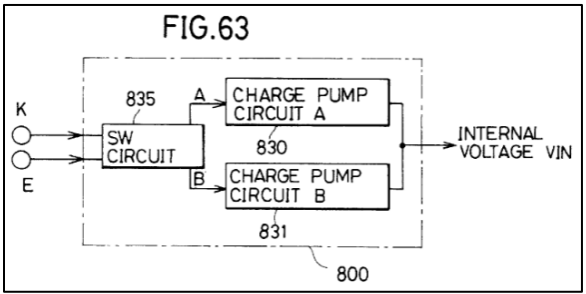


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



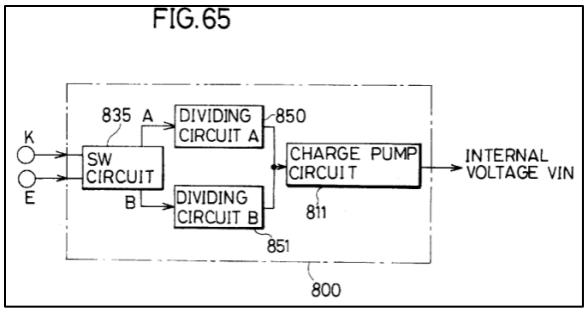
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

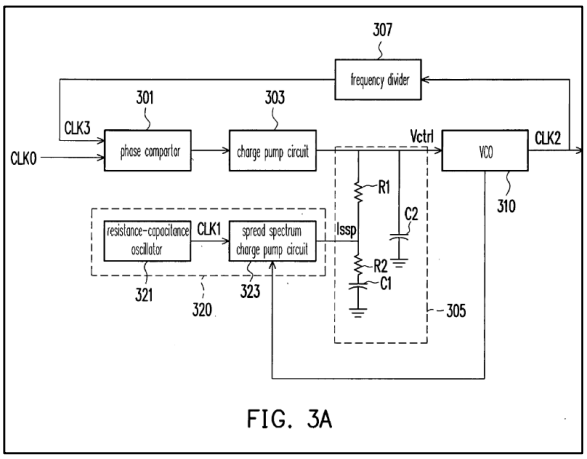


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

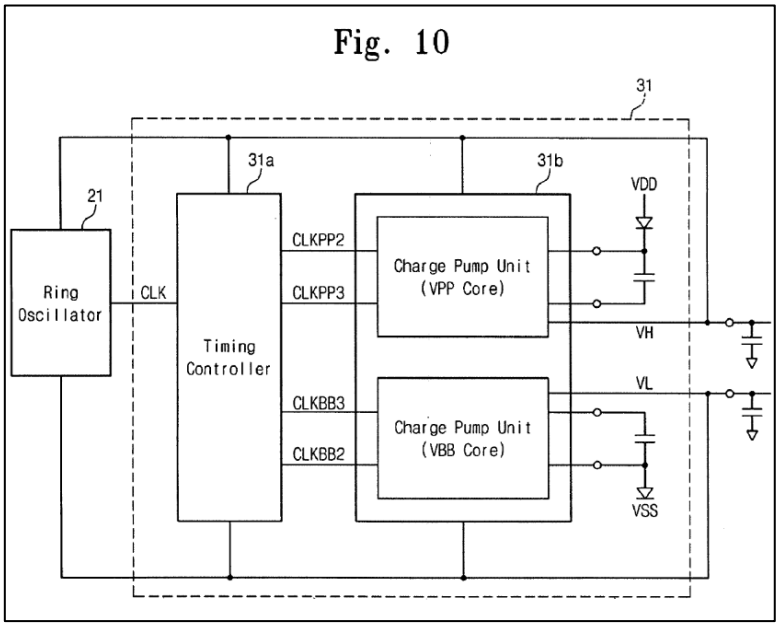


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

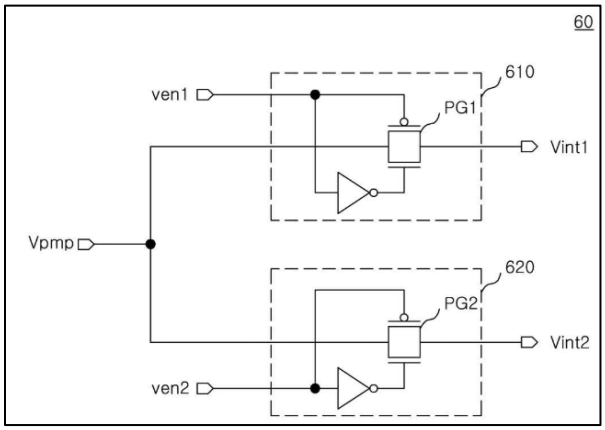
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

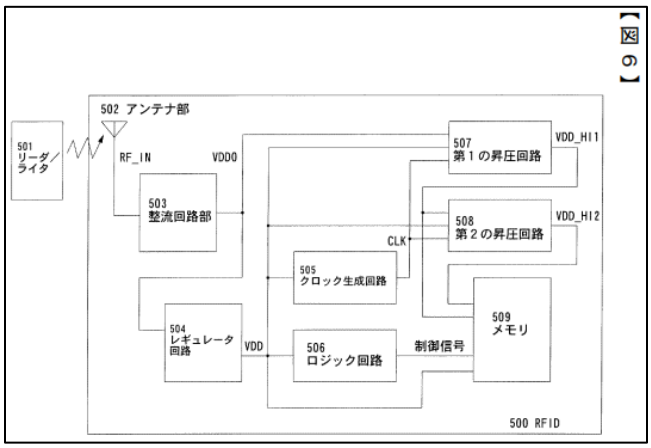
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

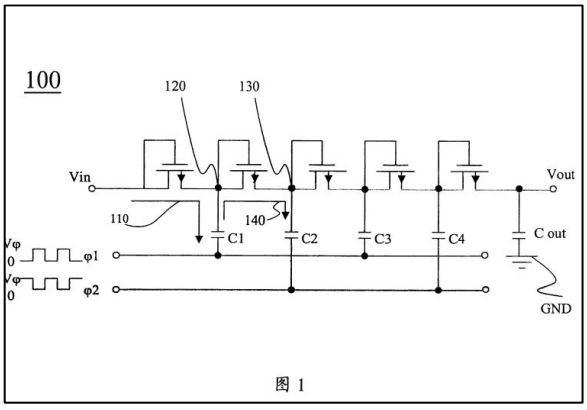
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

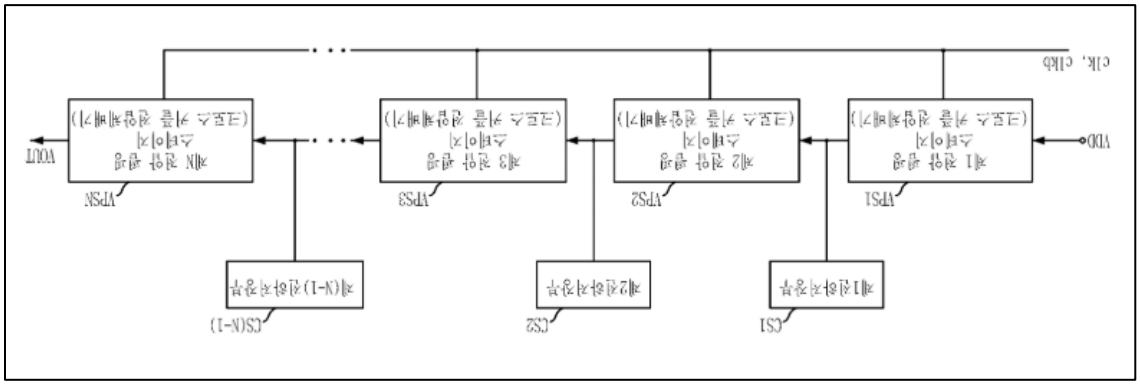
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

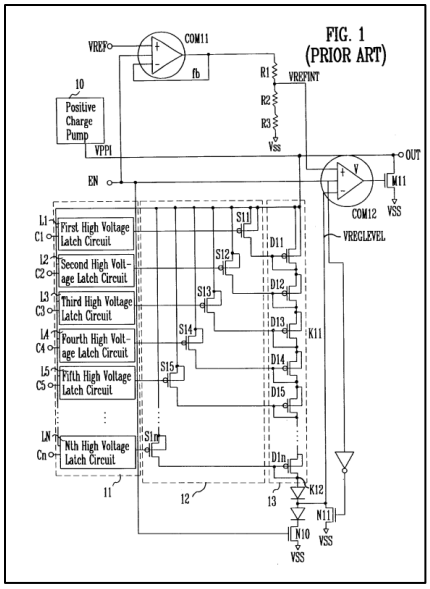
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



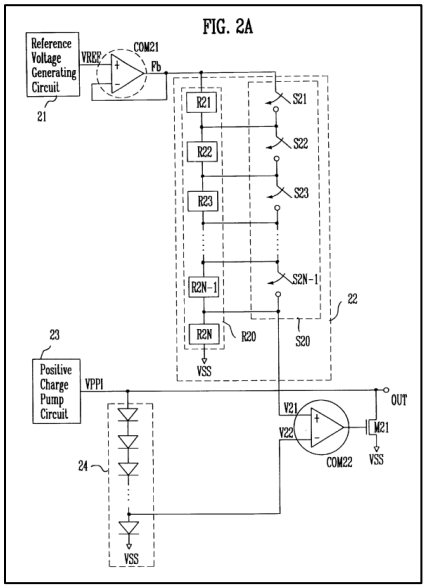
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

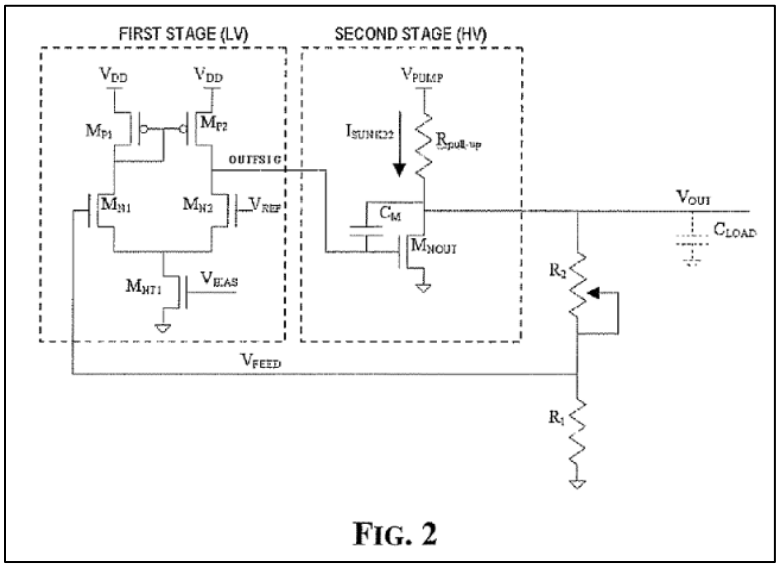


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

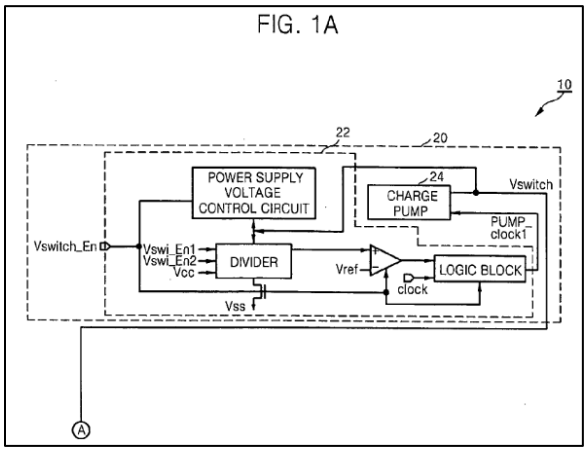
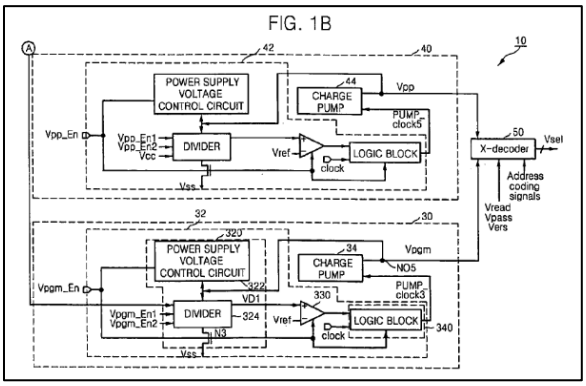
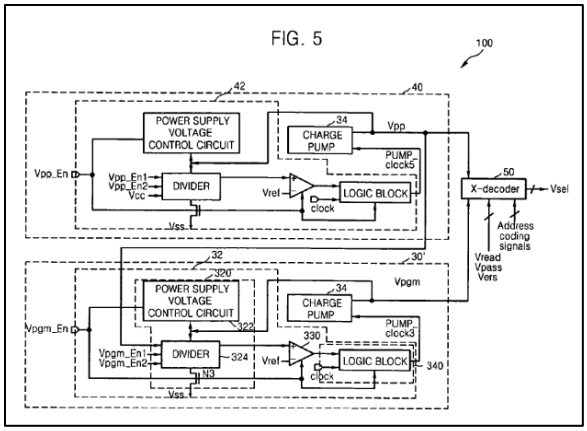


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

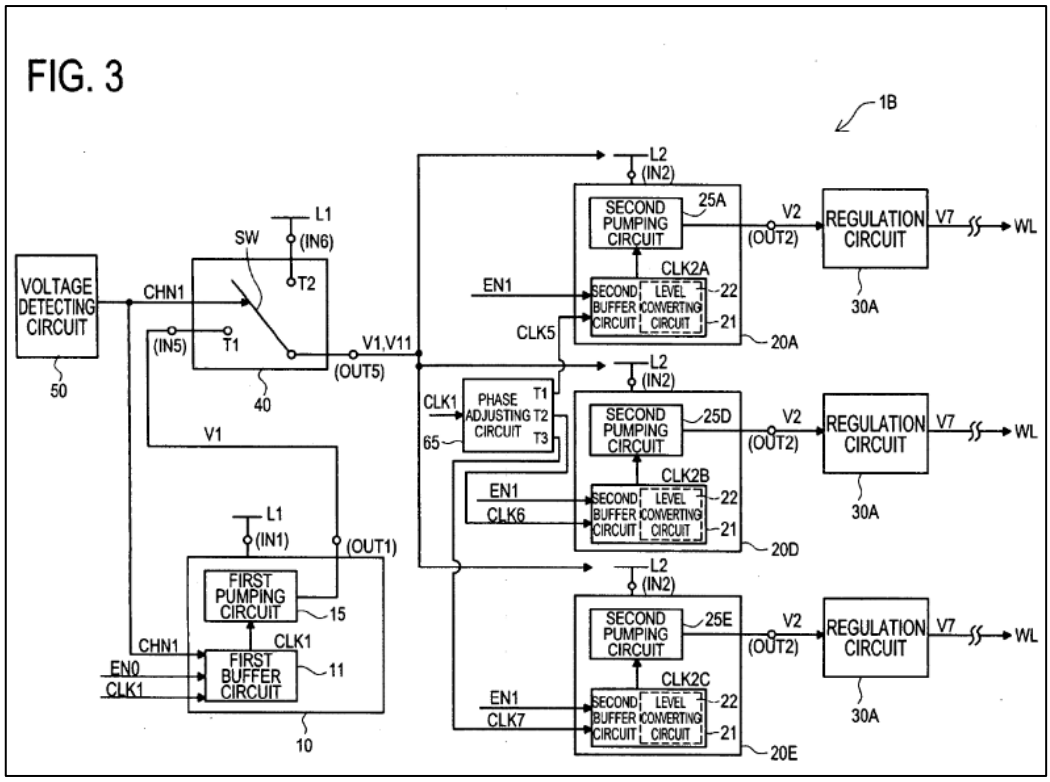
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

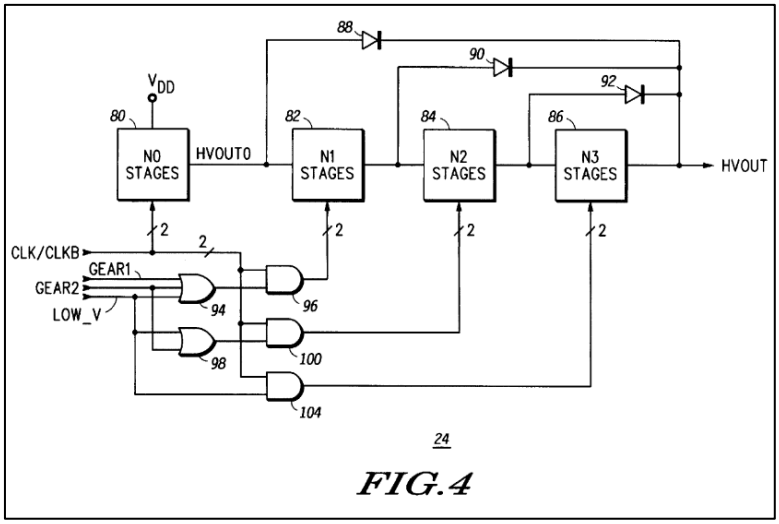


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[c] a second charge pump circuit configured to generate a third voltage from the second voltage;

The Omnibus References disclose and/or render obvious a second charge pump circuit configured to generate a third voltage from the second voltage.

See, e.g., claim limitation 1[c], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

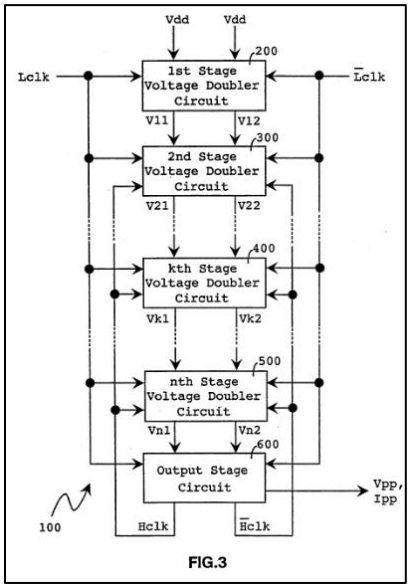


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

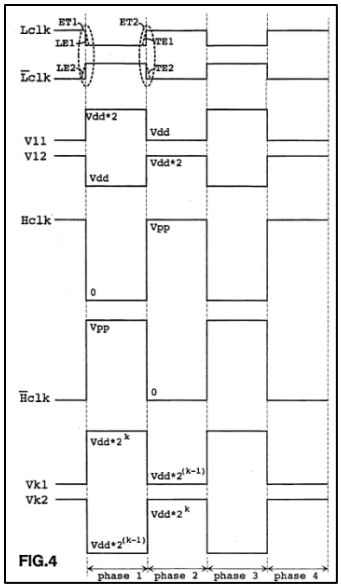


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

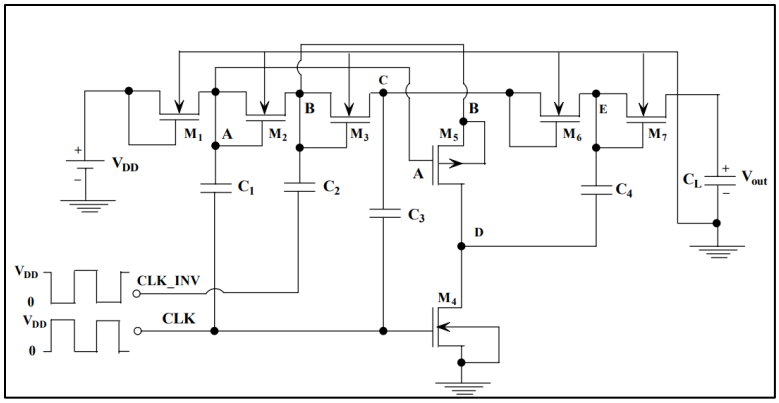
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

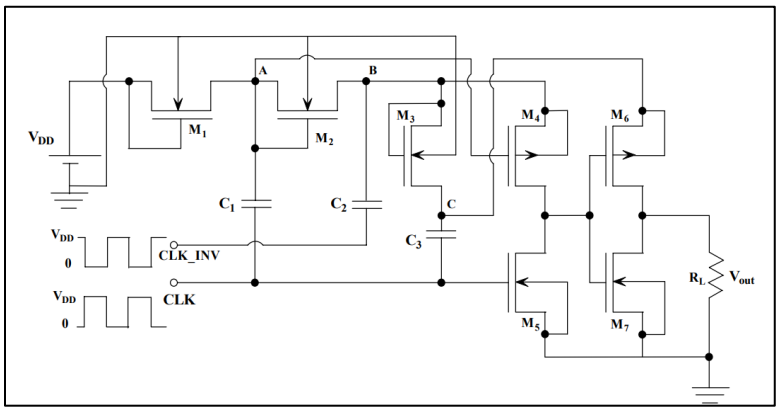
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

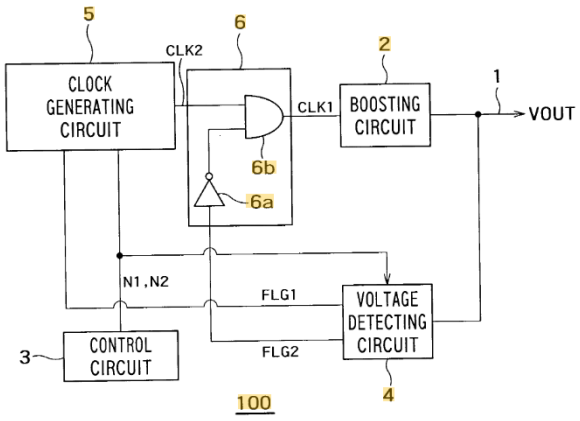


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

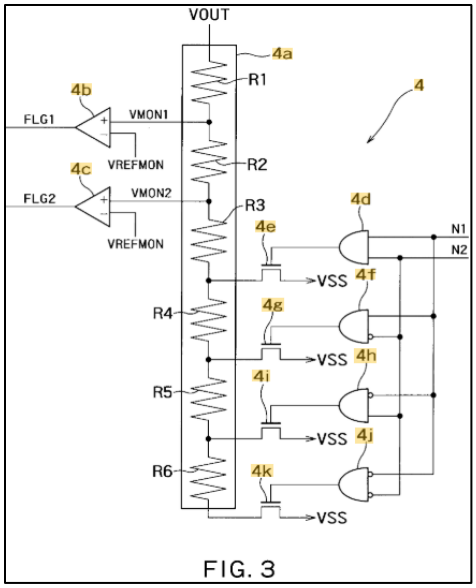


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

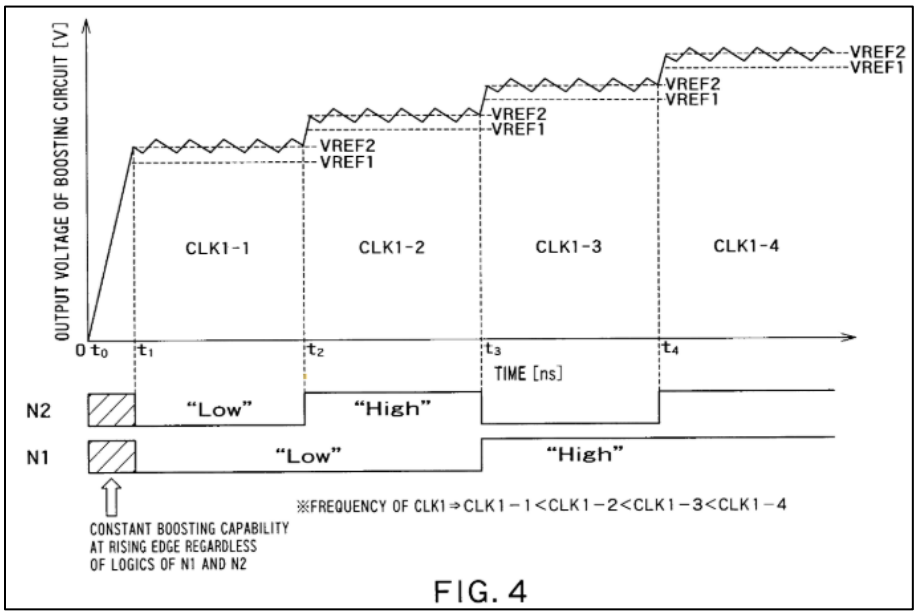


FIG. 4

Sato at [0051]:

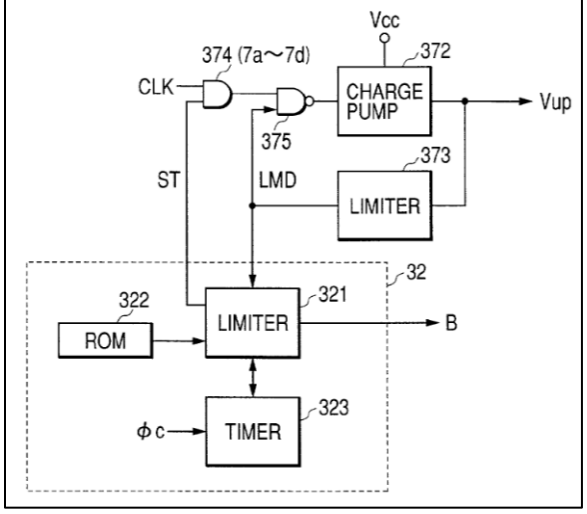
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

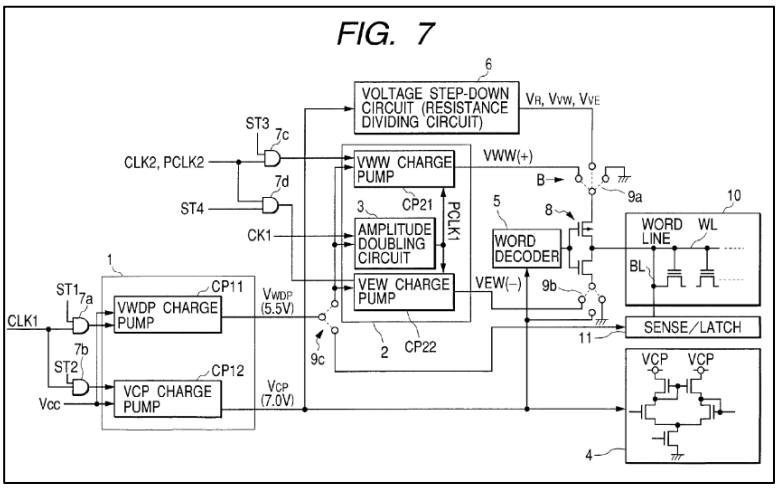
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

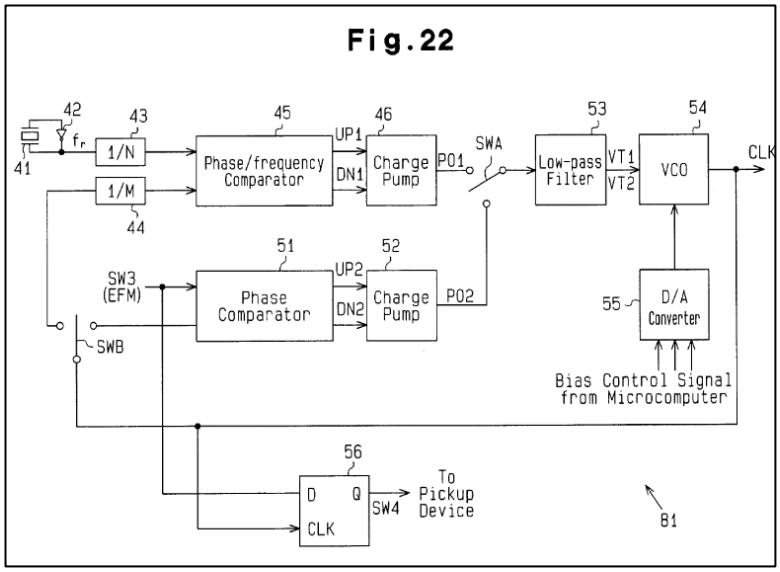
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

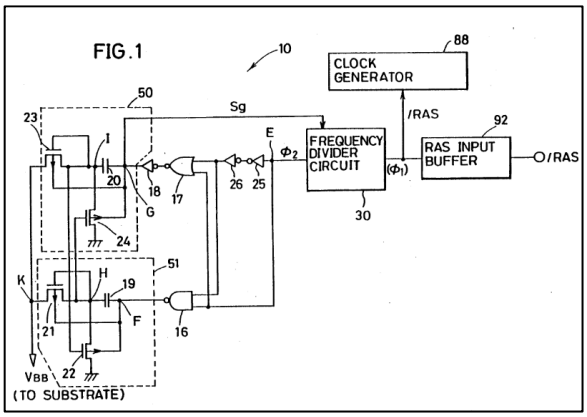


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

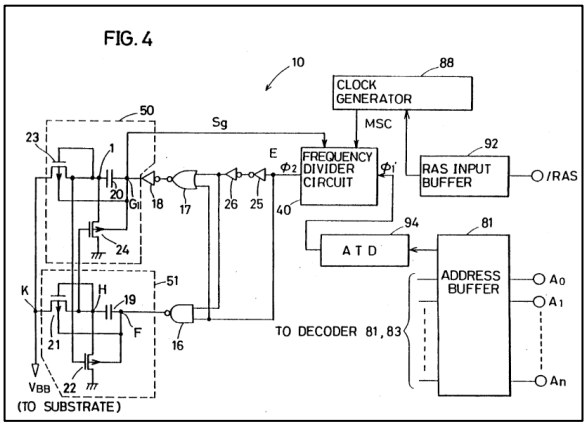
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

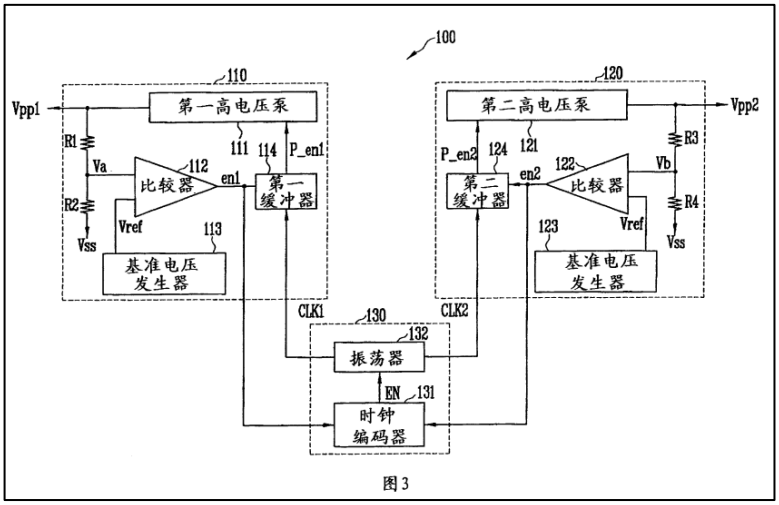


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

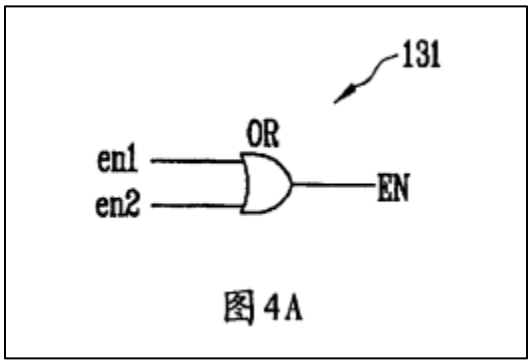


图 4A

Jiang at Fig. 6:

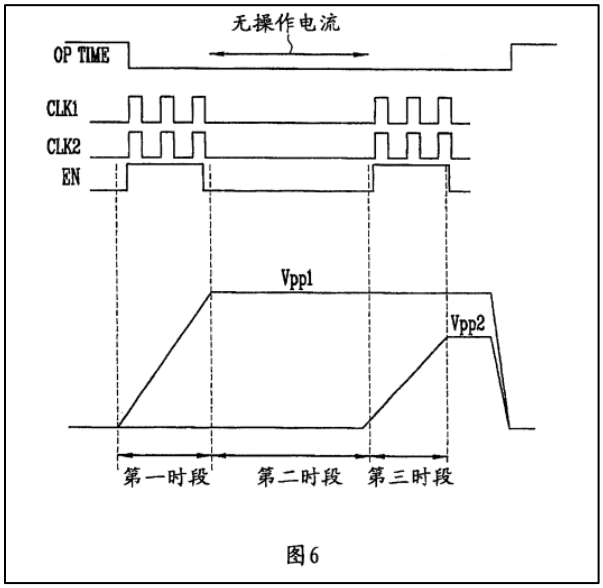
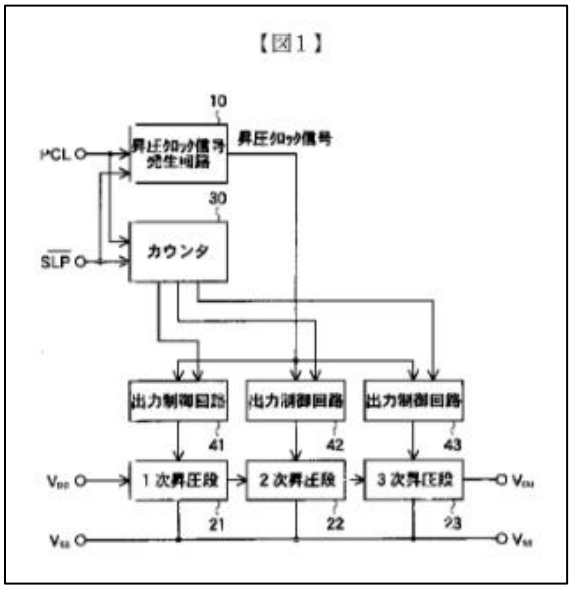


图6

Ito-633 at [0018] and Fig. 1:

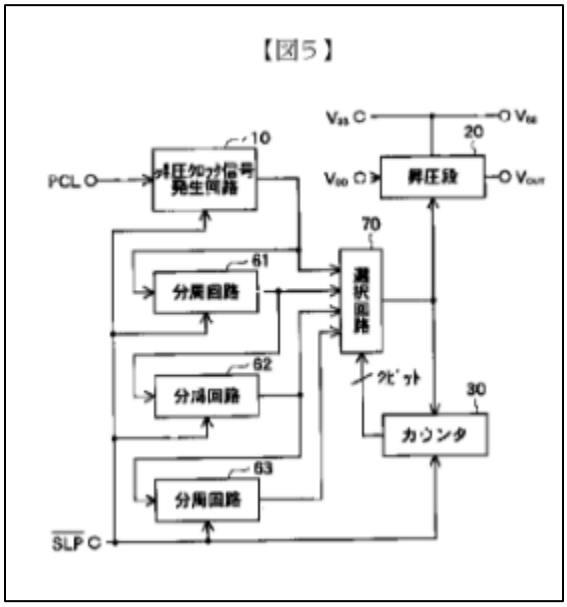
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

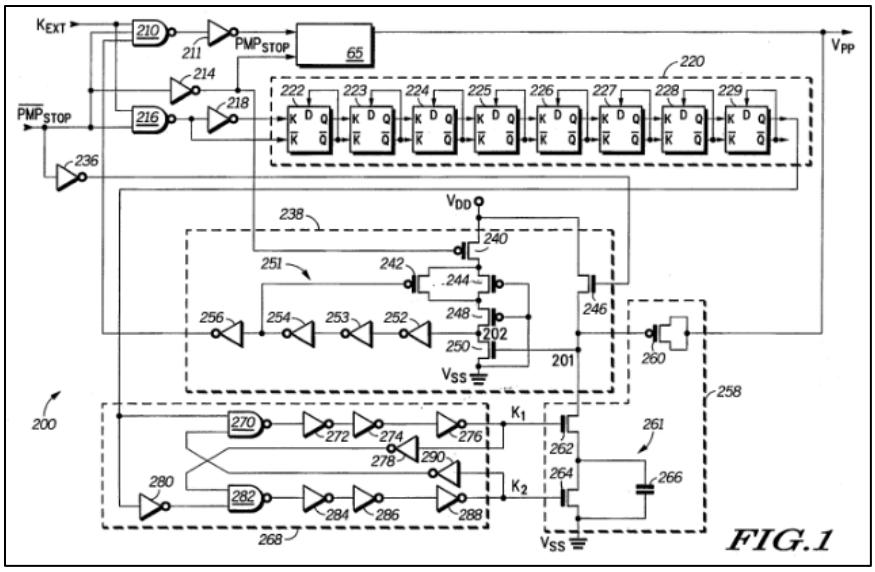


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

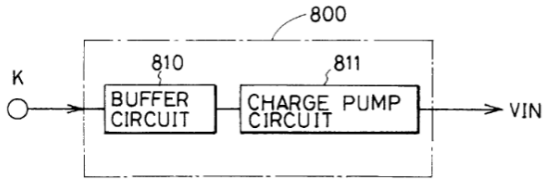


FIG.57

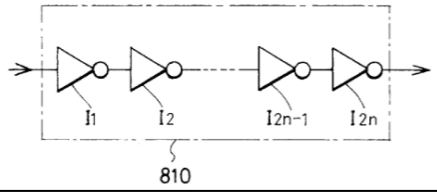


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

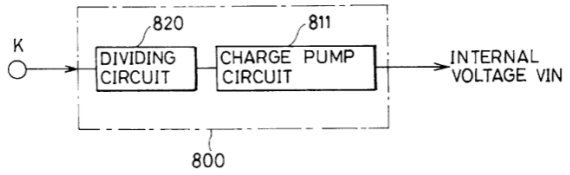
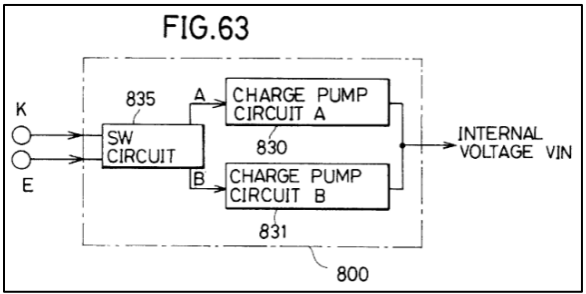


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

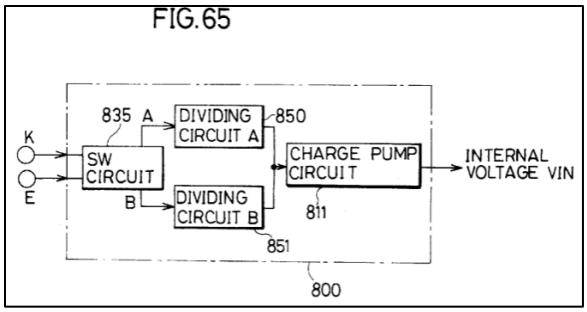
Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.

FIG.65



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

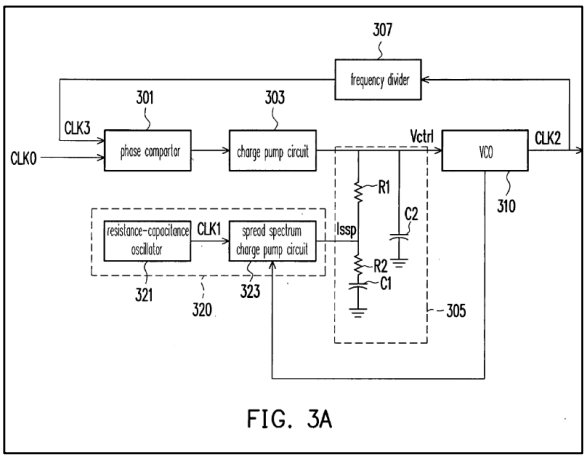


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

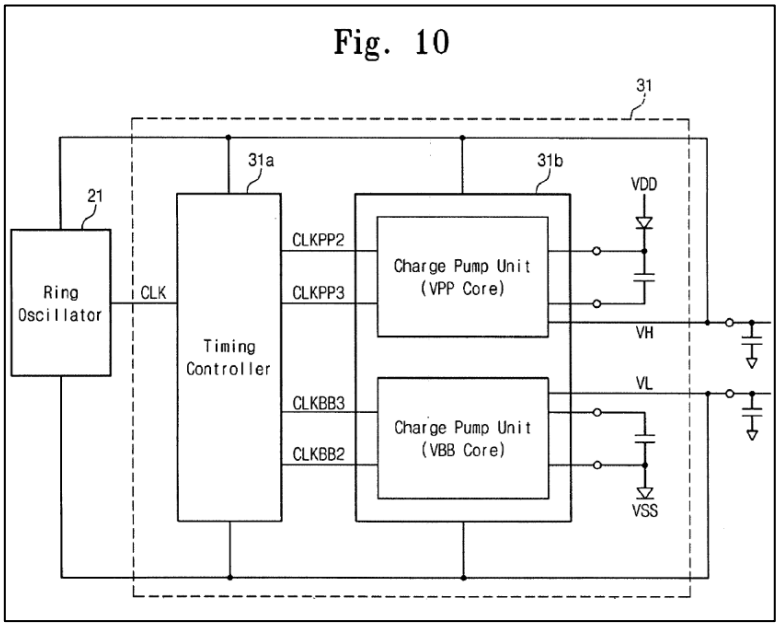


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

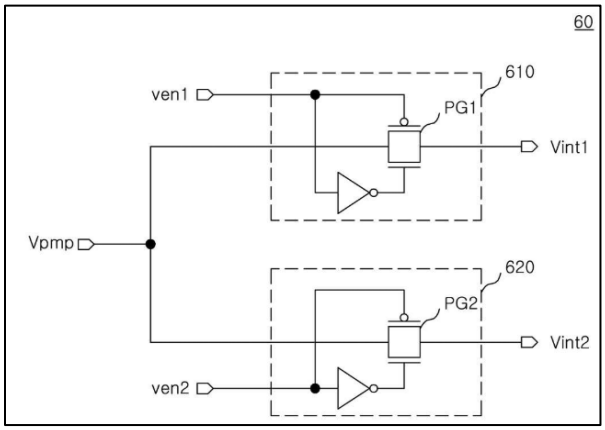
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

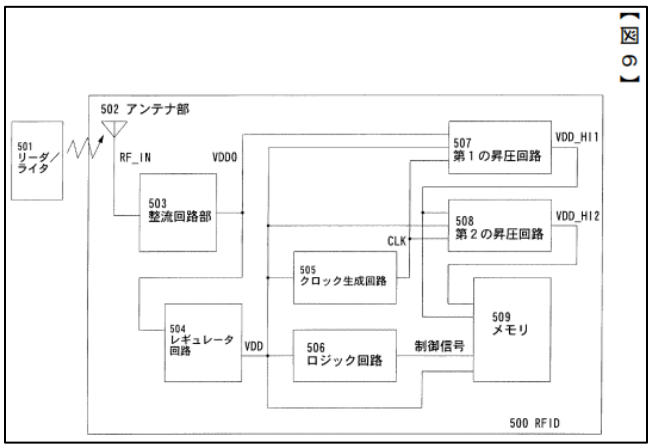
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

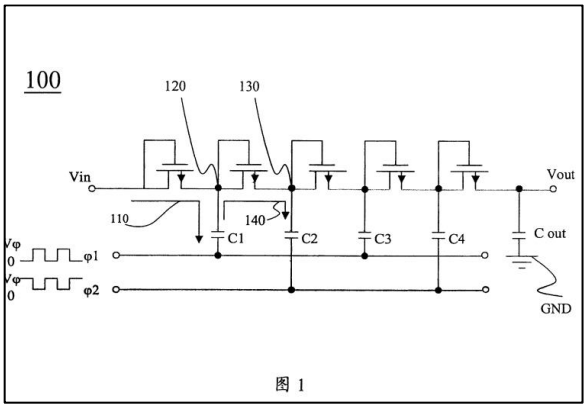
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

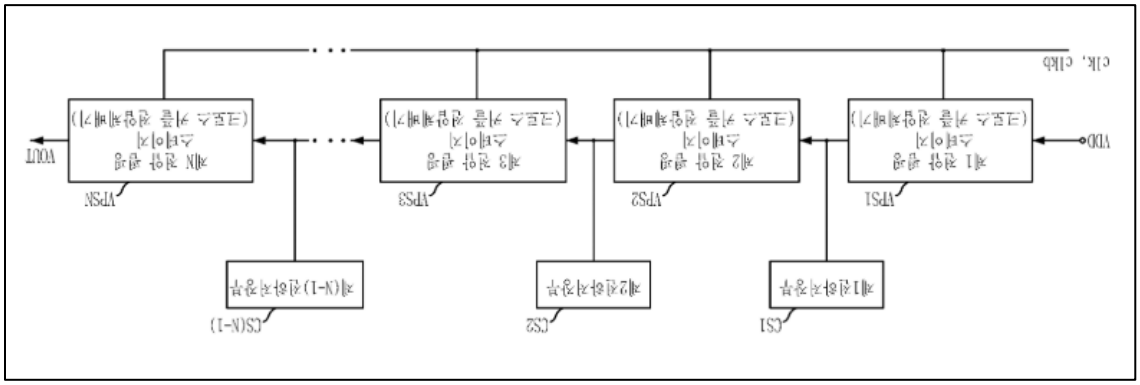
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

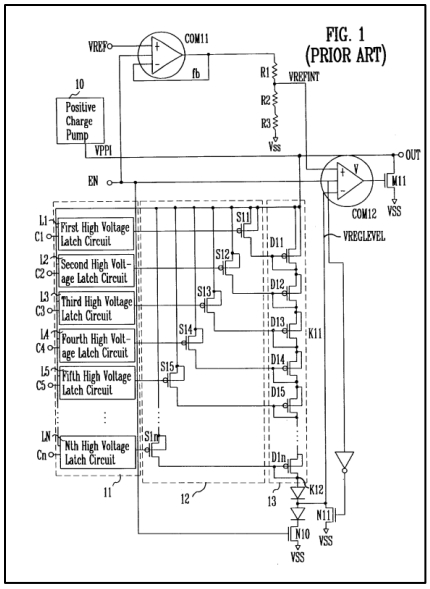
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



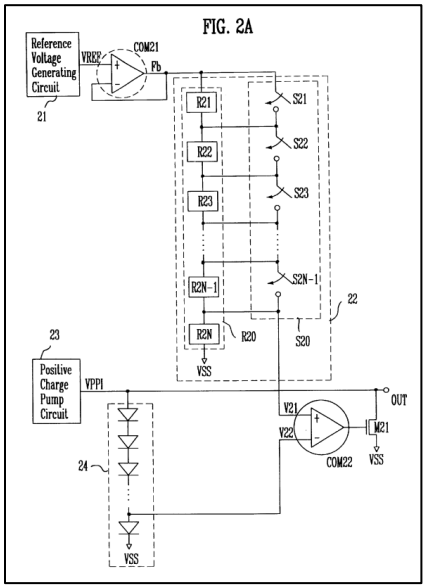
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

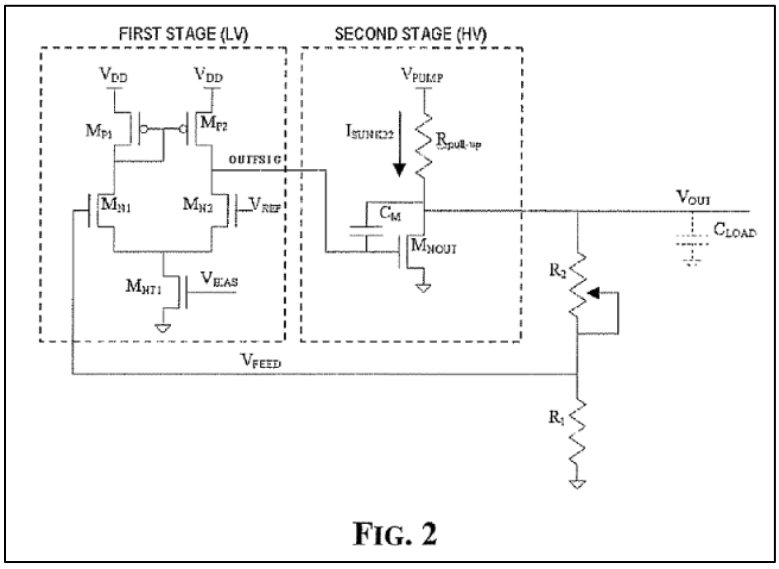


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

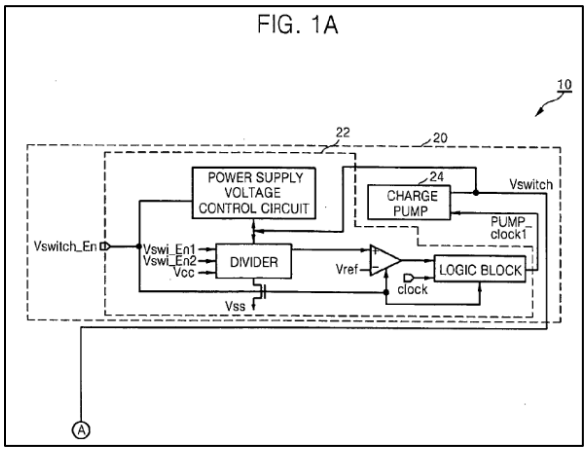
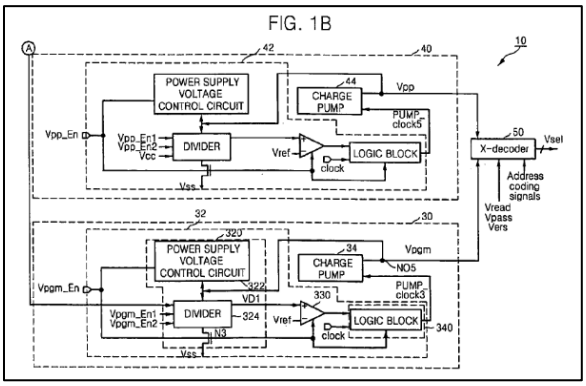
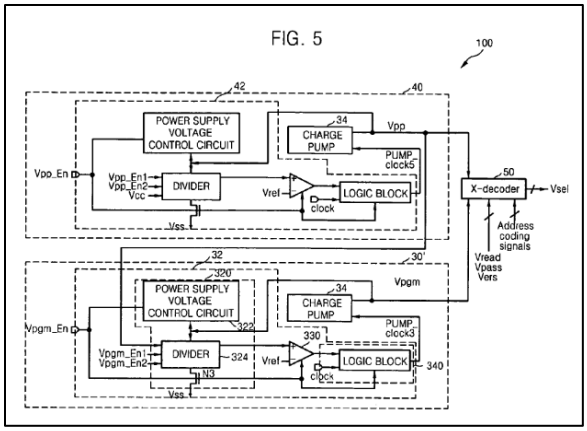


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

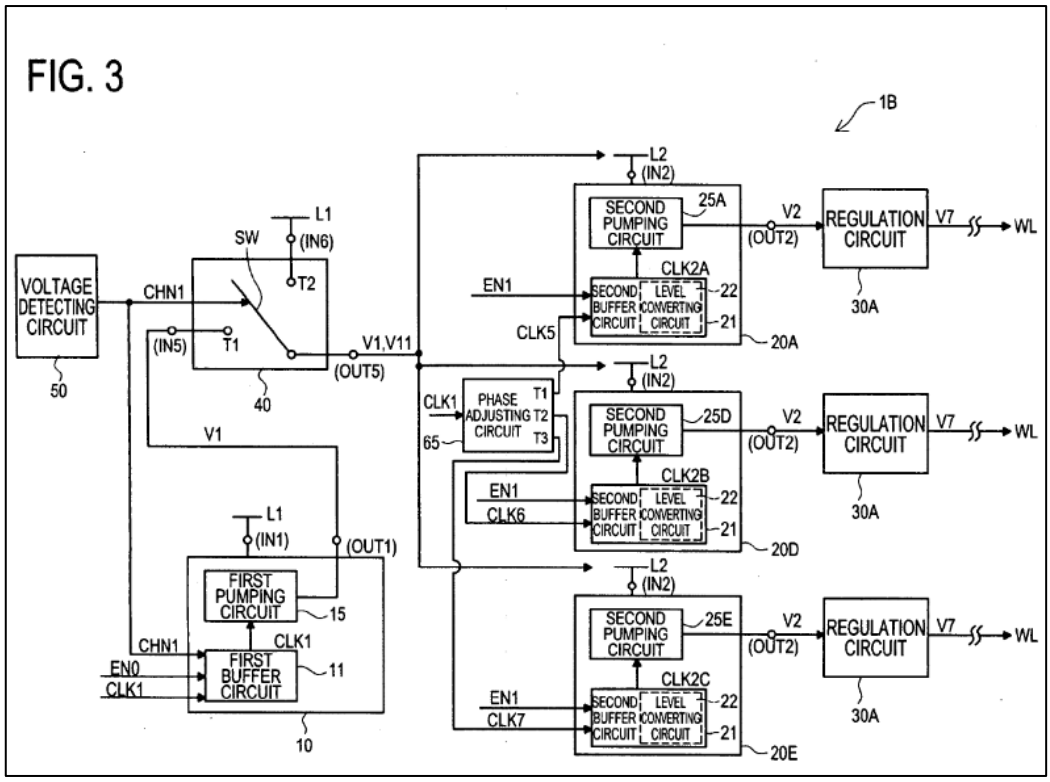
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

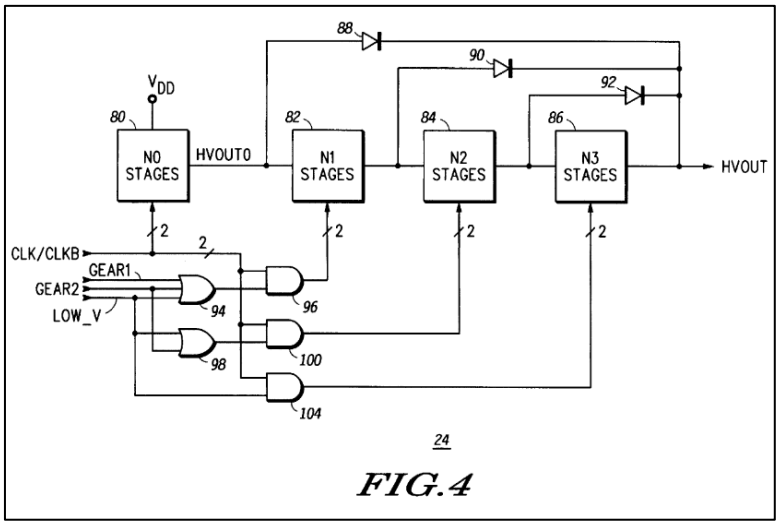


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[d] a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and

The Omnibus References disclose and/or render obvious a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal.

See, e.g., claim limitation 1[d], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

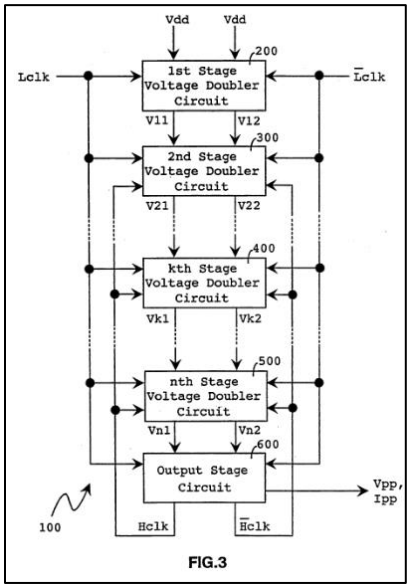


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

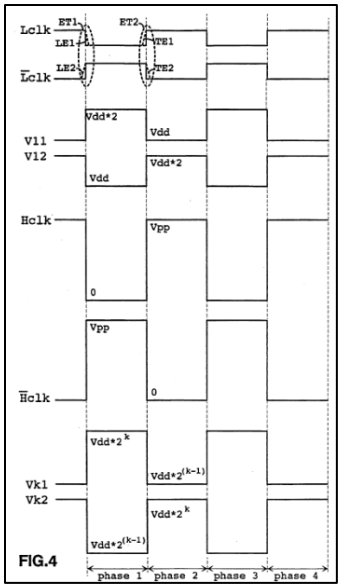


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

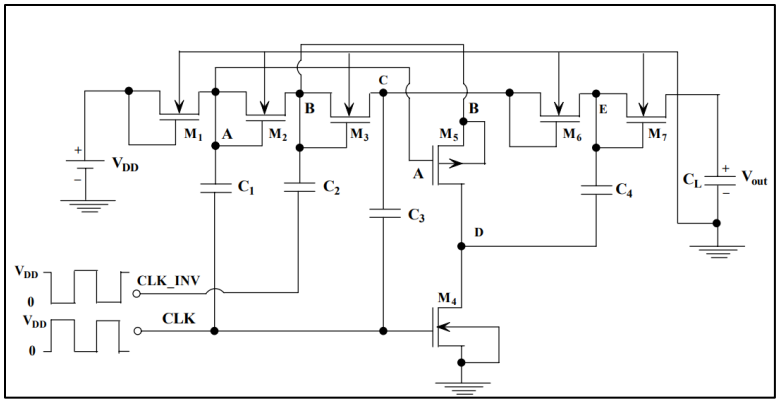
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

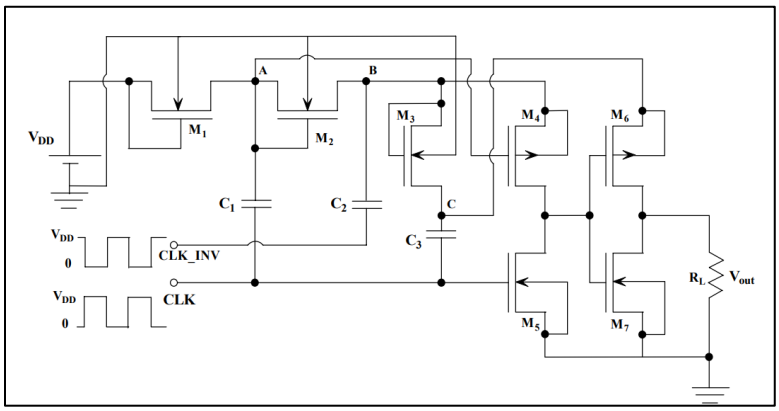
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

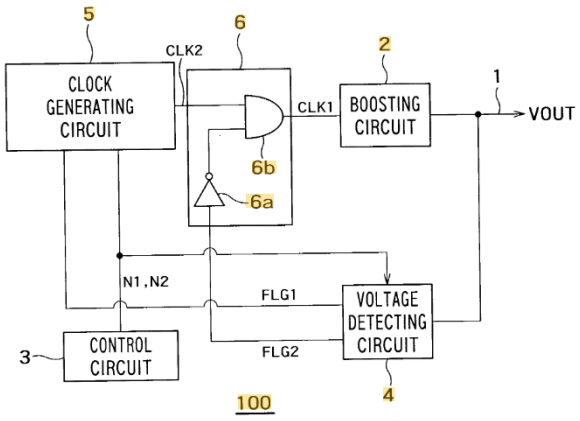


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

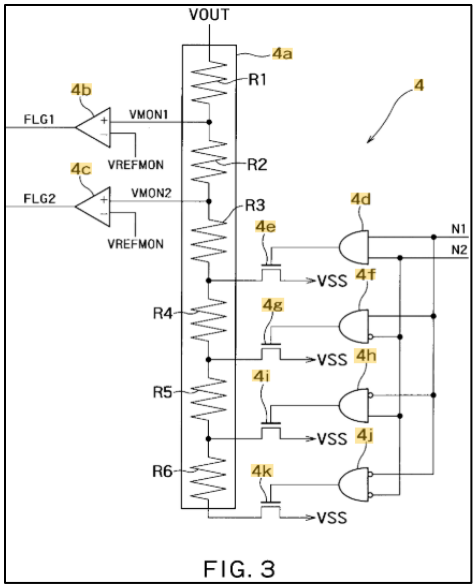


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

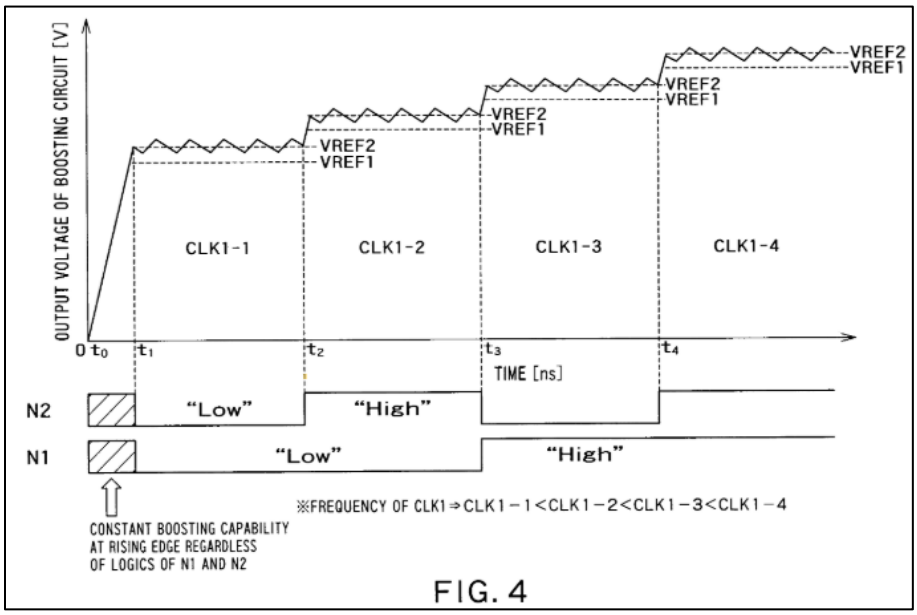


FIG. 4

Sato at [0051]:

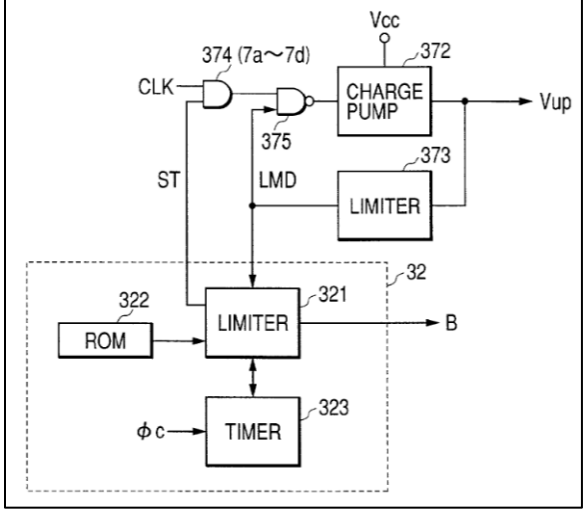
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

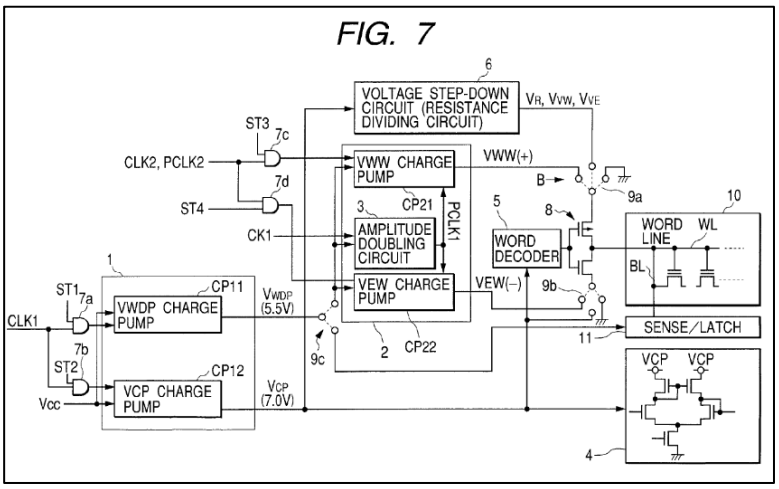
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

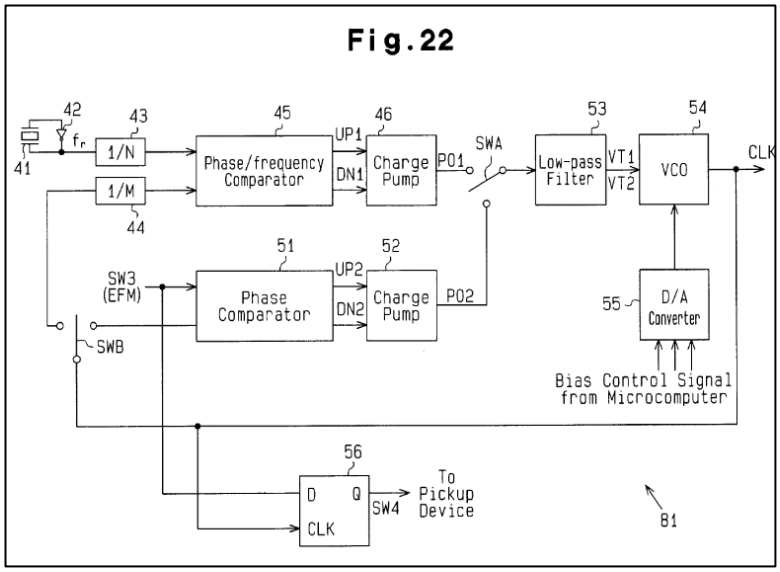
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

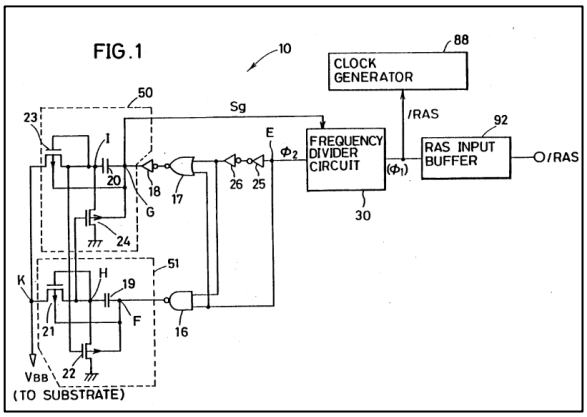


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

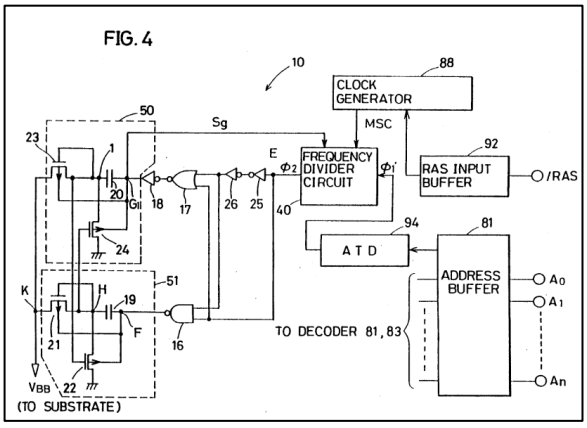
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

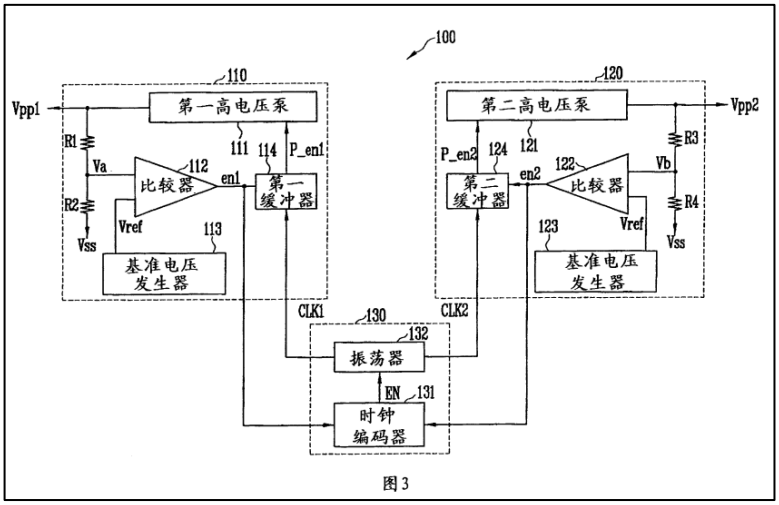


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

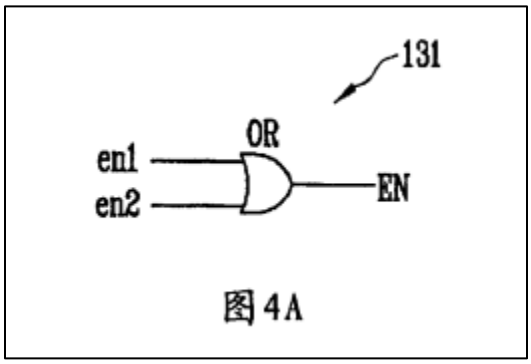


图 4A

Jiang at Fig. 6:

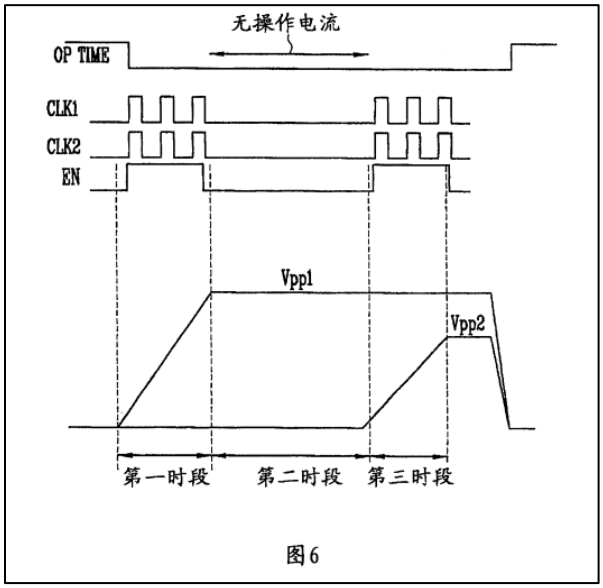
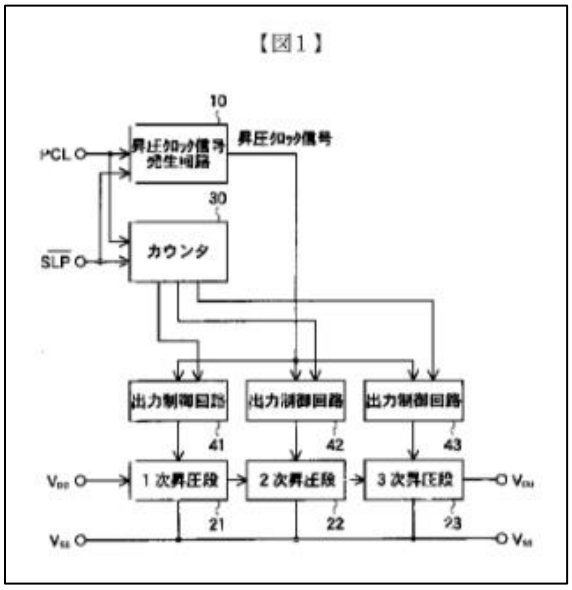


图6

Ito-633 at [0018] and Fig. 1:

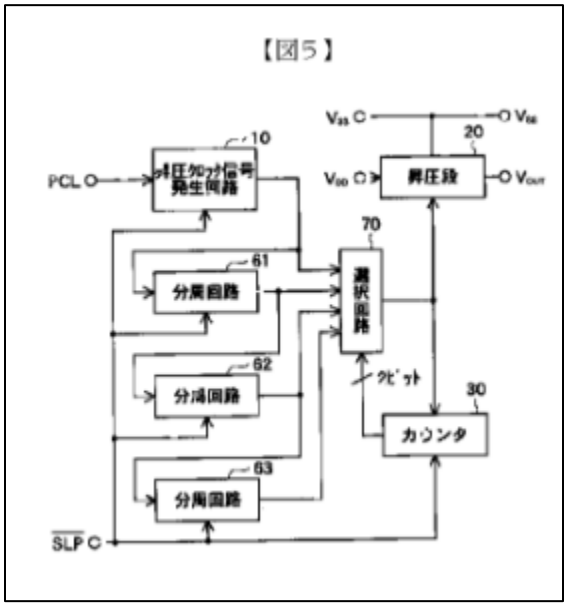
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as “boost clock signal”) based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

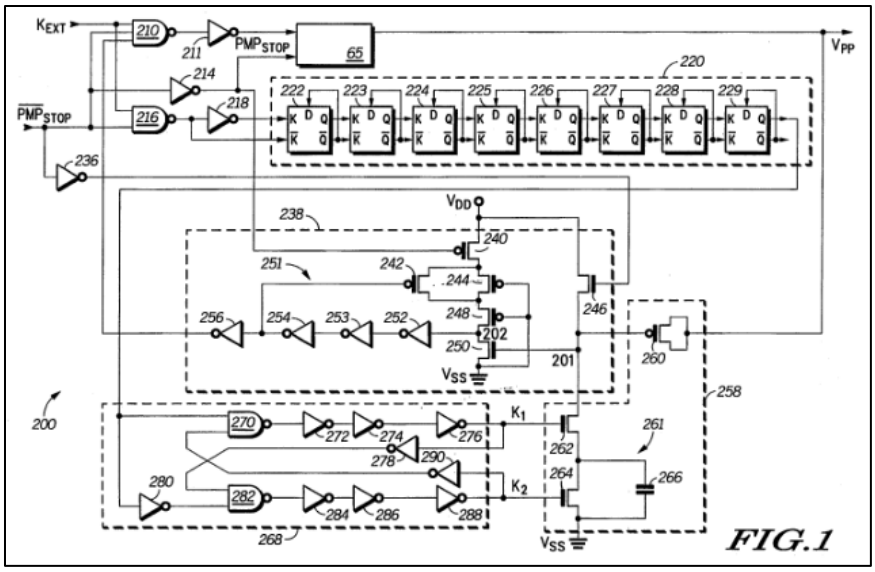


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

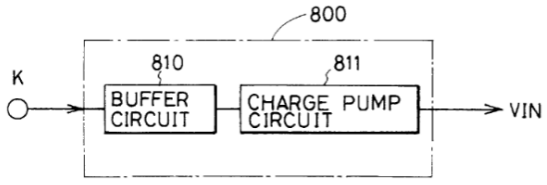


FIG.57

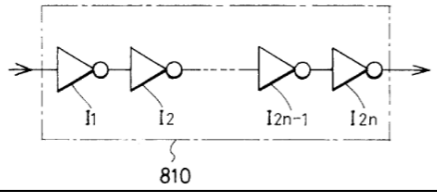


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

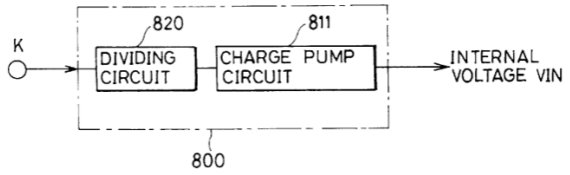
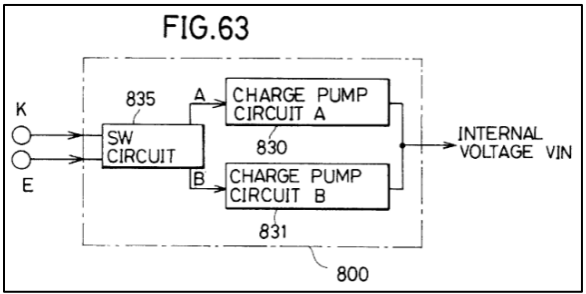


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



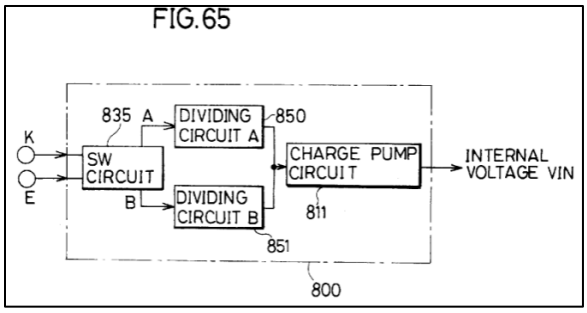
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

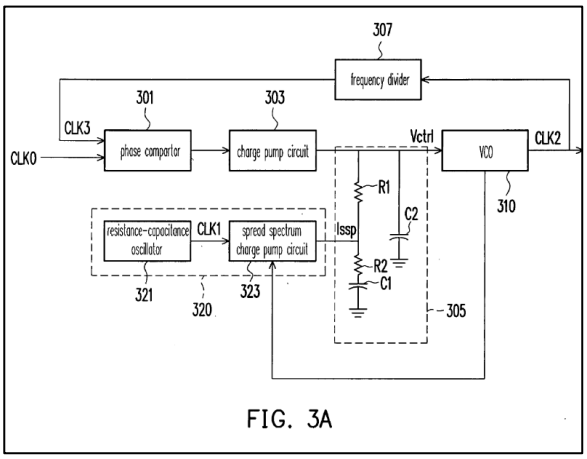


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

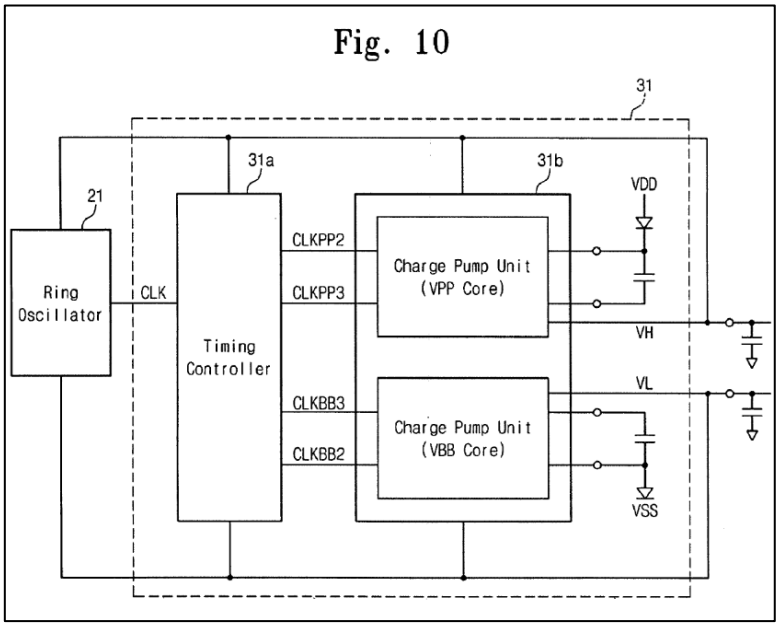


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

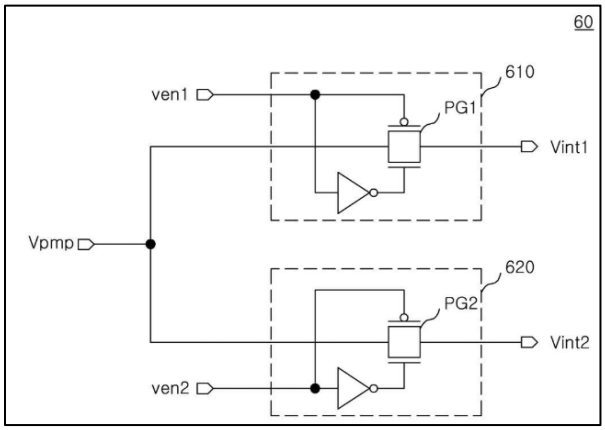
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

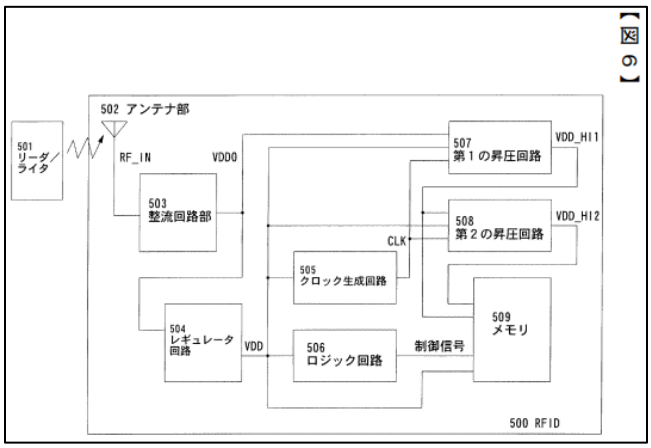
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

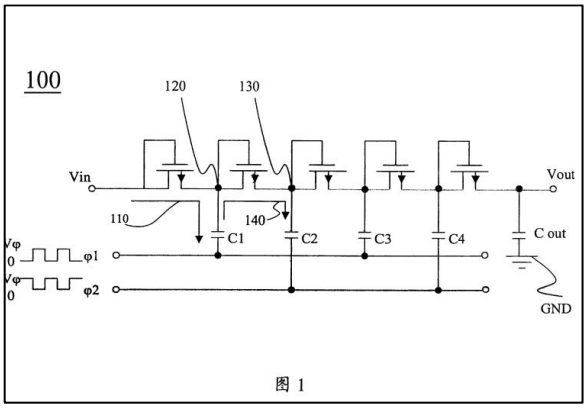
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

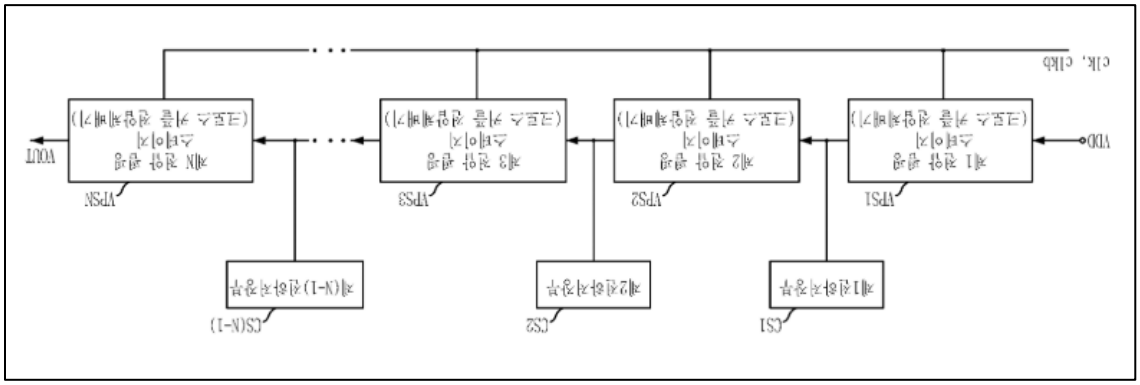
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

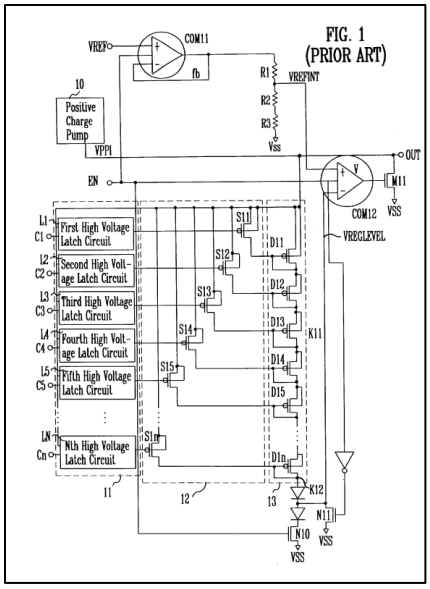
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



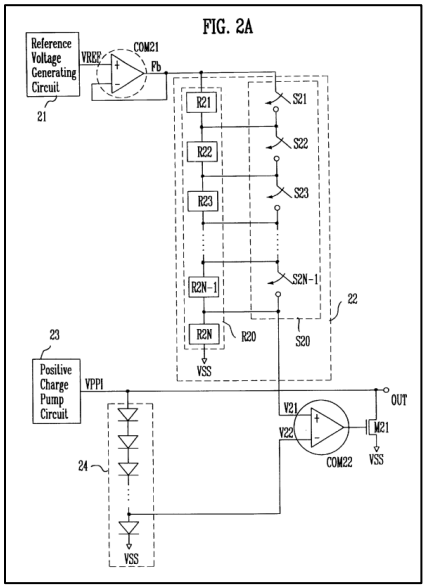
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

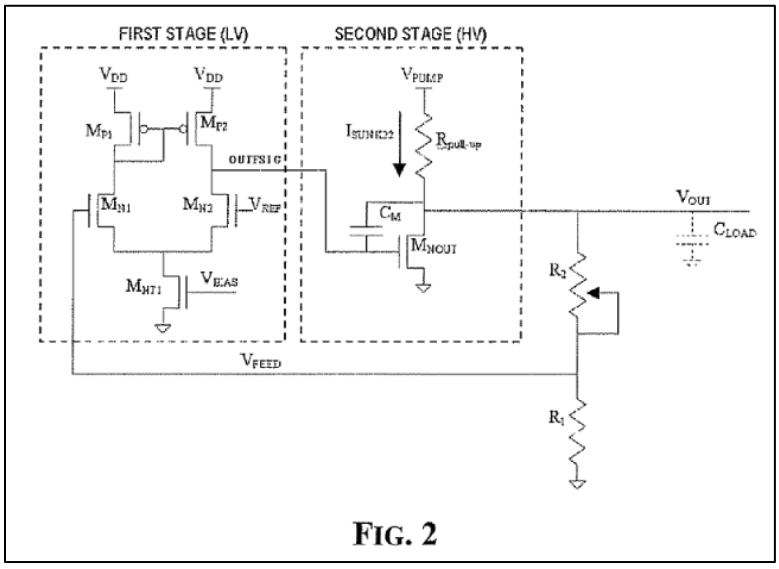


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

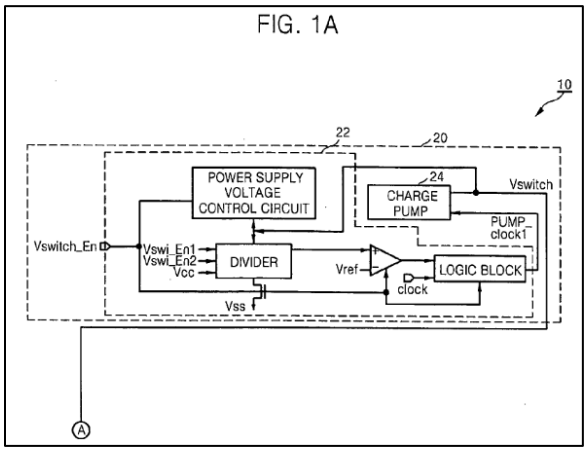
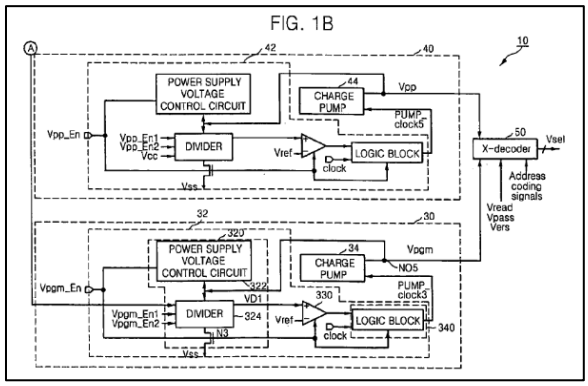
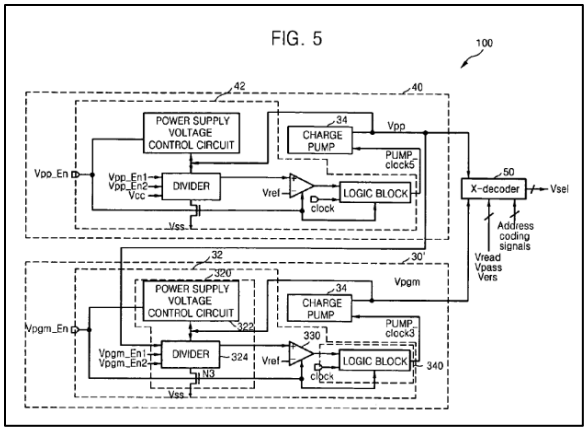


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

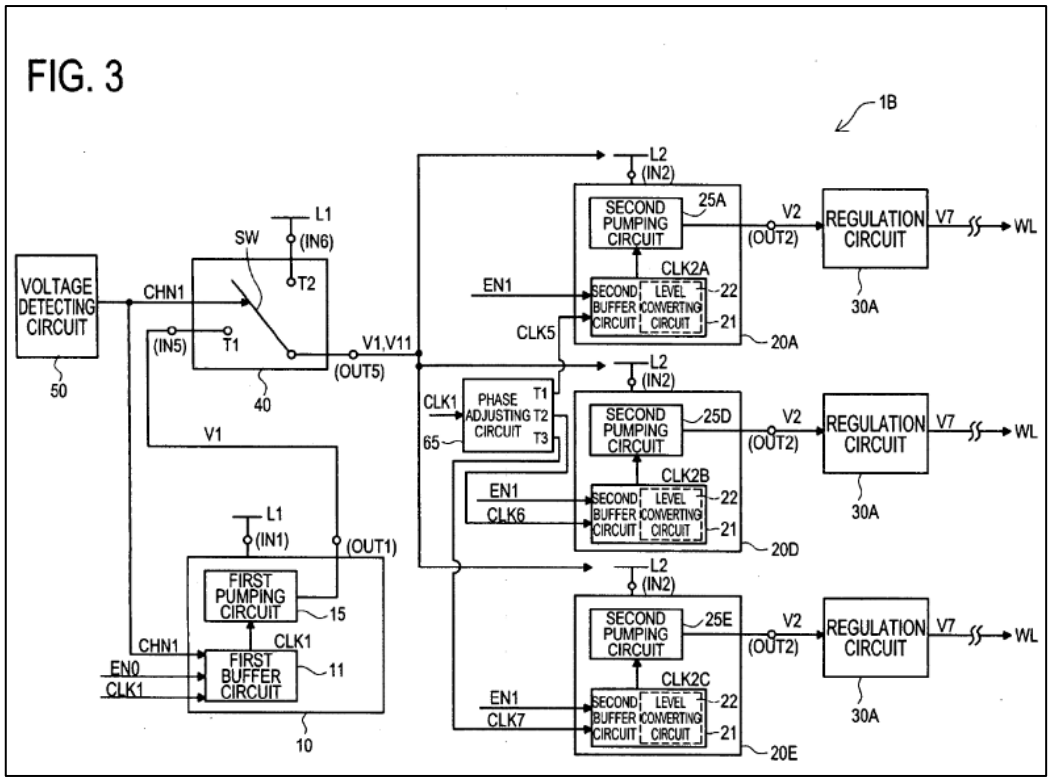
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

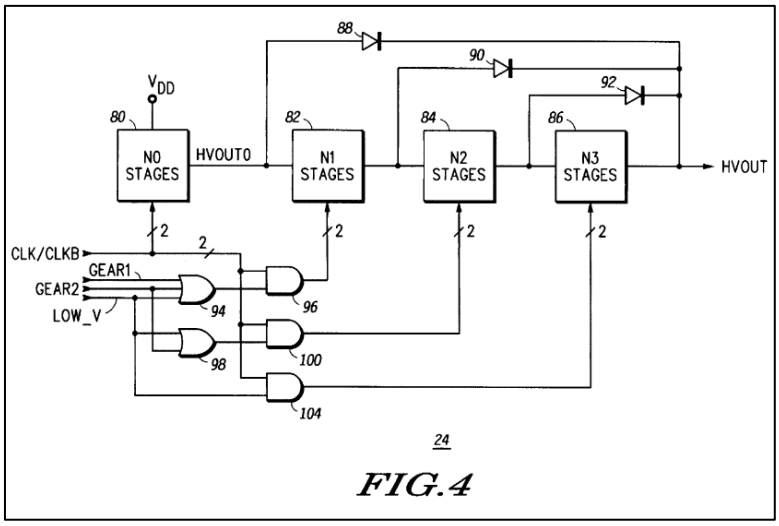


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[e] a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal,

The Omnibus References disclose and/or render obvious a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal.

See, e.g., claim limitation 1[e], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

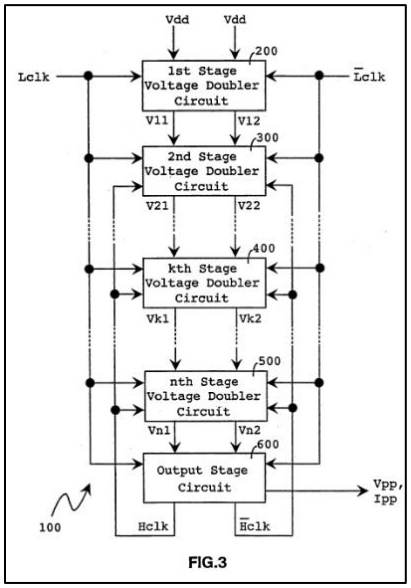


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

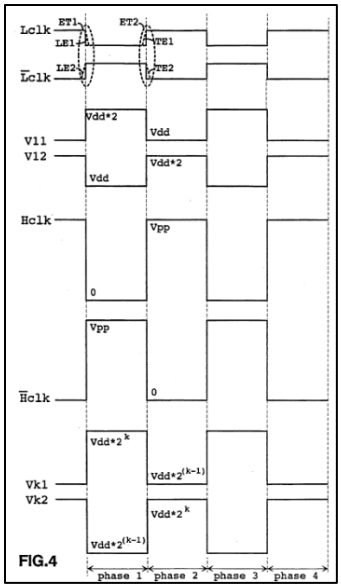


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

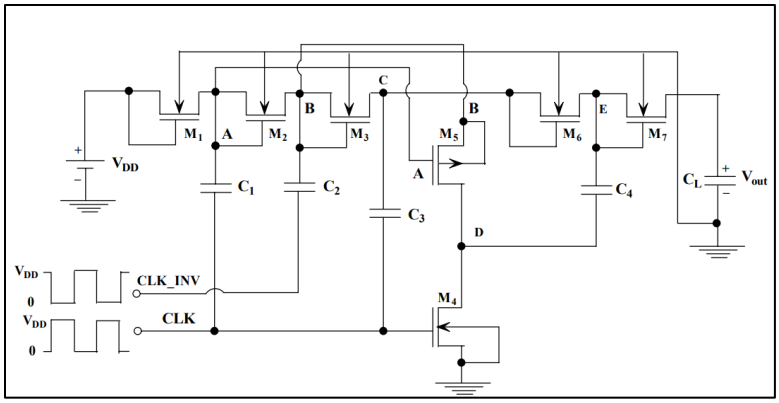
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

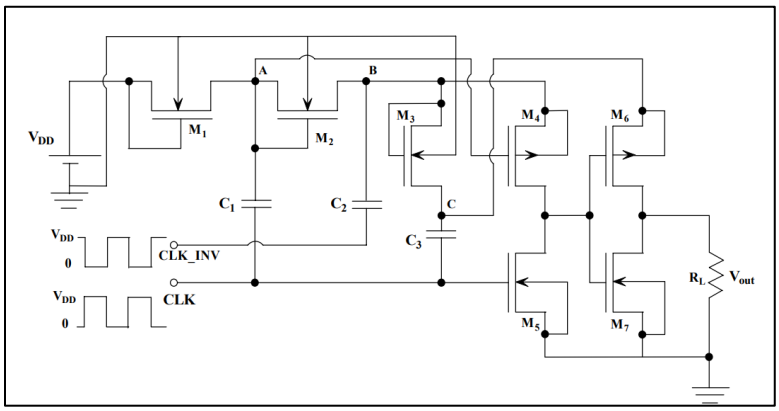
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

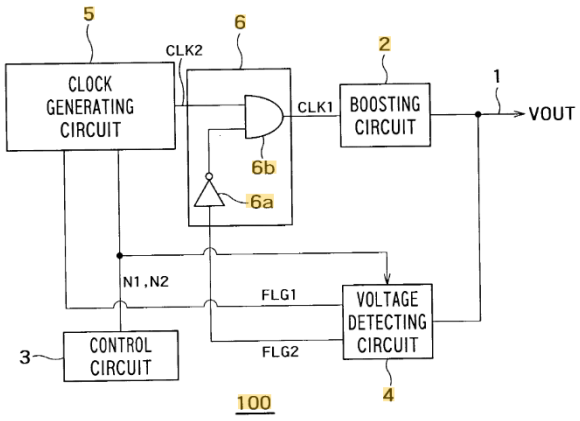


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

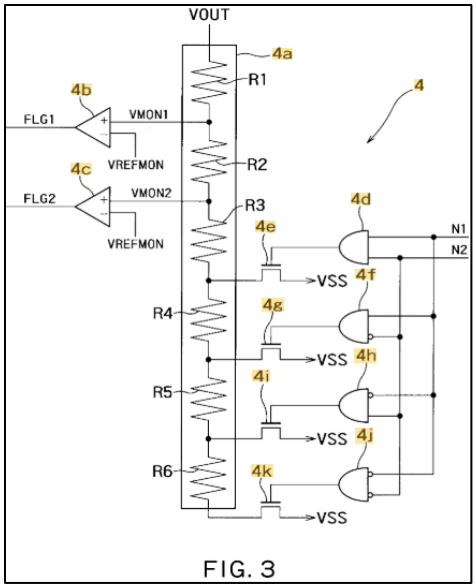


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

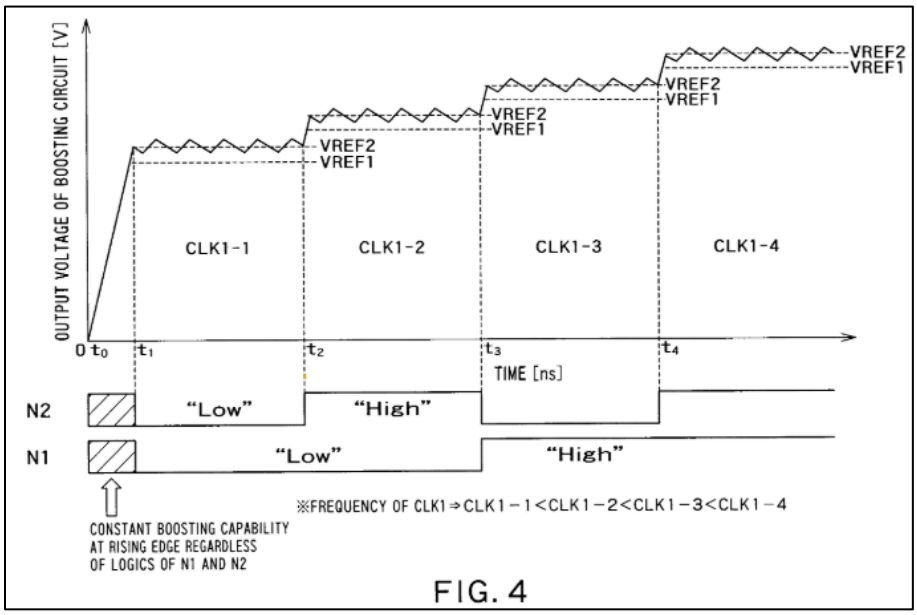


FIG. 4

Sato at [0051]:

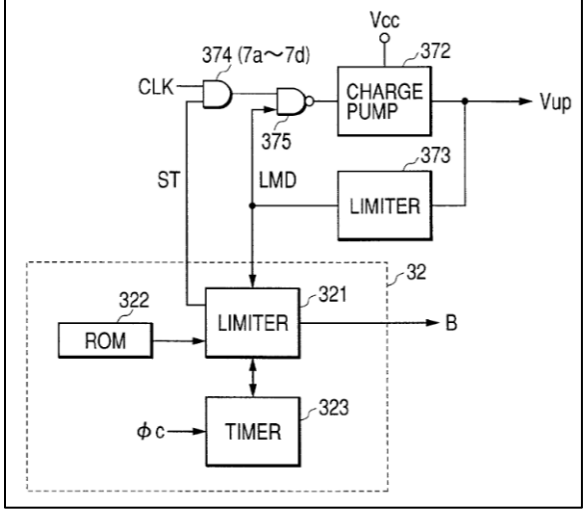
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

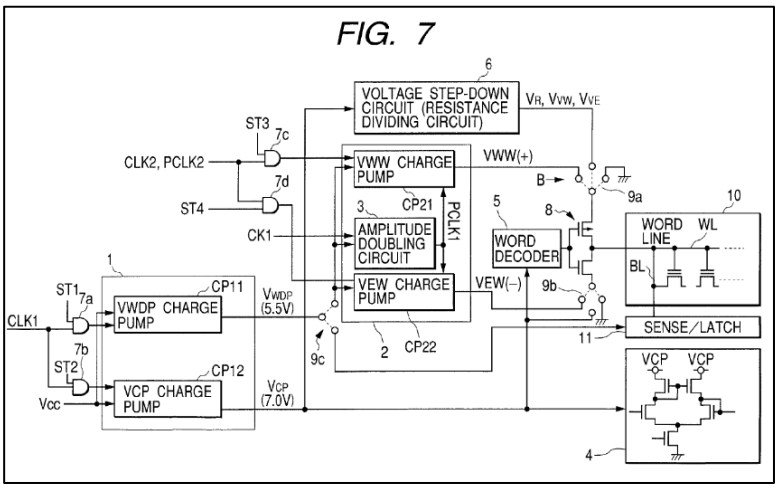
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

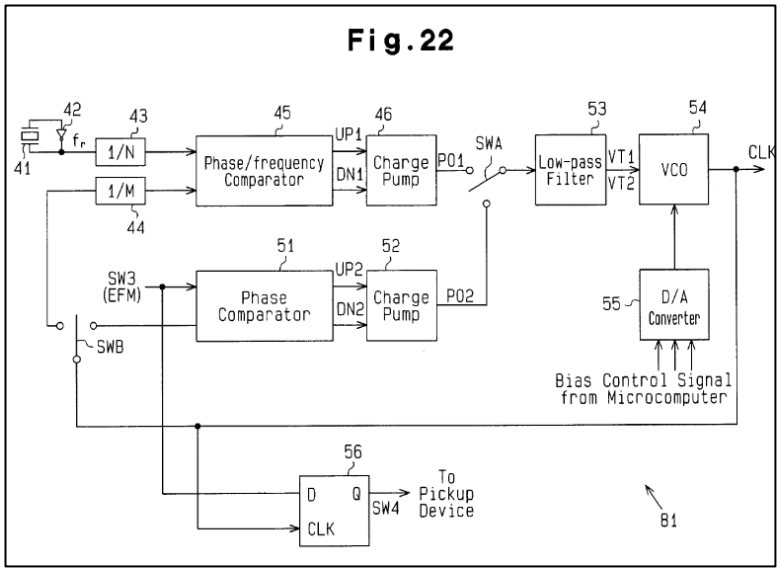
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

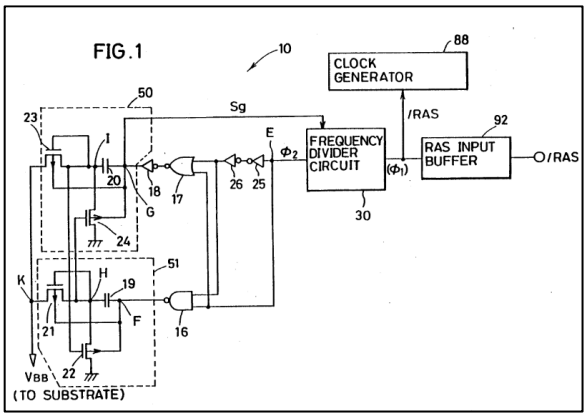


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

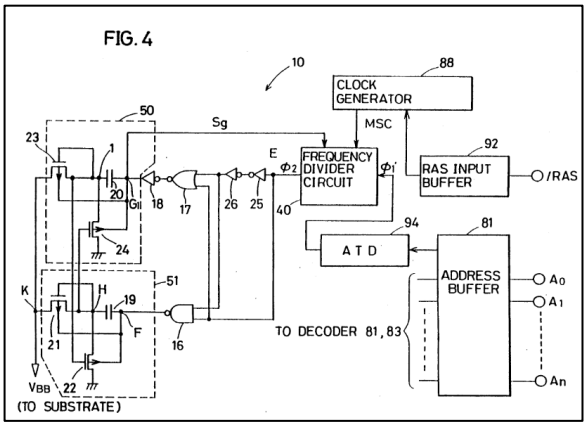
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

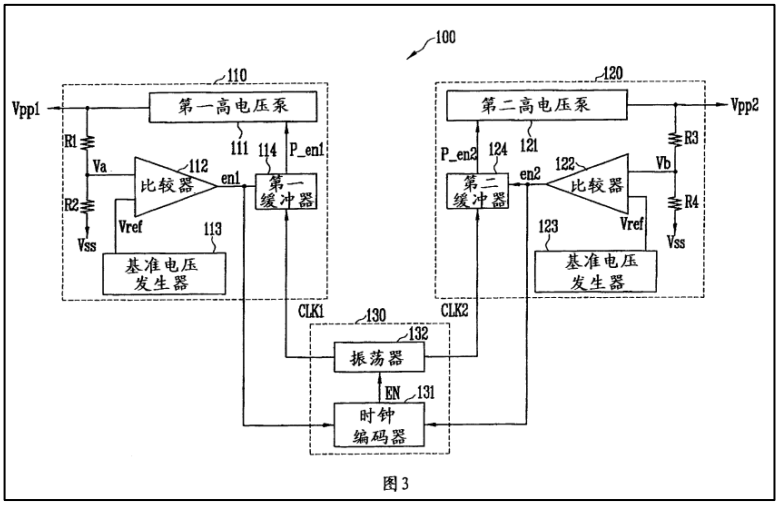


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

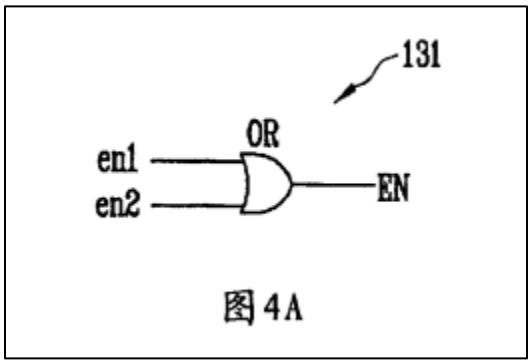


图 4A

Jiang at Fig. 6:

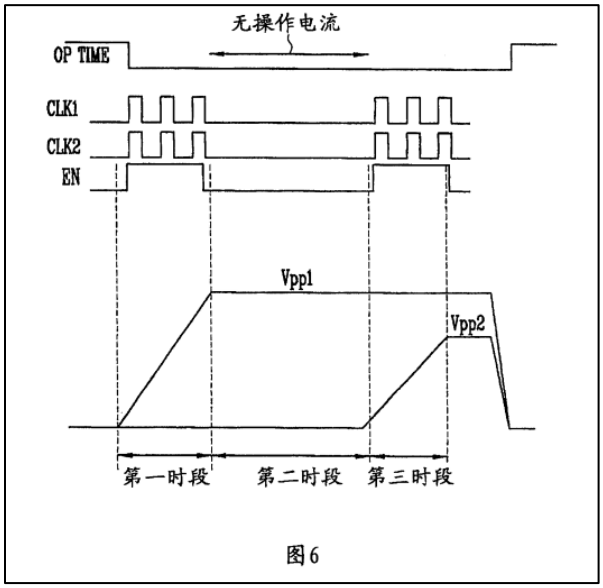
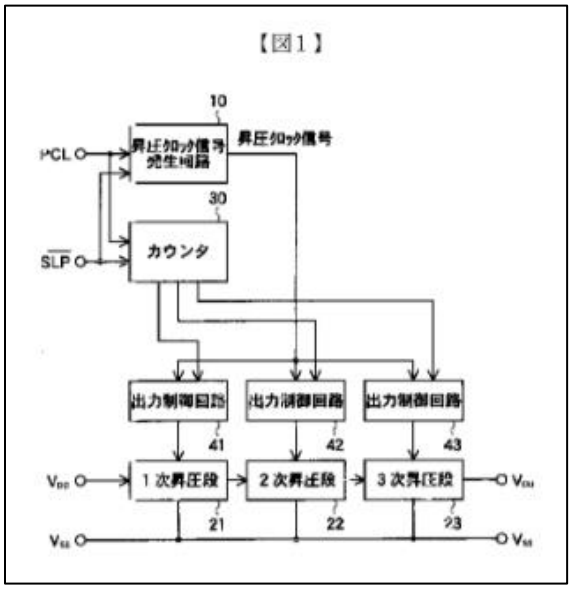


图 6

Ito-633 at [0018] and Fig. 1:

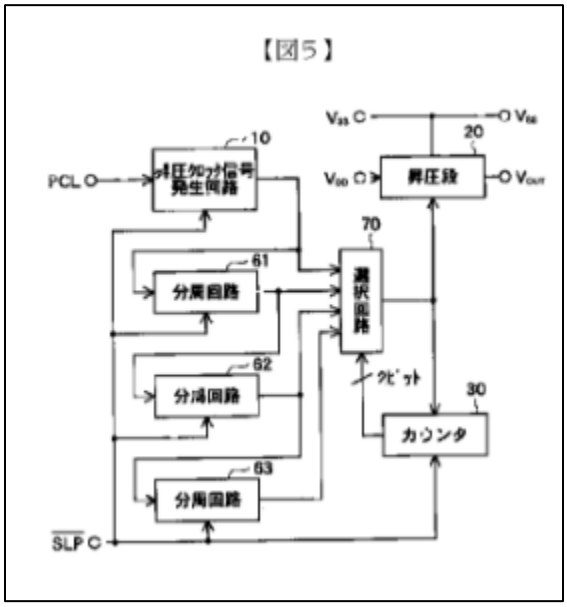
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

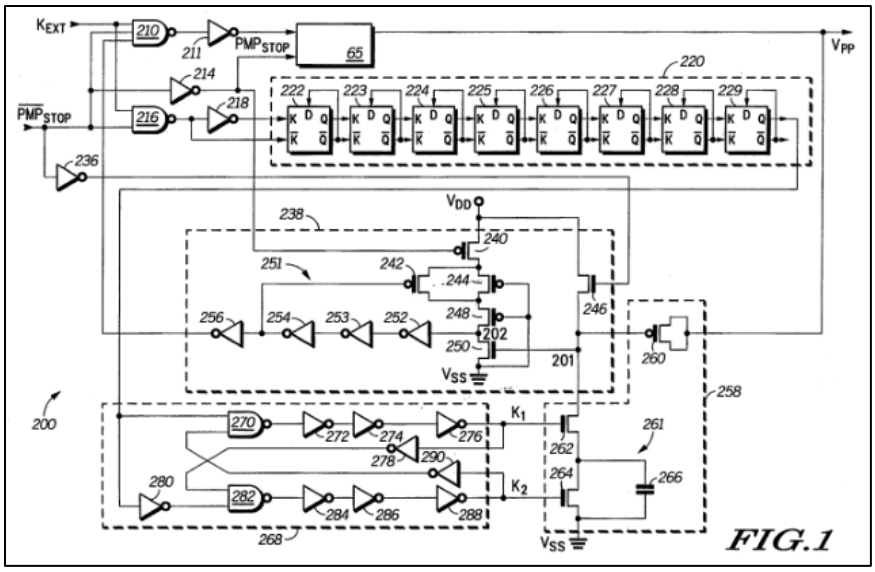


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

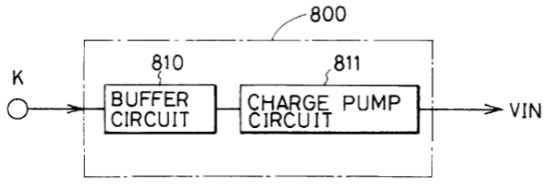


FIG.57

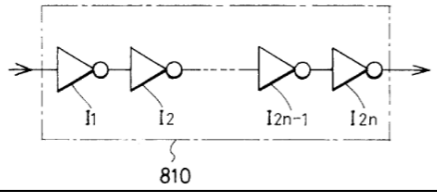


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

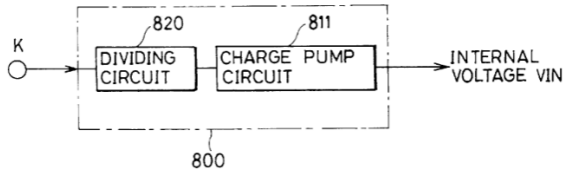
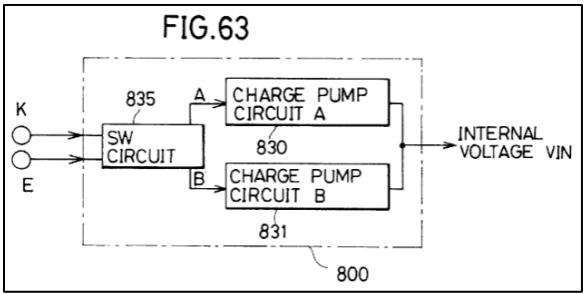


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

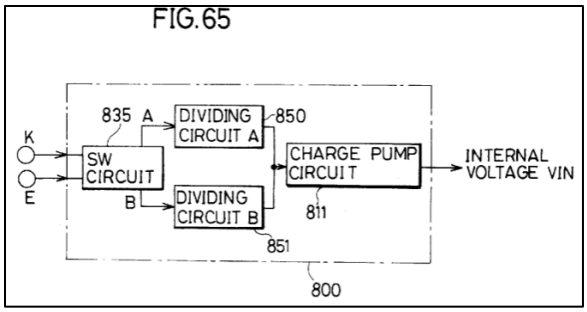
Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.

FIG.65



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

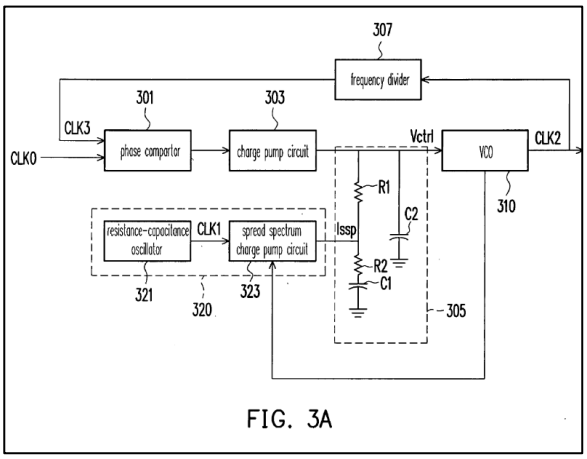


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

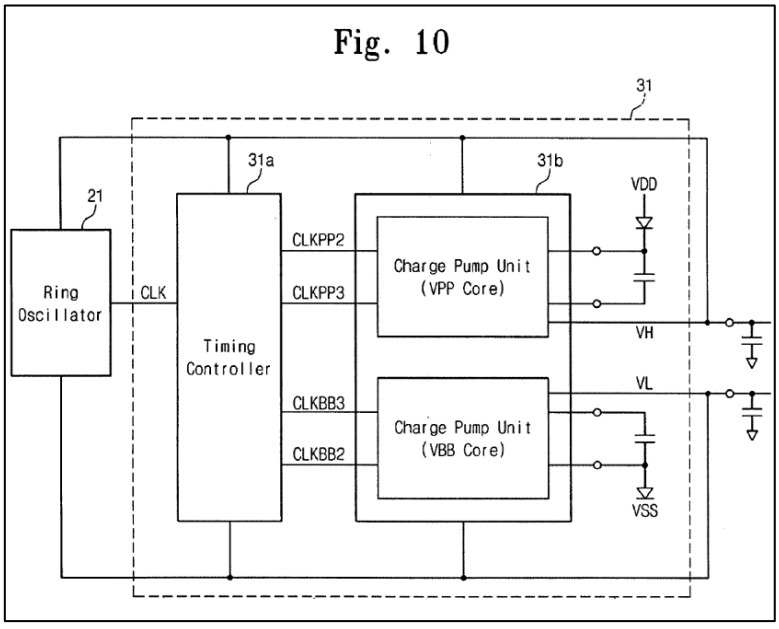


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

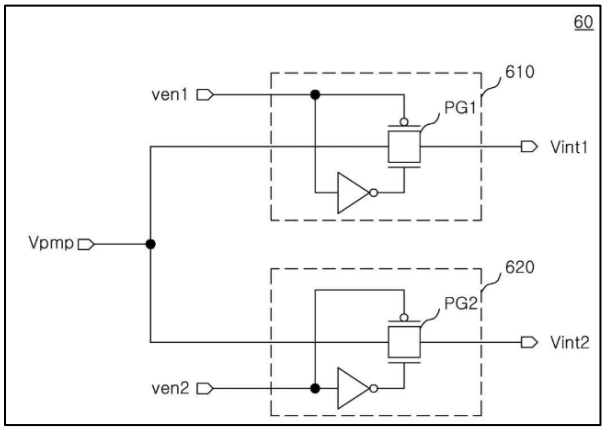
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

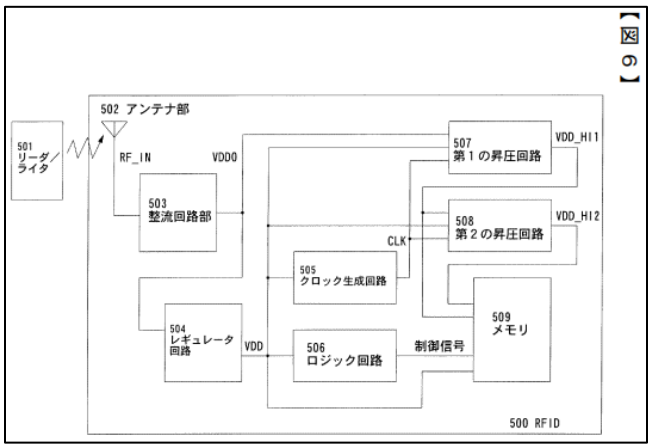
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

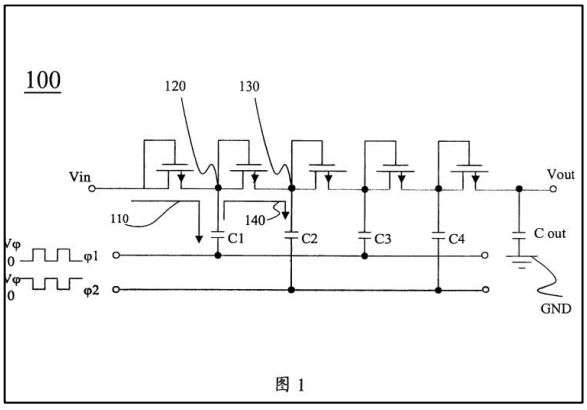
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

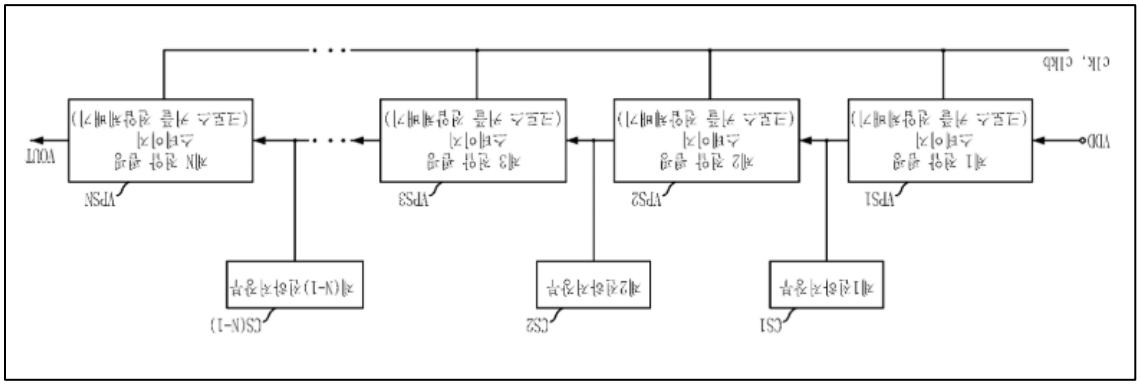
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

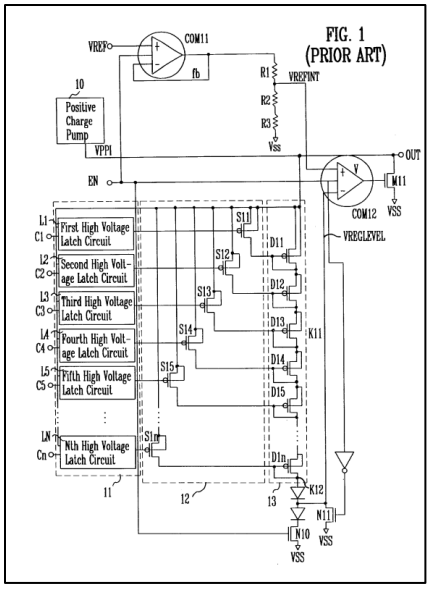
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



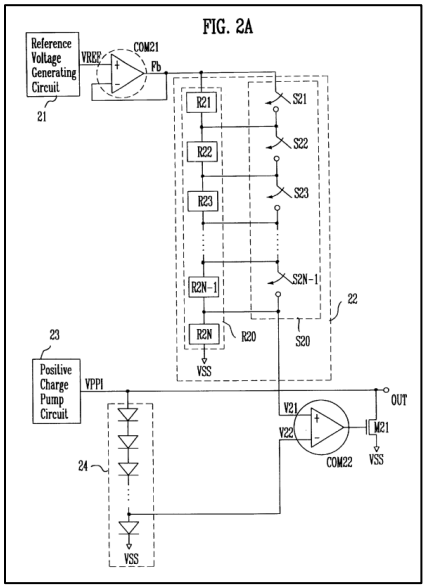
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

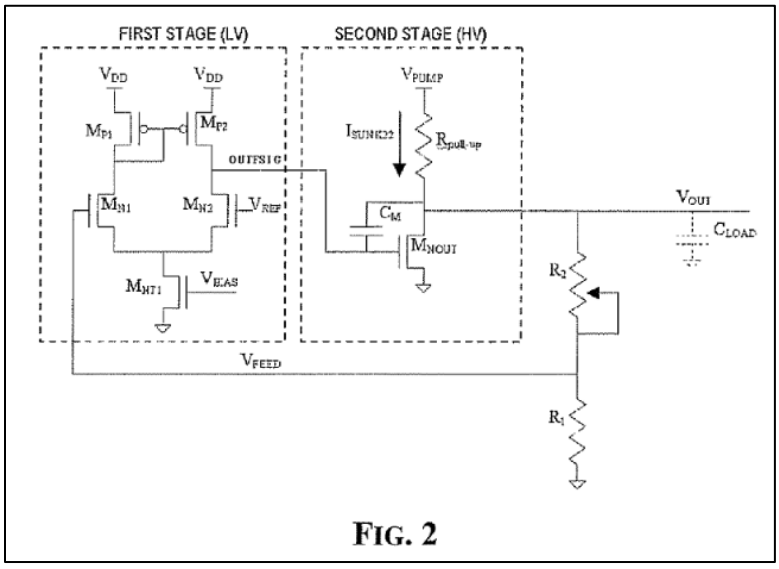


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

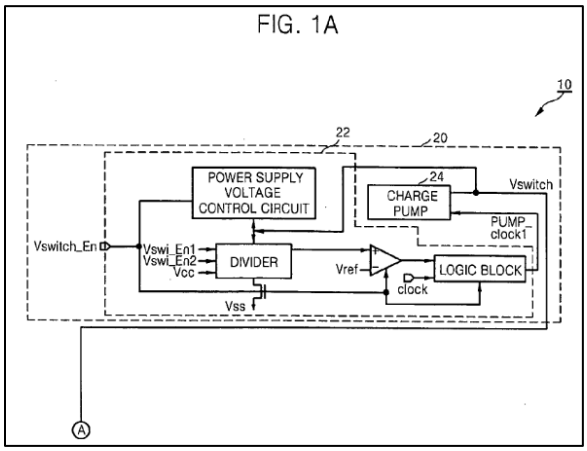
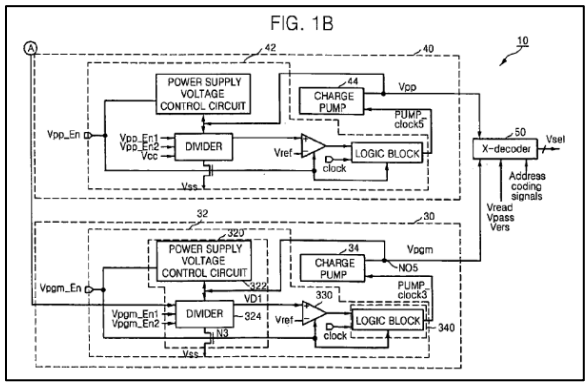
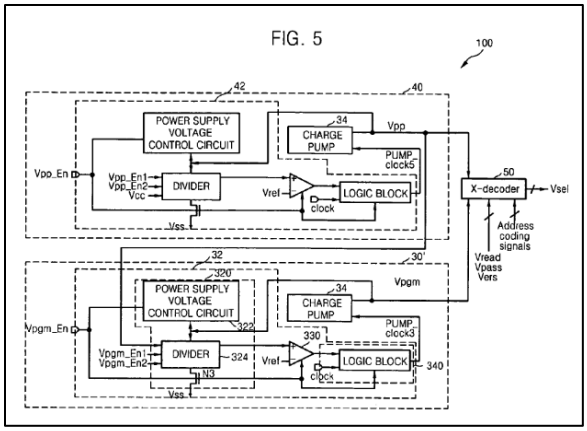


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

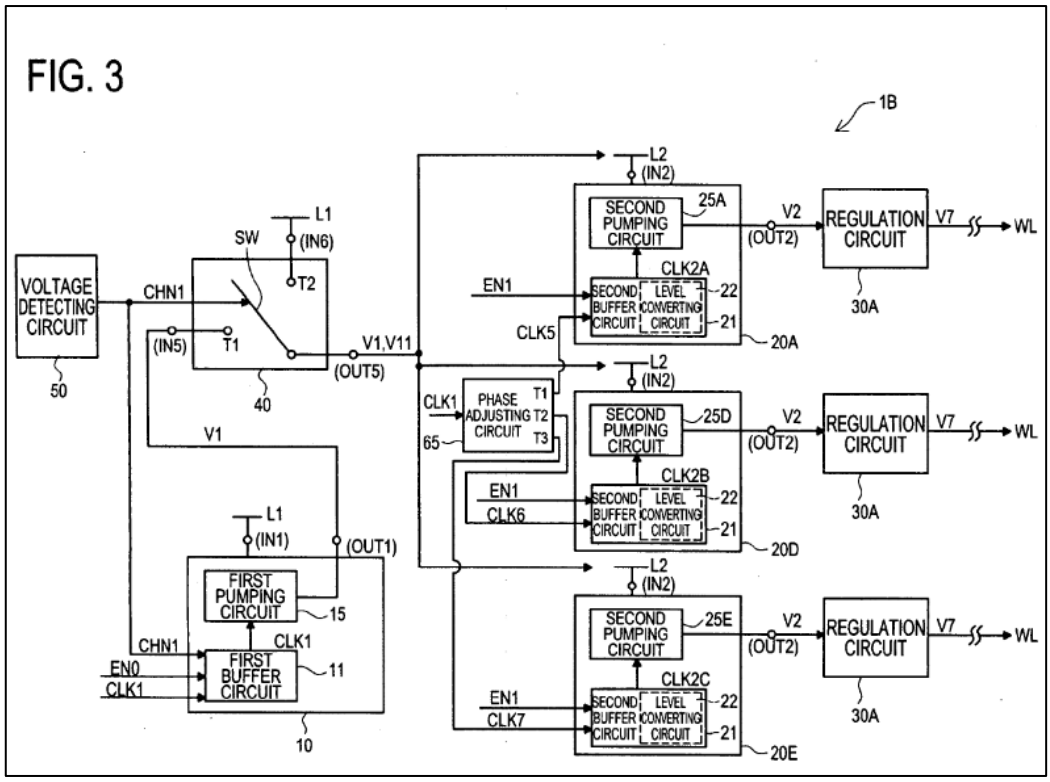
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

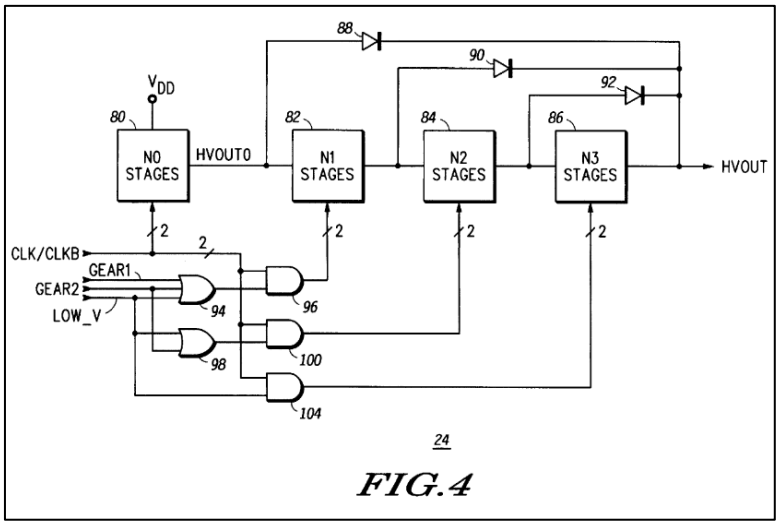


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

3[f] wherein the third clock signal is supplied to the second charge pump circuit.

The Omnibus References disclose and/or render obvious wherein the third clock signal is supplied

to the second charge pump circuit.

See, e.g., claim limitation 1[e], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

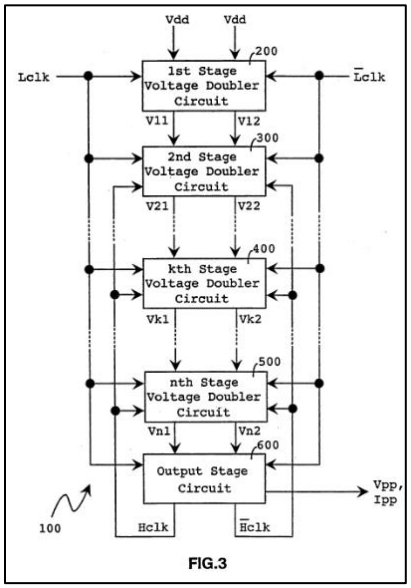


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal

to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

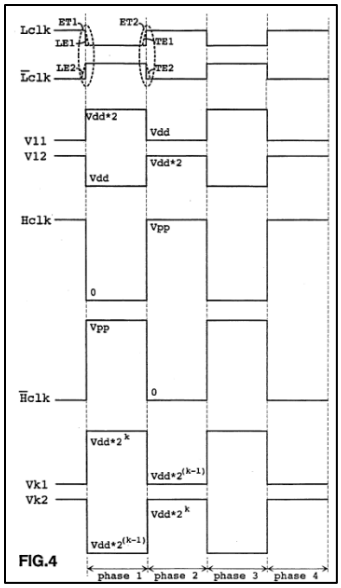


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

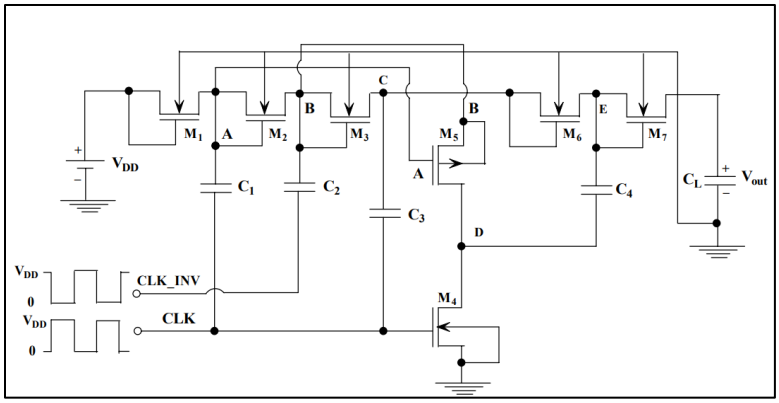
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

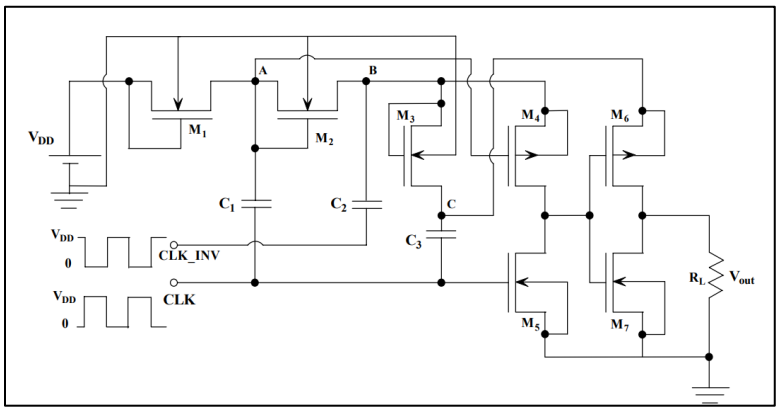
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

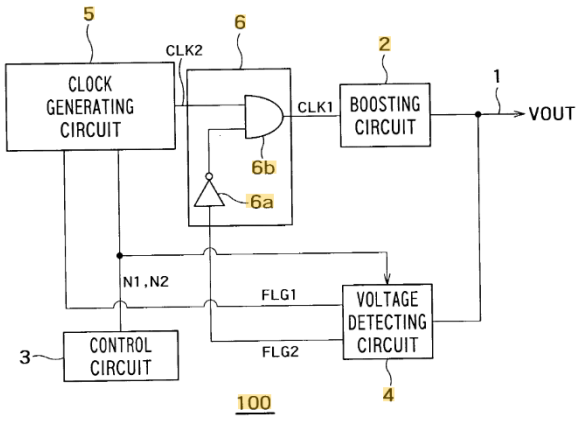


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

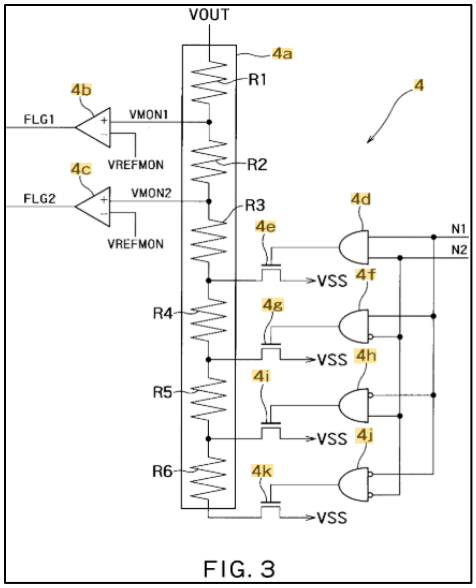


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

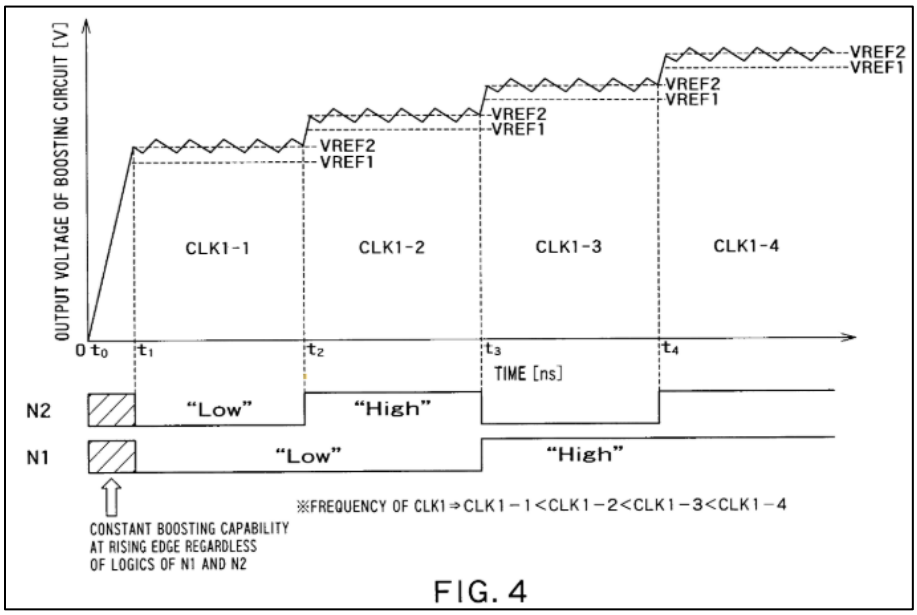


FIG. 4

Sato at [0051]:

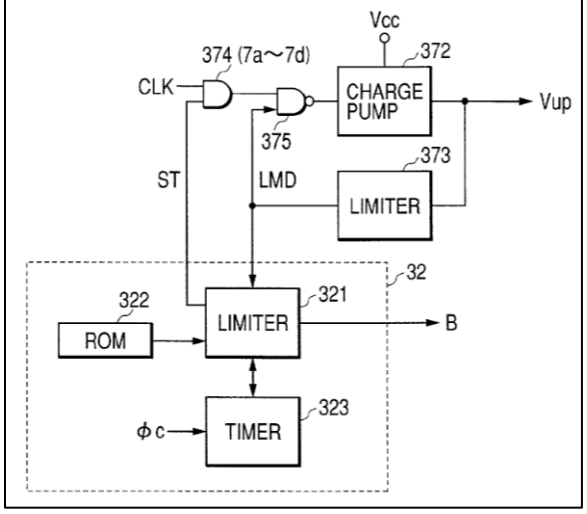
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

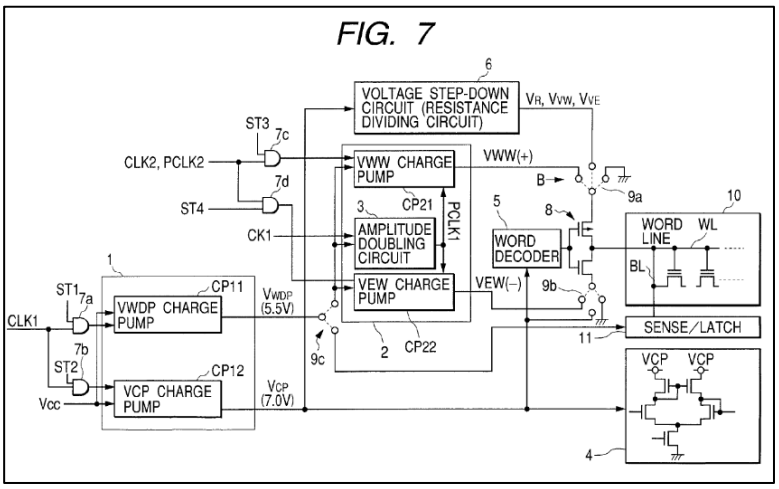
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

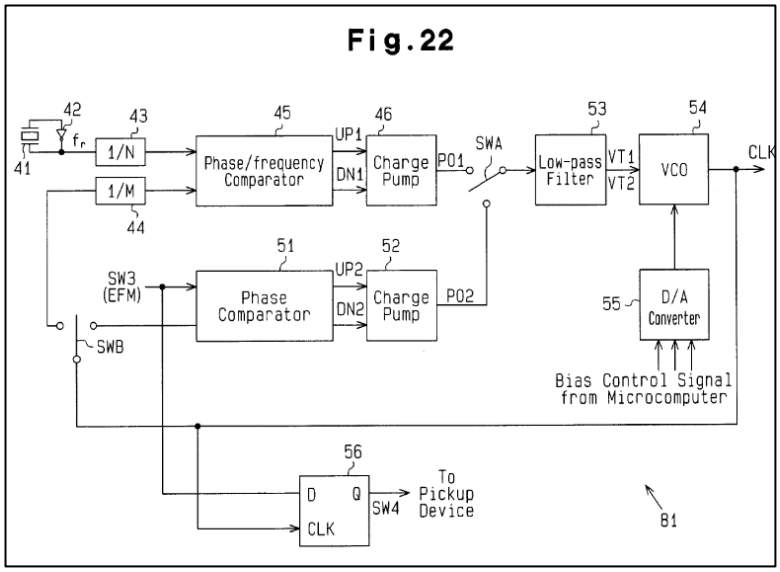
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

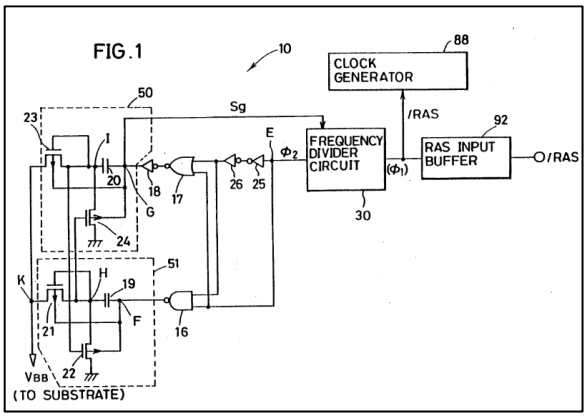


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

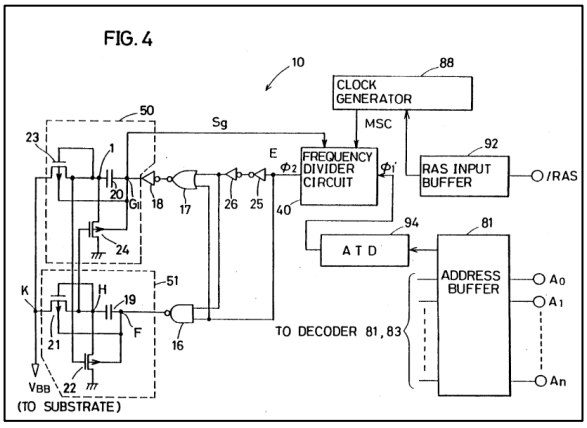
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

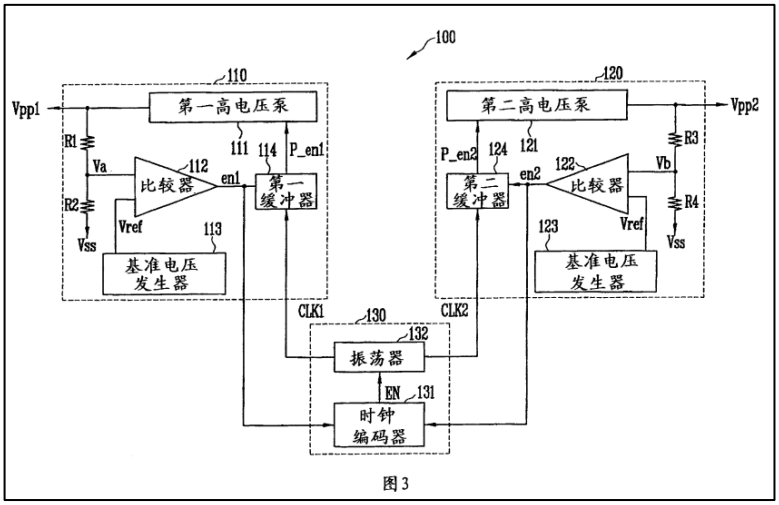


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

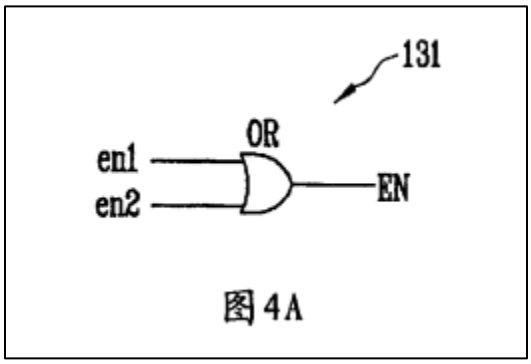


图 4A

Jiang at Fig. 6:

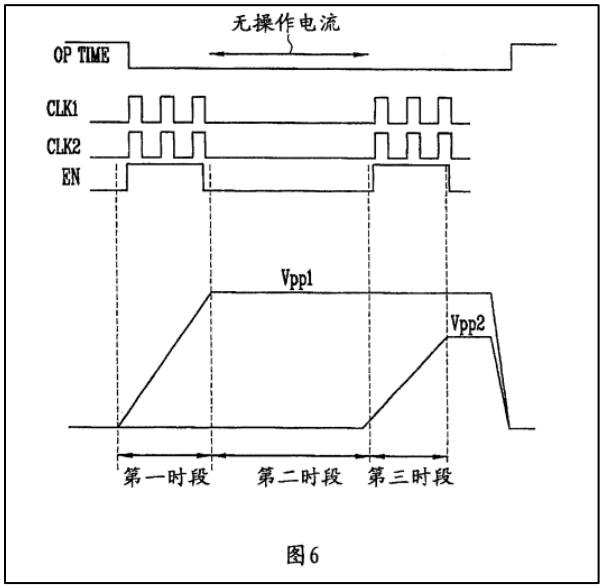
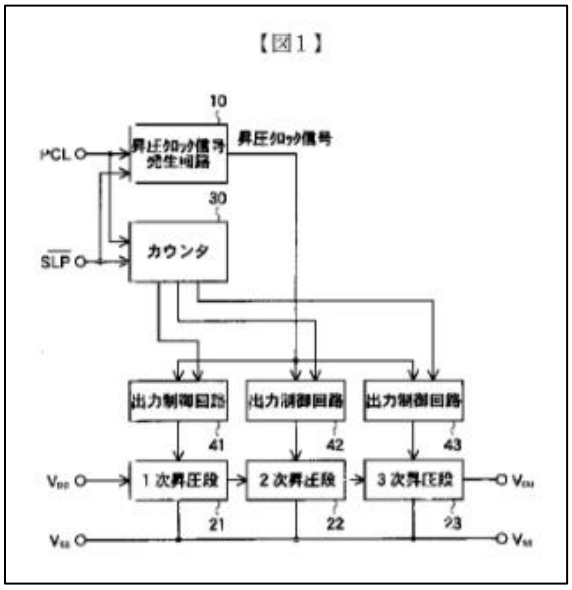


图6

Ito-633 at [0018] and Fig. 1:

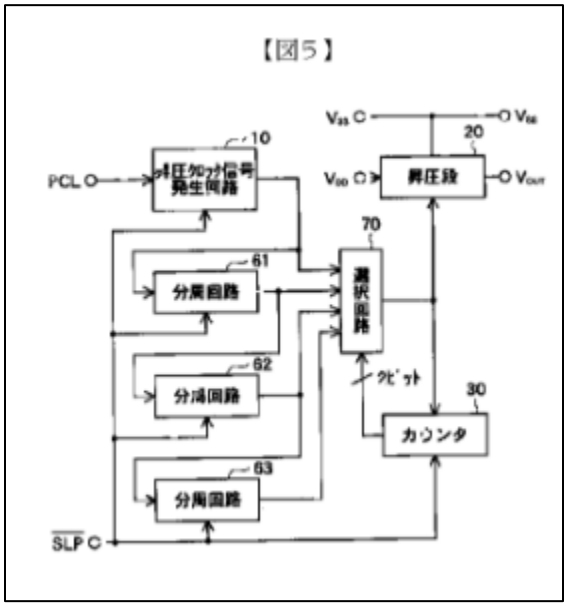
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

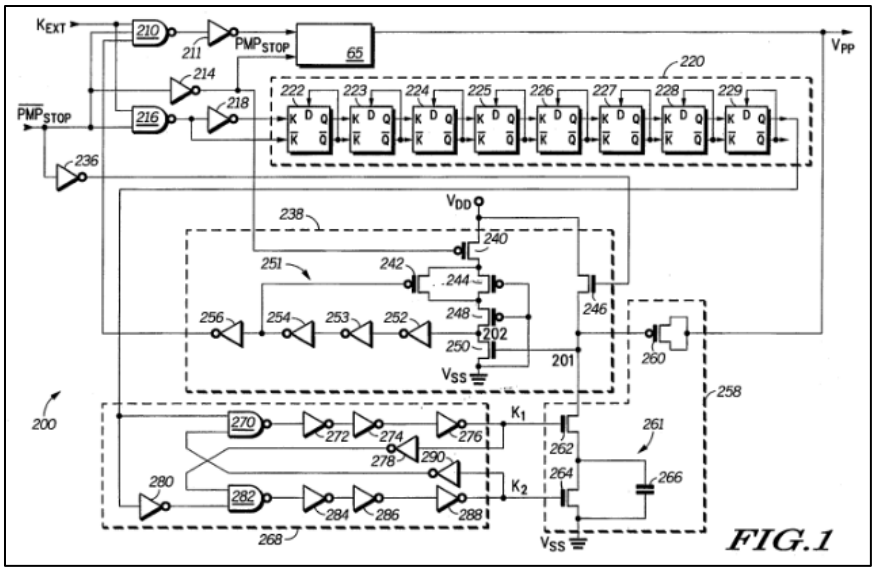


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

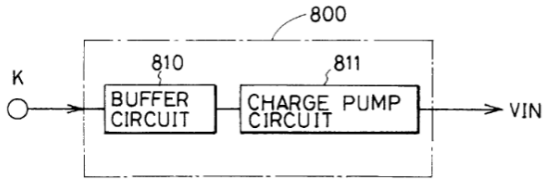


FIG.57

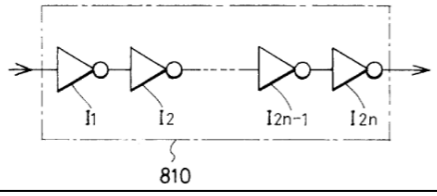


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

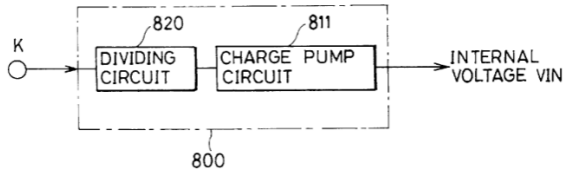
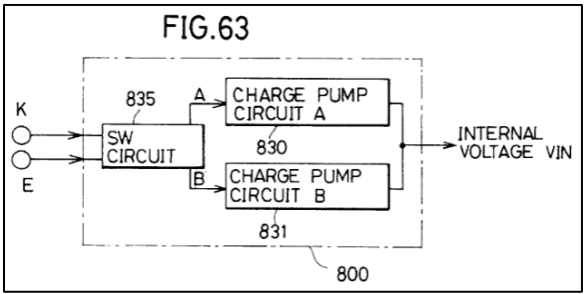


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



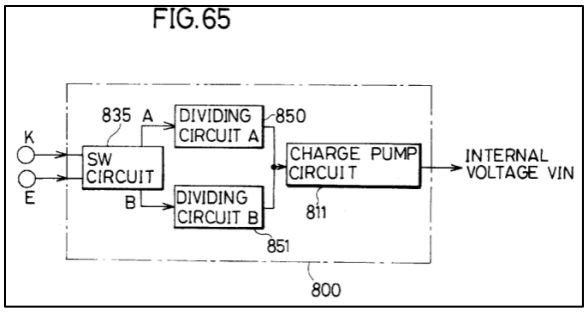
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

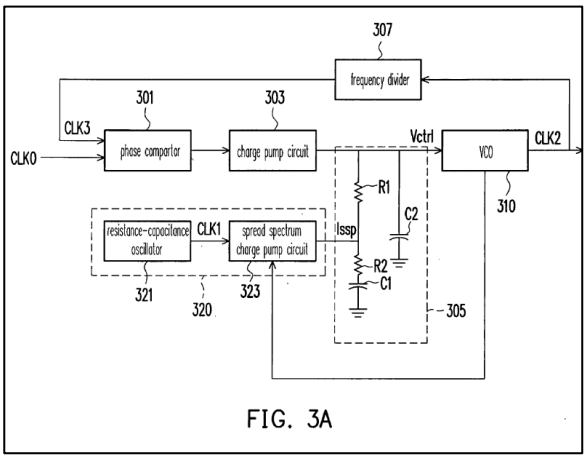


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

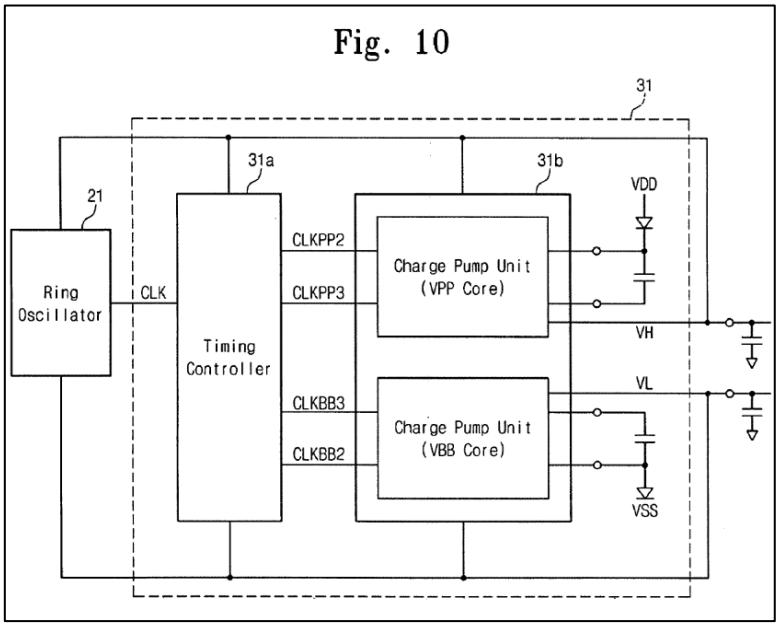


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

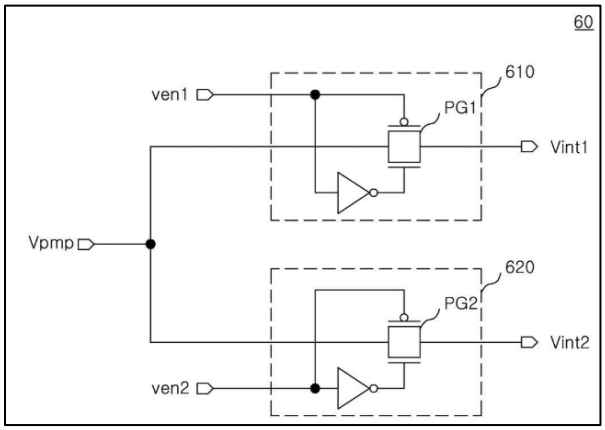
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

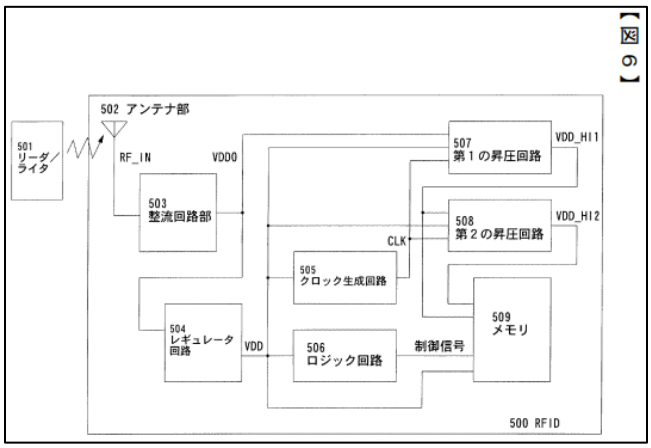
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

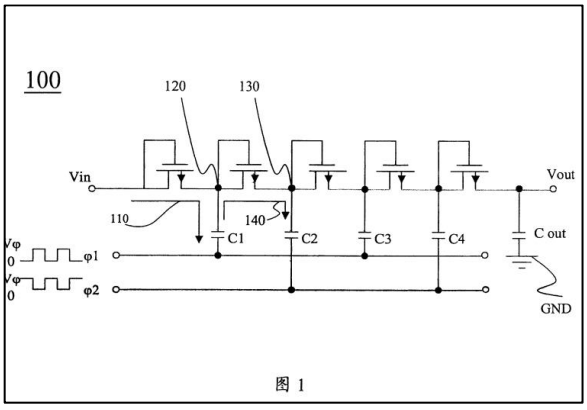
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

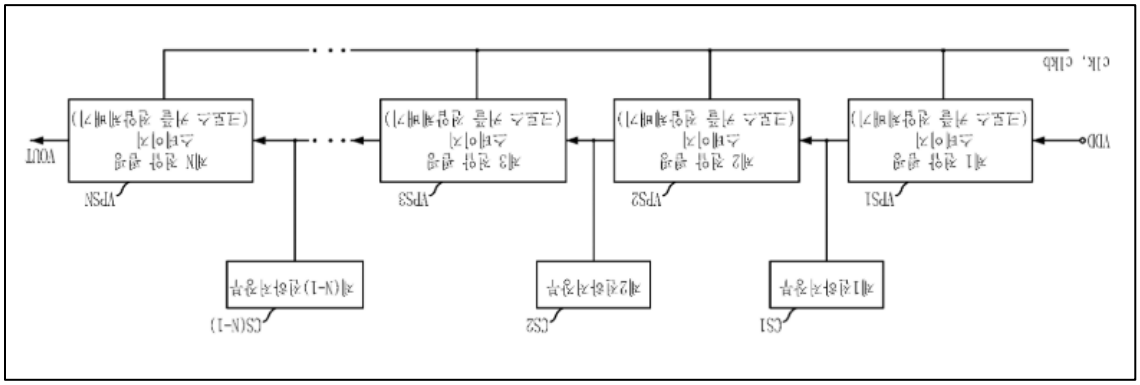
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

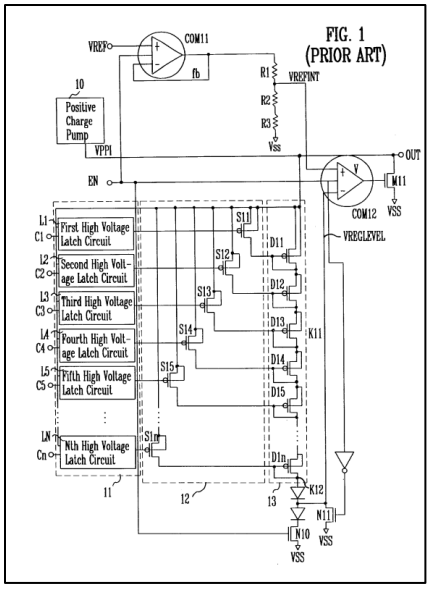
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



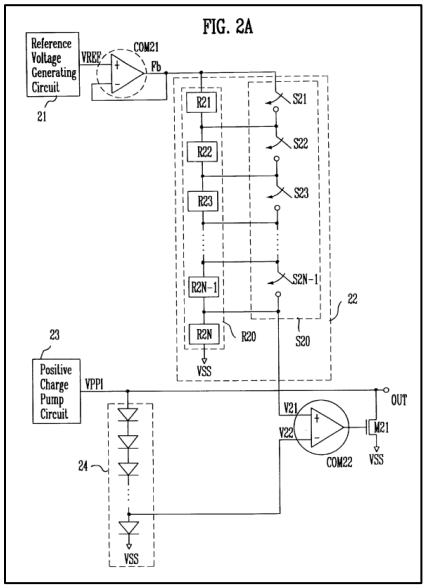
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

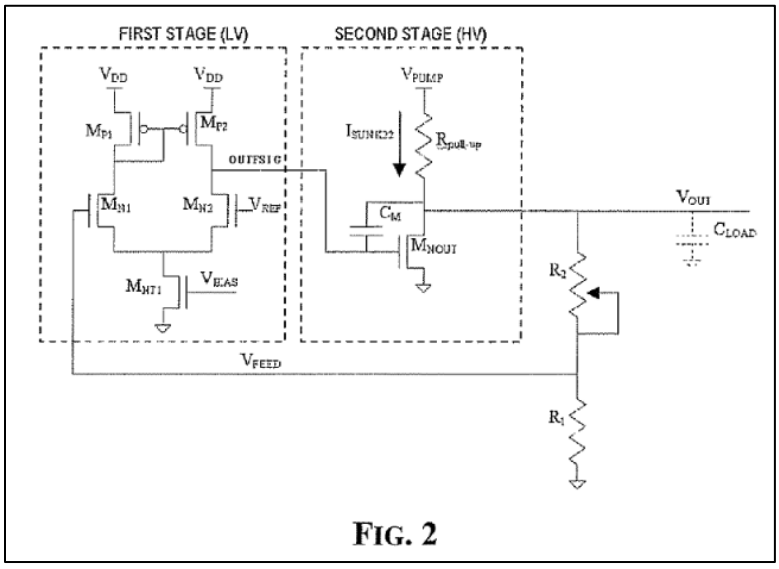


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

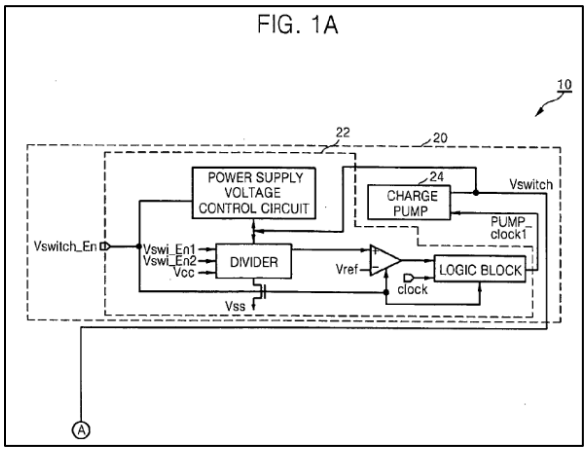
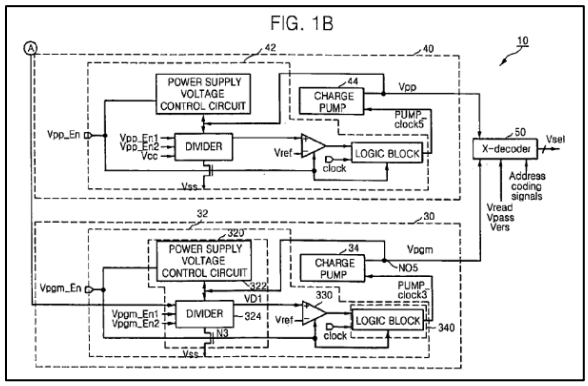
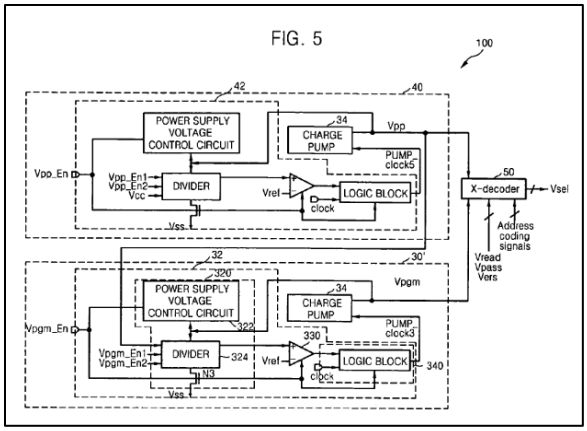


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

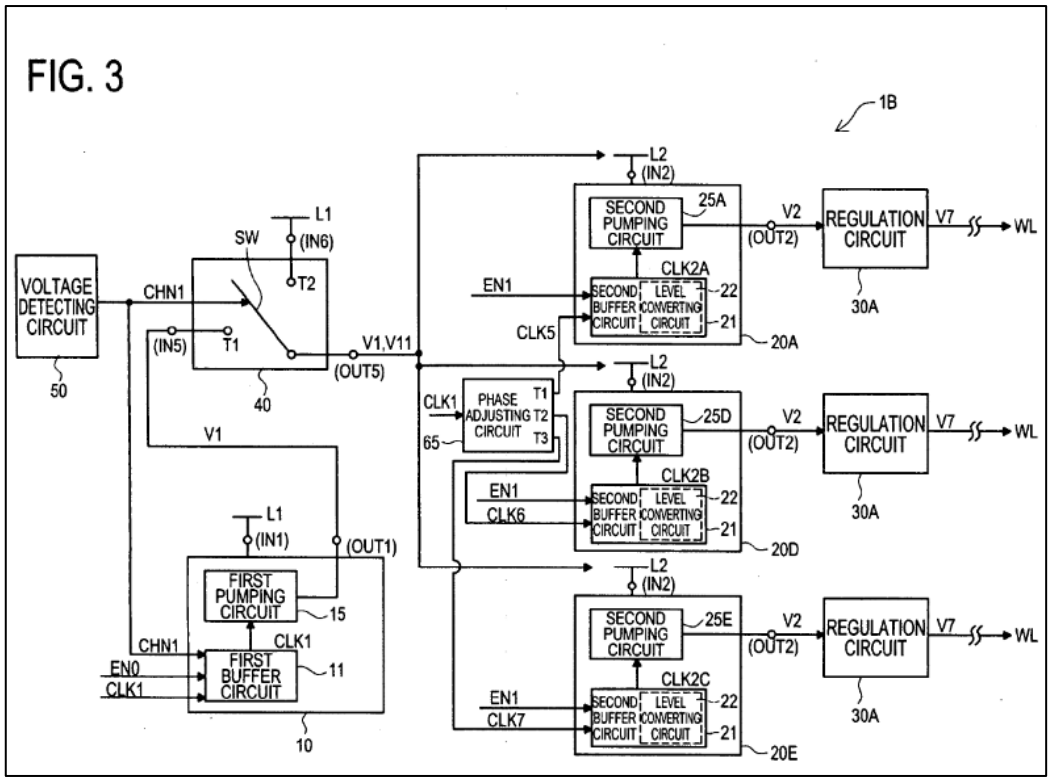
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

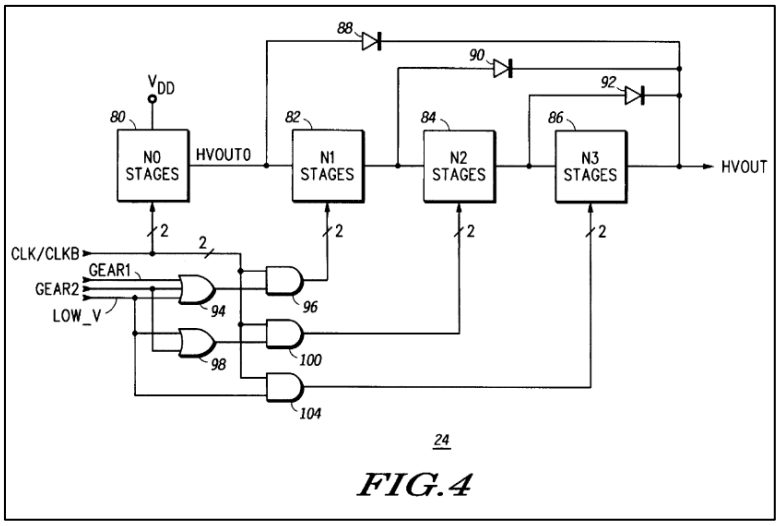


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

4[a] The internal voltage generating circuit of claim 3,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious an

internal voltage generating circuit.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

4[b] wherein a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.

The Omnibus References disclose and/or render obvious wherein a clock signal having substantially the same frequency as that of the first clock signal is supplied to the first charge pump circuit.

See, e.g., claim limitations 1[d] and 1[e], *supra.*

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

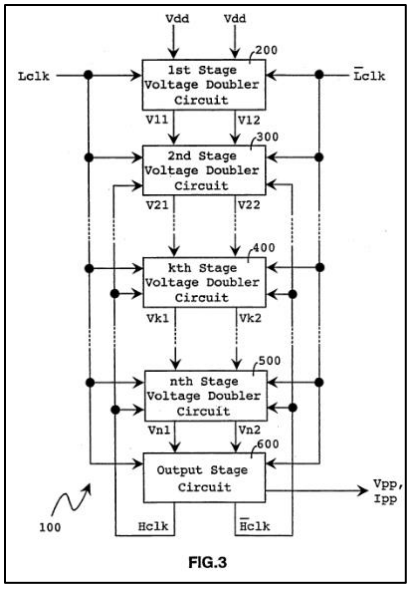


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second

voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

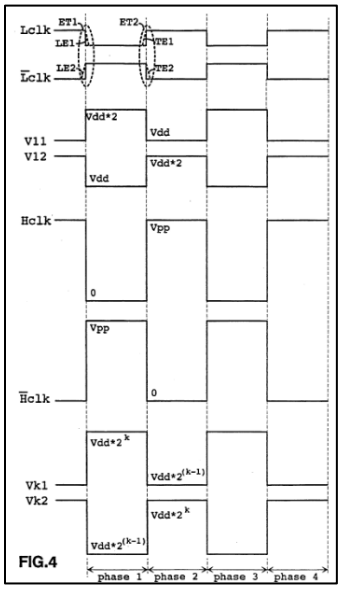


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation

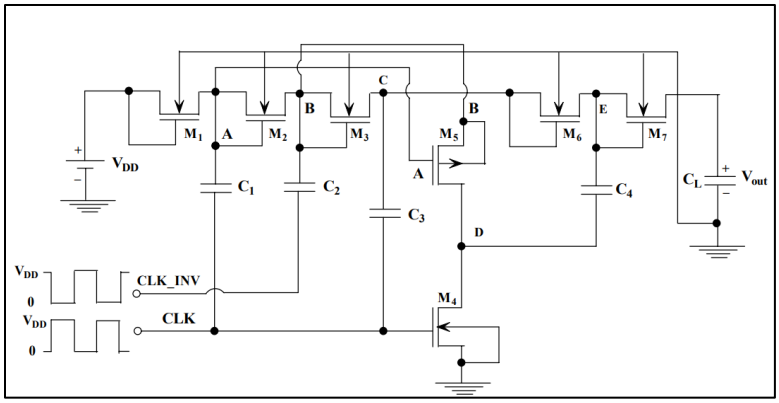
filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

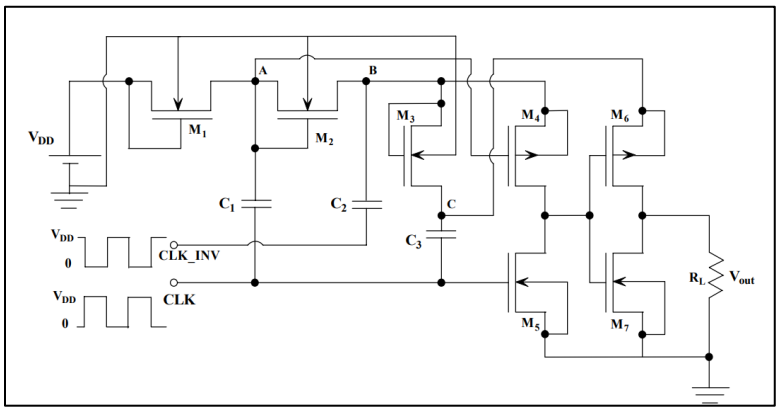
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

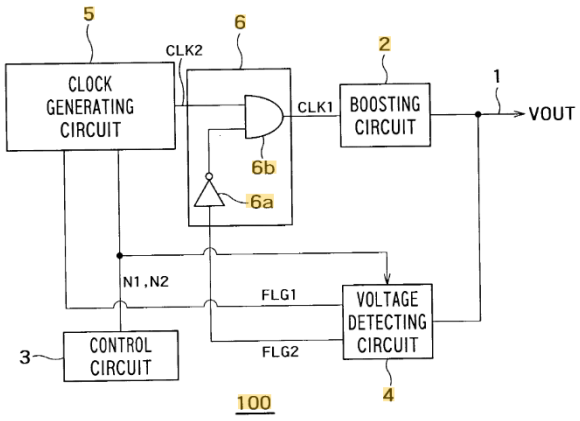


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

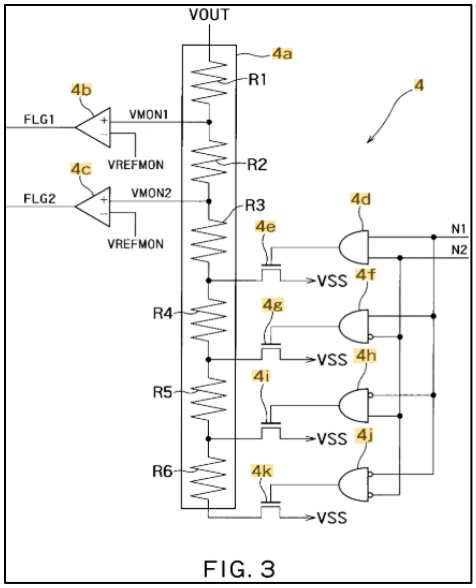


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

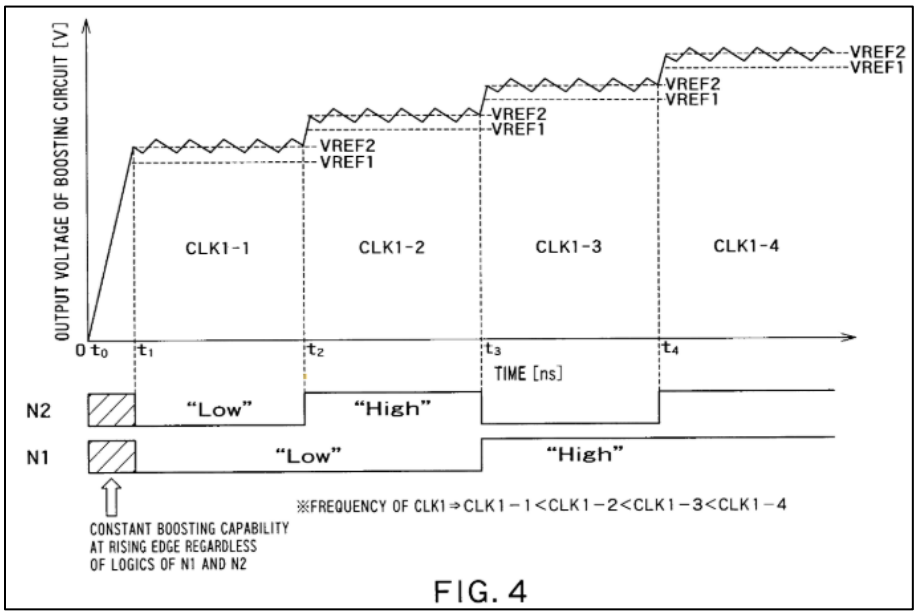


FIG. 4

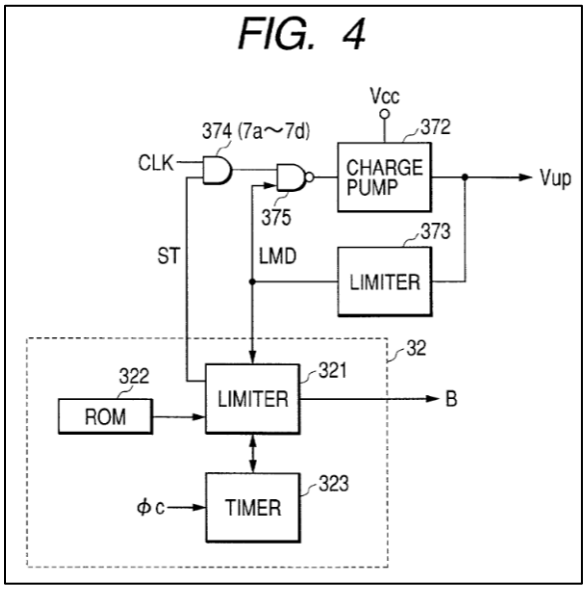
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

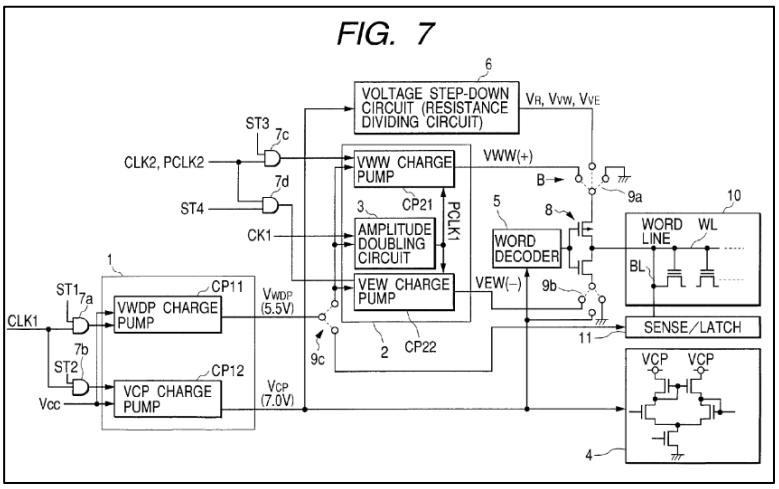
In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

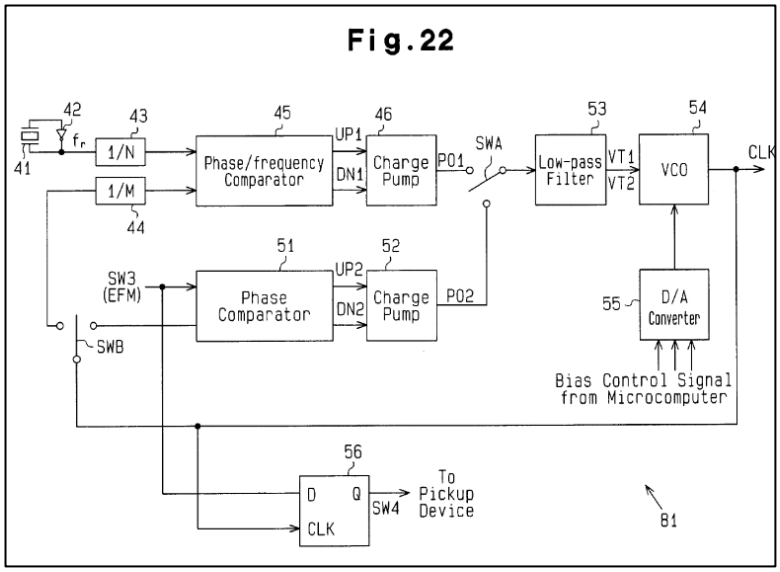
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

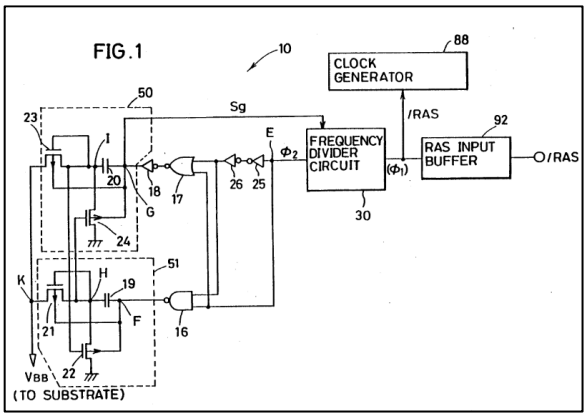


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

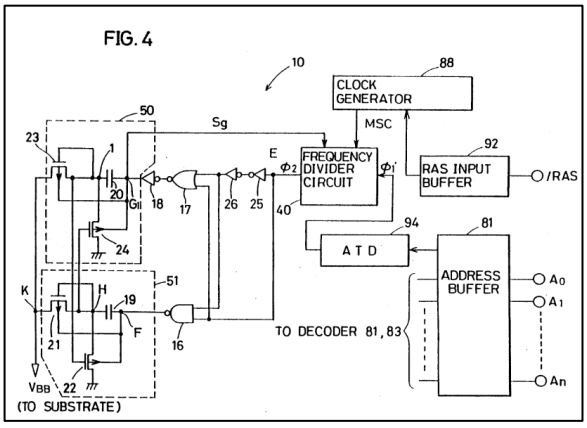
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

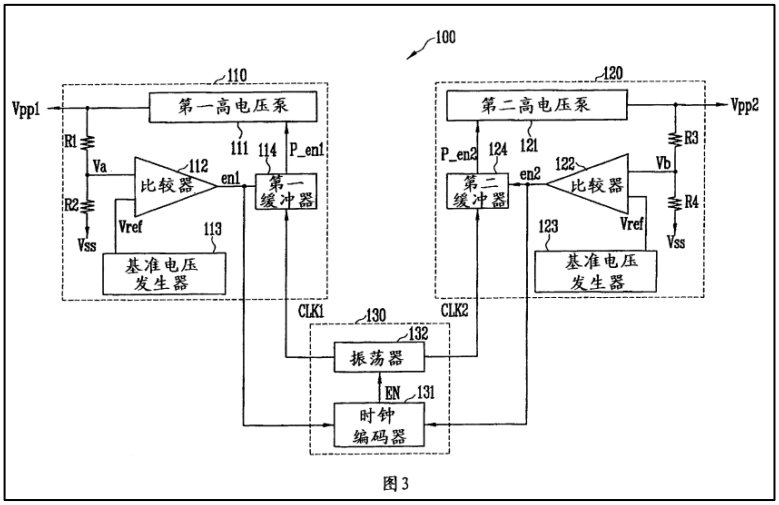


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

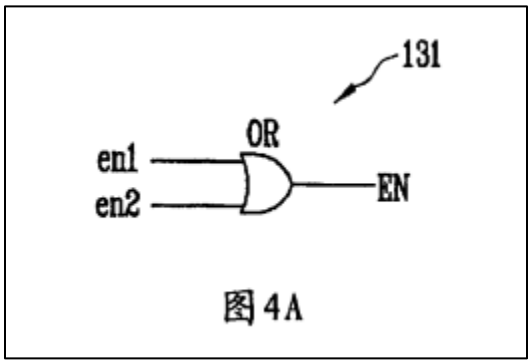


图 4A

Jiang at Fig. 6:

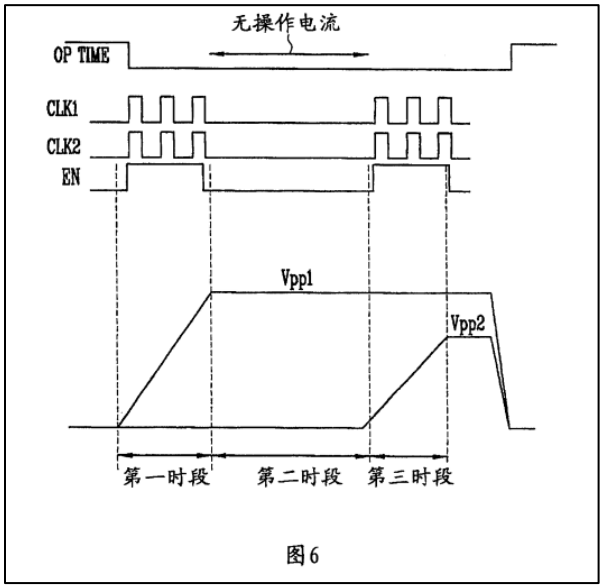
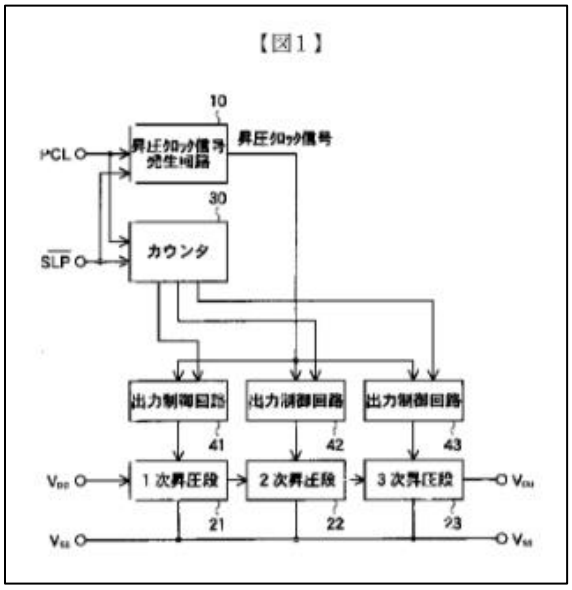


图6

Ito-633 at [0018] and Fig. 1:

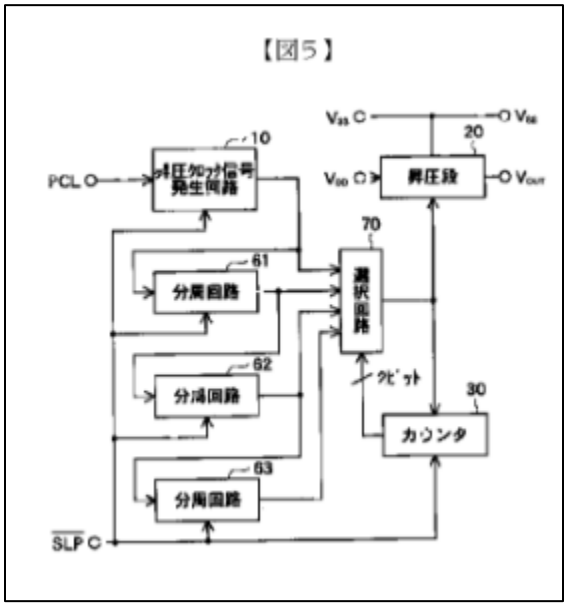
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

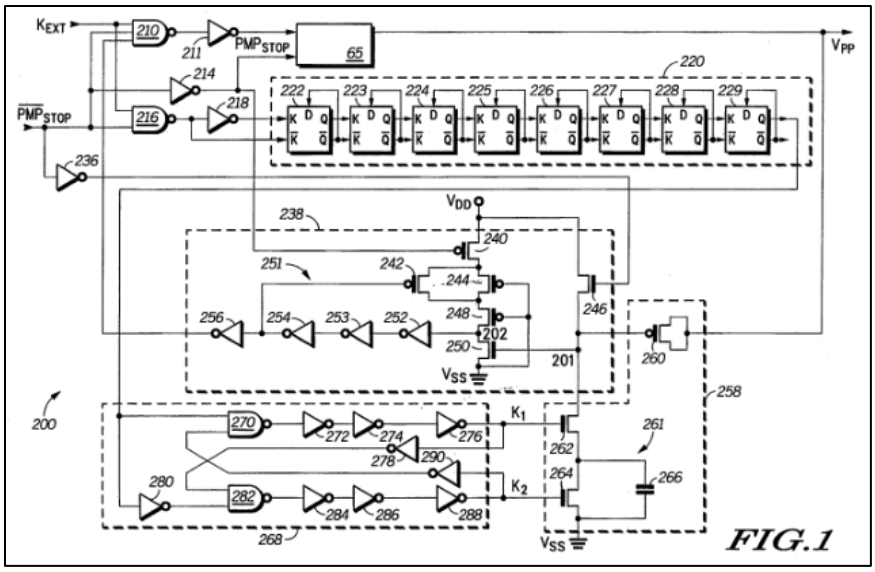


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

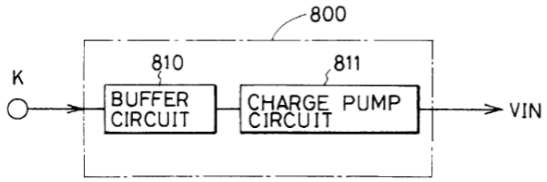


FIG.57

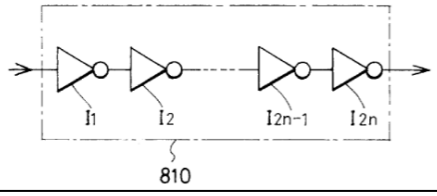


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

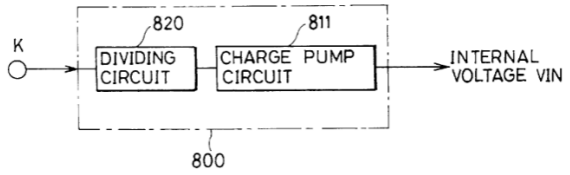
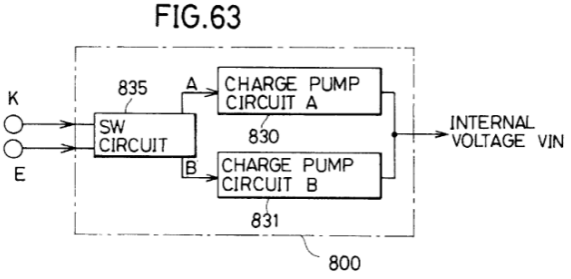


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG. 63



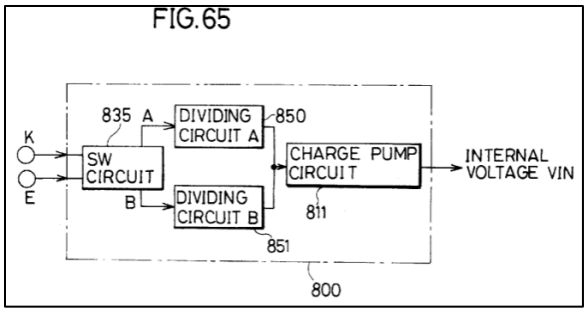
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

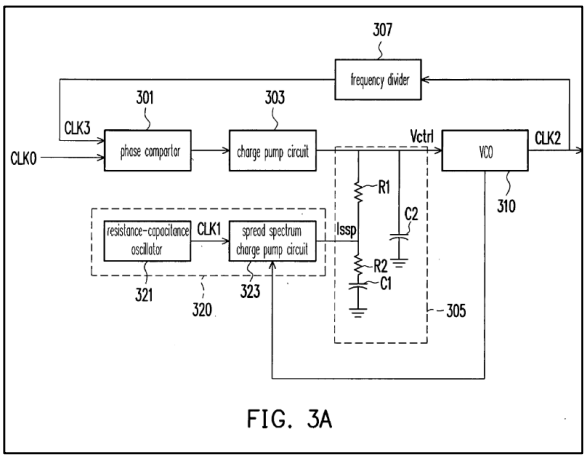


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

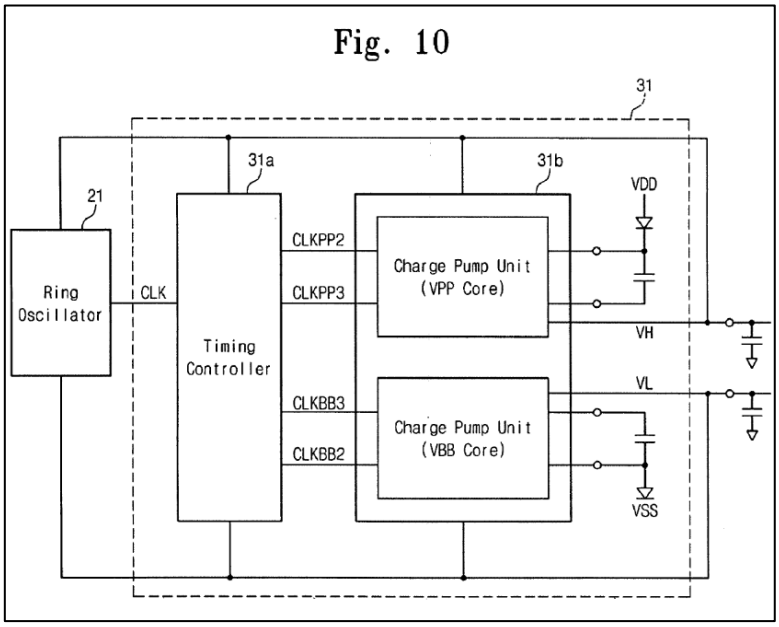


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

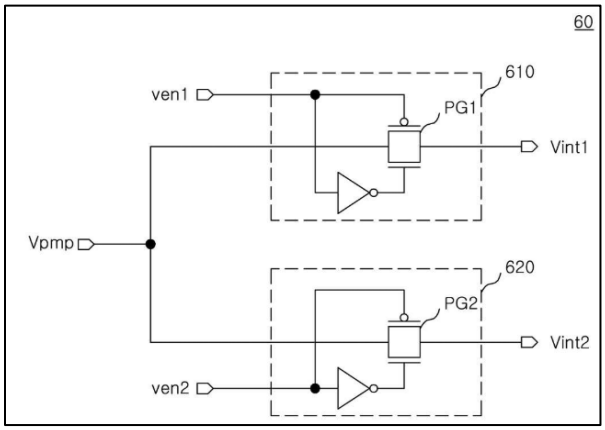
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

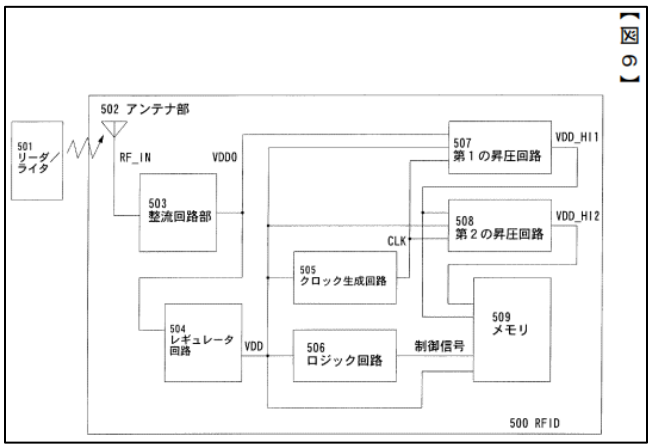
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

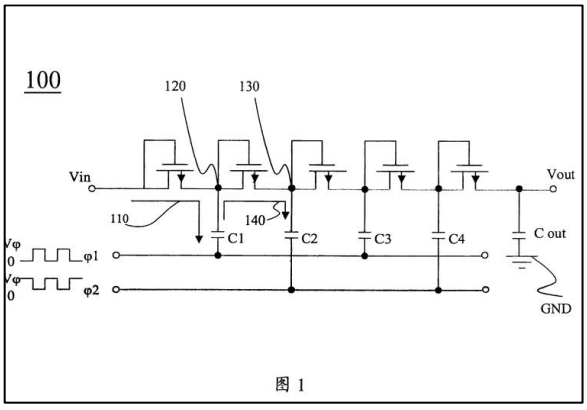
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

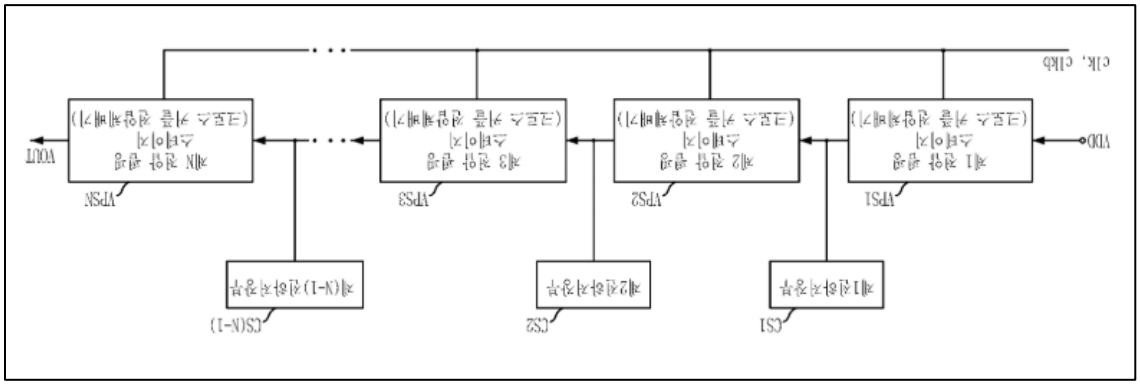
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

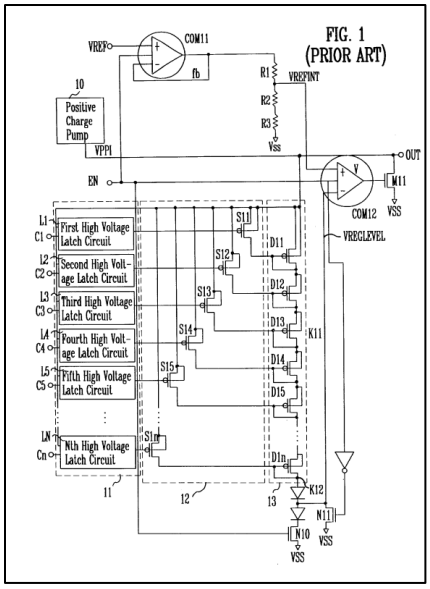
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



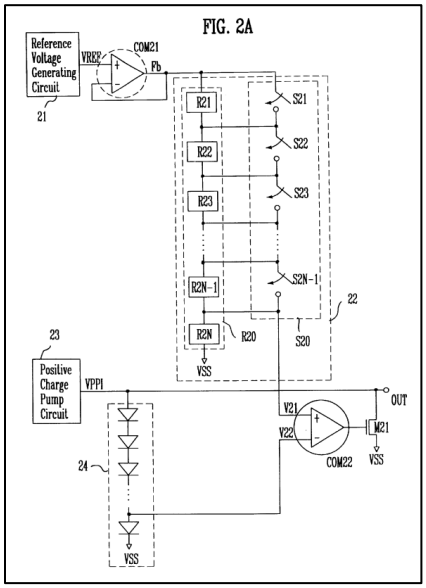
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

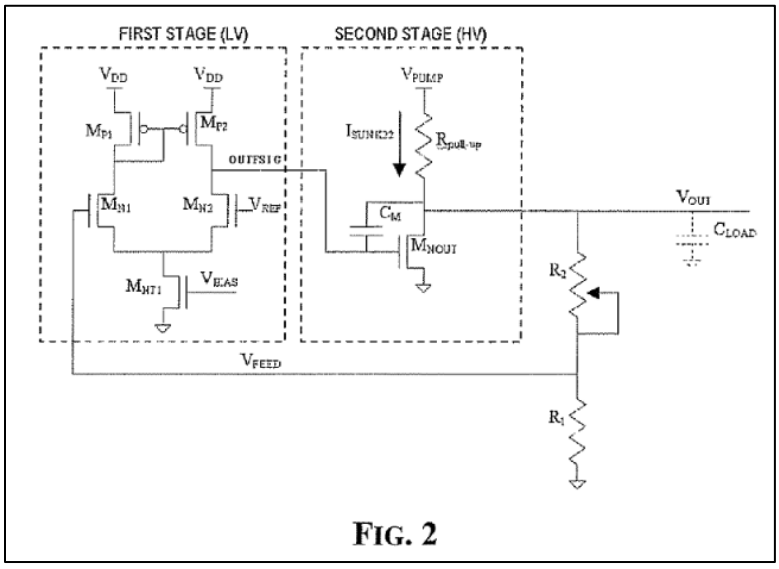


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

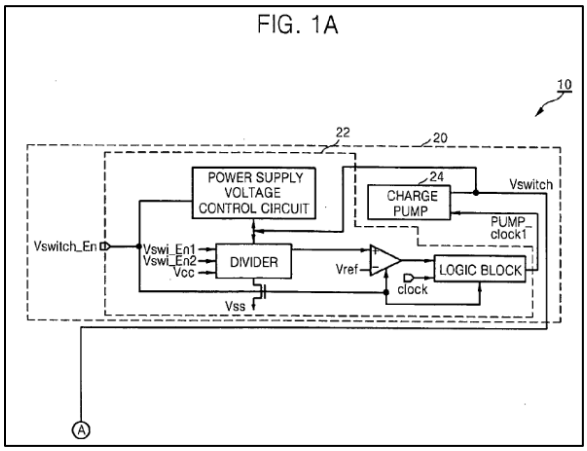
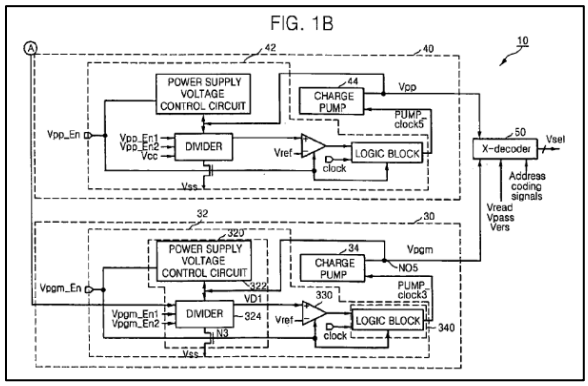
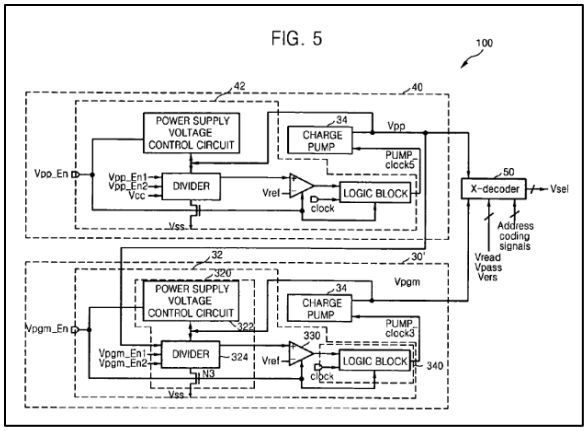


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

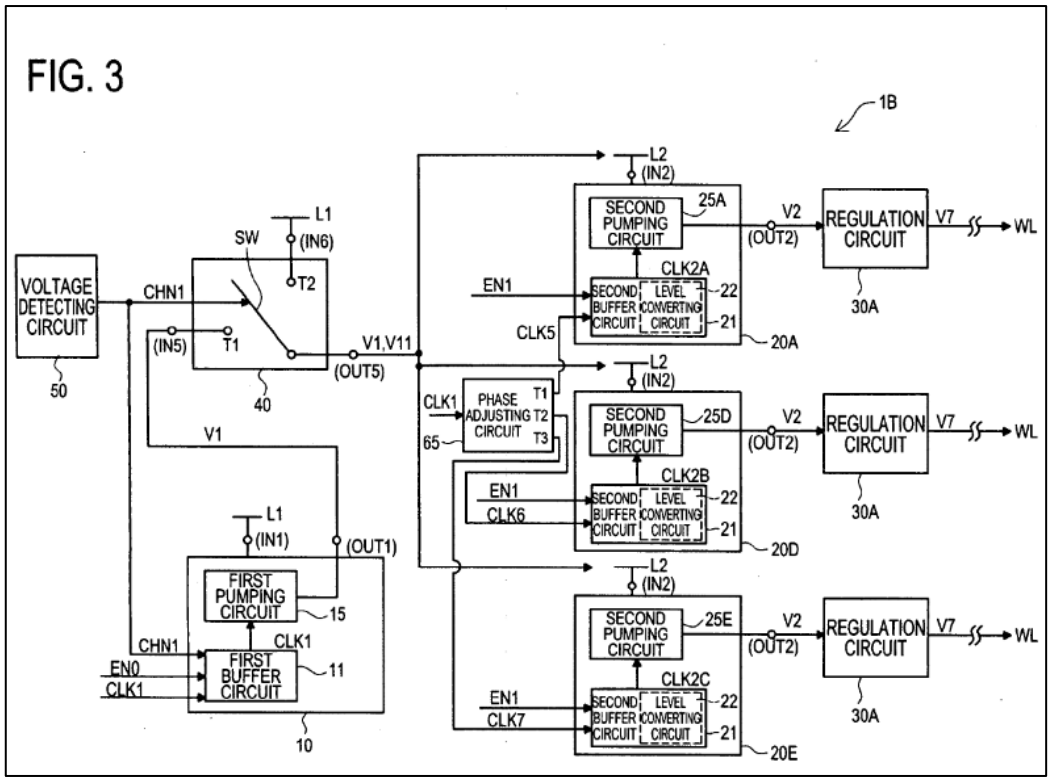
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

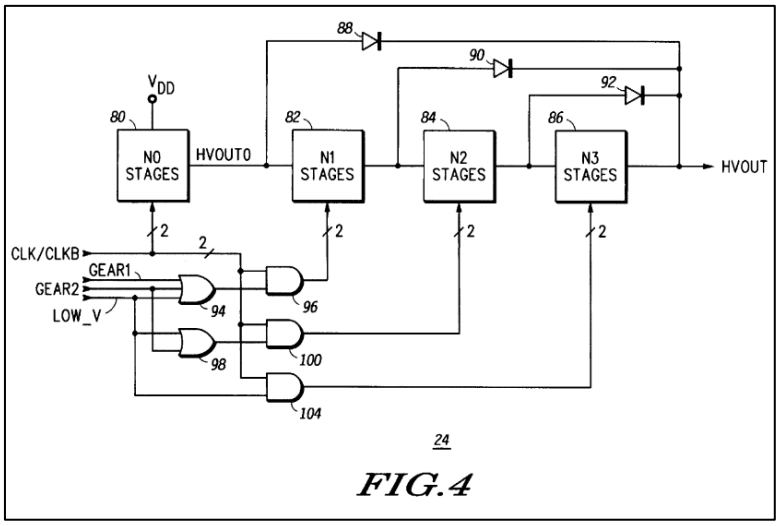


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

6[a] An internal voltage generating circuit comprising:

To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious an

internal voltage generating circuit .

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

6[b] a first charge pump circuit configured to generate a second voltage from a first voltage; and

The Omnibus References disclose and/or render obvious a first charge pump circuit configured to generate a second voltage from a first voltage.

See, e.g., claim limitation 1[b], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

6[c] a second charge pump circuit configured to generate a third voltage from the second voltage,

The Omnibus References disclose and/or render obvious a second charge pump circuit configured to generate a third voltage from the second voltage.

See, e.g., claim limitation 1[c], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

6[d] wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal, and

The Omnibus References disclose and/or render obvious wherein a frequency of a clock signal to be su shied [sic] to the second charge pump circuit is changed in accordance with a control signal.

See, e.g., claim limitation 1[d], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases,

respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

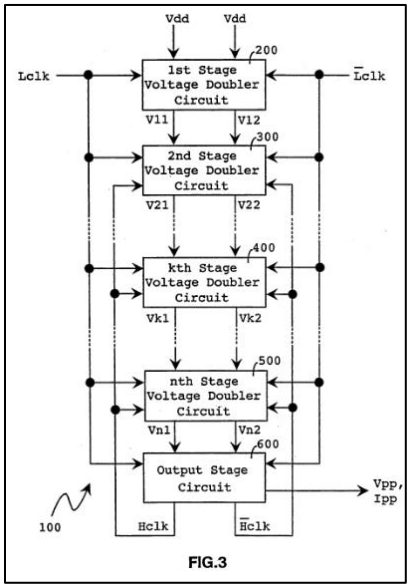


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

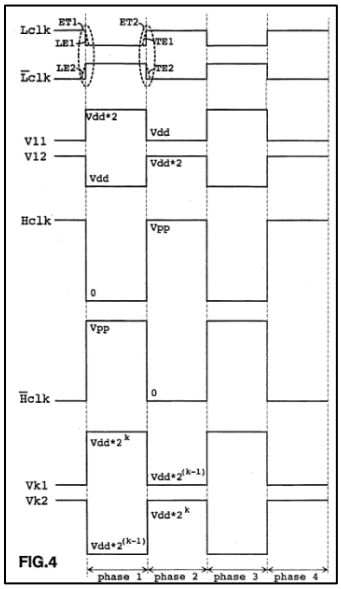
In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second

phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.



Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter

(ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be

applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

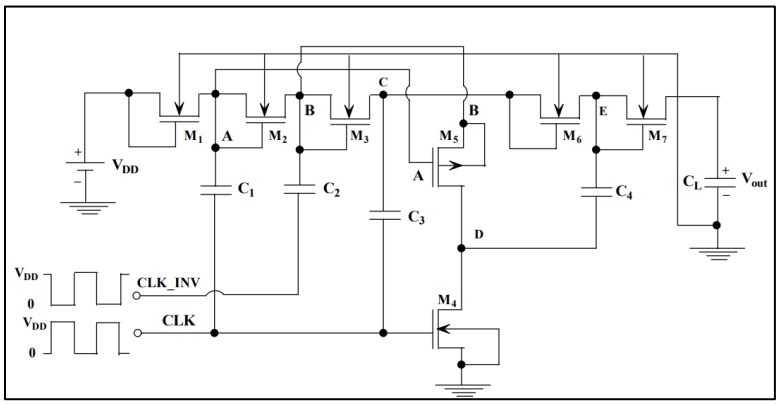
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 μs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 μs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

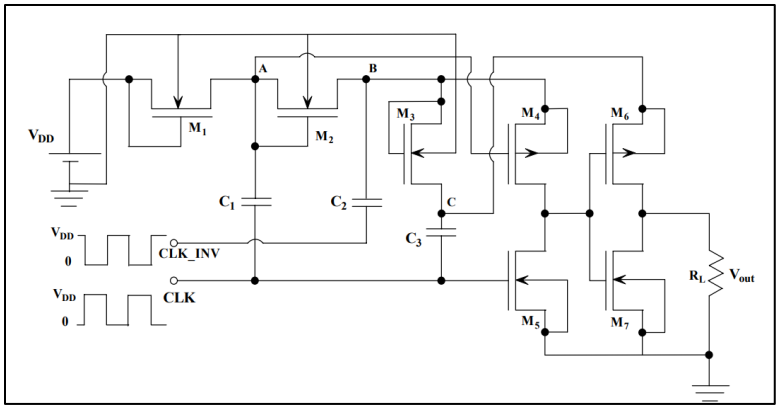
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

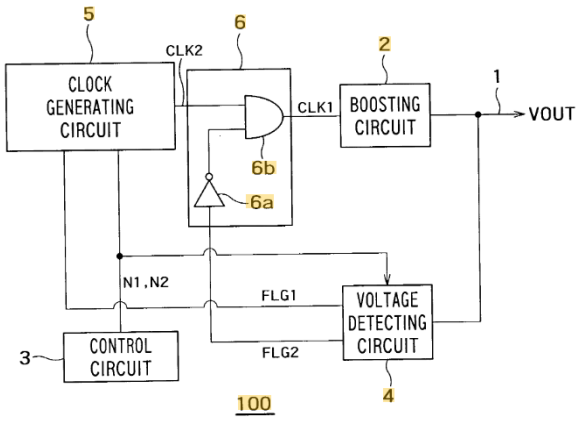


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating

circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

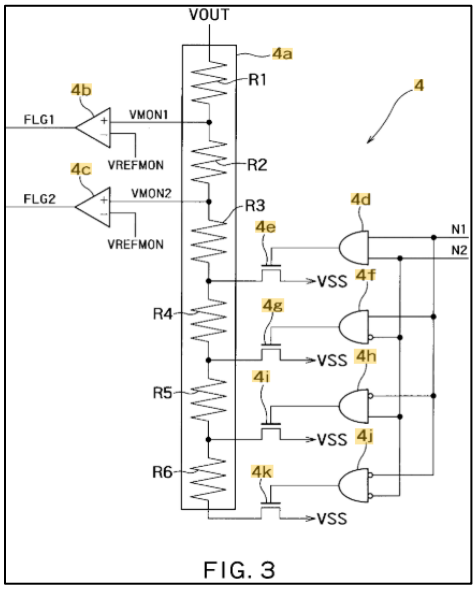


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5

includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

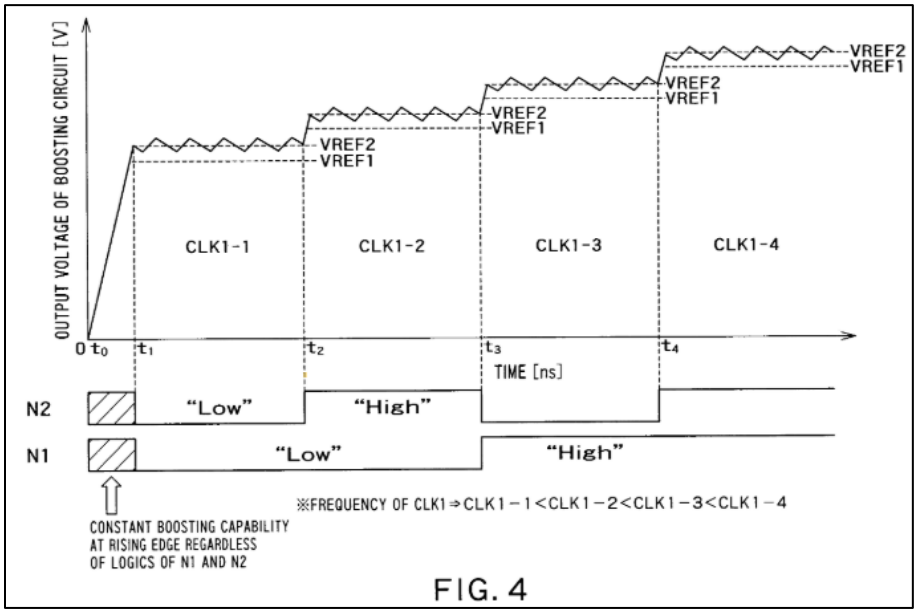


FIG. 4

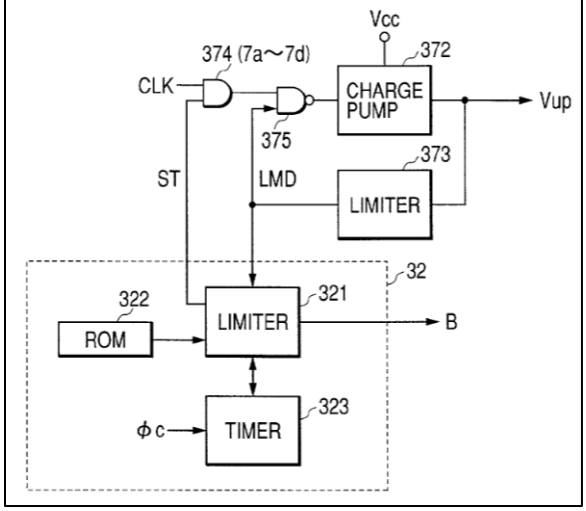
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

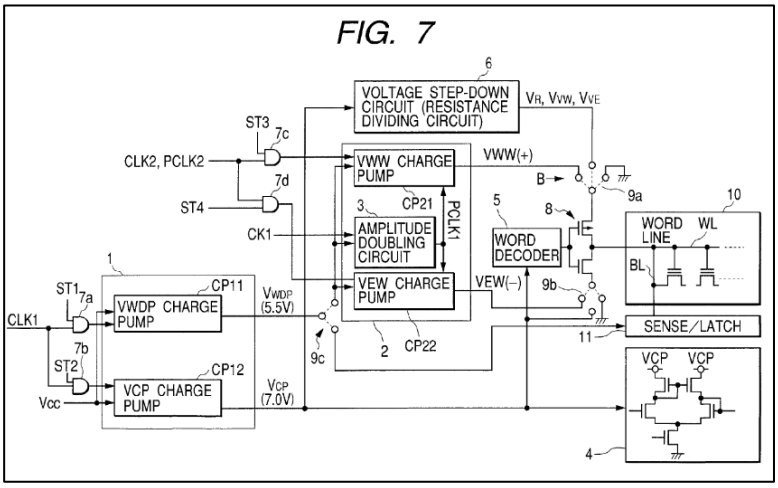
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory

having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted,

the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2 goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

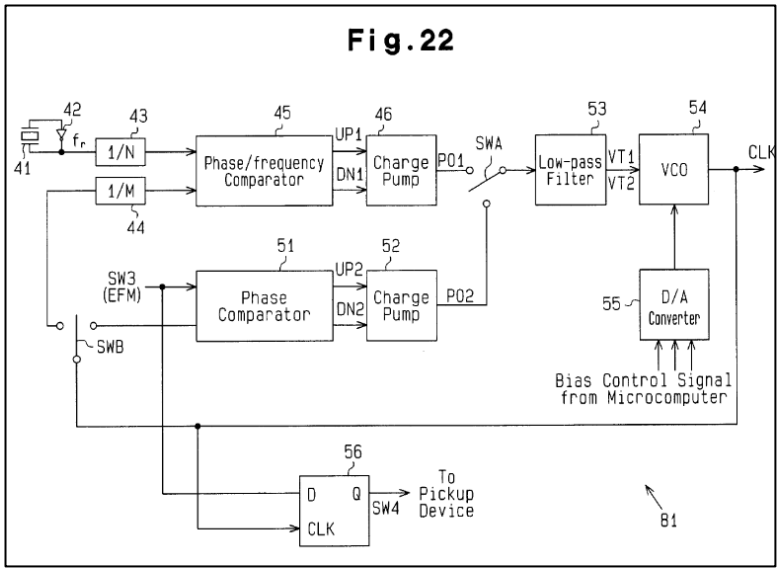
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

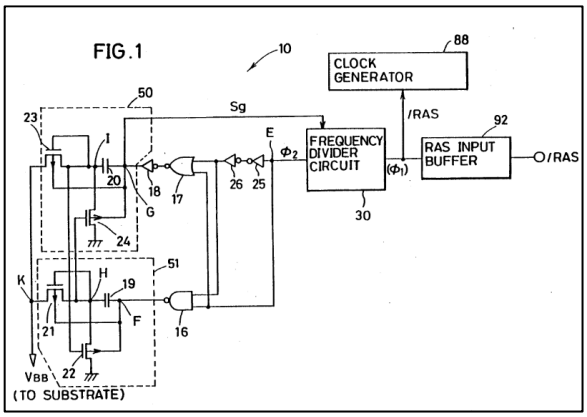


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

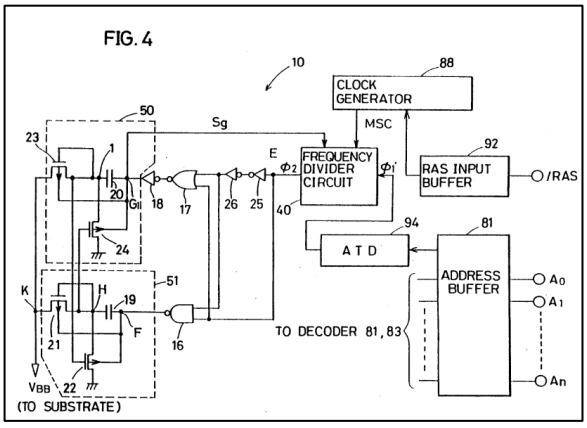
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

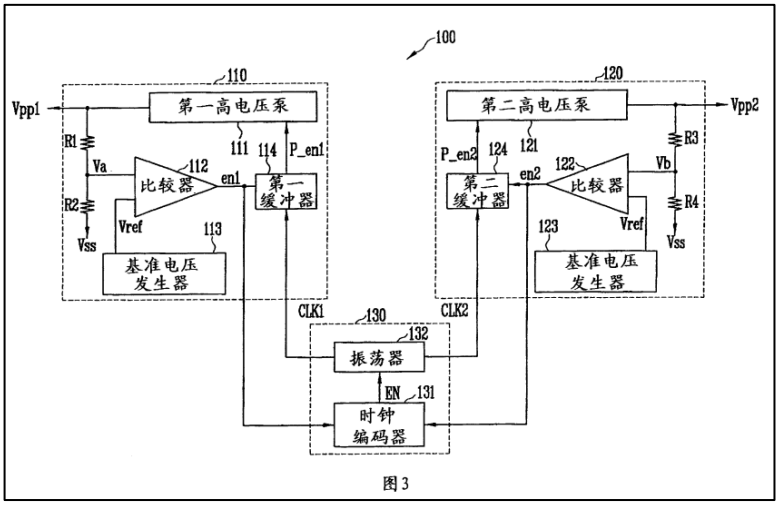


图 3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

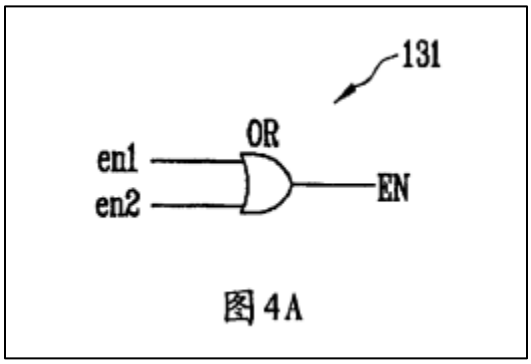


图 4A

Jiang at Fig. 6:

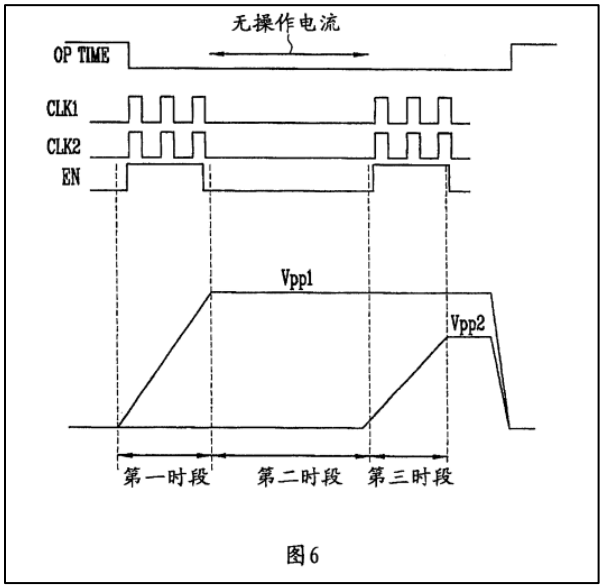
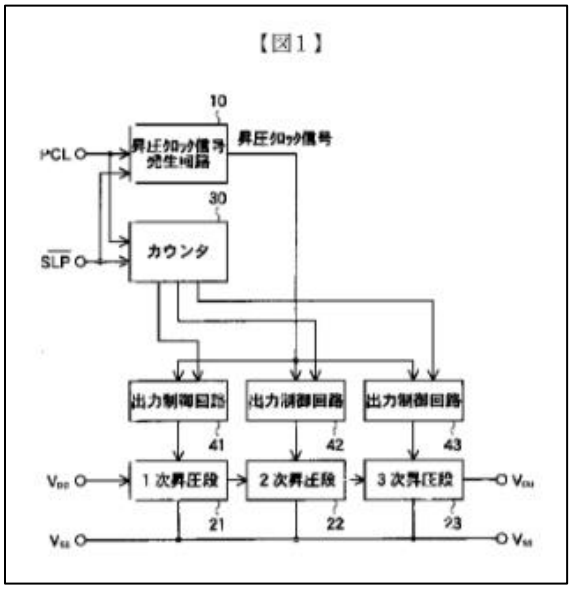


图6

Ito-633 at [0018] and Fig. 1:

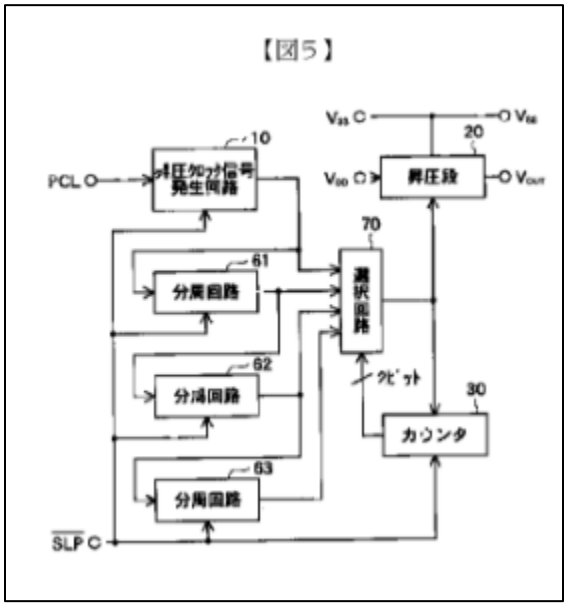
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

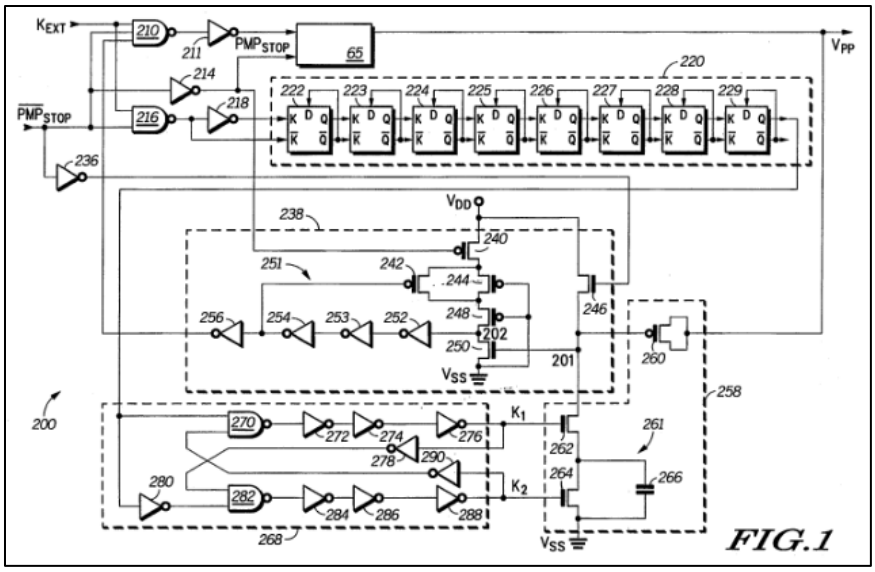


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

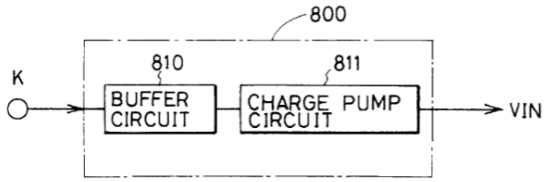


FIG.57

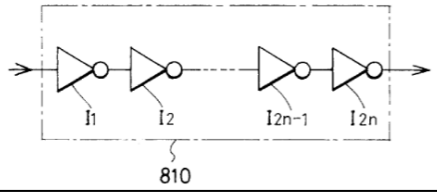


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

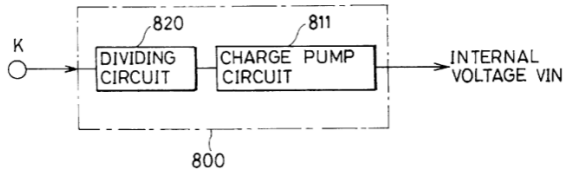
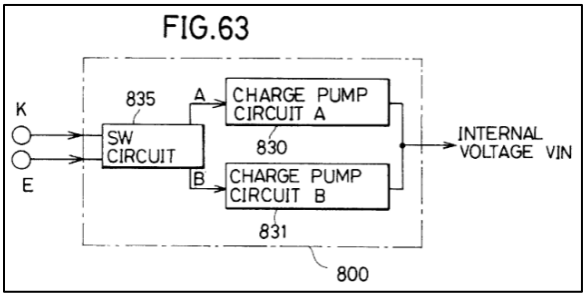


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



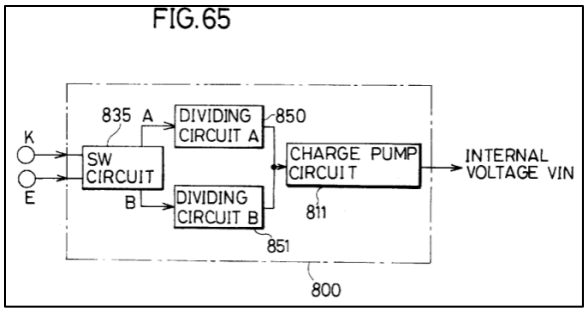
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

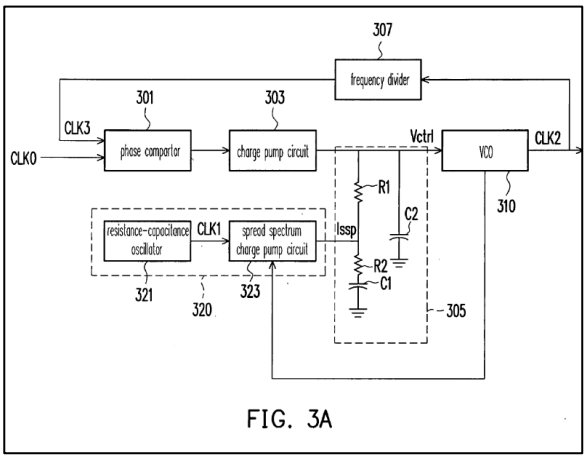


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

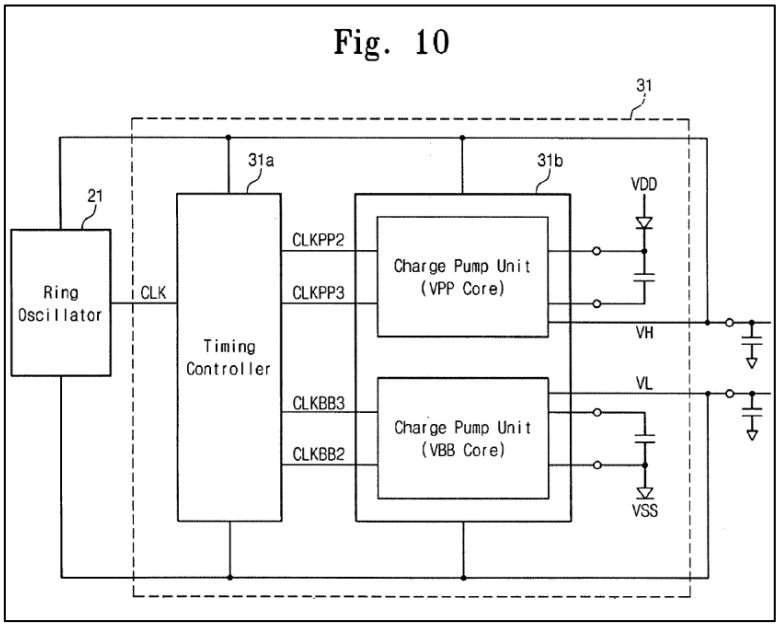


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

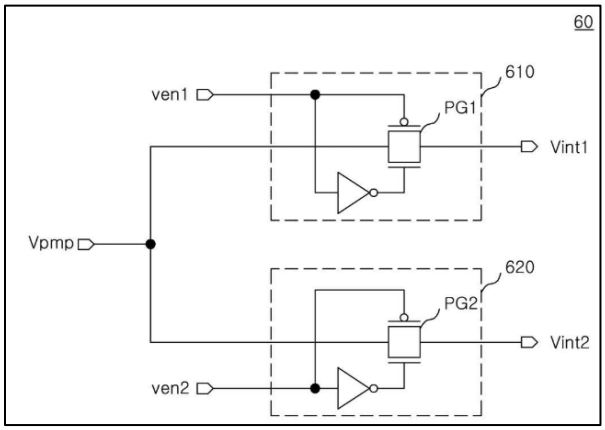
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

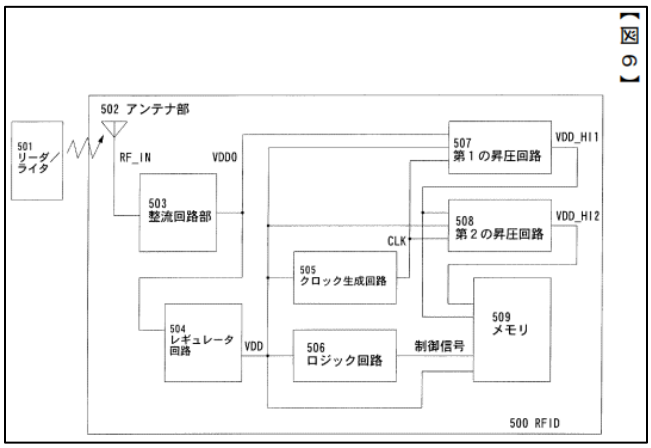
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

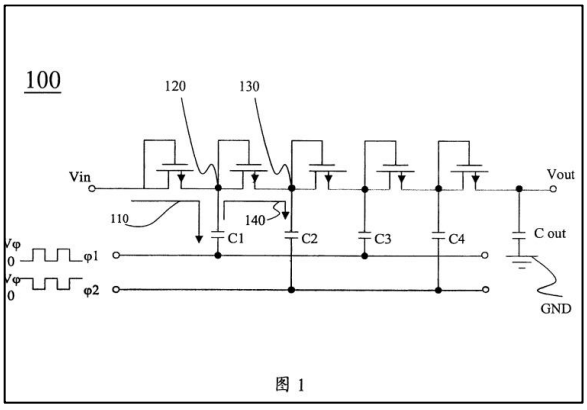
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

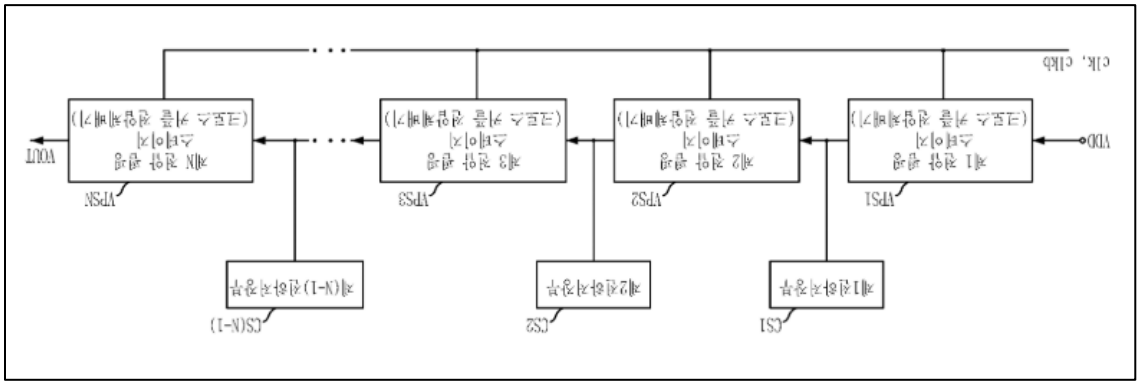
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

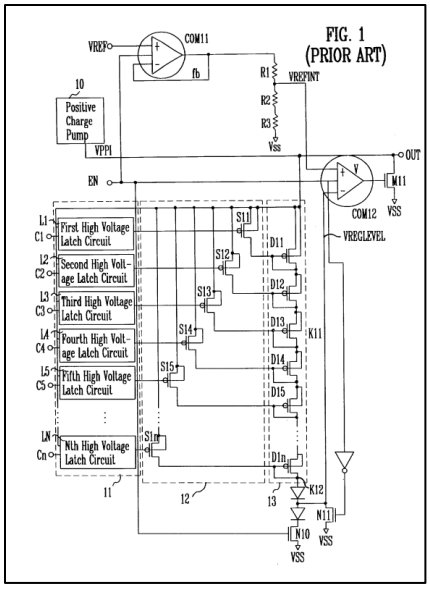
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



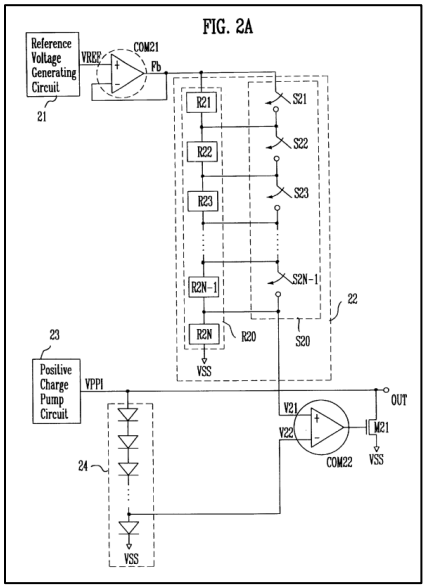
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

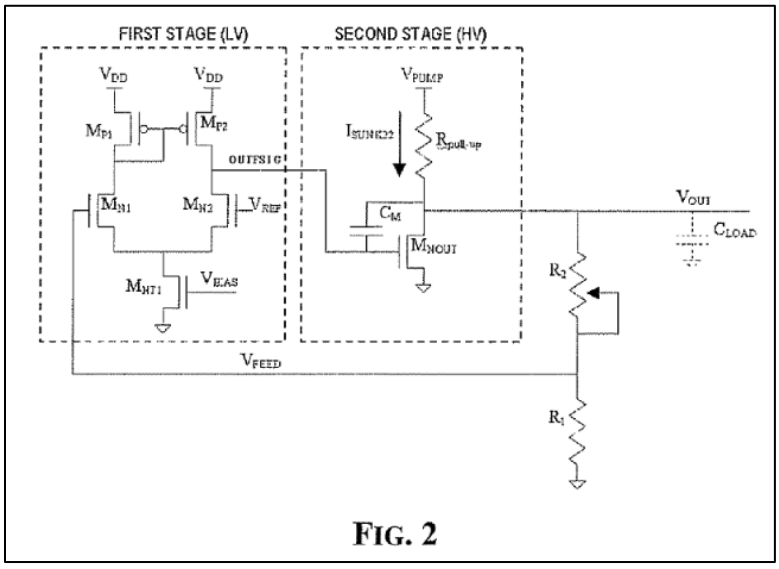


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

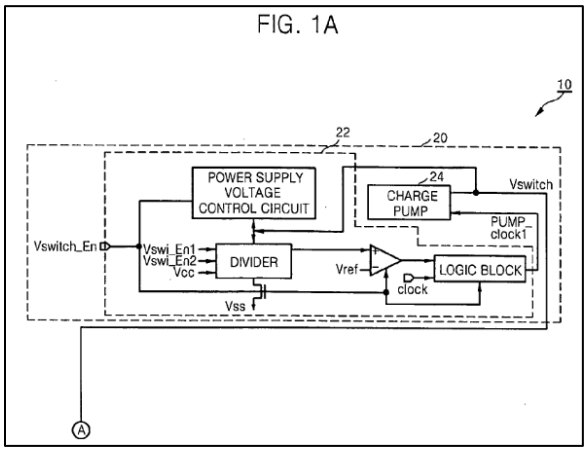
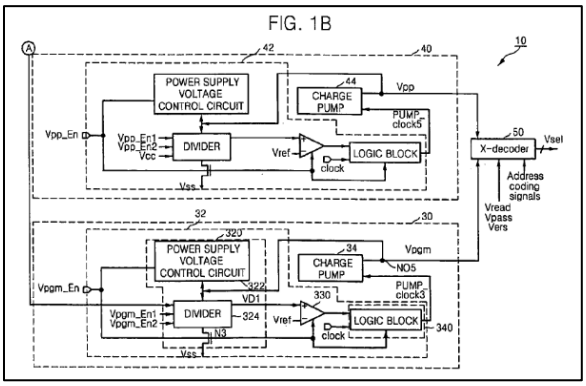
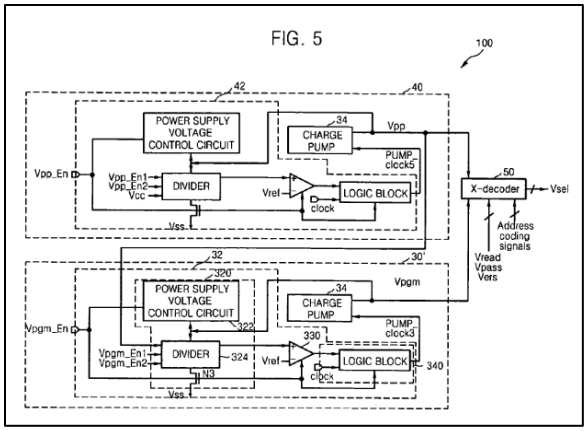


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

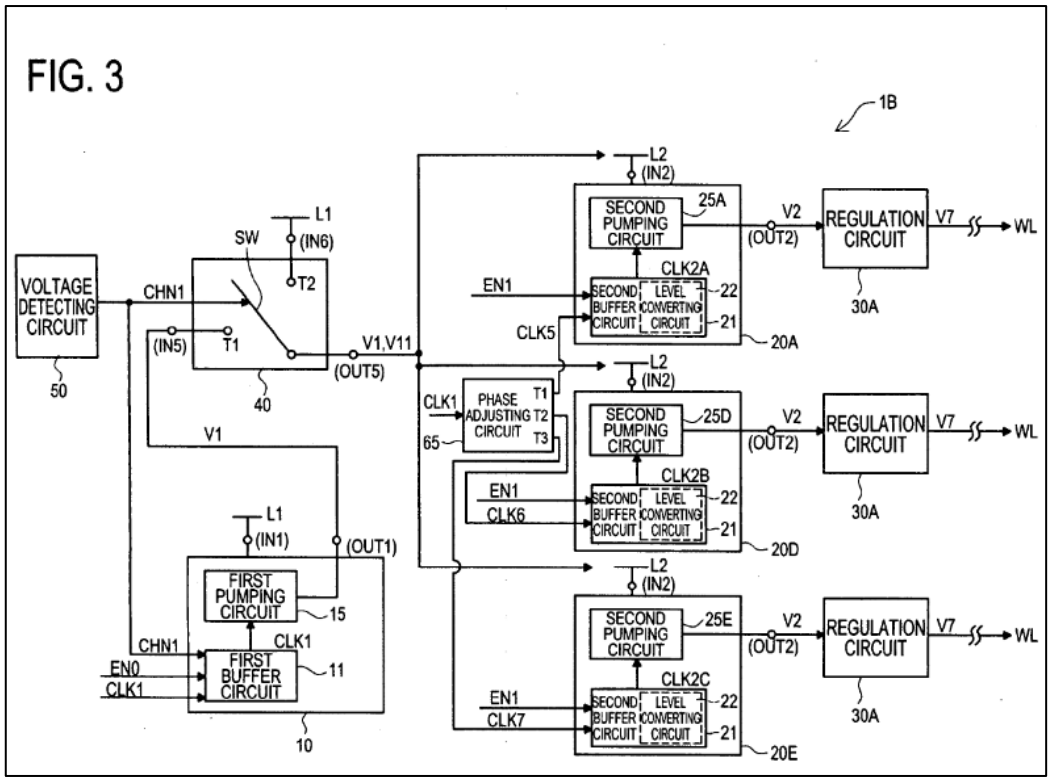
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

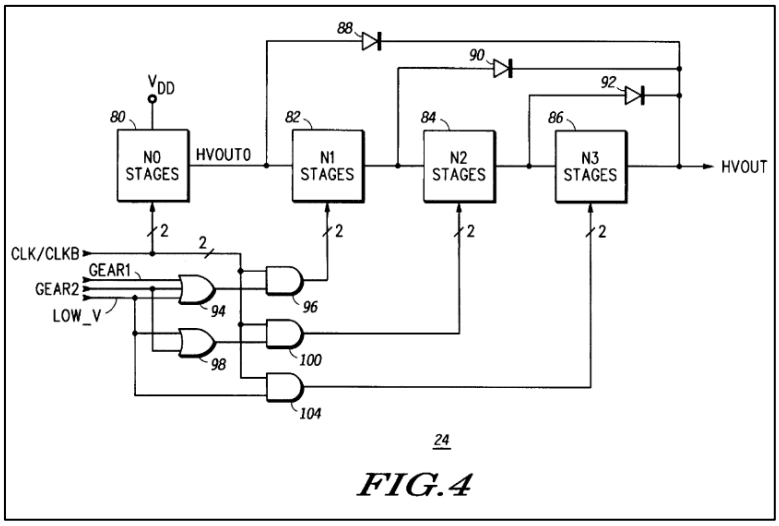


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

6[e] the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.

The Omnibus References disclose and/or render obvious the frequency of the clock signal to be supplied to the second charge pump circuit is changed to a frequency which is obtained by dividing an original frequency.

See, e.g., claim limitations 1[d] and 1[e], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

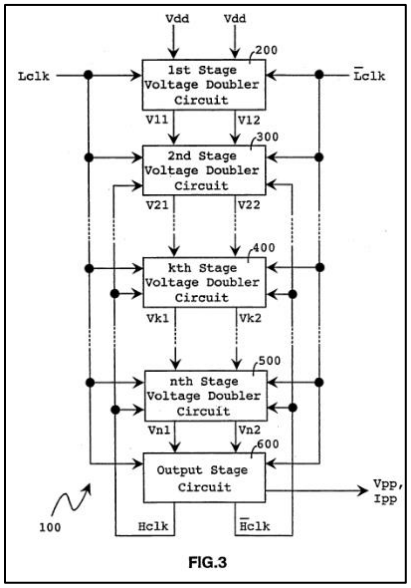


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

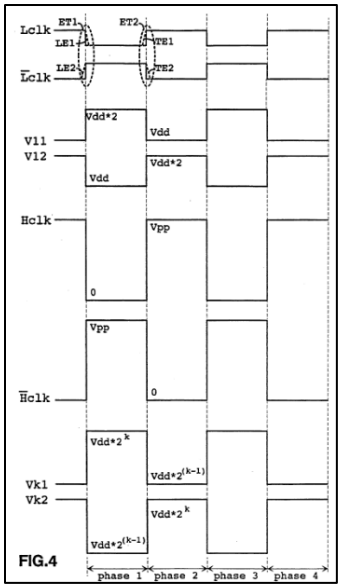


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This

is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

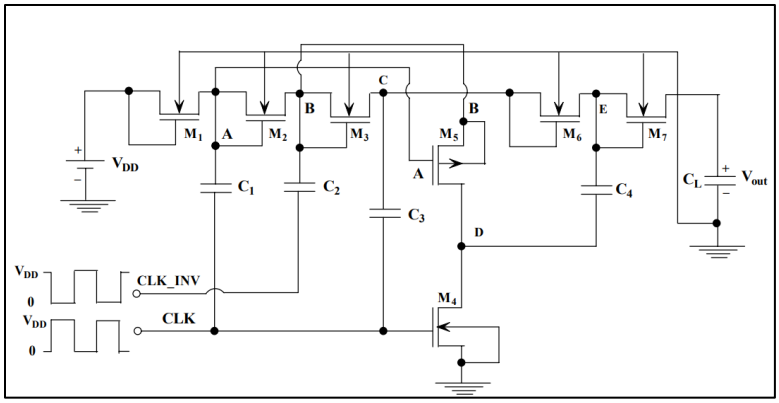
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

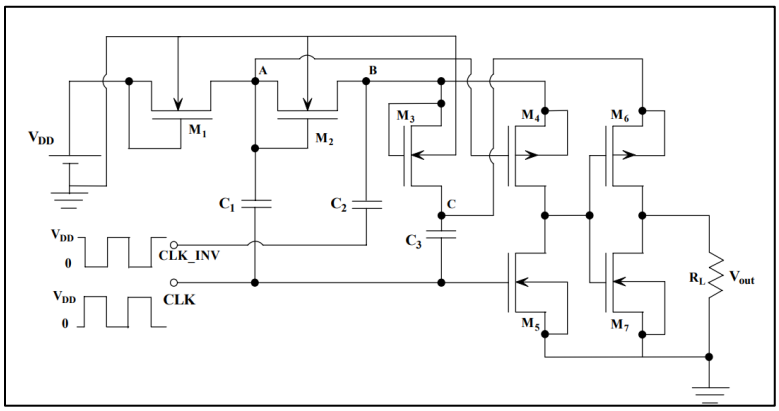
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

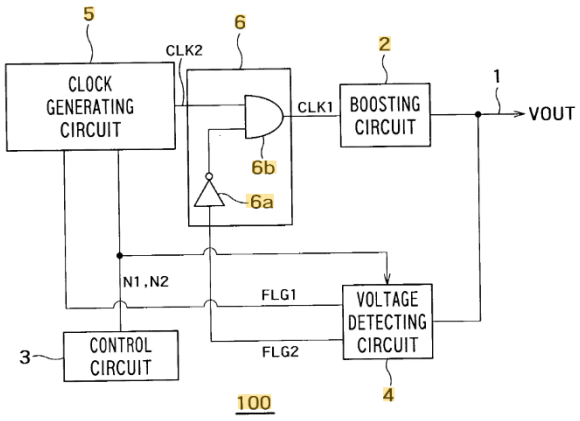


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

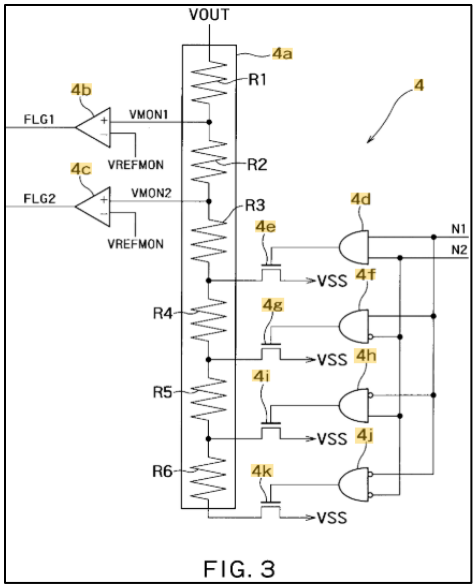


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

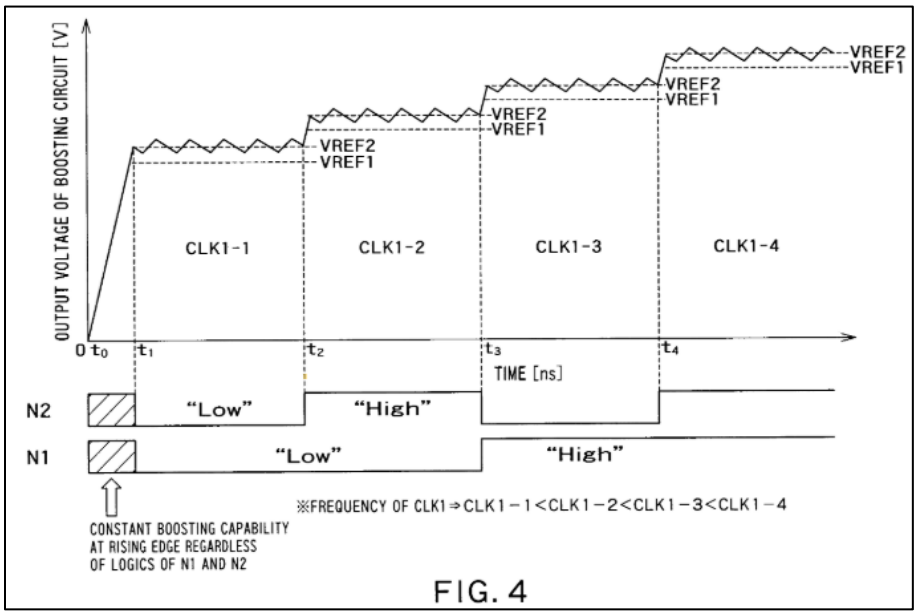


FIG. 4

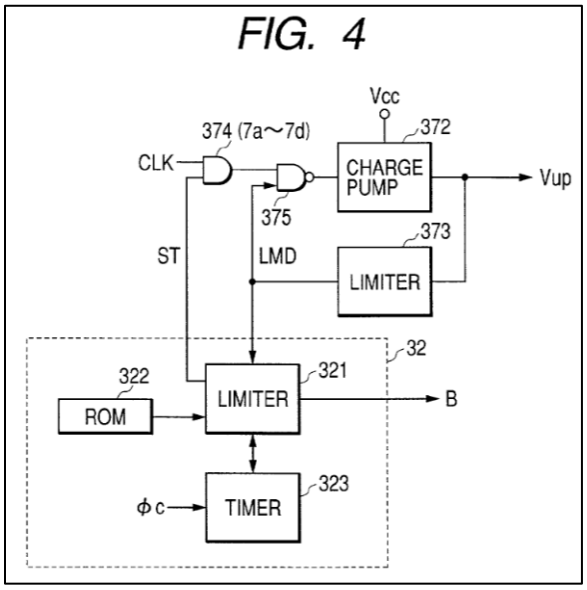
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

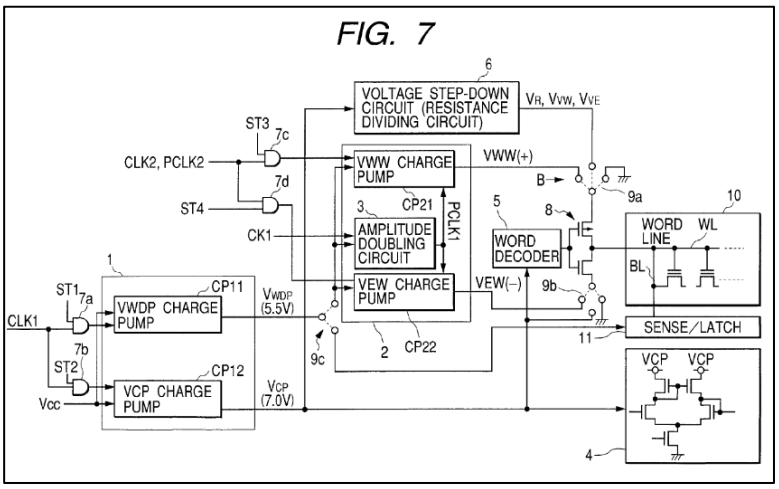
Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

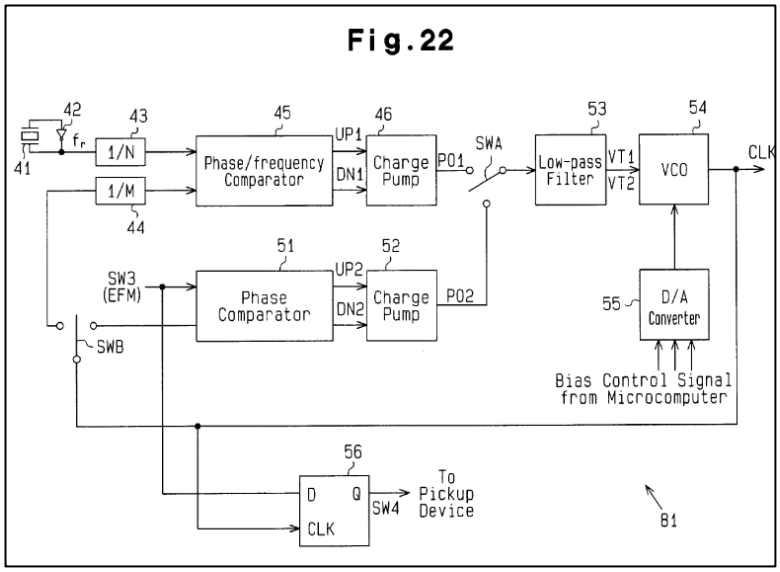
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

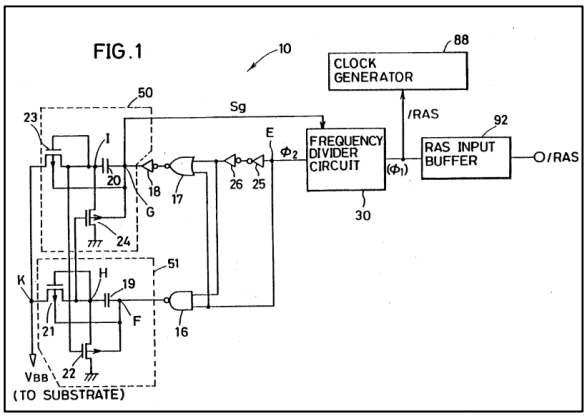


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

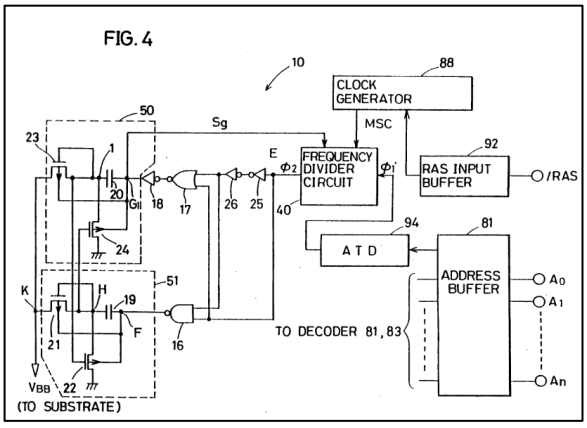
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

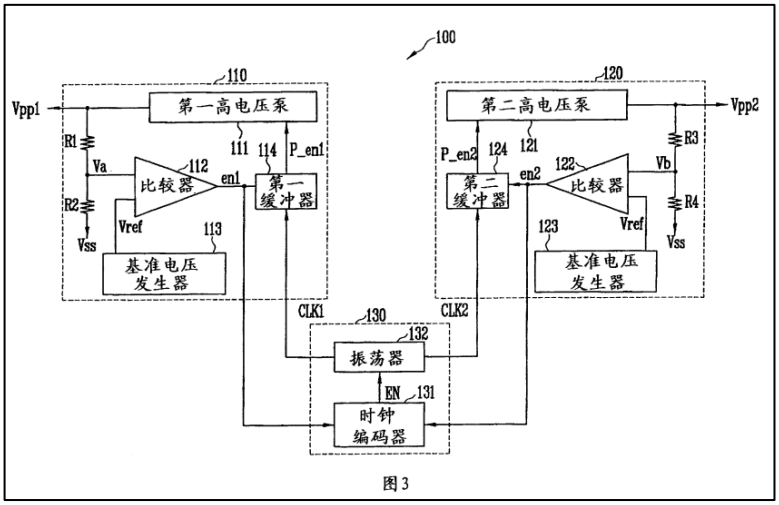


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

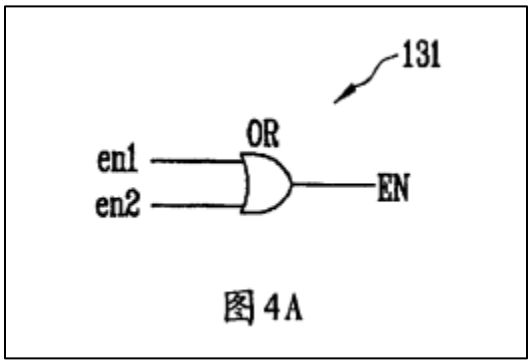


图 4A

Jiang at Fig. 6:

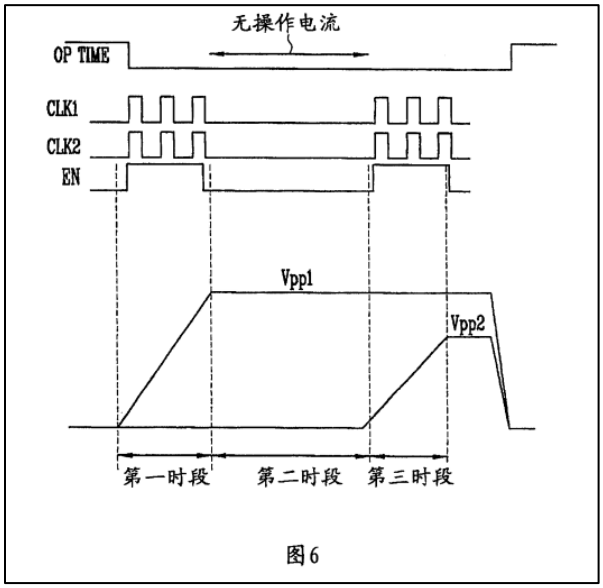
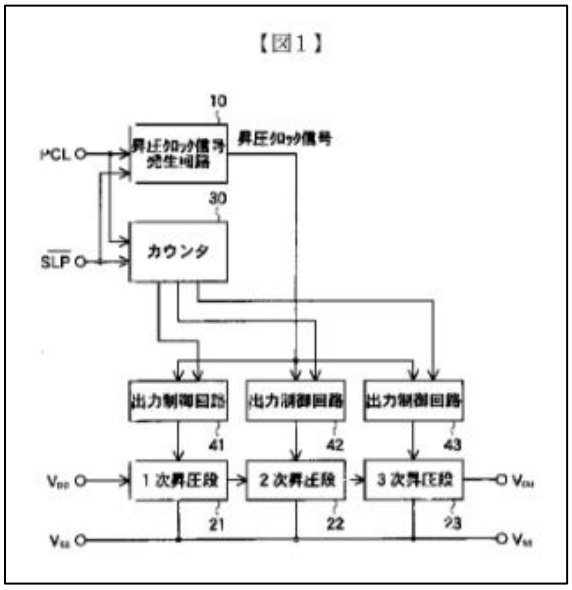


图6

Ito-633 at [0018] and Fig. 1:

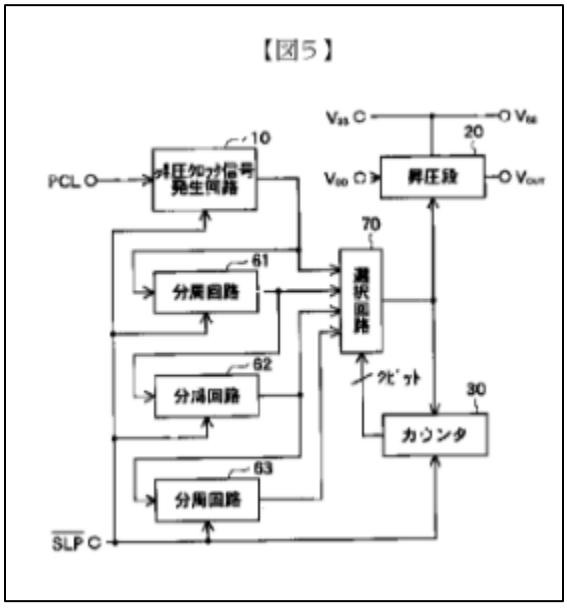
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

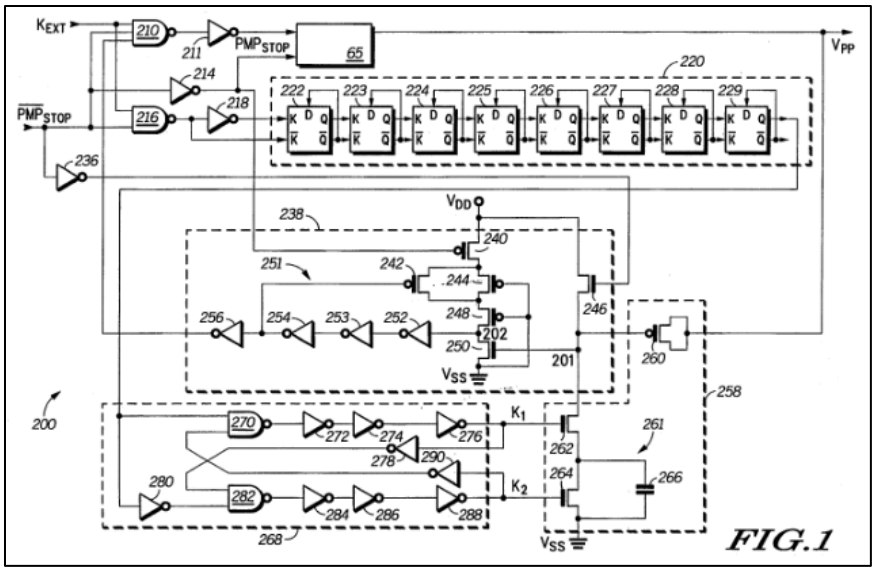


FIG.1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

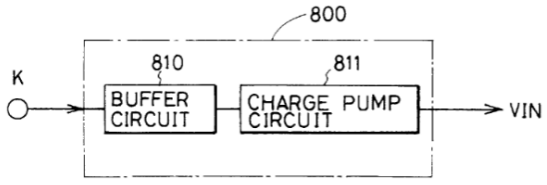


FIG.57

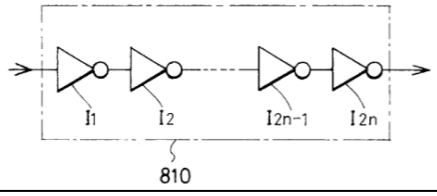


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

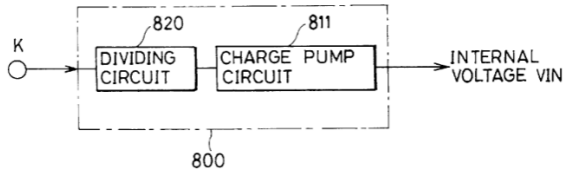
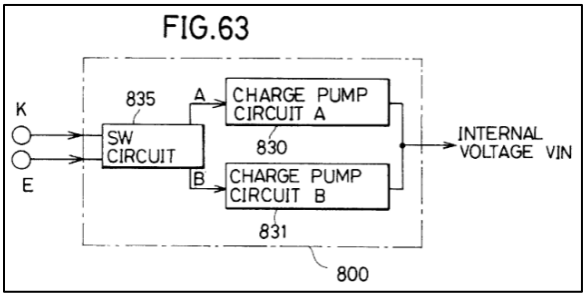


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



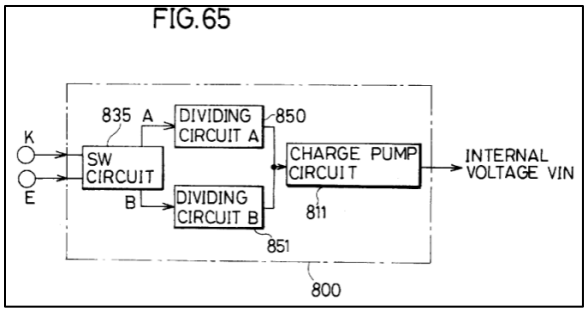
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

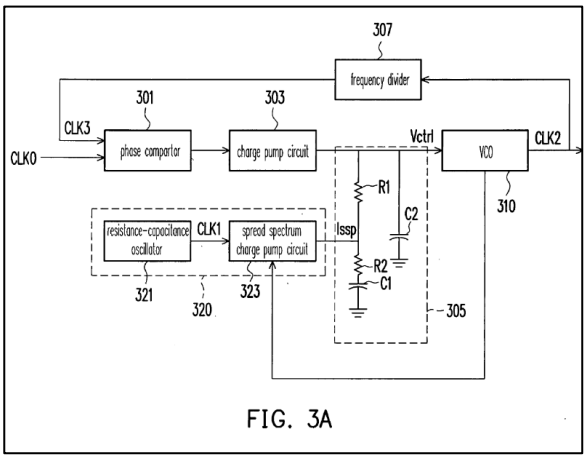


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

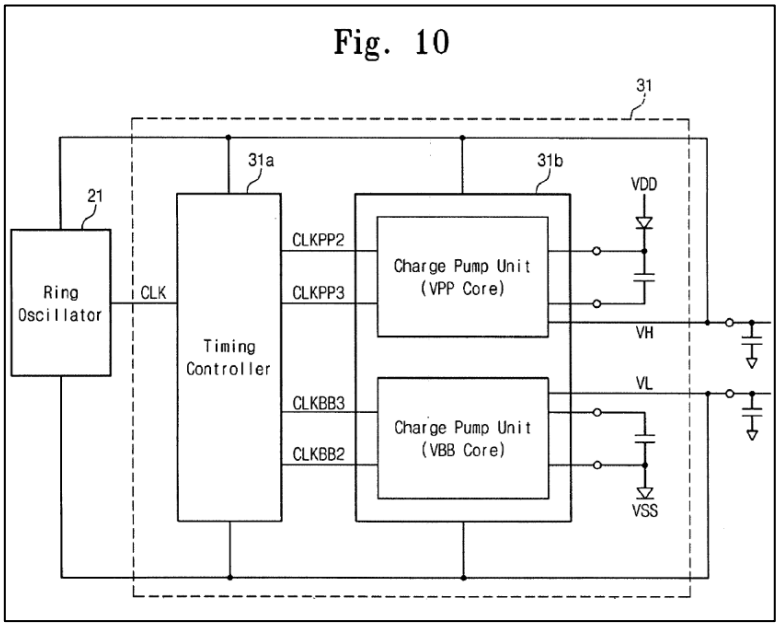


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

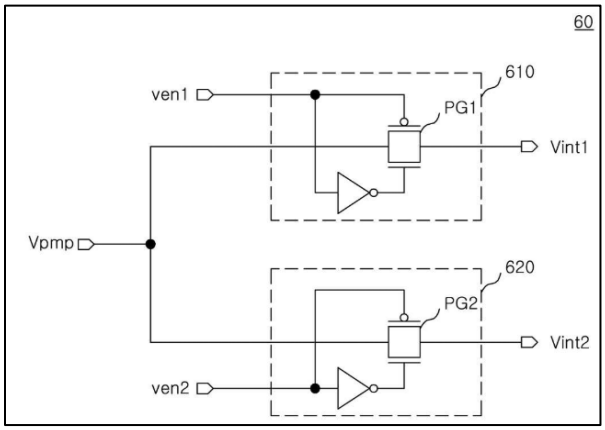
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

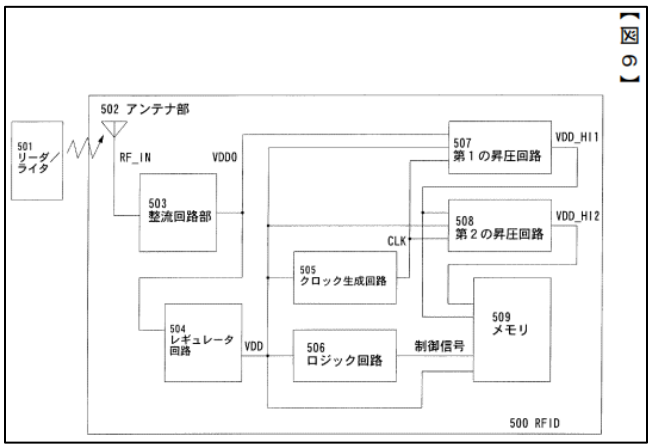
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

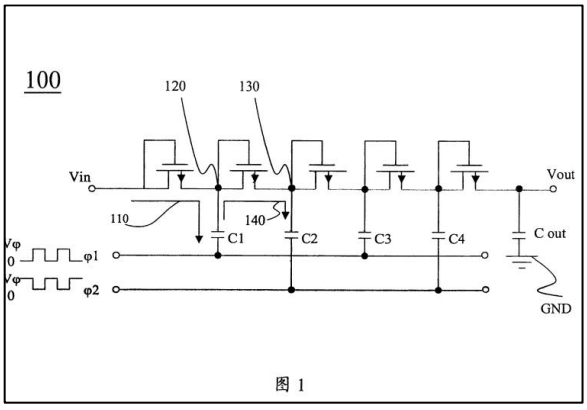
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

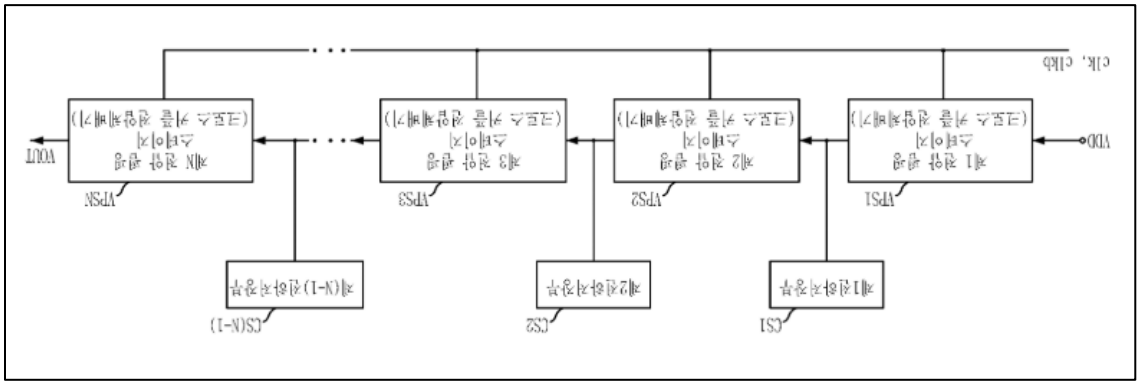
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

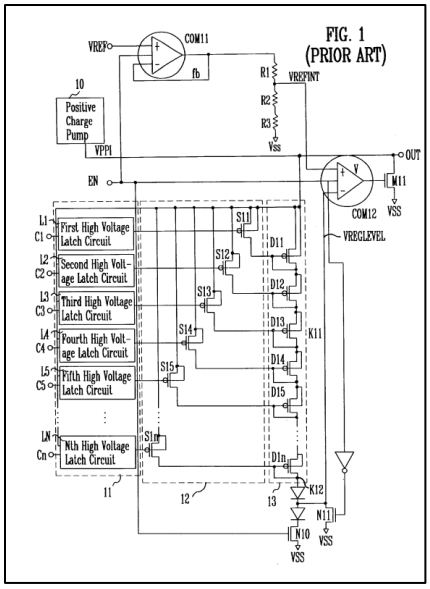
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



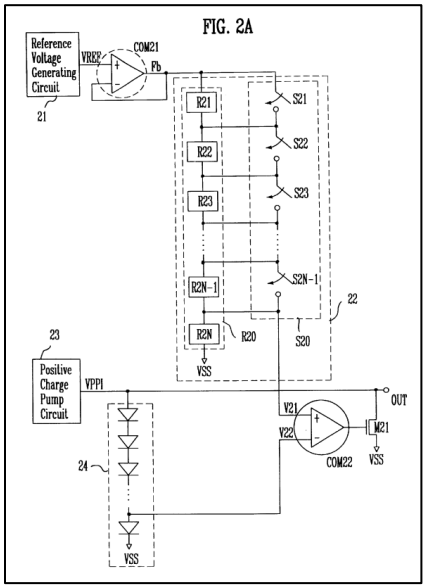
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

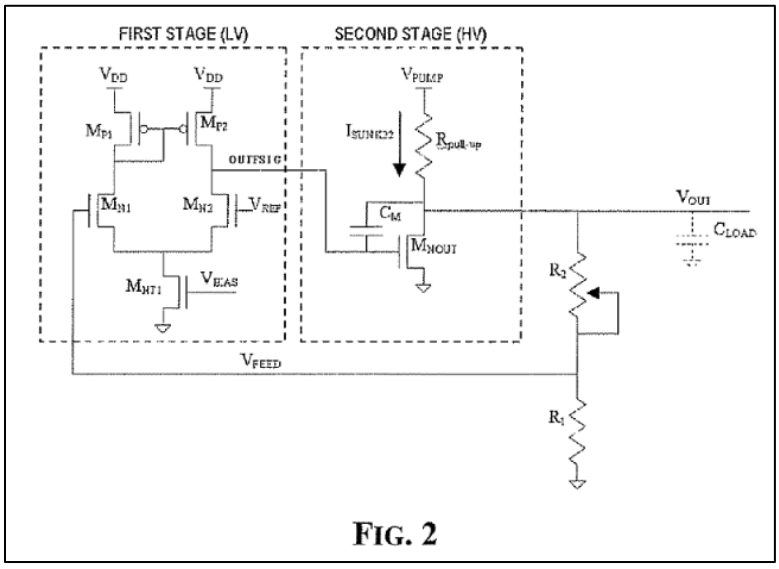


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

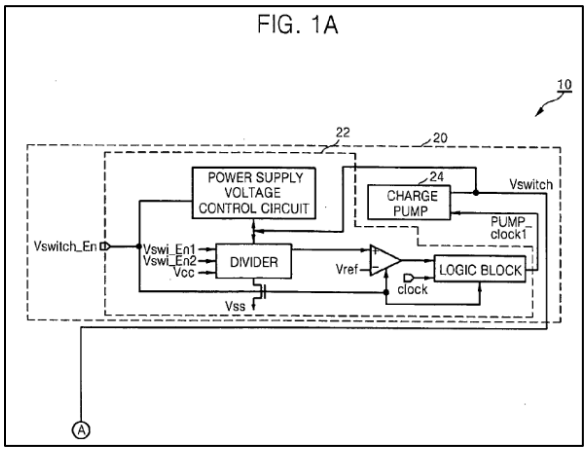
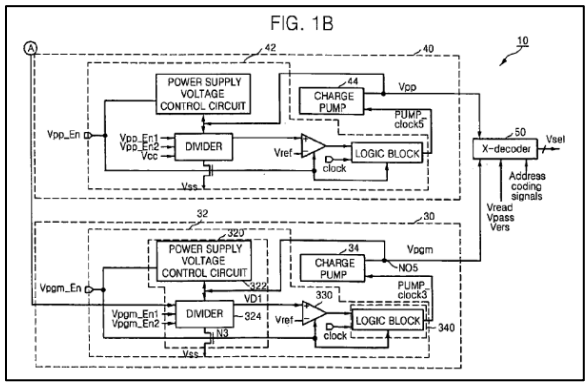
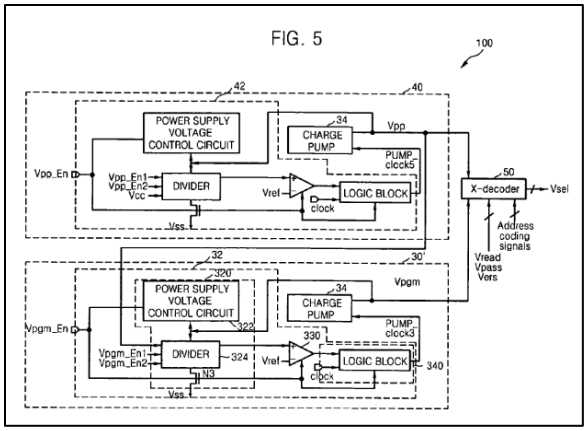


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

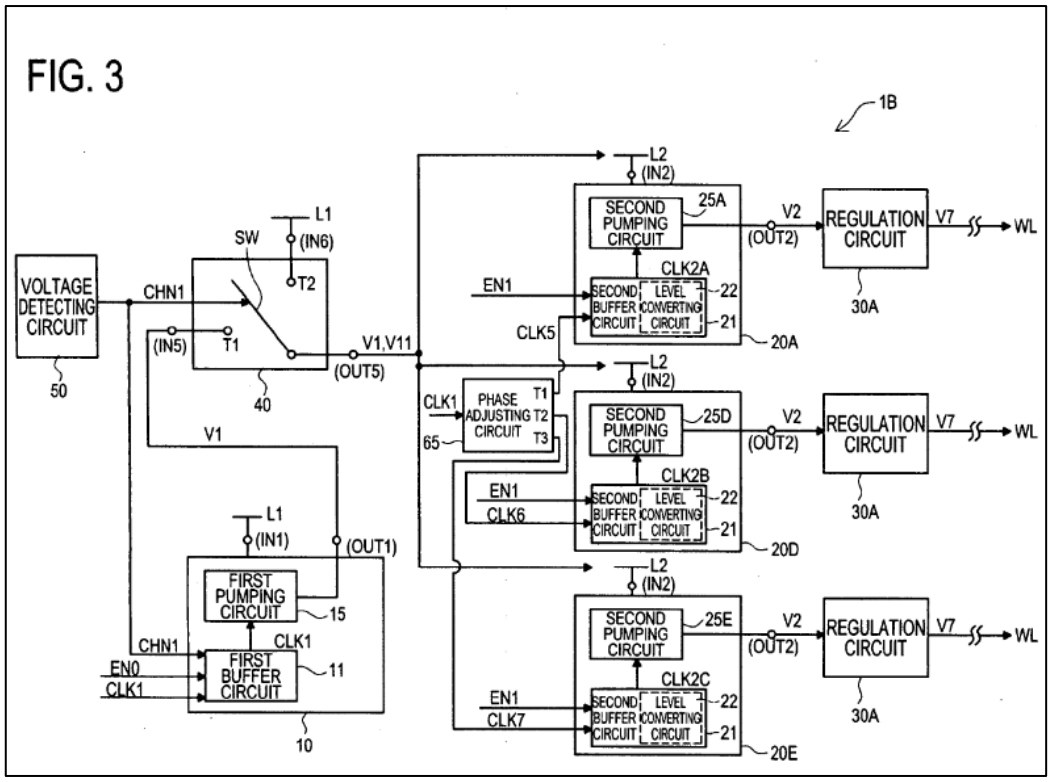
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

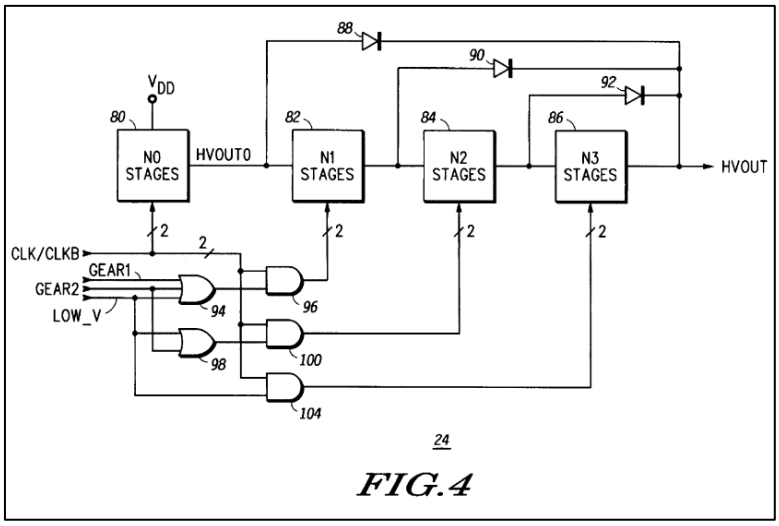


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

7[a] An internal voltage generating circuit comprising:

To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious an

internal voltage generating circuit .

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

7[b] a first charge pump circuit configured to generate a second voltage from a first voltage; and

The Omnibus References disclose and/or render obvious a first charge pump circuit configured to generate a second voltage from a first voltage.

See, e.g., claim limitation 1[b], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

7[c] a second charge pump circuit configured to generate a third voltage from the second voltage,

The Omnibus References disclose and/or render obvious a second charge pump circuit configured to generate a third voltage from the second voltage.

See, e.g., claim limitation 1[c], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

7[d] wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.

The Omnibus References disclose and/or render obvious wherein a length of a period in which a clock signal to be supplied to the second charge pump circuit is in a high state is changed in accordance with a control signal.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that

when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

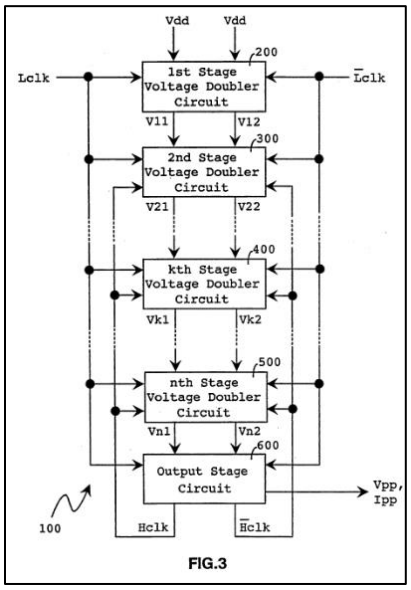


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

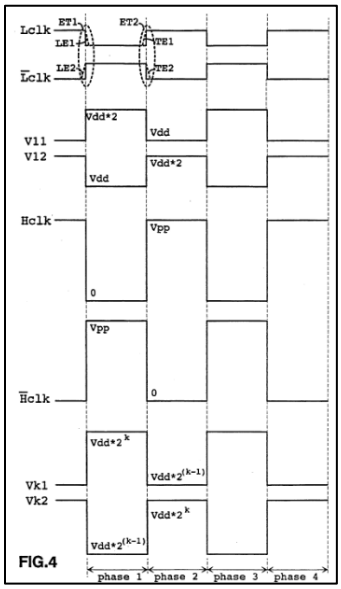
In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is

HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.



Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter

and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and

AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

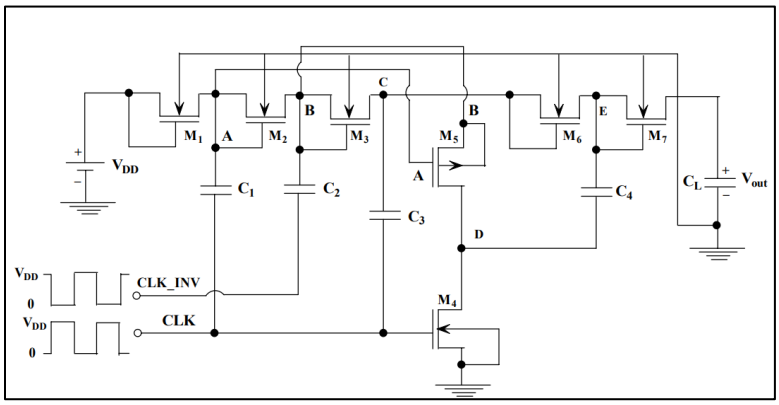
The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

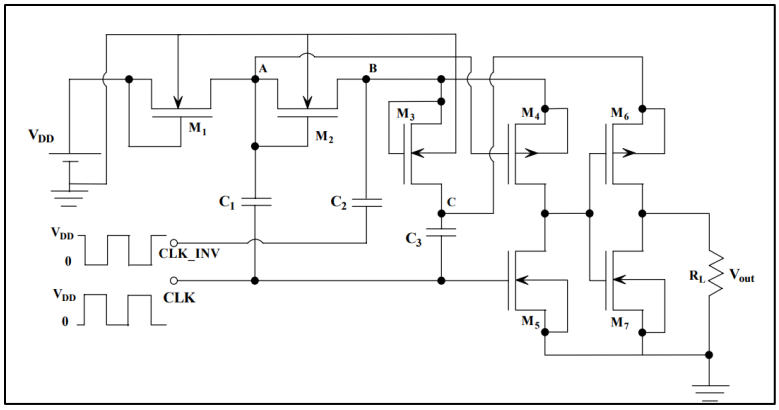
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

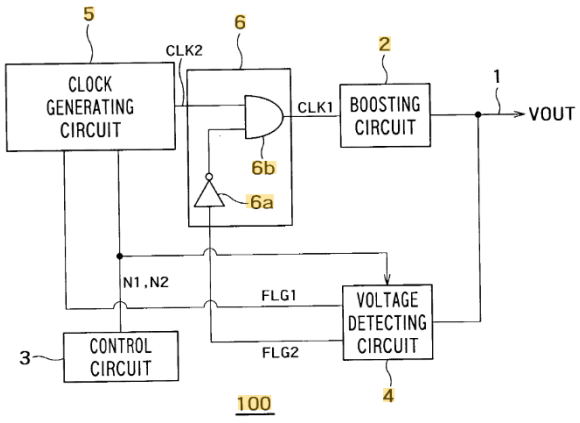


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating

circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

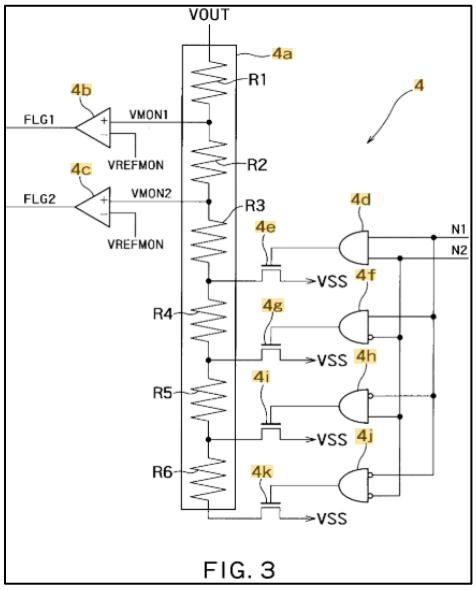


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5

includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

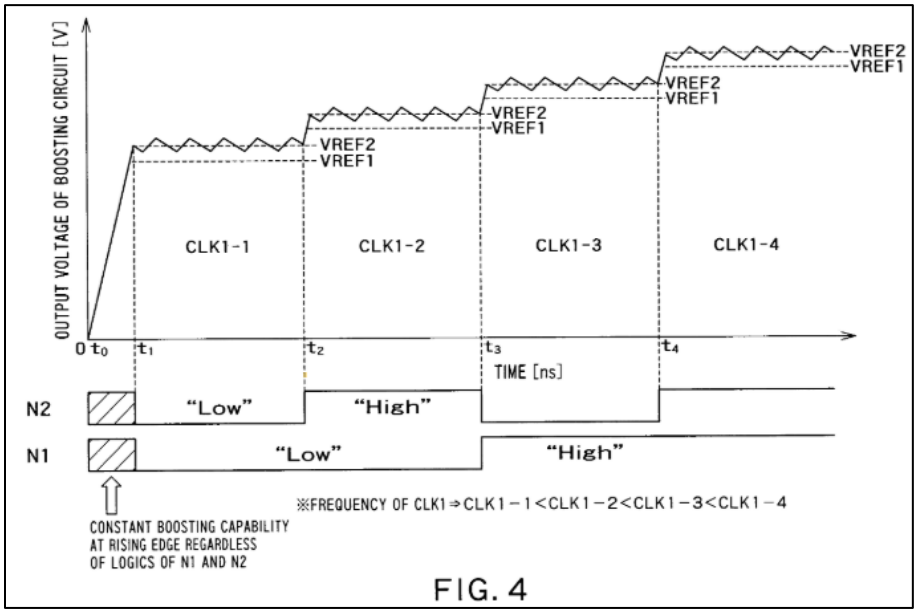


FIG. 4

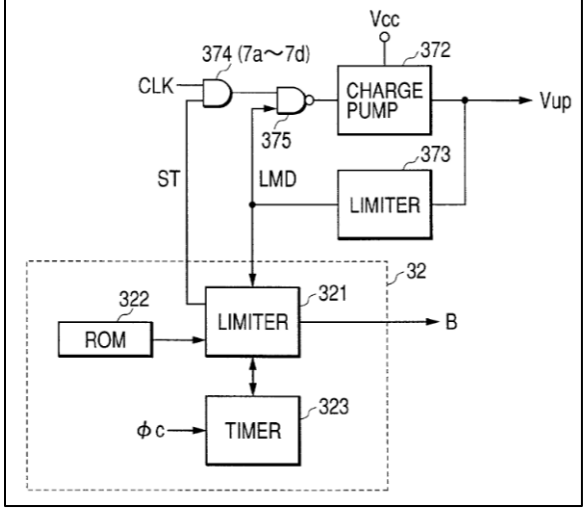
Sato at [0051]:

Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

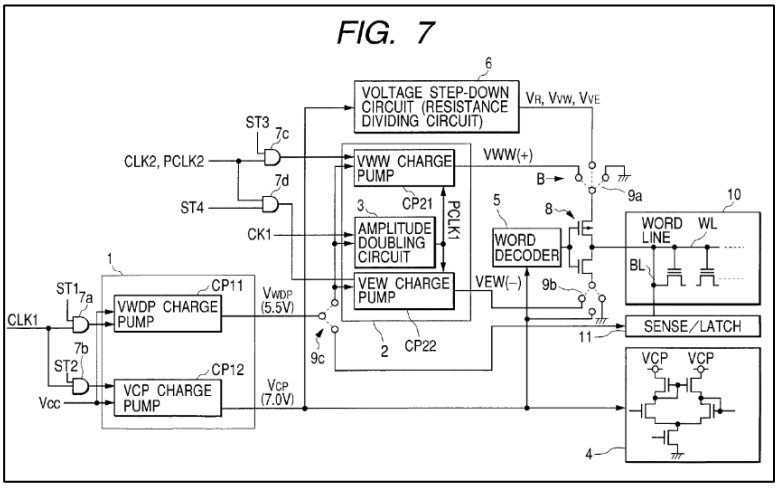
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory

having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted,

the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2 goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

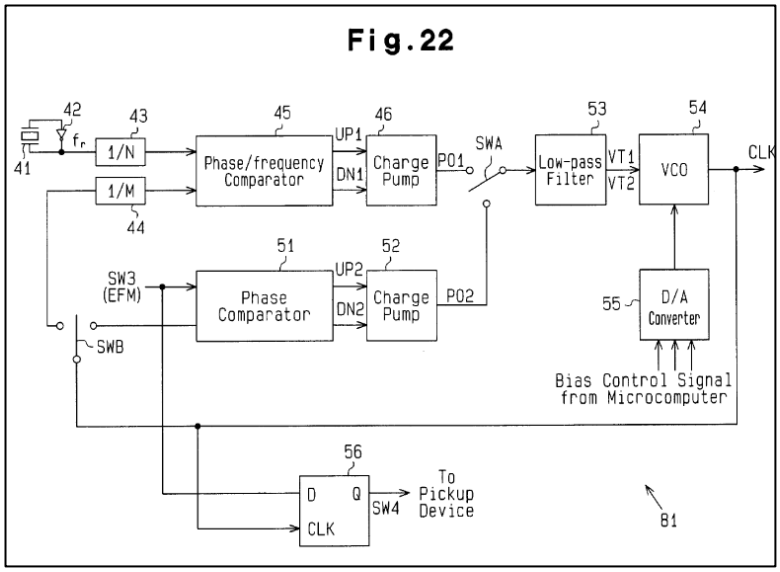
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

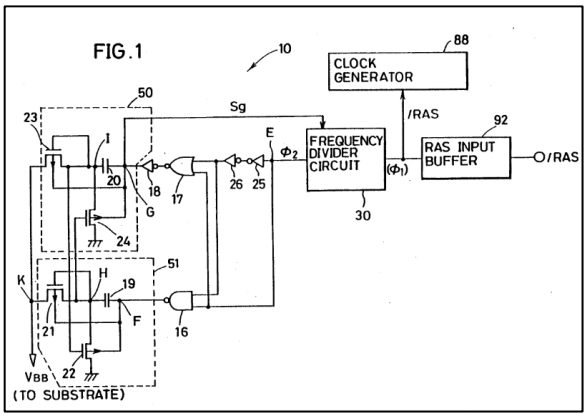


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

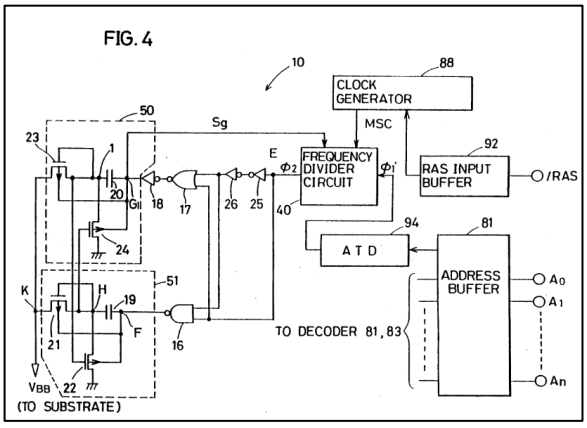
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

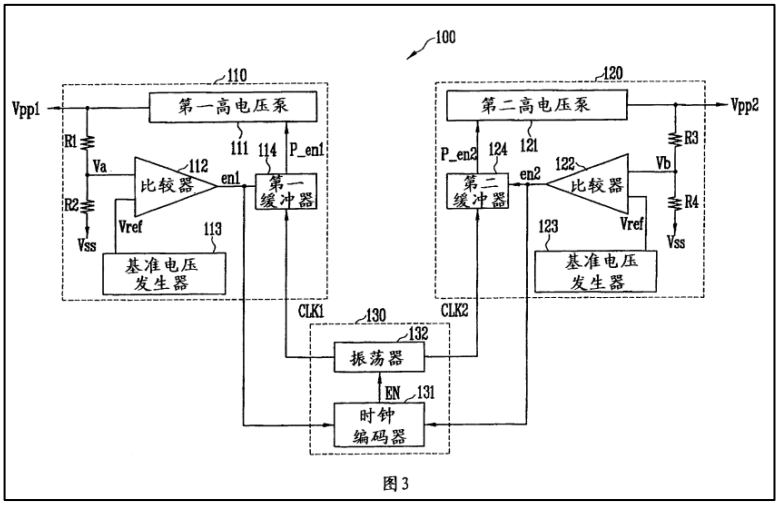


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

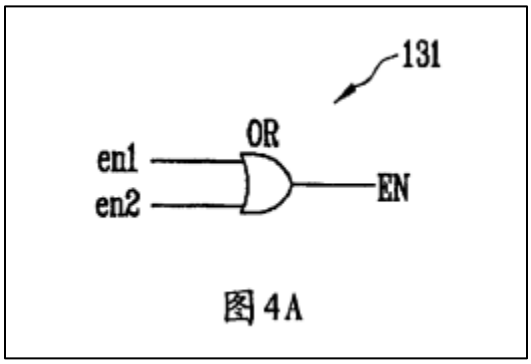


图 4A

Jiang at Fig. 6:

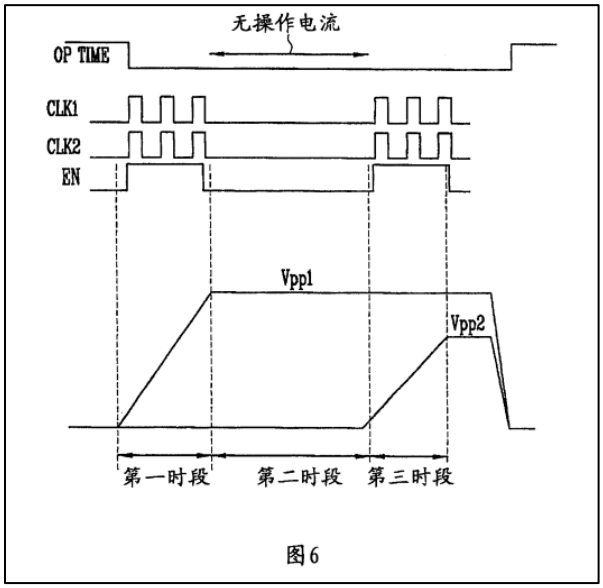
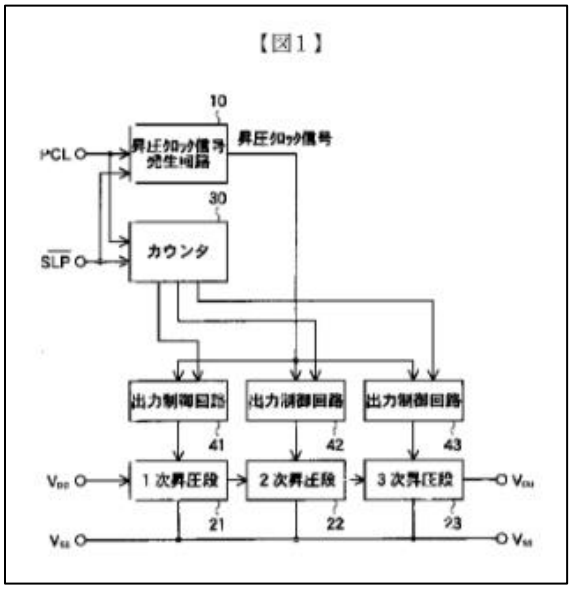


图6

Ito-633 at [0018] and Fig. 1:

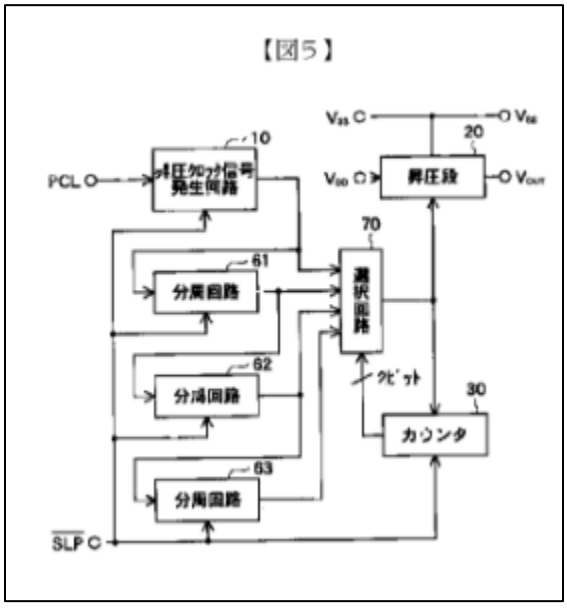
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

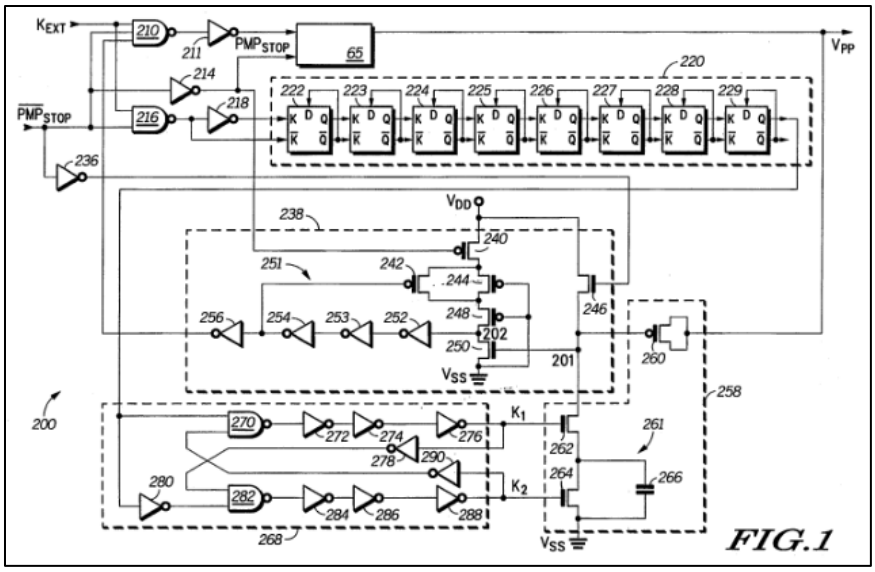


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

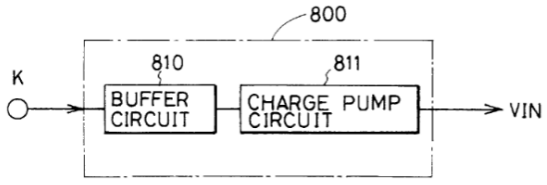


FIG.57

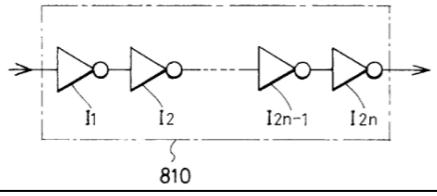


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

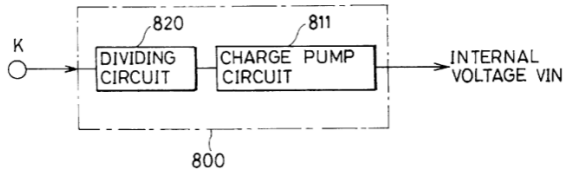
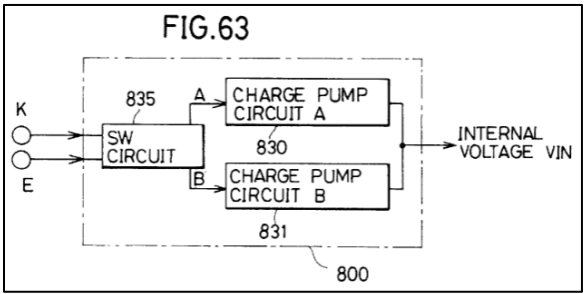


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

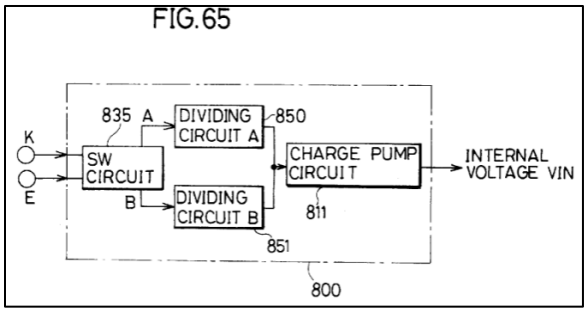
Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.

FIG.65



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

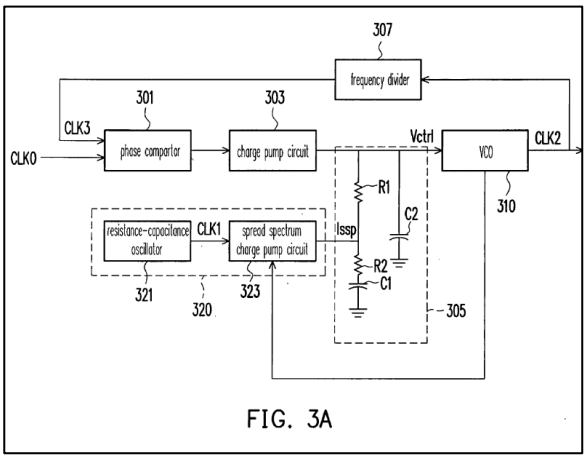


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

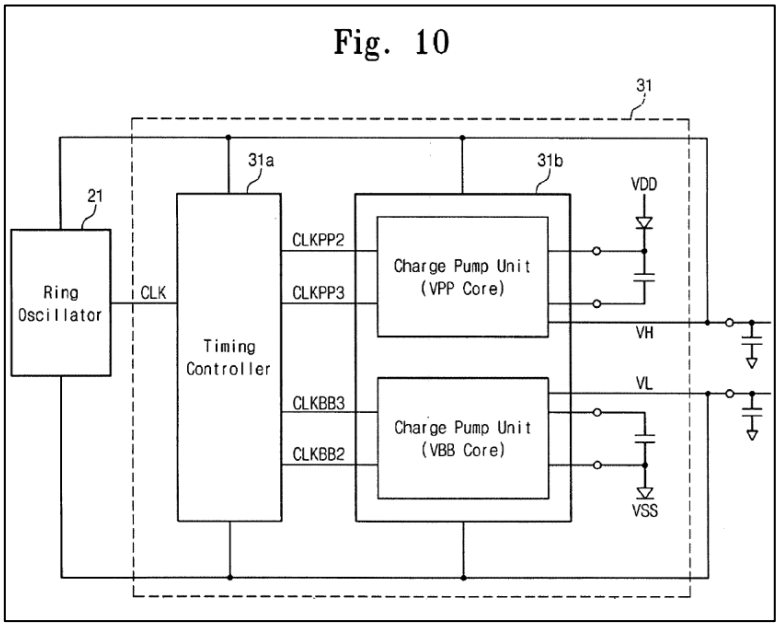


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

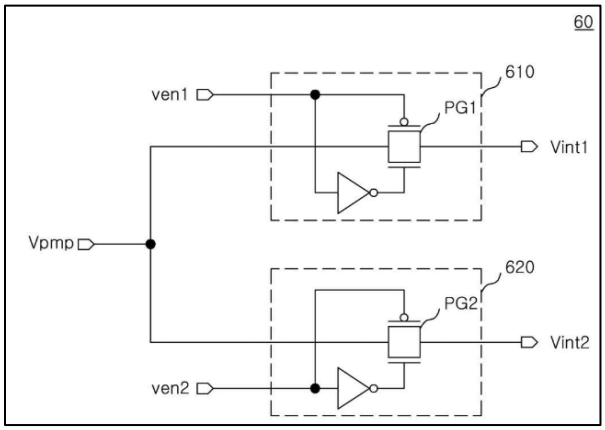
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

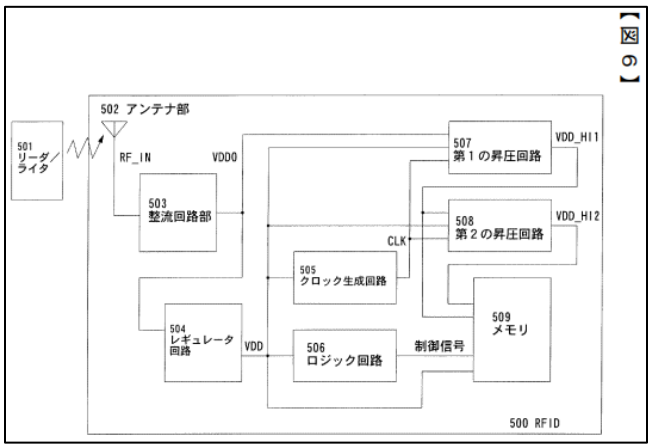
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

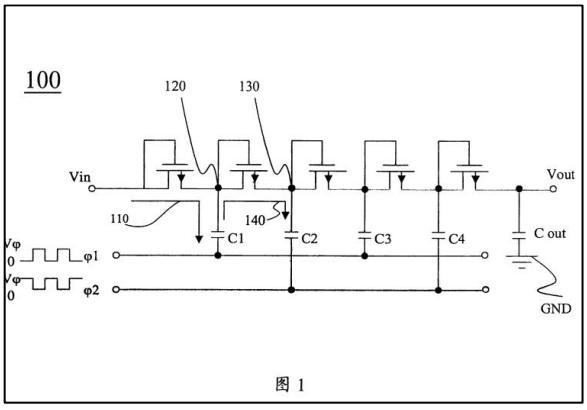
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

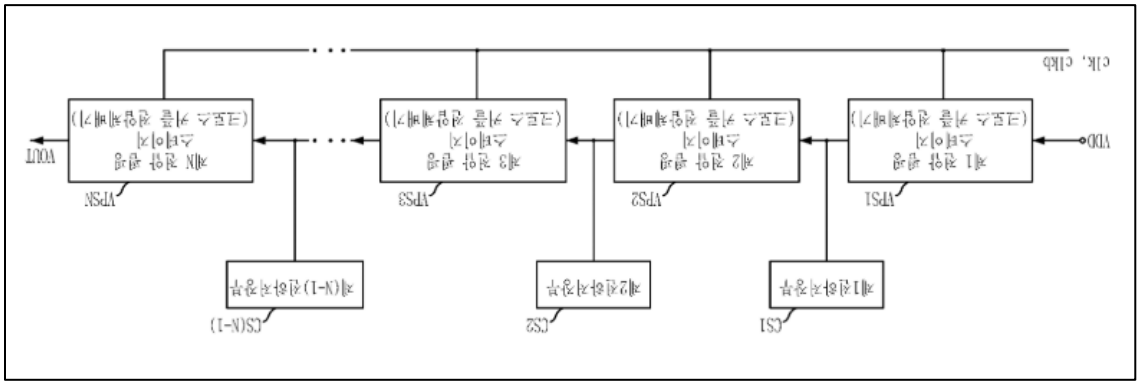
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

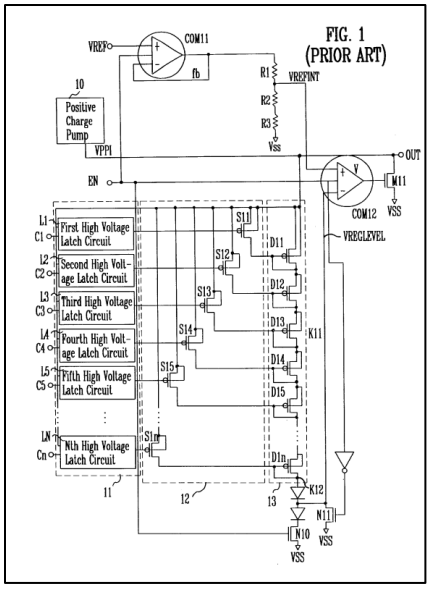
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



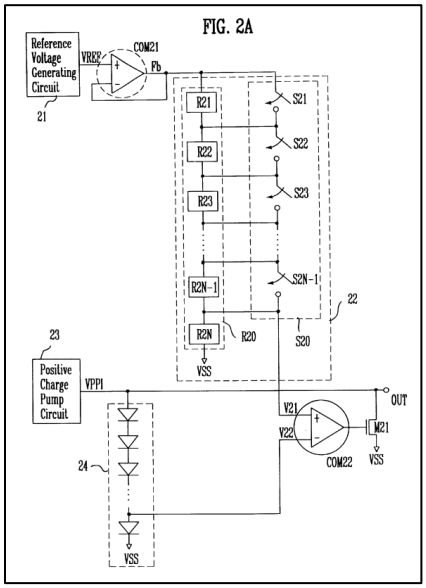
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

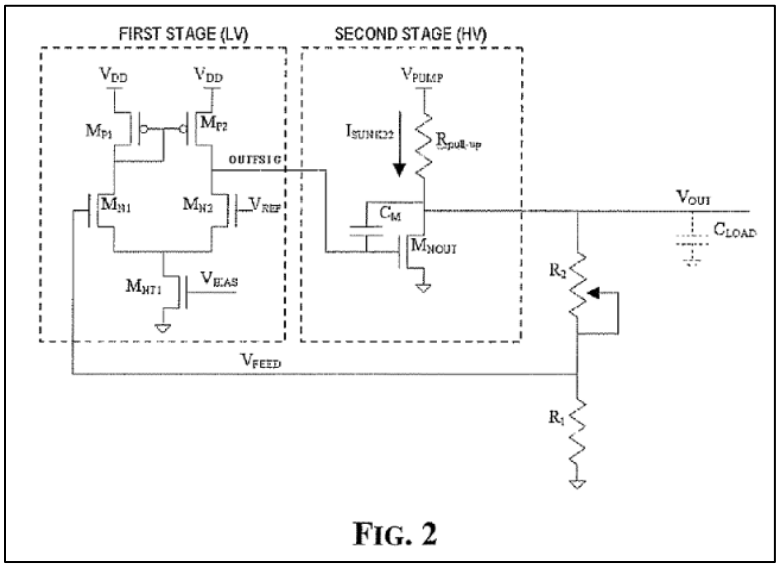


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

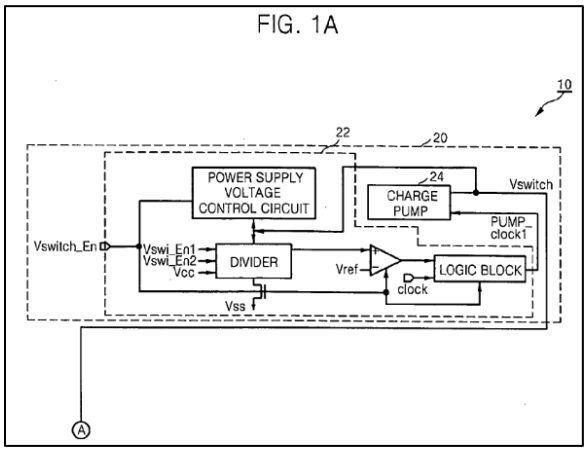
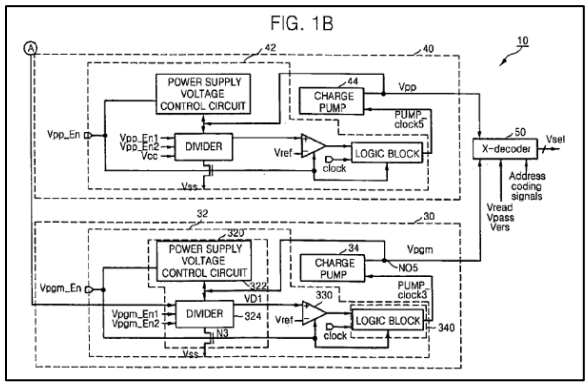
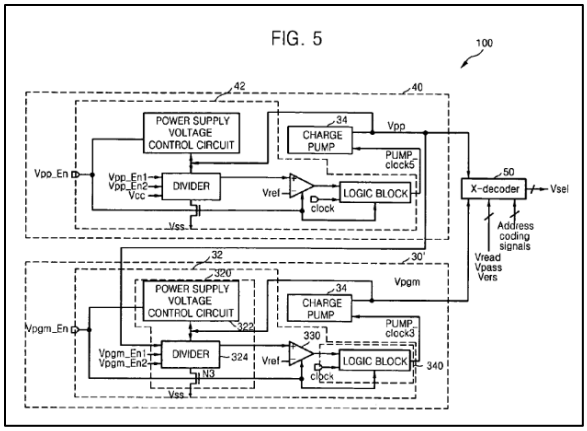


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

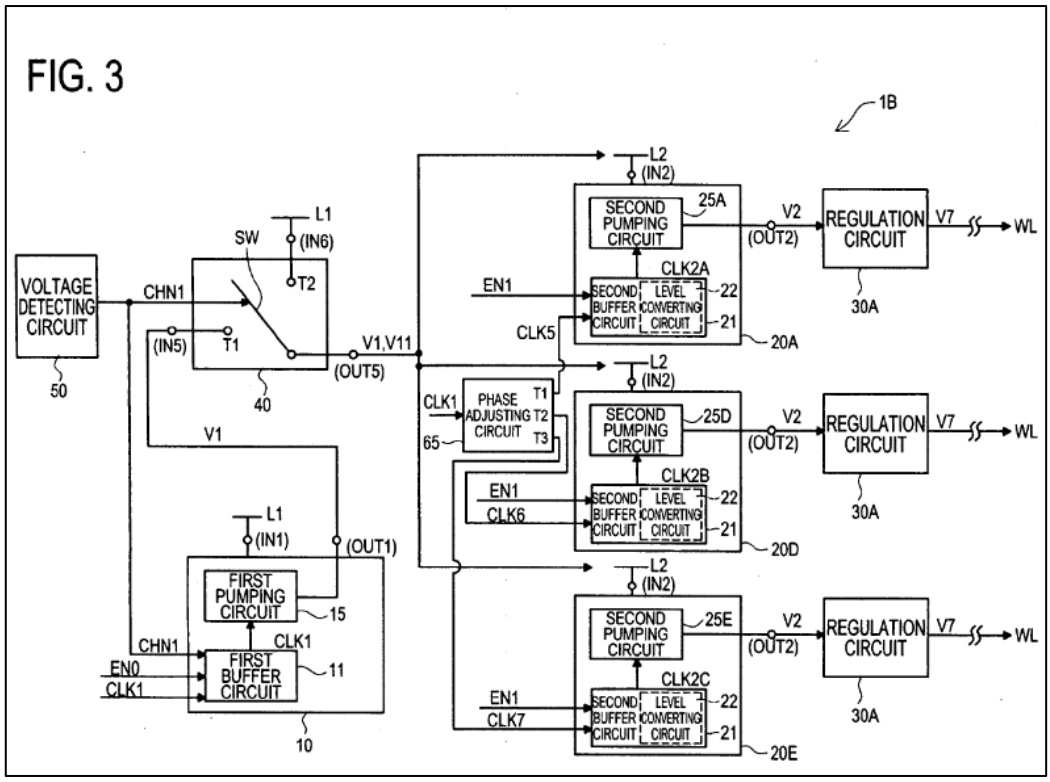
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

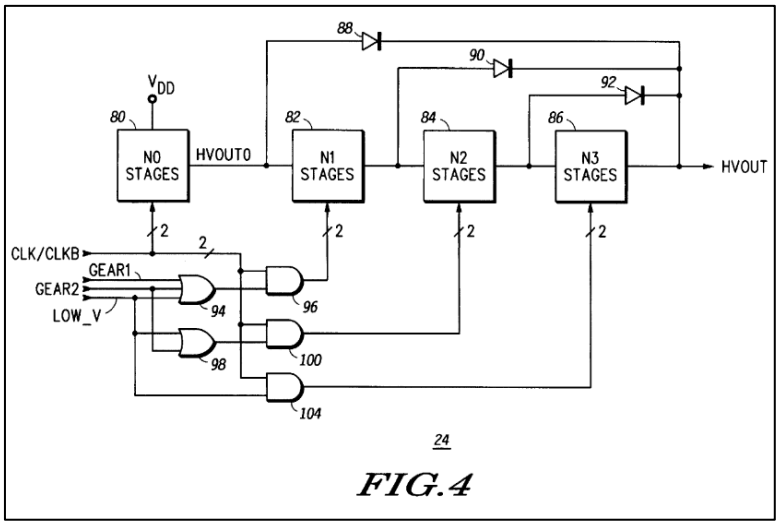


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

8[a] The internal voltage generating circuit of claim 7,

To the extent the preamble is limiting, The Omnibus References disclose and/or render obvious an

internal voltage generating circuit .

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.

8[b] wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.

The Omnibus References disclose and/or render obvious wherein the length of a period in which the clock signal to be supplied to the second charge pump circuit is in a high state is changed to a frequency which is obtained by dividing an original frequency.

See, e.g., claim limitation 7[d], *supra*.

Cernea at Abstract:

A charge pump circuit comprises a plurality of voltage doubler circuits connected together such that a first voltage output generated by a first portion of a kth one of the voltage doubler circuits is substantially equal to Vdd*2k and Vdd*2k-1) on odd and even phases, respectively, of a first clock signal, and a second voltage output generated by a second portion of the kth one of the voltage doubler circuits is substantially equal to Vdd*2k-1) and Vdd*2k on the odd and even phases, respectively, of the first clock signal. Each of the voltage doubler circuits is constructed such that when its first portion is providing a voltage of Vdd*2k and a current to a next stage, its second portion is recharging a capacitor in that portion to Vdd*2k-1), and when its second portion is providing a voltage of Vdd*22 and a current to the next stage, its first portion is recharging a capacitor in that portion to Vdd*2k-1). An output circuit is connected to a last one of the voltage doubler circuits to provide other circuitry with a substantially constant output voltage Vpp and output current Ipp, by providing such voltage and current from a first voltage output of the last voltage doubler circuit on odd phases of the first clock signal, and from a second voltage output of the last voltage doubler circuit on even phases of the first clock signal.

Cernea at 4:26-58 and Fig. 3:

FIG. 3 illustrates, as an example, a block diagram of a charge pump circuit 100, utilizing aspects of the present invention. The charge pump circuit 100 comprises a plurality (e.g., n) of voltage doubler circuits (e.g., 200-500). A 1st stage voltage doubler circuit 200 receives a voltage Vdd from a voltage source (not shown), and generates first and second voltage outputs, V11 and V12, respectively, in response to first and second clock signals, Lclk and Lclk, respectively.

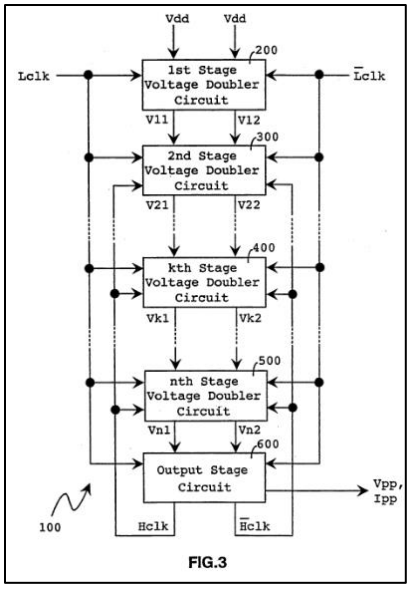


FIG.3

The first voltage output V11 is substantially equal to Vdd*2 and Vdd on first and second phases, respectively, of the first clock signal Lclk, and the second voltage output V12 is substantially equal to Vdd and Vdd*2 on first and second phases, respectively, of the second clock signal Lclk. The second clock signal, Lclk, is generally an inverted version of the first clock signal, Lclk, so that when the first phase of the first clock signal Lclk is LOW, the first phase of the second clock signal Lclk is HIGH, and vice versa.

In the preferred embodiment of the invention, when the first phase of the first clock signal Lclk is LOW, the first voltage output V11 is substantially equal to Vdd*2, and when the second phase of the first clock signal Lclk is HIGH, the first voltage output V11 is substantially equal to Vdd. Since the first phase of the second clock signal Lclk is HIGH when the first phase of the first clock signal Lclk is LOW, the second voltage output V12 is equal to Vdd during this time, and since the second phase of the second clock signal Lclk is LOW when the second phase of the first clock signal is HIGH, the second voltage output V12 is substantially equal to Vdd*2 during this time.

A 2nd stage voltage doubler circuit 300 receives the first and second voltage outputs, V11 and V12, respectively, from the 1st stage voltage doubler circuit 200, first and second high voltage clock signals, Hclk and Hclk, respectively, from an output stage circuit 600, and the first and second clock signals, Lclk and Lclk, respectively, and generates first and second 2nd voltage outputs, V21 and V22, respectively, in response thereof.

Cernea at 6:64 and Fig. 4:

FIG. 4 illustrates, as examples, timing diagrams for four phases of the first and second clock signals, Lclk and Lclk, first and second 1st voltage outputs, V11 and V12, first and second high voltage clock signals, Hclk and Hclk, and first and second kth voltage outputs, Vk1 and Vk2. As previously described, when the first clock signal Lclk is LOW (e.g., odd phases 1 and 3), the second clock signal Lclk is HIGH, the second high voltage clock signal Hclk is HIGH, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH, the first high voltage clock signal Hclk is LOW, and each of the second

voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW. Conversely, when the first clock signal Lclk is HIGH (e.g., even phases 2 and 4), the second clock signal Lclk is LOW, the second high voltage clock signal Hclk is LOW, each of the first voltage outputs (e.g., V11, Vk1 . . . Vn1) of each of the plurality of voltage doubler circuits (e.g., 200-500) is LOW, the first high voltage clock signal Hclk is HIGH, and each of the second voltage outputs (e.g., V12, Vk2 . . . Vn2) of each of the plurality of voltage doubler circuits (e.g., 200-500) is HIGH.

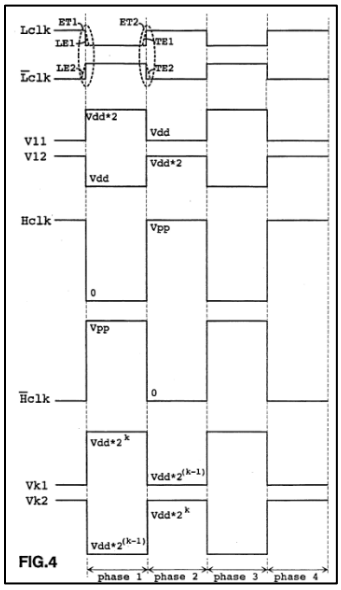


FIG.4

Anantha at Abstract:

In this work a programmable decimator design has been presented in 1.5 μm n-well CMOS process for integration with an existing modulator to form a sigma-delta analog-to-digital converter (ADC). The decimator is implemented using a second order Cascaded Integrator Comb (CIC) filter and can be programmed to work with two different oversampling ratios of 64 and 16. The input to the decimator is provided from a first order modulator. With oversampling ratios of 64 and 16, an output resolution of 10-bit and 7-bit, respectively are achieved for the ADC. The ADC can be operated with an oversampling clock frequency of up to 8 MHz and with an input signal bandwidth of up to 65 KHz. An in-built clock divider circuit has been designed which generates two output clocks whose frequencies are equal to the input clock frequency divided by the oversampling ratios 64 and 16. CHARGE PUMP CIRCUITS: The charge pump CMOS circuits are presented which are designed based on a new technique of internal clock voltage boosting. Four and six-stage charge pumps are implemented in 1.5 μm n-well CMOS process. The charge pump circuits can be operated in 1.2 V - 3 V power supply voltage range. Outputs of 12.5 V and 17.8 V are measured from four and six-stage charge pumps, respectively with a 3 V power supply. The charge pump circuits can also be used to generate clock voltages higher than the input clock voltage. In the present design, clock voltages of 8 V and 11 V have been generated from four-stage and six-stage charge pumps, respectively which are nearly 2.5 and 4 times the input clock voltage of 3 V. The technique of boosting the clock internally has been applied in implementation of a revised version of battery powered Bio-implantable Electrical Stimulation System (BESS) integrated circuit.

Anantha at p. 29:

The coder circuit of integrator 2 increases the resolution from 5-bit output of the first integrator stage to 9-bits by complementing the bit-5 and substituting its value in bits 5 through 9. Due to the use of two's complement scheme no data will be lost due to register overflow. The integrator circuit could cause register overflow but since the differentiator circuit follows the integrator, it performs the difference operation which eliminate the problem with register overflow [28]. The differentiator circuit is operated at a lower frequency compared to that of the integrator stage. This is made possible by using a clock divider circuit which generates a clock signal at reduced frequency. Since the CIC filter can be programmed, the clock divider circuit generates clocks of two frequencies for two oversampling ratios. One output gives a clock signal whose frequency is divided by the oversampling ratio 64 and the other output is a clock signal with frequency reduced by the ratio 16. The circuit for programmability is used to selects either one of the clock outputs based on the chosen oversampling ratios.

Anantha at p. 32:

The decimator operates at the same oversampling clock as that of the modulator but the differentiator circuit, which is a part of the decimator, also needs another clock signal for performing the decimation along with the low pass filtering operation. A clock divider circuit is used to provide the additional clock signal to the differentiator. It is used to generate a clock signal of frequency fs/K, where fs is the oversampling frequency. Since the designed decimator can be programmed to work with two different oversampling ratios of 64 and 16, the clock divider circuit should be able to generate two clock signals with frequencies fs/64 and fs/16.

Anantha at p. 34:

The clock divider circuit uses the oversampling clock signal as the input and generates two different clock outputs. An enable signal is used to select one out of the two outputs that should be applied to the differentiator. A clock divider circuit is a sequential circuit which uses flip flops and AND gates. The clock division is achieved through the edge triggering concept of a flip flop. An edge triggered T-flip flop, also called toggle flip flop changes its present output from the previous output state at every clock edge. A flip flop can be designed to work for a positive edge or a negative edge trigger operation. In the present design, a negative edge triggered T-flip flop is used. T-flip flops are usually made using a master-slave JK or master-slave D-flip flop. The present design uses a T-flip flop designed using a D-flip flop. Figure 4.5 shows a D-flip flop converted to a T-flip flop by connecting the Q' output back to the D input. In order to make a T-flip flop from a JK flip flop, J and K inputs have to be considered in the design which consumes more area compared with that of a D-flip flop design. A T-flip flop is a single input and single output device with clock being the input. The output is also a clock signal but the frequency is reduced by a factor of 2 from the input clock frequency. At every falling edge of the input clock, the output changes its state from the previous state. This way a reduction in the clock frequency by multiples of two can be achieved.

Anantha at p. 67:

The level shifted output is applied as the input to the Cascaded Integrator Comb (CIC) decimation

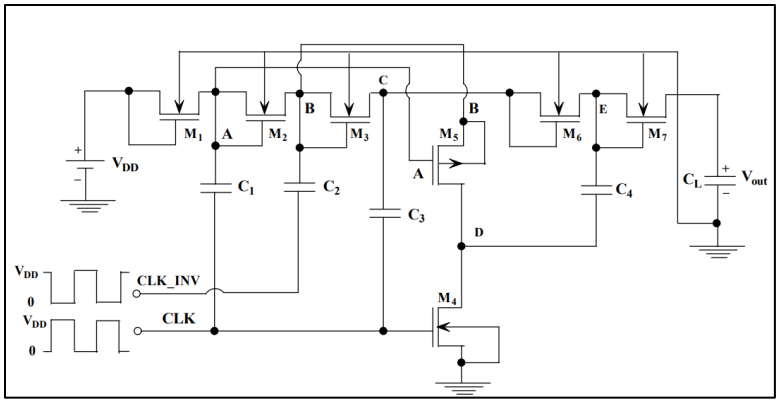
filter. Since the decimator is programmed to work for two different oversampling ratios the clock divider circuit generates two clock signals for frequency division by the ratio 64 and 16. Either one of the two clock frequency divider circuit outputs are taken based upon the enable signal which is set at the beginning of the ADC operation. The output of the clock divider circuit for frequency division by 64 is shown in Fig. 5.4. In the Fig. 5.4, label Lab1 11 is the actual input oversampling clock signal of frequency 256 KHz and the label Lab1 10 is the output showing the clock frequency division by the ratio K = 64.

Anantha at p. 69:

The time spacing between the two pulses shown in the Fig. 5.4 is equal to the KTs, where Ts is the time period of the oversampling clock signal. The time spacing between every two pulse is measured to be 250 µs. The oversampling clock samples the analog input sine wave such that at every clock period there exists a sample of the input i.e., for every clock period there is a sample of the input signal. The same clock frequency divider circuit can also be used to achieve frequency division by another oversampling ratio of 16. The output of the circuit showing the frequency division by the ratio 16 is shown in Fig. 5.5. In Fig. 5.5, label Lab1 11 is the actual input oversampling clock signal of frequency 64 KHz. Label Lab1 10 is used to represent the output of clock frequency division by 16. The time spacing between every two samples is KTs and in the present case the time spacing is 250 µs. Each pulse is separated from the preceding pulse by 16 samples i.e., by the oversampling ratio. In both the cases of clock frequency division outputs, the time spacing between every two pulses is same. The reason for this is that the analog input sine wave frequency is taken as the constant and the oversampling clock frequency is set as the variable. In the previous case, for K=64 the oversampling frequency was 256 KHz and in the present case of K=16 the frequency is 64 KHz. The oversampling frequency and the oversampling ratio are dropped by the same amount for the later case, hence the time spacing equation KTs remains constant for both the cases

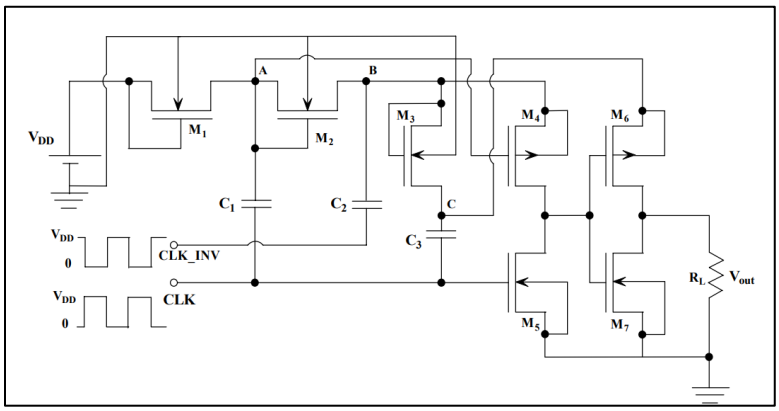
Anantha at p. 84 and Fig. 7.2:

Figure 7.2 shows a four-stage charge pump CMOS circuit design based on the idea of boosting the clock voltage internally. The design is a four-stage since it is based on the number of coupling capacitors used. Each coupling capacitor forms a crucial part of each pumping stage. Capacitors, C1, C2, C3 and C4 are used as coupling capacitors and the pumped charge is transferred to the load capacitor, CL using complementary clock signals. The charge is transferred from one pumping stage to the next in alternate clock cycles. The NMOS transistors M1 to M3, M6 and M7 are in the diode connected configurations and act as one-directional switches transferring the charge from their respective input terminal to the output terminal. The PMOS transistor, M5 and the NMOS transistor, M4 form an inverter circuit but their gates are not tied together. These two transistors forming an inverter do the work of boosting the clock voltage internally. By using a complementary clock scheme, the voltage on each pumping node gets boosted and is transferred in the forward direction through the one directional switches in alternate cycles as in the Dickson charge pump circuit in Fig. 7.1. In the Fig. 7.2, nodes, A, B and C have two voltage levels depending upon the low and high value of the clock. Initially all capacitors are assumed to be charged. The voltage on the capacitor C1 is VDD – VTN, the voltage on capacitor C2 is 2VDD – 2VTN and voltage on capacitor C3 is 3VDD – 3VTN. With this initial condition, voltages on the capacitor C4 and the load capacitor, CL can be obtained as follows under clocking conditions.



Anantha at p. 95 and Fig. 7.13:

The clock voltage boosting technique that has been used in the design of charge pump can be used specifically to design a circuit for generating higher clock voltages. The circuit is shown in Fig. 7.13 and its simulation results are presented in Fig. 7.14. In Fig. 7.13, the combination of the buffer circuit formed by transistors M4 to M7 and the pumping stage containing capacitor C3 forms the clock voltage boosting stage. By using the coupling capacitor C3, the voltage power supply to the inverter formed by the transistors M6 and M7 is boosted to the voltage stored on capacitor, C3 plus the clock amplitude VDD. The booster circuit which is shown in the Fig. 7.13 is slightly different from the one that has been used in the design of the fourstage and six-stage charge pumps. The operation of the circuit can be explained in similar lines to that of a four-stage charge pump case.



Nakai at Abstract:

A power supply circuit outputs different set potentials in response to control signals, wherein a voltage detecting circuit changes levels of a first reference potential and a second reference potential in response to inputs of control signals, and a clock generating circuit increases a frequency of the frequency divided clock signal when the levels of the first reference potential and the second reference potential are greatly changed in response to the inputs of the control signals.

Nakai at [0062]-[0063] and Fig. 1:

FIG. 1 shows the main configuration of a power supply circuit 100 according to a first embodiment

which is an aspect of the present invention. FIG. 2 shows an example of a boosting circuit applied to the power supply circuit of FIG. 1. FIG. 3 shows an example of a voltage detecting circuit applied to the power supply circuit of FIG. 1.

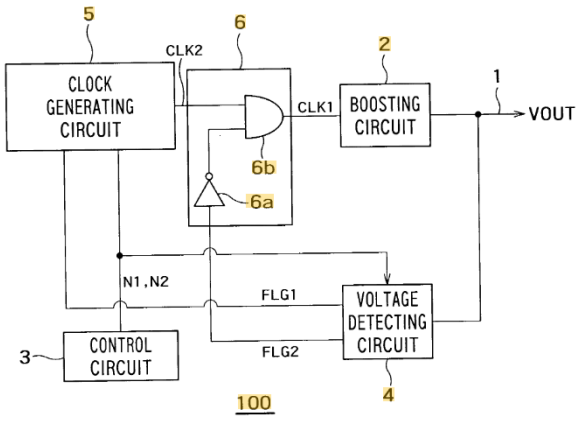


FIG. 1

As shown in FIG. 1, the power supply circuit 100 for outputting different set potentials in response to control signals N1 and N2 includes an output terminal 1 for outputting the set potentials, a boosting circuit 2 for boosting, in response to an input of a boosting clock signal CLK1, a voltage supplied from a power supply VCC and outputting the boosted voltage to the output terminal 1, and a control circuit 3 for outputting the control signals N1 and N2. Furthermore, as shown in FIG. 1, the power supply circuit 100 includes a voltage detecting circuit 4, a clock generating circuit 5, and a logic circuit 6.

Nakai at [0069]-[0070] and Fig. 3:

The voltage detecting circuit 4 detects the output potential VOUT outputted from the output terminal 1. After that, the voltage detecting circuit 4 compares a first reference potential VREF1 and the output potential VOUT and outputs a first flag signal FLG1 including information about the comparison result. Moreover, the voltage detecting circuit 4 compares a second reference potential VREF2 higher than the first reference potential VREF1 with the output potential VOUT and outputs a second flag signal FLG2 for instructing activation or deactivation of the boosting circuit.

As shown in FIG. 3, the voltage detecting circuit 4 includes a voltage dividing circuit 4 a, a first comparator amplifier circuit 4 b, and a second comparator and amplifier circuit 4 c.

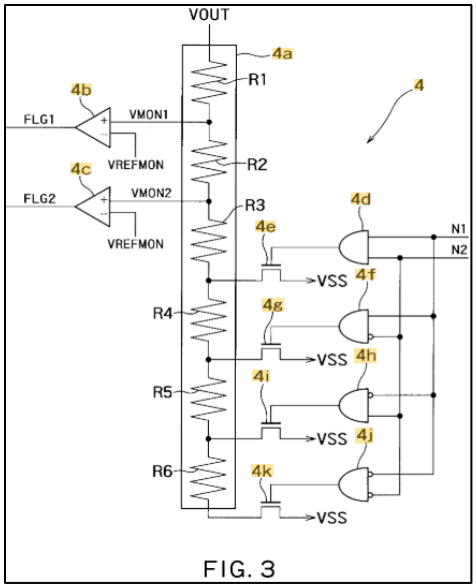


FIG. 3

Nakai at [0085]-[0089]:

The clock generating circuit 5 outputs a clock signal CLK2 with a reference clock when the first flag signal FLG1 is at, for example, “Low” level, that is, logic “0” (when the output potential VOUT is lower than the first reference potential VREF1).

Furthermore, when the first flag signal FLG1 is at, for example, “High” level, that is, logic “1” (when the output potential VOUT is higher than the first reference potential VREF1), the clock generating circuit 5 outputs the clock signal CLK2 with a divided clock obtained by dividing the reference clock.

As described above, when the output potential VOUT is lower than the first reference potential VREF1, the clock generating circuit 5 outputs the reference clock signal in response to the input of the first flag signal FLG1. When the output potential VOUT is higher than the first reference potential VREF1, the clock generating circuit 5 outputs the frequency divided clock signal obtained by dividing the reference clock signal. The division by the clock generating circuit 5 includes the division of the reference clock by an integer and the division of the reference clock by a fraction. Therefore, the clock generating circuit 5 can minutely set the frequency of the frequency divided clock signal.

When the voltage detecting circuit 4 greatly changes the levels of the first reference potential VREF1 and the second reference potential VREF2 thus in response to the inputs of the control signals N1 and N2, the clock generating circuit 5 increases the frequency of the frequency divided clock signal.

The logic circuit 6 includes an inverter 6 a which is fed with the second flag signal FLG2 and outputs the inverted second flag signal FLG2 and an AND circuit 6 b which is fed with the output signal of the inverter 6 a and the clock signal (the reference clock signal or the frequency divided clock signal) CLK2 outputted from the clock generating circuit 5, calculates these signals, and outputs the boosting clock signal CLK1.

Nakai at [0096] and Fig. 4:

As shown in FIG. 4, first, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "Low" level from time t0 to time t1. The clock generating circuit 5 outputs the clock signal CLK2 with the reference clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the reference clock and performs the boosting operation. In this way, at the start of the boosting operation, the boosting circuit 2 has constant boosting capability from the output potential VOUT of 0 V to the initial first reference potential VREF1 regardless of the logics of the control signals N1 and N2. Subsequently, at time t1, the voltage detecting circuit 4 outputs the first flag signal FLG1 at "High" level. The clock generating circuit 5 outputs the clock signal CLK2 with the divided clock in response to the first flag signal FLG1. Thus the boosting circuit 2 is activated by the boosting clock signal CLK1 with the divided clock and performs the boosting operation.

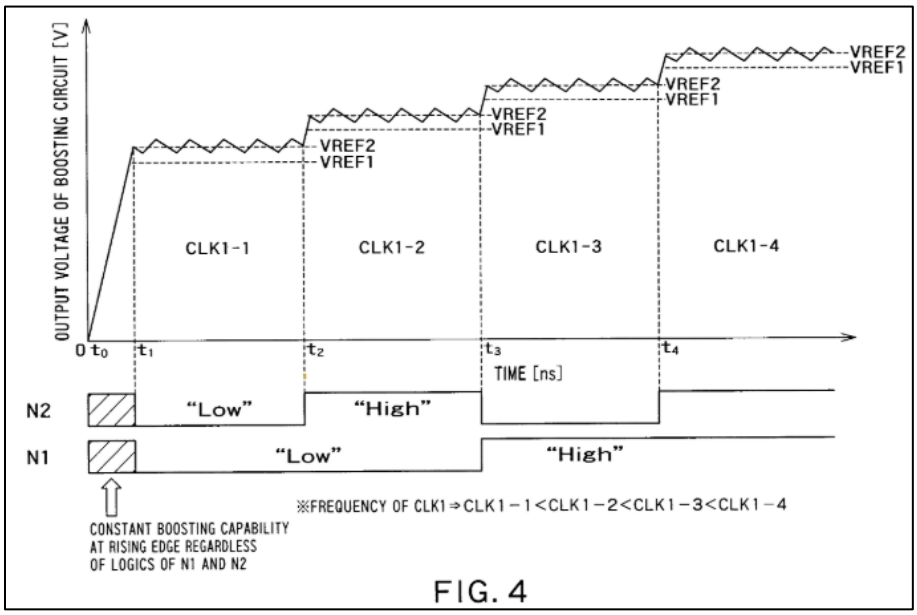


FIG. 4

Sato at [0051]:

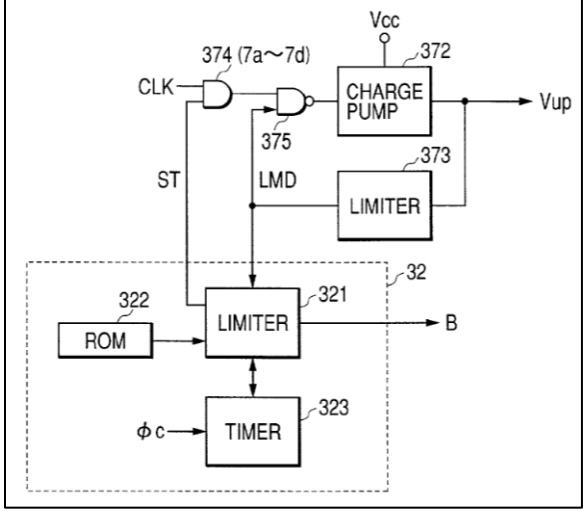
Other than the above circuits, the multi-value flash memory of the embodiment further has: a write/erase determining circuit 33 for determining whether a writing or erasing operation is finished or not on the basis of data of the sense and latch column SL, notifying the control circuit 32 of the result of determination, and finishing the writing or erasing operation; a clock generating circuit 34 having an oscillator and a frequency divider, for generating a plurality of timing clocks necessary for operations of internal circuits, such as operation clocks CK 1, CK 2, CLK 1, CLK 2, and PCLK 2 for a booster which will be described hereinlater and a clock phic for a timer and supplying the clocks to the circuits in the memory; a status and test circuit 35 having the functions of generating and outputting a ready/busy signal R/B in which the status of the memory is reflected and which indicates whether the memory can be accessed from the outside or not and testing an internal circuit; a main amplifier circuit 36 for amplifying a signal read from the memory array 10; a power circuit 37; an input/output control circuit 38 for capturing an address signal, a write data signal, and a command input from the outside, supplying the captured signal to a predetermined

circuit on the inside, and outputting a read data signal to the outside; an input/output buffer 39 for receiving a control signal input from the outside and supplying the signal to the control circuit 32 an other predetermined internal circuit; an address control circuit 40; and a redundancy circuit 41 for replacing a defective bit in the memory array with a spare memory row.

Sato at [0061] and Fig. 4:

In the example of FIG. 4, an AND gate 375 for receiving, as input signals, an output of an AND gate 374 for controlling the clock CLK to the charge pump 372 in response to a start signal ST from the CPU 321 and the output signal LMD of the limiter 373 is provided, and the supply of the clock signal CLK to the charge pump 372 is controlled by the limiter output LMD. When the boosted voltage output from the charge pump 372 becomes higher than the desired level, the operation of the charge pump 372 is stopped, so that excess power consumption can be reduced.

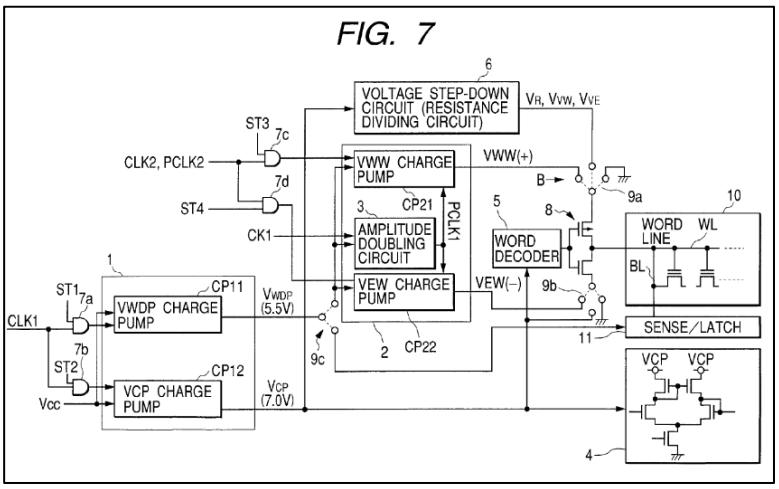
FIG. 4



Sato at [0068] and Fig. 7:

FIG. 7 shows a schematic configuration of the internal power source circuit of the flash memory having the booster according to the invention. In FIG. 7, reference numeral 1 denotes a first booster for performing a boost of a first stage on the basis of the source voltage Vcc of 1.8V to 3.3V from the outside, and 2 indicates a second booster for performing a boost of a second stage on the basis of a voltage VWDP boosted by the first booster 1. In the embodiment, the first booster 1 has two charge pumps CP 11 and CP 12 each of a capacitor parallel type. The second booster 2 has two charge pumps CP 21 and CP 22 each of a capacitor serial type.

FIG. 7



Sato at [0070]:

In the capacitor serial type charge pumps CP 21 and CP 22 in the second booster 2, the charge pump CP 21 generates a positive write voltage VWW such as +18V to be applied to the word line WL as a capacitive load in the memory array 10 which is a nonvolatile memory device, and the charge pump CP 22 generates a negative erase voltage VEW such as -16V to be applied to the word line WL. In the capacitor parallel type charge pumps CP 11 and CP 12 in the first booster 1, the voltage VWDP boosted by the charge pump CP 11 is supplied to the second booster 2 and the Y decoder and sense and latch circuit 11 for precharging a bit line BL in the memory array 10, and the voltage VCP boosted by the charge pump CP 12 is supplied to an internal logic gate circuit 4, a word decoder 5, a voltage step-down circuit 6 constructed by a resistance dividing circuit or the like, for generating a read voltage to be applied to the word line WL, and the like. The voltage step-down circuit 6 generates a read voltage VR in a normal read mode, a verify voltage VVW in a write mode, and an erasure verify voltage VVE in an erasure mode.

Sato at [0072]-[0073]:

Further, the second booster 2 is provided with an amplitude doubling circuit 3 for doubling the amplitude of the clock CK1. The amplitude doubling circuit 3 is constructed to generate a clock PCLK1 having an amplitude of 2VWDP on the basis of the boosted voltage VWDP generated by the booster 1.

The clocks CK 1, CLK1, and CLK2 are supplied from the clock generating circuit (of the block 34 in FIG. 1) in the chip. The supply of the clocks to the charge pumps CP11, PC12, CP21, and CP22 can be interrupted by gates 7 a, 7 b, 7 c, and 7 d controlled by start signals ST1, ST2, ST3, and ST4 from the control circuit (block 32 in FIG. 1). When the supply of a clock is interrupted, the corresponding charge pump stops the boosting operation

Sato at [0097]:

In the flash memory of the embodiment, the timer 323 is activated on start of the boosting operation of the charge pump CP21 in response to the start signal ST3 from the CPU 321. When the timer counts up the predetermined time before the detection signal LMD2 from the limiter circuit LM2

goes high, the CPU 321 switches the switch signal CS2 to the selector SEL2 to supply the boosted voltage VWW generated by the charge pump CP21 to the word driver 14 a. When the boosted voltage VWW is supplied to the word driver 14 a, the timer 323 starts counting a time of application of the write voltage. When the CPU 321 determines that the predetermined time has elapsed on the basis of the timer, the CPU 321 negates the start signals ST1 and ST3 to the charge pumps CP11 and CP21.

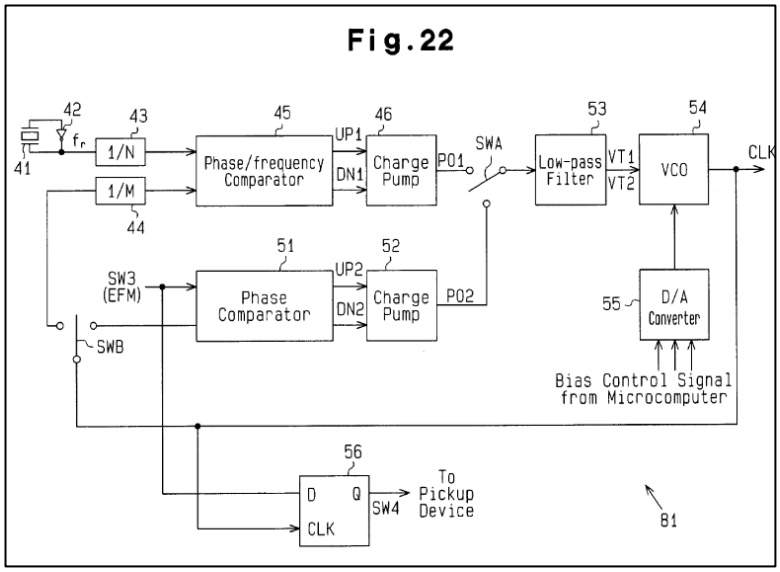
Tanishima at 17:60-18:27:

(b) As shown in FIG. 22, the reference clock generator circuit 25 and the data generation circuit 29 may be combined to form a signal generation circuit 81. The signal generation circuit 81 includes a crystal oscillator 41, an inverter circuit 42, first and second frequency dividers 43, 44, a phase/frequency comparator 45, a charge pump 46, a phase comparator 51, a charge pump 52, a low-pass filter 53, a VCO 54, a D/A converter 55, and an output circuit 56. Further, the signal generation circuit 81 includes switches SWA, SWB controlled by the microcomputer 14. Control of the switches may be performed by the recording control circuit 23.

The first switch SWA is provided to selectively supply one of an output signal PO1 from the first charge pump 46 and an output signal PO2 from the second charge pump 52 to the low-pass filter 53. The second switch SWB is provided to supply a reference clock signal CLK from the VCO 54 selectively to one of the second frequency divider 44 and the second comparator 51.

First, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a reference clock generator circuit. The signal generation circuit 81 sets the division ratios M, N of the respective first and second frequency dividers 43, 44, based on the wobble signal SG1 read from the disk D and the position information POS from the pickup device 11, and locks the frequency of the reference clock signal CLK to a frequency corresponding to the position of the pickup device 11. Then, the microcomputer 14 switches between the first and second switches SWA and SWB to cause the signal generation circuit 81 to operate as a data generator. The signal generation circuit 81 changes the phase of the reference clock signal CLK using the EFM-modulated signal SW3 as a reference signal, and supplies a recording signal SW4 to the pickup device 11 according to the modified clock signal CLK.

Tanishima at Fig. 22:

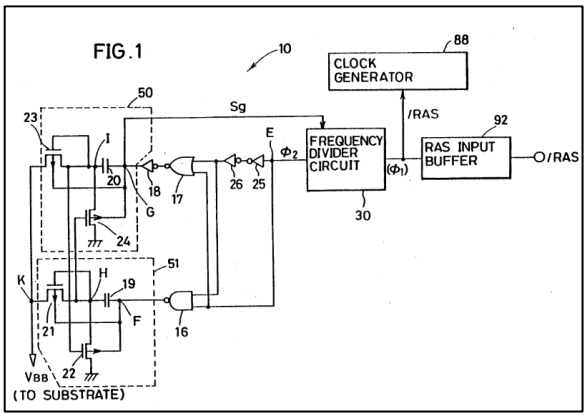


Nakayama at 1:9-14:

The invention relates generally to a substrate bias generating circuit and, more particularly, to a substrate bias generating circuit driven in response to an externally applied clock signal. The invention has particular applicability to dynamic random access memories (DRAMs).

Nakayama at 7:6-25 and Fig. 1:

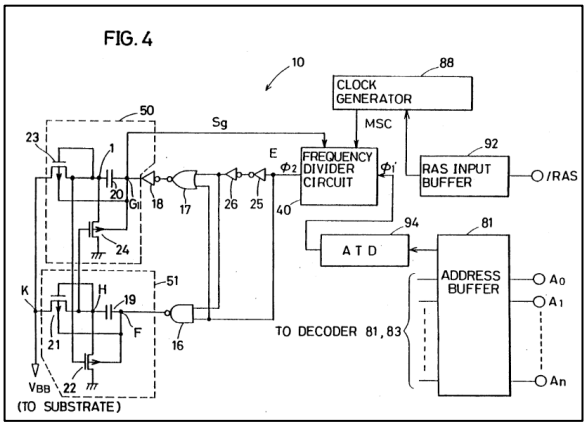
Referring to FIG. 1, a frequency division circuit 30 is provided at a preceding stage to a substrate bias generating circuit 10. A signal /RAS is applied to a RAS input buffer 92. RAS input buffer 92 outputs an internal signal /RAS in response to an externally applied signal /RAS, and applies it to a clock generator 88 and frequency division circuit 30. Frequency division circuit 30 receives the applied internal signal /RAS as an input clock signal φ1. In addition, frequency division circuit 30 is connected to receive a signal Sg defining one divided period which is output from a charge pump circuit 50. Frequency division circuit 30 divides input clock signal φ1 by a predetermined ratio of division and applies the divided output clock signal φ2 to substrate bias generating circuit 10. Substrate bias generating circuit 10 is driven by an applied clock signal φ2 and supplies a substrate bias voltage VBB to a substrate not shown. Operation of substrate bias generating circuit 10 is the same as that of the conventional circuit 93 shown in FIG. 9, and therefore the description is not repeated.



Nakayama at 8:6-26 and Fig. 4:

Frequency division circuit 30 shown in FIG. 1 receives an output clock signal φ1 from a RAS input buffer 92; however, it is pointed out that it is possible to supply an output signal from CAS input buffer 91 shown in FIG. 8 in place of RAS input buffer 92. Further, it is also pointed out that, in some cases, ATD pulse generated from an address transition detector (ATD) can be supplied in place of RAS input buffer 92.

FIG. 4 is a circuit diagram of a substrate bias generating circuit showing another embodiment of the invention. Referring to FIG. 4, compared to the circuit shown in FIG. 1, an improved frequency division circuit 40 is provided in place of frequency division circuit 30. Frequency division circuit 40 receives an ATD pulse generated from an ATD circuit 94 as an input clock signal φ1'. In addition, frequency division circuit 40 receives a static column mode signal /MSC generated from a clock generator 88. Therefore, frequency division circuit 40 divides input clock signal φ1' applied only in a static column mode in response to signal /MSC.



Nakayama at 9:13-29:

Additionally, the following advantage is also pointed out. As described above, charge pump circuits 50 and 51 are driven alternately in response to an applied clock signal, that is, divided clock signal φ2. As an operation speed of a DRAM increases, generally, frequencies of signal /RAS and ATD pulse increase, so that a frequency of clock signal φ2 is generally increased. Therefore, charge pump circuits 50 and 51 should be operated at a high speed. By newly providing

frequency division circuit 30 or 40, an operation speed needed for charge pump circuit 50 and 51 is decreased, and therefore efficiency of generation of substrate voltage VBB in these circuits 50 and 51 is improved. That is, charging/discharging of capacitors 19 and 20 provided in charge pump circuits 50 and 51 is carried out during a longer time period obtained by providing a frequency division circuit 30 or 40, so that it is possible to perform complete charge/discharge of capacitors 19 and 20.

Nakayama at 3:52-63 and Fig. 9:

FIG. 9 is a circuit diagram of substrate bias generating circuit 93 shown in FIG. 8. Referring to FIG. 9, the substrate bias generating circuit 93 comprises cascaded inverters 25 and 26 for shaping a waveform of an input clock signal φ4, a NAND gate 16 for outputting clock signals inverted from each other, a NOR gate 17, an inverter 18, and two charge pump circuits 50 and 51. Externally applied signal /RAS is received by RAS input buffer 92. The received input signal /RAS is applied to clock generator 88. Input signal /RAS is applied also to substrate bias generating circuit 93 as the above mentioned signal φ4.

Nakayama at 3:64-4:9 and Fig. 10:

FIG. 10 is a timing chart for describing operation of substrate bias generating circuit 93 shown in FIG. 9. Referring to FIGS. 9 and 10, the operation of substrate bias generating circuit 93 will be described below. Input clock signal φ4 is applied, so that a potential of node E changes as shown in FIG. 10. Therefore, potentials of an output node F of NAND gate 16 and an output node C of NOR gate 17 also change as shown in FIG. 10. Since an output signal of NOR gate 17 is inverted by inverter 18, an output node G of inverter 18 changes as shown in FIG. 10. Charge pump circuits 50 and 51 respectively receive clock signals which are obtained from input clock signal φ4 and inverted from each other.

Jiang at p. 4 and Fig. 3:

Embodiment

Specific embodiment according to this patent is described with reference to the accompanying drawings.

Fig. 3 is the circuit diagram according to the high-voltage generator of the semiconductor devices of the embodiment of the invention.

With reference to figure 3, high-voltage generator 100 comprises first high voltage pump unit 110, second high voltage pump unit 120 and clock generation unit 130.Can use a plurality of high voltage pump unit generating a plurality of different high voltages, but for present embodiment, describe the situation that high-voltage generator spare 100 wherein comprises two high voltage pump unit 110 and 120 as an example.

First high voltage pump unit 110 comprises first high voltage pump 111, comparer 112, pedestal generator 113, first impact damper 114 and resistor R 1 and R2.

Resistor R 1 and R2 are connected in series between the first high voltage Vpp1 and the ground

voltage Vss.The first high voltage Vpp1 is shared to generate dividing potential drop Va according to the resistance value of resistor R 1 and R2.

The reference voltage V ref that comparer 112 compares dividing potential drop Va and exports from pedestal generator 113.When dividing potential drop Va was lower than reference voltage V ref, comparer 112 was output as high level with impact damper enable signal en1.

First impact damper, 114 response buffer enable signal en1 and being activated, and output and the synchronous pump enable signal P_en1 of first clock signal clk 1 that exports from clock generation unit 130.

First high voltage pump, 111 response pump enable signal P_en1 and carry out pumping operation, and generate the first high voltage Vpp1.

Second high voltage pump unit 120 has like configurations and the operation as first high voltage pump unit 110, and will not be described in detail for simplicity.

Clock generation unit 130 comprises clock coder 131 and oscillator 132.Impact damper enable signal en1 and en2 that clock coder 131 coding generates from first high voltage pump unit 110 and second high voltage pump unit 120 respectively, and generate oscillator enable signal EN.Oscillator 132 responds oscillator enable signal EN and generates clock signal clk 1 and CLK2.

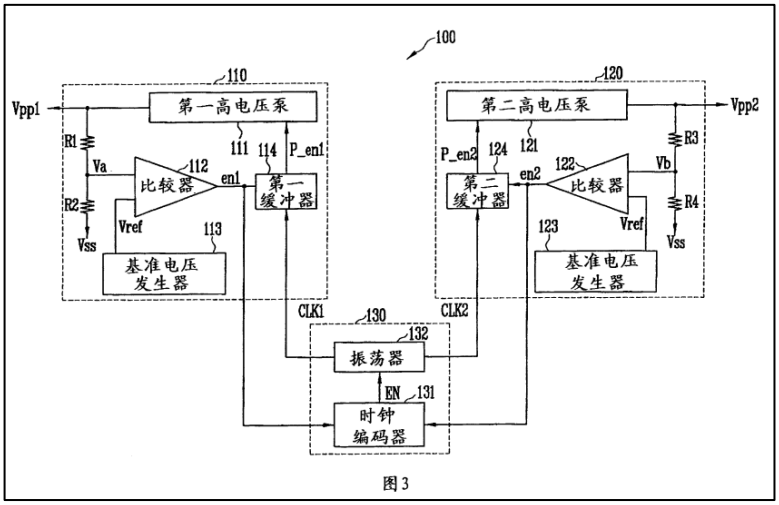


图3

Jiang at 8-9 and Figs. 4a-4b:

Fig. 4 a is the detailed circuit diagram of the clock coder 131 that shows among Fig. 3.

With reference to figure 4a, can use the OR door to realize clock coder 131.OR gate logic ground combined buffers enable signal en1 and en2, and output oscillator enable signal EN.

Fig. 4 b is the detailed circuit diagram of clock coder 131, and it is used in the high-voltage generator with 3 or more high voltage pump.

With reference to figure 4b, clock coder 131 comprises that a plurality of NOR door NOR1 are to NOR5, NAND door ND11 and ND12 and phase inverter IV11.Dual input NOR door NOR1 logically makes up a plurality of impact damper enable signal en1 respectively to en8 to NOR4, and exports 4 composite signals.Dual input NAND door ND11 and ND12 logically make up respectively from described 4 composite signals of NOR door NOR1 to NOR4, and export two composite signals.NOR door NOR5 logically makes up from described two composite signals of NAND door ND11 and ND12 output, and the output composite signal.The output signal of the anti-phase NOR door of phase inverter IV11 NOR5, and output oscillator enable signal EN.

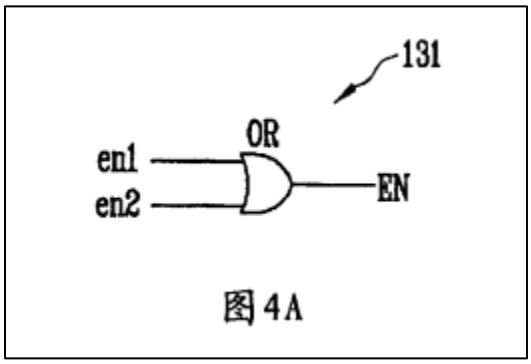


图 4A

Jiang at Fig. 6:

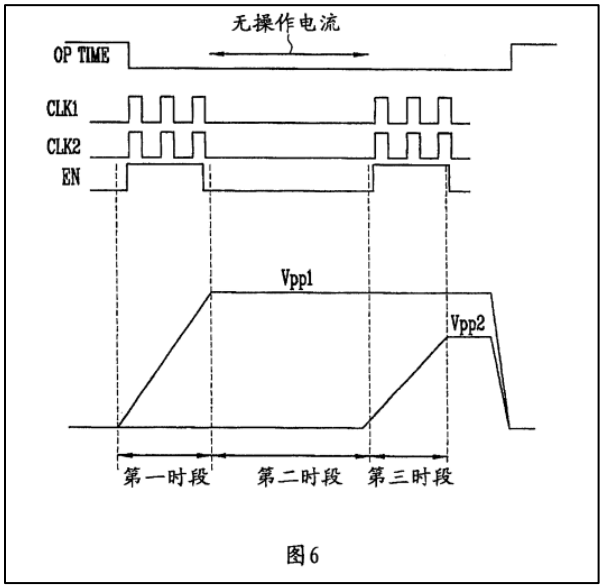
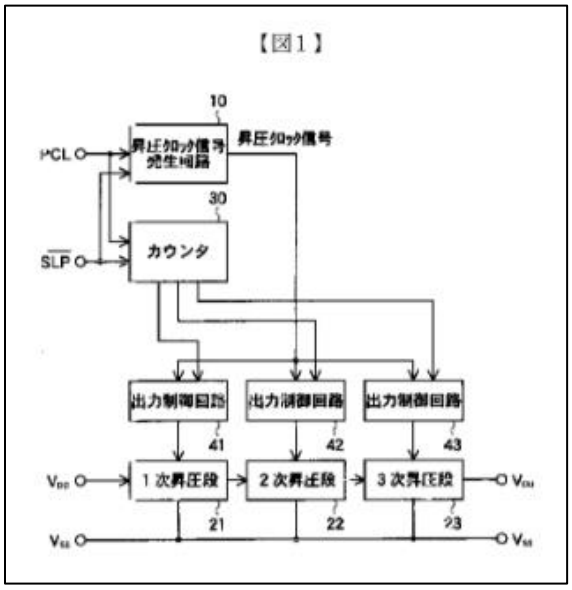


图6

Ito-633 at [0018] and Fig. 1:

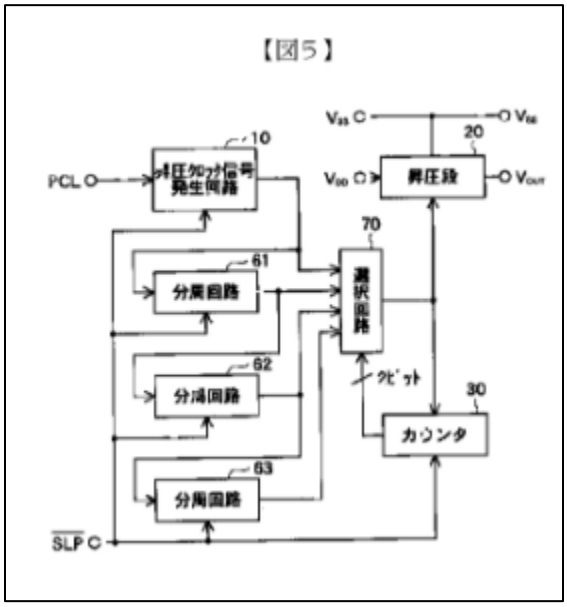
FIG. 1 is a block diagram showing the configuration of a voltage multiplier circuit according to the first embodiment of the invention. As shown in Fig. 1, this boost circuit consists of a boost clock signal generator circuit 10 that generates a clock signal used for boosting (hereinafter also referred to as "boost clock signal") based on the applied power clock signal PCL, The circuit includes a plurality of boost stages (in Fig. 1, the primary to tertiary boost stages 21-23 are shown) that sequentially boost the voltage between the first power supply potential VDD and the second

power supply potential VSS (in this embodiment, the ground potential) to output an output potential VOUT. Each of the boost stages has a configuration as shown, for example, in Figure 9.



Ito-633 at [0032] and Fig. 5:

Figure 5 is a block diagram showing the configuration of a boost circuit according to the third embodiment of the invention. As shown in Fig. 5, this boost circuit includes a boost clock signal generation circuit 10 that generates a boost clock signal based on the applied power clock signal PCL, a plurality of frequency divider circuits 61 to 63 that divide the boost clock signal and output a plurality of frequency divider clock signals respectively, and a selection circuit 70 that selects one clock signal from the boost clock signal and the plurality of frequency dividing clock signals.



Morton at Abstract:

A charge pump with controlled ramp rate (200) includes a charge pump (65), an RC differentiator circuit (258), and a trigger circuit (238). The charge pump (65) receives a clock signal and provides a high output voltage for programming and erasing an EEPROM. The RC differentiator circuit (258) provides a control voltage that is proportional to the ramp-up rate of the high output voltage. The trigger circuit (238) receives the control voltage, and provides a control signal to disable the charge pump (65) if the ramp-up rate exceeds a predetermined rate. When the ramp-up rate falls below the predetermined rate, the trigger circuit (238) provides a control signal to enable the charge pump (65). The trigger circuit (238) has hysteresis to regulate its switching point. Controlling the ramp-up rate of the output voltage reduces the peak tunneling current in the EEPROM cell to increase reliability.

Morton at 2:40-3:30 and Fig. 1:

FIG. 1 illustrates in partial logic diagram form and partial schematic diagram form charge pump with controlled ramp rate 200 in accordance with the present invention. Charge pump with controlled ramp rate 200 includes NAND logic gates 210 and 216, inverters 211,214, 218, and 236, charge pump 65, frequency divider circuit 220, trigger circuit 238, RC differentiator circuit 258, and clock control logic circuit 268. Frequency divider circuit 220 includes series-connected D-type flip-flops 222-229. Trigger circuit 238 includes P- channel transistors 240, 242, 244, and 248, N- channel transistors 246 and 250, and buffer/inverter circuit 251. Buffer/inverter circuit 251 includes inverters 252, 253, 254, and 256. RC differentiator circuit 258 includes MOS (metal-oxide semiconductor) capacitor 260 and switched capacitor 261. Switched capacitor 261 includes N-channel transistors 262 and 264, and capacitor 266. Clock control logic circuit 268 includes NAND logic gates 270 and 282, and inverters 272, 274, 276, 278, 280, 284, 286, 288, and 290.

NAND logic gate 210 has a first input terminal for receiving an external clock signal labeled "KEXT ", a second input terminal, a third input terminal, and an output terminal. Inverter 211 has an input terminal connected to the output terminal of NAND logic gate 210, and an output terminal. Charge pump 65 has a first input terminal connected to the output terminal of inverter 211, a second input terminal, and an output terminal for providing an output voltage labeled "VPP ". Inverter 214 has an input terminal connected to the second input terminal of NAND logic gate 210, and a output terminal connected to the second input terminal of charge pump 65. NAND logic gate 216 has a first input terminal connected to the first input terminal of NAND logic gate 210, a second input terminal for receiving a pump stop signal labeled "PMPSTOP ", and an output terminal. Inverter 218 has an input terminal connected to the output terminal of NAND logic gate 216, and an output terminal. D-type flip-flops 222-229 each have an input terminal labeled "D", clock input terminals labeled "K" and "K", and output terminals labeled "Q" and "Q". D-type flip-flop 222 has clock terminal K connected to the output terminal of inverter 218, and clock terminal K connected to the output terminal of NAND logic gate 216. Note that a bar over a signal name or terminal name indicates that the signal or terminal is a logical complement of a signal or terminal having the same name but lacking the bar. Each of flip-flops 222-229 have output terminal Q connected to input terminal D. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Flip-flop 222 has output terminal Q connected to clock terminal K of flip-flop 223, flip-flop 223 has output terminal Q connected to clock terminal K of flip-flop 224, and so on. Inverter 236 has an input terminal connected to the second input terminal of NAND logic gate 216, and an output terminal.

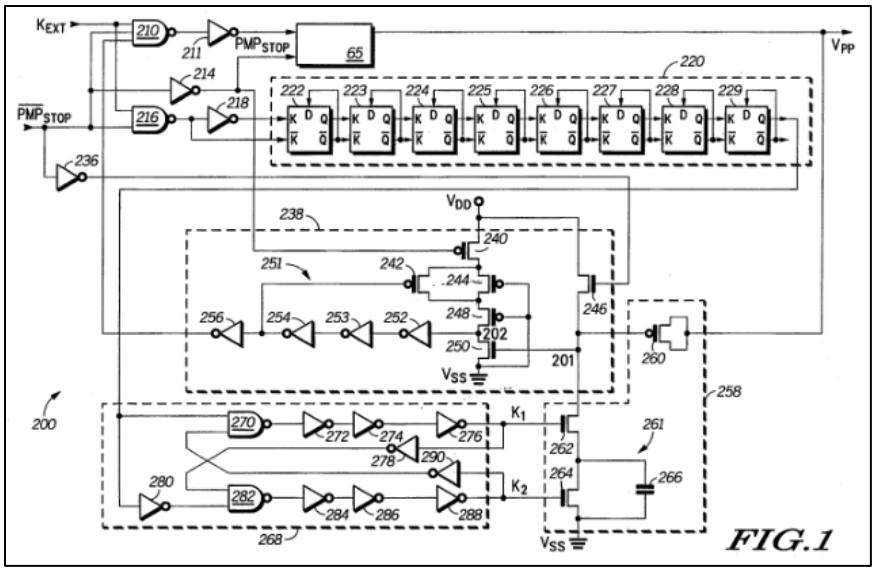


FIG. 1

Kumanoya at Abstract:

A semiconductor memory device receives an external control signal repeatedly generated independently of an access to the memory device. The memory device includes an internal voltage generator for generating a desired internal voltage in response to the control signal. The internal voltage generator includes a charge pump circuit responsive to the control signal. The internal voltage may provide a negative voltage such as a substrate bias voltage, or may be a positive voltage boosted over an operating power supply voltage and used as a boosted word line drive signal. This scheme eliminates an oscillator for generating a repeated clock signal to the charge pump circuit, leading to reduced current consumption and reduced chip area for the semiconductor memory device.

Kumanoya at 43:18-67 and Figs. 56-58:

FIG. 56 is a block diagram showing an example of a specific structure of internal voltage generating circuit shown in FIG. 55. Referring to FIG. 56, internal voltage generating circuit 800 includes a buffer circuit 810 for buffering the clock signal K, and a charge pump circuit 811 for generating internal voltage VIN by a charge pump operation in response to the clock signal buffered in the buffer circuit 810. Buffer circuit 810 is necessary when internal voltage generating circuit 800 directly receives the external clock signal K. Therefore, when clock buffer 254 is provided as shown in FIG. 11, buffer circuit 810 is not necessary. Although buffer circuit 810 and charge pump circuit 811 are provided separately in the structure of FIG. 56, a buffer circuit and a charge pump circuit may be regarded as one charge pump circuit.

FIG.56

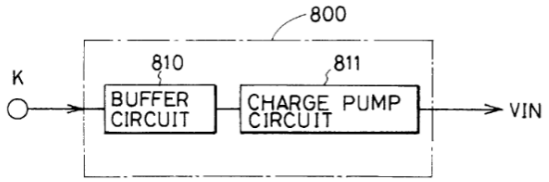


FIG.57

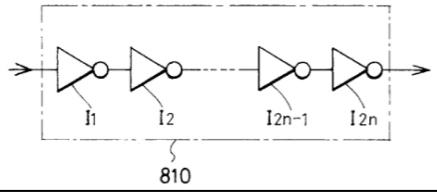


FIG. 57 shows an example of a specific structure of buffer circuit 810 shown in FIG. 56. Referring to FIG. 57, buffer circuit 810 includes an even number of serially (cascade) connected inverter circuits I1 to I2 n. Since clock signal K is applied constantly, the number of inverter circuits included in buffer circuit 810 may be odd-number. More specifically, charge pump circuit 811 supplies and removes positive charges in response to the rise and fall of the clock signal K. Therefore, when the clock signal K is repeatedly and constantly applied, even if the clock signal K is inverted and applied, the resulting operation is the same. Therefore, the buffer circuit 810 may have a function of inverting and outputting the applied signal.

FIG. 58 shows an example of a specific structure of charge pump circuit 811. Referring to FIG. 58, charge pump circuit 811 includes a capacitance CP10 receiving a buffered clock signal K′, an n channel MOS transistor TQ50 diode connected between a node 812 a and the ground potential, and a transistor TQ51 diode connected between nodes 812 a and 812 b. Transistor TQ50 has its gate and one conduction terminal connected to node 812 a. Transistor TQ51 has its gate and one conduction terminal connected to node 812 b. An internal voltage VIN such as a substrate bias potential Vbb is generated from node 812 b. The operation of charge pump circuit 811 will be briefly described.

Kumanoya at 44:42-58 and Fig. 60:

FIG. 60 shows another example of an internal data generating circuit. Internal data generating circuit 800 shown in FIG. 60 includes a dividing circuit 820 which frequency-divides an internal or external clock signal K by a prescribed ratio of division, and a charge pump circuit 811 responsive to a signal from the dividing circuit 820 for carrying out charge pump operation to generate an internal voltage VIN. Capability of supplying negative charges (or removal of positive charges) of the charge pump circuit is determined by capacitance value of the capacitors included therein and on frequency of applied clock signal. If the clock signal K has high frequency, charge pump circuit has higher capability of supplying negative charges, so that a predetermined bias voltage is faster provided stably at the level at which negative charge injection by the charge pump circuit 81 and positive charge injection due to memory operation are balanced with each other.

FIG. 60

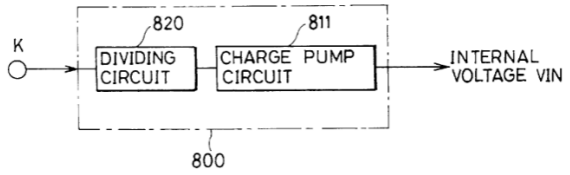
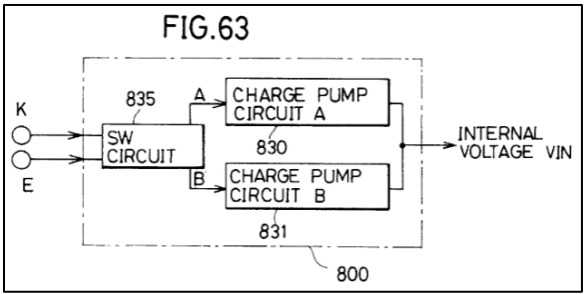


FIG. 61

Kumanoya at 45:33-57 and Fig. 63:

FIG. 63 is a block diagram showing an example of a specific structure of internal voltage generating circuit 800 shown in FIG. 62. Referring to FIG. 63, internal voltage generating circuit 800 includes a first charge pump circuit 830 and a second charge pump circuit 831 having different capabilities. The capabilities of the charge pump circuits 830 and 831 are adjusted by changing capacitance values of the capacitance of the charge pump. Internal voltage generating circuit 800 of FIG. 53 further includes a switch circuit 835 responsive to clock signal K and chip enable signal E for driving either charge pump circuit 830 or charge pump circuit 831. Switch circuit 835 selectively transmits clock signal K to charge pump circuit 830 or 831 in response to active/inactive state of chip select signal E.

FIG.63



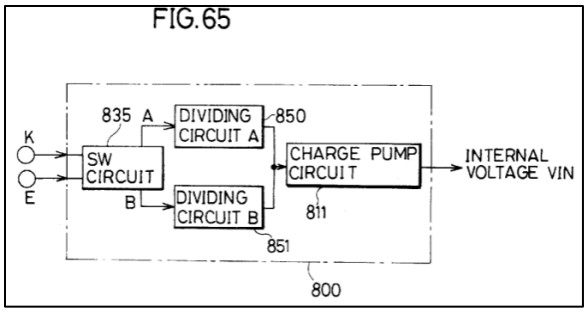
Switch circuit 835 may have a structure which transmits clock signal K to one of charge pump circuits 830 and 831 when chip select signal E is active and transmits the clock signal to the other one of charge pump circuits when chip select signal E is inactive for selectively driving the charge pump circuit 830 or 831.

Switch circuit 835 may have a structure which transmits clock signal K to both of charge pump circuits 830 and 831 when chip select signal E is active, and transmits clock signal K to one of the charge pump circuits when chip select signal E is inactive.

Kumanoya at 46:28-52 and Fig. 65:

FIG. 65 shows a further example of internal voltage generating circuit shown in FIG. 62. Referring to FIG. 65, internal voltage generating circuit 800 includes one charge pump circuit 811, dividing circuits 850 and 851 having different division ratio, and switch circuit 835 responsive to a chip select signal E for selectively transmitting clock signal K to the dividing circuits 850 and 851. Current supplying capability of charge pump circuit is changed dependent on the frequency of an

oscillating signal applied thereto. Therefore, by changing the frequency of an oscillating signal for the charge pump operation dependent on the selected/non-selected state of the semiconductor memory device, driving capability of the internal voltage generating circuit 800 can be adjusted. The structure shown in FIG. 61 may be used as the dividing circuit 850 and 851, and oscillating frequency thereof can be adjusted by changing the number of 1 bit binary counters.



Switch circuit 835 selectively transmits clock signal K to dividing circuit 850 or 851 in response to a chip select signal E. A structure shown in FIG. 64 may be used for switch circuit 835. In the structure shown in FIG. 65 also, the driving capability of internal voltage generating circuit 800 can be adjusted dependent on selected/non selected state of the semiconductor memory device, and the current consumption can be reduced.

Hsiao at Abstract:

An apparatus for generating a spread spectrum clock with constant spread ratio includes a resistance-capacitance oscillator which is used for generating a first clock signal. In addition, the present invention further includes a spread spectrum charge pump circuit, a loop filter, and a voltage controlled oscillator (VCO). The spread spectrum charge pump circuit generates a spread spectrum current according to the first clock signal for changing/discharging the loop filter, so as to make the loop filter generate a control voltage. The VCO generates a control current and a spread spectrum clock signal according to the control voltage. The VCO feeds the control current back to the spread spectrum charge pump circuit to generate the spread spectrum current.

Hsiao at [0029] and Fig. 3A:

FIG. 3A is a block view of the circuit of a PLL with a constant spread ratio fixing circuit according to a preferred embodiment of the invention. Referring to FIG. 3A, the phase comparator 301 receives a reference clock signal CLK0 and a feedback clock signal CLK3, and its output is coupled to a charge pump circuit 303. The charge pump circuit 303 transmits charging current in different flow directions into the loop filter 305 according to the output of the phase comparator 301. The loop filter 305 generates a control voltage signal Vctrl to the VCO 310 according to the flow direction of the charging current sent by the charge pump circuit 303, so that the VCO 310 generates a spread spectrum clock signal CLK2. The frequency divider 307 generates a feedback clock signal CLK3 to the phase comparator 301 after dividing the frequency of the spread spectrum clock signal CLK2.

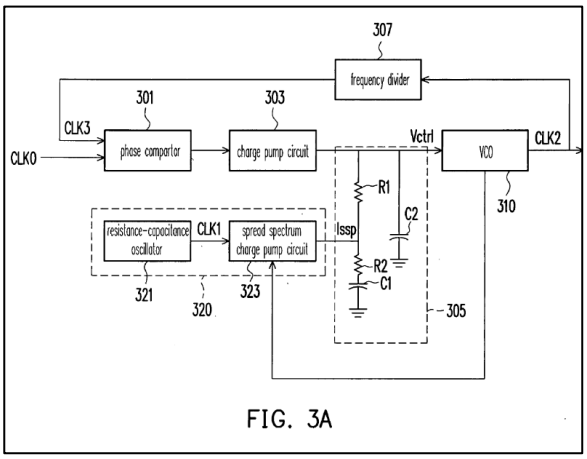


FIG. 3A

Hsiao at [0031]:

The spread ratio fixing circuit 320 mainly comprises a clock generating apparatus 321 and a spread spectrum charge pump circuit 323. The clock generating apparatus 321 is accomplished by a resistance-capacitance oscillator. The resistance-capacitance oscillator 321 provides a first clock signal CLK1 with constant frequency to the spread spectrum charge pump circuit 323. And then the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the first clock signal CLK1, and thereby a triangular wave signal with constant frequency can be loaded on the control voltage signal Vctrl output by the loop filter 305.

Hsiao at [0034]:

The circuit as shown in FIG. 3B can also be applicable to the charge pump circuit 303 of FIG. 3A. The on/off of two switches in the charge pump circuit 303 is determined based on the comparison result of the reference clock signal CLK0 and the feedback clock signal CLK3 compared by the phase comparator 301. When the two switches are switched in the charge pump circuit 303, the charge pump circuit 303 charges/discharges the loop filter 305 for enabling the loop filter to generate the control voltage signal Vctrl.

Hsiao at [0044]-[0046] and Fig. 4:

FIG. 4 is a flow chart of the steps for generating the spread spectrum clock signal according to a preferred embodiment of the invention. The method can be applied to the apparatus for generating the spread spectrum clock signal as shown in FIG. 3A. Referring to FIGS. 3A and 4, first, as shown in Step S401, a reference clock signal CLK0 is generated, and then the phase comparator 301 receives the reference clock signal CLK0 to compare it with the feedback clock signal CLK3. Then, the phase comparator 301 controls the charge pump circuit 303 to charge/discharge the loop filter 305 according to the comparison result, such that the control voltage Vctrl is generated, as shown in Step S403.

When the above steps are implemented, the resistance-capacitance oscillator 321 generates a first clock signal CLK1 with constant frequency, as shown in Step S405. Then, the spread spectrum charge pump circuit 323 charges/discharges the loop filter 305 according to the frequency of the first clock signal CLK1 (Step S407), such that a triangular wave signal is generated to modulate

the control voltage Vctrl, as shown in Step S409.

Next, the voltage/current conversion circuit 312 in the VCO 310 (as shown in FIG. 3C) performs Step S411, i.e., converts the control voltage Vctrl into the current signal Ictrl. Then, the current controlled oscillator 314 (as shown in FIG. 3C) generates the spread spectrum clock signal CLK2 according to the current signal Ictrl, as shown in Step S413. At this time, the VCO 310 can also feed the current signal Ictrl back to the spread spectrum charge pump circuit 323, as shown in Step S415, so as to control the amplitude of the aforementioned triangular wave signal.

Senda at Abstract:

A voltage boosting circuit performs variable frequency control that gradually increases frequencies of clock signals from a low frequency to a high frequency during a boosting operation period for which a low output voltage of a DC-DC converter when the power is turned on is boosted up to a predetermined voltage. Thus, the frequencies of clock signals may be set according to the boosting operation of the DC-DC converter. Consequently, the operation of the DC-DC converter may be stabilized until the stable operation period is performed after the DC-DC converter starts to operate.

Senda at [0085]-[0090] and Fig. 10:

FIG. 10 is a block diagram showing the internal construction of the DC-DC converter 31 of FIG, 9. As illustrated in FIG. 10, the DC-DC converter 31 includes a timing controller 31 a and a charge pump circuit 31 b.

The timing controller 31 a generates clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 by using clock signals CLK input from the ring oscillator 21, in which the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3 are input to two charge pump units in the charge pump circuit 31 b, respectively.

Fig. 10

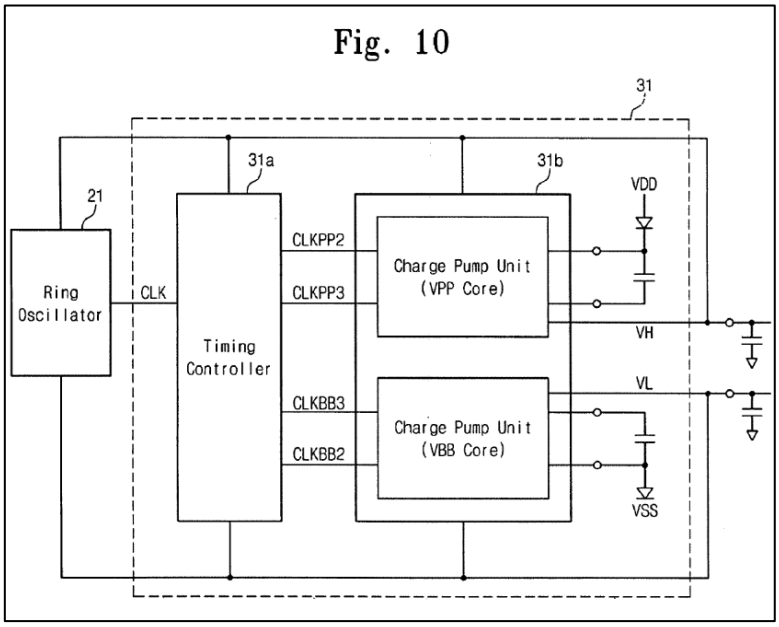


FIG. 11 is a circuit diagram showing the construction of the timing controller 31 a. As illustrated in FIG. 11, in the timing controller 31 a, an inverter D is connected to the input terminal of the timing controller 31 a and receives the clock signal CLK from the ring oscillator 21, and a timing adjustment circuit is connected to the output terminal of the input inverter D, in which the timing adjustment circuit includes a plurality of inverters and NOR circuits. Further, four output inverters are connected to the output terminals of the timing adjustment circuit, in which the four output inverters output the clock signals CLKPP2, CLKPP3, CLKBB2 and CLKBB3.

After the timing adjustment circuit of the timing controller 31 a receives the clock signals CLK from the ring oscillator 21 the timing adjustment circuit generates first clock signals CLKPP2 and CLKPP3 having an adjusted timing for the boosting charge pump unit (VPP Core), and second clock signals CLKBB2 and CLKBB3 having an adjusted timing for the dropping charge pump unit (VBB Core).

The charge pump circuit 31 b includes the boosting and dropping charge pump units. In FIG. 10, the charge pump unit VPP core is a boosting charge pump and the charge pump unit VBB core is a dropping charge pump.

The boosting charge pump unit VPP core performs a boosting operation of input voltage based on the frequencies of the clock signals CLKPP2 and CLKPP3 input from the. The dropping charge pump unit VBB core performs a dropping operation of input voltage based on the frequencies of the clock signals CLKBB2 and CLKBB3 input from the timing controller 31 a.

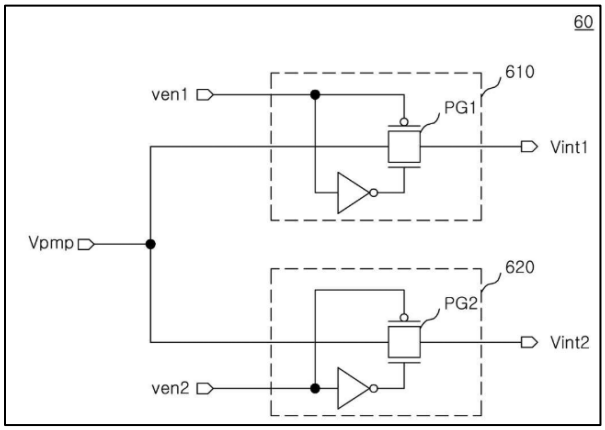
Kim at Abstract:

An internal voltage generation device of a semiconductor integrated circuit of the present invention includes a plurality of voltage sensing means for detecting whether the internal voltage exceeds a reference level and outputting a respective voltage enable signal, and a plurality of voltage enable signals in combination Signal combination means for outputting an enable signal, pulse generating means for generating a pump enable signal in response to the input of the pulse enable signal, and performing a voltage pumping operation in response to the input of the pump enable signal to generate a pumping voltage. And a voltage output means for outputting the generated voltage pump and the pumping voltage as the internal voltage corresponding to the input of each of the voltage enable signals.

Kim at [0020] and Fig. 4:

As described above, the internal voltage generation device of the semiconductor integrated circuit of the present invention comprises a first voltage detection means (10) for detecting whether a first internal voltage (Vint1) exceeds a first reference level and outputting a first voltage enable signal (ven1), a second voltage detection means (20) for detecting whether a second internal voltage (Vint2) exceeds a second reference level and outputting a second voltage enable signal (ven2), a signal combination means (30) for combining the first and second voltage enable signals (ven1, ven2) and outputting a pulse enable signal (plen), a pulse generation means (40) for generating a pump enable signal (pmen) in response to an input of the pulse enable signal (plen), a voltage pump (50) for performing a voltage pumping operation in response to an input of the pump enable signal (pmen) and generating a pumping voltage (Vpmp), and the first and second It is composed

of a voltage output means (60) that outputs the pumping voltage (Vpmp) as the first and second internal voltages (Vint1, Vint2) in response to the input of a voltage enable signal (ven1, ven2).



Saito at Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which can obtain a high potential necessary for writing data to a memory using a small circuit area. <P>SOLUTION: The semiconductor device comprises an antenna portion receiving external radio waves, a rectifier circuit portion rectifying output of the antenna portion and outputting DC voltage VDD0, a regulator circuit receiving output of the rectifier circuit portion and outputting VDD that is a constant voltage, and a booster circuit boosting the DC voltage VDD0. By using as input voltage of the booster circuit not the conventionally used output VDD of the regulator circuit 104, but rather the output VDD0 of the rectifier circuit portion 103, which is a higher potential than the VDD, the high potential necessary for writing data to a memory can be obtained with a small circuit area.

Saito at [0011]:

The present invention was made in view of this point, and its task is to generate the voltage necessary for memory write operations without increasing the circuit area as well as reducing power consumption.

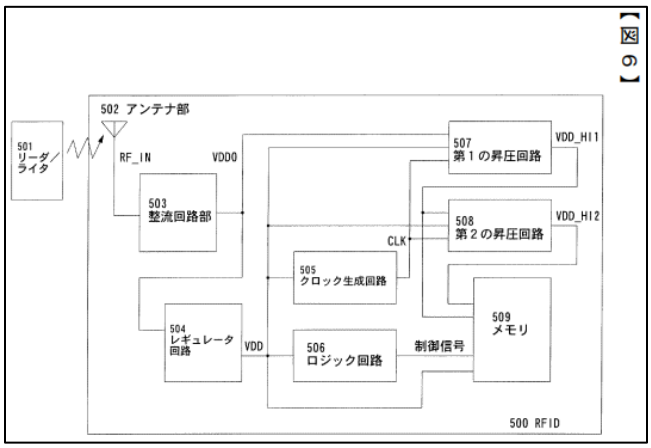
Saito at [0032]:

The clock generation circuit 105 receives the output VDD from the regulator circuit 104 to generate the clock signal CLK, and can use any known clock generator. For example, it may be generated by dividing radio waves taken from the antenna section 102, or by using an oscillation circuit such as a ring oscillator or VCO.

Saito at [0072] and Fig. 6:

FIG. 6 is a block diagram to illustrate the RFID to which the invention is applied. In Figure 6, RFID 500 comprises ... a first boost circuit 507 that receives the output of rectifier circuit section 503 and the output of clock generation circuit 505 and outputs a boosted voltage, and a second boost circuit 508 that receives the output of first boost circuit 507 and the output of clock

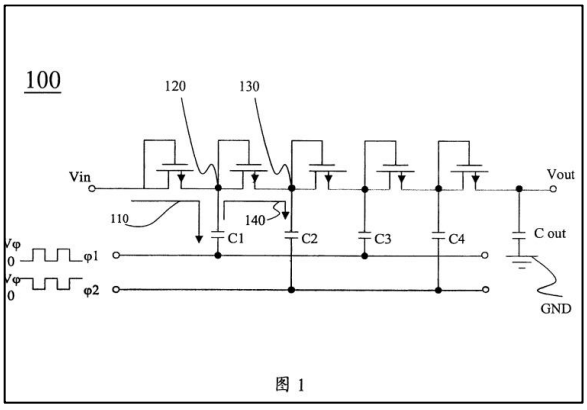
generation circuit 505 and outputs a further boosted voltage to memory 509



Wu at Abstract:

A boost charge boost circuit comprises a plurality of diode equivalent networks, at least one boost capacitor network and at least one reverse current cutoff circuit. The diode equivalent networks are electrically connected in series, with a node between every two diode equivalent networks, and each node corresponds to a boost stage, wherein the low voltage side of the diode equivalent network of the lowest boost stage is an input end of the boost charge boost circuit, and the input end receives an input voltage signal. One end point of each boost capacitor network is electrically connected to a node, and the other end point of each boost capacitor network is electrically connected to a clock signal. Each reverse current cutoff circuit is electrically connected to the diode equivalent network, wherein the reverse current cutoff circuit has at least two conduction paths, and the conduction paths are alternately turned on according to the switching of the clock signal in each boost stage.

Wu at Fig. 1:



Lee at Abstract:

The present invention prevents the loss of the threshold voltage in the switch MOS transistors of the pumping stages, thereby preventing power consumption and current transfer efficiency from deteriorating, and using a low voltage as a supply power supply (VDD). The present invention

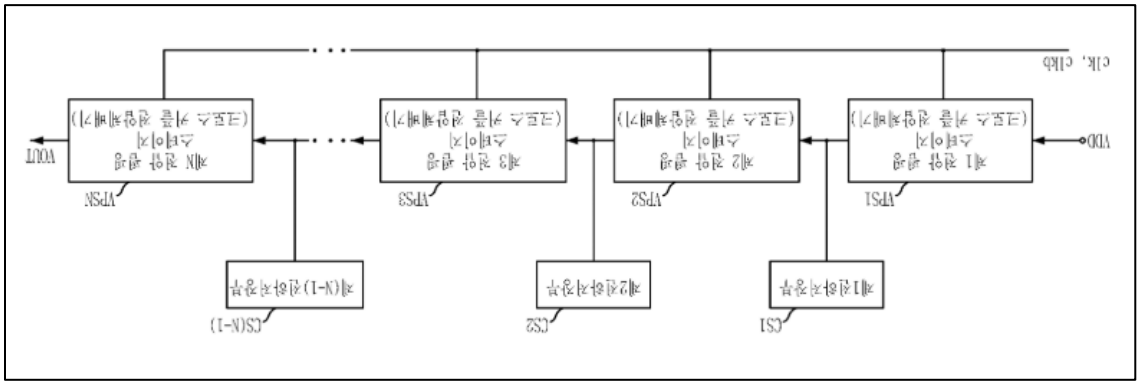
relates to a multistage voltage pumping circuit that stably generates an arbitrary 'N x VDD', wherein the multistage voltage pumping circuit of the present invention is a cross-coupled voltage driven by the first and second clocks having a phase complementary to each other. A plurality of voltage pumping stages configured to multiplier to boost a voltage applied to an input stage without losing a threshold voltage, the output stage of the voltage pumping stage being connected to an input terminal of a next voltage pumping stage; And a plurality of charge storage means connected to an output end of each of the voltage pumping stages except for the voltage pumping stage of the final stage to store charge.

Lee at [0019]:

In order to achieve the above object, the present invention provides a multi-stage voltage pumping circuit including a cross-coupled voltage multiplier driven by the first and second clocks having complementary phases, a plurality of voltage pumping stages for boosting a voltage applied to an input terminal without threshold voltage loss, wherein an output terminal of the voltage pumping stage is connected to an input terminal of a voltage pumping stage of the next stage; and a plurality of charge storage means connected to the output terminals of each of the voltage pumping stages except for the voltage pumping stage of the final stage for storing charge.

Lee at [0028] and Fig. 4:

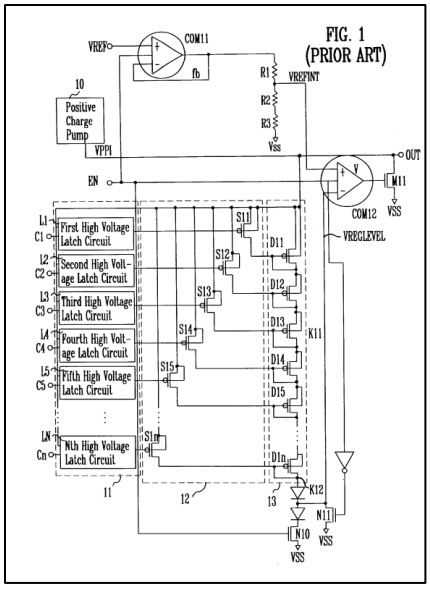
Clocks clk and clkb are non-overlapping, mutually complementary phase signals, and a typical non-overlapping clock generator is illustrated in Fig. 4.



Kim at Abstract:

The present invention describes a multi-step pulse generating circuit for a flash memory comprising a reference voltage generating circuit to generate uniform voltage: a first comparator to compare the output voltage of the first comparator with the feedback value; a voltage drop means to get desirable voltage by dropping the output voltage of the first comparator; a positive charge pump circuit to generate desirable high voltage; a diode chain to drop the output voltage of the positive charge pump circuit; a second comparator to compare the output voltage of the voltage drop means with the output voltage of the diode chain; and a switching means to control the output voltage of the positive charge pump circuit depending on the output of the second comparator.

Kim at Fig. 1:



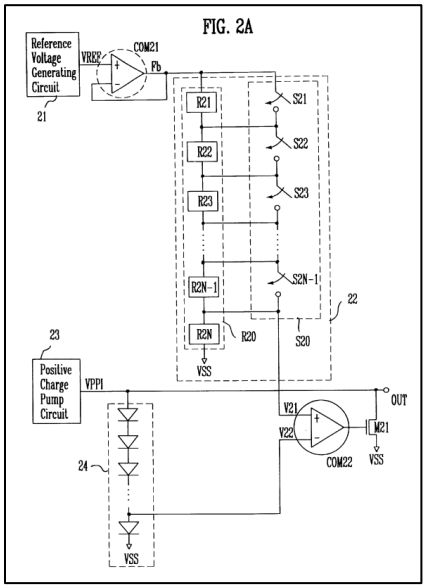
Kim at 2:20-67:

As shown in FIG. 2A a multi-step pulse generating circuit for a flash memory in accordance with a first embodiment of the present invention comprises: a reference voltage generating circuit **21** to generate uniform voltage; a first comparator COM**21** to compare the output voltage VREF of said reference voltage generating circuit **21** with the feedback value: a voltage drop means **22** to get desirable voltage by dropping the output voltage of said first comparator COM**21**; a positive charge pump circuit **23** to generate desirable high voltage; a diode chain **24** to drop the output voltage VPPI of the positive charge pump circuit; a second comparator COM**22** to compare the output voltage of the voltage drop means **22** with the output voltage of the diode chain **24**; and a switching means M**21** to control the output voltage VPPI of the positive charge pump circuit **23** depending on the output of the second comparator COM**22**.

A first comparator COM**21** compares the reference voltage VREF generated from a reference voltage generating circuit **21** with the feedback signal Fb. To operate the first comparator COM**21**, two input signals VREF and Fb of the first comparator COM**21** should keep fixed potential of VREF=Fb. The output signal of the first comparator COM**21** is entered to the second comparator COM**22** after being entered to the voltage drop means **22** and dropped as much as fixed potential. The voltage drop means **22** comprises multiple resisters (R**20**: R**21** to R2N) serially connected between the output terminal of the first comparator COM**21** and the ground terminal VSS, and multiple switches (S**20**: S**21** to S 2N−1) connected between both ends of each resistance. The voltage (VPPI) of high potential pumped and outputted from the positive charge pump circuit **23** is entered to the second comparator COM**22** after voltage drop by the diode chain **24**. The second comparator COM**22** compares the output of the voltage drop means with the output of the diode chain **24**. Then if the output of the diode chain **24** is larger than that of the voltage drop means **22**, the second comparator COM**22** outputs the potential of high level and turns on the switching means M**21**. Accordingly, current pass is formed from the positive charge pump circuit **23** to the ground terminal VSS, and thus the pumped potential does not rise any more. On the other hand, if the output of the diode chain **24** is smaller than that of the voltage drop means **22**, the second comparator COM**22** outputs potential of low level and turns off the

switching means M**21**. Therefore, current pass does not occur from the positive charge pump circuit to the ground terminal VSS and the output voltage of the positive charge pump circuit rises again.

Kim at Fig. 2A:



Crippa at Abstract:

A multistage circuit for regulating the charge voltage or the discharge current of a capacitance of an integrated device at a certain charge-pump generated boosted voltage is implemented without integrating high voltage transistor structures having a type of conductivity corresponding to the same sign of the boosted voltage (high-side transistors). The multistage circuit current includes at least a first stage, and an output stage in cascade to the first stage and coupled to the capacitance. The first stage is supplied at an unboosted power supply voltage of the integrated device, and the output stage is supplied at an unregulated charge-pump generated boosted voltage. The first stage includes a transistor having a type of conductivity corresponding to an opposite sign of the boosted voltage and of the power supply voltage. The drain of the output stage transistor is coupled to the boosted voltage either through a resistive pull-up or a voltage limiter.

Crippa at [0017]:

Basically, the multistage circuit for regulating the charge voltage or the discharge current of a capacitance in an integrated device, comprising at least a first stage and an output stage in cascade to the first stage and coupled to the capacitance, has the first stage supplied at an unboosted power supply voltage of the integrated device. The output stage is supplied at an unregulated charge-pump generated boosted voltage and is composed of a transistor of a type of conductivity opposite for the sign of the boosted voltage and of the power supply voltage.

Crippa at [0026]-[0027] and Fig. 2:

A first example embodiment of the invention, intended to provide a viable alternative to the known

voltage regulator of FIG. 1 without requiring the formation of any high voltage CMOS structure, is depicted in FIG. 2. As shown, the first stage MP1, MP2, MN1, MN2, MNT1 is a common differential stage FIRST STAGE (LV) that is powered at a normal (unboosted) power supply voltage VDD. The output stage SECOND STAGE (HV) is supplied at the unregulated charge-pump generated boosted voltage VPUMP.

By powering the first stage FIRST STAGE (LV) at VDD, the PMOS transistors of the normal low voltage (LV) structure MP1 and MP2 may be used for the load current mirror of the two branches of the differential stage. The output stage SECOND STAGE (HV) is implemented by using a HV NMOS transistor MNOUT with a resistive pull-up RPULL-UP connected to the boosted voltage node VPUMP. The boosted voltage node VPUMP is the output node of a charge-pump voltage multiplier (not shown) that generates the required boosted voltage VPUMP.

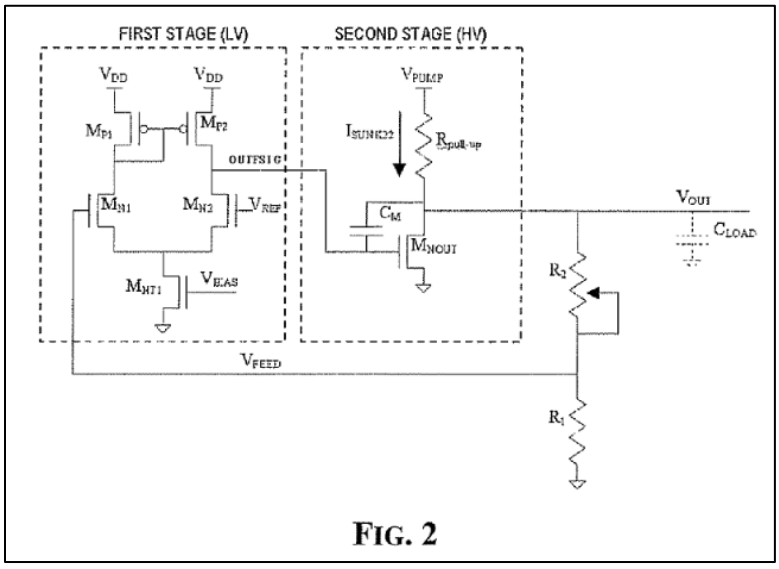


FIG. 2

Byeon at Abstract:

A semiconductor memory device comprises a first pump clock generator configured to generate a first pump clock signal based on a first power supply voltage. The device also comprises a first charge pump configured to generate a first pump output voltage in response to the first pump clock signal. The device also comprises a second pump clock generator configured to generate a second pump clock signal based on the first pump output voltage. The device also comprises a second charge pump configured to generate a second pump output voltage in response to the second pump clock signal. The device also comprises a third pump clock generator configured to generate a third pump clock signal based on the first power supply voltage. The device also comprises a third charge pump configured to generate a third pump output voltage in response to the third pump clock signal.

Byeon at [0026]. [0027], [0029] and Figs. 1A-1B:

FIGS. 1A and 1B are block diagrams of a semiconductor device 10 according to an exemplary disclosed embodiment. Referring to FIGS. 1A and 1B, the semiconductor device 10 includes a first voltage generation unit 20, a second voltage generation unit 30, a third voltage generation unit

40, and a row decoder circuit (i.e., an X-decoder) 50.

The first voltage generation unit 20 generates a first pump output voltage Vswitch based on a first voltage generation enable signal Vswitch_En and a first power supply voltage Vcc. To this end, the first voltage generation may include a number of components. These components may include, for example, a first pump clock generator 22 and a first charge pump 24.

The second voltage generation unit 30 generates a second pump output voltage Vpgm based on a second voltage generation enable signal Vpgm_En and the first pump output voltage Vswitch. Similar to the first voltage generation unit 20, the second voltage generation unit 30 also includes a second pump clock generator 32 and a second charge pump 34.

FIG. 1A

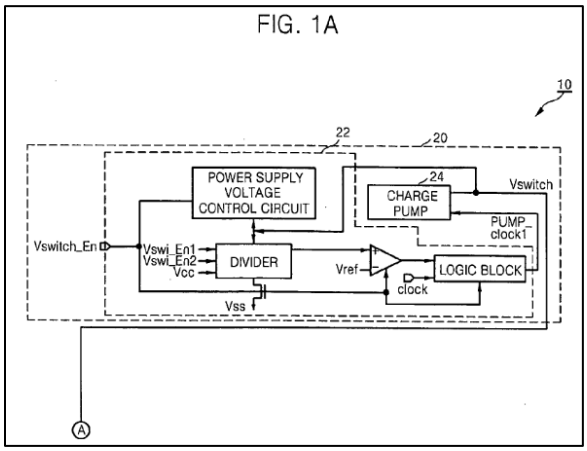
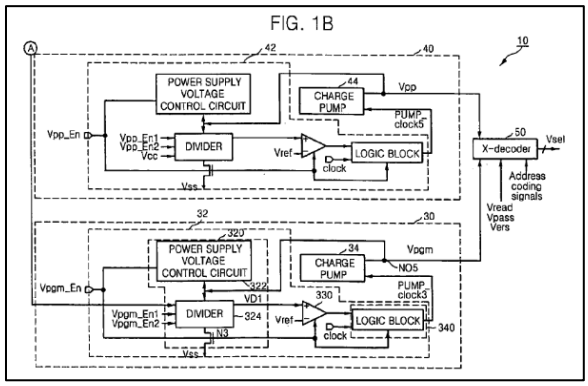
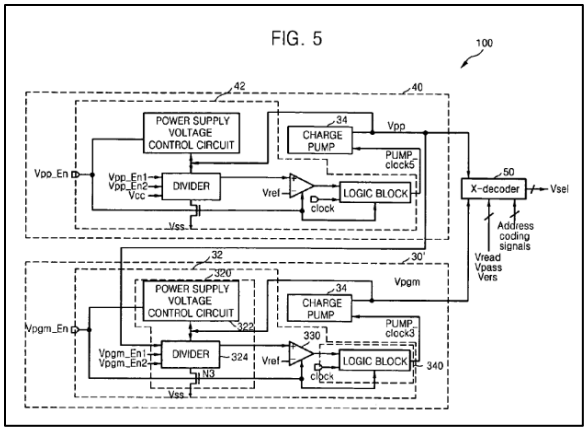


FIG. 1B



Byeon at [0057] and Fig. 5:

FIG. 5 is a block diagram of a semiconductor device 100 and is provided to compare the device 100 with exemplary disclosed embodiments. Furthermore, FIG. 6 is a graph illustrating the levels of an output voltage in the semiconductor device 100 illustrated in FIG. 5. Referring to FIGS. 1A through 6, the structure and the operation of the semiconductor device 100 illustrated in FIG. 5 is the same as or similar to that of the semiconductor device 10 illustrated in FIGS. 1A and 1B, with the exception that the semiconductor device 100 does not include the first voltage generation unit 20. Furthermore, a second voltage generation unit 30′ operates in response to the third pump output voltage Vpp generated by the third voltage generation unit 40 instead of the first pump output voltage Vswitch generated by the first voltage generation unit 20 of FIG. 1A.



Kato at Abstract:

The present invention provides a voltage generating circuit and a control method thereof which is capable of preventing an increase in the occupied area and suitable for raising the voltage of the power supply in a wide range.

This voltage generating circuit comprises a first charge pump unit to which a first clock signal is inputted, wherein the first charge pump unit generates a voltage by pumping a voltage of a first external power supply in stages by a first voltage, a voltage selector that selects the voltage generated by the first charge pump unit or a voltage of a second external power supply in accordance with a voltage selection command signal, a level converter that converts a voltage level of the first clock signal into a second voltage level, and a second charge pump unit to which the second clock signal that has been converted by the level converter is inputted, wherein the second charge pump unit and that generates a voltage and by pumping the selected voltage or the voltage of the second external power supply.

Kato at [0030]-[0035] and Fig. 3:

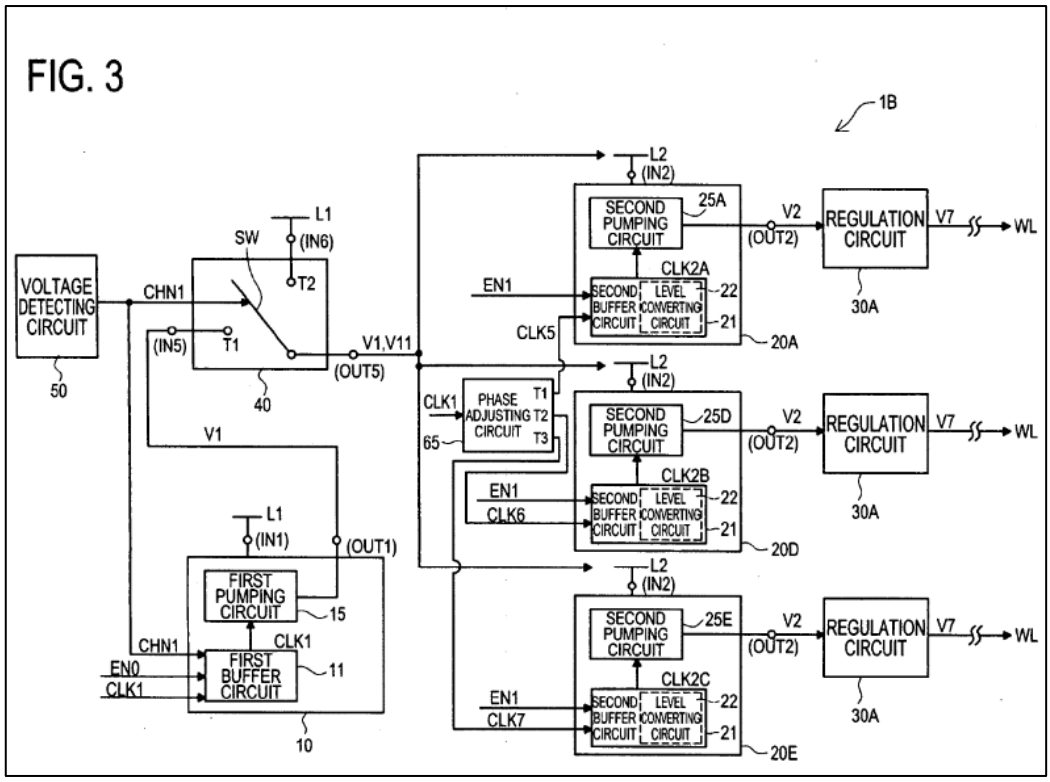
A first embodiment of the present invention will be described with reference to FIG. 1. The voltage generating circuit of the present invention will be described by taking a voltage generating unit possessed by a flash memory as an example. FIG. 1 is a block diagram showing the structure of a voltage generating portion 1 of the flash memory. The voltage generating portion 1 includes a first charge pump circuit 10, a second charge pump circuit 20, a regulation circuit 30 and a selection circuit 40.

A first charge pump circuit 10 includes a first buffer circuit 11 and a first pumping circuit 15. The first buffer circuit 11 is connected to a control circuit and an oscillation circuit (not shown). Further, the first buffer circuit 11 is connected to a voltage detecting circuit 50. The first pumping circuit 15 is connected to an external power supply line L1 via an input terminal (IN1). According to this embodiment, the value of the external power supply voltage is set to 1.8 V or 3 V. The output of the first pumping circuit 15 is connected to an output terminal (OUT1). In the meantime, the external power supply whose voltage value is 1.8 V corresponds to a first external power supply of the present invention. The external power supply whose voltage value is 3 V corresponds to a second external power supply of the present invention.

A second pumping circuit 25A of the second charge pump circuit 20A is connected to an internal power supply line L2 via an input terminal (IN2). The output of the second pumping circuit 25A is connected to an output terminal (OUT2).

The second pumping circuit 25C of the second charge pump circuit 20C are connected to the internal power supply line L2 via an input terminal (IN3). The output of the second pumping circuit 25C is connected to an output terminal (OUT4).

FIG. 3



Kato at [0039]:

The selection circuit 40 includes an input terminal (IN5), an input terminal (IN6), a switch SW, terminals T1, T2 and an output terminal (OUT5). The input terminal (IN5) is connected to the output terminal (OUT1) of the first charge pump circuit 10. Further, the input terminal (IN5) is connected to the terminal T1. The terminal T2 is connected to the external power supply line L1 via the input terminal (IN6). The switch SW is connected to the voltage detecting circuit 50 and the output terminal (OUT5). The output terminal (OUT5) is connected to the internal power supply line L2.

Dinh at Abstract:

Clock frequency and number of stages of a charge pump for nonvolatile memories are automatically adjusted to compensate for lower efficiency due to lower power supply, higher temperature, or weaker process. A low voltage detector will cause the charge pump to increase the charge pump's clock frequency and number of stages when a low voltage is detected, making the charge pump's capability constant over a voltage range. A counter timing programming/erasing

time will cause the charge pump clock frequency and number of stages to increase when the programming/erasing time exceeds certain thresholds. This boosts the charge pump's drivability for a weaker process, higher temperature, or aged cells.

Dinh at 1:42-51:

Typically, a charge pump, located on the same integrated circuit as the EEPROM array is used to generate the programming/erasing voltage. The charge pump usually includes a plurality of series-connected pump stages that are driven by two nonoverlapping clock signals. The series-connected pump stages multiply the amplitude of the clock signals. The actual voltage obtained at the charge pump output terminal depends on the number of pump stages, the clock frequency, and on the charge transfer efficiency of the pump stages.

Dinh at 5:8-22 and Fig. 4:

FIG. 4 illustrates, in partial block diagram form and partial logic diagram form, pump stages 24 of FIG. 2. Charge pump stages 24 includes a first plurality of pump stages 80, a second plurality of pump stages 82, a third plurality of pump stages 84, and a fourth plurality of pump stages 86. These pump stages are coupled together in series and include a plurality of conventional pump stages to provide output voltage HVOUT. The voltage of HVOUT is dependent upon the number of pump stages coupled in series, as well as the frequency of clock signals CLK and CLKB. Diodes 88, 90, and 92 are used to provide a backward bias protection for the plurality of pump stages 80, 82, 84, and 86. Also, included in charge pump stages 24 are OR logic gates 94 and 98 and logic gates 96, 100 and 104.

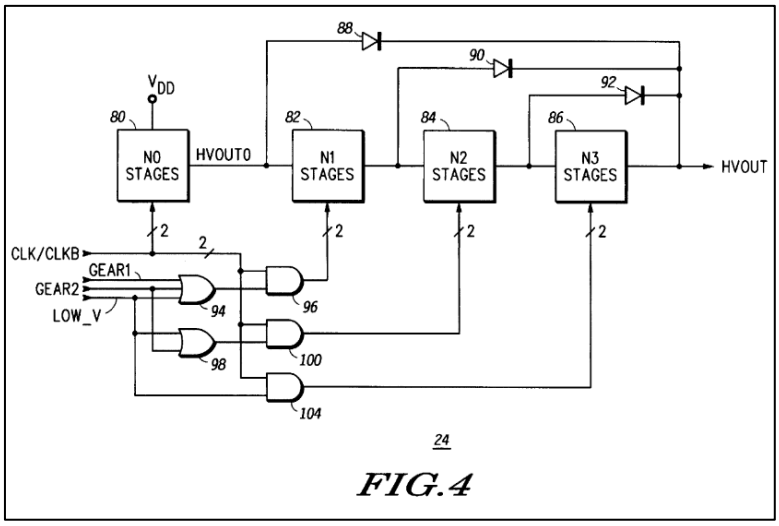


FIG. 4

To the extent that AMT contends The Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.c of its cover pleading.