

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SK HYNIX INC.,  
Petitioner,

v.

ADVANCED MEMORY TECHNOLOGIES, LLC,  
Patent Owner.

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Case IPR2025-01451  
Patent 7,969,231

**PATENT OWNER'S PRELIMINARY RESPONSE  
PURSUANT TO 37 C.F.R. § 42.107**

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**EXHIBIT LIST**

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                  |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2001           | Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 1, filed Dec. 30, 2024 (E.D. Tex.)                                                                                                                                                                             |
| 2002           | Amended Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 25, filed April 2, 2025 (E.D. Tex.)                                                                                                                                                                    |
| 2003           | Second Amended Docket Control Order, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 27, filed April 11, 2025 (E.D. Tex.)                                                                                                                                                                         |
| 2004           | Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. Micron Tech. Inc.</i> , No. 1-25-cv-01036, Dkt. No. 1, filed June 30, 2025 (W.D. Tex.)                                                                                                                                                                         |
| 2005           | Order Denying Motion for Stay Pending <i>Inter Partes</i> Review, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 79, filed Sept. 3, 2025 (E.D. Tex.)                                                                                                                                             |
| 2006           | United States District Courts — National Judicial Caseload Profile (including data through June 30, 2025), <a href="https://www.uscourts.gov/sites/default/files/document/fcms_na_distprofile0630.2025.pdf">https://www.uscourts.gov/sites/default/files/document/fcms_na_distprofile0630.2025.pdf</a> (accessed October 10, 2025). |
| 2007           | Defendant SH Hynix’s Preliminary Invalidity Contentions Cover Pleading, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)                                                                                                                                                   |
| 2008           | Omnibus Obviousness Chart C-OB for U.S. Patent No. 7,969,231, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)                                                                                                                                                             |
| 2009           | June 17, 2016 Notice of References Cited during prosecution of Application No. 14/698,542                                                                                                                                                                                                                                           |
| 2010           | U.S. Patent No. 9,690,317 to SK Hynix Inc.                                                                                                                                                                                                                                                                                          |
| 2011           | Docket Navigator Time To Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025                                                                                                                                                                                                                   |
| 2012           | Lex Machina Time to Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025                                                                                                                                                                                                                        |
| 2013           | Statutory Disclaimer, filed December 1, 2025                                                                                                                                                                                                                                                                                        |

## I. INTRODUCTION

Patent Owner Advanced Memory Technologies, LLC (“AMT”) respectfully requests that the Director deny the Petition for *inter partes* review (IPR) filed by SK Hynix Inc. (“Petitioner”) against certain claims of U.S. Patent No. 7,969,231 (the “’231 Patent”). The Petition fails to show a reasonable likelihood that Hynix would prevail with respect to any of the remaining challenged claims (claims 1, 3, and 4),<sup>1</sup> and institution would therefore be improper under 35 U.S.C. § 314(a).

**First**, the Petition fails to show that the prior art teaches or suggests the “buffer circuit” required by every challenged claim. The claims each recite a “buffer circuit” that is “configured to select” either a “first” or “second clock signal.” For each and every Ground asserted, the Petition fails to show that the cited art teaches a “buffer circuit.” Instead, Petitioner skips this recited structural “buffer” limitation and relies solely on circuits that purportedly meet the functional “configured to select” limitation. Every limitation of the claim must be shown to be disclosed or rendered obvious, and the Petition fails to present any evidence for this limitation.

**Second**, the prior art relied on suffers from myriad other deficiencies, such as:

- Petitioner identifies a triangular wave in the Abe reference (secondary in Ground 1 and the sole reference in Ground 2) as the “first clock

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<sup>1</sup> Claims 6–8 have been statutorily disclaimed. *See* EX2013.

signal,” but glosses over the fact that this wave is never used as an input to the alleged “buffer circuit.” Furthermore, Petitioner makes no effort to show how or why an ordinary artisan would have modified Abe to overcome this difference between the cited disclosure and the claimed invention, as required for obviousness.

- Hiiragizawa, which Petitioner only asserts against some of the challenged claims (Ground 3), does not disclose a “second charge pump circuit,” as recited by the challenged claims. Because it cannot identify two charge pump circuits in Hiiragizawa, Petitioner inexplicably insists that a single transistor constitutes a “charge pump circuit” and accuses AMT (without substantiation) of making similar contentions in co-pending litigation.
- Petitioner relies on two distinct embodiments from Ito, neither of which discloses all the elements of the challenged claims arranged in the manner the claims recite. But the Petition fails to show a reason why an ordinary artisan would have modified Ito by combining the distinct embodiments, as proposed for Ground 4.

For at least these reasons, and as explained in greater detail below, Petitioner cannot prevail on any Ground as to any challenged claim. The Petition should therefore be denied under 35 U.S.C. § 314(a).

## II. BACKGROUND

### A. The '231 Patent

The '231 patent was invented and developed by Seiji Yamahira of Panasonic Corporation, EX1001 at (75), a leader and pioneer in the development and manufacture of electronic equipment including semiconductors and cameras. The patent claims priority from a foreign application filed July 9, 2008 and issued on June 28, 2011. *Id.* The '231 patent is entitled “Internal Voltage Generating Circuit” and “relates to an internal voltage generating circuit employing a boost circuit.” *Id.*, at (54), 1:14–15.

#### 1. Claims

The '231 Patent issued with 8 claims. EX1001 at 10:2–64. Claims 1, 3, 6, and 7 are independent. Claims 6–8 have been disclaimed. EX2013. Claims 1 and 3 are the only remaining independent claims. EX1001 at 10:2–12, 10:18–28. Claim 1 recites:

1. An internal voltage generating circuit comprising:
  - a first boost circuit provided between a first voltage and a first terminal;
  - a second boost circuit provided between the first terminal and a second terminal;
  - a frequency dividing circuit configured to divide a first clock signal to be supplied to the first boost circuit to generate a second clock signal; and

a buffer circuit configured to select and supply the first clock signal or the second clock signal to the second boost circuit.

*Id.*, at 10:2–12. Claim 3 recites:

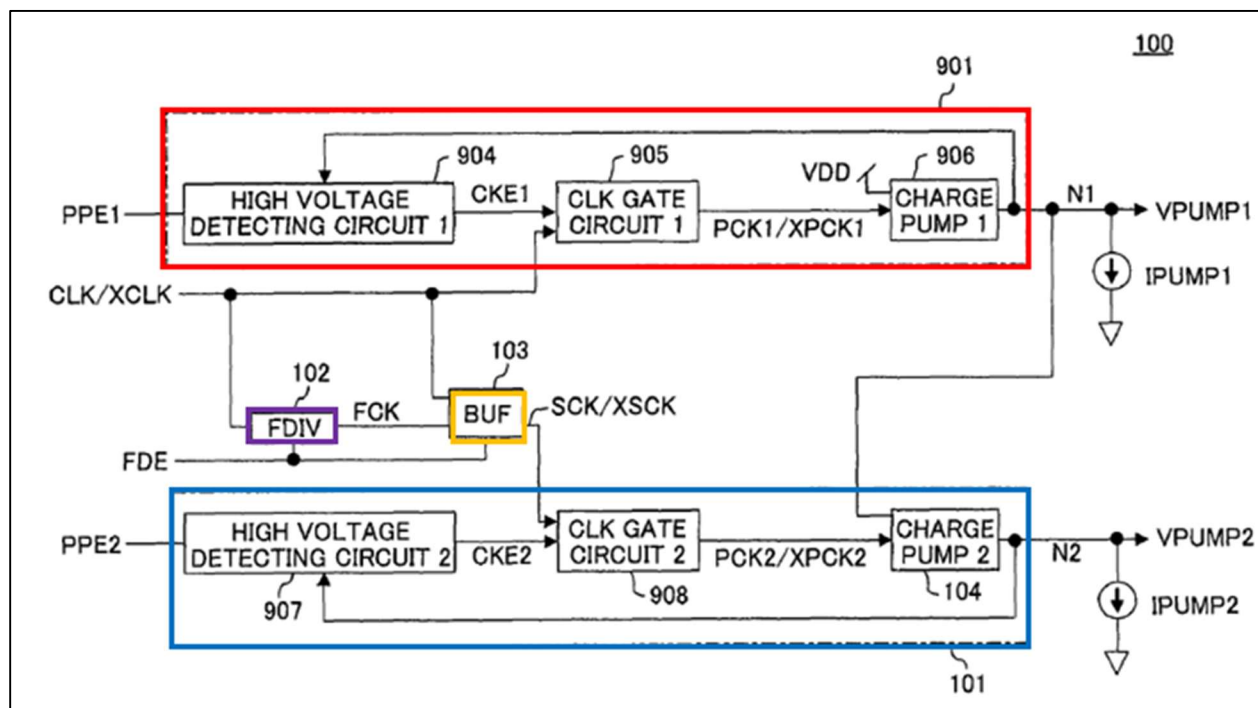
3. An internal voltage generating circuit comprising:
  - a first charge pump circuit configured to generate a second voltage from a first voltage;
  - a second charge pump circuit configured to generate a third voltage from the second voltage;
  - a frequency dividing circuit configured to divide a first clock signal to generate a second clock signal; and
  - a buffer circuit configured to select the first clock signal or the second clock signal and generate a third clock signal,wherein the third clock signal is supplied to the second charge pump circuit.

*Id.*, at 10:18–28. The remaining challenged claims depend from either claim 1 or claim 3 and incorporate the limitations of their respective base claim.

## **2. Specification**

The internal voltage generating circuit of the '231 Patent is useful in non-volatile semiconductor memory devices, such as flash memory; such devices require multiple internal voltages to perform, *e.g.*, data read or data write operations. EX1001 at 1:16–22. As shown in Figure 1, below, the '231 Patent discloses an embodiment with an internal voltage generating circuit 100 having a first boost

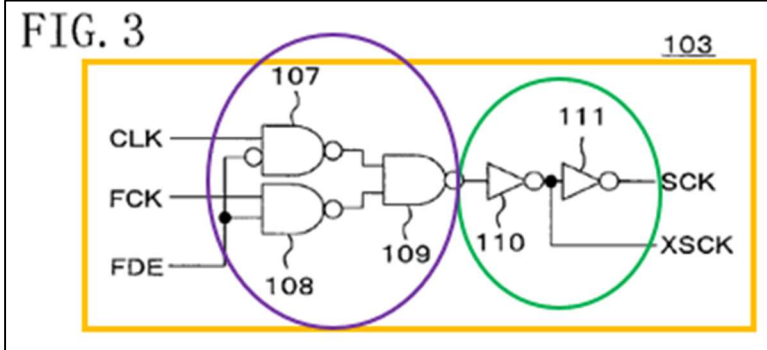
circuit 901 (highlighted in red) between a first voltage source and a first terminal. *Id.*, at 5:35–41, Fig. 1. Additionally, the internal voltage generating circuit 100 includes a second boost circuit 101 (blue) between the first terminal and a second terminal. *Id.* The '231 Patent further discloses a frequency dividing circuit 102 (purple) that divides a first clock signal into a second clock signal. *Id.* at 5:45–50. In the embodiment, a buffer circuit 103 (orange) chooses between the first clock signal and the second clock signal and sends the chosen signal to the second boost circuit 101 (blue). *Id.*, at 5:51–55.



EX1001, FIG. 1

The '231 Patent, in Figure 3, depicts a structure for buffer circuit 103 (orange). *Id.*, at 5:3–4, 6:7–8. As indicated by the purple annotations to Figure 3 (below), the buffer circuit 103 may include logic elements 107, 108, 109 that are configured to

XSCK, and act as a buffer to ensure stable clock delivery. *Id.*



**EX1001, FIG. 3**

The '231 Patent teaches that the structure of its internal voltage generating circuit provides various benefits. Boost circuits with higher current capability are slower to reach target voltages than boost circuits with lower current capability. EX1001 at 6:60–7:3. By utilizing the buffer circuit in conjunction with the frequency dividing circuit, the '231 Patent allows for adaptive control of the second boost circuit. For example, at startup, both the first and second boost circuits may be charged using the same clock signal. *Id.*, at 7:5–34. When the first boost circuit reaches target voltage, the boost operation of the first charge pump circuit stops, and the boost operation of the second charge pump circuit continues. *Id.*, at 7:45–67. After the second boost circuit reaches target voltage, both boost circuits are able to being intermittent operation to result in a more stable boosted voltage and a more

stable supply of boost current. *Id.* at 8:45–9:7. Switching the clock supplied to the second boost circuit reduces the stress on the first boost circuit and lowers the overall power consumption. *See id.*, at 8:59–9:7.

## B. Petitioner’s Asserted Grounds

The Petition asserts the following four Grounds:

| Ground | Basis                | Reference(s)                               | Claims      |
|--------|----------------------|--------------------------------------------|-------------|
| 1      | § 103 (obviousness)  | Kishimoto (EX1009) in view of Abe (EX1011) | 1, 3, and 4 |
| 2      | § 103 (obviousness)  | Abe                                        | 1, 3, and 4 |
| 3      | § 102 (anticipation) | Hiiragizawa (EX1010)                       | 3 and 4     |
| 4      | § 103 (obviousness)  | Ito (EX1008)                               | 1, 3, and 4 |

AMT summarizes Petitioner’s contentions and the disclosure on which they are based in the context of the arguments in Section VI, below. For the reasons given below, none of the references (or combinations of references) render the challenged claims unpatentable.

## III. CLAIM CONSTRUCTION

Petitioner asserts that “[n]o express constructions are required” and that it “addresses the plain meaning of certain terms in the analysis for the presented Grounds.” Petition at 12. But “a petition must state how a challenged claim is to be construed and how each element of the construed claim is found in prior art patents or printed publications.” *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*,

IPR2021-01569, Paper 16, at 5 (citing 37 C.F.R. § 42.104(b)(3)–(4)). In this case, however, Petitioner failed to address the plain meaning of the term “buffer circuit,” as discussed at greater length in Section VI below. AMT does not concede that the Petition correctly applies the plain meaning of the claim terms, nor does AMT necessarily agree that no express constructions are required. AMT reserves the right to raise arguments regarding the construction of any term, in the event of institution.

#### **IV. LEVEL OF ORDINARY SKILL IN THE ART**

Petitioner asserts that a person of ordinary skill in the art “had a master’s degree in electrical engineering, computer engineering, physics, or a related field, with at least two years of experience in the field of integrated circuits and/or memory devices. Less work experience may be compensated by a higher level of education or vice versa.” Petition at 11–12. It is unnecessary for AMT to propose a competing definition at this time because, even under Petitioner’s proposed definition, Petitioner has failed to demonstrate a reasonable likelihood of success on any of the challenged claims. AMT reserves the right to propose a different definition of a person of ordinary skill in the art if the Board institutes IPR.

#### **V. LEGAL STANDARDS**

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3))

requires that petitions must identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). To meet this burden, “the petition must specify where *each element of the claim* is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4) (emphasis added). And “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, “[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

When an expert declaration is “conclusory and unsupported,” it is “entitled to little weight.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (August 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Upjohn Co. v. Mova Pharm. Corp.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000) (“Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity

determination.”) (quoting *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985)); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 138 (Fed. Cir. 1986) (“Although in some circumstances unsupported oral testimony can be sufficient to provide prior knowledge or use, it must be regarded with suspicion and subjected to close scrutiny.”).

## **VI. PETITIONER FAILS TO SHOW A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CLAIM**

Petitioner cannot prevail on any Ground against any of the challenged claims. As shown below, none of the cited references discloses “a buffer circuit configured to select [. . .] the first clock signal or the second clock signal,” as recited by both claims 1 and 3. Additional claim limitations are absent from at least Abe, Hiiragizawa, and Ito.

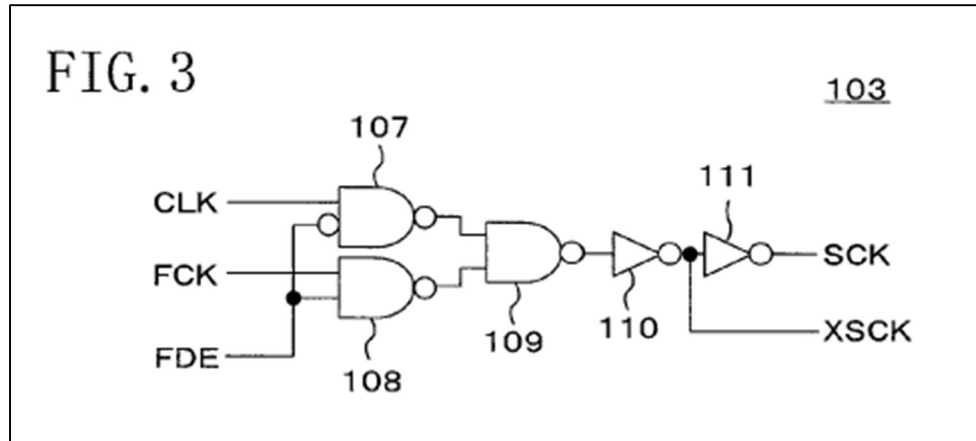
### **A. Ground 1 Fails Because Kishimoto Does Not Disclose the *Buffer Circuit* Required by the Independent Claims**

Hynix cannot prevail on Ground 1 because Kishimoto does not disclose *a buffer circuit configured to select the first clock signal or the second clock signal*, as required by both claims 1 and 3. Hynix contends that “Kishimoto’s switching circuit 52” is the claimed *buffer circuit* because it “is a multiplexer.” Petition at 23. But Hynix only addresses the selection function that the *buffer circuit* is “configured to” perform while ignoring that the term “buffer circuit” refers to a structure, independent of the selecting that it may be “configured to” perform.

**FIG. 2**

**FIG. 3**

This annotation only includes the selection logic, but the '231 Patent describes the entire structure depicted in Figure 3 (reproduced below) as the “buffer circuit 103.” EX1001 at 5:3–4, 6:7–8. The selection logic is only one part of that structure. *See id.* at 6:8–17. The inverters (110, 111) are also part of the buffer circuit, *id.* at 6:7–8, and (in the depicted embodiment) the complementary signals SCK and XSCK are both outputs, *id.* at 6:10–13, 6:14–17.



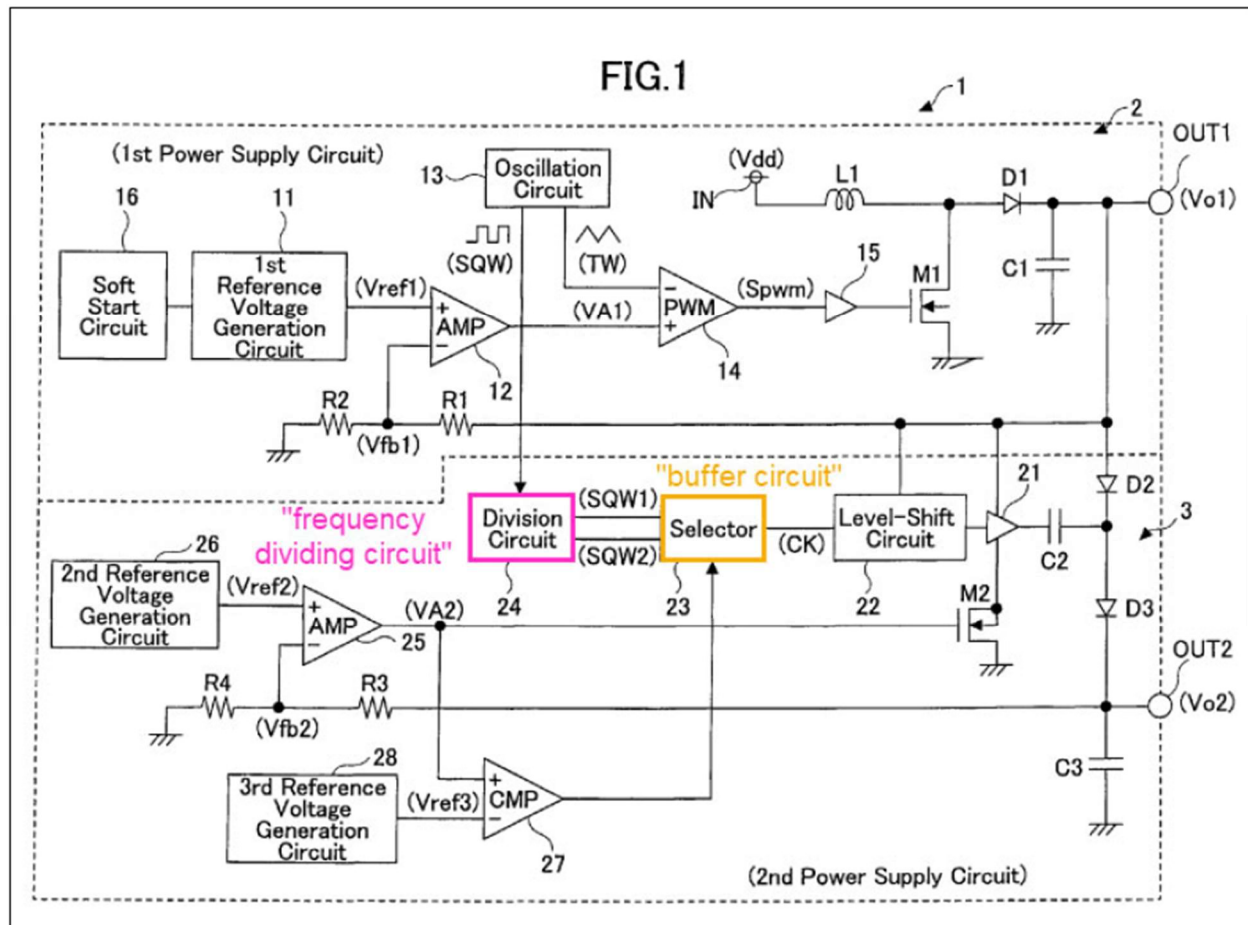
EX1001, FIG. 3

Petitioner argues that “Kishimoto’s switching circuit 52” is similar to the claimed *buffer circuit* because it “selects either CLK1 or CLK2 to output to CP20 based on a control signal from the switching control circuit 53.” Petition at 23; *see id.* at 22–23 (arguing that the selection function makes each circuit a “multiplexer”). But Petitioners focus solely on the selection logic ignores the plain claim language. Claims 1 and 3 each recite “[1] a buffer circuit [2] configured to select” between clock signals. It is not enough that a circuit be configured to perform the recited function. It must also have the recited structure: a buffer circuit.

Despite this, the Petition asserts that the cited disclosure is a “buffer” solely because it allegedly performs the selection function. *See id.*, at 22–23; *see also id.*, at 34–36 (relying on claim 1 argument for similar limitations of claim 3). By doing so, Petitioner fails to present any evidence that Kishimoto’s “switching circuit” discloses a “*buffer circuit*” that is configured to perform the recited functions of claims 1 and 3.

Petitioner also does not argue that Abe provides this limitation. *See id.*, at 27–

32. Rather, the Petition asserts that Abe “teaches an analogous buffer circuit” in the form of “selector 23,” *id.*, at 27, identified by annotation in the Figure below.



**Petition at 28 (annotating EX1011, FIG. 1)**

Petitioner makes no attempt to show that Abe’s “selector 23” has the recited structure of a “buffer circuit.” *Id.* at 28–32. Rather, the Petition attempts only to show that Abe’s “selector 23” performs the recited selection function. *See id.* But, as previously explained, that theory ignores a limitation of the claims.

For at least these reasons, Petitioner cannot prevail on Ground 1 of the Petition against any challenged claims.

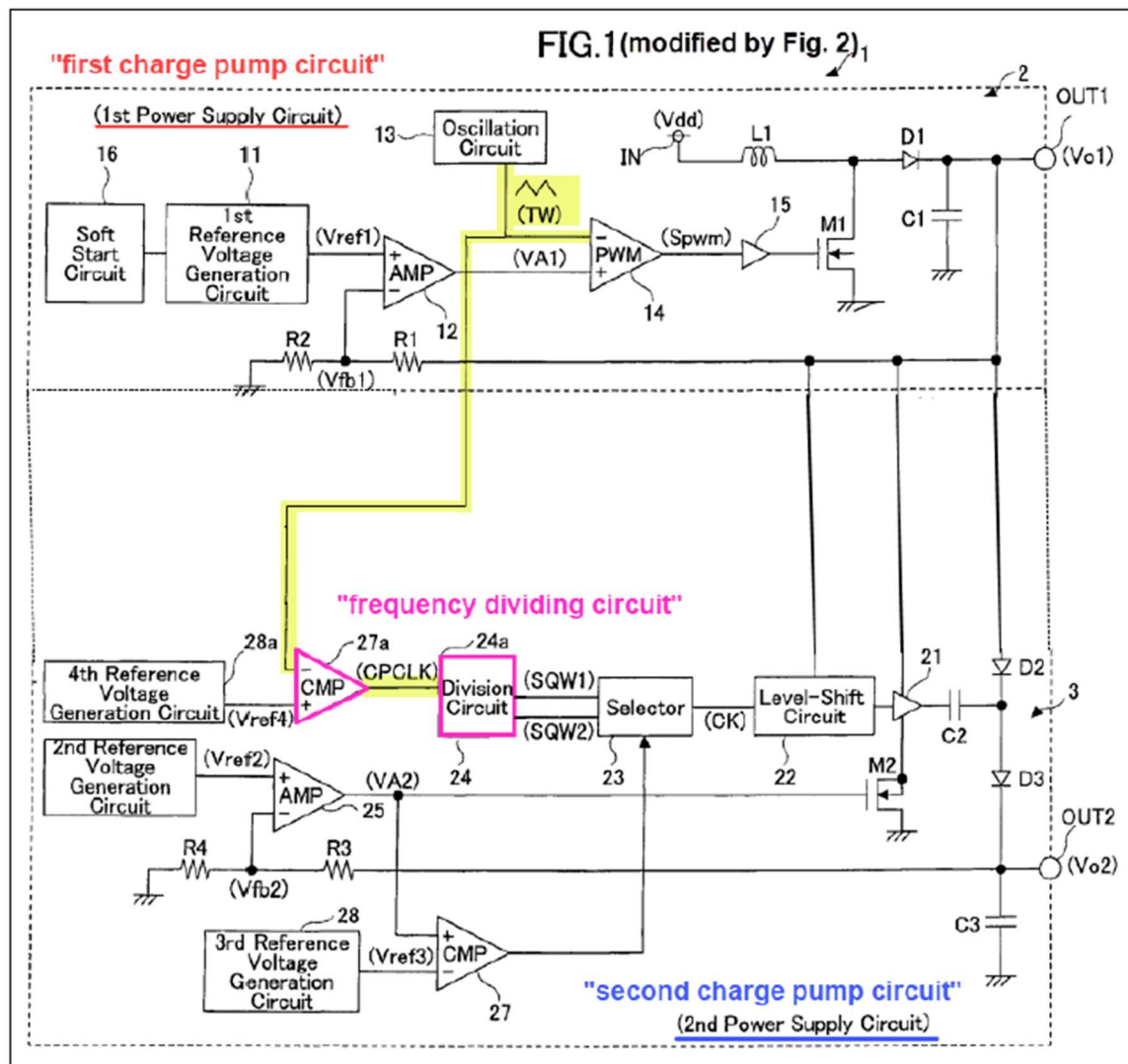
**B. Ground 2 Fails Because Abe Does Not Disclose All the Limitations of the Independent Claims**

Ground 2 fails for similar reasons to Ground 1 because, as noted above, Petitioner relies on Abe’s “selector 23” for the recited *buffer circuit* without making any attempt to show that the “selector” has the recited structure: a *buffer*. See Petition at 51–53, 56–57. Similar to its arguments for Ground 1, Petitioner argues that Abe’s “selector 23” is a *buffer circuit* because (according to Petitioner) both it and “the claimed ‘buffer circuit’ of the ’231 Patent . . . [are] multiplexer[s].” *Id.*, at 51. Compare *id. with id.*, at 22–23 (similar argument about Kishimoto’s “switching circuit 52”).

Independent of this deficiency, Ground 2 also fails because, even under the Petition’s theory, Abe’s selector does not select between the alleged *first clock signal* and *second clock signal*, as required for the *buffer circuit* claimed. EX1001 at 10:10–12, 10:25–26. Petitioner identifies the triangular wave (“TW” in Abe’s Figures) as the *first clock signal* for both claim 1 and claim 3. Petition at 52, 56. The alleged *second clock signal*, according to the Petition, would be one of two square waves (“SQW1 or SQW2” in Abe’s Figures), *id.*, which supposedly would be generated by dividing the triangular wave TW. See *id.*, at 51. The triangular wave TW is never

received by the selector, even in the modified version of Abe on which the Petition relies.

First, Petitioner argues that it would have been obvious to combine features of Abe's Figure 1 and Figure 2 embodiments, as depicted in the modified, annotated Figure below (reproduced from the Petition). *See* Petition at 48–50.

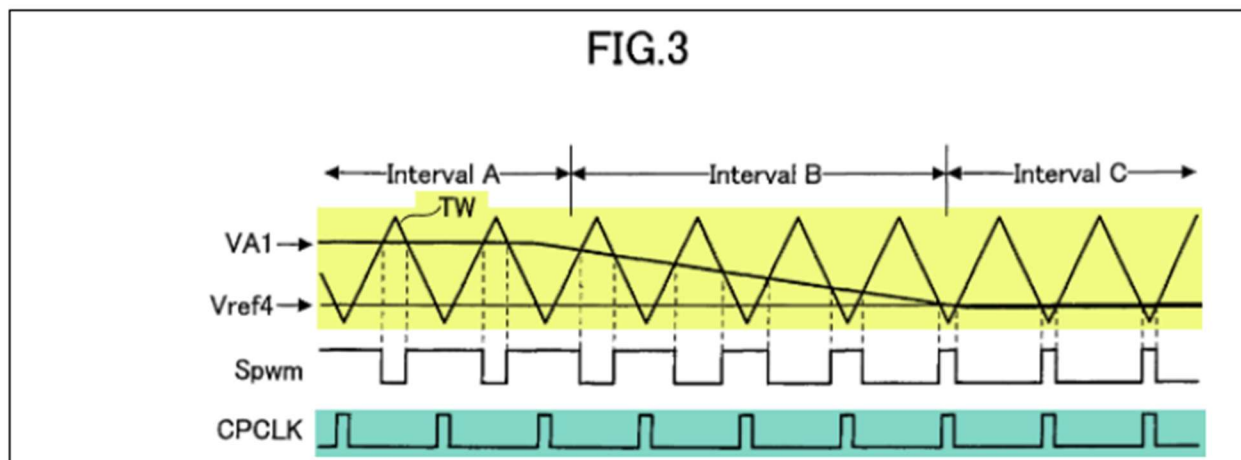


**Petition at 50 (combining EX1011, FIGS. 1 & 2; annotating)**

In this modified version of Abe's device (as in Figure 2), triangular wave TW is supplied (in inverted form), along with a reference voltage ( $V_{ref4}$ ), to comparator

27a (CMP). *See* EX1011 at 10:40–43, FIG. 2. Comparator 27a outputs a signal labeled CPCLK in both Figure 2 and Petitioner’s modified Figure.

As shown in the modified figure from the Petition, CPCLK is the input received by Abe’s “division circuit 24a”; the division circuit does not receive triangular wave TW. *See* Petition at 50 (“[T]he output signal CPCLK from the comparator 27a is input to the division circuit 24a,’ which ‘divides the frequency of the output signal CPCLK by the present division ratio.’” (quoting EX1001 at 11:61–64)). Indeed, as shown in Petitioner’s own annotations to Abe’s Figure 3 (below), CPCLK is a **rectangular wave** and not a triangular wave at all.



**Petition at 51 (annotating EX1011, FIG. 3)**

Moreover, as a rectangular wave, CPCLK can be divided into square waves (SQW1, SQW2) using “division circuit 24a,” as depicted in Abe’s Figure 2 and Petitioner’s combination of Abe’s Figures 1 and 2 (above). *See* EX1011 at 10:43–48, FIG. 2. Petitioner does not attempt to argue that it would have been obvious to

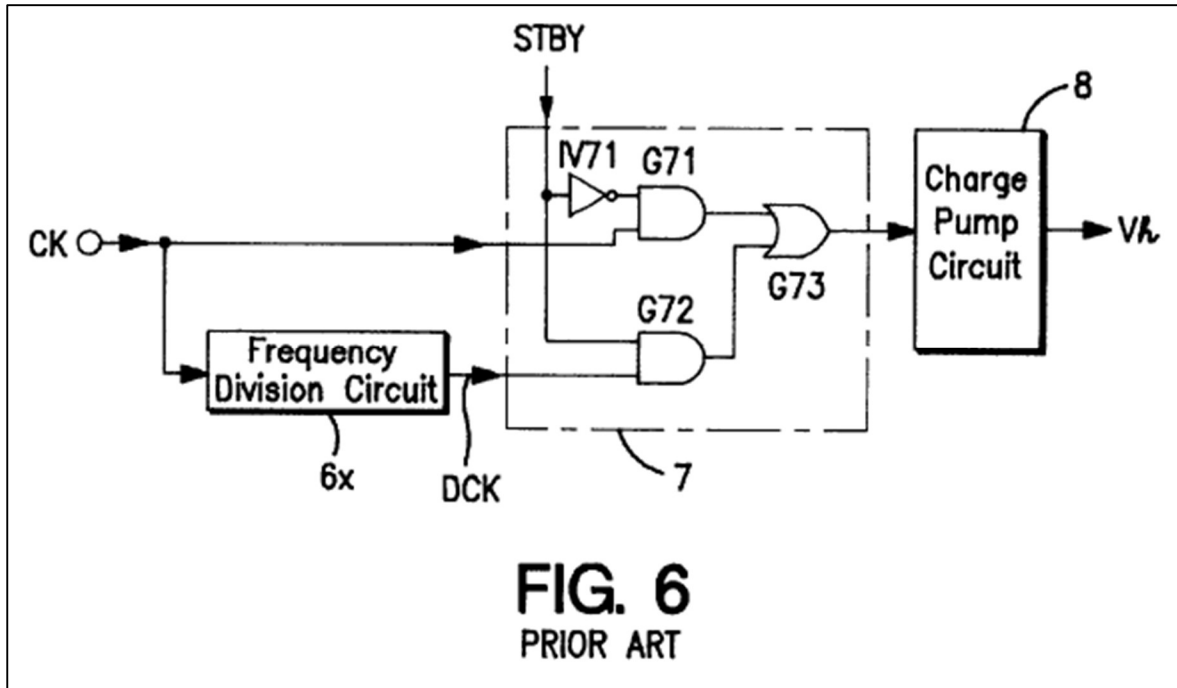
remove comparator 27a or that “division circuit 24a” could be used to divide a triangular wave to produce square waves SQW1 and SQW2.

Instead, Petitioner asserts that CPCLK has “the same frequency as the input triangular signal TW,” then assumes that this means the dividing circuit is configured to divide TW as the *first clock signal*. Petition at 50–51. The Petition makes no attempt to justify this assumption, nor could it have done so. The claims recite “a first clock signal” and “a second clock signal,” and frequency is only one characteristic of a clock signal. Abe itself shows this, given the need to convert triangular wave TW into a rectangular signal with the same frequency.

Because Abe does not satisfy all the limitations of the claims, even with Petitioner’s proposed modifications, Ground 2 fails.

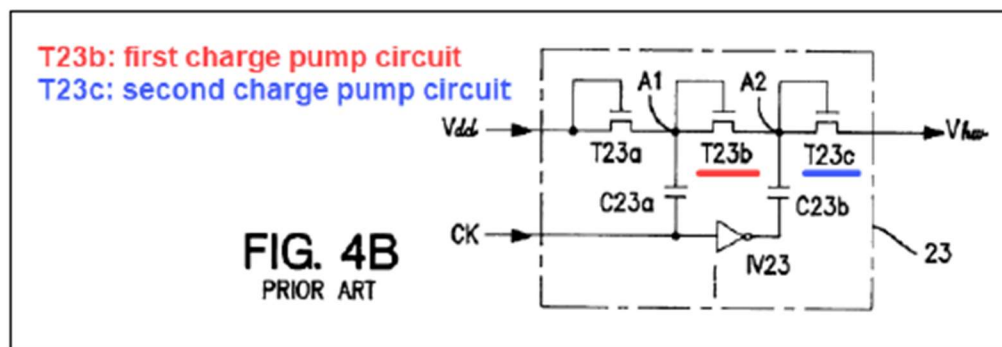
**C. Ground 3 Fails Because Hiiragizawa Does Not Disclose All the Limitations of Independent Claim 3**

Ground 3 fails because Hiiragizawa cannot anticipate independent claim 3. (Petitioner does not even assert that Hiiragizawa renders claims 1 or 2 unpatentable. Petition at 1.) Indeed, Hiiragizawa does not even disclose the *second charge pump circuit* required by the claimed invention. As shown in Figure 6 of Hiiragizawa (reproduced below), the device of Hiiragizawa includes a single “charge pump circuit 8.” EX1010, FIG. 6; *see also id.*, FIG. 1.



EX1010, FIG. 6

Petitioner attempts to overcome this glaring omission from the cited reference by asserting that a single transistor (T23b) is the *first charge pump circuit* and a second, single transistor (T23c) is the *second charge pump circuit*. See Petition at 66. This is illustrated by Petitioner’s annotations to Figure 4 of Hiiragizawa (below).



Petition at 66

Petitioner makes no effort to show that an ordinary artisan would have considered a single transistor to be a “charge pump circuit,” in the ordinary and

customary meaning of that term. Petitioner instead refers to AMT’s litigation infringement contentions, but fails to show that AMT has ever asserted that a single transistor could constitute a *charge pump circuit* of the claimed invention. *See id.* at 66–67. Indeed, Petitioner makes no effort to show that any alleged “charge pump circuit” in Hiiragizawa bears any structural similarity to a corresponding structure in an accused product. In short, there is no evidence that Hiiragizawa discloses a *second charge pump circuit*, as required by claim 3.

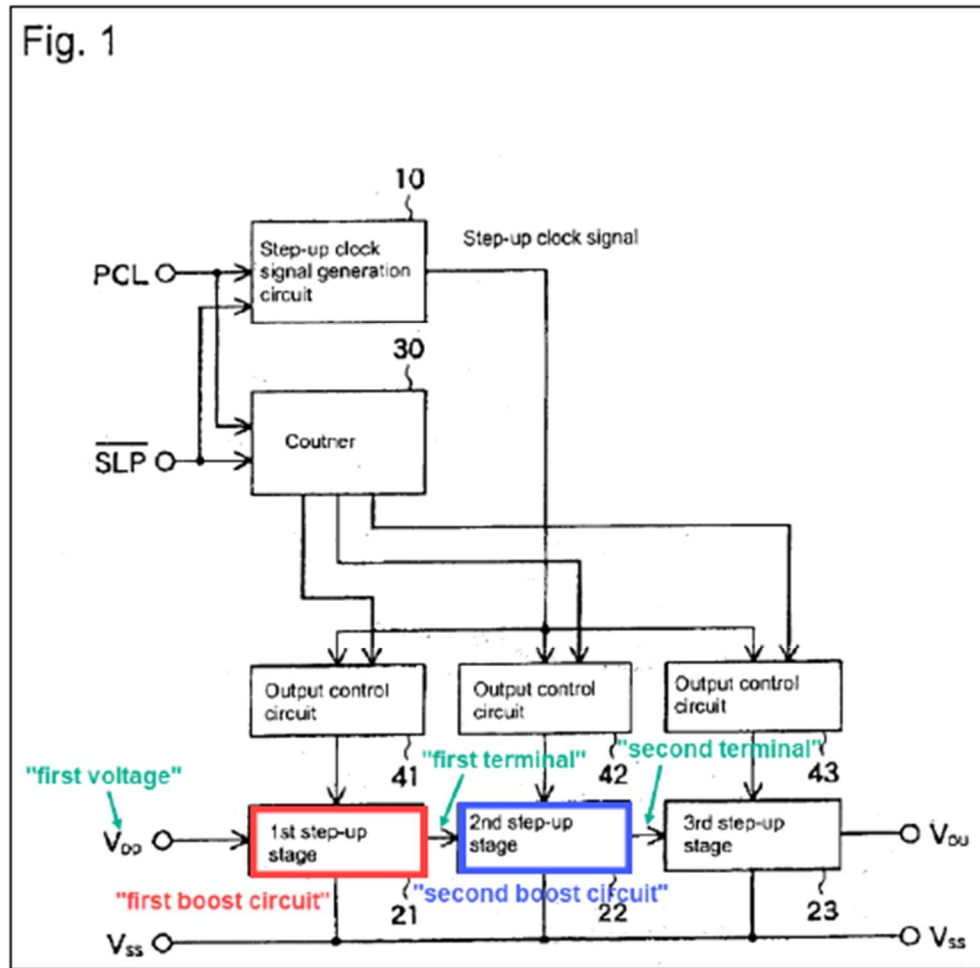
Independent of the foregoing, Ground 3 also fails because Petitioner, as it did in Grounds 1 and 2, fails to show that the alleged *buffer circuit* has the required structure. *See* Petition at 69. Petitioner relies on Hiiragizawa’s “switching circuit 7” for the recited *buffer circuit* without making any attempt to show that the “selector” has the recited structure: a *buffer*. *See id.* Instead, Petitioner’s sole argument is that “switching circuit 7” allegedly performs the selection function recited by claim 3. *See id.*, at 69–70.

**D. Ground 4 Fails Because Ito Does Not Disclose All the Limitations of the Independent Claims**

Ground 4 fails in part because Petitioner, as it did in Grounds 1–3, fails to show that the alleged *buffer circuit* has the required structure. *See* Petition at 86–87. Petitioner relies on Ito’s “selector circuit 70” for the recited *buffer circuit* without making any attempt to show that the “selector” has the recited structure: a *buffer*. *See id.* Instead, Petitioner once again relies on the argument that a multiplexer is a

buffer circuit, *i.e.*, because the '231 Patent teaches embodiments of buffer circuits that allegedly perform as multiplexers. *See id.* That argument remains flawed, as shown in the discussion of Ground 1 above.

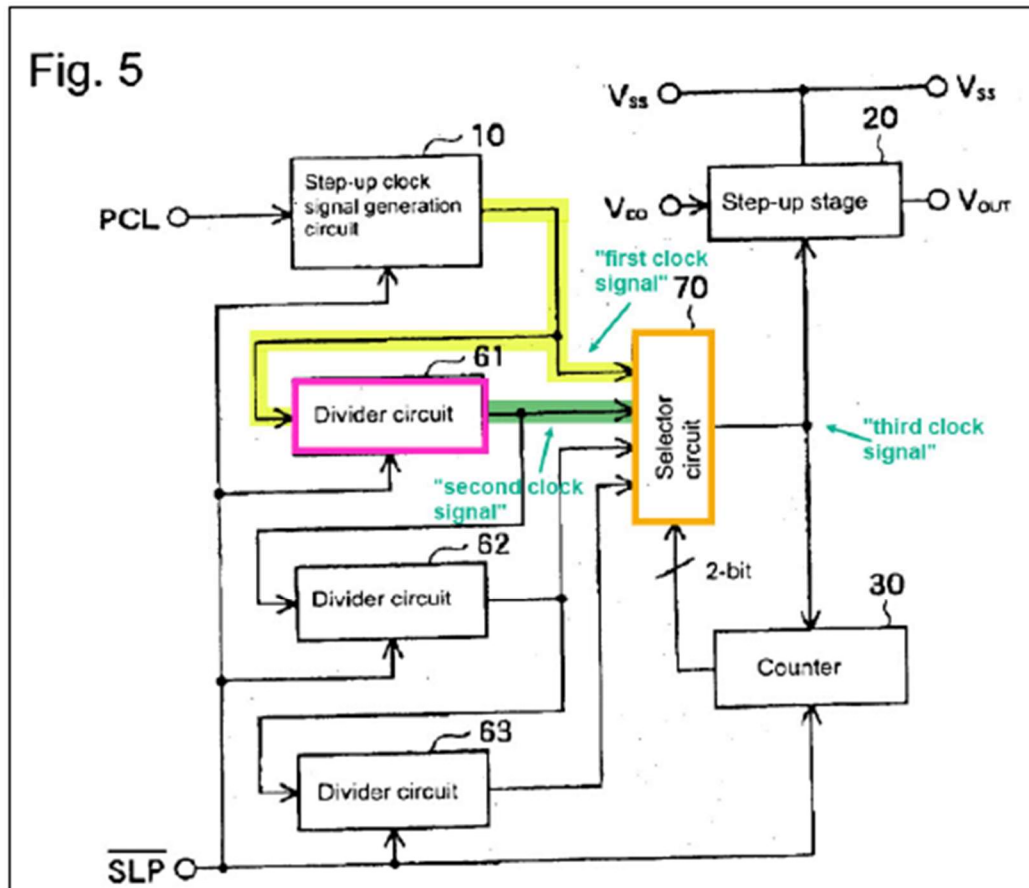
Independent of this deficiency, Ground 4 also fails because Petitioner relies on a combination of disparate teachings from multiple embodiments of Ito but fails to meet its burden of proving such a combination would have been obvious. *See Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361 (Fed. Cir. 2016) (“[I]n appropriate circumstances, a patent can be obvious in light of a single prior art reference *if it would have been obvious to modify that reference to arrive at the patented invention.*” (italics added)). Claim 1 of the '231 Patent recites “first” and “second boost circuit[s],” and claim 3 recites “first” and “second charge pump circuit[s].” EX1001 at 10:3–6, 10:19–22. For these limitations, Petitioner relies on Figure 1 of Ito. Petition at 80–84, 88–90. As illustrated by the annotated Figure below, Petitioner identifies Ito’s “first step-up stage 21” and “second step-up stage 22” as the *first* and *second boost circuits* of claim 1. *See id.* at 83. Likewise, Petitioner identifies the same two components as the *first* and *second charge pump circuits* of claim 3. *See id.* at 89.



Petition at 83 (annotating EX1008, FIG. 1)

For the recited *frequency divider circuit* and *buffer circuit* of each claim, Petitioner relies instead on the embodiment of Ito's Figure 5. See Petition at 84–87, 90–92. Ito's Figure 5 depicts only a single “step-up stage 20,” as shown in the annotated version from the Petition (reproduced below). EX1008, FIG. 5. And, as evident from Figure 1 above, Ito does not disclose any divider circuits or selection circuits in the embodiment of Figure 1. *Id.*, FIG. 1. And Ito teaches that Figure 1 and Figure 5 depict distinct embodiments. See, e.g., *id.*, at 3:10–12 (“FIG. 1 shows a block diagram of a structure of a Step-up circuit in accordance with *a first*

*embodiment* of the present invention.” (emphasis added)), 3:22–24 (“FIG. 5 shows a block diagram of a structure of a step-up circuit in accordance with *still other embodiments* of the present invention.” (emphasis added)).



Petition at 92 (annotating EX1008, FIG. 5)

Petitioner also relies, at least in part, on Ito’s statement that the embodiment of Figure 5 includes “at least one step-up stage 20.” EX1008 at 5:58; *see* Petition at 82, 83–84. Ito provides no additional detail regarding how a second (or subsequent) step-up stage would be connected to any of the divider circuits 61–63 or the selector circuit 70. And the Petition makes no effort to show how or why an ordinary artisan

would have connected these various components in a manner that would have achieved the claimed invention.

Because Petitioner relies on the combined teachings of multiple embodiments of Ito for each of the claims, Petitioner must show that the combination of teachings would have been obvious to an ordinary artisan. *See Arendi S.A.R.L.*, 832 F.3d at 1361. Petitioner fails to do so. The Petition includes no obviousness analysis at all for claim 1. *See* Petition at 80–87. And the only obviousness discussion presented for claim 3 fails to address any connection between the divider and selector circuits 61–63, 70 and the alleged *second charge pump circuit* (which is absent from Figure 5). *See id.*, at 93–94. In any event, that discussion is based on conclusory expert testimony. Specifically, the Petition asserts that the proposed combination “would involve no more than a routine combination of known circuit elements.” *Id.*, at 94. But the only proffered evidence is the declaration of Dr. Carl Sechen, which merely parrots the Petition without adding any additional support, analysis, or reasoning. *See* EX1002 ¶ 202. That testimony cannot support the Petition. *See Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (August 24, 2022) (precedential) (holding testimony insufficient when “it merely repeats, *verbatim*, the conclusory assertion for which it is offered to support”).

Accordingly, Petitioner has no chance of prevailing as to Ground 4 against any challenged claim.

## VII. CONCLUSION

For at least the reasons stated herein, AMT respectfully requests that the Director (or his delegee) deny institution of *inter partes* review in this proceeding.

Dated: December 1, 2025

Respectfully submitted,

By: /Michael F. Heim /  
Michael F. Heim (Reg. No. 32,702)  
Attorney for Patent Owner  
Advanced Memory Technologies,  
LLC

**CERTIFICATE OF SERVICE**

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,969,231 was served to the following counsel of record for SK Hynix as follows:

| Lead Counsel for Petitioner                                                                                                                                                                | Back-up Counsel for Petitioner                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| James M. Glass (Reg. No. 46,729)<br>jimglass@quinnemanuel.com<br><br>QUINN EMANUEL URQUHART<br>& SULLIVAN, LLP<br>295 5TH Avenue, 9th Floor<br>New York, NY 10016<br>Phone: (212) 849-7000 | Brian Saunders (Reg. No. 72,451)<br>briansaunders@quinnemanuel.com<br>QUINN EMANUEL URQUHART &<br>SULLIVAN, LLP<br>1300 I St NW #900<br>Washington, DC 20005<br>Phone: (202) 538-8000<br><br>Kevin (Gyushik) Jang ( <i>pro hac vice to be<br/>filed</i> )<br>kevinjang@quinnemanuel.com<br>QUINN EMANUEL URQUHART &<br>SULLIVAN, LLP<br>50 California Street, 22nd Floor<br>San Francisco, California 94111<br>Phone: (415) 875-6600<br><br>John Yin ( <i>pro hac vice to be filed</i> )<br>johnyin@quinnemanuel.com<br>QUINN EMANUEL URQUHART &<br>SULLIVAN, LLP<br>865 S. Figueroa St., 10th Floor<br>Los Angeles, CA 90017<br>Phone: (213) 443-3000 |

Dated: December 1, 2025

Respectfully submitted,

By: /Michael F. Heim /

CASE IPR2025-01451

PATENT 7,969,231

Michael F. Heim (Reg. No. 32,702)

Attorney for Patent Owner

Advanced Memory Technologies, LLC

**CERTIFICATE OF WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 4,380 words.

Dated: December 1, 2025

Respectfully submitted,

By: /Michael F. Heim /  
Michael F. Heim (Reg. No. 32,702)  
Attorney for Patent Owner  
Advanced Memory Technologies, LLC