

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK hynix Inc.
Petitioner

v.

Advanced Memory Technologies, LLC
Patent Owner

IPR2025-01452
Patent No. 7,777,557

**DECLARATION OF CARL SECHEN, PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,777,557**

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EXHIBIT LIST

Ex.	Description
1001	U.S. Patent No. 7,777,557 (“’557 patent”)
1002	File History for U.S. Patent No. 7,777,557
1003	Declaration of Dr. Carl Sechen
1004	<i>Curriculum vitae</i> of Dr. Carl Sechen
1005	U.S. Patent No. 6,107,864 (“Fukushima”)
1006	U.S. Patent No. 6,501,325 (“Meng”)
1007	U.S. Patent No. 6,914,791 (“Park”)
1008	<i>Advanced Memory Techs., LLC v. SK hynix Inc.</i> , No. 2:24-cv-01078-JRG-RSP (E.D. Tex. Apr. 2, 2025), Infringement Contentions Exhibit A (Patent Owner’s infringement claim chart for ’557 patent)
1009	G. Campardo et al., <i>VLSI-Design of Non-Volatile Memories</i> , Springer (2005)
1010	M.-D. Ker et al., “Design of Charge Pump Circuit With Consideration of Gate-Oxide Reliability in Low-Voltage CMOS Processes,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. 41, No. 5, pp. 1100-07 (May 2006)
1011	J. F. Dickson, “On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique,” <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-11, No. 3, pp. 374-78 (June 1976)

I. INTRODUCTION

1. I have been retained on behalf of SK hynix Inc. (“SK hynix” or “Petitioner”) as an independent expert consultant in this *Inter Partes* Review (“IPR”) proceeding before the United States Patent and Trademark Office against Advanced Memory Technologies, LLC (“Patent Owner”) regarding U.S. Patent No. 7,777,557 (“’557 patent”) (EX1001).¹

2. I have been asked to submit this Declaration on behalf of Petitioner in connection with Petitioner’s related petition for IPR of the ’557 patent, which I am informed is being filed concurrently with this declaration. I have been asked to consider whether certain references disclose or render obvious the features recited in claims 1-12 and 14 (collectively, the “Challenged Claims”) of the ’557 patent. My opinions are set forth below. Based on my experience and expertise, it is my opinion that the prior art anticipates and/or renders obvious all limitations of the Challenged Claims, as I discuss in detail below.

3. I receive compensation at an hourly rate of \$500 per hour for my time working on this matter, plus expenses. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’557 patent.

outcome of this or any other proceeding. I have no financial interest in SK hynix or in the patents involved in this litigation.

4. I am personally knowledgeable about the matters stated herein and am competent to make this Declaration. All of my opinions stated in this Declaration are based on my own personal knowledge and professional judgment. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth in this Declaration.

II. BACKGROUND AND QUALIFICATIONS

5. My qualifications and credentials are set forth herein as further evidenced by my *curriculum vitae* (EX1004).

6. I earned a B.E.E. in Electrical Engineering from the University of Minnesota in 1975, followed by an M.S. in Electrical Engineering from the Massachusetts Institute of Technology in 1977. I earned a Ph.D. in Electrical Engineering from the University of California, Berkeley in 1986.

7. I have been a Professor of Electrical Engineering for 39 years. Since August 15, 2005, I have been a Professor of Electrical and Computer Engineering at the University of Texas at Dallas. From July 1992 to August 14, 2005, I served as a Professor of Electrical Engineering at the University of Washington. From July 1986 through June 1992, I served as an Assistant Professor and then Associate Professor of Electrical Engineering at Yale University.

8. Over these years, my research has focused on the design and computer-aided design of digital integrated circuits, including the design of dynamic random-access memory (“DRAM”) and static random-access memory (“SRAM”) modules. I have also designed several chips that included various types of embedded DRAM (eDRAM). In this research work, I have designed multiple sense amplifier circuits for the various DRAMs, embedded DRAMs, and SRAMs. I have authored or coauthored over 200 papers and one book, the majority of which concern digital integrated circuit design and memory design. I have also designed, fabricated and tested numerous integrated circuits.

9. As a professor, I have developed and taught numerous courses, including several courses that teach digital integrated circuit design and memory design, including extensive coverage of flash memory design. I have taught these courses continuously for the past 30 years. I have taught digital integrated circuit design and memory design, including flash memory design, to undergraduate and graduate students at the University of Washington and at the University of Texas at Dallas. DRAM and embedded DRAM design is covered in these courses, as is the design of sense amplifier circuits for various types of memory. NAND-Flash memory design is taught in detail, including both SLC (single-level cell) and MLC (multi-level cell) variants.

10. I was elected a Fellow of the Institute of Electrical and Electronics Engineers (“IEEE”) in 2002 for contributions to placement and routing of ASICs. Since then I have been promoted to Life Fellow. IEEE is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of “Fellow” to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

11. I received several research and teaching awards during my career. I received the Semiconductor Research Corporation’s Inventor’s Recognition Award in 1988 and in 2001. I also received the Technical Excellence Award from the Semiconductor Research Corporation in 1994. While serving as a professor at the University of Washington, I received the Outstanding Research Advisor award from the Department of Electrical Engineering in 2002. In 2008, I received the Distinguished Teacher of the Year Award from the Department of Electrical and Computer Engineering (ECE) at the University of Texas at Dallas. I also received the Distinguished Teaching Award for the Erik Johnson School of Engineering and Computer Science in 2014. In addition, I received the Graduate Teaching Excellence Award from the ECE Department at UT Dallas, May 2024.

12. Over the years, I have also received funding to conduct research in computer circuits and memory designs, including area-efficient and reliable embedded DRAM and SRAM design. Together with my graduate students, I have designed and fabricated various types of computational VLSI chips.

13. I am a co-inventor on four issued patents directed to transistor and computational logic technologies. Three of the patents concern transistor-level programmable logic.

14. Additional details about my employment history, fields of expertise, courses taught, and publications are further included in my *curriculum vitae* attached as EX1004.

15. In summary, I am an expert in the field of circuit design generally and as applied within the context of the '557 patent, including the design of flash memory and other non-volatile memories ("NVM"). As set forth above, my experience includes practical product development, including performance considerations and design choices involving the memory technology state of the art before the earliest, January 17, 2007, priority date applicable to the Challenged Claims.

16. Based on my professional experience, I believe I am qualified to testify as an expert on matters related to the '557 patent. As an expert, I am qualified to evaluate, interpret and rely on reports, patents, scholarly papers and professional opinions of others, within my areas of expertise, as to authenticity and accuracy.

Moreover, I am qualified to provide an opinion as to what a person of ordinary skill in the art (“POSITA”) would have understood, known and concluded before January 17, 2007, including the context in which a POSITA would understand and construe teachings and terminology in written publications.

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

17. In preparing this Declaration, I have reviewed the ’557 patent and have considered each of the documents cited herein upon which I specifically rely. In formulating my opinions, I have relied upon my experience, education, and knowledge in the relevant art, including other background documents. I have also considered the viewpoint of a person of ordinary skill in the art of computer memories at the time of the alleged invention of the ’557 patent, that is, close to, but earlier than January 17, 2007.

18. This Declaration is limited to my opinions on invalidity with respect to the Challenged Claims 1-12 and 14 of the ’557 patent. Those opinions, as set forth in detail in this Declaration, are summarized below:

A. The Challenged Claims 1, 3, 5, 10-12, and 14 are anticipated by U.S. Patent No. 6,107,864 (“Fukushima”), including incorporated references.

B. The Challenged Claims 1-3, 9, 10, and 14 are anticipated by U.S. Patent No. 6,501,325 (“Meng”), including incorporated references.

C. The Challenged Claims 1-12 and 14 are obvious over Meng, including incorporated references, in view of U.S. Patent No. 6,914,791 (“Park”) and the knowledge of a POSITA of the extensive background technology.

19. While Fukushima, Meng, Park, and other references cited below as background technology form the primary bases for my opinion, I note that there are many other relevant references which further support a finding of invalidity as discussed herein. I reserve the possibility of amending or supplementing this Declaration should additional information arise which may affect my opinions.

IV. LEGAL UNDERSTANDING

20. I am not an attorney. However, as outlined in my *curriculum vitae* addended hereto as EX1004, I have formed and presented opinions according to my technology expertise and the legal standards which are relevant to my analysis and opinions. I summarize here the understandings relevant for this declaration, noting that greater detail may be provided upon any cross-examination, and others may be provided for any amendment or supplementation reserved above.

21. **What Constitutes Prior Art that May Invalidate a Patent.** I understand that former 35 U.S.C. § 102 (*i.e.*, Pre-AIA § 102) listed conditions that may invalidate a patent, including what is considered “prior art” to a patent such as the ’557 patent. I understand the most pertinent conditions are:

(i) under § 102(a), if the invention was known or used by others in this country, or was patented or described in a printed publication in this or a foreign country, before the date of the invention of the asserted patent; or

(ii) under § 102(b), if the invention was patented or described in a printed publication in this or a foreign country, or in public use or on sale in this country, more than one year before the effective filing date of the asserted patent; or

(iii) under § 102(e), if the invention was described in (a) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (b) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent.

22. I understand that one or more of the above conditions apply to the art relied upon here for my invalidity analysis.

23. **How the Prior Art Is Applied in the Invalidity Analysis:**
Anticipation. I understand that a patent claim may be found to be invalid as “anticipated” under a subsection of Pre-AIA 35 U.S.C. § 102 if a single prior art reference (including any other prior art incorporated by reference in the prior art document) under that subsection describes every element of the claim explicitly or

inherently (*i.e.*, necessarily present) as understood by a POSITA to allow making and using the claimed invention.

24. How the Prior Art Is Applied in the Invalidity Analysis:

Obviousness. I understand that a patent claim may be invalid as “obvious” under Pre-AIA 35 U.S.C. § 103 if the differences between the claimed invention and the prior art (including any other prior art incorporated by reference in the prior art document) are such that the claimed invention, as a whole, would have been obvious to a POSITA before the effective filing date of the claimed invention. The analysis calls for consideration of (a) level of ordinary skill in the pertinent art; (b) the scope and content of the prior art; (c) the differences between the prior art as a whole and the claim at issue; and (d) as appropriate, objective indicia of non-obviousness. The objective indicia, appropriate if there is a nexus with the claimed invention, include: (1) commercial success attributable to the invention; (2) long-felt but unsolved need for the invention; (3) failure of others; (4) skepticism by experts; (5) praise by others; (6) teaching away by others; (7) recognition of a problem which the claimed invention addresses; (8) copying by others; and (9) unexpected results.

25. I understand that obviousness may be found on a single reference (and any of its incorporated references) considered in view of the knowledge of the POSITA, and that a patent that incorporates another document by reference includes the disclosure of the incorporated document as if it was explicitly contained in the

patent. Where multiple references are proffered, I understand that while there is no requirement of an explicit teaching, suggestion or motivation to combine, generally there needs to be put forth some reason why a POSITA (if only by common sense or ordinary creativity) would have made the particular combination and that there is a reasonable expectation of success of the combination.

V. PERSON OF ORDINARY SKILL IN THE ART

26. I am informed by counsel that “a person of ordinary skill in the art at the time of the inventions” (“POSITA”) is a hypothetical person who is presumed to be familiar with the relevant field and its literature at the time of the invention. I have further been informed that this hypothetical POSITA would also be a person of ordinary creativity, capable of understanding the scientific principles applicable to the relevant field, and not an automaton.

27. In view of this instruction, my experience with the issues, and the ’557 patent, it is my opinion that a POSITA as of January 17, 2007, would have had a master’s degree in electrical engineering, computer engineering, physics, or a related field, with at least two years of experience in the field of integrated circuits and/or memory devices. More education can supplement for less experience, and vice versa. I exceeded this definition by the priority date of January 17, 2007.

VI. TECHNOLOGY OVERVIEW

28. Below I provide a summary of the technology at issue, which is a two-row charge pump utilizing an analog comparison circuit to provide well biasing.

A. Background

29. An integrated circuit implies that the electrical components comprising a circuit are fabricated on a single piece of silicon, or “chip.” The electrical components may consist of transistors, resistors, capacitors, and inductors. The resistors, capacitors, and inductors are passive components, whereas a transistor is referred to as an active component. A circuit component that delivers power or power gain in an electric circuit or can function as a switch is known as an active component. By contrast, a circuit element that only absorbs power, converts power into heat, and/or stores it in an electric field or magnetic field is known as a passive component.

30. The most common type of transistor used in integrated circuits is the MOSFET (meta-oxide-semiconductor field effect transistor). These transistors are often referred to as MOS devices, and they have three terminals: the source, the drain, and the gate, where the latter (*i.e.*, the gate) controls the degree of conduction between the source and drain. The conduction, if any, takes place in the so-called channel between the source and drain terminals. MOS devices come in two flavors: the NMOS device and the PMOS device. An NMOS device features an N-type

source and drain terminal. The source and drain terminals are fabricated into a so-called substrate, which is a P-type material for an NMOS device. Silicon that has been doped such that it has become an N-type material is characterized by having many free electrons while silicon that has been doped in a manner that has made it into a P-type material is characterized by having many free holes. Holes behave similarly to electrons but are positively charged rather than negatively charged as in the case of electrons.

31. When an NMOS device is turned on by a sufficiently high gate voltage, said to be above the transistor's threshold voltage, the P-type substrate between the source and drain terminals becomes converted to an N-type material at the surface of the substrate near the gate. This portion of the substrate that is converted to an N-type material is called the channel. When a channel is so formed, conduction of current will proceed from the drain to the source if the drain voltage is higher than the source voltage. In an absence of a channel (in which case the NMOS transistor is said to be turned off), only small leakage currents proceed from the drain to the source if the drain voltage is higher than the source voltage. Regardless of the transistor being turned on or off, if the drain voltage equals the source voltage then no current proceeds from the drain to the source.

32. A PMOS device features a P-type source and drain terminal, and an N-type substrate. When a PMOS device is turned on by a sufficiently low gate voltage

(lower than its negative threshold voltage), the N-type substrate between the source and drain terminals becomes converted to a P-type material at the surface of the substrate near the gate. This portion of the substrate that is converted to a P-type near the surface is called the channel. When a channel is so formed, conduction of current will proceed from the source to the drain if the source voltage is higher than the drain voltage. In an absence of a channel (in which case the PMOS transistor is said to be turned off), only small leakage currents proceed from the source to the drain if the source voltage is higher than the drain voltage. Regardless of the transistor being turned on or off, if the source voltage equals the drain voltage, no current proceeds from the source to the drain.

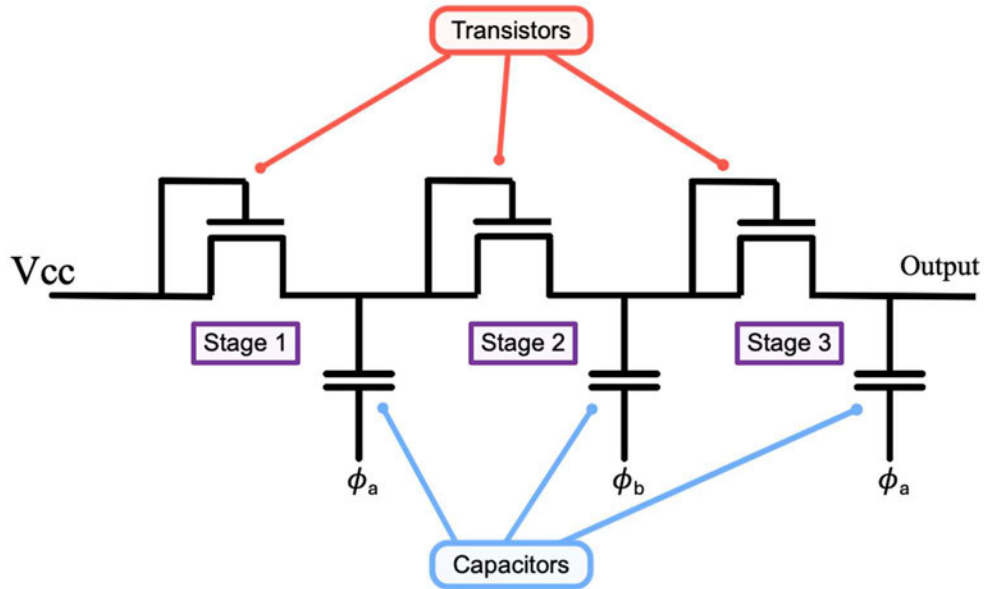
33. Integrated circuits commonly use both NMOS and PMOS devices, and are thus referred to as CMOS integrated circuits, where the letter “C” refers to the use of the complementary devices, that is, the use of both NMOS and PMOS devices. Logic gates that use both NMOS and PMOS devices are referred to as CMOS logic gates. Examples of CMOS logic gates include inverters, switches or transmission gates, NAND gates, and NOR gates. The CMOS logic family is useful for general purpose computing, because it provides very low power consumption.

B. Booster Circuit

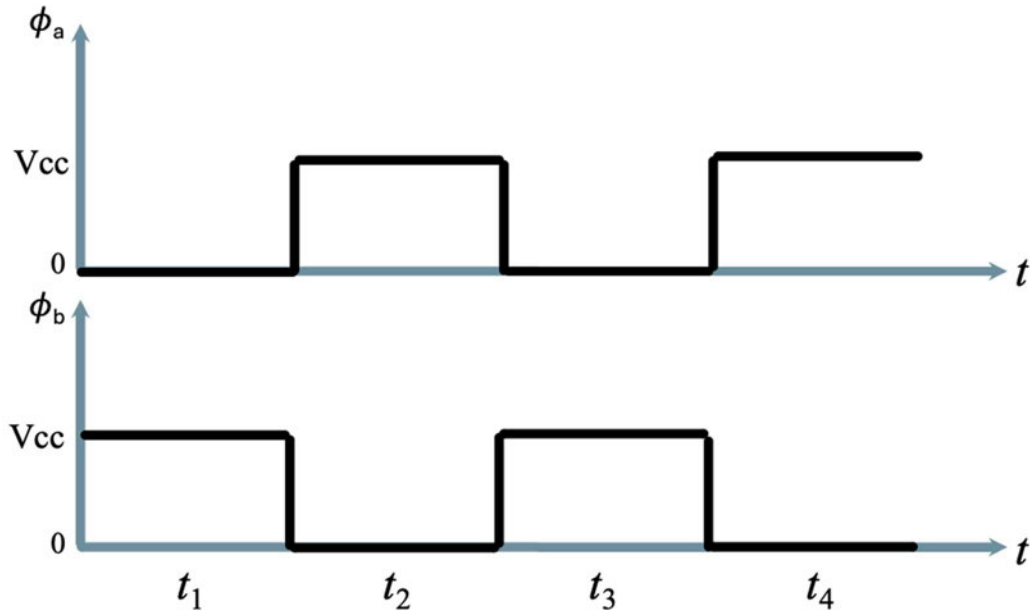
34. Booster circuits (*i.e.*, charge pumps) are circuits that take a supply voltage and increase, or “boost,” the voltage to output a voltage that is higher than

the supply voltage. Long before the critical date of the '557 patent, a booster circuit was a widely used in memory devices such as a flash memory because the higher voltage output of a booster circuit was used for writing and erasing programmable elements. *Id.*

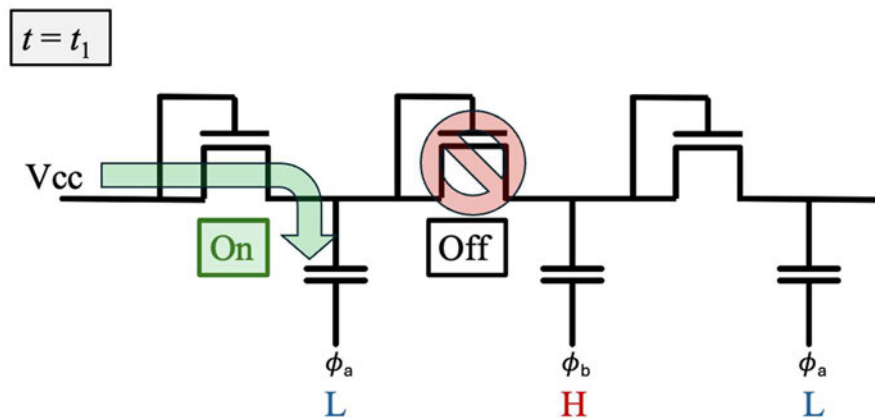
35. A conventional, single row charge pump was first introduced in 1976 by John F. Dickson. EX1011, Fig. 2, 375. The so-called Dickson charge pump circuit is shown in the schematic below. EX1011, Fig. 2. The charge pump shown below is a three-stage charge pump, where each stage comprises a diode-connected transistor (*e.g.*, an NMOS transistor) and a capacitor that is switched. For an NMOS transistor, the drain terminal is at a voltage that is higher than (or equal) to the source terminal voltage. The diode-connected transistors in the figure permit conduction from left to right if the left (drain) terminal of a transistor is at a higher voltage than the right (source) terminal. EX1011, 375. Such transistors, however, prevent current conduction from right to left even if the right (drain) terminal is at a higher voltage than the left (source) terminal since the gate-to-source voltage would be exactly zero due to the connection between gate and source. *Id.*



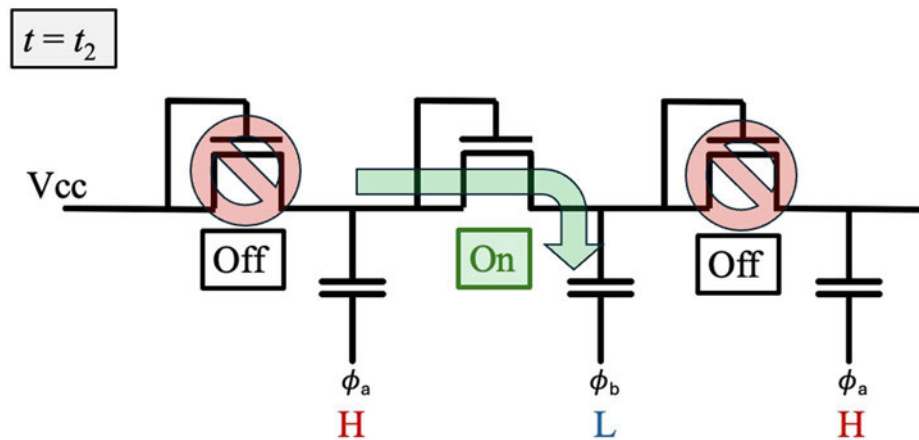
36. The capacitors are driven by two clock signals, ϕ_a and ϕ_b , each of which is characterized as a periodic square-wave where the maximum is the supply voltage (V_{cc}) and the minimum is set to ground (0V). As illustrated below, ϕ_a and ϕ_b are identical except that they are out of phase with one another (*e.g.*, ϕ_b is at a minimum when ϕ_a is at a maximum). At time t_1 , ϕ_a is at a minimum voltage (*i.e.*, “low”) and ϕ_b is at a maximum voltage (*i.e.*, “high”). EX1011, Fig. 3, 375.



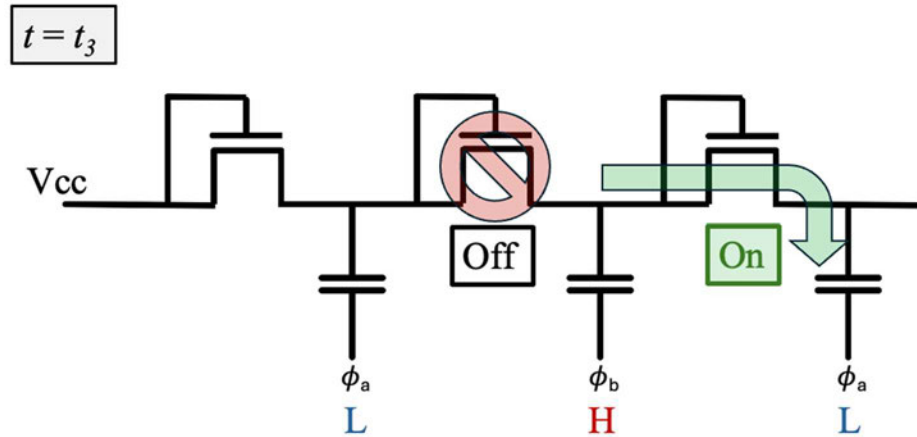
37. When ϕ_a is low, the first stage transistor is turned on since the gate (and drain) voltage (V_{cc}) is greater than the voltage at the source (right terminal) of the first stage transistor due to ϕ_a pulling low. Meanwhile, the second stage transistor is turned off since its gate-to-source voltage is zero due to ϕ_a pulling low and ϕ_b pulling high (making the left terminal of the second stage transistor the source). This allows the first stage capacitor to charge to a voltage of $V_{cc}-V_t$, where V_t is the threshold voltage drop across the transistor.



38. At t_2 , ϕ_a goes high while ϕ_b goes low, resulting in the first stage transistor and third stage transistor turning off and the second stage transistor turning on. The signal ϕ_a going high raises the voltage of the bottom terminal of the first stage capacitor by V_{cc} , in turn causing the voltage at the top terminal of the first stage capacitor to increase by V_{cc} (due to the nature of a capacitor, the voltage across it does not change instantaneously). As a result, the top terminal of the first stage capacitor is thus $2V_{cc}-V_t$, which is subsequently transmitted across the second stage transistor to charge the second stage capacitor to a voltage of $2V_{cc}-2V_t$ (accounting for the threshold voltage drop across the second stage transistor).



39. At t_3 , ϕ_b goes high while ϕ_a goes low, resulting in the second stage transistor turning off and the third stage transistor turning on. As a result, the voltage at the top of the second stage capacitor increases by V_{cc} , thus increasing to $3V_{cc}-2V_t$. This voltage is subsequently transmitted across the third stage transistor to charge the third stage capacitor to a voltage of $3V_{cc}-3V_t$.



40. As a result of the multiple booster stages and the alternating clock signals providing periodic voltage boosts, a booster circuit is capable of taking an input voltage (V_{cc}) and amplifying it to a higher output voltage ($3V_{cc}-3V_t$). EX1011, Fig. 3, 375-76.

C. Deep N-well Layer

41. Before the priority date of the '557 patent, a structure employing multiple layers of different conductivity (*i.e.*, well regions) was commonly used in integrated circuits. EX1009, 32-33. A cross-sectional illustration of a multiple-well structure for NMOS transistors is shown below, and comprises two well regions of different conductivity types: an N-type layer (*i.e.*, a deep N-well) fabricated on a P-type substrate, and a P-type layer (*i.e.*, a P-well) fabricated in the deep N-well. EX1007, Fig. 9; *see also* EX1009, Fig. 15.17.

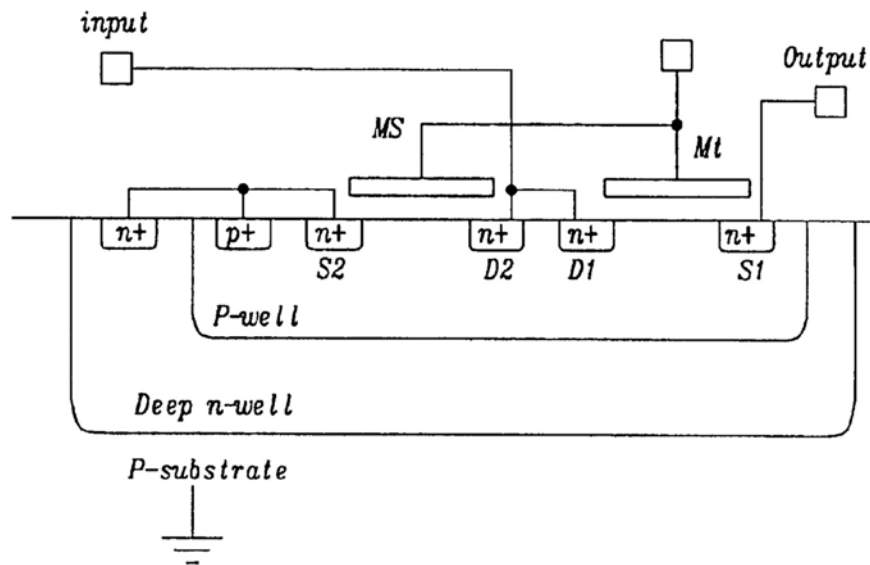


FIG. 9

42. It was well known that the use of multiple wells enabled a reduction of the body effect of a transistor (*i.e.*, reduction of the threshold voltage associated with a transistor by reducing the reverse bias of the body-source PN-junction), since the body of one or more transistors can have their body voltages individually tuned. EX1009, 100, 329, 371-73, 383. This reduction in body effect makes it easier to turn on a transistor and reduces the supply voltages necessary for operating a booster circuit. EX1009, 41. It was also well known that the use of multiple well regions, specifically a deep N-well, improved the isolation of switching elements from the bulk substrate and helped suppress occurrences of latch-up. EX1009, 142.

D. Two-Row Structure of a Booster Circuit

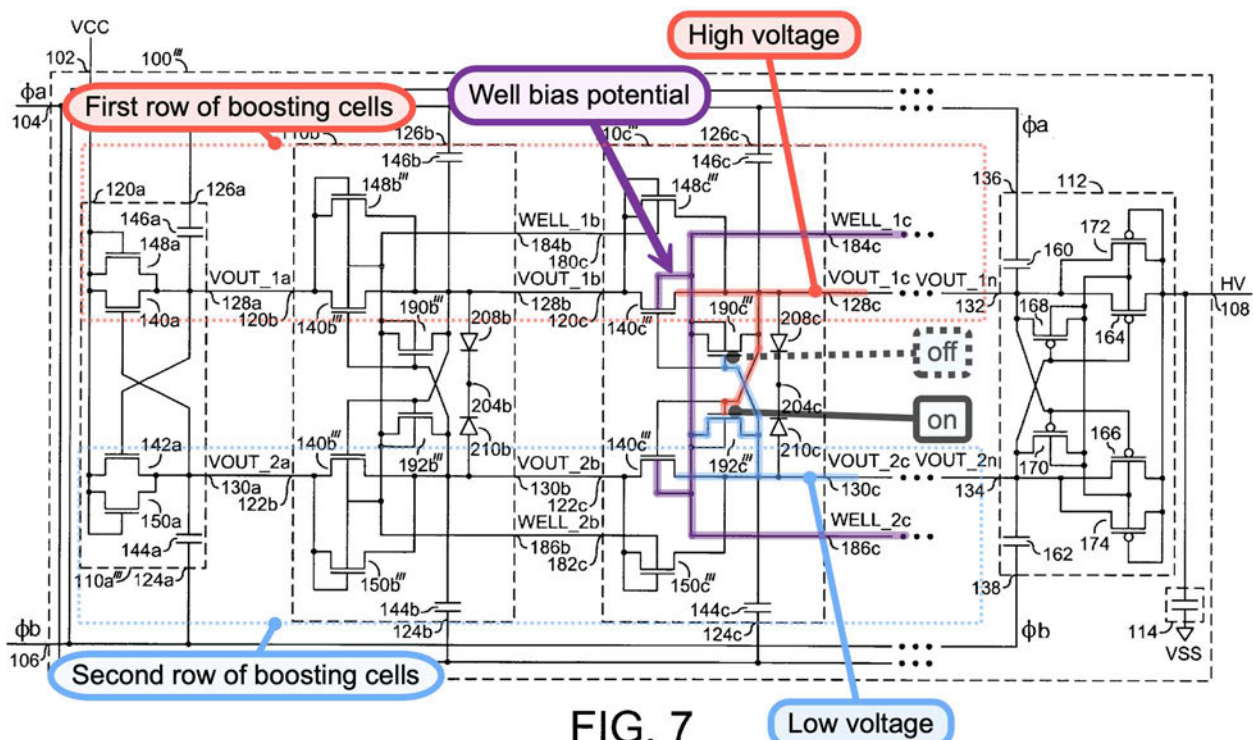
43. It was conventional, before the priority date of the '557 patent, to construct a charge pump circuit using two rows of boosting cells. EX1010, Fig. 3;

44. A two-row structure was known to enable a variety of advantages in the structure and function of booster circuits. For example, two-row structures can



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exploit the complementary clock signals ϕ_a and ϕ_b that are applied to a given boosting stage by using those complementary clock signals to control the switching elements contained in that boosting stage. EX1010, Fig. 3(a), 1102-03. This concept is further demonstrated in Figure 7 of Meng, shown below. EX1006, Fig. 7. The complementary clock signals applied to a given stage are at a **high voltage** for one boosting cell (**first row**) and a **low voltage** for the other boosting cell (**second row**). EX1006, Fig. 7, 3:21-27, 5:26-48. The complementary clock signals affect the voltage at nodes $128i$ and $130i$, which in turn control (*i.e.*, activate) switches $192'''i$ and $190'''i$, respectively. EX1006, 9:9-32. For example, a high voltage present at node $128i$ will turn on $192'''i$ while the corresponding low voltage present at node $130i$ will turn off $190'''i$.



45. Two-row structures exploit the complementary clocks signals to improve the efficiency of a booster circuit. EX1010, Fig. 7, 1104. With a single-row structure, the output of a boosting row is boosted or driven for half of a clock cycle, and that output voltage decays (*i.e.*, leaks away) over the subsequent half cycle. EX1010, 1104. By contrast, for a two-row structure having the final outputs of the two rows tied together, the final output common to both rows is boosted by one of the two rows while the other row is not boosting (and vice versa for the next half of the clock cycle). EX1010, Figs. 4, 8, 1104. Thus the final output of a two-row structure is being boosted over both halves of the clock cycle, helping prevent decay of the output voltage that would otherwise occur for half the clock cycle in a single-row structure. *See also* EX1005, 6:27-32; EX1010, Figs. 3(b), 4, 8, 1103-04. Moreover, the final output of a two-row structure is boosted twice as often over the same clock period, thereby enhancing the overall efficiency of the booster circuit. EX1010, Fig. 8, 1104-06.

46. Another benefit of the two-row structure is the reduction in the body effect (*i.e.*, the increase in the threshold voltage caused by an increase in the reverse bias from transistor source to body). A two-row structure minimizes the body effect by bootstrapping the well bias potential across the boosting stages. EX1010, 1102-03; EX1009, Fig. 15.20, 378. Both the low-side and high-side voltages present on the boosting cell rows increase with each successive boosting cell stage. EX1010,

Fig. 3(b). By adjusting the well bias potential to reflect the increased voltages of both rows (*e.g.*, setting the well bias potential to be the low-side voltage present at each boosting cell stage instead of leaving the body at a fixed voltage such as ground), one obtains two well-known benefits of two-row structures: prevention of forward biasing at drain-source junctions, and a reduction of the body effect at each boosting cell stage. EX1010, 1102-03; EX1009, 378.

E. Comparison Circuits

47. A comparison circuit is a circuit that receives two inputs and produces an output in response to a comparison of those two inputs, *e.g.*, an output corresponding to which input is higher. Example comparison circuits include a pair of cross-coupled transistors, or a pair of diodes with their outputs tied together. EX1006, Fig. 7, 8:16-22; EX1009, Fig. 15.20, 378. In both of these cases, the circuits take two inputs and produce an output depending on which input is higher or lower. EX1006, Fig. 8. Such comparison circuits can be utilized to apply a consistent and appropriate well bias potential to the well region(s) underlying a booster circuit. *Id.* An example of a comparison circuit being used to select and output a well bias potential based on a comparison of two voltage inputs was presented in §VI.D above, where elements 190^{'''}*i* and 192^{'''}*i* (*i.e.*, a pair of cross-coupled transistors) together form a comparison circuit. §VI.D, *supra*; EX1006, Fig. 7.

VII. THE '557 PATENT

48. Having read many patents, I am of the opinion that the '557 patent does not claim anything that might be considered new. As discussed below, the claims of the '557 patent cover well-known building blocks of voltage supply circuitry for memory devices, such as booster circuits.

A. The Challenged Claims

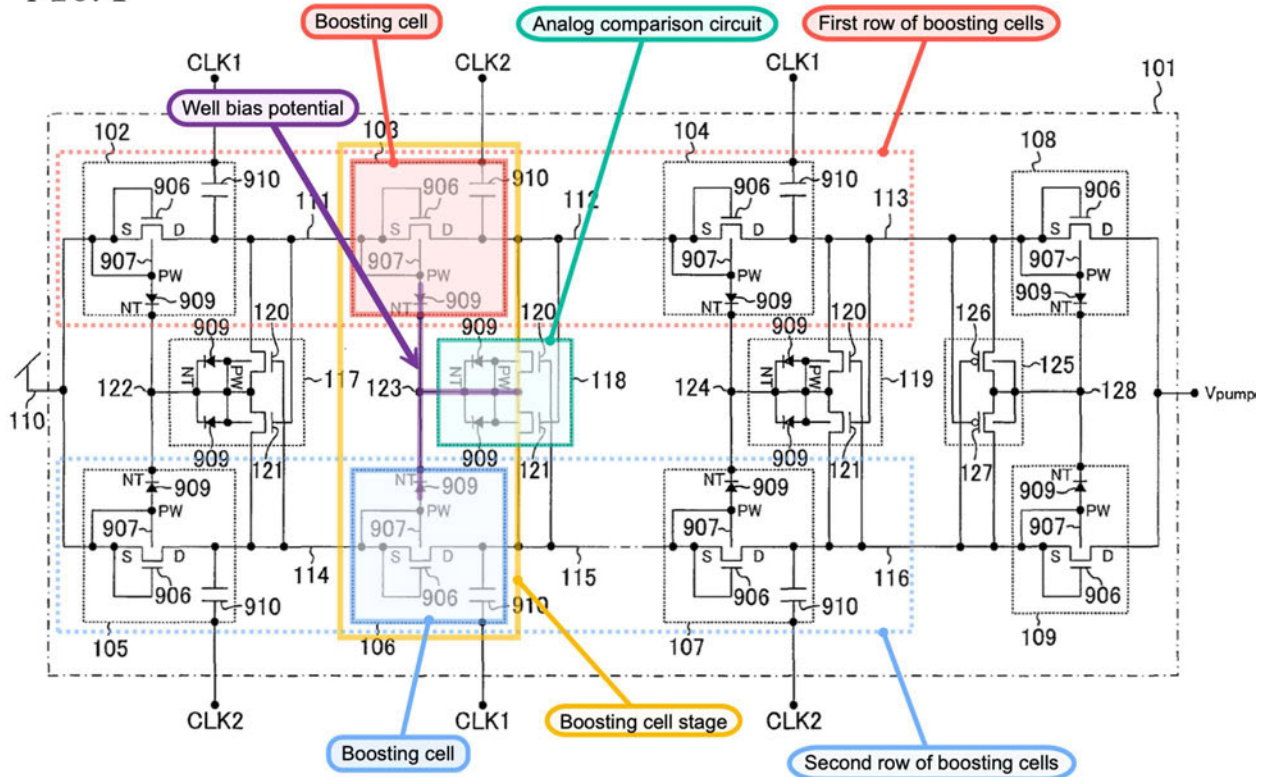
49. I understand that claims 1-12 and 14 of the '557 patent are being challenged by SK hynix (the "Challenged Claims") and I have been asked to opine on them specifically. I reserve the right to opine on other claims of the '557 patent if I am asked to do so. A table listing the claim limitations of the Challenged Claims is provided in the preamble of the Petition.

B. Overview

50. U.S. Pat. No. 7,777,557 is directed to a two-row booster circuit comprising at least one boosting cell stage and an analog comparison circuit that outputs a well bias potential that is applied to a deep N-well. EX1001, Abstract. Each boosting cell utilizes a switching element and a capacitor to transmit and store a charge as part of the voltage amplification process. EX1001, Fig. 1, 1:21-41, 7:47-54. The boosting cells further utilize a deep N-well for the switching elements. EX1001, 1:30-41, Fig. 1. An analog comparison circuit is used to compare the output voltages between the boosting cell on the first and the second row. EX1001, 7:54-8:11, 8:19-42. The analog comparison circuit is designed to output either the

higher or the lower of the two voltages to the deep N-well of the boosting cells. *Id.* Annotations to Figure 1 of the '557 patent, shown below, highlight the aforementioned elements. EX1001, Fig. 1.

FIG. 1



51. The '557 patent does not purport to have invented a two-row booster circuit utilizing an analog comparison circuit, which was widely-used in the field of memory devices long before the January 17, 2007 priority date, as I explain above in §VI.

C. Prosecution History

52. The '557 patent was filed on January 17, 2008, and claimed foreign application priority to Japanese application 2007-007694, which was filed on January 17, 2007. EX1002, 1-2, 60-61, 65-66.

53. The Examiner's initial rejection relied on Meng as anticipating claims 1-4, 8, 9, and 11-14. *Id.*, 179. The Examiner relied upon Meng's disclosure of a first and second boosting cell row, multiple stages of boosting cells comprising switching elements, each switching element having two well regions on a substrate, analog comparison circuits, and backflow preventing circuits in its initial rejection. *Id.*, 179-80. The Examiner also noted how U.S. Patent No. 6,952,129, which was included in the applicant's information disclosure statement, "shows similar circuit structures that similarly anticipate the claims." *Id.*, 180.

54. In response, the Applicant argued that Meng "fails to teach that the well potential of the analog comparison circuit is applied to the deep-n well corresponding to the first well region of the instant application." *Id.*, 191-92. Instead, Applicant noted that "Meng merely shows that its analog comparison circuit applies a well potential to a p-well corresponding to the second well region of the instant application." *Id.*

55. Following this argument, the Examiner issued a Notice of Allowance, stating that "Applicant's arguments are persuasive," effectively agreeing with the

Applicant that the prior art, namely Meng, did not disclose the application of a well bias potential to the deep N-well (*i.e.*, first well region) by an analog comparison circuit. *Id.*, 200.

56. As I discuss below, however, the Examiner was incorrect that Meng does not disclose the application of a well bias potential to the deep N-well by an analog comparison circuit. Meng does, in fact, disclose the application of a well bias potential to the deep N-well. Meng discloses two analog comparison circuits and the Examiner failed to properly identify the analog comparison circuit that indeed does apply a well bias potential to the deep N-well. Moreover, Fukushima and Park also disclose the application of a well bias potential to the deep N-well by an analog comparison circuit, as I discuss below.

VIII. CLAIM CONSTRUCTION

57. I have been informed that patent claim terms should be understood in accordance with their plain and ordinary meaning to a POSITA. In my opinion, it is not necessary to construe any of the claim terms of the '557 patent in order to determine that the Challenged Claims are invalid. To the extent relevant, I have applied the plain meaning of certain terms in my analysis of Grounds 1 through 3 below.

IX. GROUND 1: FUKUSHIMA ANTICIPATES CLAIMS 1, 3, 5, 10-12, AND 14

A. Overview of Fukushima

58. U.S. Patent No. 6,107,864 (“Fukushima”) was published on August 22, 2000, before the January 17, 2007 priority date of the ’557 patent. Fukushima qualifies as prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e) because it was patented on August 22, 2000, and thus before the January 17, 2007 priority date of the ’557 patent. I further understand that Fukushima was not considered by the Examiner during prosecution of the ’557 patent.

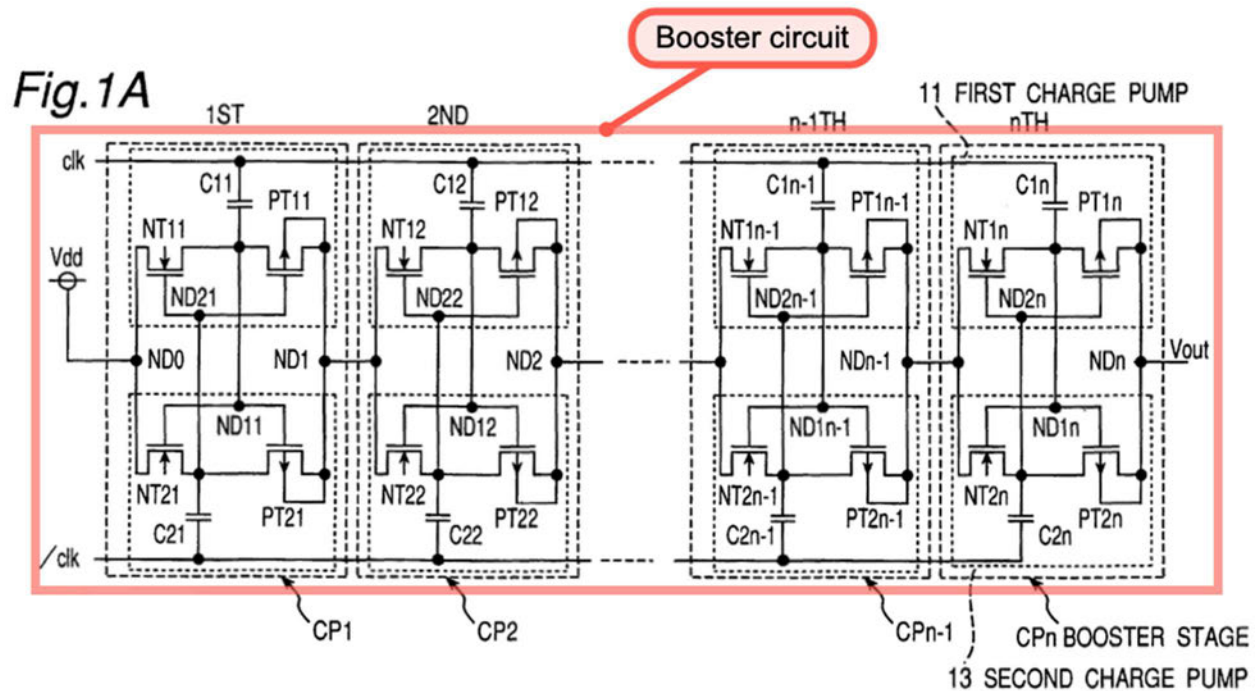
59. In my opinion, Fukushima teaches a two-row booster circuit comprising multiple boosting cell stages. EX1005, Fig. 1A, 4:49-5:3. Fukushima further teaches a comparison circuit for each boosting cell stage designed to compare the output voltages of the two rows and to output one of those two voltages as a well bias potential. EX1005, Fig. 1A, 5:58-6:26. The booster circuit described by Fukushima has a multiple-well structure comprising a P-well in a deep N-well with the deep N-well positioned on a P-type substrate. EX1005, Figs. 3A-3B, 7:16-32. The well bias potential outputted by the analog comparison circuit and applied to the deep N-well helps prevent the occurrence of forward biasing and helps minimize the substrate bias effect on NMOS transistors. EX1005, 5:35-42, 7:28-38. Fukushima also teaches, in my opinion, the sharing of a deep N-well by multiple switching elements and multiple boosting cell stages. EX1005, Figs. 3A-3B, 7:39-47.

60. In my opinion, Fukushima discloses claims 1, 3, 5, 10-12, and 14 of the '557 patent at least under Patent Owner's apparent interpretation of the claim limitations. In particular, I understand that in the infringement contentions, Patent Owner identified circuit elements having a common well region as being circuit elements that also have the same potential of the common well region. As I explain below, under this interpretation, it is my opinion that Fukushima anticipates the foregoing claims of the '557 patent.

B. Claim 1

1. 1[pre]: A booster circuit comprising:

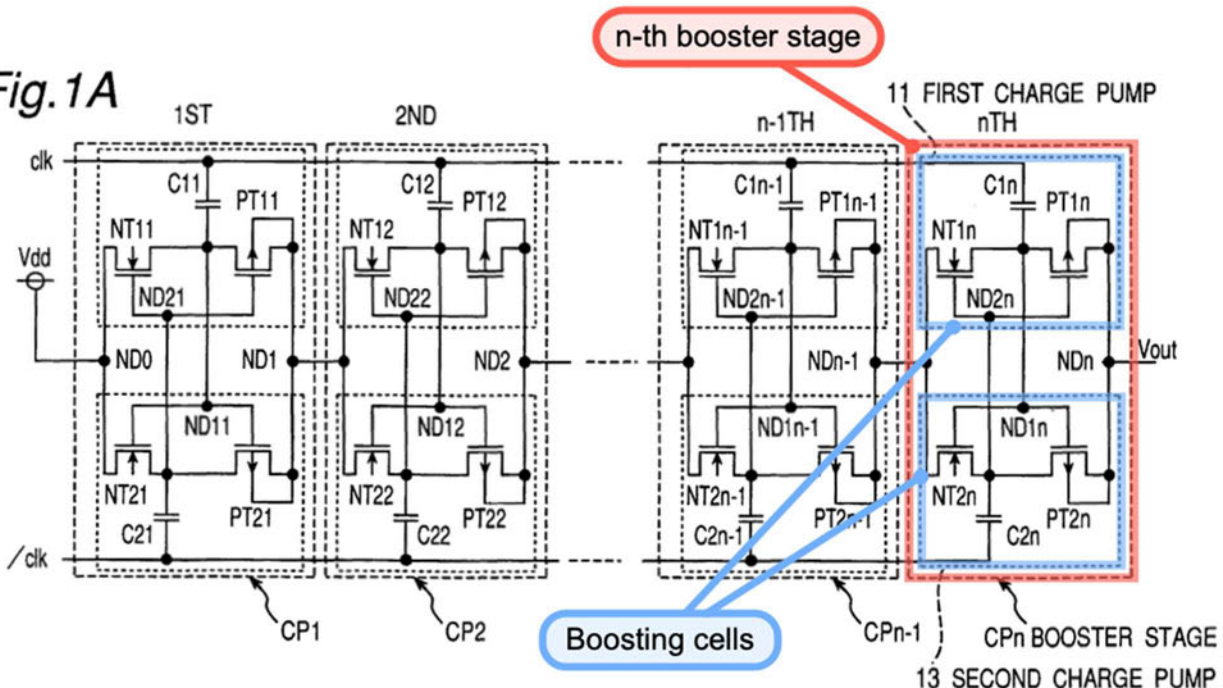
61. If the preamble is deemed to be limiting, it is my opinion that Fukushima discloses a booster circuit. EX1005, Fig. 1A; *id.*, 4:47-49 ("FIG. 1A is a circuit diagram of a charge pump circuit according to a first preferred embodiment of the present invention."). A "charge pump circuit," which receives a supply voltage and outputs a voltage that has been charged to a level higher than the supply voltage, is a "booster circuit." *See* §VI.A above.



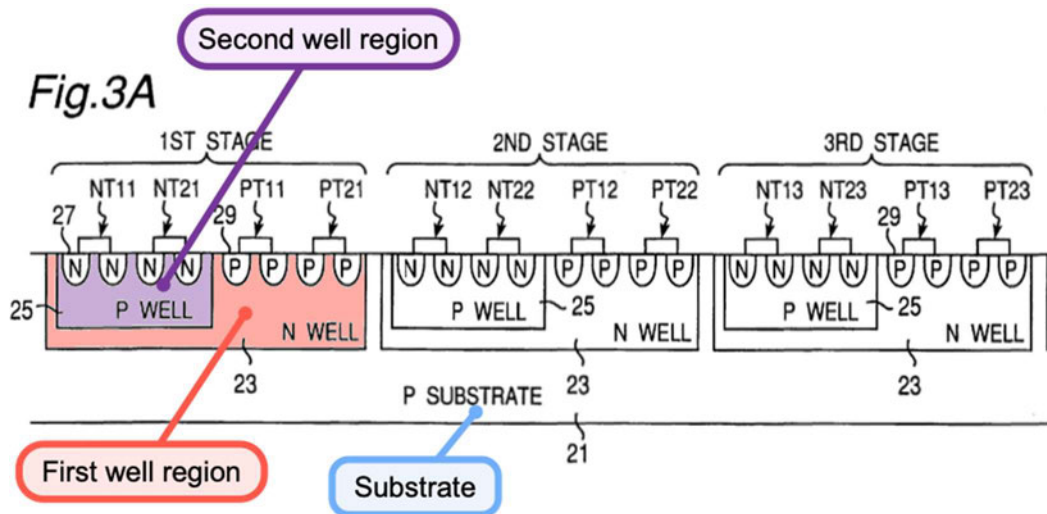
2. 1[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region,

62. In my opinion, Fukushima meets claim limitation 1[a]. Fukushima discloses a “charge pump circuit compris[ing] a plurality of booster stages CP1 to CPn connected in series” with each “[b]ooster stage CP_n further compris[ing] first and second pumps 11 and 13.” EX1005, 4:49-51, 4:66-67; *see also id.*, Fig. 1A. Charge pumps 11 and 13 are *boosting cells* capable of “*raising the potential* of the node ND_n by transferring a charge input from the node ND_n- [sic] to the node ND_n.” *Id.*, 4:67-5:2.

Fig. 1A

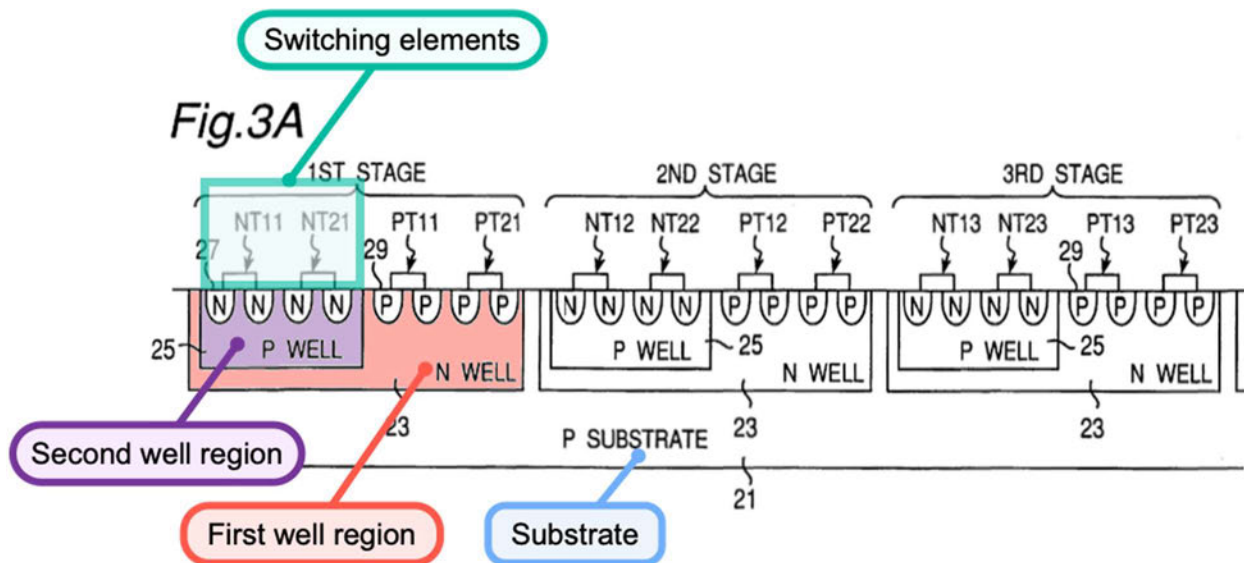


63. Fukushima also discloses in my view that each boosting cell has “a first-conductivity type first well region on a substrate” and “a second-conductivity type second well region in the first well region.” Specifically, Fukushima discloses that an “N well 23 in [a] P substrate 21 is formed separately in every booster stage,” which corresponds to a first well region on a substrate, and “a P well 25 is formed within N well 23,” which corresponds to a second well region in the first well region. EX1005, 7:21-27. Figure 3A shown below illustrates, in my opinion, the placement of the first and second well regions with respect to the substrate for the booster stages. EX1005, Figs. 3A-3B.



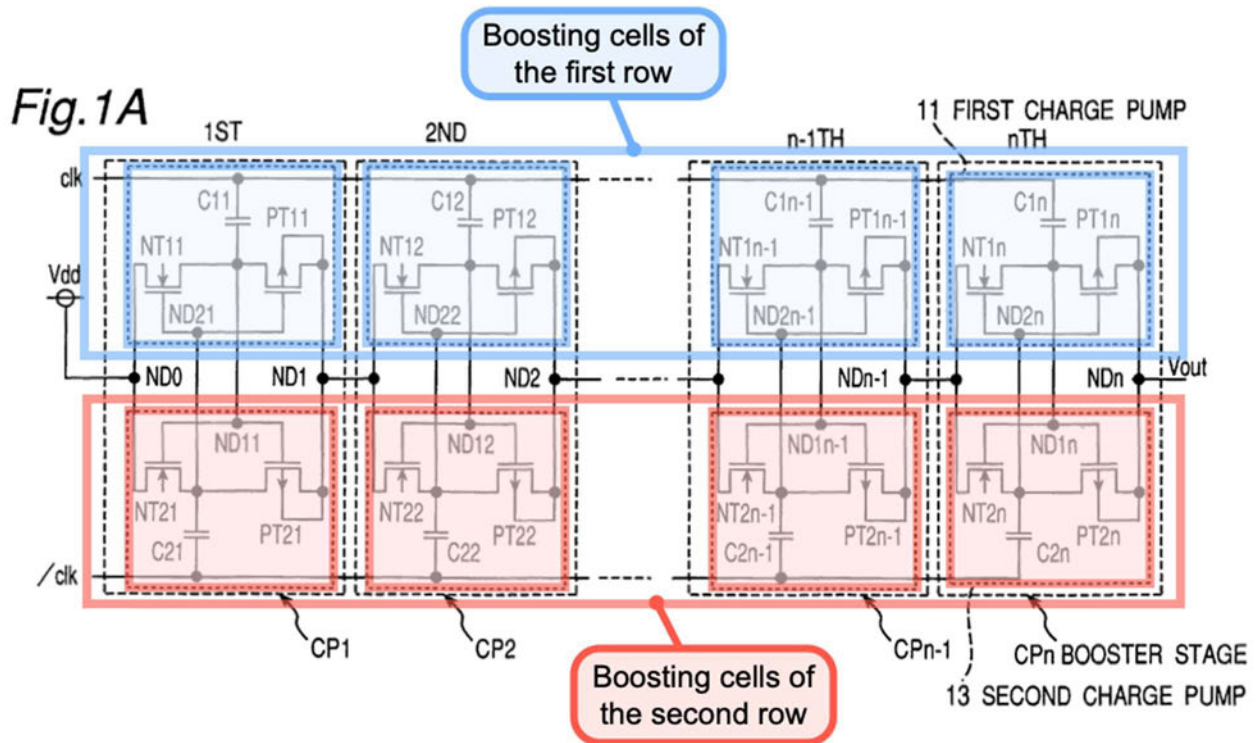
3. 1[b]: and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal;

64. In my opinion, Fukushima meets claim limitation 1[b]. Fukushima discloses a “switching element” (e.g., NMOS transistors NT1 n and NT2 n) in the first and second well regions that, as discussed above in 1[a], transfers charges from a first terminal (ND n -1) to a second terminal (ND n). EX1005, 4:67-5:2. Figure 3A, shown below, in my view illustrates how the switching element is in both the P-well (“the second well region”) and the deep N-well (“the first well region”). EX1005, Fig. 3A.



4. 1[c]: a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; a second boosting cell row including M stages ($M \geq 1$) of the boosting cells; and

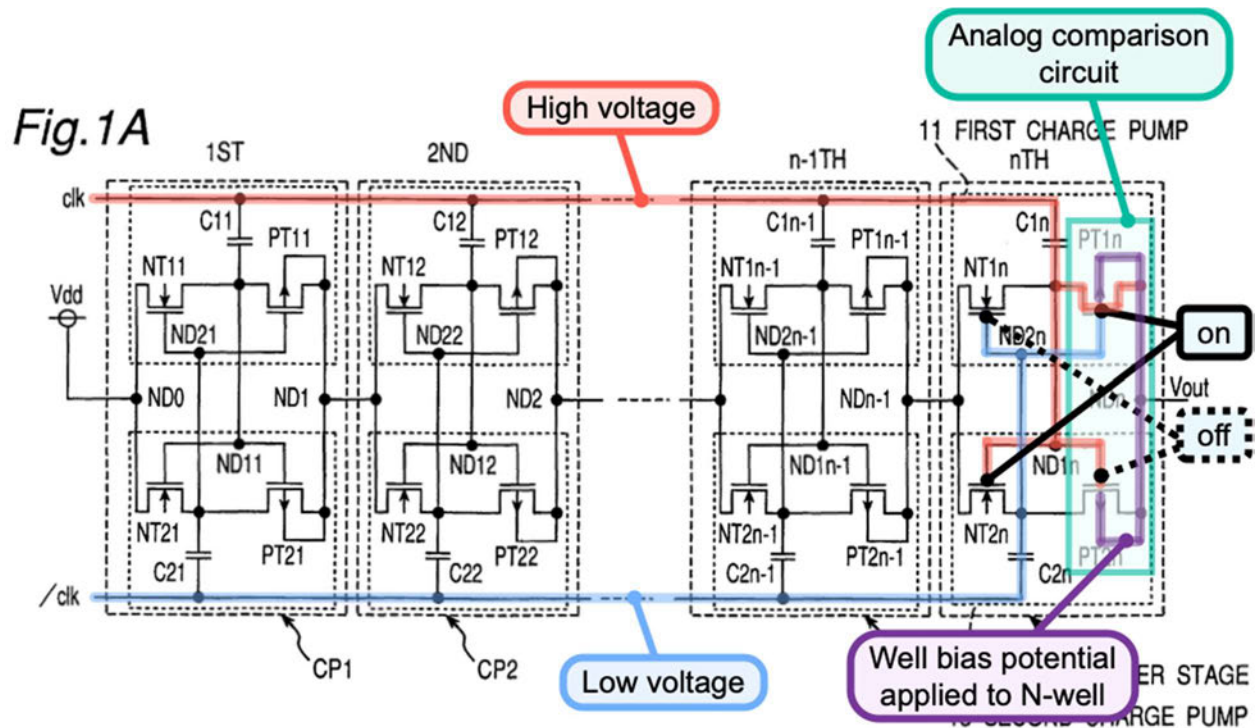
65. In my opinion, Fukushima meets claim limitation 1[c]. Fukushima's booster circuit "comprises a plurality of *booster stages* CP1 to CPn connected in series," where "[e]ach of the booster stages is identically configured." EX1005, 4:50-55. Each booster stage includes two charge pumps ("boosting cells"), such as charge pumps 11 and 13. EX1005, Fig. 1A, 4:66-67. The top charge pumps in the n booster stages are in my opinion "a *first boosting cell row* including N stages ($N \geq 1$) of the boosting cells;" and the bottom charge pumps in the n booster stages are "a *second boosting cell row* including M stages ($M \geq 1$) of the boosting cells."



5. 1[d]: at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row,

66. In my opinion, Fukushima meets claim limitation 1[d]. The booster stages disclosed in Fukushima each comprise a collection of transistors that constitute an *analog comparison circuit*. An n -th booster stage, for example, has two NMOS transistors, NT1 n and NT2 n , and two PMOS transistors, PT1 n and PT2 n . EX1005, Fig. 1A. Depending on the phase of the clock cycle (e.g., clk is high and /clk is low), “NMOS transistor NT2 n and PMOS transistor PT1 n go on, and PMOS transistor PT2 n and NMOS transistor NT1 n go off,” in which case an electric charge (i.e., *well bias potential*) is supplied (i.e., *generated*) by PT1 n to its N-well as well

as to the N-well of PT2 n , as shown by the purple trace in the annotated version of Figure 1A. EX1005, 5:58-64, Fig. 1A.



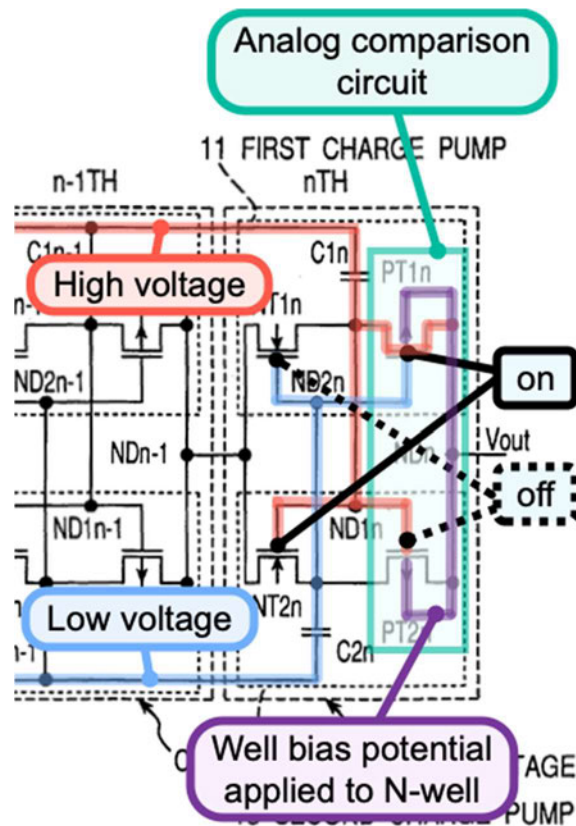
67. In my opinion, the PMOS transistors in each booster stage, identified by the green box, form an “analog comparison circuit” because they operate by comparing the analog voltage levels at nodes ND1 n and ND2 n (i.e., the **output potentials** of the n -th stage of the first and second boosting cell rows, respectively). EX1005, 5:58-64, 6:9-15. Whichever of the nodes ND1 n or ND2 n has the lower voltage determines which row generates the well bias potential that is applied to the well regions associated with the n -th booster stage.

68. Lastly, in my view, the aforementioned n -th stage is the “ i -th stage $1 \leq i \leq N$ ” and “ i -th stage $1 \leq i \leq M$ ” because n is greater than or equal to 1 and less

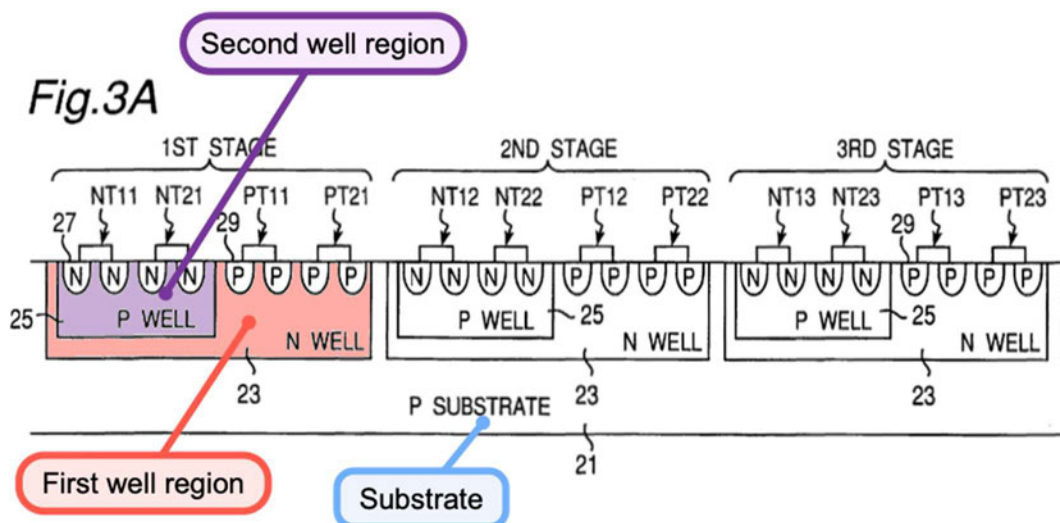
than or equal to N and M , *i.e.*, the number of booster stages in the first and second boosting cell rows, respectively.

6. **1[e]: wherein the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.**

69. In my opinion, Fukushima meets claim limitation 1[e]. As I discussed in connection with claim limitation 1[d], Fukushima teaches the well bias potential outputted by the PMOS transistors PT1 n and PT2 n (“the analog comparison circuit”) is applied to the N-well of the PMOS transistors PT1 n and PT2 n in the n -th booster stage. *See* §IX.B.5 above. In my opinion, the application of the well bias potential to the N-well of PT1 n and PT2 n is shown in the excerpted version of Figure 1A below. EX1005, Fig. 1A. Specifically, as depicted by the **purple** line below in Figure 1A, the well bias potential is applied to the N-well by virtue of the direct connection between the source and the body of the PMOS transistors PT1 n and PT2 n , and the fact that PMOS transistors (*i.e.*, PT1 n and PT2 n) sit in N-type well regions (*i.e.*, the body is an N-well). EX1005, Fig. 1A.



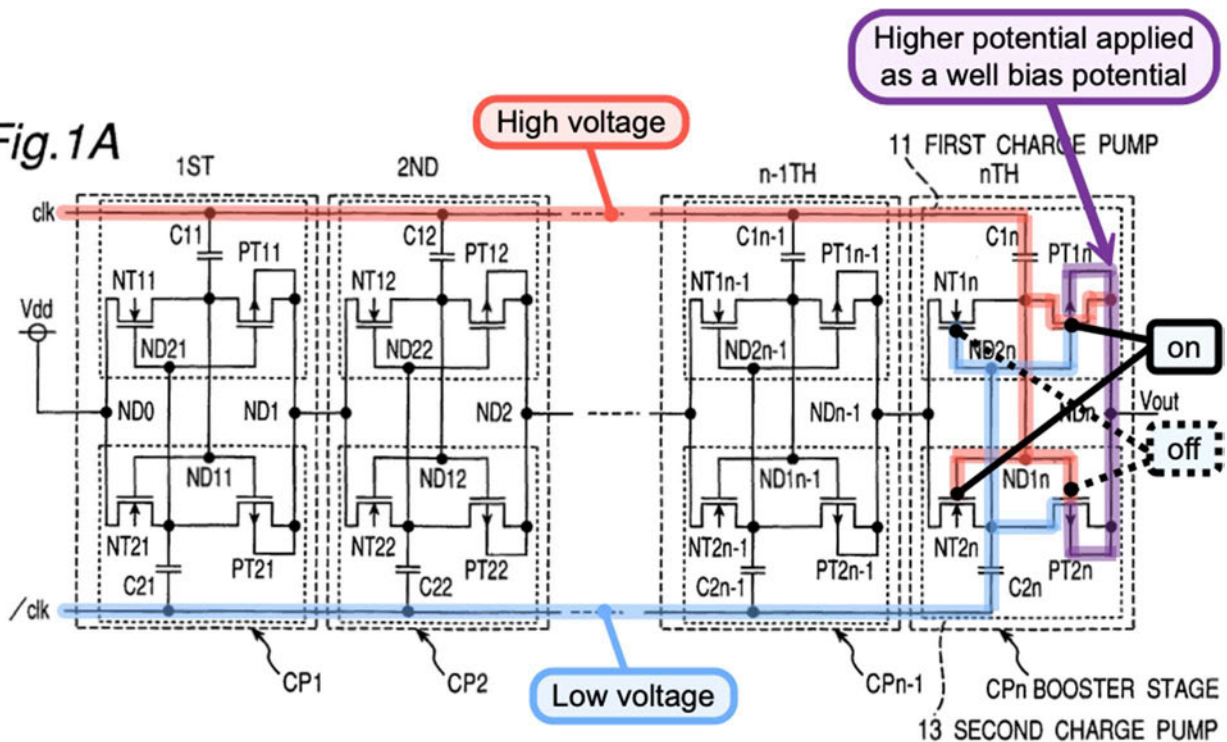
70. As shown below in Figure 3A, the N-well region in which PT1 n and PT2 n sit is also a deep N-well region (*i.e.*, first well region) encompassing a P-well (*i.e.*, second well region) that itself encompasses NMOS transistors of the first and second boosting cell rows (*i.e.*, NT1 n and NT2 n). EX1005, Fig. 3A. Therefore, the well bias potential outputted by the analog comparison circuit (*i.e.*, PT1 n and PT2 n) is, in my opinion, applied to a deep N-well (*i.e.*, first well region) of the switching element included in the at least one boosting cell of the first and second boosting cell rows (*i.e.*, NT1 n and NT2 n).



- C. **Claim 3:** The booster circuit of claim 1, wherein the well bias potential is the higher potential out of the output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

71. In my opinion, Fukushima discloses claim 3. As I discussed in connection with claim limitation 1[d], the PMOS transistors PT1 n and PT2 n (*i.e.*, the “analog comparison circuit”) compare the potential at nodes ND1 n and ND2 n (*i.e.*, the **output potentials** of the n -th stage of the first and second boosting cell rows, respectively), as shown below in Figure 1A. EX1005, Fig. 1A; §IX.B.5, *supra*. Whichever of the nodes ND1 n or ND2 n has the lower potential will cause the PMOS transistor on the opposite row to switch on and transmit that row’s **higher** potential. That higher potential is, as I discussed in connection with claim limitation 1[e], applied as a well bias potential to the N-well of the n -th booster stage, as shown below in Figure 1A. EX1005, Fig. 1A; §IX.B.6, *supra*.

Fig. 1A



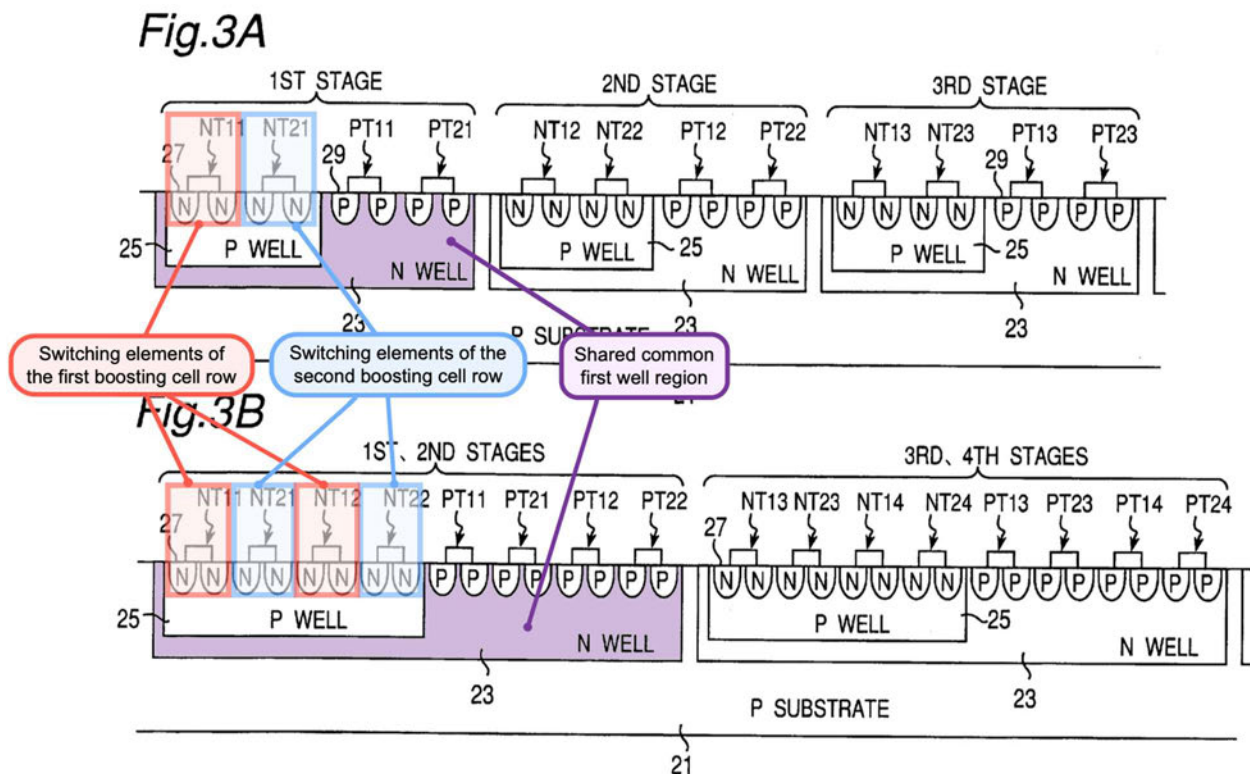
- D. **Claim 5:** The booster circuit of claim 1, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.

72. In my opinion, Fukushima discloses claim 5. Fukushima discloses, in my opinion, a connection between the P-well (*i.e.*, second well region) and the first terminal of a switching element such that both share the same potential. EX1005, 7:28-32 (“By thus forming *P well* 25 [*i.e.*, *second well region*] for an NMOS transistor in the N well 23, and separating the P well 25 from the P substrate 21, the *source of an NMOS transistor* [*i.e.*, *first terminal*] formed in the P well 25 *has the same potential as the P well* 25[.]”).

- E. **Claim 10:** The booster circuit of claim 1, wherein the at least one switching elements having the same potential of the first well region

of the first and second boosting cell rows share a common first well region.

73. In my opinion, Fukushima discloses claim 10. The NMOS transistors NT1 n and NT2 n serve as the switching elements of the first and second boosting cell rows, respectively. EX1005, Fig. 1A. As shown below in Figure 3A, the switching elements NT1 n and NT2 n share a common N-well (*i.e.*, first well region). EX1005, Fig. 3A.



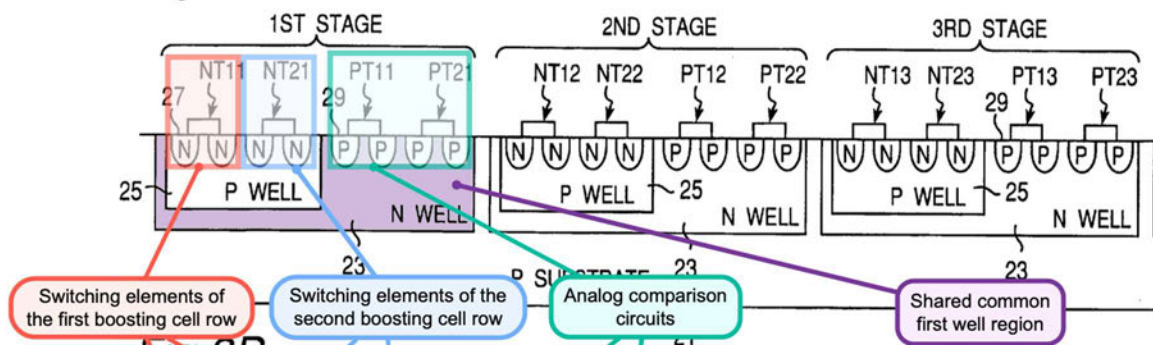
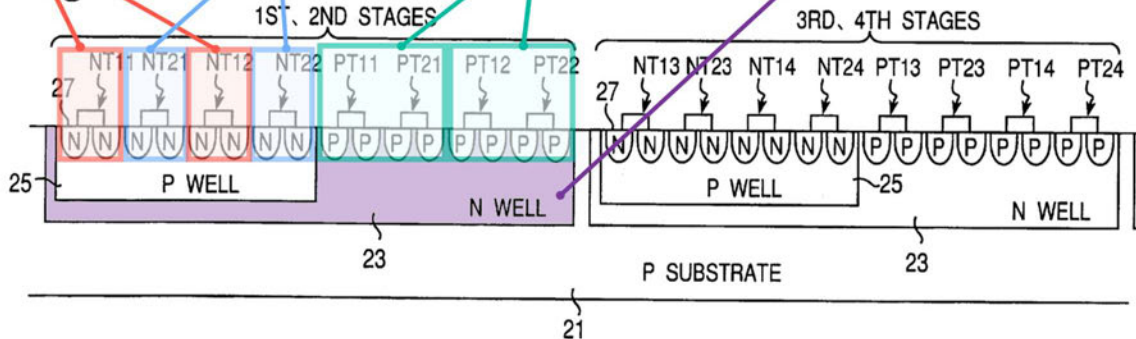
74. Moreover, identifying the NMOS transistors NT1 n and NT2 n as “having the same potential of the first well region” is consistent with how the Patent Owner interpreted claim 10. In particular, I understand that in the infringement contentions in the related district court litigation, the Patent Owner mapped the

claimed “switching elements having the same potential of the first well region” to the switching elements of the first and the second boosting cell rows having a common first well region (N-type).

75. Accordingly, based on at least the Patent Owner’s apparent interpretation, it is my opinion that Fukushima discloses at least one switching elements having the same potential of the first well region.

F. Claim 11: The booster circuit of claim 1, wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region.

76. In my opinion, Fukushima discloses claim 11. The NMOS transistors NT1 n and NT2 n serve as the switching elements of the first and second boosting cell rows, respectively, and, as discussed in 1[d], the PMOS transistors PT1 n and PT2 n form an analog comparison circuit for the n -th stage. EX1005, Fig. 1A; §IX.B.5, *supra*. As shown below in Figure 3A, the switching element(s) NT1 n and NT2 n and the analog comparison circuit(s) PT1 n and PT2 n all share a common N-well (*i.e.*, first well region). EX1005, Fig. 3A.

Fig.3A**Fig.3B**

77. Moreover, identifying the switching elements NT1 n and NT2 n and analog comparison circuit PT1 n and PT2 n as “having the same potential of the first well region” is consistent with how the Patent Owner interpreted claim 11. In particular, I understand that in the infringement contentions in the related district court litigation, the Patent Owner mapped the claimed “switching elements having the same potential of the first well region of the first and second boosting cell rows” to [REDACTED]

[REDACTED] EX1008 at 44.

78. Accordingly, based on at least the Patent Owner’s apparent interpretation, it is my opinion that Fukushima discloses at least one switching

elements and at least one analog comparison circuit having the same potential of the first well region.

G. Claim 12

1. 12[pre]:The booster circuit of claim 1, wherein

79. In my opinion, Fukushima discloses 12[pre] as I discussed in connection with claim 1. *See* §IX.B above.

2. 12[a]: the at least one switching circuit of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

80. As I discussed in claim 11, it is my opinion that Fukushima discloses a switching circuit of an n -th booster stage of the first boosting cell row (*i.e.*, NMOS transistor NT1 n) sharing a common first well region (*i.e.*, N-well) with an analog comparison circuit (*i.e.*, PMOS transistors PT1 n and PT2 n). *See* §IX.F above. PMOS transistor PT1 n is the first element of the analog comparison circuit. EX1005, Fig. 1A.

Fig.3A

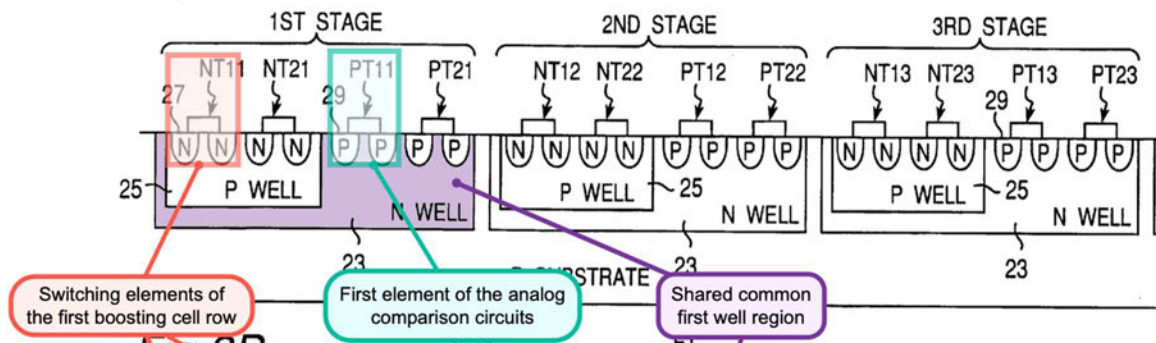
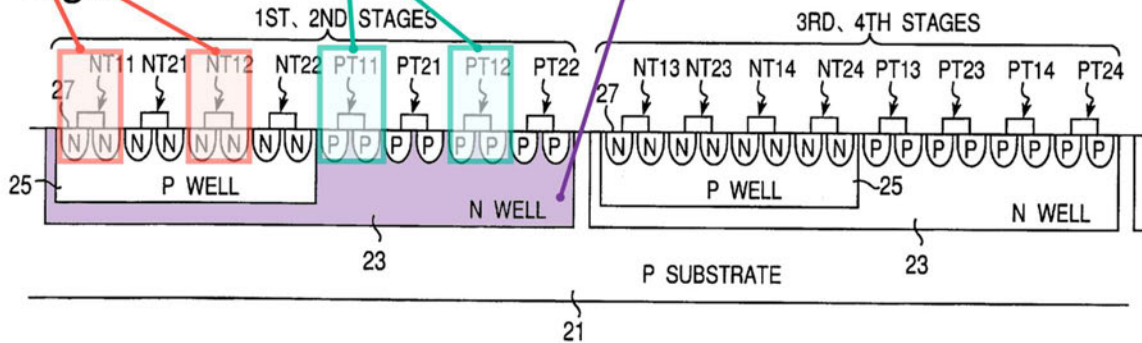
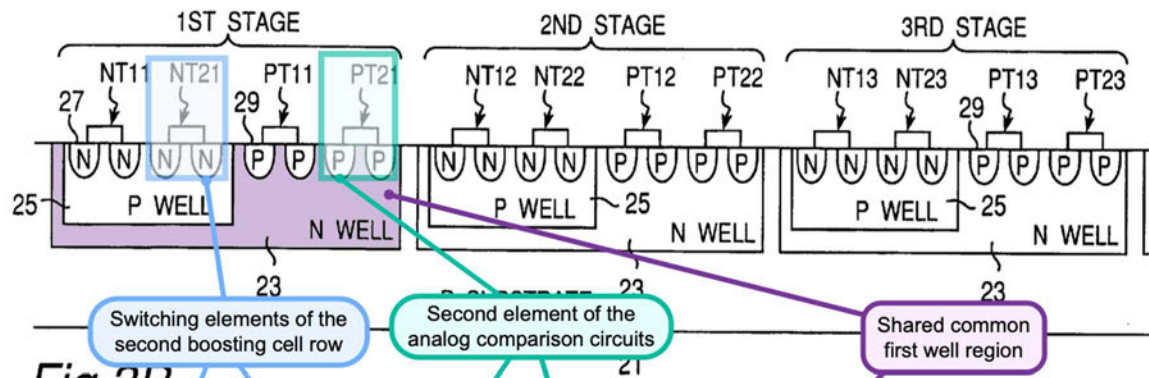
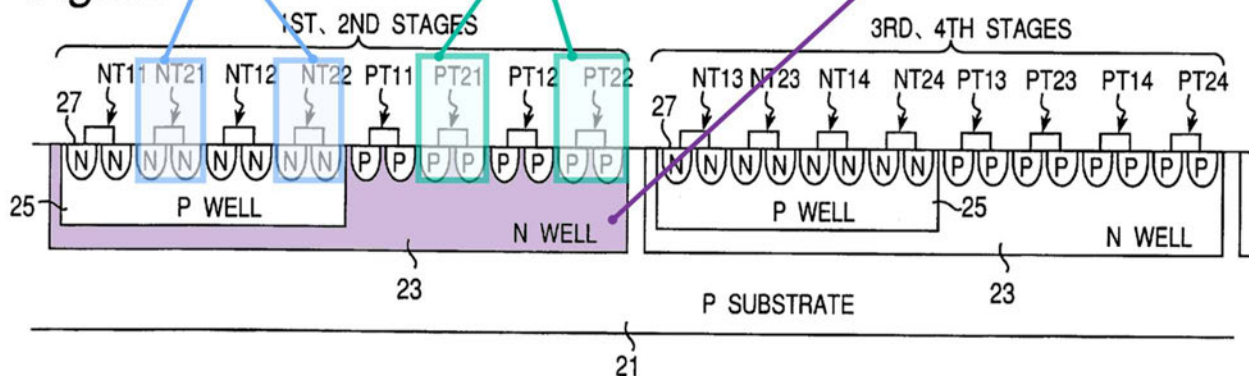


Fig.3B



3. 12[b]: the at least one switching circuit of the boosting cell on the i -th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

81. As I discussed in claim 11, it is my opinion that Fukushima discloses a switching circuit of an n -th booster stage of the second boosting cell row (*i.e.*, NMOS transistor NT2 n) sharing a common first well region (*i.e.*, N-well) with an analog comparison circuit (*i.e.*, PMOS transistors PT1 n and PT2 n). See §IX.F above. PMOS transistor PT2 n is the second element of the analog comparison circuit. EX1005, Fig. 1A.

Fig.3A**Fig.3B**

H. Claim 14

1. 14[pre]: A booster circuit comprising:

82. In my opinion, Fukushima discloses 14[pre] as I discussed in connection with 1[pre]. See §IX.B.1 above.

2. 14[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

83. As I discussed in connection with claim limitations 1[a] and 1[b], it is my opinion that Fukushima discloses boosting cells having a first-conductivity type first well region (*i.e.*, a deep N-well) on a P-type substrate, a second-conductivity

type second well region (*i.e.*, a P-well) in the deep N-well, and at least one switching element (*i.e.*, NMOS transistors NT1 n and NT2 n of an n -th booster stage) in either or both of the deep N-well and the P-well. *See* §IX.B.2 and §IX.B.3 above.

3. **14[b]: wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;**

84. In my opinion, Fukushima discloses claim limitation 14[b]. As I discussed in connection with claim limitation 1[d], it is my opinion that the switching elements NT1 n and NT2 n and the switching elements of the analog comparison circuit PT1 n and PT2 n periodically switch on and off to transfer and block charges from a node on the left (*i.e.*, the first terminal) to a node on the right (*i.e.*, the second terminal). *See* §IX.B.5 above.

4. **14[c]: a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;**

85. In my opinion, Fukushima discloses 14[c] as I discussed in connection with claim limitation 1[c]. *See* §IX.B.4 above.

5. **14[d]: wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first**

boosting cell row and an output potential of the boosting cells of the second boosting cell row.

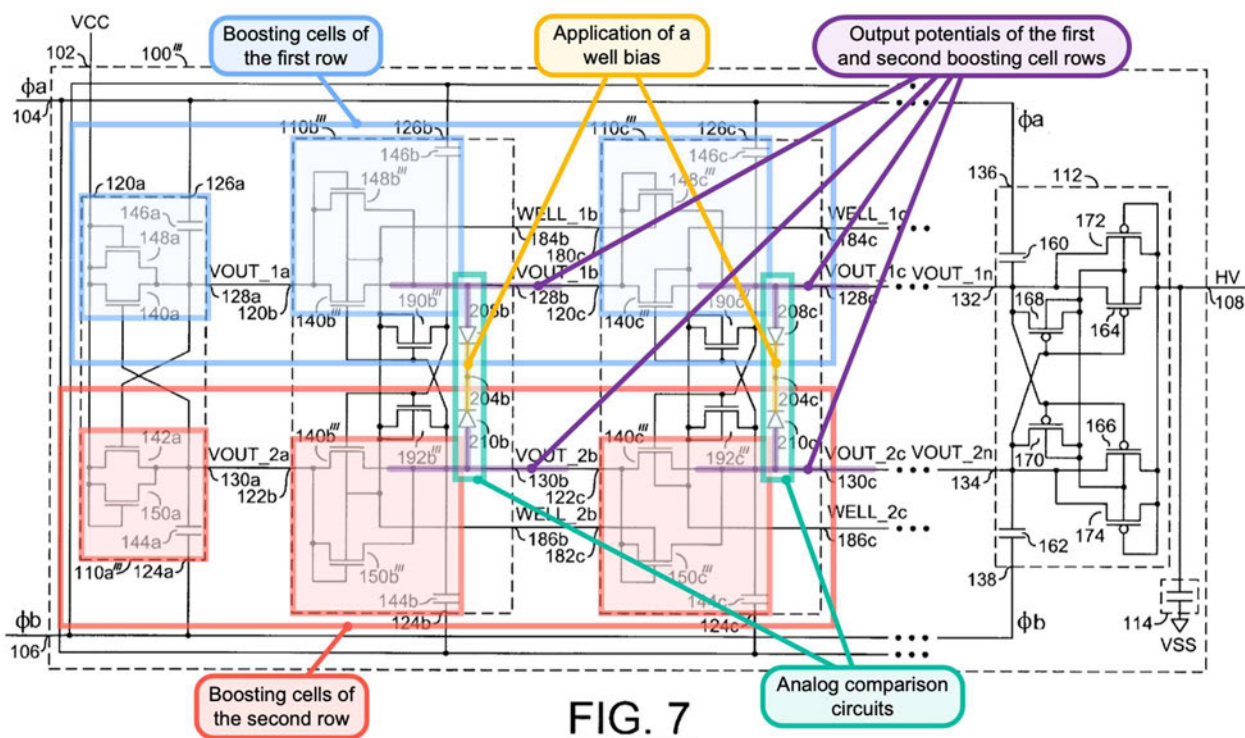
86. As I discussed in connection with claim limitations 1[d] and 1[e], it is my opinion that Fukushima discloses an analog comparison circuit (PMOS transistors PT1 n and PT2 n) that applies a well bias potential to the first well region (*i.e.*, N-well) of the switching elements (NMOS NT1 n and NT2 n) included in the boosting cells in the first and second boosting cell rows. *See* §IX.B.5 and §IX.B.6 above. As I discussed in connection with claim limitation 1[d], it is my opinion that the well bias potential outputted (*i.e.*, applied) by the analog comparison circuit (*i.e.*, one of PT1 n and PT2 n) depends on whichever of the nodes ND1 n and ND2 n that has the lowest potential. *See* §IX.B.5 above. The voltage at nodes ND1 n and ND2 n corresponds to the output potentials of the boosting cells of the n -th booster stage. EX1005, 5:58-61 (“In period A, the potential of node ND1 n rises by voltage Vdd due to capacitance coupling with pumping capacitor C1 n since clock clk supplies voltage Vdd. The potential of node ND2 n also drops because clock /clk supplies 0 Volt.”); *id.*, 6:9-12 (“In period B, the potential of node ND2 n rises by voltage Vdd due to capacitance coupling with pumping capacitor C2 n since clock /clk outputs voltage Vdd. The potential of node ND1 n also drops because clock clk supplies 0 Volt.”). Fukushima therefore teaches, in my view, that the well bias potential applied to the N-well is controlled according to the output potential of the boosting cells of the first and second boosting cell rows (*i.e.*, nodes ND1 n and ND2 n).

X. GROUND 2: MENG ANTICIPATES CLAIMS 1-3, 9, 10, AND 14

A. Overview of Meng

87. U.S. Patent No. 6,501,325 (“Meng”) was published on December 31, 2002, before the January 17, 2007 priority date of the ’557 patent. Meng qualifies as prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e) because it was patented on December 31, 2002, and thus before the January 17, 2007 priority date of the ’557 patent.

88. In my opinion, Meng teaches a two-row booster circuit comprising “cross-coupled charge pump stages configured to generate an output voltage ... [that] has a greater magnitude than the supply voltage.” EX1006, 2:24-29. Figure 7 of Meng, shown below with annotations, illustrates the booster circuit and its two-row structure, as well as the use of analog comparison circuits to compare voltages across two rows and to select and output a well bias potential to a deep N-well for numerous boosting cell stages. EX1006, Fig. 7.



89. Meng further teaches the use of a multiple-well structure for its switching elements, as shown below in Figure 4. EX1006, Fig. 4. The deep N-well of a switching element receives the well bias potential output by the analog comparison circuit. EX1006, Figs. 4, 7, 8:66-9:36.

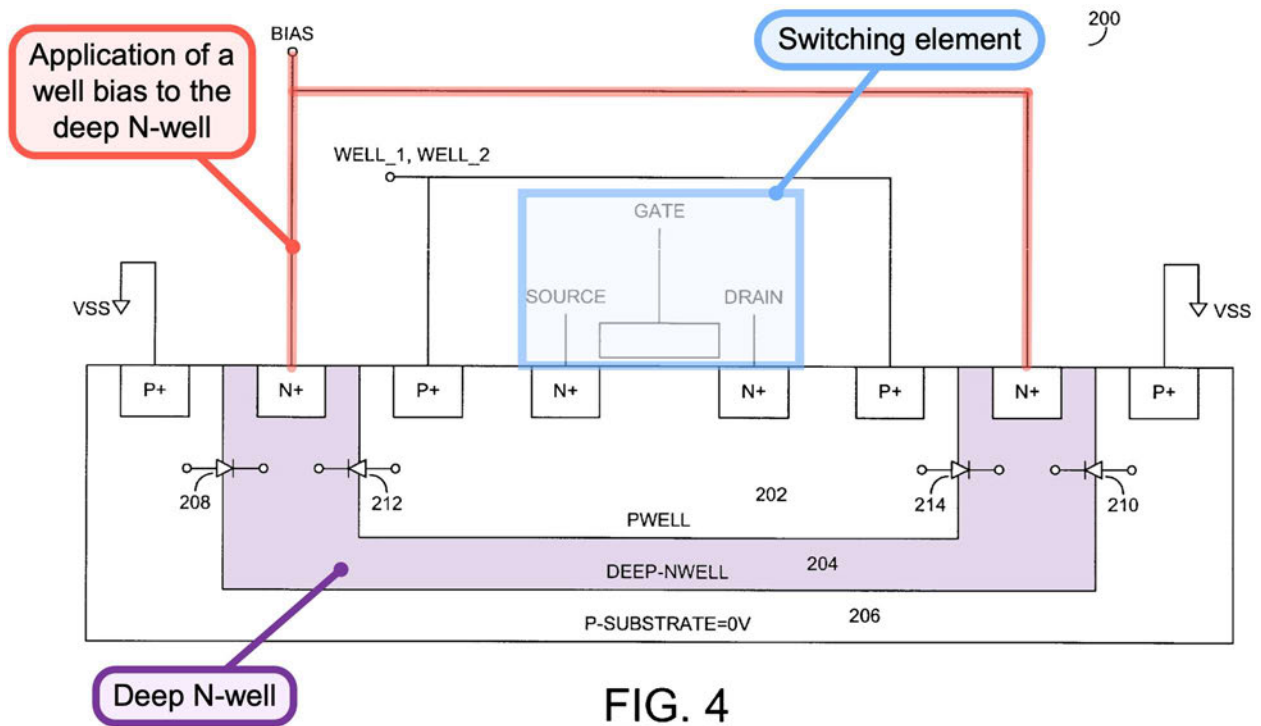


FIG. 4

90. The architecture of the booster circuit disclosed in Meng is designed to “(i) have improved efficiency, (ii) have reduced diode drop, (iii) perform well at low supply voltages, (iv) reduce the need for higher breakdown voltage transistors, (v) require little extra die area, and/or (vi) be easily implemented.” EX1006, 2:33-37.

91. In my opinion, Meng discloses claims 1-3, 9, 10, and 14 of the '557 patent at least under Patent Owner's apparent interpretation of the claim limitations. In particular, I understand that in the infringement contentions, Patent Owner identified circuit elements having a common well region as being circuit elements that also have the same potential of the common well region. As I explain below, under this interpretation, it is my opinion that Meng anticipates the foregoing claims of the '557 patent.

B. Claim 1

1. 1[pre]: A booster circuit comprising:

92. If the preamble is deemed to be limiting, it is my opinion that Meng discloses a booster circuit. EX1006, Fig. 7; *id.*, 1:7-10 (“The present invention relates to a method and/or architecture for *charge pumps* generally and ... to a method and/or architecture for low voltage supply high efficiency cross-coupled high voltage charge pumps.”); *id.*, 3:15-25 (“The circuit 100 may be implemented, as ... cross-coupled high voltage *charge pump circuit*.”). A “charge pump circuit,” which receives a supply voltage and outputs a voltage that has been charged to a level higher than the supply voltage, is a “booster circuit.” See §VI.A above.

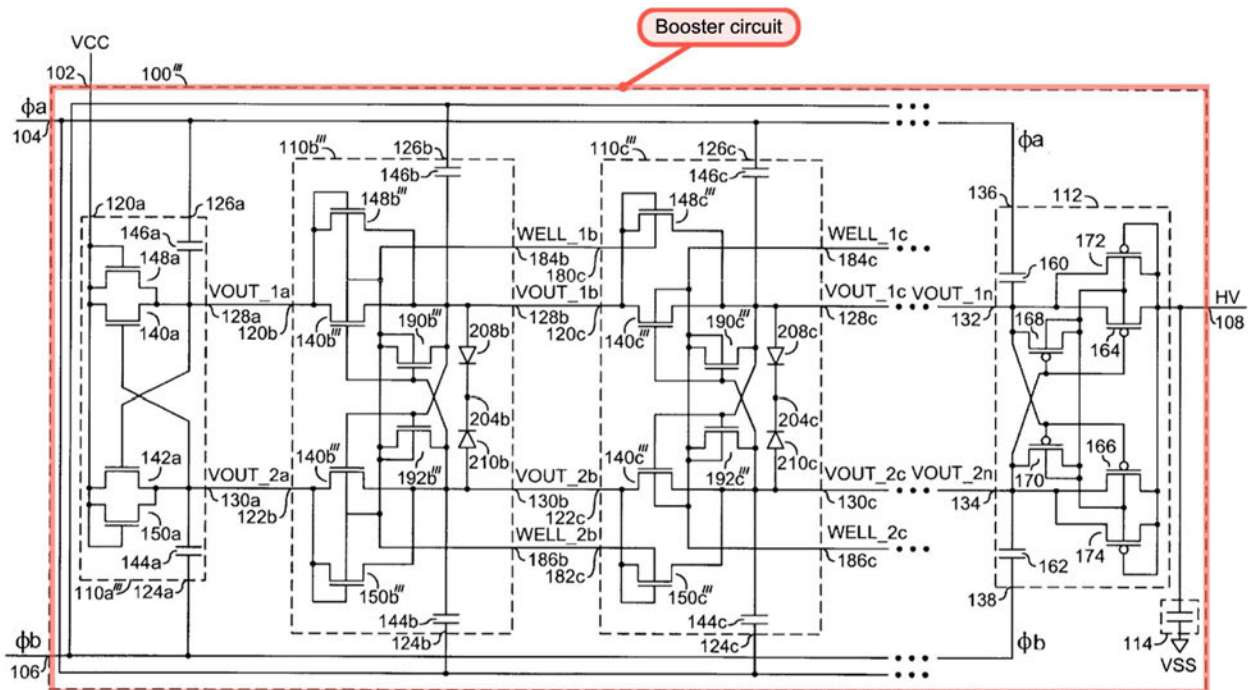


FIG. 7

2. **1[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region,**

93. In my opinion, Meng discloses claim limitation 1[a]. Meng discloses a booster circuit that “comprise[s] a number of circuits 110''*a*-110''*n*,” with each circuit representing a “stage” that comprises two “*boosting cells*.” EX1006, 8:43-46. As illustrated with annotations in Meng’s Figure 7 below, in the **boosting cell stage** 110b'', the **top boosting cell** includes transistors 140b'' and 148b'' and capacitor 146b, and the **bottom boosting cell** includes transistors 142b''² and 150b'' and capacitor 144b. EX1006, Fig. 7, 8:51-65.

² Meng’s Figure 7 incorrectly refers to the pumping transistor of the boosting cell in both the first and second boosting cell rows as 140*i*'', but in my opinion a POSITA would have identified this as a typographical error and understood the pumping transistor of the second boosting cell row to be 142*i*'', consistent with Meng’s specification. This is supported by my observation that circuit elements in the second boosting cell row are given different labels than their counterparts in the first boosting cell row. For example, a switching element in the first boosting cell row is identified in Meng’s Figure 7 as 148''*i* while the same switching element in the second boosting cell row is identified as 150''*i*. Similarly, a capacitor in the first boosting cell row is identified as 146*i* while a corresponding capacitor in the second boosting cell row is identified as 144*i*. EX1006, Fig. 7.

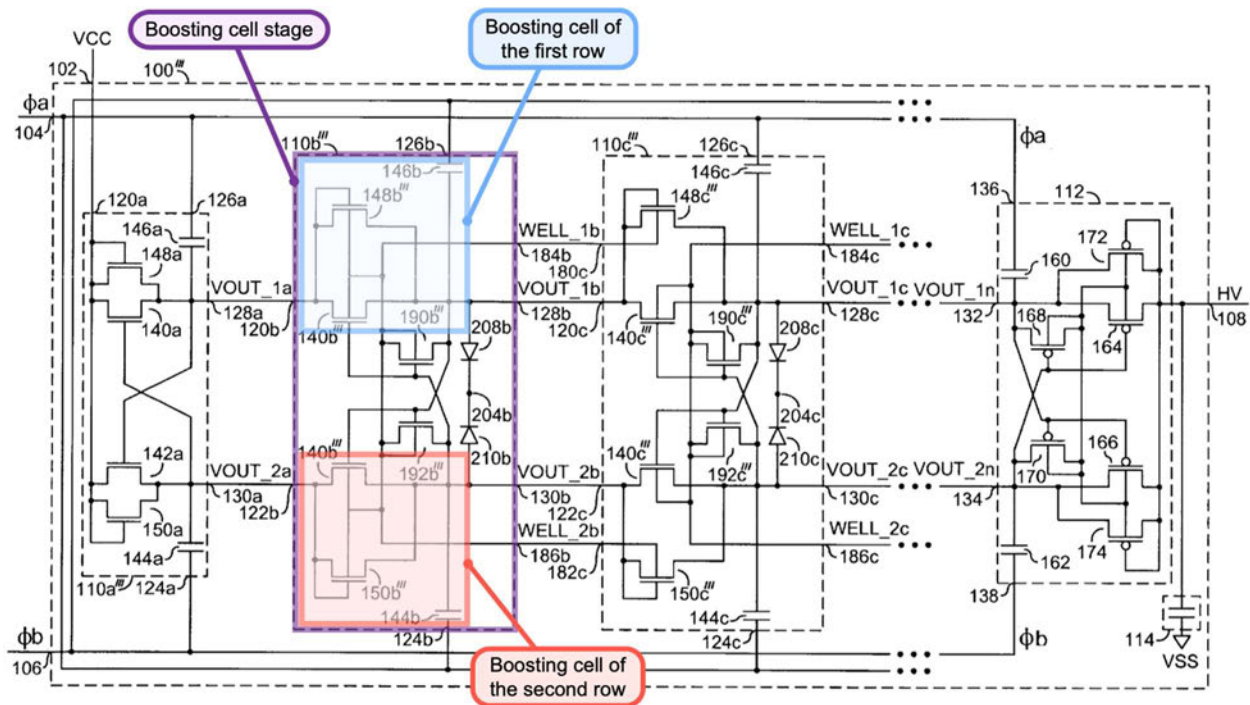


FIG. 7

94. Meng's Figure 4, shown below, provides a cross-sectional illustration of a transistor in Meng's boosting cells. EX1006, 8:61-65 ("The transistors [shown in the boosting stage of Fig. 7] may be implemented as one or more deep N-well NMOS transistors as shown in FIG. 4."). According to Meng, the transistors in each boosting cell "may have a *P-well region* ..., a *deep N-well region* ..., and a *P-substrate region*[" EX1006, 7:5-10. The deep N-well region—which is a first-conductivity type first well region—is placed on a substrate, and the P-well region—which is a second-conductivity type second well region—is placed in the deep N-well region (*i.e.*, the first well region).

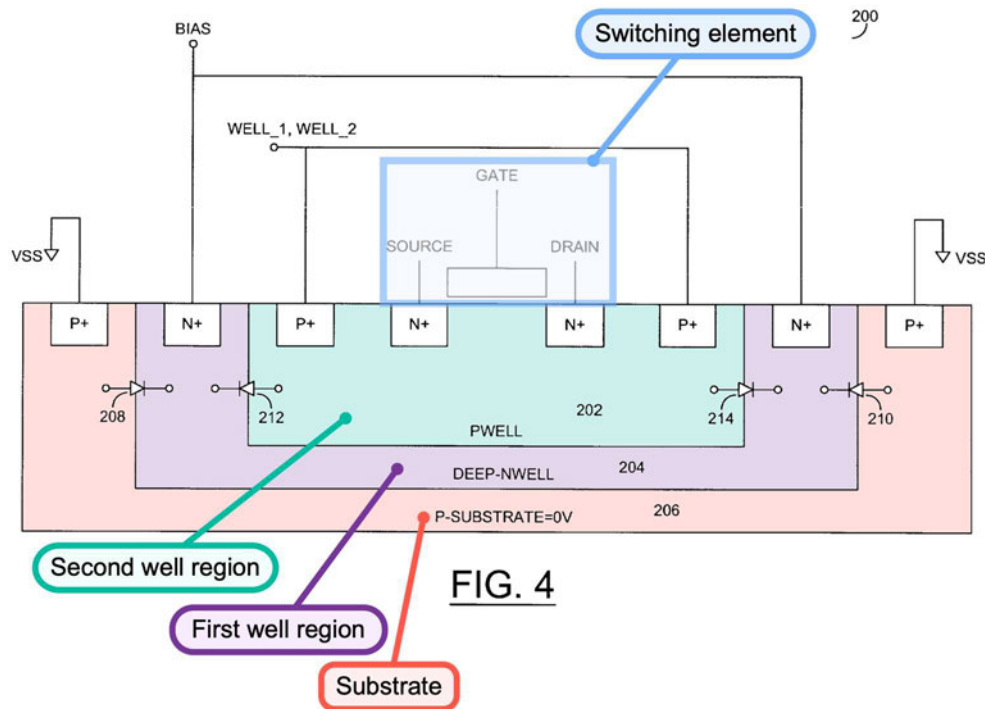


FIG. 4

3. 1[b]: and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal;

95. In my opinion, Meng meets claim limitation 1[b]. Meng discloses “at least one switching element,” comprising a source, gate, and drain, in both “the first well region” (*i.e.*, DEEP-NWELL 204) and “the second well region” (*i.e.*, PWELL 202). EX1006, 7:5-10, Fig. 4. In my view, the source, gate, and drain form a transistor, which is a “switching element” because the transistor switches the channel between its source and drain on and off based on a change in the voltage at its gate.

96. Meng discloses that “the at least one switching element switches to transfer charges from a first terminal to a second terminal.” The “transistors 140'''b-140'''n, 142'''b-142'''n, 148'''b-148'''n, 150'''b-150'''n, 190'''b-190'''n, and 192'''b-

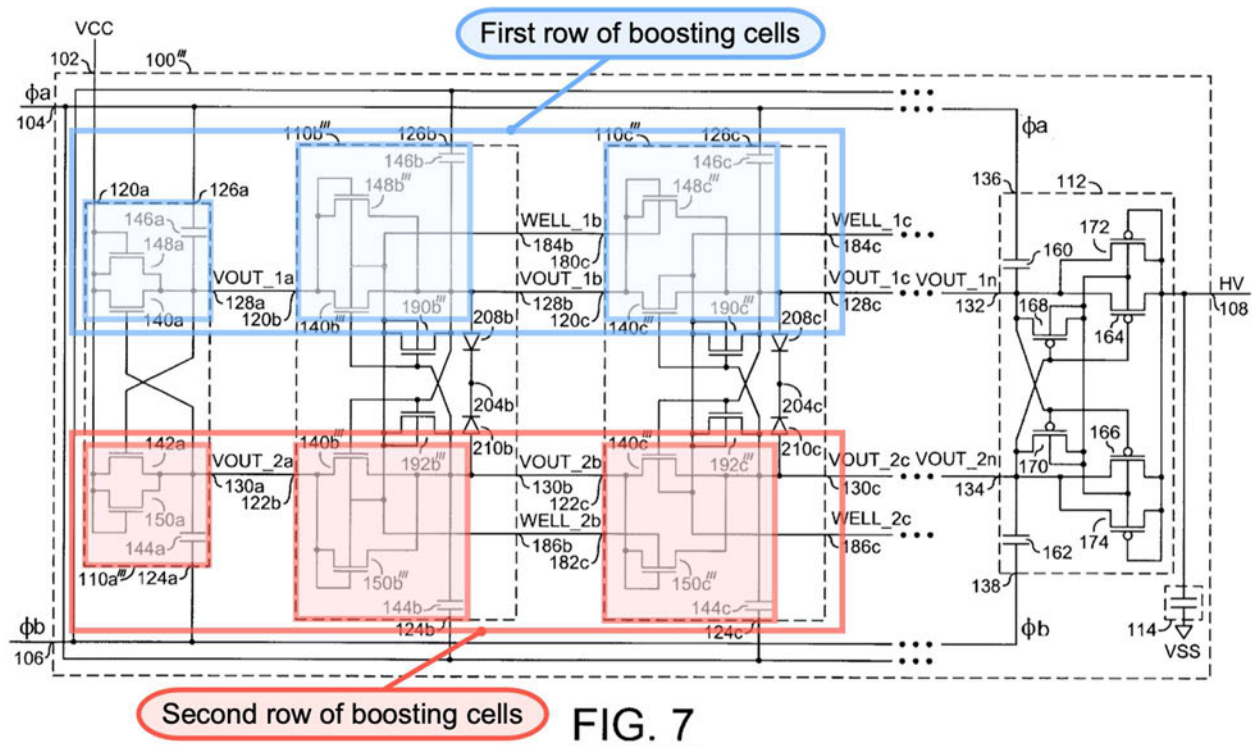
connection with claim limitation 1[a], Meng discloses boosting cell stages with each



97. In my opinion, Meng discloses claim limitation 1[c]. As I discussed in

66

stage comprising a boosting cell on the first row and a boosting cell on the second row. See §X.B.2 above. Figure 7, shown below, illustrates in my view “a **first boosting cell row**” including at least three stages of boosting cells ($N=3$) and “a **second boosting cell row**” also including at least three stages of boosting cells ($M=3$). EX1006, Fig. 7.

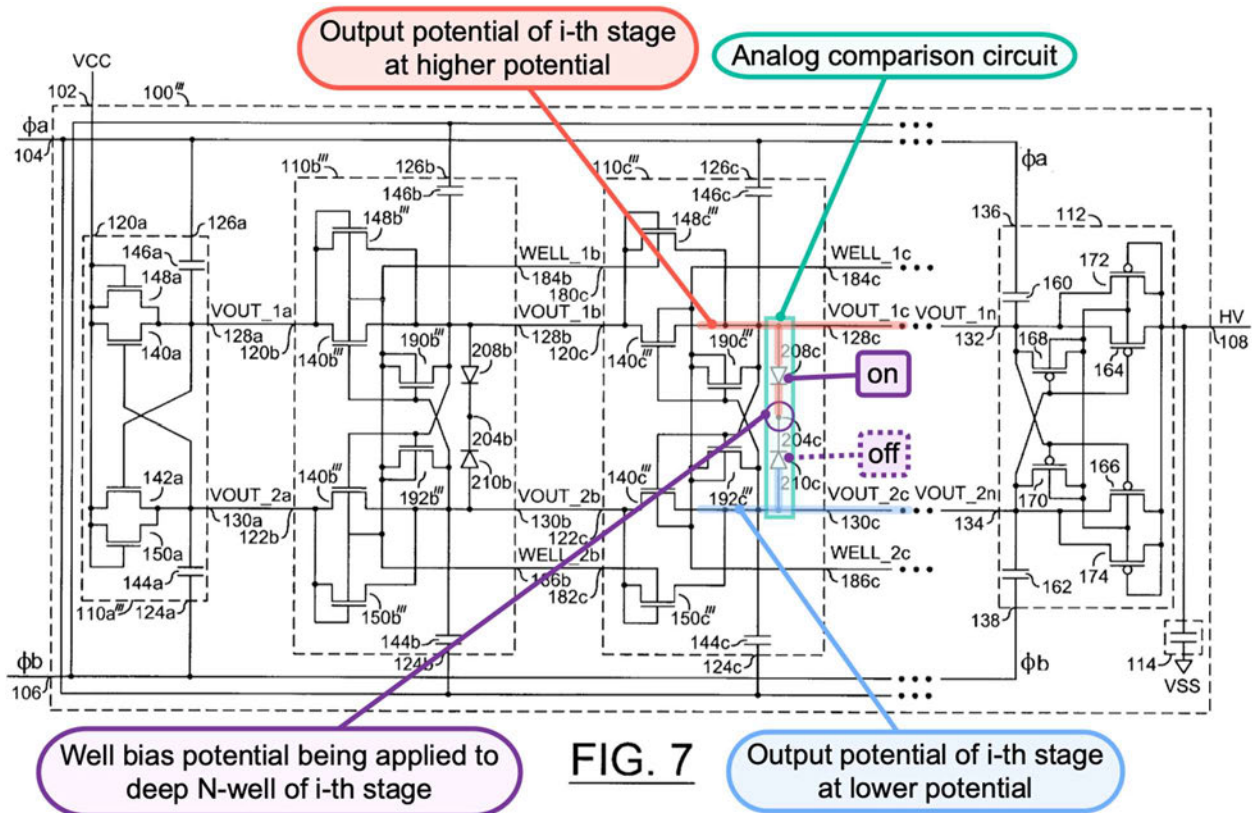


5. 1[d]: at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row,

98. In my opinion, Meng meets claim limitation 1[d]. As illustrated with annotations in Figure 7 below, Meng discloses an **analog comparison circuit** for outputting a **well bias potential** generated by the output potentials of the i -th

boosting cell stage of the first and second rows (**red** and **blue**, respectively).

EX1006, Fig. 7.



99. The analog comparison circuit, as shown above in Figure 7, comprises in my opinion two explicit diodes (*i.e.*, NMOS transistors with their drains tied to their gates, and with the input being the drain-gate connection and the output being the source terminal), namely, elements 208*i* and 210*i*, with inputs that correspond to the output potentials of the *i*-th stage of the first and second boosting cell rows, respectively. EX1006, Fig. 7.

100. In my opinion, identifying the analog comparison circuit as comprising elements 208*i* and 210*i* is consistent with Meng's Figure 8, shown below. EX1006,

Fig. 8. The analog comparison circuit comprising 208*i* and 210*i* outputs the higher voltage present at nodes 128*i* and 130*i* (VOUT_1*i* and VOUT_2*i*, respectively), which is consistent with the waveforms in Figure 8 which shows the output of the analog comparison circuit (*i.e.*, “DEEP N-WELL REGION 204*i* BIAS”) as consistently being the greater of VOUT_1*i* and VOUT_2*i* at any given instant in time.

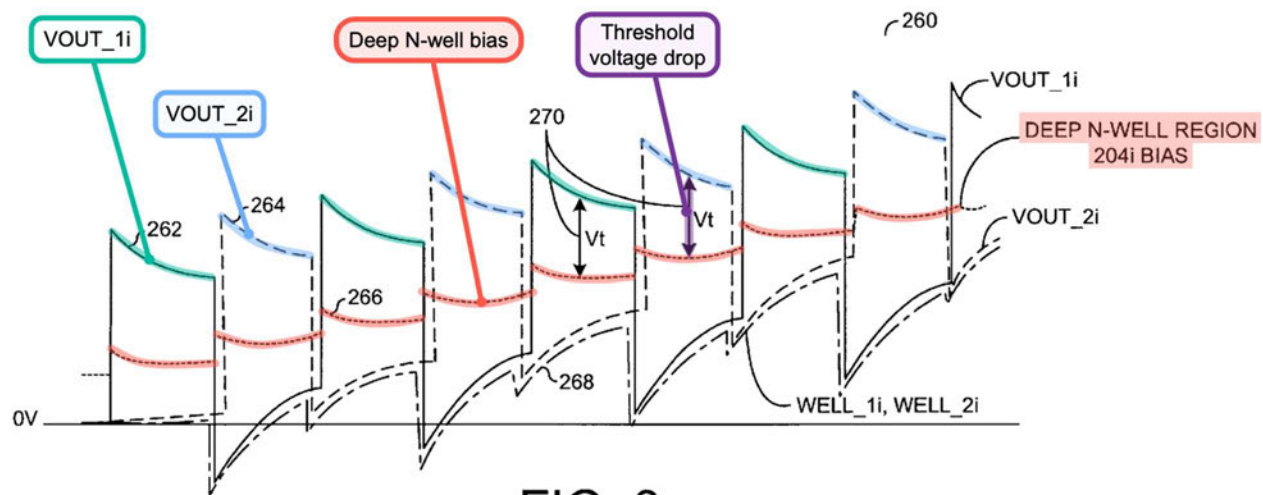


FIG. 8

101. Another basis for my opinion that 208*i* and 210*i* comprise an analog comparison circuit is the fact that nodes 128*i* and 130*i* serve as the drain/source terminals of transistors 140*i* and 142*i*, respectively. The drain/source terminals of transistors 140*i* and 142*i* are N-type because 140*i* and 142*i* are NMOS transistors. Further, the output of 208*i* and 210*i* is to 204*i*, and since 204*i* is identified by Meng as being a deep N-well, element 204*i* is by definition an N-type material. EX1006, 9:6-7 (“The node 204*i* may be the deep N-well region[.]”). And so both ends of 208*i*

and 210*i* are connected to N-type material, and this type of connection is only feasible if 208*i* and 210*i* are explicit diodes (diode-connected transistors). If 208*i* and 210*i* were parasitic diodes, both elements would have to be N-type on one end and P-type on the other end. Therefore, the switching elements 208*i* and 210*i* are in my opinion explicit diodes (diode-connected transistors) consistent with what a POSITA would have understood comparison circuits to be.

102. Another basis for my opinion that 208*i* and 210*i* comprise an analog comparison circuit, and more specifically that 208*i* and 210*i* are explicit diodes (diode-connected transistors), is the fact that Meng's Figure 8, shown below, presents waveform 266 (*i.e.*, "DEEP N-WELL REGION 204*i* BIAS") as having a voltage drop of V_t (*i.e.*, a transistor threshold voltage). EX1006, Fig. 8. Such a voltage drop of V_t would only occur across an explicit diode, that is, a diode-connected transistor. If 208*i* and 210*i* were instead parasitic diodes, then the voltage drop would not be identified as V_t , but would instead be labelled V_d .

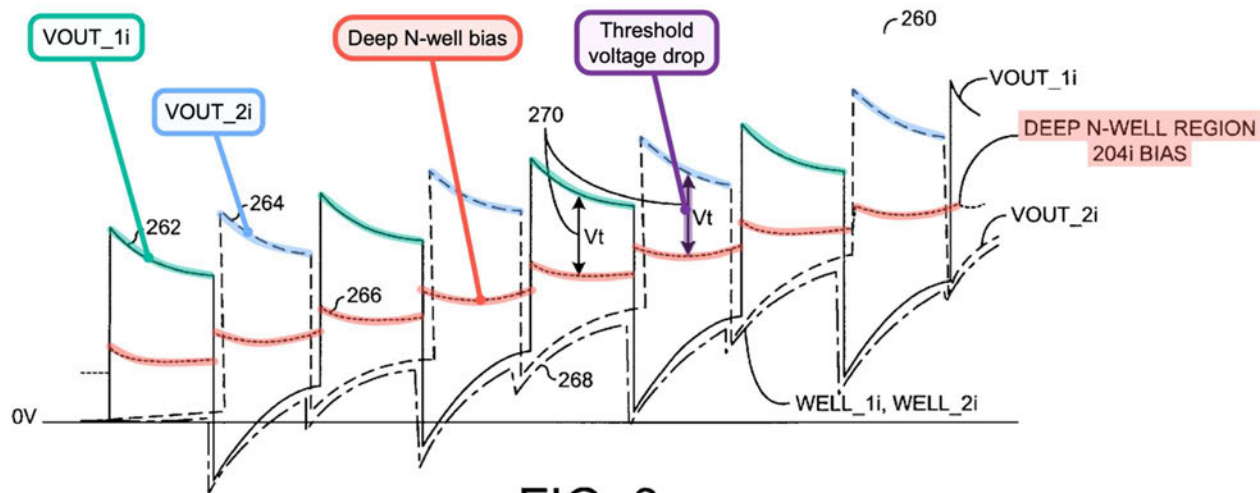


FIG. 8

103. Furthermore, the symbol associated with 208*i* and 210*i* in Meng's Figure 7 is also used to represent an explicit diode, as a POSITA would have understood on the priority date of the '557 patent. In terms of implementation, the analog comparison circuit comprising 208*i* and 210*i* could be implemented in the same way as elements 148*i* and 150*i* (*i.e.*, as diode-connected transistors).

104. Identifying elements 208*i* and 210*i* as comprising an analog comparison circuit is also consistent with Meng's teaching that "[t]o ensure the diodes 212 and 214 are reverse biased, the deep N-well region 204 is generally biased to a voltage (e.g., the signal BIAS) that is higher than the P-well region 202 (e.g., the deep N-well region 204 is generally biased to the higher positive voltage of the source of the drain voltages)." EX1006, 7:39-43. An analog comparison circuit comprising 208*i* and 210*i* helps implement this important teaching, *i.e.*,

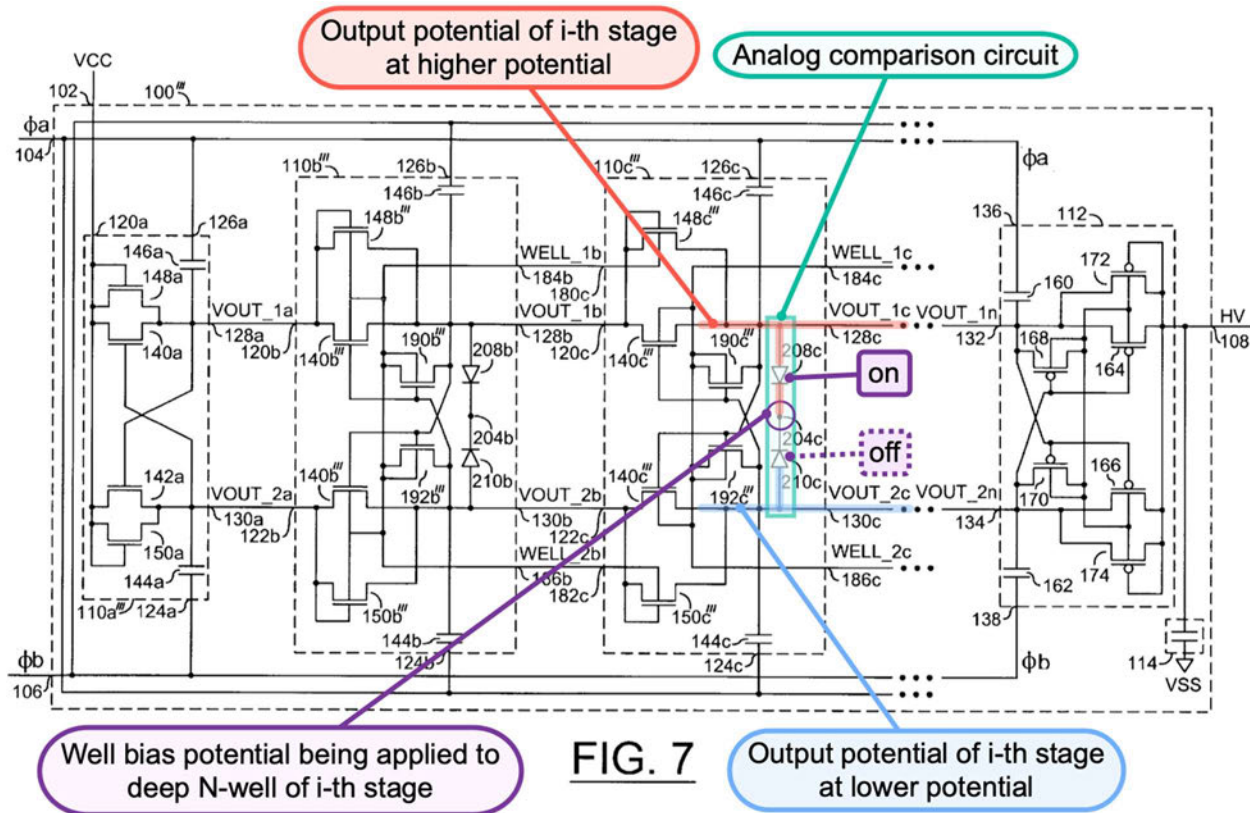
biasing the deep N-well to the higher positive voltage of the first and second boosting cell rows in order to avoid forward-biasing.

105. As I discussed above in §VI.D, for any given stage, one row of the boosting stage will have an output potential that is higher than the output potential of the other row due to the alternating clock signals that are applied to the boosting stage. Whichever of the two diodes in the analog comparison circuit 208*i* and 210*i* has the higher potential at its input terminal is the diode that switches on and outputs a well bias potential generated by the higher input potential³; the opposing diode in the analog comparison circuit remains off thereby blocking any charge transmission. The diode (*i.e.*, transistor) that switches on does so because the voltage difference between its input and output is greater than the threshold voltage V_t (*i.e.*, the minimum voltage needed for activation) for that diode; the opposing diode remains off because the voltage difference between its input and output would be negative and far less than the threshold voltage. *See* EX1006, Fig. 8 (illustrating the relationship between V_t and the activation of a diode-connected transistor). Meng therefore discloses, in my opinion, an analog comparison circuit that outputs a well bias potential generated by the output potentials of the first and second rows of the boosting stage.

³ According to Figure 7 of Meng, the *inputs* to the analog comparison circuit are the *outputs* of the boosting stage.

6. **1[e]: wherein the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.**

106. In my opinion, Meng discloses claim limitation 1[e]. Meng teaches that “[t]he circuit 100” [*i.e.*, the booster circuit] may be implemented using P-well biasing and deep N-well biasing.” EX1006, 8:46-48. As I discussed above in connection with claim limitation 1[d] and shown below in Figure 7, Meng teaches an analog comparison circuit that outputs a well bias potential to a node 204*i*. EX1006, Fig. 7. According to Meng, “[t]he node 204*i* may be the ***deep N-well region*** of the transistors 140"*i*, 142"*i*, 148"*i*, 150"*i*, 190"*i*, and 192"*i*,” where transistor 140"*i* is the switching element included in the *i*-th boosting cell of the first boosting cell row and transistor 142"*i* is the switching element included in the *i*-th boosting cell of the second boosting cell row. EX1006, 9:6-8, Fig. 7. The analog comparison circuit therefore applies, in my opinion, a well bias potential to a deep N-well region (*i.e.*, first well region) of the switching elements included in the at least one boosting cell of the first and second boosting cell rows.



107. That the well bias potential is applied to the deep N-well (*i.e.*, first well region) is further confirmed in my opinion by Meng’s Figure 8, which “illustrat[es] example [voltage] waveforms of the circuit 100” of FIG. 7” for “a stage 110” i of the circuit 100” over a number of cycles of the signals ϕa and ϕb during pump up.” EX1006, Fig. 8, 9:37-41. As shown below in Figure 8, waveforms 262 and 264 illustrate the output potentials of the i -th stage of the first and second boosting cell rows (VOUT_{1i} and VOUT_{2i}), respectively, while “waveform 266 may illustrate the ***bias voltage*** [*i.e.*, well bias potential] ***at the deep N-well region*** 204 i [*i.e.*, first well region].” EX1006, 9:41-44, Fig. 8. And as would be expected for voltage transmission across a switching element, “[t]he waveforms 262 and 264 [*i.e.*, the

output potentials of the i -th boosting cell that are inputs to the analog comparison circuit] and the waveform 266 [*i.e.*, well bias potential applied to the deep N-well region] may have a difference 270” which “may be the threshold voltage V_t ” of the diodes (diode-connected transistors) 208 i and 210 i . EX1006, 9:46-48.

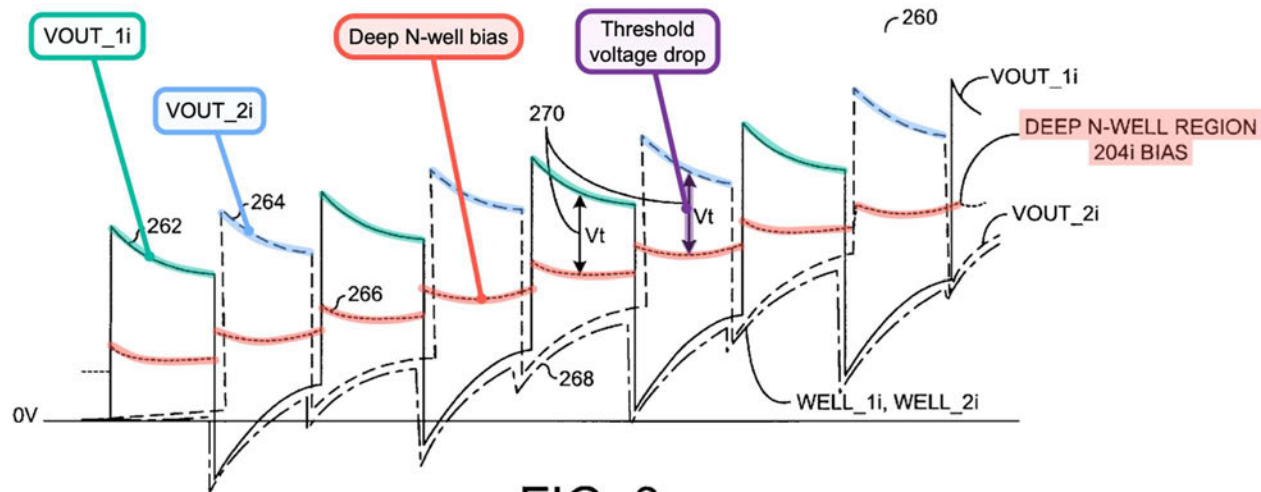


FIG. 8

C. Claim 2

1. 2[pre]: The booster circuit of claim 1, wherein:

108. In my opinion, Meng discloses 2[pre] as I discussed in connection with claim 1. See §X.B above.

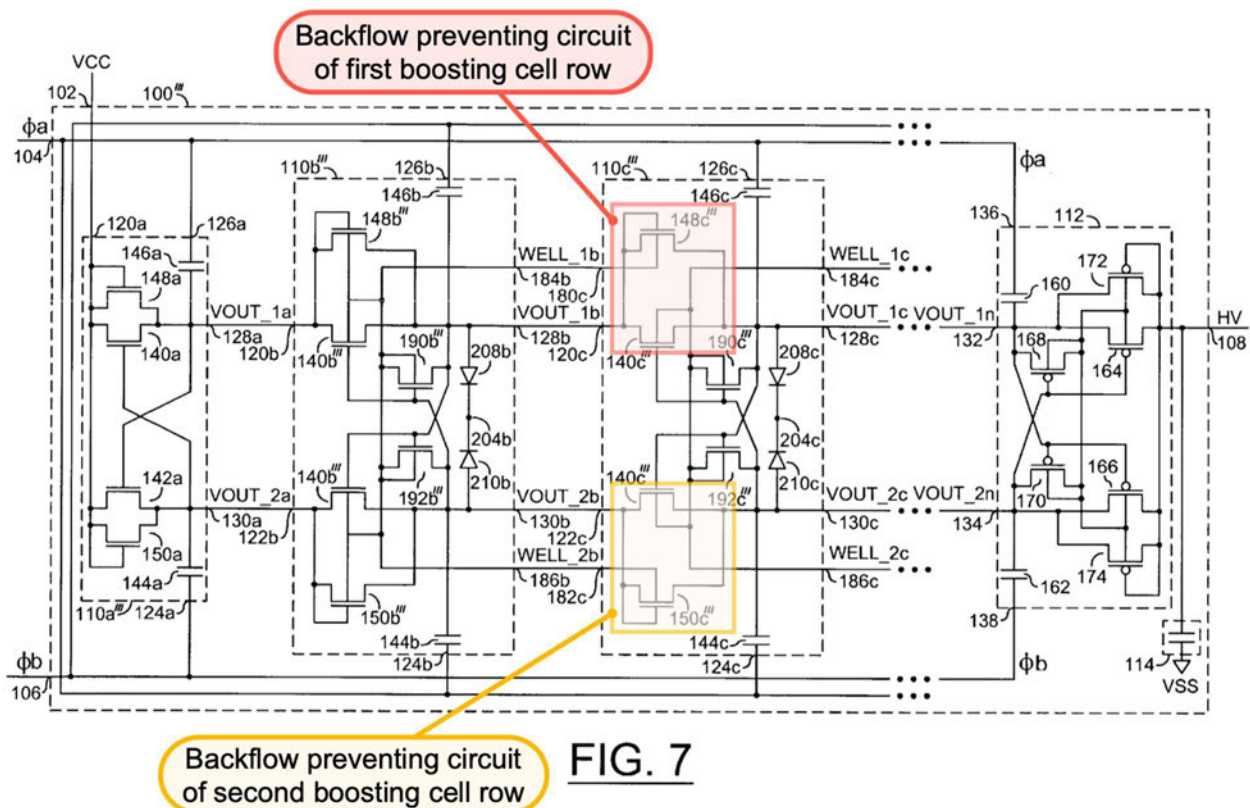
2. 2[a]: the first boosting cell row includes N stages ($N \geq 1$) of the boosting cells and at least one backflow preventing circuit; the second boosting cell row includes M stages ($M \geq 1$) of the boosting cells and at least one backflow preventing circuit; and

109. In my opinion, Meng discloses 2[a]. As I discussed in connection with claim limitation 1[c], it is my opinion that Meng discloses two boosting cell rows

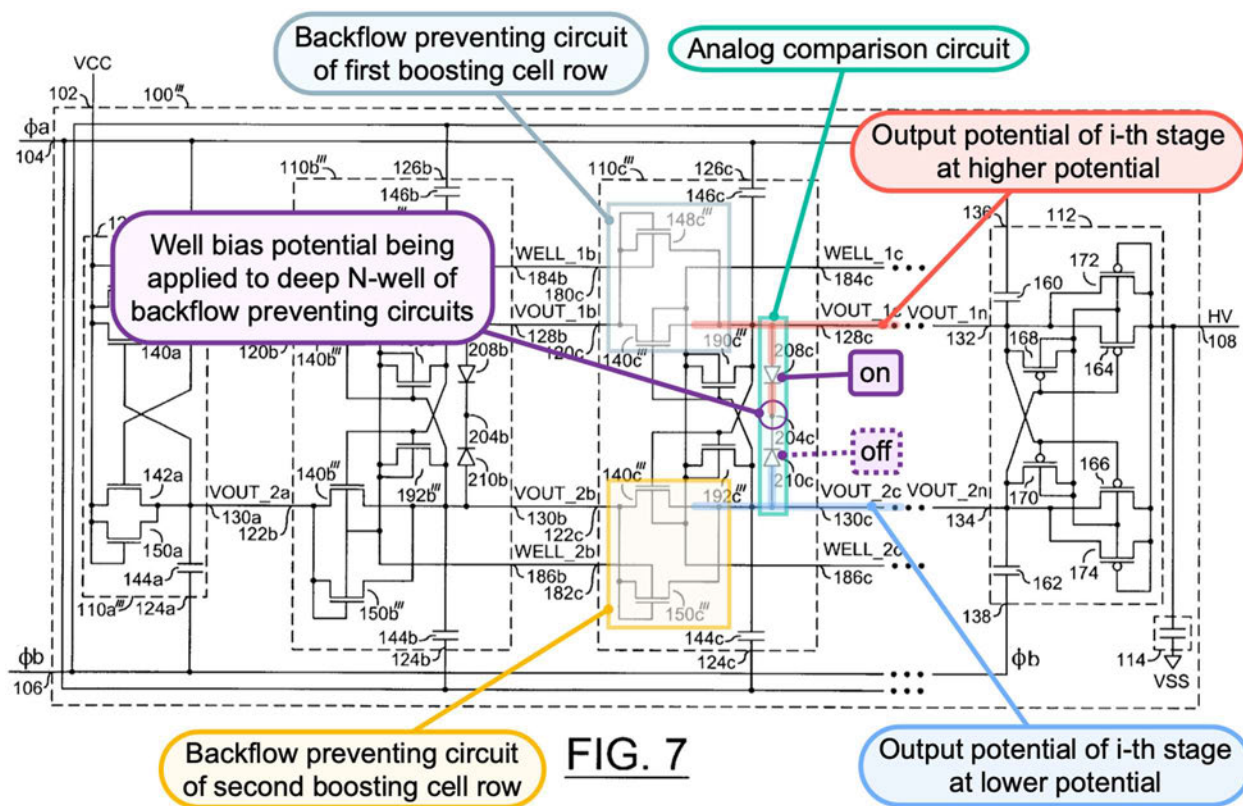
(*i.e.*, a first and a second boosting cell row), each including at least one boosting cell stage. *See* §X.B.4 above.

110. In my opinion, Meng also discloses at least one backflow preventing circuit in both the first and second boosting cell rows. As shown in Figure 7 below, transistors 140^{'''i} and 148^{'''i} serve as the backflow preventing circuit for the first boosting cell row, and transistors 142^{'''i} and 150^{'''i} serve as the backflow preventing circuit for the second boosting cell row. EX1006, Fig. 7. As I discussed in connection with claim limitation 1[b], there is charge transfer in the desired rightward direction across transistor 140^{'''i} and 148^{'''i} in the first row, and also across transistors 142^{'''i} and 150^{'''i} in the second row. *See* §X.B.3 above. This rightward charge transfer occurs when the input node of the *i*-th boosting stage (*i.e.*, 120ⁱ and 122ⁱ) has a higher voltage than the output node (*i.e.*, 128ⁱ and 130ⁱ) since pump transistors 140^{'''i} and 148^{'''i} for the first row, and pump transistors 142^{'''i} and 150^{'''i} for the second row are switched on by virtue of their gate potentials being greater than their source (right terminal) potentials. The occurrence of backflow (*i.e.*, undesirable charge transfer in the leftward direction) is prevented by the backflow preventing circuits 148^{'''i} and 150^{'''i} since they switch off whenever the output nodes 128ⁱ and 130ⁱ have a higher voltage than the input nodes 120ⁱ and 122ⁱ; they switch off and prevent charge transfer because the gate and source (left terminals) potentials are equivalent. Transistor 140^{'''i} is also a backflow preventing circuit since once it

charges its output 128*i* high, the output on the opposite row 130*i* is pulled low by the clock signal, which then switches transistor 140'''*i* off thereby preventing backflow (leftward). Similarly, transistor 142'''*i* is also a backflow preventing circuit since once it charges its output 130*i* high, the output on the opposite row 128*i* is pulled low by the clock signal, which then switches transistor 142'''*i* off thereby preventing backflow (leftward).

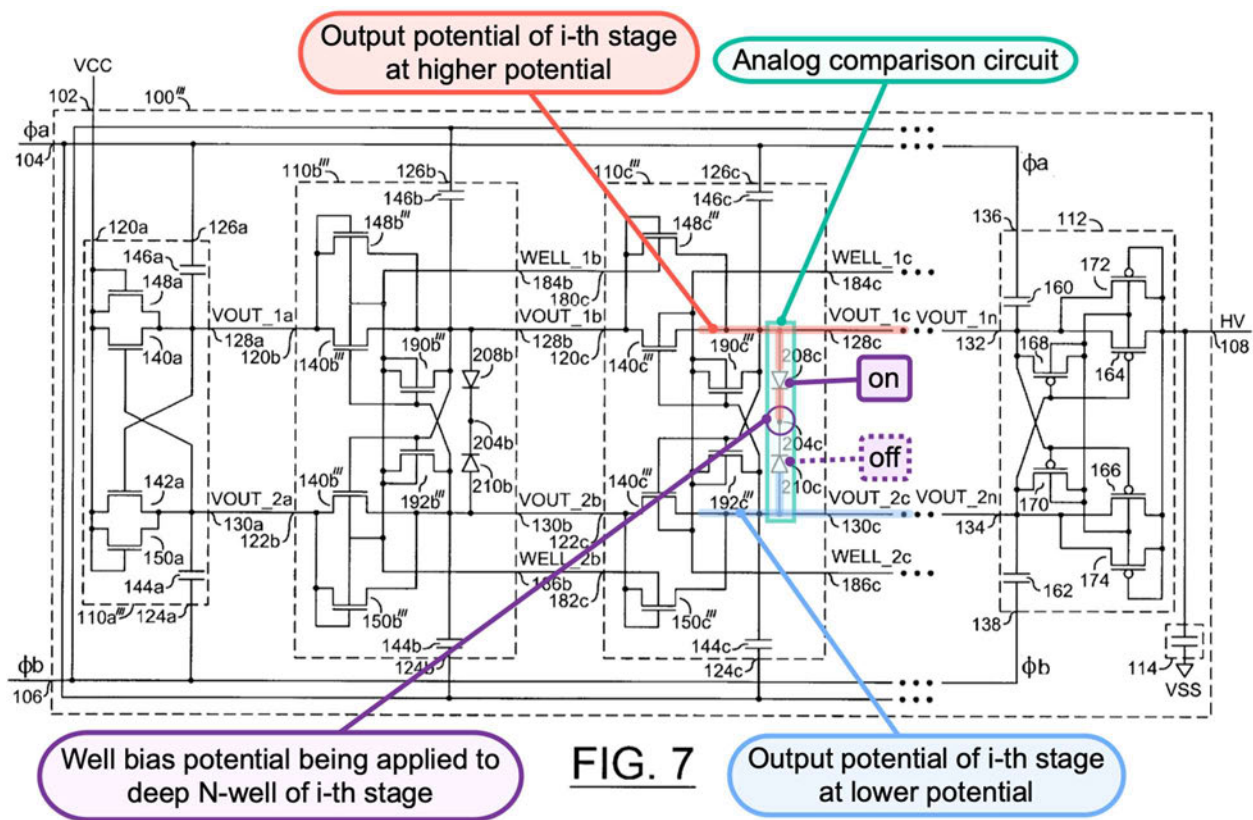


an analog comparison circuit that outputs a well bias potential to a node 204i. §X.B.5, *supra*; EX1006, Fig. 7. According to Meng, “[t]he node 204i may be the **deep N-well region** of the transistors 140ⁱ, 142ⁱ, 148ⁱ, [and] 150ⁱ,” where, as I discussed in connection with claim limitation 2[a], transistor 140ⁱ is the switching element included in the backflow preventing circuit of the first boosting cell row, and transistor 142ⁱ is the switching element included in the backflow preventing circuit of the second boosting cell row. EX1006, 9:6-8, Fig. 7; §X.C.2, *supra*. In my opinion, the analog comparison circuit therefore applies a well bias potential to a deep N-well region (*i.e.*, first well region) of the switching elements included in the at least one backflow preventing circuit of the first and second boosting cell rows.



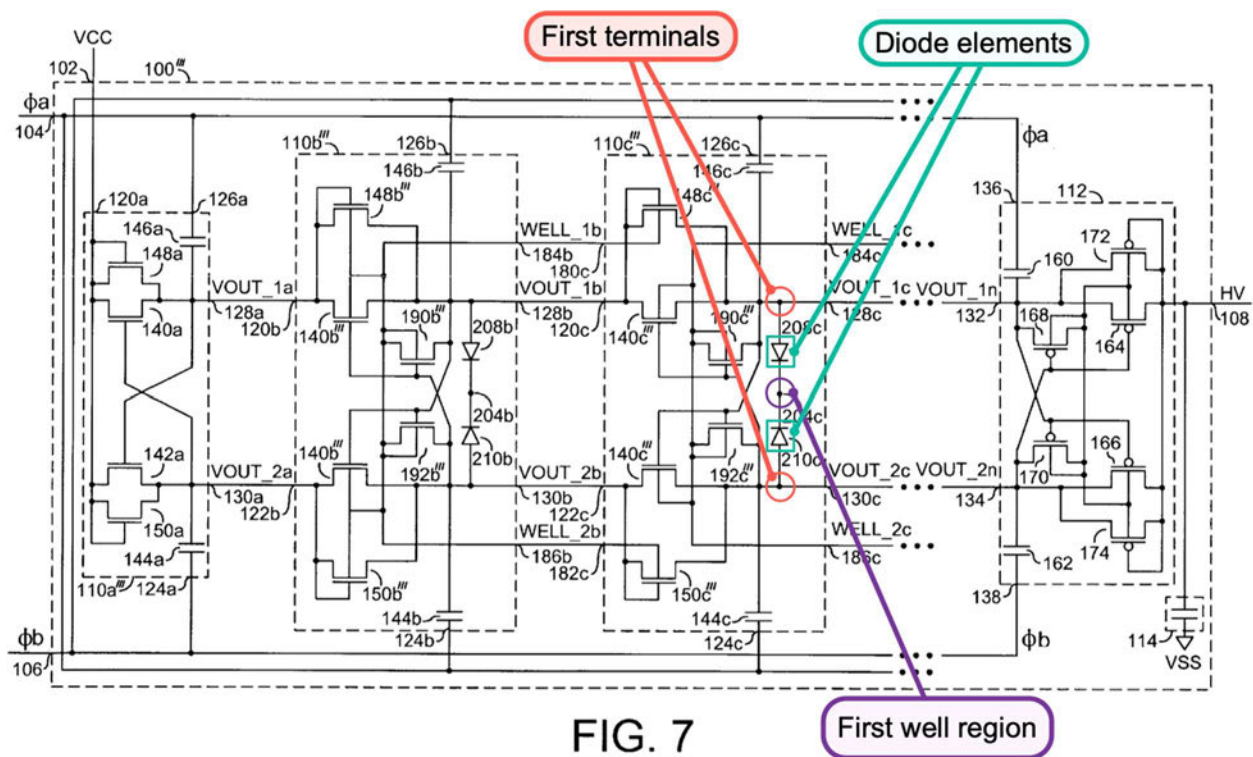
- D. Claim 3:** The booster circuit of claim 1, wherein the well bias potential is the higher potential out of the output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

112. In my opinion, Meng discloses claim 3. As I discussed in connection with claim limitation 1[d], Meng discloses an analog comparison circuit that outputs a well bias potential that is the higher potential out of the output potentials of the first and second rows of the boosting stage. See §X.B.5 above. As shown below in Figure 7, the diode of the analog comparison circuit (i.e., 208i and 210i) that switches on is a diode that outputs the **higher** potential of the two boosting stage output potentials. EX1006, Fig. 7.



E. Claim 9: The booster circuit of claim 1, wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

113. In my opinion, Meng discloses claim 9. As I discussed in connection with claim limitation 1[d] and as shown below in Figure 7, Meng discloses a diode 208*i* that is provided between a first terminal 128*i* and the deep N-well node 204*i* (*i.e.*, first well region), as well as a diode 210*i* that is provided between a first terminal 130*i* and the deep N-well node 204*i*. EX1006, Fig. 7; §X.B.5, *supra*.



F. Claim 10: The booster circuit of claim 1, wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region.

114. In my opinion, Meng discloses claim 10. In Figure 7, shown below, Meng discloses switching elements of the first and second boosting cell rows that

115. As identified by the annotations to Figure 7 above, transistor 140'''i is the ***switching element*** of the first boosting cell row, and transistor 142'''i is the switching element of the second boosting cell row. EX1006, Fig. 7. And Meng teaches, in my opinion, transistors 140'''i and 142'''i (*i.e.*, switching elements of the first and second boosting cell rows, respectively) all share a common deep N-well (*i.e.*, first well region). EX1006, 9:6-7 (“The node 204i may be the deep N-well region of the transistors 140'''i [and] 142'''i.”).

116. Moreover, identifying transistors 140''i and 142''i as “having the same potential of the first well region” is, according to my understanding, consistent with



how the Patent Owner interpreted claim 10. In particular, I understand that in the infringement contentions in the related district court litigation, the Patent Owner contended that [REDACTED]

[REDACTED]

[REDACTED] EX1008 at 42.

117. Accordingly, based on at least the Patent Owner's apparent interpretation, it is my opinion that Meng discloses at least one switching elements having the same potential of the first well region.

G. Claim 14

1. 14[pre]: A booster circuit comprising:

118. In my opinion, Meng discloses claim limitation 14[pre] as I discussed in connection with 1[pre]. *See* §X.B.1 above.

2. 14[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

119. As I discussed in connection with claim limitation 1[a], it is my opinion that Meng discloses boosting cells each having a deep N-well (*i.e.*, first-conductivity type first well region) on a P-type substrate, and a P-well (*i.e.*, second-conductivity type second well region) in the deep N-well. *See* §X.B.2 above. And as I discussed in connection with claim limitation 1[b], it is my opinion that Meng discloses a switching element in both the deep N-well and P-well. *See* §X.B.3 above.

3. **14[b]: wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;**

120. As I discussed in connection with claim limitation 1[b], it is my opinion that Meng discloses switching elements that transfer charges from a first terminal to a second terminal. *See* §X.B.3 above. As I discussed in connection with claim limitations 1[d] and 1[e], it is my opinion that Meng discloses switching elements that are capable of switching on and off in order to transfer or block charges between terminals on opposing sides of the switching element. *See* §X.B.5 and §X.B.6 above.

4. **14[c]: a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;**

121. As I discussed in connection with claim limitation 1[c], it is my opinion that Meng discloses two boosting cells rows (*i.e.*, a first and a second boosting cell row) with each boosting cell row including at least one boosting cell stage. *See* §X.B.4 above.

5. **14[d]: wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.**

122. As I discussed in connection with claim limitation 1[d], it is my opinion that Meng discloses an analog comparison circuit that outputs a well bias potential.

See §X.B.5 above. As I discussed in connection with claim limitation 1[e], it is my opinion that the well bias potential outputted by the analog comparison circuit is applied to the deep N-well (*i.e.*, first well region) of the switching element(s) included in the boosting cell of the first and second boosting cell rows. *See* §X.B.6 above. And as I discussed in connection with claim limitations 1[d] and 1[e], it is my opinion that the operation of the analog comparison circuit, and by extension the well bias potential, is controlled according to an output potential of the boosting cell of the first row and the output potential of the boosting cell of the second row. *See* §X.B.5 and §X.B.6 above.

XI. GROUND 3: MENG AND PARK RENDER OBVIOUS CLAIMS 1-4, 6-12, AND 14

A. Overview of Park

123. U.S. Patent No. 6,914,791 (“Park”) was published on July 5, 2005, before the January 17, 2007 priority date of the ’557 patent. Park qualifies as prior art under pre-AIA 35 U.S.C. §§102(a), (b), and (e) because it was patented on July 5, 2005, and thus before the January 17, 2007 priority date of the ’557 patent. I further understand that Park was not considered by the Examiner during prosecution of the ’557 patent.

124. In my opinion, Park teaches a “multi-stage charge pump circuit” comprising “MOSFET devices within a triple well.” EX1007, 3:38-44. The charge pump detailed by Park includes “an auxiliary device Ms that couples a boosted drain

potential of the charge transfer MOS device to the P-well and the deep N-well to switch the coupling between the charge transfer MOS device and the substrate region, thus ... reducing the body effect on the charge transfer MOS device.” EX1007, 5:31-36. By having “the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt” whenever Mt is turned on, the “charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without any voltage loss caused by the body effect.” EX1007, 6:60-7:1. In other words, the application of a well bias potential to both the P-well and deep N-well reduces the body effect, thereby “allow[ing] [the charge pump] to provide more voltage and current at the output so that the charge pump circuit can be implemented in fewer stages.” EX1007, 6:24-26.

B. Combining Meng with Park

125. In my opinion, a POSITA would have been motivated to combine Meng’s two-row booster circuit structure comprising multiple well regions and an analog comparison circuit with Park’s teaching of applying a well bias potential to both the P-well and deep N-well. The figure shown below illustrates how in my view Park can be combined with Meng to yield a two-row booster circuit with an analog comparison circuit that outputs a well bias potential to a deep N-well. EX1006, Fig. 7; EX1007, Fig. 9.

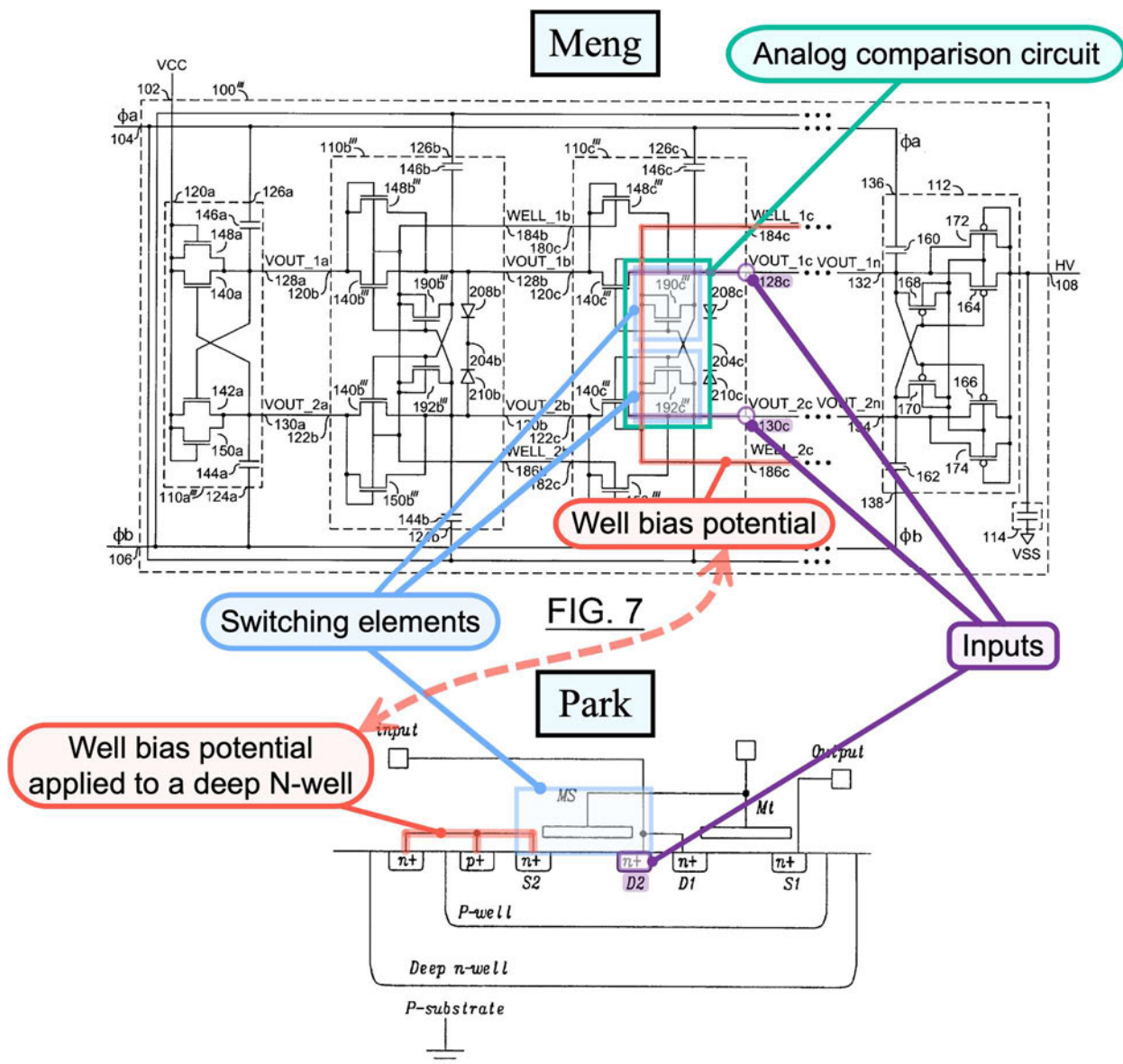


FIG. 9

126. In my opinion, a POSITA would have found it obvious to combine Meng and Park in order to effectuate Meng's teaching that "[t]he combination of P-well biasing and deep N-well biasing ... may (i) **reduce body effect** and (ii) minimize the threshold voltage V_t across all of the [charge pump] stages." EX1006, 8:30-33; *see also id.*, 9:32-36 ("The combination of P-well biasing and deep N-well biasing

... may (i) reduce body effect and (ii) minimize the threshold voltage V_t across all of the [charge pump] stages.”). Park states that it is “an *objective* of the present invention to *reduce the body effect* to the charge transfer MOSFET device [*i.e.*, the pump transistor] by the transfer of the boosted source voltage by an auxiliary MOSFET device to the P-well and N-well of each stage.” EX1007, 3:62-66. A POSITA would therefore have been motivated, in my view, to give effect to Meng’s teachings by incorporating Park’s disclosure of an “auxiliary device [that] *reduces a body effect* on [a] charge transfer device by transferring a boosted ... voltage of the charge transfer device *to the P-well and the deep N-well.*” EX1007, cl. 10.

127. Both Meng and Park offer in my opinion a charge pump design that offers *greater efficiency*, which in turn enables a *reduction in the silicon die area* utilized by the charge pump. EX1006, 2:30-37 (“The objects, features and advantages of the present invention include ... [an] architecture for ... [a] charge pump that may (i) have *improved efficiency*, ... [and] (v) require *little extra die area.*”); EX1007, 6:21-27 (the reduction of the body effect “allows [the charge pump] to provide more voltage and current at the output [*i.e.*, *increased efficiency*] so that the charge pump circuit can be implemented in fewer stages, which results in *less silicon die area*”). In my opinion, a POSITA would have been motivated to incorporate Park’s teachings into Meng because the benefits and improvements offered by Park were aligned with the design objectives described by Meng.

128. Indeed, it is my opinion that a POSITA would have had a reasonable expectation of success in the combination of Meng and Park. Both Meng and Park provide significant detail, in my view, regarding the architecture of the charge pump circuit, and both utilize the same set of well-known, conventional circuit components in their charge pump circuit designs. Implementing Meng using Park's wired connection between the P-well and deep N-well would have been straightforward and well within the capabilities of a POSITA at the time of the '557 patent. Moreover, the combination of Meng and Park would have yielded predictable results because both references were directed to charge pump circuits utilizing a multiple-well structure incorporating the same set of circuit components and operating under the same set of parameters.

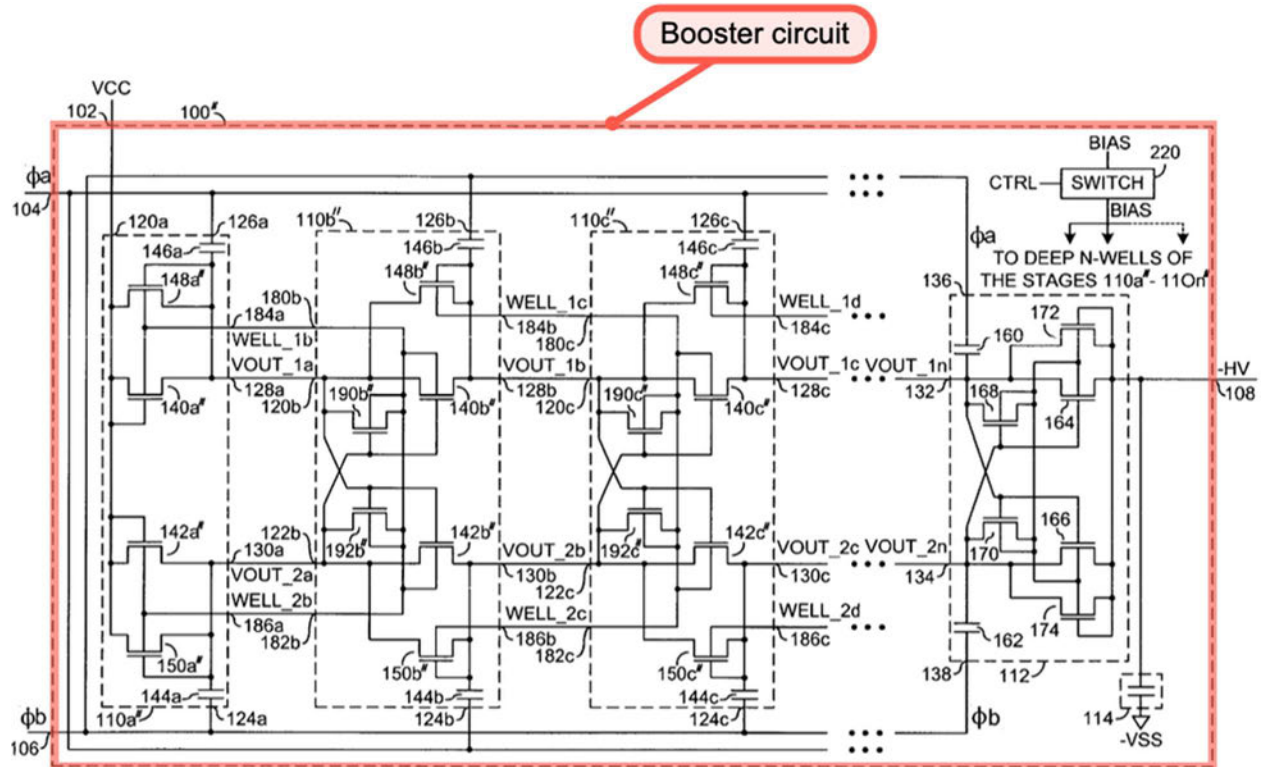
129. Finally, it is my opinion that Meng, Park, and the '557 patent are directed to the same field of endeavor, namely, the design of charge pump circuits that apply a well bias potential to the well regions of a multiple-well structure. EX1001, Abstract, 1:6-7; EX1006, 1:7-10, 7:5-14, 7:49-56; EX1007, Abstract.

C. Claim 1

1. 1[pre]: A booster circuit comprising:

130. If the preamble is deemed to be limiting, it is my opinion that Meng discloses 1[pre] for the reasons I provided in Ground 2. *See* §X.B.1 above. Meng

also discloses, in my opinion, an alternative embodiment shown in Figure 5 below that is a booster circuit. EX1006, Fig. 5.



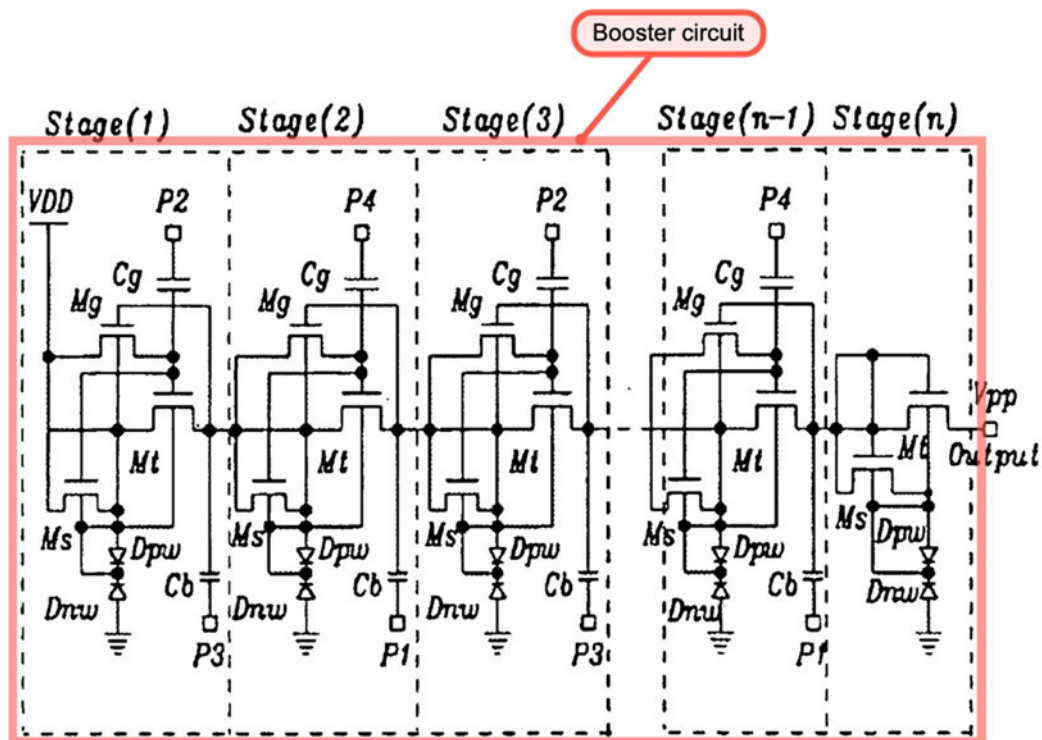
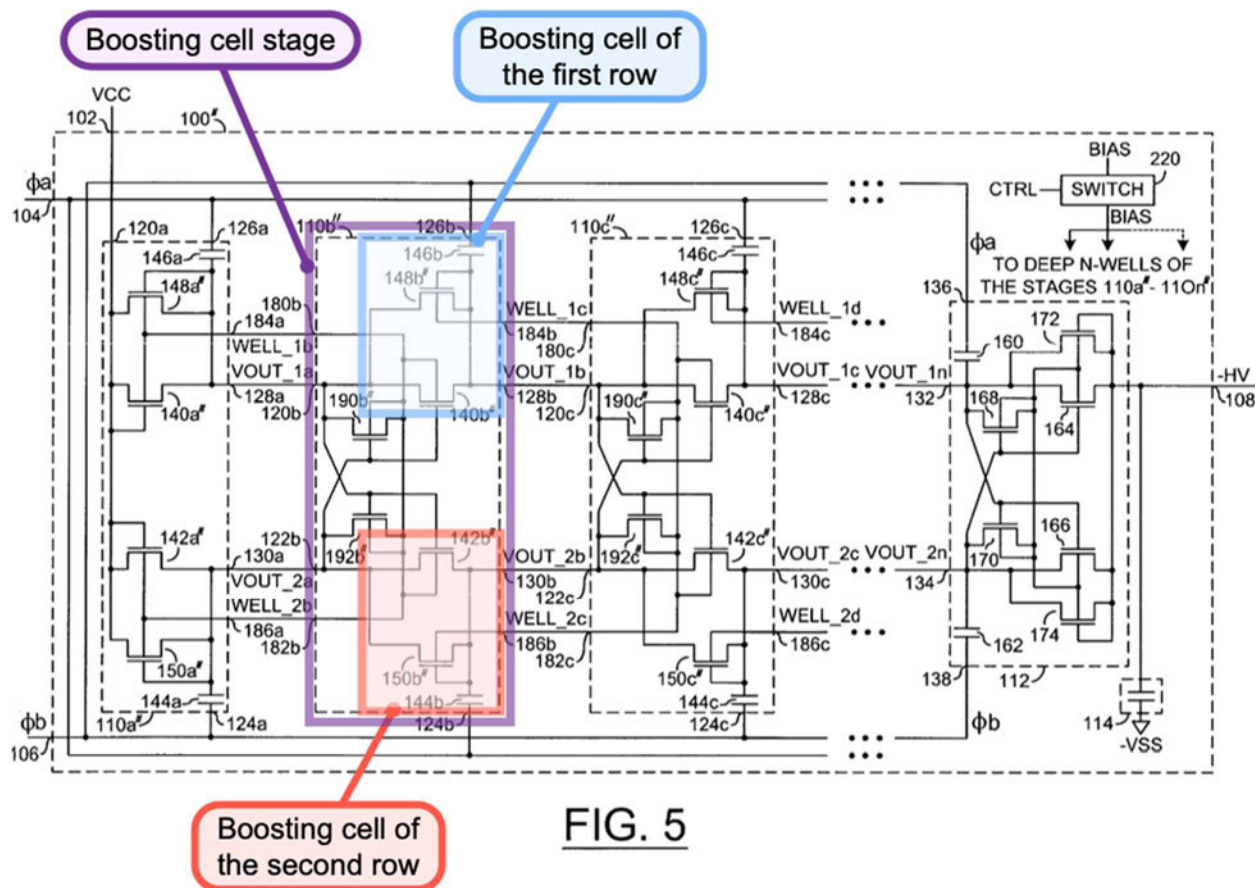


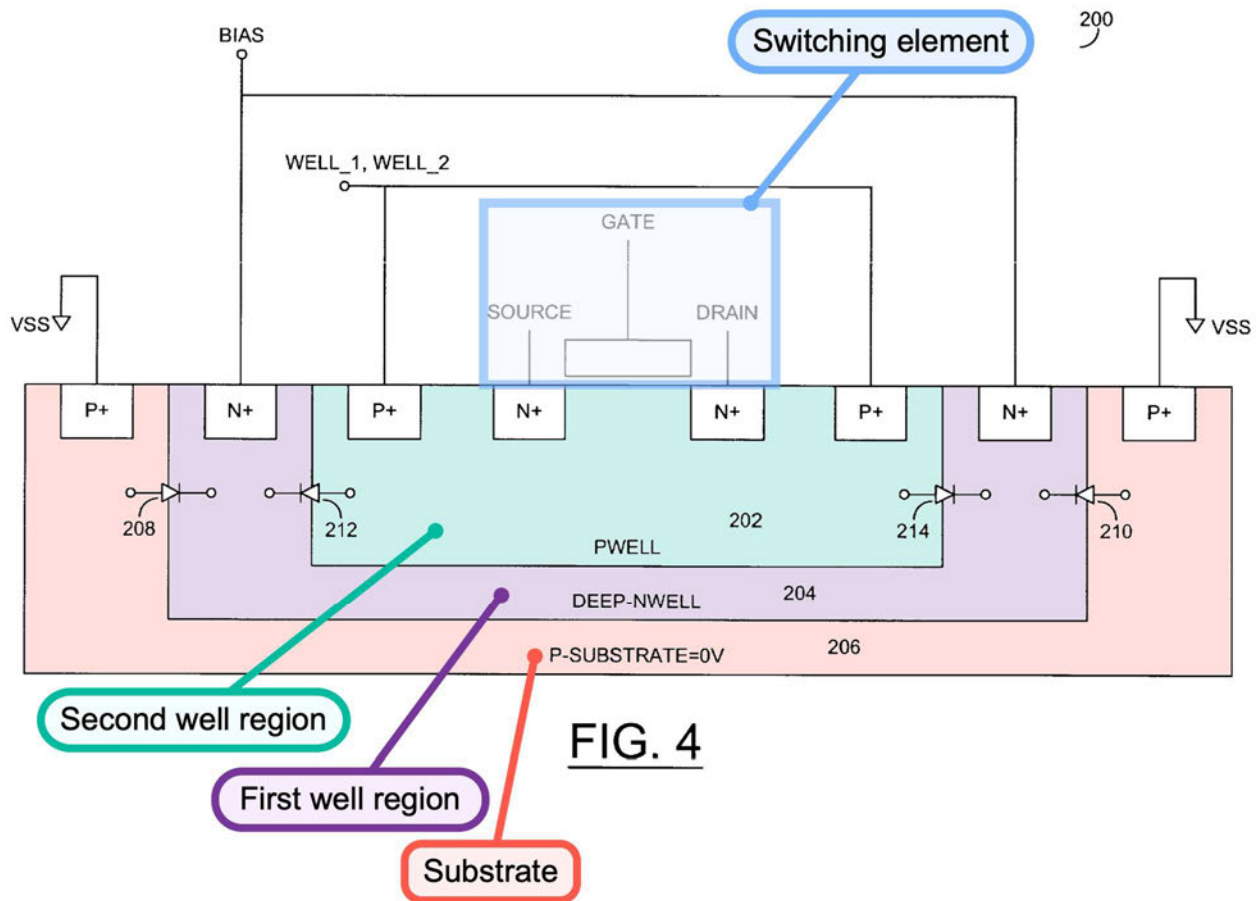
FIG. 7

2. 1[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region,

132. In my opinion, Meng discloses claim limitation 1[a] for the reasons I provided in Ground 2. See §X.B.2 above. In my opinion, Meng discloses an alternative embodiment in Figure 5 that “comprise[s] a number of circuits 110”a-110”n,” with each circuit representing a “stage” that comprises two “*boosting cells*.” EX1006, 7:49-52. As illustrated with annotations in Meng’s Figure 5 below, in the *i*-th **boosting cell stage** 110”*i*, the **top boosting cell** includes transistors 140”*i* and 148”*i* and capacitor 146*i*, and the **bottom boosting cell** includes transistors 142”*i* and 150”*i* and capacitor 144*i*. EX1006, Fig. 5, 7:63-65.



133. Figure 4, shown below, provides a cross-sectional illustration of a transistor in the boosting cells in Meng’s alternative embodiment. EX1006, 7:58-61 (“The transistors [shown in the boosting stage of Fig. 5] may be implemented as one or more deep N-well NMOS transistors as shown in FIG. 4.”). According to Meng, the transistors in each boosting cell “may have a *P-well region* ..., a *deep N-well region* ..., and a *P-substrate region*[.]” EX1006, 7:5-10.



134. In my opinion, Park also discloses claim limitation 1[a]. Park discloses a booster circuit comprising a series of “pumping stages,” which are “boosting cells” because they output a voltage that is greater in magnitude than the input. EX1007, 5:37-45 (“[The booster circuit] includes a plurality of stages [*i.e.*, boosting cells] each having the same formation as represented by the first stage. The input to the first stage is the power supply voltage V_{dd} , and ... [t]he output of the final stage produces a voltage V_{pp} that has been pumped up to a higher voltage than the power supply voltage.”). Park teaches, in my opinion, that “[e]ach pumping stage is formed in its own P-well [*i.e.*, second-conductivity type second well region] and deep N-

well [*i.e.*, first-conductivity type first well region].” EX1007, 5:22-25. Figure 9, shown below, provides a cross-sectional illustration of the switching elements of a boosting cell. EX1007, Fig. 9. According to Park, “[t]he MOS devices Mt and Mg [sic] [*i.e.*, Mt and Ms are switching elements of a boosting cell] are shown in a *P-well* within the *deep N-well* of a stage of the charge pump residing on a *P-substrate*.” EX1007, 6:32-34.

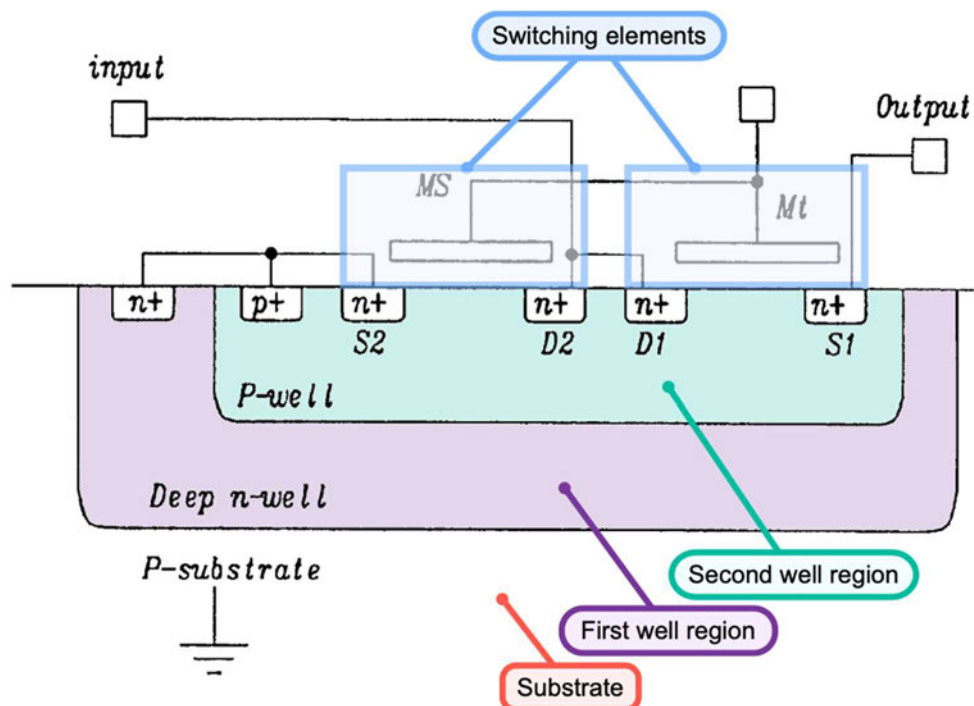


FIG. 9

3. 1[b]: and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal;

135. In my opinion, Meng discloses claim limitation 1[b] for the reasons I provided in Ground 2. See §X.B.3 above. In my opinion, Meng’s alternative

embodiment also discloses claim limitation 1[b]. As I discussed in connection with claim limitation 1[a], it is my opinion that Meng's alternative embodiment illustrated in Figure 5 discloses switching elements in both "the first well region" (*i.e.*, DEEP-NWELL 204) and "the second well region" (*i.e.*, PWELL 202). EX1006, 7:5-10, Fig. 4. Also as I discussed in connection with claim limitation 1[a], the "transistors [in Meng's alternative embodiment shown in Fig. 5] may be implemented as one or more deep N-well *NMOS transistors*," which transfer charges from a "first terminal" (*e.g.*, source) to a "second terminal" (*e.g.*, drain). EX1006, 7:58-61. For example, transistor 140c ("a **switching element**") in Figure 5 shown below is designed to transfer charges from input node 120c ("a **first terminal**") to output node 128c ("a **second terminal**"). EX1006, Fig. 5.

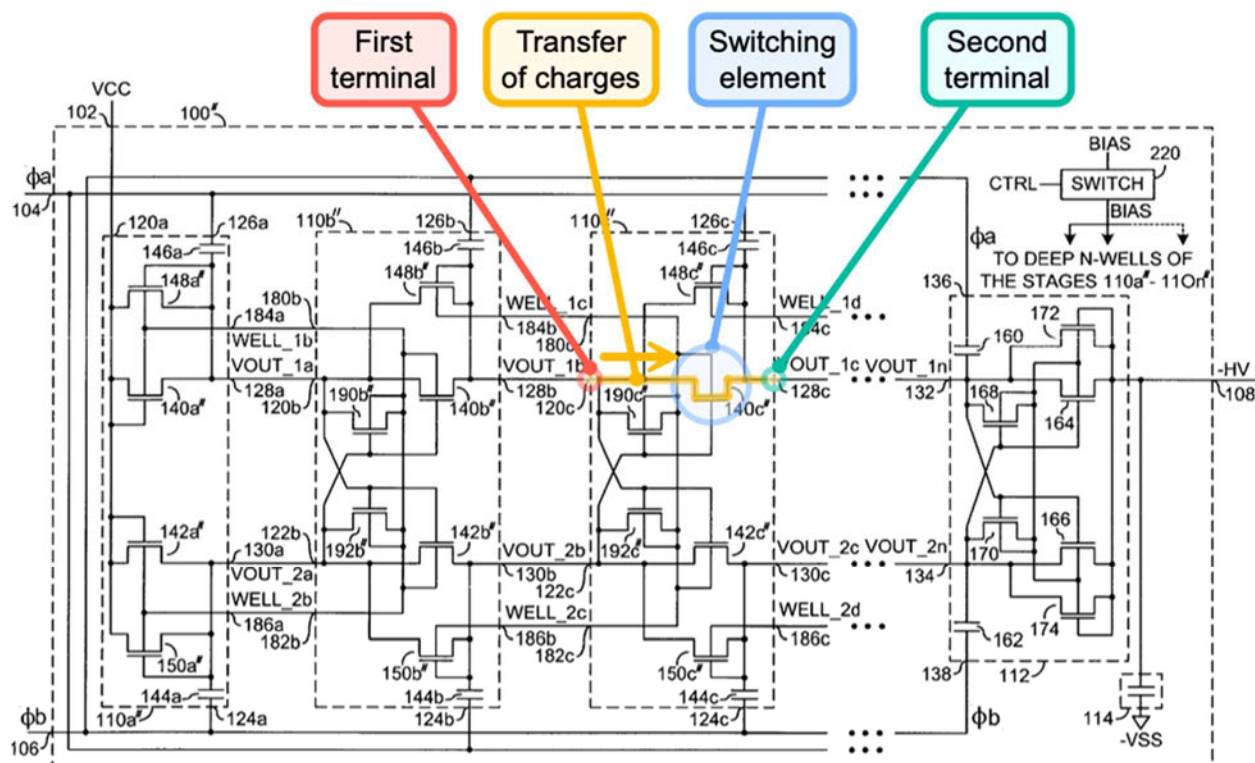


FIG. 5

136. In my opinion, Park also discloses claim limitation 1[b]. As I discussed in connection with claim limitation 1[a], it is my opinion that Park discloses “MOS device[] Mt [*i.e.*, a switching element] ... shown [below in Figure 9 to be] ***in a P-well within the deep N-well*** of a stage of the charge pump residing on a P-substrate.” EX1007, 6:32-34.

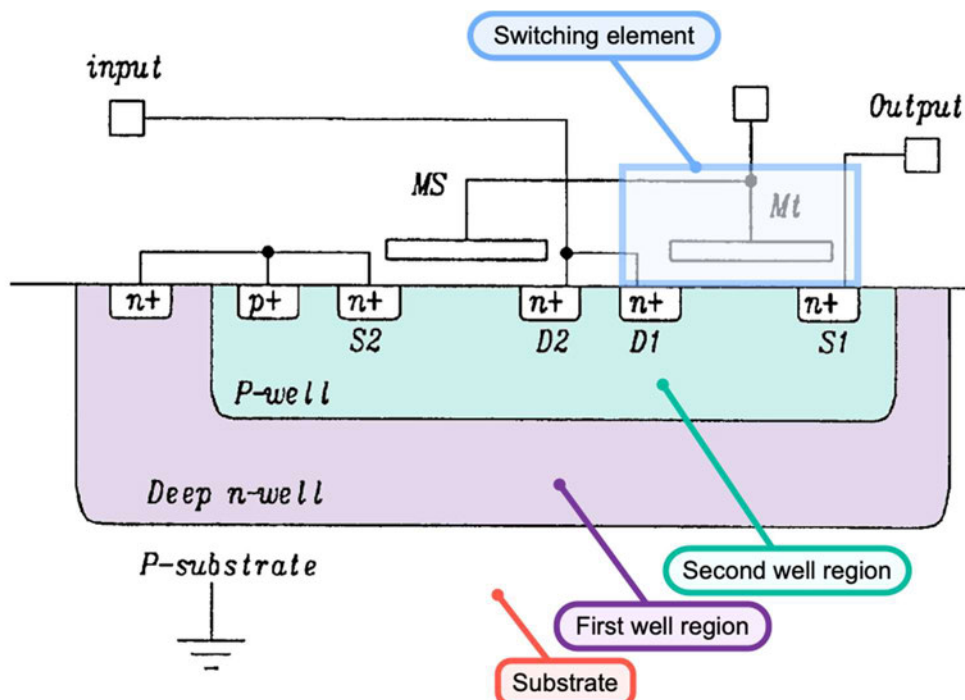


FIG. 9

137. Moreover, according to Park, the MOS device Mt is “a *charge transfer MOS device*” that transfers charges between a first and second terminal. EX1007, 5:27-33. The switching element Mt and its corresponding first and second terminals is shown below in Figure 9. EX1007, Fig. 9.

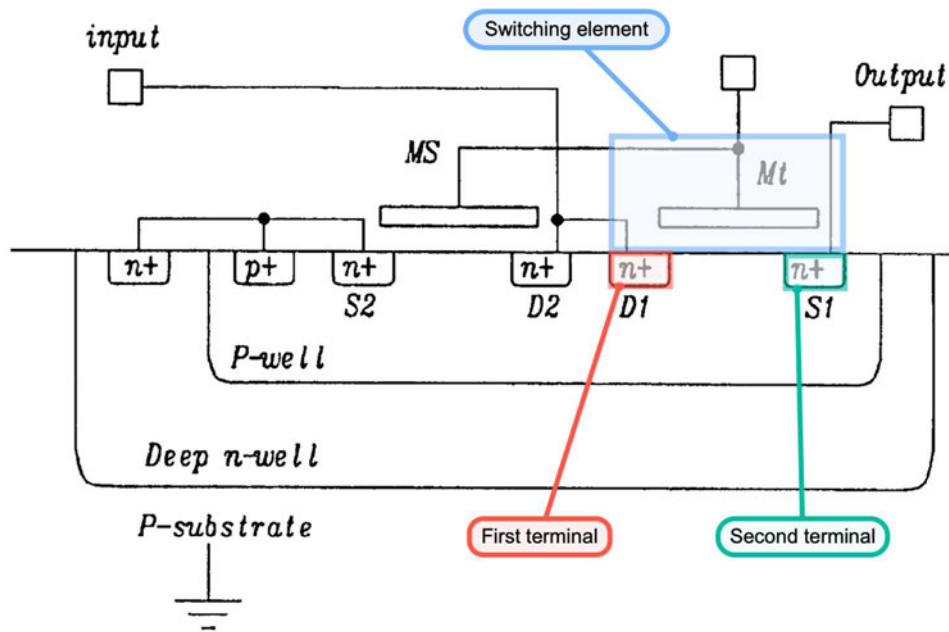
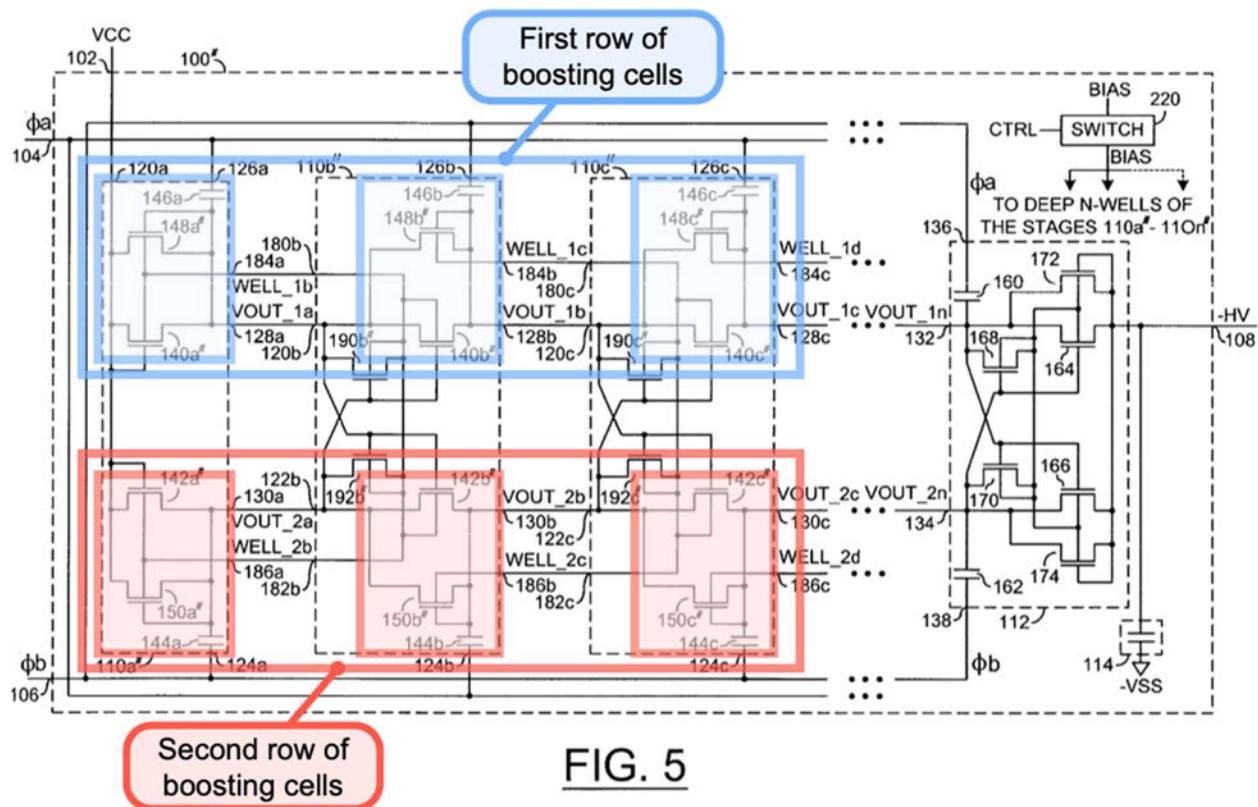


FIG. 9

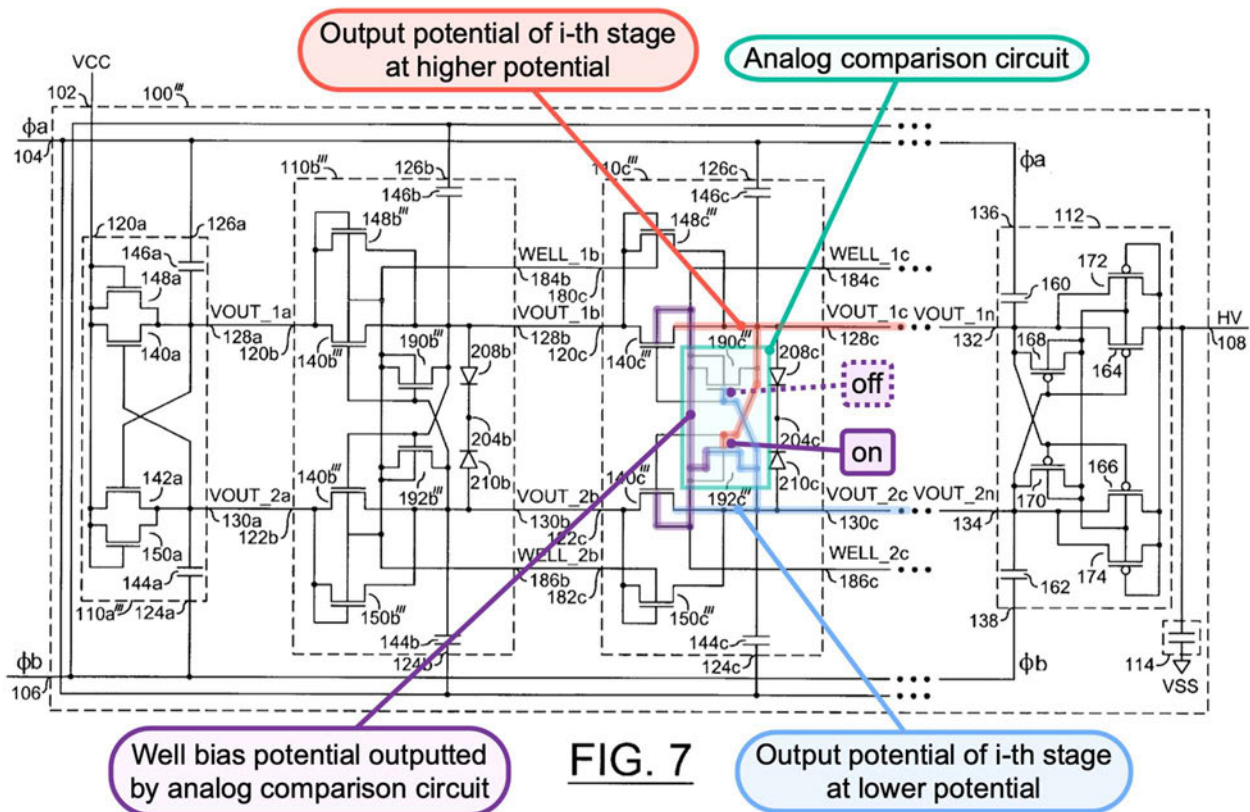
4. 1[c]: a first boosting cell row including $N \geq 1$ of the boosting cells; a second boosting cell row including $M \geq 1$ of the boosting cells; and

138. In my opinion, Meng discloses claim limitation 1[c] for the reasons I provided in Ground 2. See §X.B.4 above. In my opinion, Meng's alternative embodiment illustrated in Figure 5 also discloses claim limitation 1[c]. Figure 5, shown below, illustrates in my opinion "a **first boosting cell row**" including three stages of boosting cells ($N=3$) and "a **second boosting cell row**" also including three stages of boosting cells ($M=3$). EX1006, Fig. 5.



5. 1[d]: at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row,

139. In my opinion, Meng discloses claim limitation 1[d]. As illustrated with annotations in Figure 7 below, it is my opinion that Meng discloses an **analog comparison circuit** for outputting a **well bias potential** generated by the output potentials of the i -th boosting cell stage of the first and second rows (**red** and **blue**, respectively). EX1006, Fig. 7.



140. The analog comparison circuit, as shown above in Figure 7, comprises, in my opinion, two cross-coupled NMOS transistors, elements 190^{'''i} and 192^{'''i}, with inputs that correspond to the output potentials of the *i*-th stage of the first and second boosting cell rows, respectively. EX1006, Fig. 7; *id.*, 9:17-28 (“The signal VOUT_1i may be presented at ... a source of the transistor 190^{'''i}, a gate of the transistor 192^{'''i} [...] ... The signal VOUT_2i may be presented at ... a gate of the transistor 190^{'''i}, a source of the transistor 192^{'''i} [...]”). As I discussed above in §VI.D, for any given stage, one row will have an output that has a higher potential than the other due to the alternating clock signals that are applied to the boosting cells of that stage. §VI.D, *supra*. Whichever of the two NMOS transistors in the analog

comparison circuit 190*"i* and 192*"i* has the higher potential applied to its gate is the transistor that switches on and outputs a well bias potential; the opposing NMOS transistor in the analog comparison circuit remains off thereby blocking any charge transmission. EX1006, 9:9-10 (“The ***bias signals*** WELL_1*i* and WELL_2*i* may be ***generated by*** the transistors 190*"i* and 192*"i* [*i.e.*, an ***analog comparison circuit***].”). The NMOS transistor that switches on does so because the voltage difference between the gate and source (*i.e.*, the terminal with the lower potential) is greater than the threshold voltage; the opposing NMOS transistor remains off because the voltage difference between the gate and the source less than zero.

141. Given that the NMOS transistors 190*"i* and 192*"i* have gates that are cross-coupled to the output potential of the opposite boosting cell row (VOUT_1*i* or VOUT_2*i*), one of the NMOS transistors will have a higher potential applied to its ***gate***, and therefore will be switched on due to its gate being cross-coupled to an opposing boosting cell row that has a ***higher*** output potential (*e.g.*, VOUT_1*i*). EX1006, Fig. 7. The NMOS transistor that is switched on will have an ***input*** that is the ***lower*** boosting stage output potential (*e.g.*, VOUT_2*i*), which means that the well bias potential that is outputted by the analog comparison circuit is ***generated by*** the ***lower*** of the two boosting stage output potentials (*i.e.*, VOUT_1*i* and VOUT_2*i*). EX1006, Fig. 7. Meng therefore teaches, in my opinion, an analog comparison circuit (*i.e.*, transistors 190*"i* and 192*"i*) for outputting a well bias potential (*i.e.*,

bias signals WELL_1*i* and WELL_2*i*) generated by the output potentials of the boosting cells of the first and second boosting cell rows (*i.e.*, signals VOUT_1*i* and VOUT_2*i*).

142. It is my opinion that Meng teaches, in an alternative embodiment, an analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cells of the first and second rows. As illustrated with annotations in Figure 5 below, Meng discloses, in my opinion, an **analog comparison circuit** comprising transistors 190"*i* and 192"*i* for outputting a **well bias potential** generated by the output potentials of the *i*-th boosting stage of the first and second rows (**red** and **blue**, respectively). EX1006, Fig. 5. In my opinion, the cross-coupled transistors 190"*i* and 192"*i* operate in the same manner as the transistors 190'"*i* and 192'"*i* described above with respect to the embodiment illustrated in Figure 7. For the analog comparison circuit identified below in Figure 5, one of the transistors 190"*i* and 192"*i* will switch on (*i.e.*, the transistor with a gate that is cross-coupled to the boosting cell row with the higher potential), thereby outputting a well bias potential. EX1006, Fig. 5; *see also id.*, 8:16-18 ("Where a stage 110"*i* is any one of the stages 110"*b*-110"*n*, at each stage 110"*i*, the **bias signals** WELL_1*i* and WELL_2*i* may be **generated by** the transistors 190"*i* and 192"*i* [*i.e.*, an **analog comparison circuit**]."). And as I discussed above with respect to the embodiment illustrated in Figure 7, it is my opinion that the analog comparison circuit comprising

143. It is my opinion that, to the extent there is any argument that Meng does not disclose claim limitation 1[e], it is rendered obvious by Meng in view of Park. Specifically, Meng, modified to apply the well bias potential outputted by the analog



- 6.**

143. It is my opinion that, to the extent there is any argument that Meng does

comparison circuit to the first well region as taught by Park, meets, in my opinion, claim limitation 1[e].

144. For the reasons I provided in connection with claim limitation 1[d], it is my opinion that Meng discloses an analog comparison circuit that outputs a well bias potential. See §XI.C.5 above. Park teaches applying a well bias potential to the first well region (*i.e.*, deep N-well) of a boosting cell. EX1007, Figs. 7, 9, 6:38-40, 6:53-56. As illustrated with annotations in Figure 9 below, Park teaches that “[t]he source S2 [*i.e.*, node that outputs a well bias potential] of the auxiliary MOSFET device Ms is *connected to both the P-well and the deep N-well* [*i.e.*, second and first well regions, respectively].” EX1007, Fig. 9, 6:38-40.

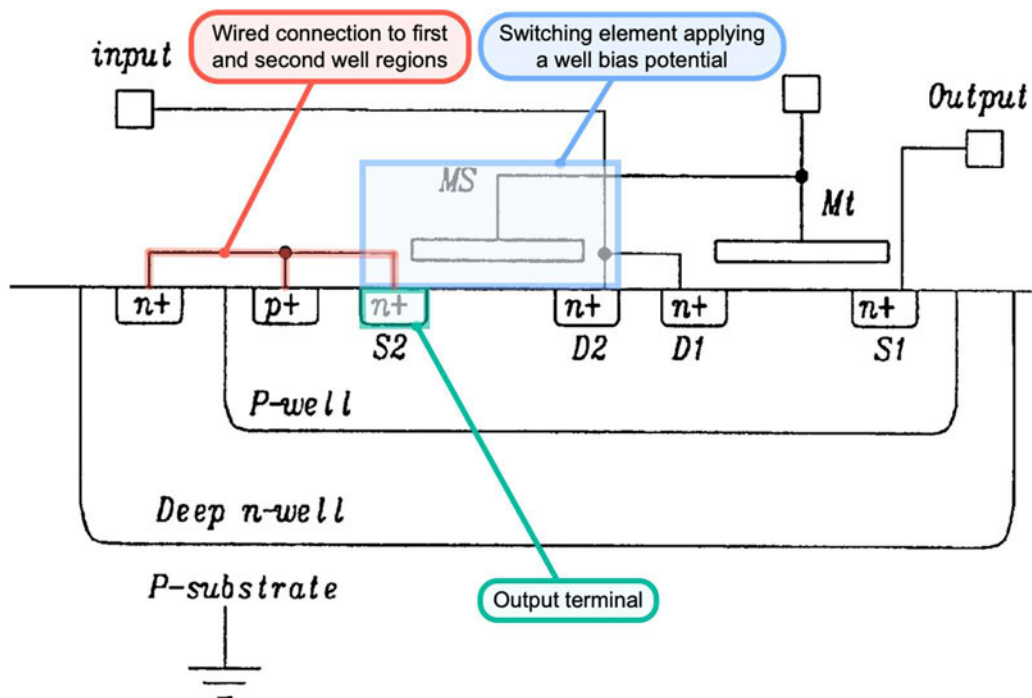
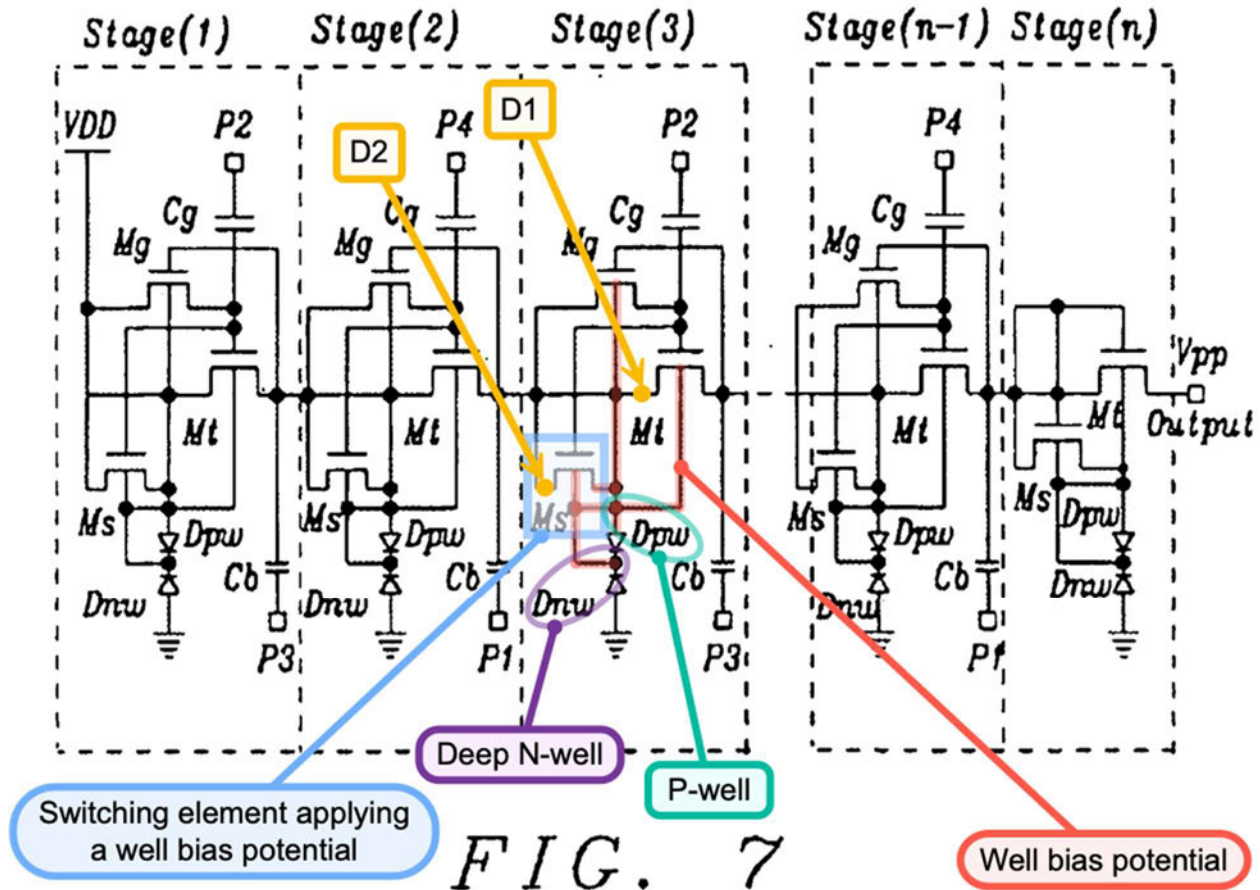


FIG. 9

145. Another view of Park’s teaching is presented below in Figure 7⁴, which illustrates how “[t]he *input voltage* at the drains D1 and D2 *of* the charge transfer MOS device Mt and *the auxiliary MOS device Ms*, respectively, *is coupled to the P-well and the deep N-well* by the auxiliary MOS device Ms.” EX1007, Fig. 7, 6:53-56.

⁴ The node to the immediate upper left of the label “Mt” in Park’s Figure 7 is, in my opinion, erroneously placed and should be removed. Park does not reference this erroneously placed node in its specification. Further, it is my opinion that a POSITA would have understood that the inclusion of this erroneously placed node would result in the transistor Ms being turned off at all times and that its inclusion would render the circuit taught by Park unworkable. If the transistor Ms remained off at all times then the transistor Mt would not receive the necessary well biasing which would in turn lead to forward biasing of the source/drain of Mt and the well regions of Mt. This would prevent the proper functioning of the circuit taught by Park and undermine its teachings. Of course, a POSITA would never add an always OFF transistor into a circuit since it merely adds area while providing no benefit.



146. As I discussed in connection with claim limitation 1[d], it is my opinion that Meng discloses two embodiments, illustrated in Figures 5 and 7, that include an analog comparison circuit that outputs a well bias potential generated by the lower of the two boosting stage output potentials (*i.e.*, VOUT_{1i} or VOUT_{2i}). See §XI.C.5 above. As shown in Meng's Figures 5 and 7 below, it is my opinion that the well bias potential outputted by the analog comparison circuit is applied to the switching elements included in the *i*-th boosting cell of the first and second boosting cell rows (*i.e.*, transistors 148"*i* and 150"*i* for Meng's Figure 5, and transistors 140"*i* and 142"*i* for Meng's Figure 7). EX1006, Figs. 5, 7.

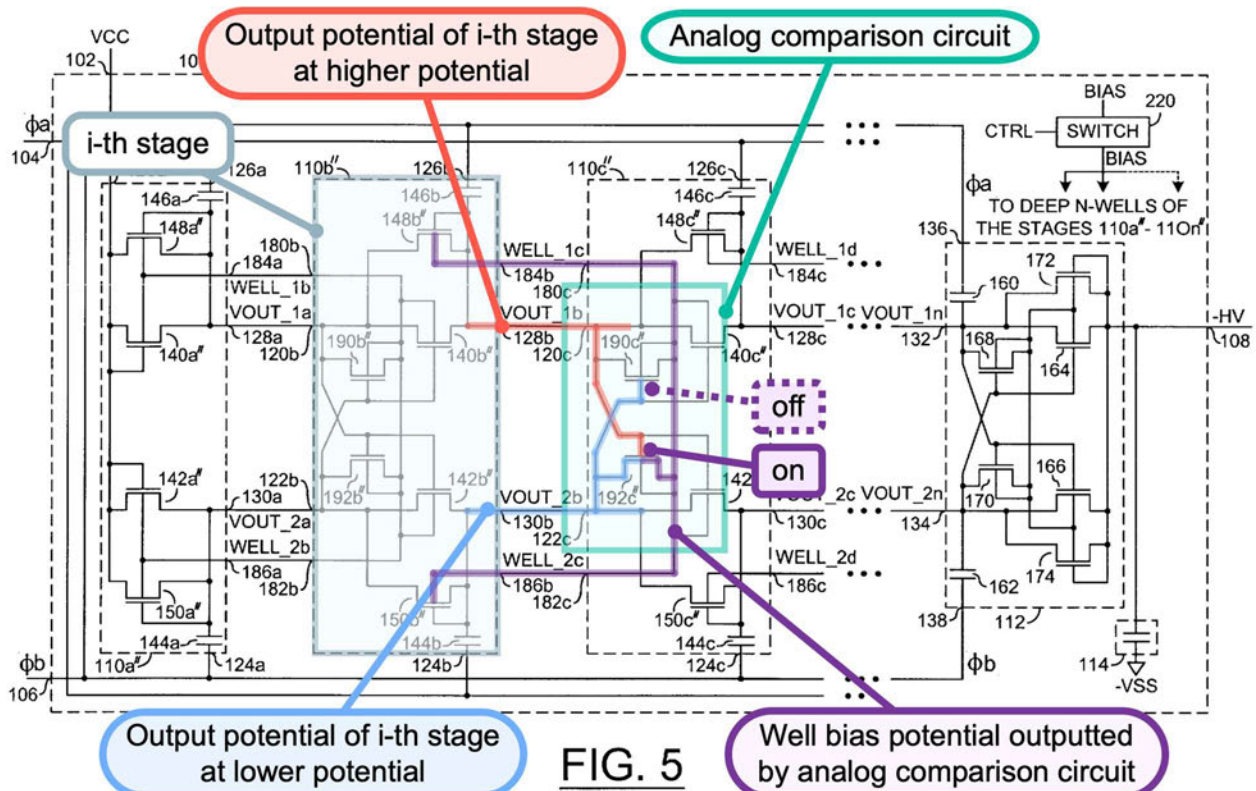


FIG. 5

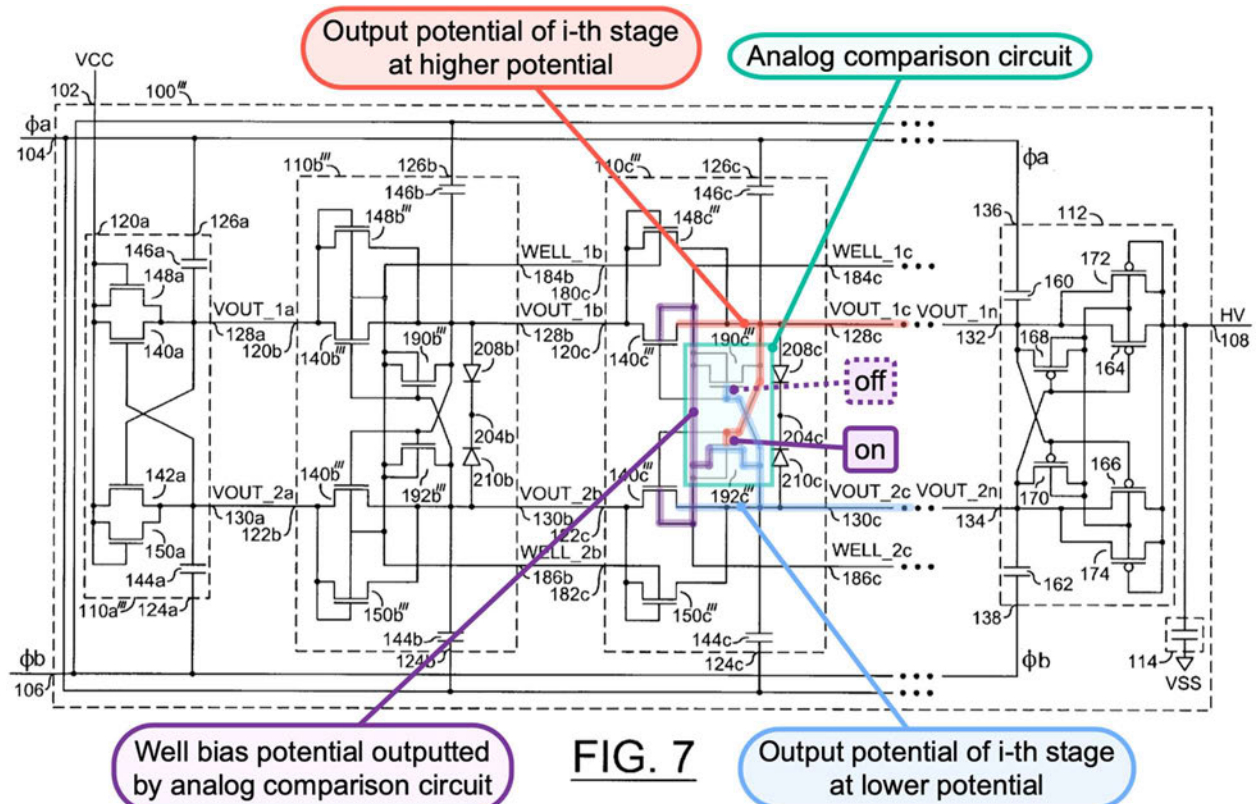
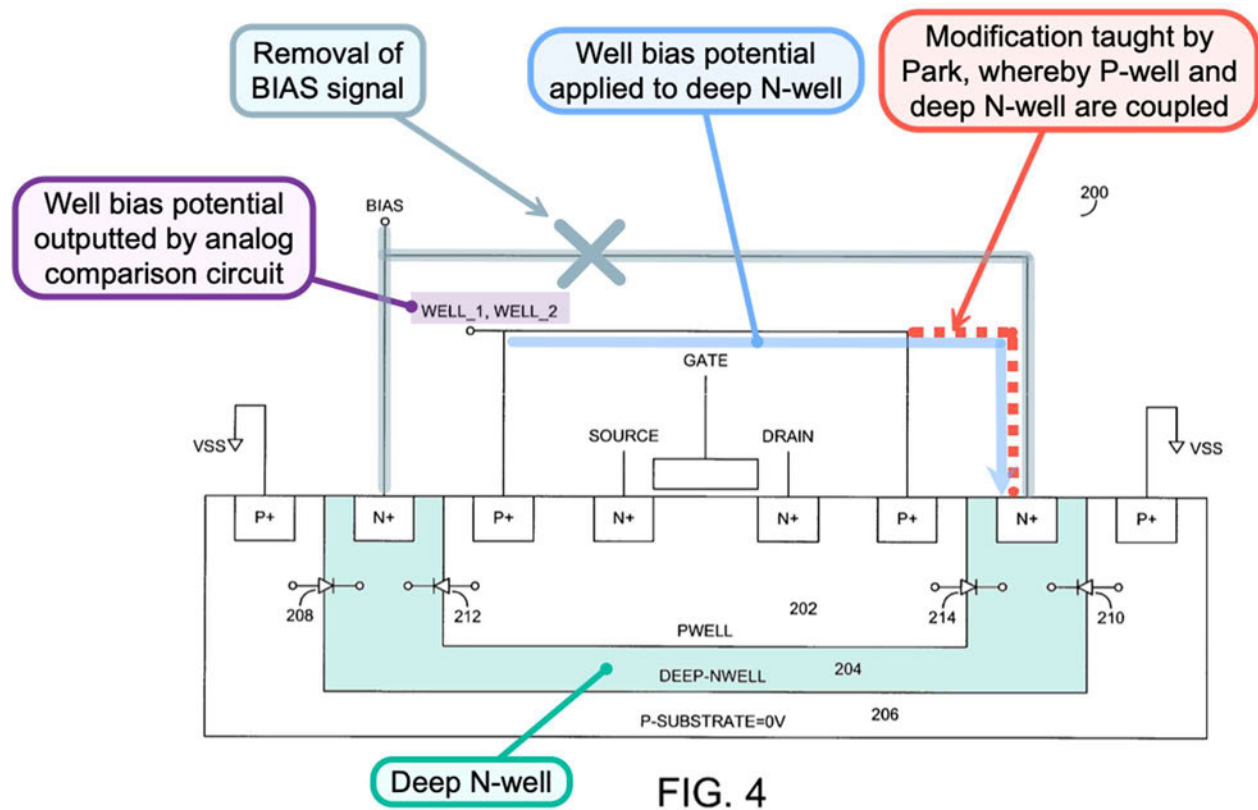


FIG. 7

147. In my opinion, Meng's embodiments in Figure 5 and 7, modified in view of Park, disclose applying a well bias potential (*i.e.*, WELL_1*i* or WELL_2*i*) to the first well region (*i.e.*, deep N-well) of the switching elements included in the at least one boosting cell of the first and second boosting cell rows (*i.e.*, transistors 148"*i* and 150"*i* for Meng's Figure 5, and transistors 140"*i* and 142"*i* for Meng's Figure 7). The modification taught by Park to Meng's embodiments in Figures 5 and 7 is illustrated below in Meng's Figure 4. EX1006, Fig. 4.



D. Claims 2, 3, 9, and 10

148. In my opinion, Meng discloses claims 2, 3, 9, and 10 for the reasons I provided in Ground 2. *See* §§X.C, X.D, X.E, X.F, above, respectively.

- E. Claim 4: The booster circuit of claim 1, wherein the well bias potential is the lower potential out of the output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and the output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.**

149. As I discussed in connection with claim limitation 1[d], it is my opinion that Meng discloses an analog comparison circuit outputting a well bias potential that is the lower potential out of the output potentials of the i -th boosting cells of the first and second rows. *See* §XI.C.5 above.

- F. Claim 5: The booster circuit of claim 1, wherein the second well region and the first terminal are connected to each other so that the second well region and the first terminal have the same potential.**

150. In my opinion, Meng in view of Park discloses claim 5. As I explain above, Meng discloses the booster circuit of claim 1. *See* §XI.C above. Park discloses, in my opinion, a **direct connection** between the second well region (*i.e.*, P-well) and the second terminal of the switching element, as shown below in Park's Figure 9. EX1007, Fig. 9. The direct connection between the first and second terminal via the **switching element** therefore enables, in my view, a direct connection between the first terminal and the second well region such that they have the same potential.

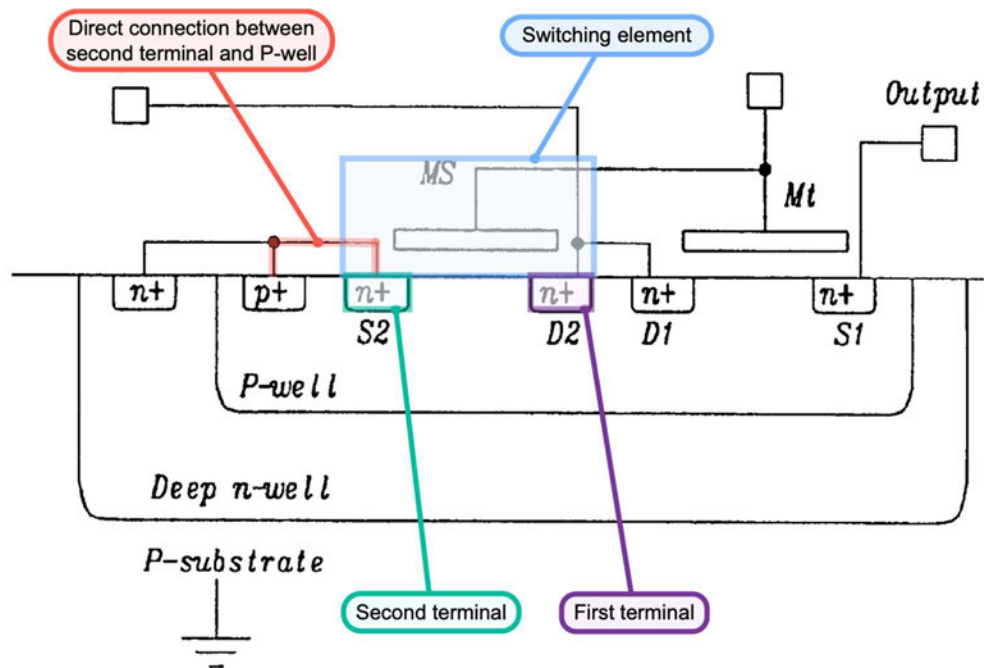


FIG. 9

G. **Claim 6:** The booster circuit of claim 1, wherein the second well region and the first well region are connected to each other so that the second well region and the first well region have the same potential.

151. In my opinion, Meng in view of Park discloses claim 6. As I explain above, Meng discloses the booster circuit of claim 1. See §XI.C above. Park discloses, in my opinion, a **direct connection** between the first well region (*i.e.*, deep N-well) and the second well region (*i.e.*, P-well), as shown below in Park's Figure 9, so that the second well region and the first well region have the same potential. EX1007, Fig. 9.

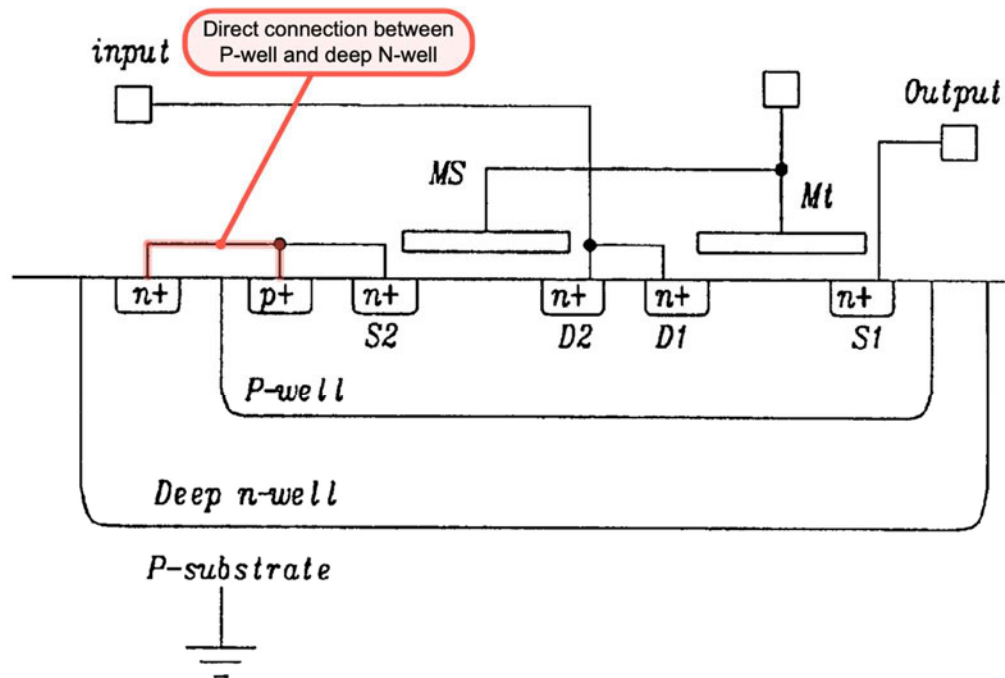


FIG. 9

H. Claim 7

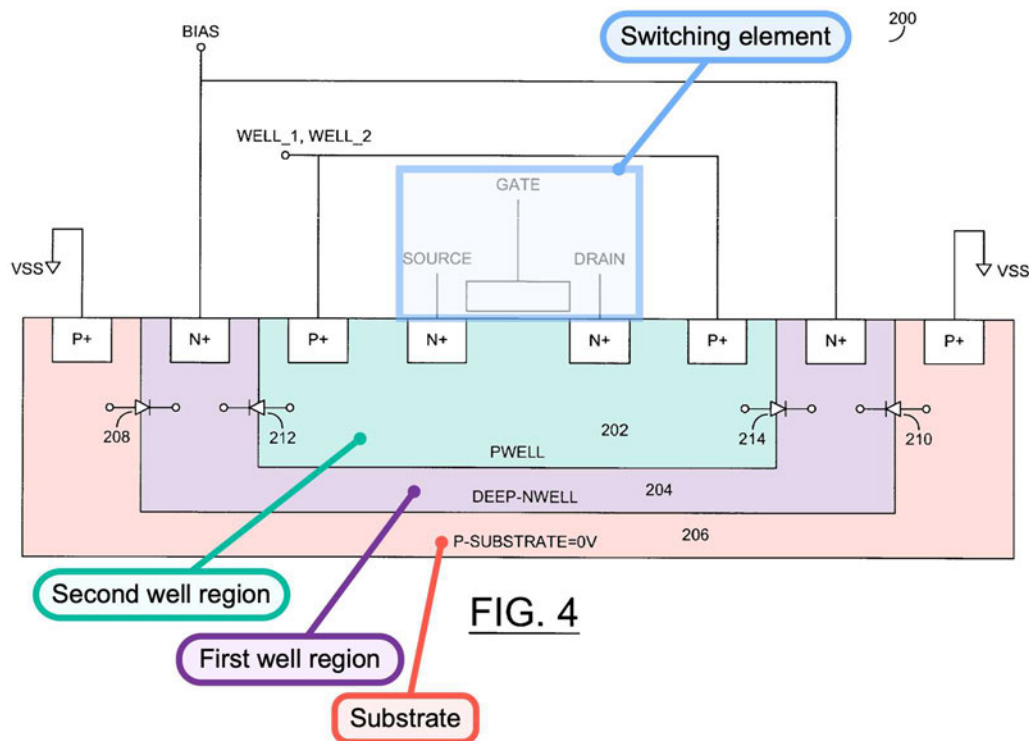
1. 7[pre]: The booster circuit of claim 1, wherein

152. In my opinion, both Meng and Park disclose 7[pre] as I discussed in connection with claim 1. See §XI.C above.

2. 7[a]: the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and

153. In my opinion, Meng discloses claim limitation 7[a]. As I discussed in connection with claim limitation 1[d], Meng discloses an analog comparison circuit comprising transistors 190*i* and 192*i*. §XI.C.5, *supra*; EX1006, Fig. 5. And according to Meng, the analog comparison circuit's transistors 190*i* and 192*i* “may

be implemented as one or more *deep N-well* NMOS transistors as shown in FIG. 4.” EX1006, 7:58-61. The cross-section of a deep N-well NMOS transistor, shown below in Meng’s Figure 4, confirms that the analog comparison circuit comprising the NMOS transistors 190*i* and 192*i* has “a P-well region 202 [*i.e.*, second-conductivity type second well region] ..., a deep N-well region 204 [*i.e.*, first-conductivity type first well region] ..., and a P-substrate region 206[.]” EX1006, Fig. 4, 7:5-10. Meng therefore discloses, in my opinion, at least one analog comparison circuit that has a first well region on a substrate, a second well region in the first well region, and at least one switching element (*i.e.*, transistors 190*i* and 192*i*) in the first or second well regions.



I. Claim 8

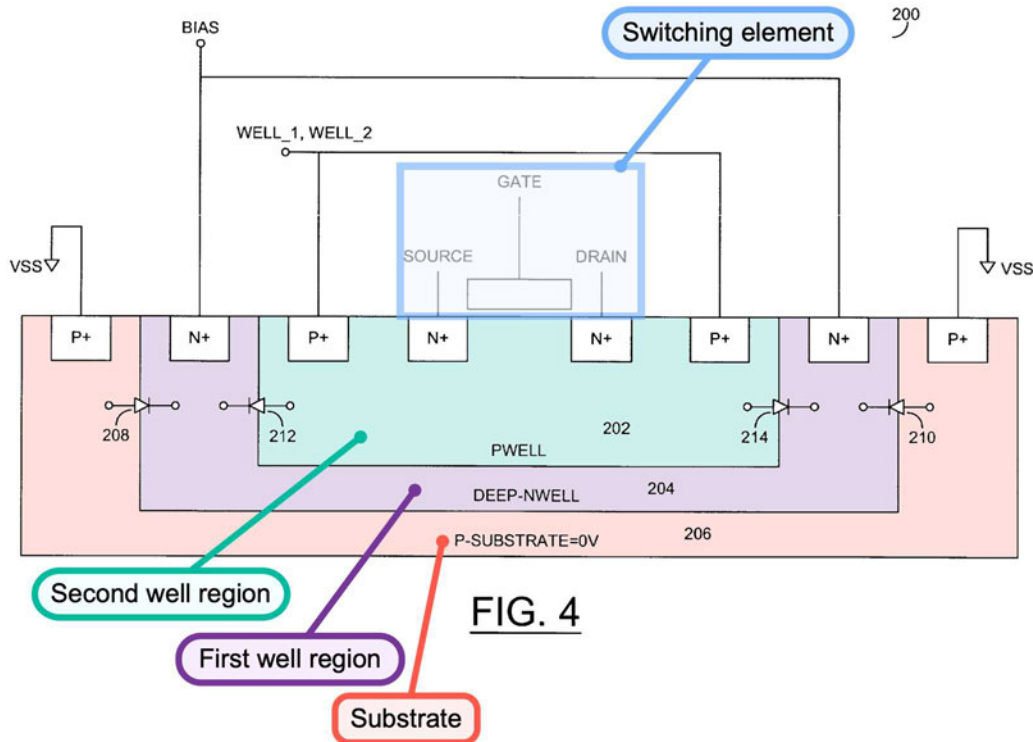
1. 8[pre]: The booster circuit of claim 1, wherein

155. In my opinion, both Meng and Park disclose 8[pre] as I discussed in connection with claim 1. *See* §XI.C above.

2. 8[a]: the at least one analog comparison circuit has a first-conductivity type first well region on the substrate, a second-conductivity type second well region in the first well region, and at least one switching element in the first well region or the second well region, and at least one analog comparison circuit is provided for the first and second boosting cell rows, and

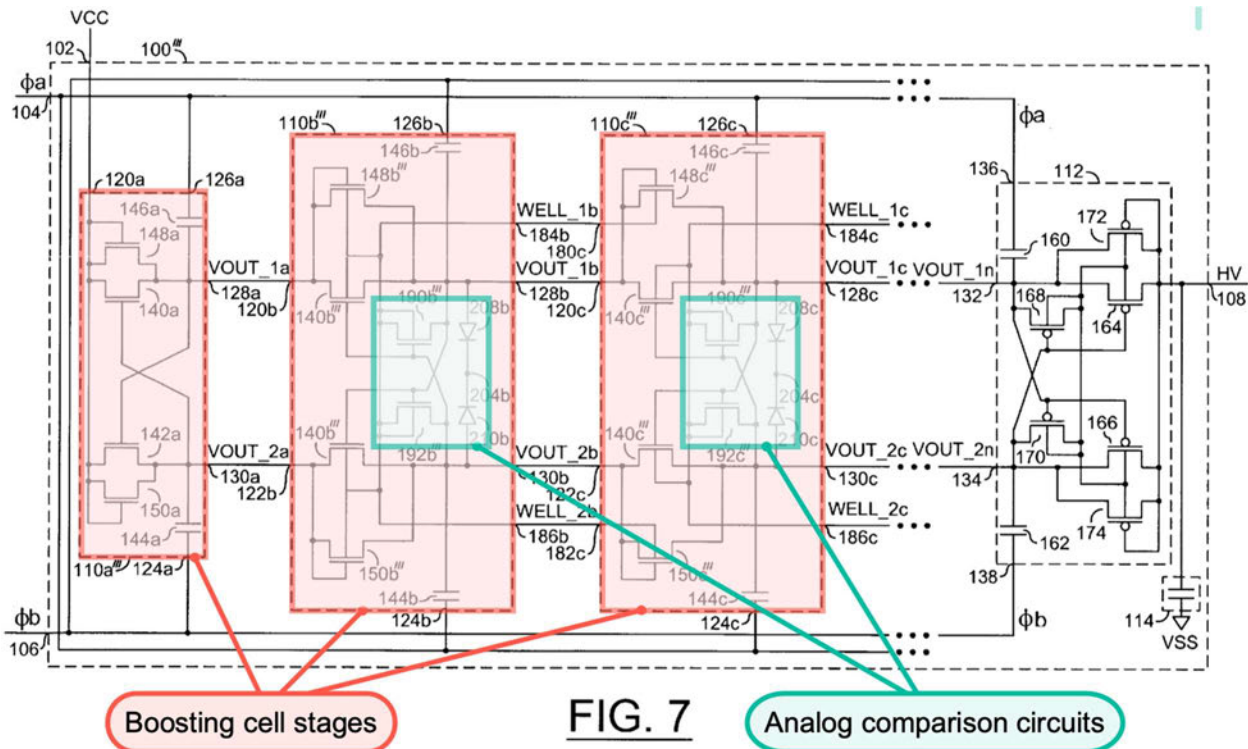
156. As I discussed in connection with claim limitation 1[d], Meng discloses, in my opinion, at least one analog comparison circuit that is provided for the first and second boosting cell rows. *See* §XI.C.5 above. Moreover, according to Meng, the analog comparison circuit's transistors 190*"i* and 192*"i* “may be implemented as one or more *deep N-well* NMOS transistors as shown in FIG. 4.” EX1006, 8:61-65. The cross-section of a deep N-well NMOS transistor, shown below in Meng's Figure 4, confirms in my opinion that the analog comparison circuit comprising the NMOS transistors 190*"i* and 192*"i* has “a P-well region 202 [*i.e.*, second-conductivity type second well region] ..., a deep N-well region 204 [*i.e.*, first-conductivity type first well region] ..., and a P-substrate region 206[.]” EX1006, Fig. 4, 7:5-10. Meng therefore discloses, in my opinion, at least one analog comparison circuit that has a first well region on a substrate, a second well region in

the first well region, and at least one switching element (*i.e.*, transistors 190*"i* and 192*"i*) in the first or second well regions.



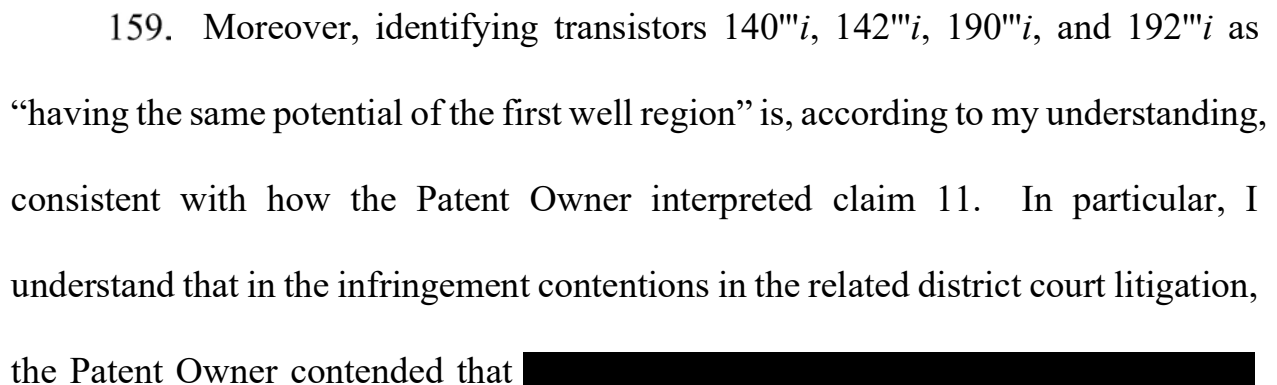
3. 8[b]: the at least one analog comparison circuit is provided one every arbitrary number of boosting cell stages.

157. In my opinion, Meng discloses claim limitation 8[b]. As shown with annotations in Figure 7 below, Meng discloses, in my opinion, a booster circuit that includes two **analog comparison circuits** for at least three **boosting cell stages**, *i.e.*, an “arbitrary number of boosting cell stages.” EX1006, Fig. 7. There is therefore, in my opinion, an analog comparison circuit provided for an arbitrary number of boosting cell stages in the embodiment shown in Meng’s Figure 7.



- J. **Claim 11:** The booster circuit of claim 1, wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region.

158. In my opinion, Meng discloses claim 11. In Figure 7, shown below, Meng discloses switching elements of the first and second boosting cell rows and an analog comparison circuit that *share a common node 204i*, with “*node 204i* [being] the *deep N-well region* [i.e., first well region] of the transistors 140^{'''i}, 142^{'''i}, ... 190^{'''i}, and 192^{'''i}.” EX1006, 9:6-8. As identified by the annotations to Figure 7 below, transistor 140^{'''i} is the switching element of the first boosting cell row, transistor 142^{'''i} is the switching element of the second boosting cell row, and transistors 190^{'''i} and 192^{'''i} form the analog comparison circuit. EX1006, Fig. 7. And Meng teaches transistors 140^{'''i}, 142^{'''i}, 190^{'''i}, and 192^{'''i} (i.e., switching



EX1008 at 44.

160. Accordingly, based on at least the Patent Owner's apparent interpretation, it is my opinion that Meng discloses at least one switching elements and at least one analog comparison circuit having the same potential of the first well region.

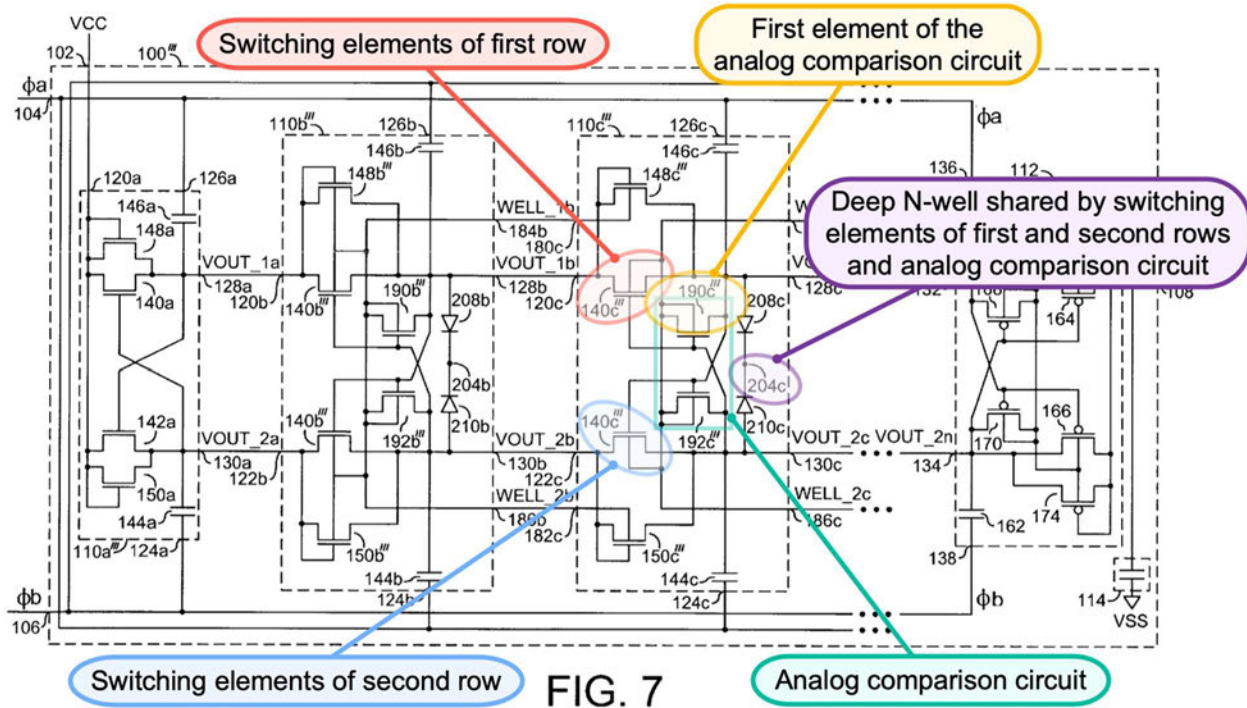
K. Claim 12

1. 12[pre]: The booster circuit of claim 1, wherein

161. In my opinion, both Meng and Park disclose 12[pre] as I discussed in connection with claim 1. *See* §XI.C above.

2. 12[a]: the at least one switching circuit of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

162. As I discussed in connection with claim 11, it is my opinion that Meng discloses a switching circuit (*i.e.*, switching element 140"*i*) of the *i*-th boosting cell of the first boosting cell row sharing a common first well region with an analog comparison circuit (*i.e.*, transistors 190"*i* and 192"*i*). *See* §XI.J above. Transistor 190"*i* is, in my opinion, the first element of the analog comparison circuit. EX1006, Fig. 7.



3. 12[b]: the at least one switching circuit of the boosting cell on the i -th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

163. As I discussed in connection with claim 11, it is my opinion that Meng discloses a switching circuit (*i.e.*, switching elements 142^{'''i} and 150^{'''i}) of the i -th boosting cell of the second boosting cell row sharing a common first well region with an analog comparison circuit (*i.e.*, transistors 190^{'''i} and 192^{'''i}). See §XI.J above. Transistor 192^{'''i} is, in my opinion, the second element of the analog comparison circuit. EX1006, Fig. 7.

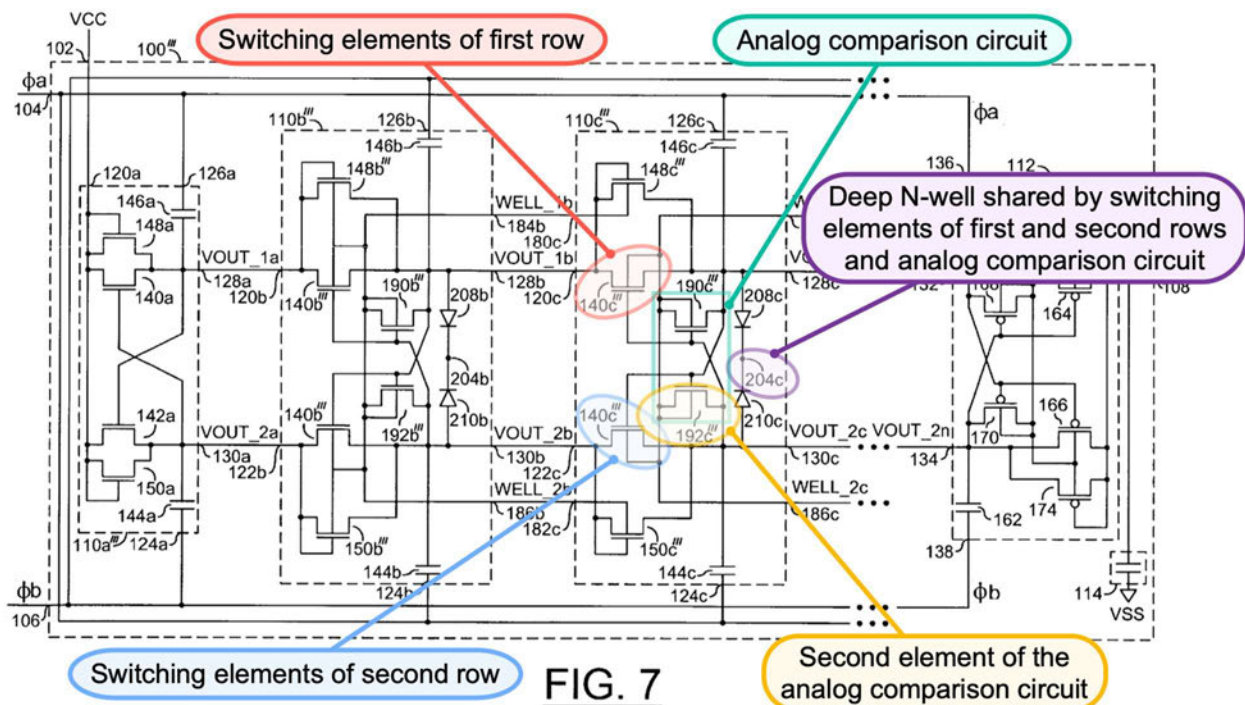


FIG. 7

L. Claim 14

1. 14[pre]: A booster circuit comprising:

164. In my opinion, both Meng and Park disclose 14[pre] as I discussed in connection with 1[pre]. See §XI.C.1 above.

2. 14[a]: boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,

165. As I discussed in connection with claim limitation 1[a], it is my opinion that both Meng and Park disclose boosting cells each having a deep N-well (*i.e.*, first-conductivity type first well region) on a P-type substrate, and a P-well (*i.e.*, second-conductivity type second well region) in the deep N-well. See §XI.C.2 above. And as I discussed in connection with claim limitation 1[b], it is my opinion that

both Meng and Park disclose a switching element in both the deep N-well and P-well. *See* §XI.C.3 above.

3. **14[b]: wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;**

166. As I discussed in connection with claim limitation 1[b], it is my opinion that both Meng and Park disclose switching elements that transfer charges from a first terminal to a second terminal. *See* §XI.C.3 above. And as I discussed in connection with claim limitation 1[e], it is my opinion that both Meng and Park disclose switching elements that are capable of switching on and off in order to transfer or block charges between terminals on opposing sides of the switching element. *See* §XI.C.6 above.

4. **14[c]: a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;**

167. As I discussed in connection with claim limitation 1[c], it is my opinion that Meng discloses two boosting cells rows (*i.e.*, a first and a second boosting cell row) with each boosting cell row including at least one boosting cell stage. *See* §XI.C.4 above.

5. **14[d]: wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first**

boosting cell row and an output potential of the boosting cells of the second boosting cell row.

168. As I discussed in connection with claim limitation 1[d], it is my opinion that Meng discloses an analog comparison circuit that outputs a well bias potential. *See* §XI.C.5 above. As I discussed in connection with claim limitation 1[e], it is my opinion that Meng in view of Park teaches the well bias potential outputted by the analog comparison circuit is applied to the deep N-well (*i.e.*, first well region) of the switching element(s) included in the boosting cell of the first and second boosting cell rows. *See* §XI.C.6 above. And as I discussed in connection with claim limitations 1[d] and 1[e], it is my opinion that the operation of the analog comparison circuit, and by extension the well bias potential, is controlled according to an output potential of the boosting cell of the first row and the output potential of the boosting cell of the second row. *See* §XI.C.5 and §XI.C.6 above.

XII. CONCLUSION

169. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Respectfully submitted,

Date: 29 August 2025

By: Carl Sechen
Carl Sechen, Ph.D.