

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Exhibit A-OB: Omnibus Obviousness Chart

The following chart demonstrates that asserted claims 1, 2, 4, 7, 9, 10, 11, 12, and 14 of U.S. Patent No. 7,777,557 (the '557 patent") are obvious in view of the references discussed in Exhibits A-1 – A-5 and A-X1 – A-X2 alone, or in combination with one or more of the following references (collectively the "Omnibus References"), consistent with the obviousness combinations and rationale set forth in the cover pleading hereto:

- U.S. Pat. No. 6,100,557 ("Hung")
- U.S. Pat. No. 6,952,129 ("Lin '129")
- U.S. Pat. No. 6,121,821 ("Miki")
- U.S. Pat. No. 6,914,791 ("Park '791")
- U.S. Pat. No. 6,175,264 ("Jinbo")
- VLSI-Design of Non-Volatile Memories by G. Campardo, R. Micheloni, and D. Novosel ("Campardo")

As set out below, each limitation was well known in the art and would have been obvious to a person of ordinary skill in the art as it was part of the general knowledge of one of ordinary skill in the art, as shown by the teachings of at least one of the prior art references set forth above. A person of ordinary skill in the art would have been motivated to combine any of these references with at least one or more of the foregoing prior art references for at least the reasons set forth in the cover document of SK hynix's invalidity contentions and/or as further set out in Exhibits A-1 – A-5 and A-X1 – A-X2.

This chart incorporates by reference—for each respective claim and claim limitation of the '557 patent—the exemplary prior art disclosures identified in SK hynix's charts Exhibits A-1, A-2, A-3, A-4, A-5, A-X1, and A-X2. Those disclosures are each incorporated into this chart in this Exhibit A-OB as if fully set forth, but which for brevity are not repeated verbatim below. This chart therefore sets out the additional disclosures from the remaining references described above which, together with such other references incorporated or noted in this chart, render obvious each and every claim limitation of the '557 patent, to the extent such limitation(s) are not anticipated.

The analysis in this chart is based on the apparent claim constructions and interpretations that AMT has advanced to allege infringement of the asserted claims of the '557 patent, as set forth in AMT's infringement contentions served April 2, 2025. Nothing in this chart should be interpreted as SK hynix conceding that AMT's apparent claim constructions and interpretations are correct or supported by intrinsic or extrinsic evidence.

The analysis in this chart is preliminary, and SK hynix's investigation into the invalidity of the asserted claims of the '557 patent is ongoing. SK hynix reserves the right to provide additional theories under which the cited prior art anticipates or renders obvious the asserted claims of the '557 patent, including in response to the receipt of third party discovery currently ongoing and to be produced in this litigation. The citations to specific disclosure of the prior art references in this chart are exemplary, and SK hynix reserves the right to rely on additional disclosures to the same references. SK hynix also reserves the right to offer expert testimony and opinions

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explaining how a person of skill in the art would understand the disclosures of the cited prior art references.

Exemplary Disclosures

1[a] A booster circuit comprising:

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious a booster circuit.

See, e.g.:

Hung at Abstract:

An improved charge pump design is disclosed. This charge pump comprises at least one pumping transistor having a triple well arrangement. This triple pump transistor has a source and a drain region of a first conductive type formed on a first well having an opposite conductive type. A second well having the first conductive type is formed outside of the first well. The source region, first well and second well are set to substantially the same potential. One aspect of this configuration is that the first well forms a semiconductor diode with the drain region. Another aspect of this arrangement is that the body effect of the transistor is reduced. The reduction in body effect reduces the threshold voltage of the transistor. It is found that the above mentioned diode and threshold voltage reduction, singly and in combination, allow the charge pump to operate more efficiently.

Hung, Fig. 1:

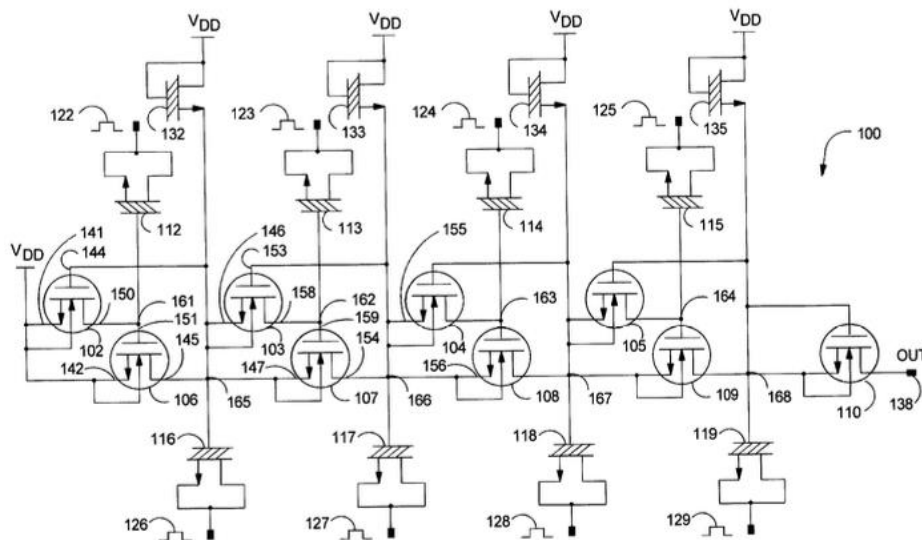


FIG.1

Hung, col. 1:

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A charge pump is a circuit that can generate an output voltage that is higher than the voltage supplied to the charge pump. One of the applications of charge pumps is to develop voltage for erasing and programming some kinds of non-volatile semiconductor memory devices, such as electrical erasable programmable read only memory (EEPROM) and flash memory. One way to operate these memory devices is

Hung, col. 2:

The present invention related to a novel charge pump system. The following description is presented to enable any person skilled in the art to make and use the invention. Descriptions of specific applications are provided only as

Hung, col. 7:

The operation of charge pump **100** is now explained. FIGS. 5A–5C show voltage profiles at nodes **161–168** and **138** of FIG. 1. FIG. 5A shows four clock signals which are the same as signals **124**, **125**, **128** and **129** of FIG. 2. These clock signals are shown here again so as to provide a reference to understand the voltage profiles. FIG. 5B shows the voltage profiles **361–365** at nodes **165–168** and **138**, respectively. FIG. 5C shows the voltage profiles **366–369** at nodes **161–164**, respectively. It can be seen at regions **371–373** of FIG. 5B that charges are being pumped to subsequent stages when the triple well transistors **107–109** are turned on. As a result, the voltages of the two adjoining stages are equal at these regions. This pumping effect is enhanced by the extra diode and reduced threshold voltage of the corresponding triple well transistor of the present invention. The improved effect of other triple well transistors can be easily analyzed by person skilled in the art, and will be not explained in detail here.

Hung, col. 7:

The present invention can be applied to a negative charge pump having a negative output voltage. FIG. 6 is a schematic diagram of a negative charge pump **500** in accordance with the present invention. Charge pump **500** comprises eleven triple well NMOS transistors **502–512** and ten

Lin '129 at Abstract:

A four-phase dual pumping circuit has a number of stages according to the required output voltage based on an input voltage. Each stage has a first pumping unit and a second pumping unit that are mirror and identical to each other and electrically coupled to each other. The dual pumping circuit is controlled by four-phase clocks which are made from one pair of out of phase clocks. The transistors of the dual pumping circuit have special substrate connection to minimize body effects. The four-phase dual pumping circuit uses NMOSFETS for negative pumping and PMOSFETS for positive pumping.

Lin '129, Fig. 5:

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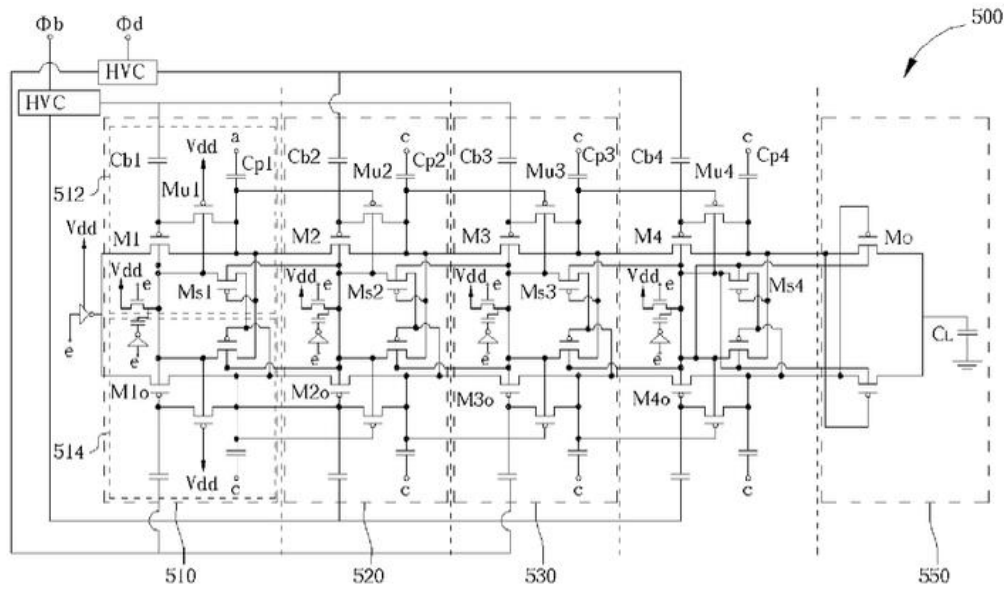


Fig. 5

Lin '129, Fig. 15:

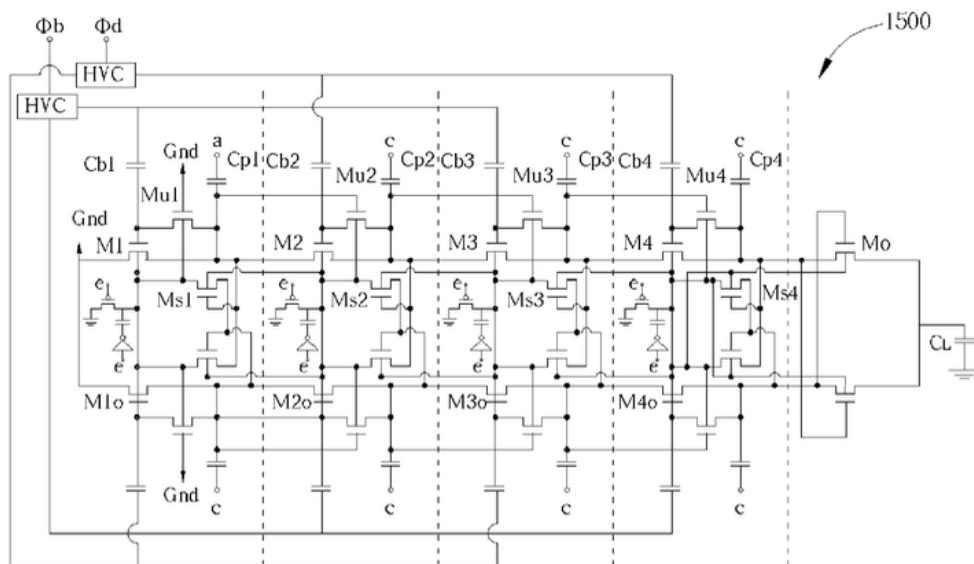


Fig. 15

Lin '129, col. 2:

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35

40

Miki, col. 1:

1. Field of the Invention

The present invention relates to a booster circuit for boosting a voltage supplied from a power supply, in particular, to a booster circuit for generating a plurality of power supply voltages, the booster circuit being disposed in 10 for example a semiconductor non-volatile storage device.

Park '791, Fig. 7:

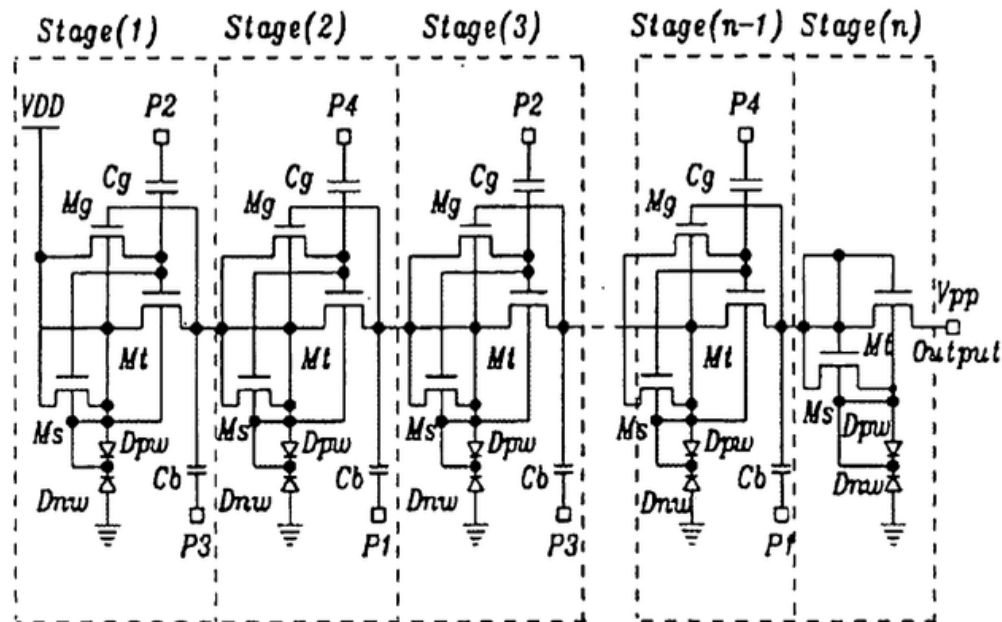


FIG. 7

Park '791, Fig. 11:

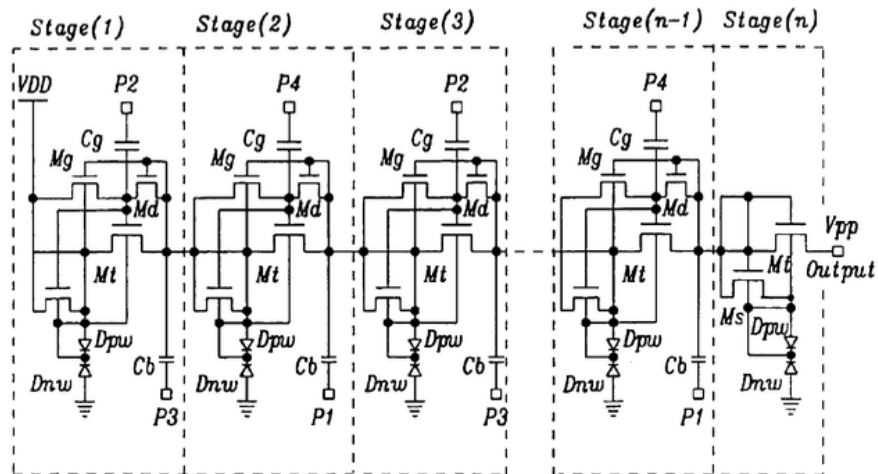


FIG. 11

Park '791, col. 1:

1. Field of Invention

The present invention relates to integrated circuits and more specifically to charge pump circuits providing high output voltage and current at low power supply voltages.

Jinbo, Fig. 7:

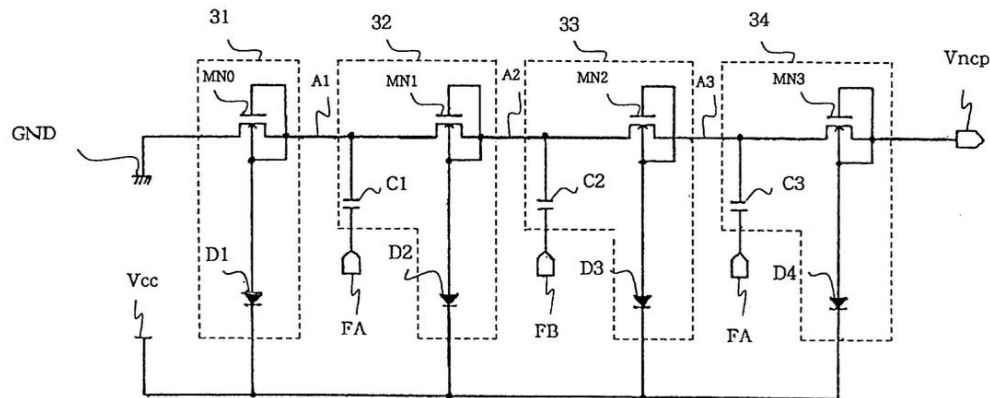


Fig. 7

Jinbo, Fig. 17:

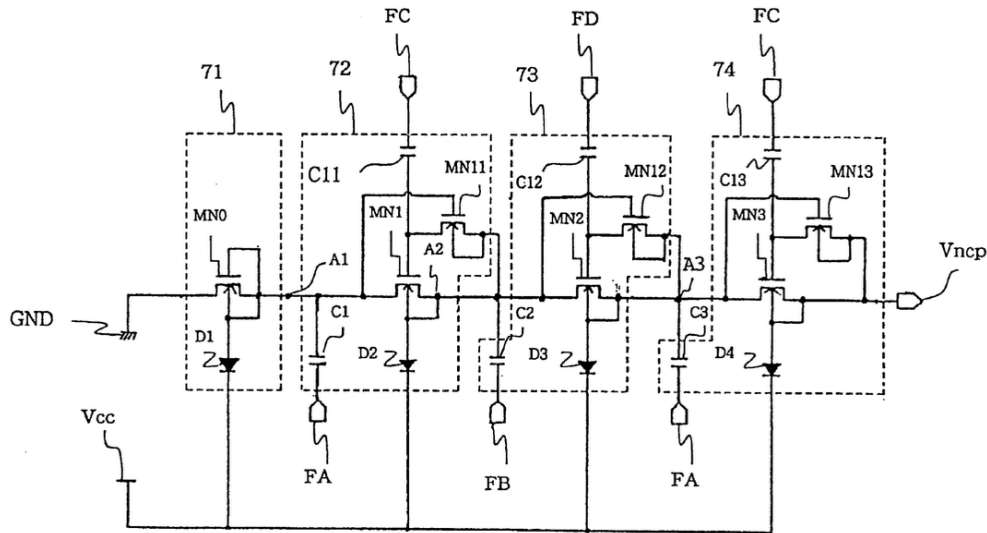


Fig. 17

Jinbo, Fig. 19:

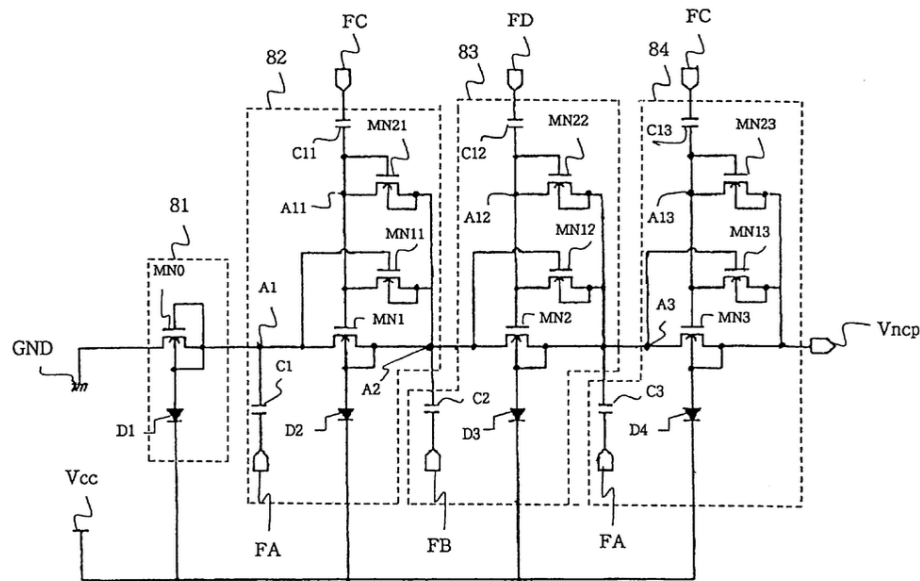


Fig. 19

Jinbo, col. 1:

This invention relates to a charge pump and, more particularly to a charge pump incorporated in a semiconductor non-volatile memory device such as, for example, an electrically erasable and programmable read only memory ¹⁰ device and a semiconductor structure for the charge pump circuit.

Jinbo, col. 3:

It is therefore an important object of the present invention 65
to provide a charge pump circuit, which is improved in
boosting characteristics.

Campardo at 376-380:

15.4.4 Voltage Doubler

Another circuit whose task is to raise the voltage, also known in literature as voltage doubler, is shown in Fig. 15.18. It is a feedback system that can duplicate the power supply, and it is composed of two n-channel transistors, (M_{N1} and M_{N2}) and two capacitors (C_{T1} and C_{T2}) of the same size.

In order to understand the principle of operation of this circuit it can be assumed that, at the beginning, nodes A and B, as well as phases CK and CK#, are at GND. In this way, both transistors M_{N1} and M_{N2} are turned off.

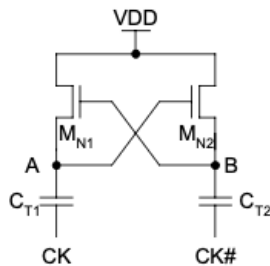


Fig. 15.18. Voltage doubler

As soon as CK phase toggles from GND to VDD, the value of node A becomes VDD, activating transistor M_{N2} . Since phase CK# remains at GND, the charge starts flowing from power supply to capacitor C_{T2} until B reaches a value equal to $VDD - V_{TH^{N2}}$. When phase CK goes to GND again, it brings node A along, thus turning off transistor M_{N2} . Now phase CK# gets to the value of VDD, therefore the value of node B becomes $VDD - V_{TH^{N2}} + VDD$ turning on transistor M_{N1} , through which C_{T1} is charged until it reaches VDD. Of course when CK# goes to GND again, node B is biased at a voltage equal to $VDD - V_{TH^{N2}}$. At this point the phases repeat. It is worth noting that each capacitance is boosted first, then charged, changing its value from VDD to 2 VDD. Since these operations are performed alternately on each half of the circuit, during a whole period either node A or node B is at 2 VDD (thus the reason for calling this circuit a “voltage doubler”). If, at this point, it is possible to design a circuit that can transmit on its output the 2 VDD voltage, independently of which node (either A or B) is biased at that value, then passing from the voltage doubler to the charge pump is relatively simple: in fact, it is sufficient to repeat such a structure where the output of a stage is used as the supply voltage for the following stage.

A PMOS output stage properly connected to nodes A and B, as the one shown in Fig. 15.19, is the simplest circuit to obtain an output voltage of 2 VDD: when CK is at VDD, A is at 2 VDD, while B is at VDD. Transistor M_{N1} is therefore turned off, while M_{P1} is active, transferring the voltage of node A to node OUT. In the meanwhile M_{P2} is turned off and M_{N2} is turned on, charging capacitor C_{T2} . When CK goes back to GND and CK# becomes VDD, then the circuit behaves in the opposite way: M_{N1} and M_{P2} are active (the former charges capacitor C_{T1} , the latter transfers the voltage of node B to the output) while M_{N2} and M_{P1} are turned off. The way the circuit is conceived, there are no direct paths between VDD and node OUT: these paths would jeopardize the functionality of the circuit itself.

Also in this case, the issue of the bulk biasing of the transistors exists (of course under the assumption that triple-well NMOS are used).

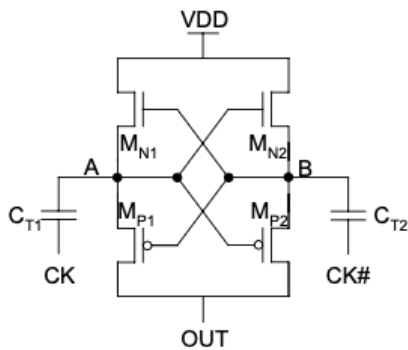


Fig. 15.19. Voltage doubler with PMOS output stage

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378 15 Circuits Used in Program and Erase Operations

Again, the solutions described in previous sections apply, and the same pros and cons hold true: one solution is to connect the bulk terminal to the power supply for the n-channel transistor and to the output node for the p-channel transistor, another one is the “dynamic biasing” of the bulk nodes. Figure 15.20 represents a possible circuit solution that allows keeping the body of the NMOS transistors to the lowest voltage, and the body of the PMOS transistors to the highest voltage, under any circumstances.

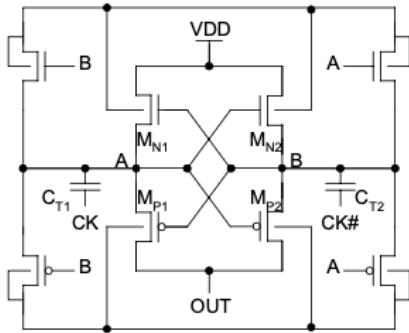


Fig. 15.20. Biasing of the bulk nodes of the transistors

A small specification is required at this point: when more stages are cascaded to realize a pump as shown in Fig. 15.21, we can decide to drive the capacitances of the stage with a signal whose swing is either GND/VDD or GND/supply of the stage. In the former case, the gain of each stage is about VDD; in the latter the gain is about 2 VDD. In any case, from an implementation point of view, the former solution is preferable.

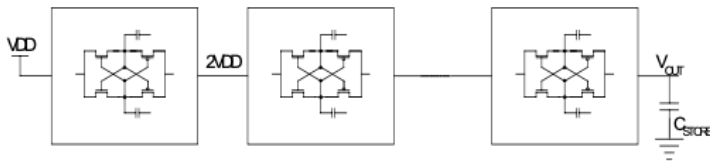


Fig. 15.21 Implementation of a charge pump by cascading a series of voltage doubler circuits; V_{OUT} output voltage is equal to $(n + 1) VDD$ if CK and CK# signals have a $0 - VDD$ swing, while it is equal to $2^n VDD$ if the swing of CK and CK# for the i -th stage is $0 - \text{supply of the } i\text{-th stage}$

This structure has several advantages:

- the possibility of driving the capacitances using only two complemented phases. This implies a relatively simple phase generator circuit with respect to the one used in the pumps described in the previous section;
- the possibility of realizing the circuit using “low voltage” transistors (i.e. transistors that can bear a voltage difference at their terminal lower than power supply) since the voltage difference at the terminals of each transistor does not go above VDD in any operating phase of the circuit;
- no boost capacitors are required for the pass transistors (since we can use the one implemented for the charge transfer), thus achieving a reduction of the area occupation and limiting the dissipated power to the one really needed to produce the desired voltage;
- a decrease of the ripple that naturally comes from the pump.

In fact, due to the operation of the charge pump and of the capacitors in general, the output of the pump is more or less noisy depending on the phase that is toggling at a given time. Let's refer to Fig. 15.5: when the clock CK goes high, the charge stored in the capacitor C_{T3} is transferred to the storage capacitor. V_{OUT} instantaneously charges to a value equal to the previous one plus the supply voltage; the corresponding waveform will show at that time an upward peak; then V_{OUT} discharges until CK goes back to GND and CK# goes to VDD. The waveform of V_{OUT} will show an upward peak again, but its height is less than the previous case, since the charge is now shared between two capacitors (i.e. C_{T3} and C_{STORE}). Now the discharge of V_{OUT} occurs again until the new phase comes in.

When talking about “ripple”, we generally refer to the height of the “peaks” that can be found in the output node waveform.

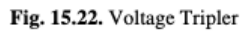
Analyzing the output of the voltage doubler as a function of different frequencies it can be seen that it is better if the clock is as short as possible. This fact can be a limitation for the circuit, since in these kinds of applications, the clock generators are often the result of a trade-off between area occupation and precision: in other words the risk is that it may be difficult to implement structures that occupy a small area and at the same time guarantee the same clock period as voltage and temperature conditions vary.

15.4.5 Voltage Tripler

This circuit is derived from the voltage doubler and provides an output voltage whose value is three times the supply voltage value.

Figure 15.22 shows the schematic of such a stage.

Since the structure is symmetric, it is possible to understand the circuit behavior by studying just one half of it. Let's start again from the condition where both CK and CK# are forced to GND, i.e. all the transistors are turned off. When CK goes to VDD, CK# remains at GND. Under these conditions, B is biased at VDD, A is biased at 2 VDD and since M_{N5} is turned on, D is biased at VDD. On the contrary, F is driven to GND by M_{N6} and transistor M_{P4} is turned off.



Contrary to the two-phases pump analyzed above, this pump cannot be implemented using low voltage transistors only, since the voltage drop at the terminals of the transistors can go above VDD under certain operating conditions.

See, e.g.:

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Hung, col. 1:

The present invention relates to using triple well transistors to increase the efficiency of a charge pump. The inventive charge pump comprises a plurality of pumping transistors arranged to increase the voltage level, or push the voltage level to a negation valve, from a first pumping transistor to a last pumping transistor in response to clock pulses applied to these pumping transistors. At least one of the plurality of pumping transistors has a source and a drain region of a first conductivity type formed on a first well having an opposite conductivity type.

A second well having the first conductivity type can be formed outside of the first well. The second well is fabricated on a substrate. This transistor design is commonly referred to as a “triple well” transistor. The source region, first well and the second well are preferably set to substantially the same potential. In one embodiment of the present invention, the second well can be set to the highest positive potential of the charge pump.

Hung, col. 2:

100 of the present invention. Charge pump **100** comprises nine triple well NMOS transistors **102–110** and twelve normal NMOS transistors **112–119** and **132–135**. These normal NMOS transistors are preferably native n-channel devices that have a low threshold voltage. Normal NMOS transistors **132–135** function as pull up transistors. Normal NMOS transistors **112–119** function as capacitors, and are coupled to clock signals **122–129**. The clock signals are coupled to the corresponding triple well NMOS transistors via the capacitive action of transistors **112–119**. Although

Hung, Fig. 3:

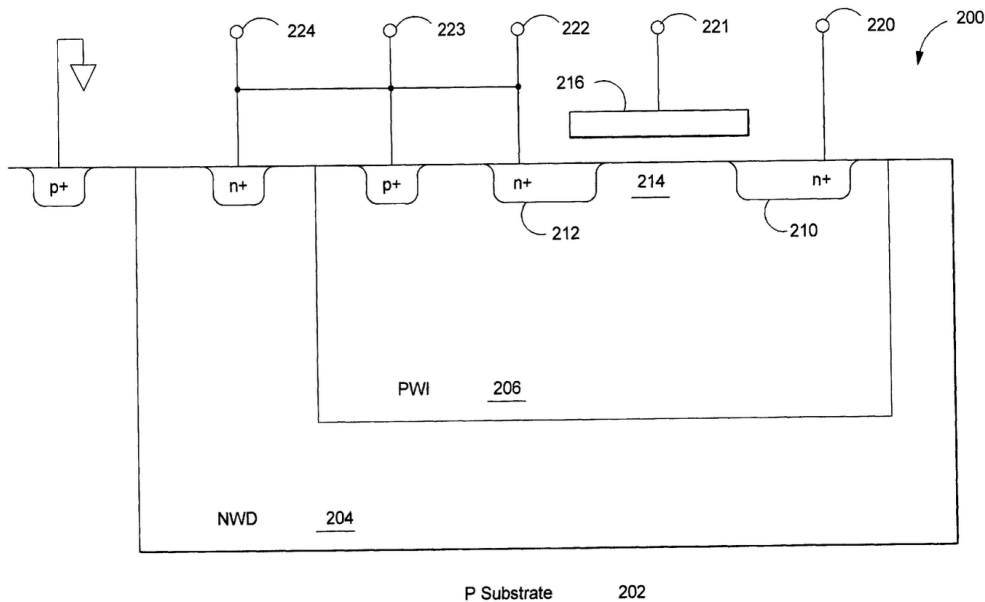


FIG.3

Hung, Fig. 4:

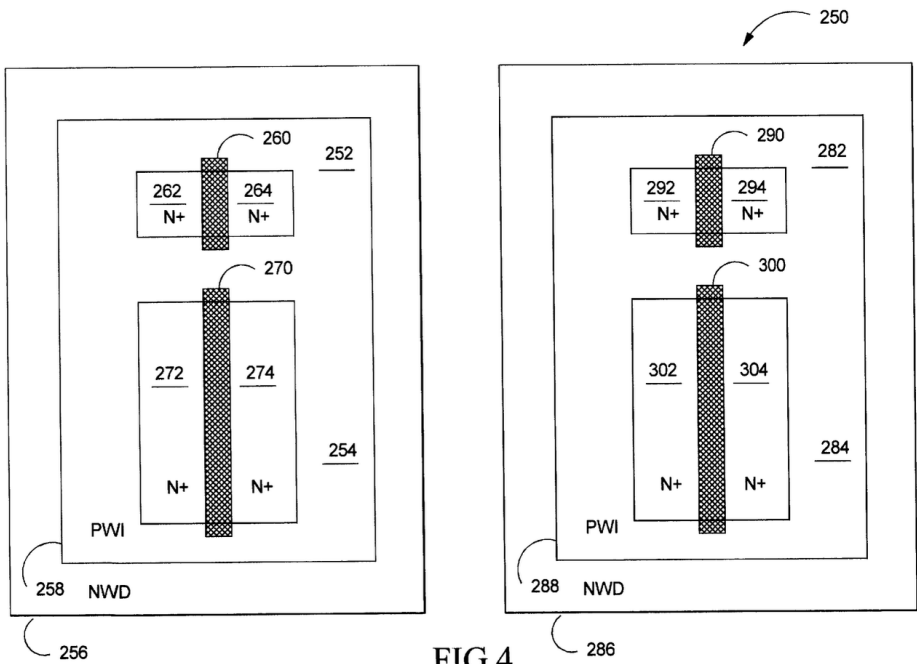


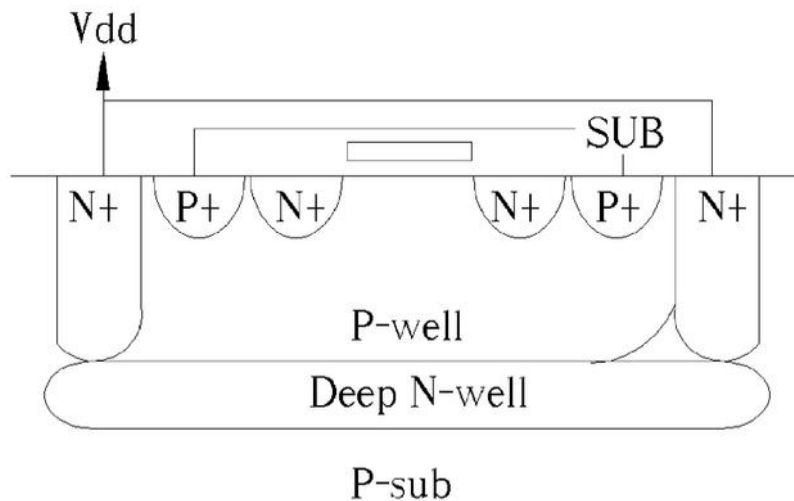
FIG.4

Hung, col. 3:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor **200** that can be used for transistors **102–110** of FIG. 1. Transistor **200** is fabricated on a p-type substrate **202**. An N well **204** is formed in substrate **202**, and a P well **206** is formed in N well **204**. An N+ type drain region **210** is formed in P well **206**, as is an N+ source region **212**. A channel region **214** is defined between source and drain regions in P well **206**. A polysilicon gate **216** is positioned above channel region **214**. A thin gate oxide is deposited between gate **216** and channel region **214**. Drain region **210**, gate **216**, source region **212**, P well **206**, and N well **204** are coupled to individual terminals **220–224**, respectively. Thus, triple well transistor **200** can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Lin '129, Fig. 18:



NMOS transistor

Fig. 18

Lin '129, col. 9:

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Please refer to FIGS. 18 and 19 which show the triple-well structure which is suitable for both NMOS and PMOS transistors in the dual pumping circuit of the present invention. The triple-well structure MOSFET with p-substrate technology is well known for those skilled in the art and will not be described in the details. FIG. 18 shows a NMOS transistor that is used in the negative dual pumping circuit in FIG. 15 and FIG. 19 shows a PMOS transistor that is used in the positive dual pumping circuit in FIG. 5. The NMOS transistor in FIG. 18 has a bias voltage of the n-well to the supply voltage Vdd. In FIG. 19, the voltage difference between the n-well and the source and drain of the PMOS transistor is close to zero so the threshold voltage is minimized having a Vtp of -0.89V and body effect is eliminated.

Lin '129, col. 2:

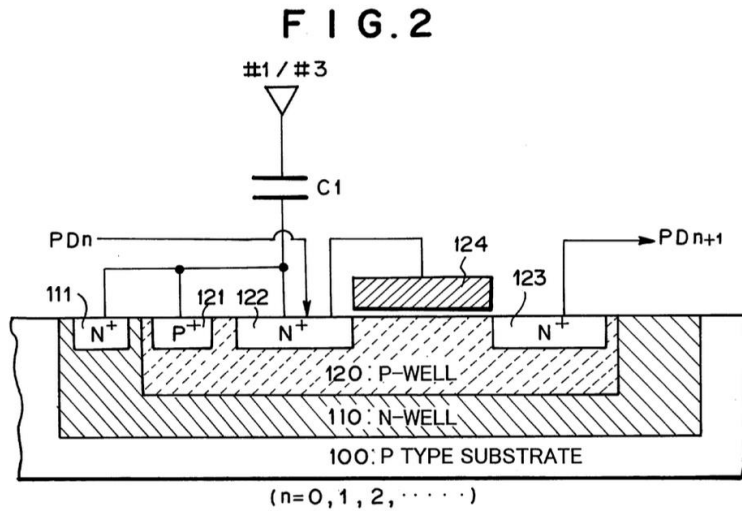
It is therefore a primary objective of the claimed invention to provide four-phase dual pumping circuits that provide a high positive voltage that is above the supply voltage and at the same time a high negative voltage that is lower than the ground voltage which are required for write and erase operations in memory devices to solve the abovementioned problem.

It is another objective of the claimed invention to provide four-phase dual pumping circuits that efficiently generates the required high positive and high negative voltages using the same triple-well technology at a low supply voltage.

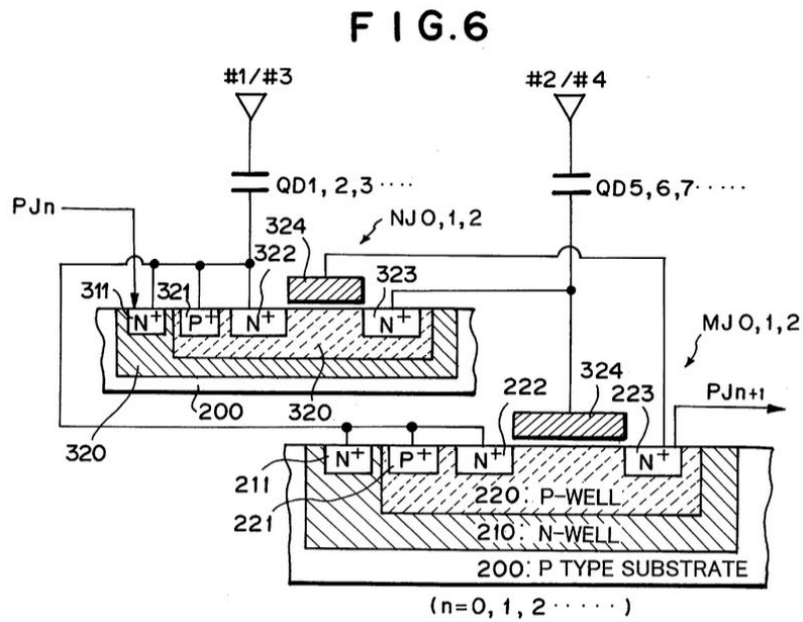
Miki, col. 4:

A first aspect of the present invention is a booster circuit having a plurality of booster cells tandem-connected, each of the boosters having a transfer transistor and a capacitor, an input terminal, a drain, and a gate of the transfer transistor being connected, a source of the transfer transistor being an output terminal, a first terminal of the capacitor being connected to the source of the transfer transistor, a clock signal being supplied to a second terminal of the capacitor, wherein the transfer transistor is composed of a triple-well having a first well and a second well, the first well being formed on a semiconductor substrate, the second well being formed on the first well, and wherein the semiconductor substrate is connected to a reference voltage, a diffusion layer in the first well, a first diffusion layer in the second well, a second diffusion layer in the second well, the first terminal of the capacitor, and the gate of the transfer transistor being connected, the conduction type of the first well being the same as the conduction type of the diffusion layer in the first well, the conduction type of the second well being the same as the conduction type of the first diffusion layer in the second well, the conduction type of the second well being different from the conduction type of the second diffusion layer in the second well.

Miki, Fig. 2:



Miki, Fig. 6:



Miki, col. 7:

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Each of the transfer transistors MD0 to MD3 of the booster cells is composed of a triple-well semiconductor shown in FIG. 2. The triple-well semiconductor is composed of an N type first well 110 and a P type second well 120. The N type first well is formed on a P type semiconductor substrate 100. The P type second well 120 is formed on the N type first well 110. The semiconductor substrate 100 of each of the transfer transistors MD0 to MD3 is connected to a reference voltage. An output terminal PDn of a booster cell in the preceding stage, an N+ diffusion layer 111 in the first well 110, a P+ diffusion layer 121 in the second well 120, an N+ diffusion layer 122 in the second well 120, a first terminal of the capacitor C1, and a gate 124 of each of the transfer transistors MD0 to MD3 are connected. The conduction type of the first well 110 is the same as the conduction type of the N+ diffusion layer 111. The conduction type of the second well 120 is the same as the conduction type of the P+ diffusion layer 121. The conduction type of the second well 120 is different from the conduction type of the N+ diffusion layer 122. The N+ diffusion layer 123 in the second well 120 is an output terminal PDn+1 of the booster cell.

Miki, col. 9:

FIG. 6 is a sectional view showing a real example of the structure of each booster cell shown in FIG. 5. As shown in FIG. 6, each booster cell is composed of a triple-well semiconductor device. Each transfer transistor MJn comprises an N type first well 210 and a P type second well 220. The N type first well 210 is formed on a P type semiconductor substrate 200. The P type second well 220 is formed on the N type first well 210. Each transfer transistor NJn comprises an N type first well 310 and a P type second well 320. The N type first well 310 is formed on a P type semiconductor substrate 200. The P type second well 320 is formed on the N type first well 310.

The P type semiconductor substrates 200 and 300 are connected to a reference voltage. N+ diffusion layers 211 and 311 in the first wells 210 and 310, P+ diffusion layers 221 and 321 in the second wells 220 and 320, N+ diffusion layers (drains) in the second wells 220 and 320, and first terminals of capacitors QD1 and QD2 are directly connected. The conduction type of the first wells 210 and 310 is the same as the conduction type of the N+ diffusion layers 211 and 311. The conduction type of the second wells 220 and 320 is the same as the conduction type of the P+ type diffusion layers 221 and 321. The conduction type of the second wells 220 and 320 is different from the conduction type of the N+ diffusion layers (drains) 222 and 322.

N+ diffusion layers (sources) 323 of the transfer transistors NJ0 to NJ3, gates 224 of the transfer transistors MJ0 to MJ3, and first terminals of capacitors QD5 and QD6 are directly connected. Gates 324 of the transfer transistors NJ0 to NJ3 and N+ diffusion layers (sources) 223 of the transfer transistors MJ0 to MJ3 are connected. A diffusion layer 223 of the second well 220 is an output terminal of the booster cell.

Park '791, Fig. 5:

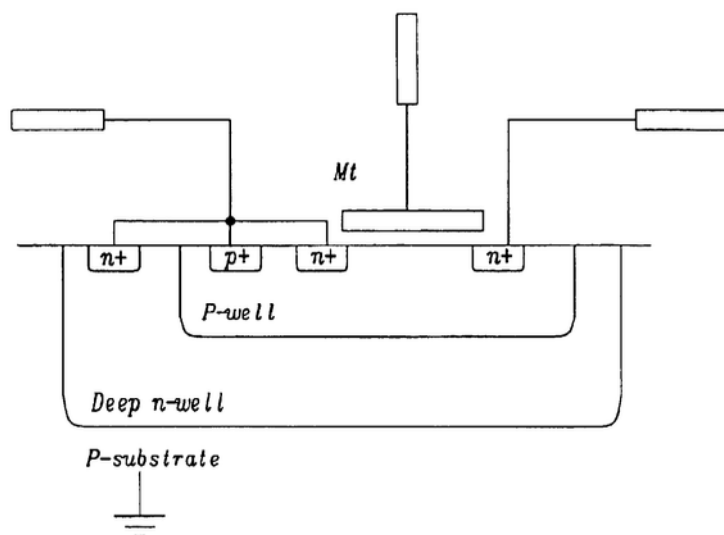


FIG. 5 - Prior Art

Park '791, Fig. 9:

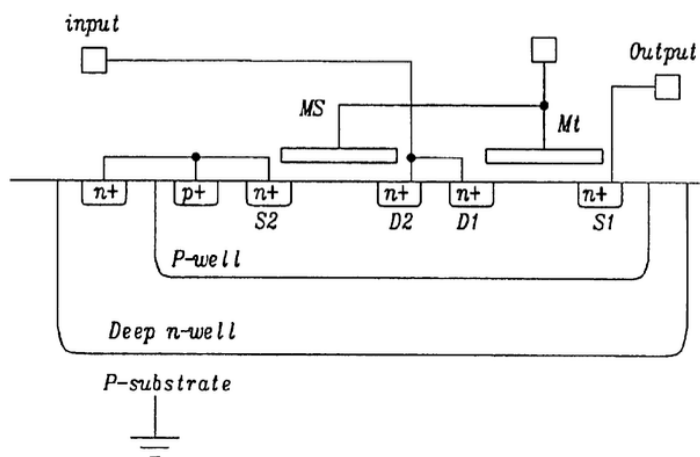
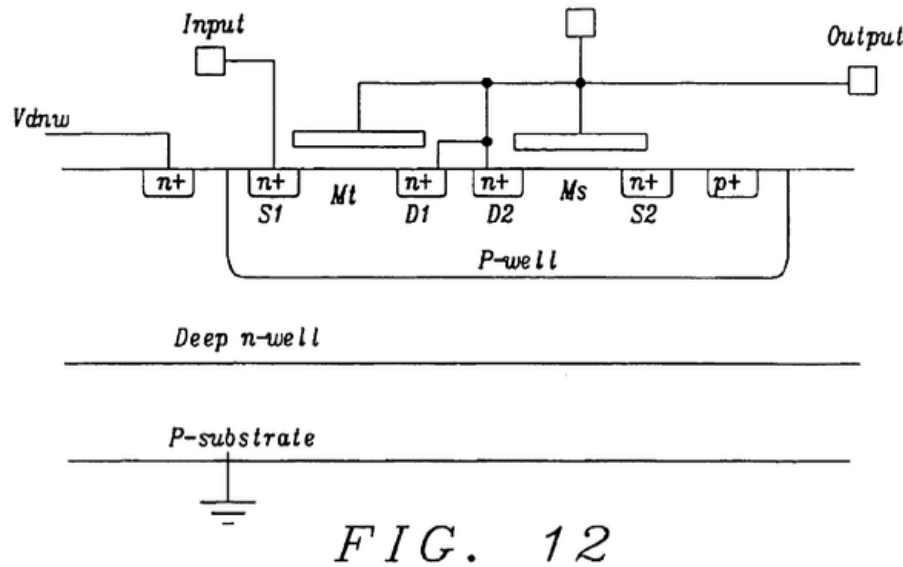


FIG. 9

Park '791, Fig. 12:



Park '791, cols. 2-3:

60 A prior art charge pump circuit using a floating well is described in U.S. Pat. No. 5,986,947 (Choi et al.). The charge pump circuits using a triple well P-N junction and MOS diodes are disclosed in "A 3.3V only 16 Mb DINOR flash memory", IEEE International Solid State Circuits
65 Conference, Digest of Technical Papers, 1995, pp 122-123, and in U.S. Pat. No. 6,100,557 (Hung et al.), respectively. The triple well charge pump provides greater efficiency with

increased suppression of the body effect over other prior art. This improvement is due to the extra diode inherently formed between the well and the source of the charge transfer MOS device that can help increase the forward conduction current.

5

Park '791, col. 5:

FIG. 7 shows a circuit diagram of the charge pump of the present invention where the negative effects of the triple well 15 are reduced by the inclusion of the auxiliary MOSFET device Ms. Included in the circuit diagram are Dpw, the parasitic diode between the P-well and the deep N-well, and Dnw, the parasitic diode between the deep N-well and the P-substrate. Other, and less important, parasitic diodes and capacitances associated with MOS devices are not shown for 20 ease of understanding of the circuit diagram. Pumping stages are connected in series from power supply VDD to the high voltage output Vpp. Each pumping stage is formed in its own P-well and deep N-well. The P-well acts as 25 substrate region of the MOS devices in the pumping stage.

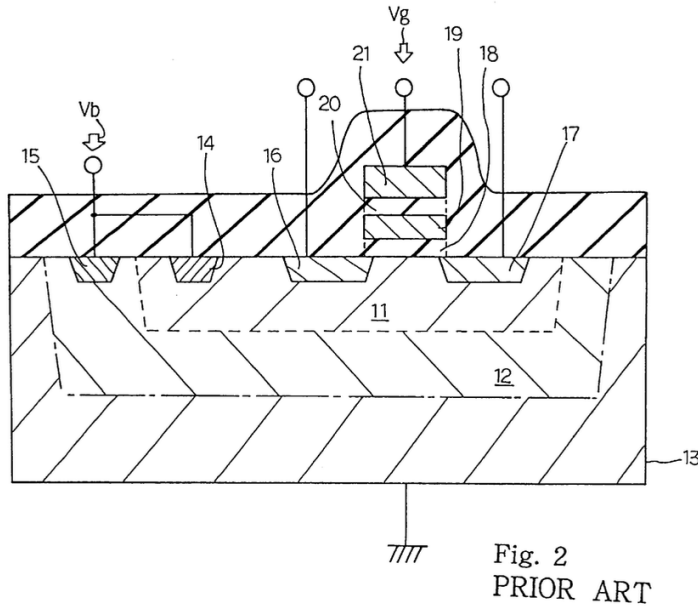
Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

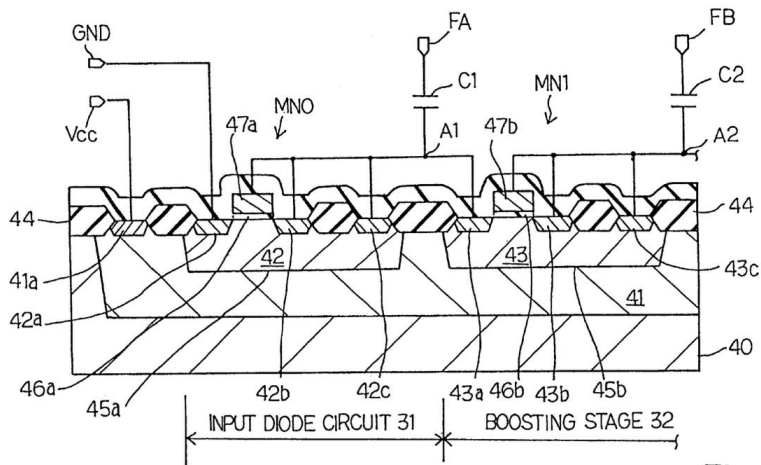
any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Jinbo, Fig. 2:



Jinbo, Fig. 8:



Jinbo, col. 1:

FIG. 2 illustrates another kind of the non-volatile memory cell. A p-type well 11 is nested in an n-type well 12, which is formed in a surface portion of a p-type semiconductor substrate 13. A heavily-doped p-type region 14 and an heavily-doped n-type region 15 are respectively formed in the p-type well 11 and the n-type well 12, and both of the heavily-doped p-type region 14 and the heavily-doped n-type region 15 are electrically connected to each other.

An n-type source region 16 and an n-type drain region 17 are formed in the p-type well 11, and are spaced from each other. A tunnel gate oxide layer 18, a floating gate electrode 19, an interpoly oxide layer 20 and a control gate electrode 21 are stacked over the channel region between the n-type source region 16 and the n-type drain region 17.

Jinbo, col. 6:

- 20 FIG. 8 illustrates the structure of the charge pump circuit integrated on a semiconductor substrate 40. The charge pump circuit forms a part of an integrated circuit device such as, for example, a flash EEPROM device. In this instance, the semiconductor substrate 40 is formed of p-type silicon.
- 25 An n-type well 41 is formed in a surface portion of the semiconductor substrate 40, and p-type wells 42/43 are formed in the n-type well 41. The n-type well 41 electrically isolates the p-type wells 42/43 from the p-type semiconductor substrate 40. The p-type wells 42/43 are spaced from
- 30 each other, and a thick filed oxide layer 44 are selectively grown so as to offer electrical insulation between the n-type well 41 and the p-type wells 42 and 43.

Jinbo, col. 7:

The capacitors C1/C2/C3 are implemented by p-channel depletion type field effect transistors formed in the n-type well 41, respectively. One of the p-channel depletion type field effect transistors is shown in FIG. 9. A p-type well 48 is formed in another surface portion of the n-type well 41, 20 and heavily-doped p-type impurity regions 48a/48b are spaced from each other in the p-type well 48. A thin gate insulating layer 48c is grown over the p-type well 48 between the heavily-doped p-type impurity regions 48a and 48b, and a gate electrode 48d is laminated on the thin gate 25 insulating layer 48c. The gate electrode 48d is, by way of example, connected to the boosted node A1, and the clock signal FA is supplied to the heavily-doped p-type impurity regions 48a/48b. The gate potential is not consumed in the depletion type field effect transistor for generating an inver- 30 sion layer, and a large amount of electric charge is accumulated between the depletion channel 48 and the gate electrode 48d.

Campardo at 375-376:

If we could use N-channel transistors in triple-well, we might think about connecting the body of the switch to its drain.

In this way, not only do we save area on silicon, because structure like bulk bi-aser or dynamic bulk biaser are no longer required, but we also have a positive side effect, i.e. a bipolar diode is created inside the triple well transistor (Fig. 15.17), which starts transferring charge as soon as the voltage difference between drain and source is equal to its V_T . This fact has several consequences. On one hand it is possible to start the charge transfer from one capacitor to the following one earlier and the resistance for the NMOS transistor is reduced, since the charge transfer takes place through two paths: one is the channel when the MOS is activated, the other one is the bipolar (at least until the bipolar diode is active). On the other hand, the pre-charge of capacitors C_p might be still incomplete, therefore the boost of the gate of the transistors might become inefficient. Another issue due to the presence of the bipolar is the possibility that latch-up phenomena occur.

To transfer the charges from the last transfer capacitor to the storage capacitor on the output a diode-connected transistor or a further pass-transistor can be used. Both solutions have pros and cons.

A diode-connected transistor has the advantage of being easily designed, while the disadvantage is that it requires a voltage difference at its terminal in order to operate correctly; as a consequence the voltage transferred to the output is equal to the voltage of the last stage minus the threshold voltage of the diode. On the contrary, the pass-transistor allows transferring all the voltage to the output, but it requires a boost structure for its gate (identical to the one required by the internal stages of the pump) to be properly driven, i.e. to be able to correctly transfer the voltage. Power consumption increases when this pump structure is compared to the pumps previously seen. In fact the phases must be created “ad hoc”: delays must be carefully introduced so that under every operating condition of the pump simultaneous boost of the pass-transistors or of capacitors belonging to different

376 15 Circuits Used in Program and Erase Operations

stages are avoided. Therefore the phase generator grows in complexity and its power consumption grows as well. Furthermore part of the charge stored in the transfer capacitors is used to precharge capacitor C_p placed on the gate of the pass-transistor. As a consequence not all the charge is transferred, but part of it is lost for this operation.

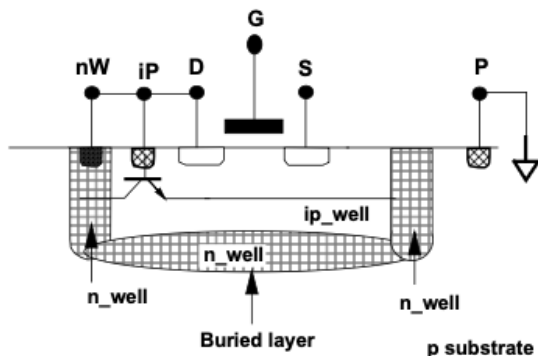


Fig. 15.17. Charge transfer using bipolar parasitic diode

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

1[c] a second-conductivity type second well region in the first well region, and

The Omnibus References disclose and/or render obvious a second-conductivity type second well region in the first well region.

See, e.g.:

Hung, col. 1:

The present invention relates to using triple well transistors to increase the efficiency of a charge pump. The inventive charge pump comprises a plurality of pumping transistors arranged to increase the voltage level, or push the voltage level to a negation valve, from a first pumping transistor to a last pumping transistor in response to clock pulses applied to these pumping transistors. At least one of the plurality of pumping transistors has a source and a drain region of a first conductivity type formed on a first well having an opposite conductivity type.

A second well having the first conductivity type can be formed outside of the first well. The second well is fabricated on a substrate. This transistor design is commonly referred to as a “triple well” transistor. The source region, first well and the second well are preferably set to substantially the same potential. In one embodiment of the present invention, the second well can be set to the highest positive potential of the charge pump.

Hung, col. 2:

45 **100** of the present invention. Charge pump **100** comprises nine triple well NMOS transistors **102–110** and twelve normal NMOS transistors **112–119** and **132–135**. These normal NMOS transistors are preferably native n-channel devices that have a low threshold voltage. Normal NMOS transistors **132–135** function as pull up transistors. Normal NMOS transistors **112–119** function as capacitors, and are coupled to clock signals **122–129**. The clock signals are coupled to the corresponding triple well NMOS transistors via the capacitive action of transistors **112–119**. Although

Hung, Fig. 3:

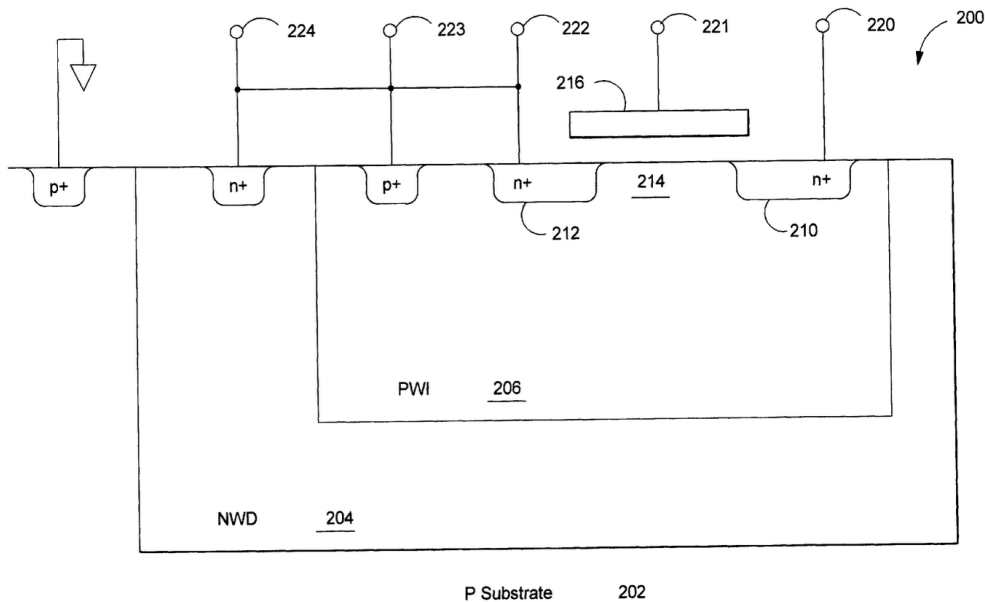


FIG.3

Hung, Fig. 4:

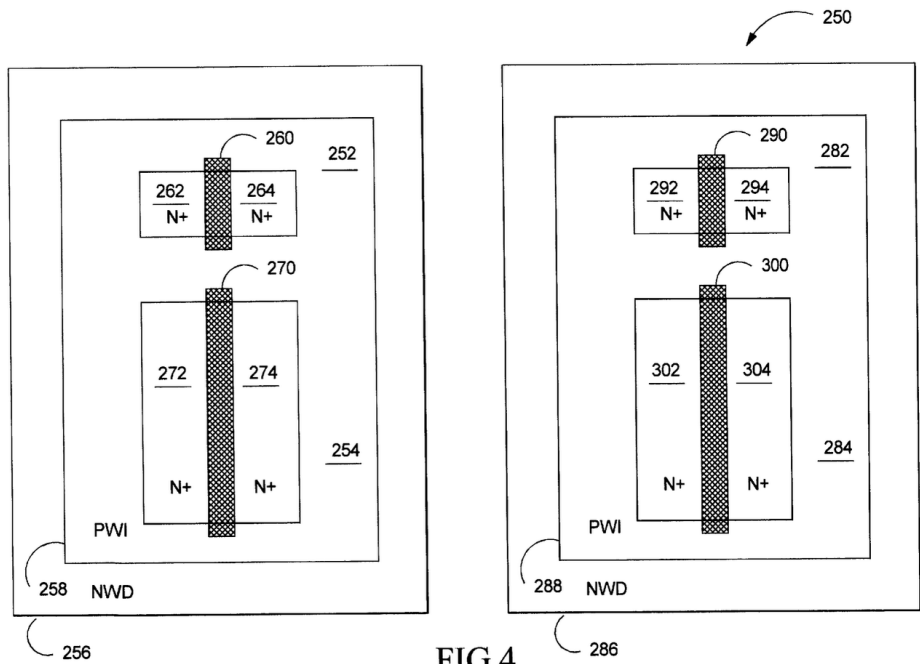


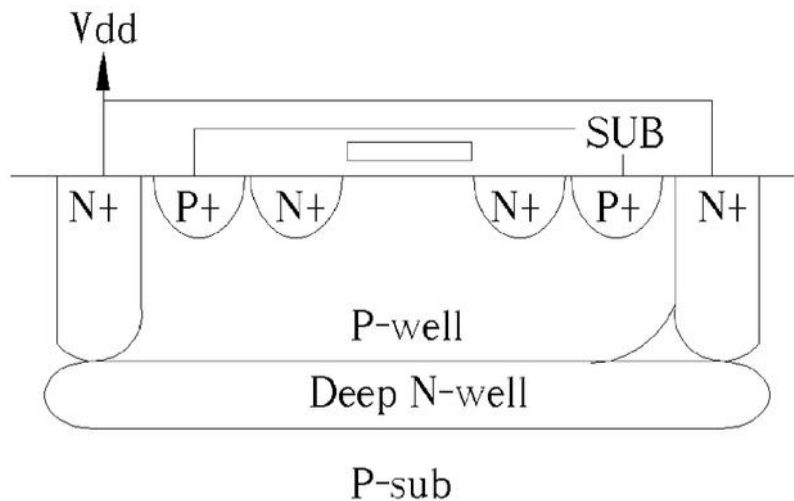
FIG.4

Hung, col. 3:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor 200 that can be used for transistors 102–110 of FIG. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed in substrate 202, and a P well 206 is formed in N well 204. An N+ type drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220–224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Lin '129, Fig. 18:



NMOS transistor

Fig. 18

Lin '129, col. 9:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please refer to FIGS. 18 and 19 which show the triple-well structure which is suitable for both NMOS and PMOS transistors in the dual pumping circuit of the present invention. The triple-well structure MOSFET with p-substrate technology is well known for those skilled in the art and will not be described in the details. FIG. 18 shows a NMOS transistor that is used in the negative dual pumping circuit in FIG. 15 and FIG. 19 shows a PMOS transistor that is used in the positive dual pumping circuit in FIG. 5. The NMOS transistor in FIG. 18 has a bias voltage of the n-well to the supply voltage Vdd. In FIG. 19, the voltage difference between the n-well and the source and drain of the PMOS transistor is close to zero so the threshold voltage is minimized having a Vtp of -0.89V and body effect is eliminated.

Lin '129, col. 2:

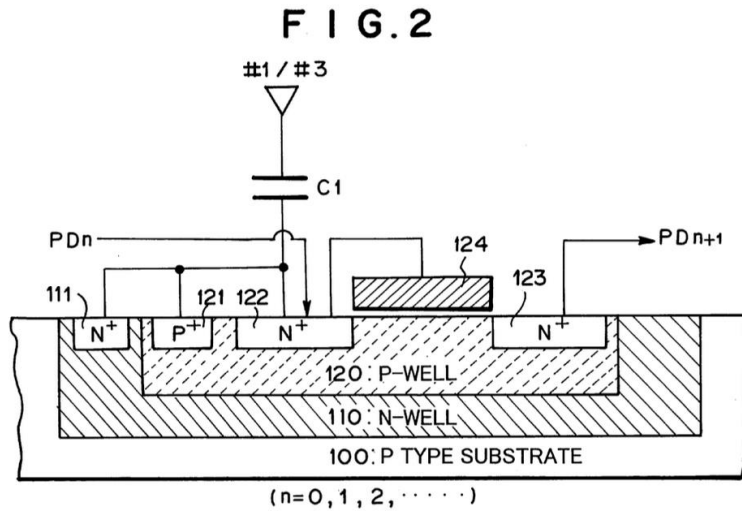
It is therefore a primary objective of the claimed invention to provide four-phase dual pumping circuits that provide a high positive voltage that is above the supply voltage and at the same time a high negative voltage that is lower than the ground voltage which are required for write and erase operations in memory devices to solve the abovementioned problem.

It is another objective of the claimed invention to provide four-phase dual pumping circuits that efficiently generates the required high positive and high negative voltages using the same triple-well technology at a low supply voltage.

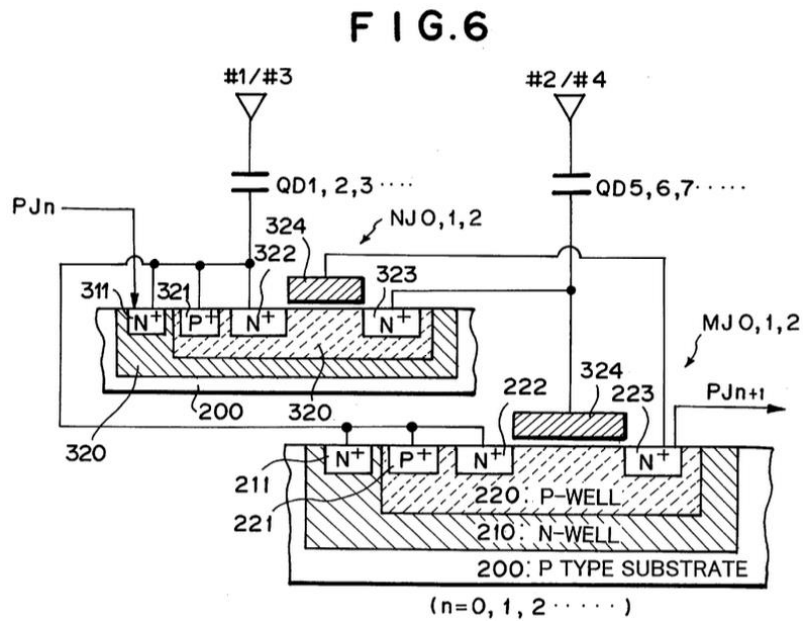
Miki, col. 4:

A first aspect of the present invention is a booster circuit having a plurality of booster cells tandem-connected, each of the boosters having a transfer transistor and a capacitor, an input terminal, a drain, and a gate of the transfer transistor being connected, a source of the transfer transistor being an output terminal, a first terminal of the capacitor being connected to the source of the transfer transistor, a clock signal being supplied to a second terminal of the capacitor, wherein the transfer transistor is composed of a triple-well having a first well and a second well, the first well being formed on a semiconductor substrate, the second well being formed on the first well, and wherein the semiconductor substrate is connected to a reference voltage, a diffusion layer in the first well, a first diffusion layer in the second well, a second diffusion layer in the second well, the first terminal of the capacitor, and the gate of the transfer transistor being connected, the conduction type of the first well being the same as the conduction type of the diffusion layer in the first well, the conduction type of the second well being the same as the conduction type of the first diffusion layer in the second well, the conduction type of the second well being different from the conduction type of the second diffusion layer in the second well.

Miki, Fig. 2:



Miki, Fig. 6:



Miki, col. 7:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Each of the transfer transistors MD0 to MD3 of the booster cells is composed of a triple-well semiconductor shown in FIG. 2. The triple-well semiconductor is composed of an N type first well 110 and a P type second well 120. The N type first well is formed on a P type semiconductor substrate 100. The P type second well 120 is formed on the N type first well 110. The semiconductor substrate 100 of each of the transfer transistors MD0 to MD3 is connected to a reference voltage. An output terminal PDn of a booster cell in the preceding stage, an N+ diffusion layer 111 in the first well 110, a P+ diffusion layer 121 in the second well 120, an N+ diffusion layer 122 in the second well 120, a first terminal of the capacitor C1, and a gate 124 of each of the transfer transistors MD0 to MD3 are connected. The conduction type of the first well 110 is the same as the conduction type of the N+ diffusion layer 111. The conduction type of the second well 120 is the same as the conduction type of the P+ diffusion layer 121. The conduction type of the second well 120 is different from the conduction type of the N+ diffusion layer 122. The N+ diffusion layer 123 in the second well 120 is an output terminal PDn+1 of the booster cell.

Miki, col. 9:

FIG. 6 is a sectional view showing a real example of the structure of each booster cell shown in FIG. 5. As shown in FIG. 6, each booster cell is composed of a triple-well semiconductor device. Each transfer transistor MJn comprises an N type first well 210 and a P type second well 220. The N type first well 210 is formed on a P type semiconductor substrate 200. The P type second well 220 is formed on the N type first well 210. Each transfer transistor NJn comprises an N type first well 310 and a P type second well 320. The N type first well 310 is formed on a P type semiconductor substrate 200. The P type second well 320 is formed on the N type first well 310.

The P type semiconductor substrates 200 and 300 are connected to a reference voltage. N+ diffusion layers 211 and 311 in the first wells 210 and 310, P+ diffusion layers 221 and 321 in the second wells 220 and 320, N+ diffusion layers (drains) in the second wells 220 and 320, and first terminals of capacitors QD1 and QD2 are directly connected. The conduction type of the first wells 210 and 310 is the same as the conduction type of the N+ diffusion layers 211 and 311. The conduction type of the second wells 220 and 320 is the same as the conduction type of the P+ type diffusion layers 221 and 321. The conduction type of the second wells 220 and 320 is different from the conduction type of the N+ diffusion layers (drains) 222 and 322.

N+ diffusion layers (sources) 323 of the transfer transistors NJ0 to NJ3, gates 224 of the transfer transistors MJ0 to MJ3, and first terminals of capacitors QD5 and QD6 are directly connected. Gates 324 of the transfer transistors NJ0 to NJ3 and N+ diffusion layers (sources) 223 of the transfer transistors MJ0 to MJ3 are connected. A diffusion layer 223 of the second well 220 is an output terminal of the booster cell.

Park '791, Fig. 5:

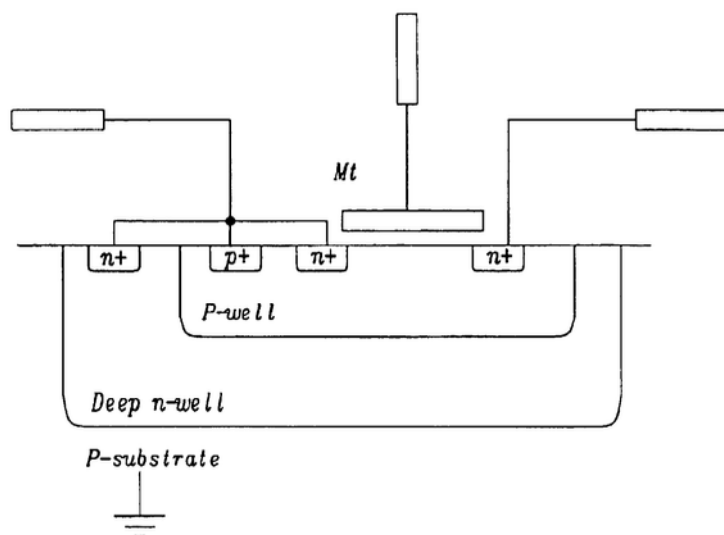


FIG. 5 - Prior Art

Park '791, Fig. 9:

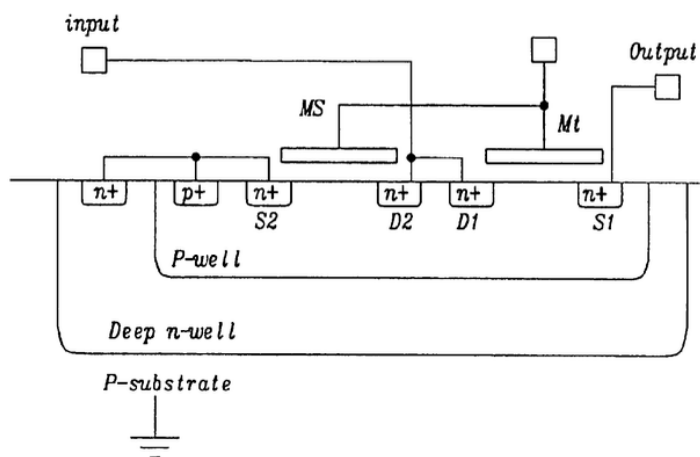
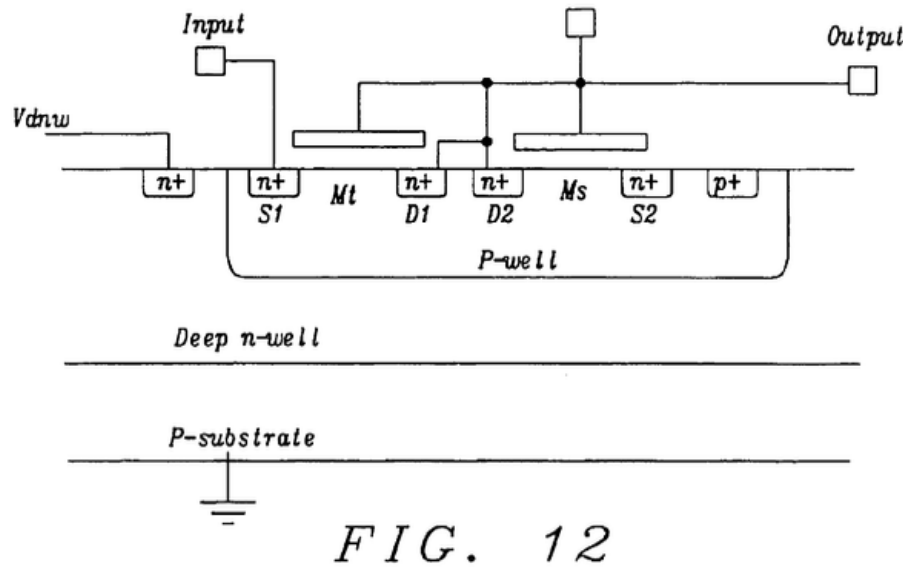


FIG. 9

Park '791, Fig. 12:



Park '791, cols. 2-3:

60 A prior art charge pump circuit using a floating well is described in U.S. Pat. No. 5,986,947 (Choi et al.). The charge pump circuits using a triple well P-N junction and MOS diodes are disclosed in "A 3.3V only 16 Mb DINOR flash memory", IEEE International Solid State Circuits
65 Conference, Digest of Technical Papers, 1995, pp 122-123, and in U.S. Pat. No. 6,100,557 (Hung et al.), respectively. The triple well charge pump provides greater efficiency with

increased suppression of the body effect over other prior art. This improvement is due to the extra diode inherently formed between the well and the source of the charge transfer MOS device that can help increase the forward conduction current.

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Park '791, col. 5:

FIG. 7 shows a circuit diagram of the charge pump of the present invention where the negative effects of the triple well 15 are reduced by the inclusion of the auxiliary MOSFET device Ms. Included in the circuit diagram are Dpw, the parasitic diode between the P-well and the deep N-well, and Dnw, the parasitic diode between the deep N-well and the P-substrate. Other, and less important, parasitic diodes and capacitances associated with MOS devices are not shown for 20 ease of understanding of the circuit diagram. Pumping stages are connected in series from power supply VDD to the high voltage output Vpp. Each pumping stage is formed in its own P-well and deep N-well. The P-well acts as 25 substrate region of the MOS devices in the pumping stage.

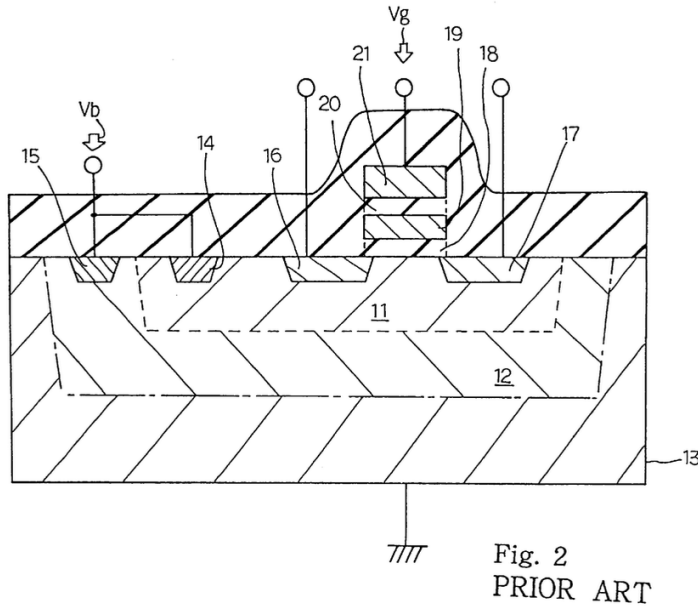
Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

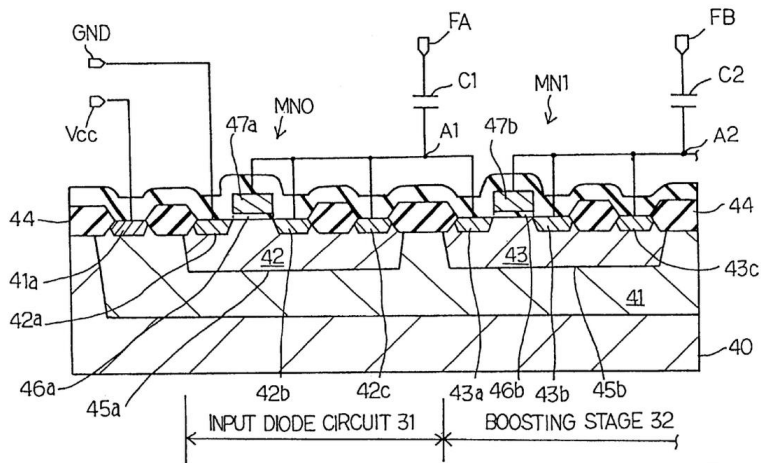
any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Jinbo, Fig. 2:



Jinbo, Fig. 8:



Jinbo, col. 1:

FIG. 2 illustrates another kind of the non-volatile memory cell. A p-type well 11 is nested in an n-type well 12, which is formed in a surface portion of a p-type semiconductor substrate 13. A heavily-doped p-type region 14 and an heavily-doped n-type region 15 are respectively formed in the p-type well 11 and the n-type well 12, and both of the heavily-doped p-type region 14 and the heavily-doped n-type region 15 are electrically connected to each other.

An n-type source region 16 and an n-type drain region 17 are formed in the p-type well 11, and are spaced from each other. A tunnel gate oxide layer 18, a floating gate electrode 19, an interpoly oxide layer 20 and a control gate electrode 21 are stacked over the channel region between the n-type source region 16 and the n-type drain region 17.

Jinbo, col. 6:

20 FIG. 8 illustrates the structure of the charge pump circuit integrated on a semiconductor substrate 40. The charge pump circuit forms a part of an integrated circuit device such as, for example, a flash EEPROM device. In this instance, the semiconductor substrate 40 is formed of p-type silicon.

25 An n-type well 41 is formed in a surface portion of the semiconductor substrate 40, and p-type wells 42/43 are formed in the n-type well 41. The n-type well 41 electrically isolates the p-type wells 42/43 from the p-type semiconductor substrate 40. The p-type wells 42/43 are spaced from

30 each other, and a thick filed oxide layer 44 are selectively grown so as to offer electrical insulation between the n-type well 41 and the p-type wells 42 and 43.

Jinbo, col. 7:

The capacitors C1/C2/C3 are implemented by p-channel depletion type field effect transistors formed in the n-type well 41, respectively. One of the p-channel depletion type field effect transistors is shown in FIG. 9. A p-type well 48 is formed in another surface portion of the n-type well 41, 20 and heavily-doped p-type impurity regions 48a/48b are spaced from each other in the p-type well 48. A thin gate insulating layer 48c is grown over the p-type well 48 between the heavily-doped p-type impurity regions 48a and 48b, and a gate electrode 48d is laminated on the thin gate 25 insulating layer 48c. The gate electrode 48d is, by way of example, connected to the boosted node A1, and the clock signal FA is supplied to the heavily-doped p-type impurity regions 48a/48b. The gate potential is not consumed in the depletion type field effect transistor for generating an inver- 30 sion layer, and a large amount of electric charge is accumulated between the depletion channel 48 and the gate electrode 48d.

Campardo at 375-376:

If we could use N-channel transistors in triple-well, we might think about connecting the body of the switch to its drain.

In this way, not only do we save area on silicon, because structure like bulk bi-aser or dynamic bulk biaser are no longer required, but we also have a positive side effect, i.e. a bipolar diode is created inside the triple well transistor (Fig. 15.17), which starts transferring charge as soon as the voltage difference between drain and source is equal to its V_T . This fact has several consequences. On one hand it is possible to start the charge transfer from one capacitor to the following one earlier and the resistance for the NMOS transistor is reduced, since the charge transfer takes place through two paths: one is the channel when the MOS is activated, the other one is the bipolar (at least until the bipolar diode is active). On the other hand, the pre-charge of capacitors C_p might be still incomplete, therefore the boost of the gate of the transistors might become inefficient. Another issue due to the presence of the bipolar is the possibility that latch-up phenomena occur.

To transfer the charges from the last transfer capacitor to the storage capacitor on the output a diode-connected transistor or a further pass-transistor can be used. Both solutions have pros and cons.

A diode-connected transistor has the advantage of being easily designed, while the disadvantage is that it requires a voltage difference at its terminal in order to operate correctly; as a consequence the voltage transferred to the output is equal to the voltage of the last stage minus the threshold voltage of the diode. On the contrary, the pass-transistor allows transferring all the voltage to the output, but it requires a boost structure for its gate (identical to the one required by the internal stages of the pump) to be properly driven, i.e. to be able to correctly transfer the voltage. Power consumption increases when this pump structure is compared to the pumps previously seen. In fact the phases must be created “ad hoc”: delays must be carefully introduced so that under every operating condition of the pump simultaneous boost of the pass-transistors or of capacitors belonging to different

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stages are avoided. Therefore the phase generator grows in complexity and its power consumption grows as well. Furthermore part of the charge stored in the transfer capacitors is used to precharge capacitor C_p placed on the gate of the pass-transistor. As a consequence not all the charge is transferred, but part of it is lost for this operation.

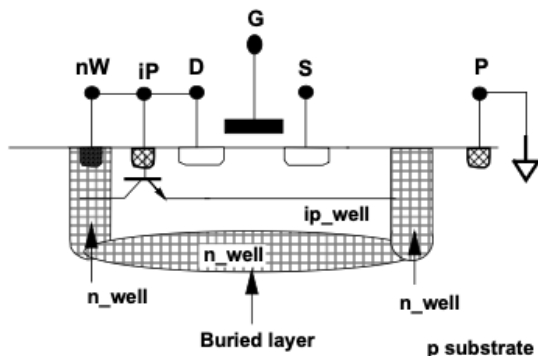


Fig. 15.17. Charge transfer using bipolar parasitic diode

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

1[d] at least one switching element in either or both of the first well region and the second well region,

The Omnibus References disclose and/or render obvious at least one switching element in either or both of the first well region and the second well region.

See, e.g.:

Hung, col. 2:

45 **100** of the present invention. Charge pump **100** comprises nine triple well NMOS transistors **102–110** and twelve normal NMOS transistors **112–119** and **132–135**. These normal NMOS transistors are preferably native n-channel devices that have a low threshold voltage. Normal NMOS
50 transistors **132–135** function as pull up transistors. Normal NMOS transistors **112–119** function as capacitors, and are coupled to clock signals **122–129**. The clock signals are coupled to the corresponding triple well NMOS transistors via the capacitive action of transistors **112–119**. Although

Hung, Fig. 3:

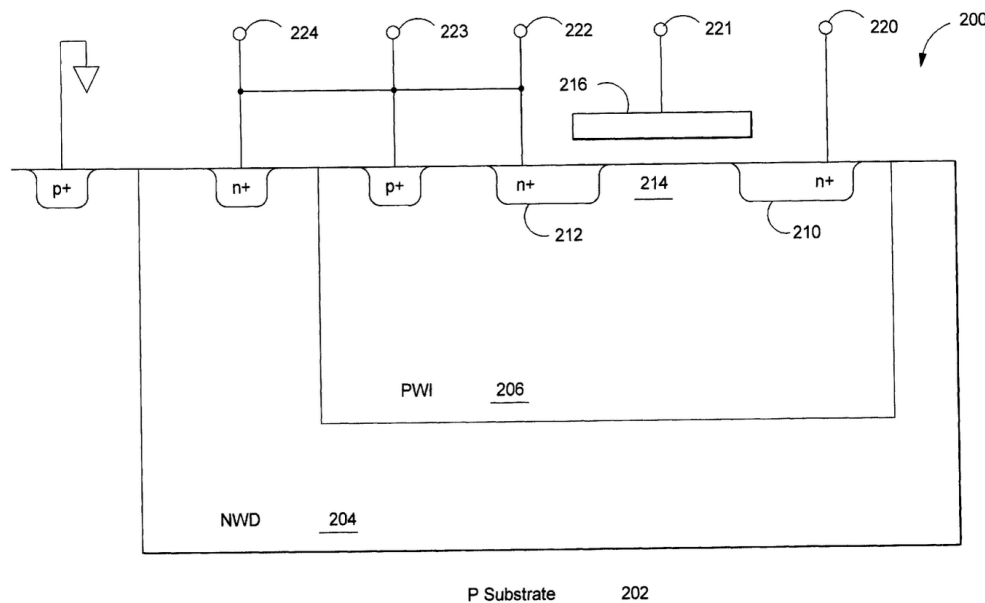


FIG.3

Hung, Fig. 4:

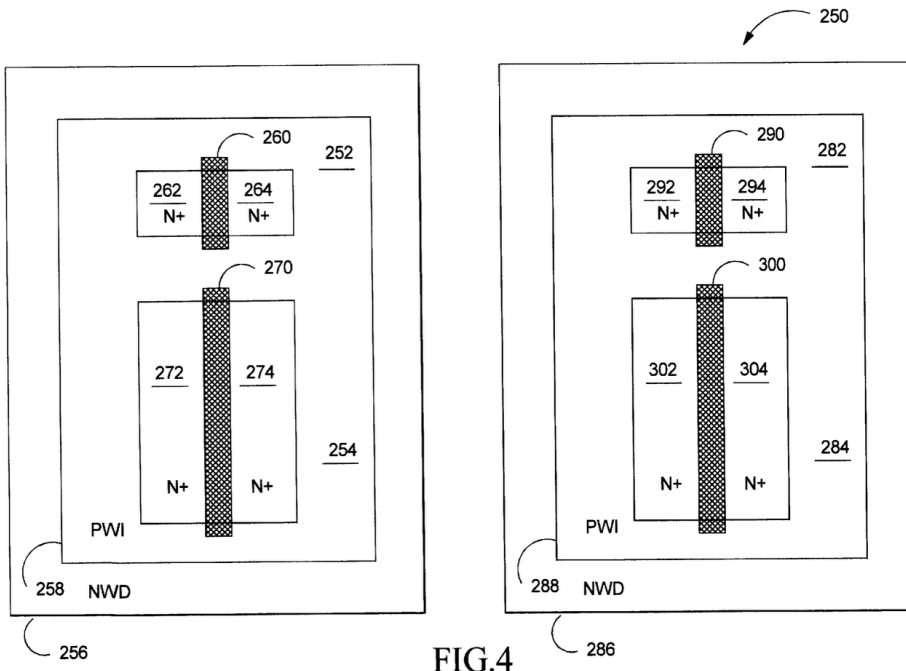


FIG. 4

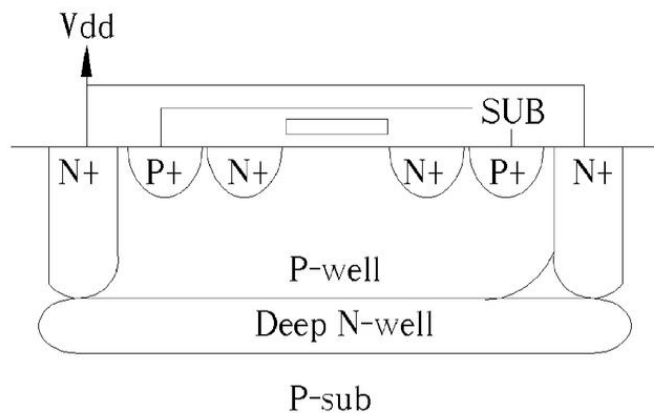
Hung, col. 3:

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor 200 that can be used for transistors 102–110 of FIG. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed in substrate 202, and a P well 206 is formed in N well 204. An N+ type drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220–224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Hung, col. 4:

FIG. 4 shows a top view 250 of four triple well transistors used in the present invention. It shows two transistors 252 and 254 formed inside a P well 258 and an N well 256. Transistor 252 further comprises a gate 260, a source region 262 and a drain region 264. Transistor 252 could correspond to transistor 102 of FIG. 1. Transistor 254 further comprises a gate 270, a source region 272 and a drain region 274. Transistor 254 could correspond to transistor 106 of FIG. 1. FIG. 4 also shows two transistors 282 and 284 formed inside a P well 288 and an N well 286. Transistor 282 further comprises a gate 290, a source region 292 and a drain region 294. Transistor 282 could correspond to transistor 103 of FIG. 1. Transistor 284 further comprises a gate 280, a source region 282 and a drain region 284. Transistor 284 could correspond to transistor 107 of FIG. 1.

Lin '129, Fig. 18:



NMOS transistor

Fig. 18

Lin '129, col. 9:

Please refer to FIGS. 18 and 19 which show the triple-well structure which is suitable for both NMOS and PMOS transistors in the dual pumping circuit of the present invention. The triple-well structure MOSFET with p-substrate technology is well known for those skilled in the art and will not be described in the details. FIG. 18 shows a NMOS transistor that is used in the negative dual pumping circuit in FIG. 15 and FIG. 19 shows a PMOS transistor that is used in the positive dual pumping circuit in FIG. 5. The NMOS transistor in FIG. 18 has a bias voltage of the n-well to the supply voltage Vdd. In FIG. 19, the voltage difference between the n-well and the source and drain of the PMOS transistor is close to zero so the threshold voltage is minimized having a Vtp of -0.89V and body effect is eliminated.

Lin '129, cols. 8-9:

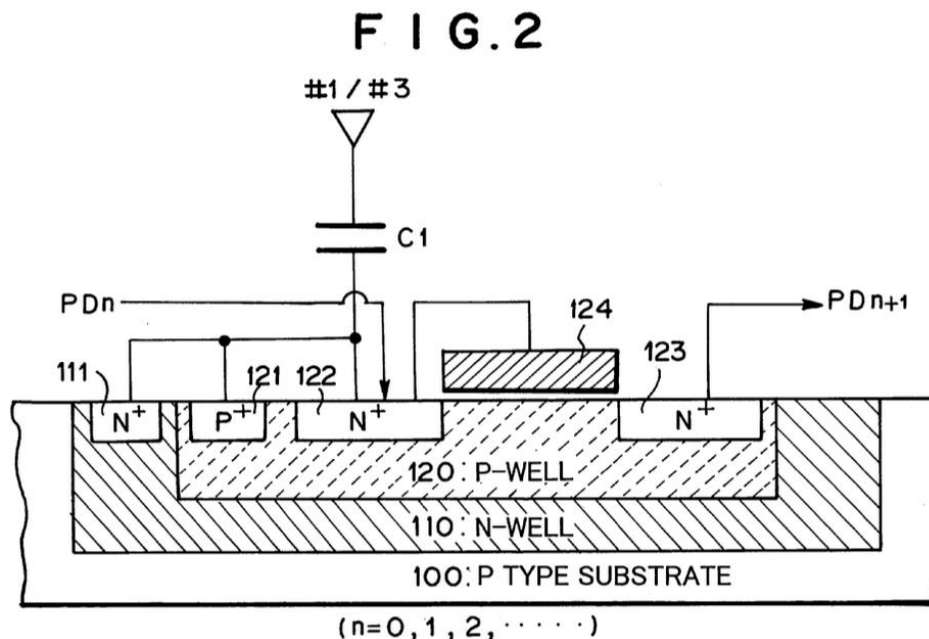
Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS

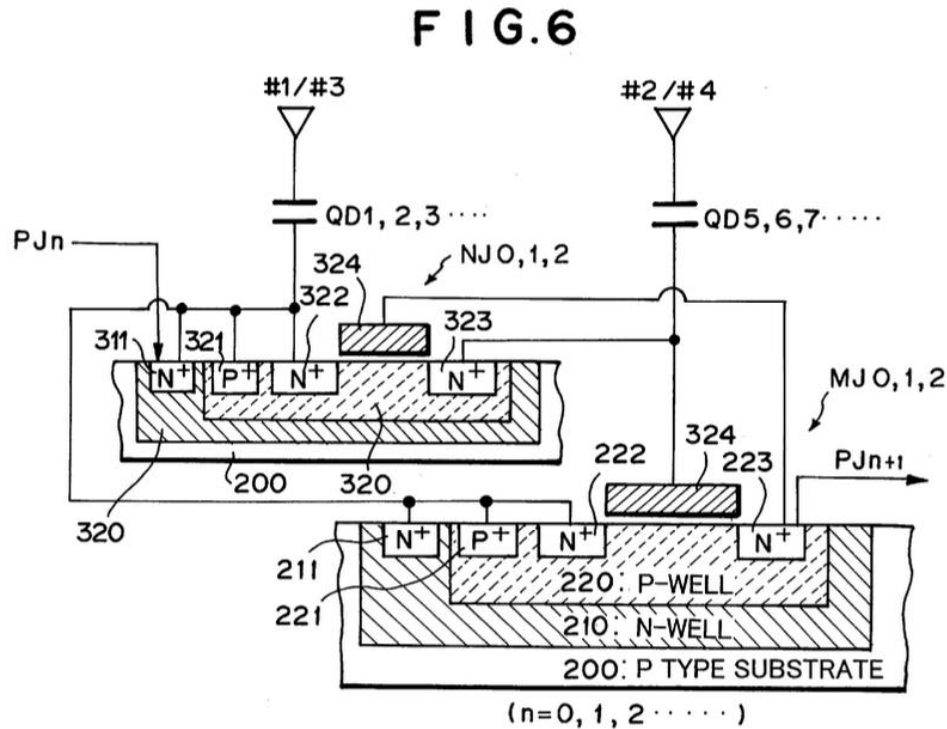
and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.

Please continue to refer to FIG. 16 which shows another embodiment of the present invention with the addition of an

Miki, Fig. 2:



Miki, Fig. 6:



Miki, col. 7:

Each of the transfer transistors MD0 to MD3 of the booster cells is composed of a triple-well semiconductor shown in FIG. 2. The triple-well semiconductor is composed of an N type first well 110 and a P type second well 120. The N type first well is formed on a P type semiconductor substrate 100. The P type second well 120 is formed on the N type first well 110. The semiconductor substrate 100 of each of the transfer transistors MD0 to MD3 is connected to a reference voltage. An output terminal PDn of a booster cell in the preceding stage, an N+ diffusion layer 111 in the first well 110, a P+ diffusion layer 121 in the second well 120, an N+ diffusion layer 122 in the second well 120, a first terminal of the capacitor C1, and a gate 124 of each of the transfer transistors MD0 to MD3 are connected. The conduction type of the first well 110 is the same as the conduction type of the N+ diffusion layer 111. The conduction type of the second well 120 is the same as the conduction type of the P+ diffusion layer 121. The conduction type of the second well 120 is different from the conduction type of the N+ diffusion layer 122. The N+ diffusion layer 123 in the second well 120 is an output terminal PDn+1 of the booster cell.

Miki, col. 9:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

FIG. 6 is a sectional view showing a real example of the structure of each booster cell shown in FIG. 5. As shown in FIG. 6, each booster cell is composed of a triple-well semiconductor device. Each transfer transistor MJn comprises an N type first well 210 and a P type second well 220. The N type first well 210 is formed on a P type semiconductor substrate 200. The P type second well 220 is formed on the N type first well 210. Each transfer transistor NJn comprises an N type first well 310 and a P type second well 320. The N type first well 310 is formed on a P type semiconductor substrate 200. The P type second well 320 is formed on the N type first well 310.

The P type semiconductor substrates 200 and 300 are connected to a reference voltage. N+ diffusion layers 211 and 311 in the first wells 210 and 310, P+ diffusion layers 221 and 321 in the second wells 220 and 320, N+ diffusion layers (drains) in the second wells 220 and 320, and first terminals of capacitors QD1 and QD2 are directly connected. The conduction type of the first wells 210 and 310 is the same as the conduction type of the N+ diffusion layers 211 and 311. The conduction type of the second wells 220 and 320 is the same as the conduction type of the P+ type diffusion layers 221 and 321. The conduction type of the second wells 220 and 320 is different from the conduction type of the N+ diffusion layers (drains) 222 and 322.

N+ diffusion layers (sources) 323 of the transfer transistors NJ0 to NJ3, gates 224 of the transfer transistors MJ0 to MJ3, and first terminals of capacitors QD5 and QD6 are directly connected. Gates 324 of the transfer transistors NJ0 to NJ3 and N+ diffusion layers (sources) 223 of the transfer transistors MJ0 to MJ3 are connected. A diffusion layer 223 of the second well 220 is an output terminal of the booster cell.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

1[e] wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal;

The Omnibus References disclose and/or render obvious wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal.

See, e.g.:

Hung, col. 1:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The present invention relates to using triple well transistors to increase the efficiency of a charge pump. The inventive charge pump comprises a plurality of pumping transistors arranged to increase the voltage level, or push the voltage level to a negative value, from a first pumping transistor to a last pumping transistor in response to clock pulses applied to these pumping transistors. At least one of the plurality of pumping transistors has a source and a drain region of a first conductivity type formed on a first well having an opposite conductivity type.

Lin '129, col. 3:

According to the claimed invention, a method for the first stage of the dual pumping circuit is provided which includes supplying an input voltage to the source terminals of the main pass transistors of the first pumping unit and the second pumping unit; during interval one to three, the first pumping unit performs charge sharing while the second pumping unit performs pre-charge; in interval one, rendering the main pass transistors of the first pumping unit and the second pumping unit, the substrate transistor of the second pumping unit, and the boosting transistor of the first pumping unit off, and the substrate transistor of the first pumping unit and the boosting transistor of the first pumping unit on; following in interval two, rendering the main pass transistor of the first pumping unit, the substrate transistor of the first pumping unit, and the boosting transistor of the second pumping unit on, and the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off; and continuing in interval three, rendering the main pass transistor of the first pumping unit, the boosting transistor of the first pumping unit, the substrate transistor of the second pumping unit, and the main pass transistor of the second pumping unit off, the boosting transistor of the second pumping unit, and the substrate transistor of the first pumping unit on.

Lin '129 at 5:64-6:3 (“For the subsequent stages, the output from every stage is commonly electrically coupled to the voltage controller of the subsequent stages so the partially pumped output voltage from each stage is used as the voltage to control the main pass transistors of the subsequent stages so the voltage difference of the source/drain and the body of all the subsequent stages is close to zero.”).

Lin '129 at col. 6:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please sequentially refer to FIGS. 8–13 which show the operation of one exemplary stage of the dual pumping circuit of the present invention. In FIGS. 8–13, each stage of the dual pumping circuit comprises a first pumping unit 802 and a second pumping unit 804 which are identical to each other and mirrored along an imaginary line i (shown only for explanation). The first pumping unit 802 comprises a first main pass PMOS transistor 812, a first boosting PMOS transistor 814, a first substrate PMOS transistor 816, a first small capacitor 818, and a first large capacitor 820. Similarly the second pumping unit comprises a second main pass PMOS transistor 822, a second boosting PMOS transistor 824, a second substrate PMOS transistor 826, a second small capacitor 828, and a second large capacitor 830. The first and the second pumping units alternately perform charge sharing which indicates that either pair of the clock pulses ϕ_a and ϕ_b or ϕ_c and ϕ_d remains unchanged while the other pair of the clock pulses revert from high to low and vice versa within a time span of half a period. The pair of clock pulses ϕ_a and ϕ_b is used to control the first pumping unit 802 and the pair of clock pulses ϕ_c and ϕ_d is used to control the second pumping unit 804. During intervals 1–3, the first pumping unit 802 performs charge sharing while the second pumping unit performs pre-charge and during intervals 4–6, the second pumping unit 804 performs charge sharing while the first pumping unit performs pre-charge.

Miki, Col. 2:

The transfer transistors shown in FIG. 16 are n-type MOS transistors formed on a p type substrate as shown in FIG. 18. An output PDn of a booster cell in a preceding stage is connected to a drain diffusion layer N+. In addition, a capacitor QQ1 (QQ3/QQ2) is connected to a gate of the n-type MOS transistor. An output PDn+1 is supplied from a source of the n-type MOS transistor to a transfer transistor in the next stage.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

1[f] a first boosting cell row including N stages ($N \geq 1$) of the boosting cells;

The Omnibus References disclose and/or render obvious a first boosting cell row including N stages ($N \geq 1$) of the boosting cells.

See, e.g.:

Lin '129, Fig. 5:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

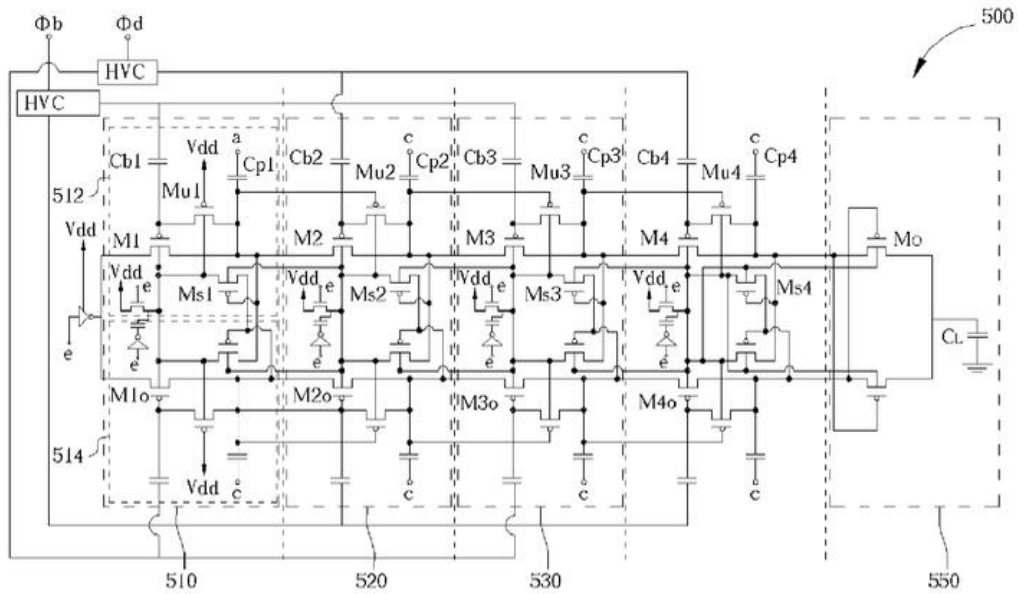


Fig. 5

Lin '129, Fig. 15:

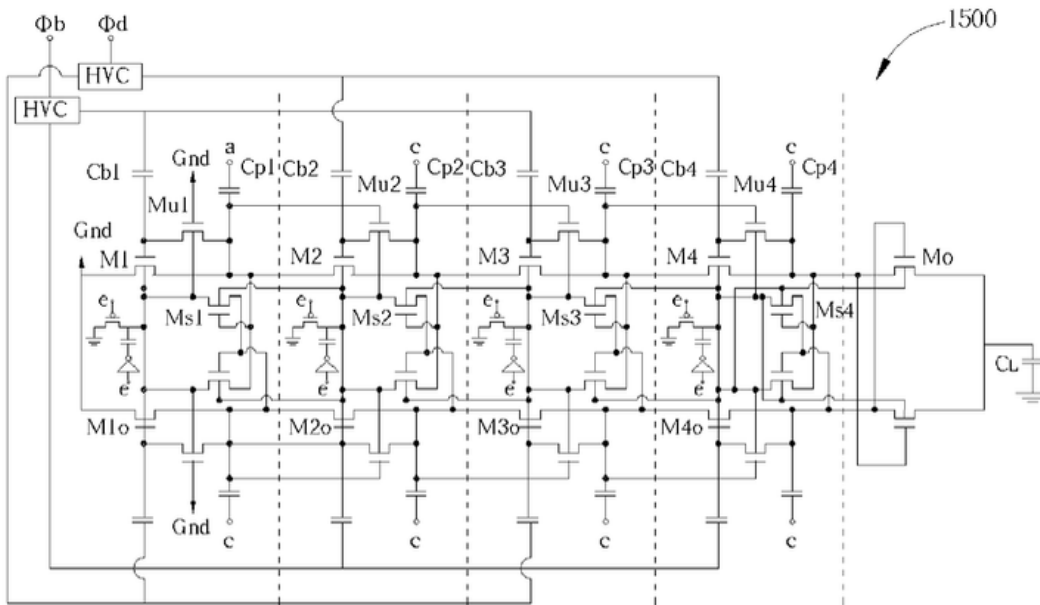


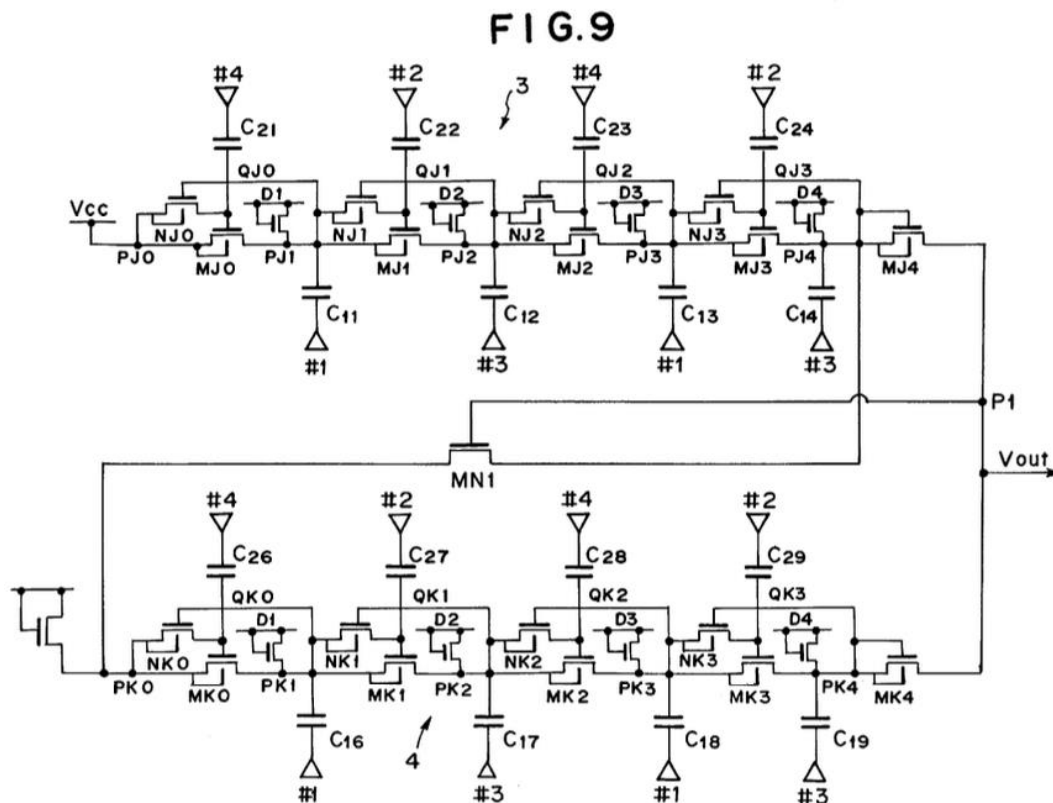
Fig. 15

Lin '129, col. 5:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The dual pumping circuit 500 comprises four serially linked stages 510, 520, 530, and 540 for achieving the required output voltage V_{out} from a low supply voltage V_{dd} . The positive dual pumping circuit 500 uses PMOS transistors based on triple-well with p-substrate technology which differs slightly that the negative dual pumping circuit 1500 that uses NMOS transistors. The stages 510, 520, 530, and 540 are all identical and each stage is comprised of a mirror structure further comprising an identical pair of a first pumping unit 512 and a second pumping unit 514. The first pumping unit 512 and the second pumping unit 514 of each stage are respectively electrically coupled to the first pumping unit and the second pumping unit of the preceding and subsequent stages with the exception that the first stage 510 of the dual pumping circuit is electrically coupled to an input voltage V_{dd} which is further electrically coupled to an inverter and the last stage 540 of the dual pumping circuit is electrically coupled to an output stage 550. The output V_{out} of the dual pumping circuit is electrically coupled to an output capacitor C_L and is cross-coupled so that the charge can be transferred to the output more efficiently.

Miki, Fig. 9:



To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

1[g] a second boosting cell row including M stages ($M \geq 1$) of the boosting cells; and

The Omnibus References disclose and/or render obvious a second boosting cell row including M stages ($M \geq 1$) of the boosting cells.

See, e.g.:

Claim limitation 1[f], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

1[h] at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and

The Omnibus References disclose and/or render obvious at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row.

See, e.g.:

Lin ’129, Fig. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

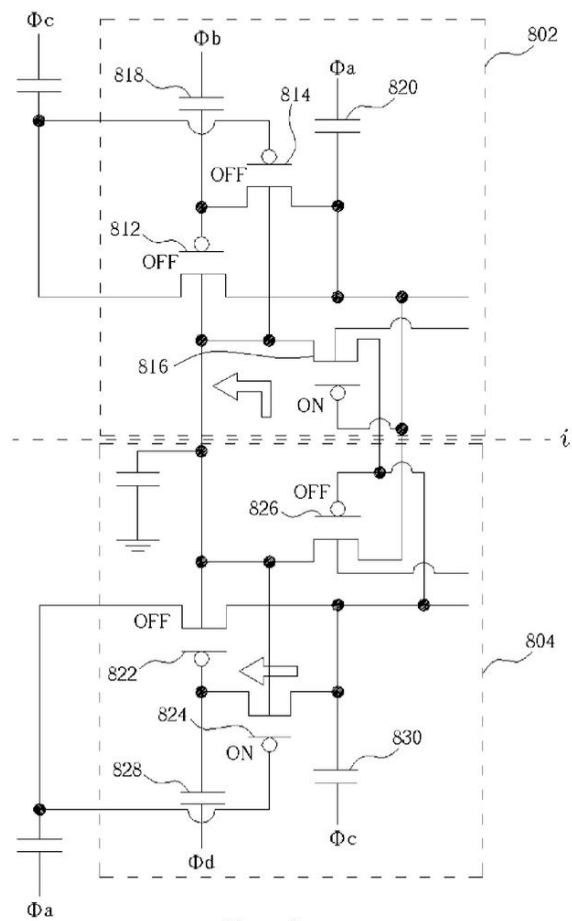


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

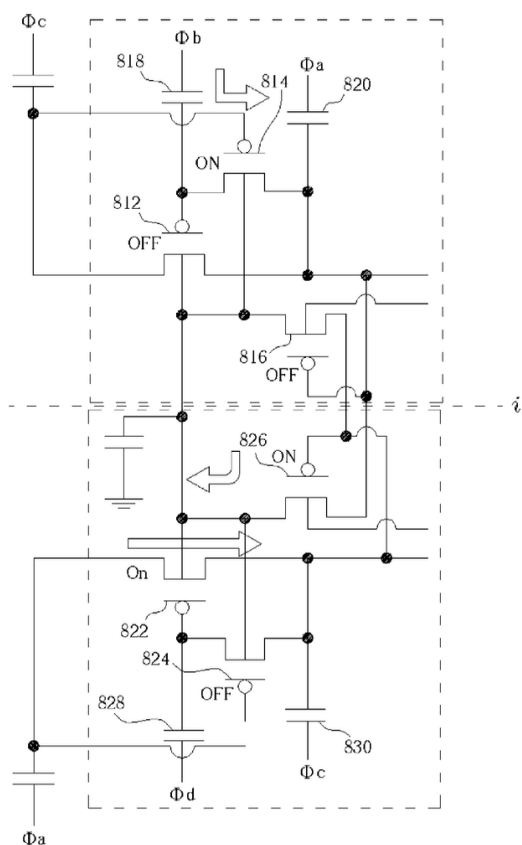


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Please refer to FIG. 14 which shows the HVC used for
 35 generating high voltage clock pulses from a low input
 voltage. The input voltage V_{in} is inputted to a first inverter
 1402 and then to a second inverter 1404 where the voltage
 signal is transferred to both a first capacitor 1406 to a third
 inverter 1408 that is further electrically coupled to a second
 40 capacitor 1416. The first capacitor 1406 is electrically
 coupled to the source of the first NMOS transistor 1410 and
 the gate of the transistor 1412 and the second capacitor 1416
 is electrically coupled to the source of the second NMOS
 transistor 1412 and the gate of the first NMOS transistor
 45 1410. As a result, the two NMOS transistors 1410 and 1412
 are cross-coupled to increase the amplitude of the input
 voltage V_{in} . To substantially reduce body effects, the body
 of the third PMOS transistor 1414 is electrically coupled to
 the drain of a fifth NMOS transistor 1424 whose source is
 50 electrically coupled to V_{dd} and gate is controlled by clock
 pulse ϕ_e which also at the same time control the third
 capacitor 1420 through a inverter 1422. The high voltage
 clock pulses ϕ_b and ϕ_d can be achieved by such cross-
 coupling scheme to increase the pumping gain at low supply
 55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 (“Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.”).

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50 a dual pumping circuit that can be implemented in either positive or negative with provides good pumping performance at low supply voltage (1V to 2V) using the popular triple-well technology. The dual pumping circuit uses four-phase clocks that has one pair of identical but out of phase 55 clocks. The other two of the clocks may be chosen to be generated by a high voltage circuit to provide better pumping at low voltage. The positive dual pumping circuit uses PMOS transistors and the negative pumping circuit uses NMOS transistors where the transistors have special sub- 60 strate connection to avoid body effect and p-n junction conduction.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, 65 that above disclosure should be construed as limited only by the metes and bounds of the appended

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

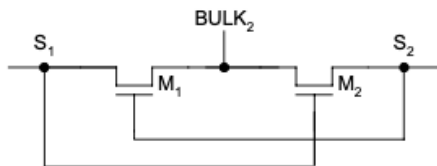


Fig. 15.14. Dynamic biasing of the bulk nodes

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The Omnibus References disclose and/or render obvious an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.

See, e.g.:

Lin '129, Fig. 8:

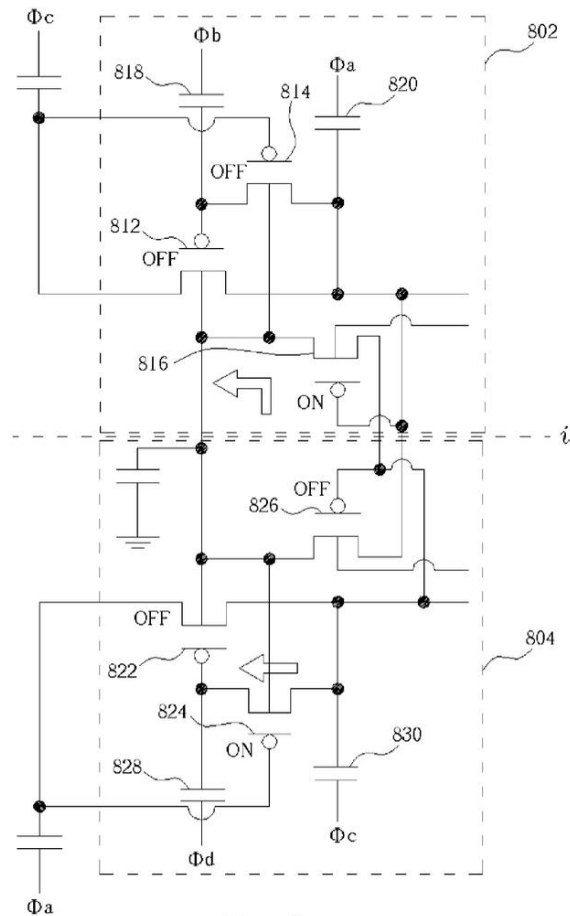


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

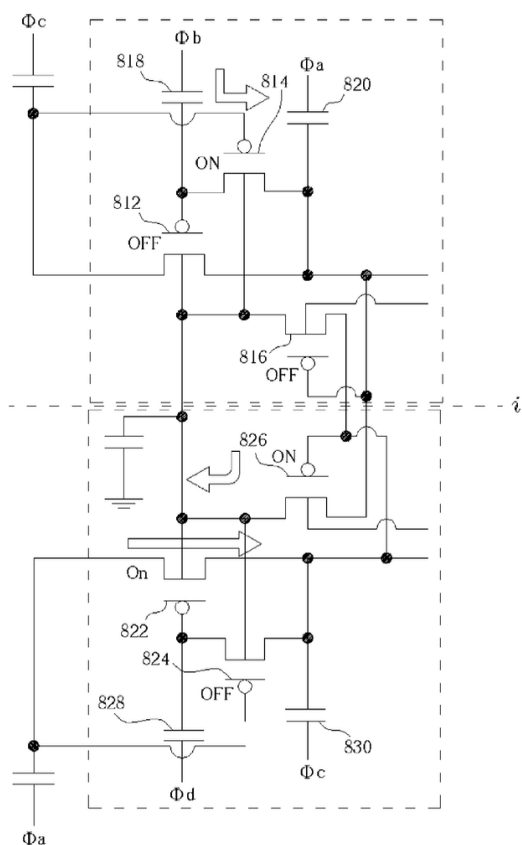


Fig. 12

Lin '129, col. 5:

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Lin '129, col. 8:

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Lin '129, col. 9:

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1[j] wherein the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

The Omnibus References disclose and/or render obvious wherein the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.

See, e.g.:

Hung, Fig. 3:

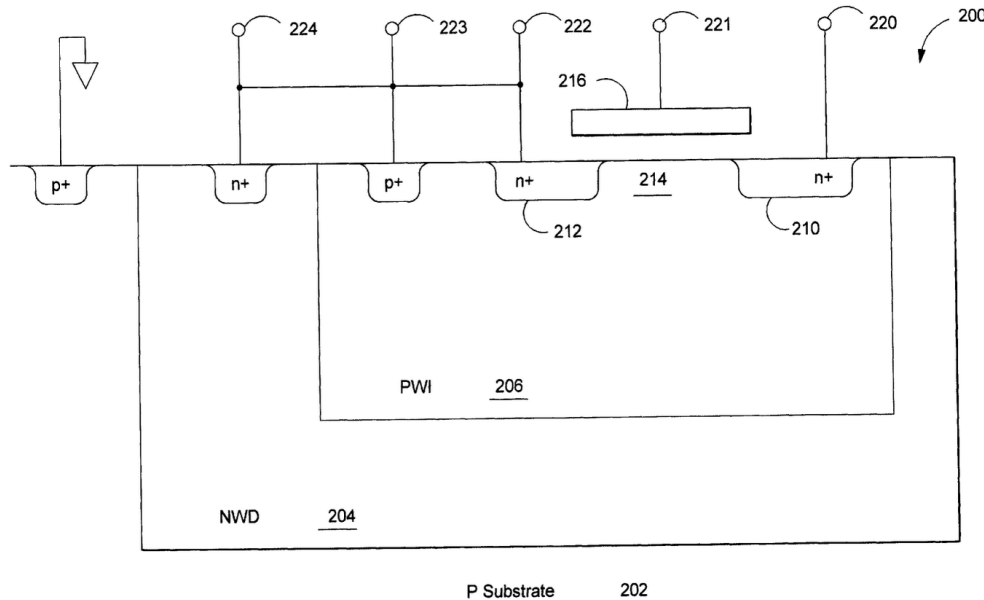


FIG.3

Hung, col. 3:

FIG. 3 shows, schematically, a cross sectional view of a ¹⁰ triple well NMOS transistor 200 that can be used for transistors 102–110 of FIG. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed in substrate 202, and a P well 206 is formed in N well 204. An N+ type ¹⁵ drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain ²⁰ region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220–224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are inter- ²⁵ changeable when the charge pump is activated because either terminal may have higher potential than the other.

Hung, col. 3:

In one embodiment of the present invention, the potential of source region 212, P well 206 and N well 204 are set to the same value. One way to meet this condition is to ³⁰ electrically connecting terminals 222, 223 and 224. The potential of substrate 202 is normally set to ground. This arrangement creates a PN diode between P well 206 and drain region 210. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. ³⁵ This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an “extra diode.” As explained in more detail below, this extra diode has the following advantageous effects: ⁴⁰

Lin '129, Fig. 8:

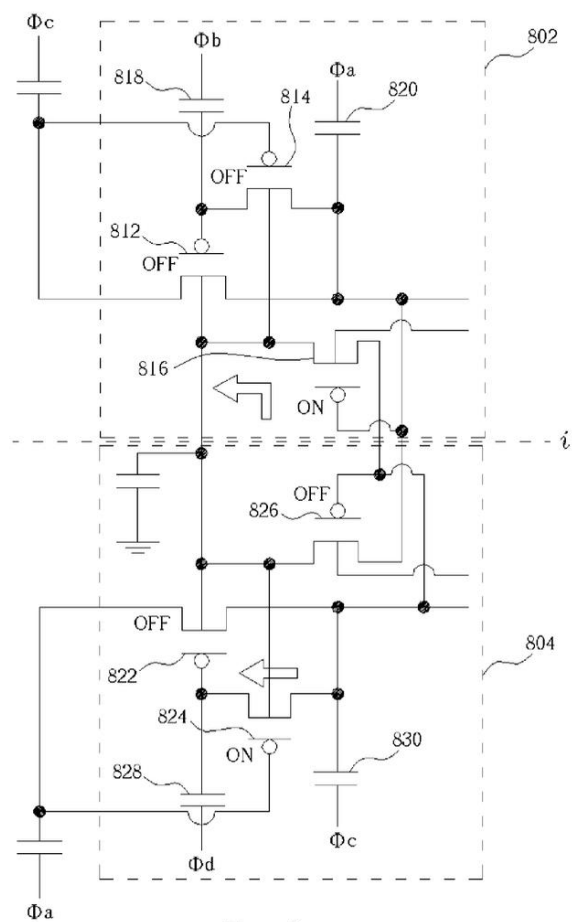


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

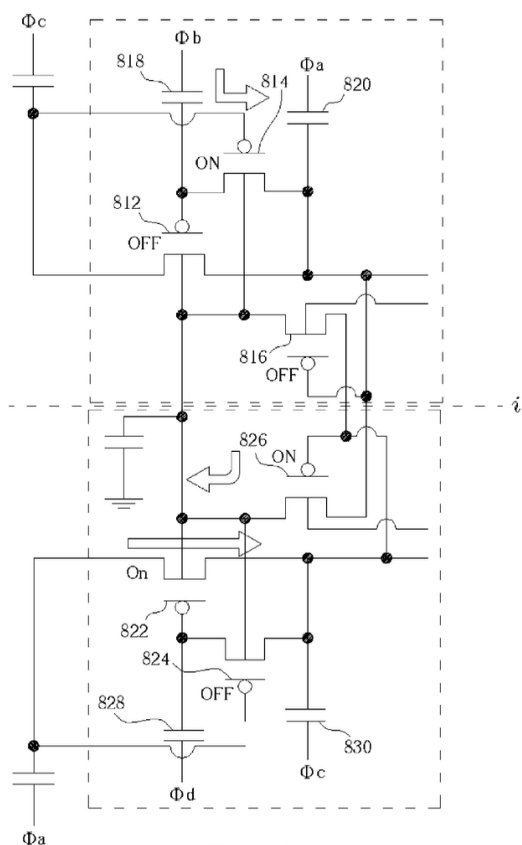


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please refer to FIG. 14 which shows the HVC used for
35 generating high voltage clock pulses from a low input
voltage. The input voltage V_{in} is inputted to a first inverter
1402 and then to a second inverter 1404 where the voltage
signal is transferred to both a first capacitor 1406 to a third
inverter 1408 that is further electrically coupled to a second
40 capacitor 1416. The first capacitor 1406 is electrically
coupled to the source of the first NMOS transistor 1410 and
the gate of the transistor 1412 and the second capacitor 1416
is electrically coupled to the source of the second NMOS
transistor 1412 and the gate of the first NMOS transistor
45 1410. As a result, the two NMOS transistors 1410 and 1412
are cross-coupled to increase the amplitude of the input
voltage V_{in} . To substantially reduce body effects, the body
of the third PMOS transistor 1414 is electrically coupled to
the drain of a fifth NMOS transistor 1424 whose source is
50 electrically coupled to V_{dd} and gate is controlled by clock
pulse ϕ_e which also at the same time control the third
capacitor 1420 through a inverter 1422. The high voltage
clock pulses ϕ_b and ϕ_d can be achieved by such cross-
coupling scheme to increase the pumping gain at low supply
55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 ("Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.").

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50
a dual pumping circuit that can be implemented in either
positive or negative with provides good pumping perfor-
mance at low supply voltage (1V to 2V) using the popular
triple-well technology. The dual pumping circuit uses four-
phase clocks that has one pair of identical but out of phase 55
clocks. The other two of the clocks may be chosen to be
generated by a high voltage circuit to provide better pump-
ing at low voltage. The positive dual pumping circuit uses
PMOS transistors and the negative pumping circuit uses
NMOS transistors where the transistors have special sub- 60
strate connection to avoid body effect and p-n junction
conduction.

Those skilled in the art will readily observe that numerous
modifications and alterations of the device may be made
while retaining the teachings of the invention. Accordingly, 65
that above disclosure should be construed as limited only by
the metes and bounds of the appended

Park '791, Fig. 7:

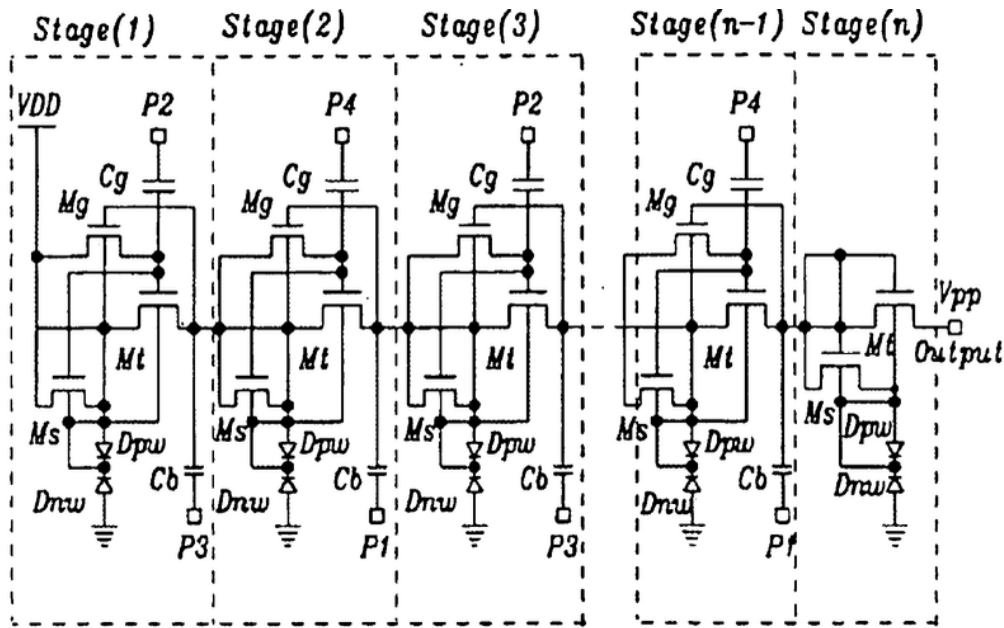


FIG. 7

Park '791, Fig. 13:

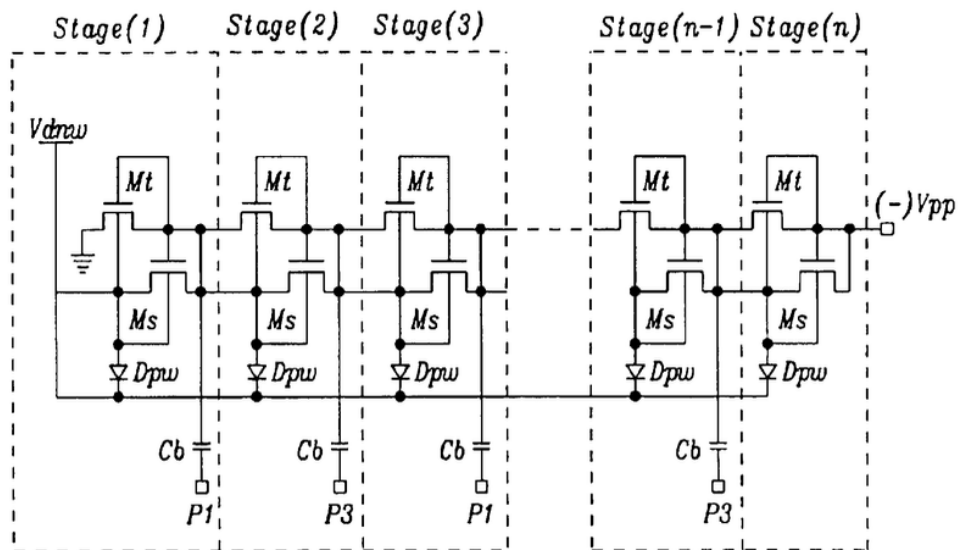


FIG. 13

Park '791, col 4:

25 The auxiliary device, which is used for pre-charging a
voltage on the gate of the charge transfer device, couples the
input signal of each stage to the gate of the charge transfer
device; and therefore, increases the boost coupling effect on
30 the charge transfer MOS device, which results in increasing
a signal level at the source (output) of the charge transfer
device. The auxiliary device, that is used for buffering the
drain of the charge transfer device from the P-well and the
N-well, couples the drain voltage of the charge transfer
35 device to the P-well and the deep N-well to reduce the body
effect and to improve capacitive coupling effect on the drain
of charge transfer MOSFET device by reducing the effects
of the P-well and Deep N-well parasitic capacitance.

40 It should be noted that although the present invention has
been oriented to a charge pump circuit formed from
N-channel MOSFET devices in a P-well within a deep
N-well on a P-substrate, a similar charge pump circuit could
be formed from P-channel MOSFET devices in an N-well
within a deep P-well residing on an N-substrate.

Park '791, col. 5:

Continuing to refer to FIG. 7, an input voltage of a stage
is applied to the drain of the charge transfer MOS device Mt
within the stage. This same input voltage is coupled to the
gate of the charge transfer MOS device Mt by means of an
auxiliary MOS device Mg and clock signal P3 in odd 50
numbered stages and clock signal P1 in even number stages.
Similarly, a boosted input signal to a stage is coupled to the
P-well Dpw and deep N-well Dnw by the auxiliary MOS
device Ms, which is gated by the gate signal of the charge
transfer MOS device Mt. Clock P2 for odd numbered stages 55
and clock P4 for even number of stages are applied to the
gate of the charge transfer MOS device through capacitor
Cg.

Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Park '791, col. 7:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

A negative high voltage output charge pump circuit can also be realized using the same triple-well structure of the present invention, except that deep N-well is connected to 50 V_{dnw}, which is a positive voltage and can be either the power supply VDD, or ground. FIG. 12 shows a cross-sectional view of the charge pump circuit of present invention for a negative high voltage output. The charge transfer MOS device M_t and auxiliary MOS device M_s are formed 55 in their own P-well which act as substrate of the MOS devices. The deep N-well can be shared with other pumping stages and connected to ground or power supply VDD. The source S₂ and drain D₂ of the auxiliary MOS M_s are coupled to the P-well and the drain D₁ of the charge transfer 60 MOS device M_t, respectively. The drains D₁ and D₂ and the gates of the charge transfer device M_t and auxiliary device M_s are coupled together and are further connected to the coupling capacitor C_b.

Park '791, cols. 7-8:

FIG. 13 is a circuit diagram of an embodiment of the 65 present invention of a charge pump for generating a negative voltage output. The circuit uses an N-channel MOSFET as

charge transfer device M_t and an auxiliary device M_s. The pumping stages are connected in series from ground to the negative output voltage (-)V_{pp}. Each pumping stage includes one charge transfer MOS device M_t, one auxiliary 5 MOS device M_s and one coupling capacitor C_b. The P-well within each pump stage, Stage (1), Stage (2), Stage (3), Stage (n-1) and Stage (n), resides within a deep N-well and isolates the circuitry of each stage. The deep N-well can be common for each P-well or separate for each P-well. The 10 auxiliary device M_s couples a boosted voltage to the P-well to reduce body effects on the pumped voltage within each stage. The diode D_{pw} represents the parasitic diode junction between the P-well and the deep N-well. A positive voltage V_{dnw}, which can be either VDD or ground, is applied to the deep N-well to insure that the diode D_{pw} remains back 15 biased throughout the negative charge pump operations.

Park '791, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The circuit operation of the negative charge pump is carried out in the same manner as the positive charge pump circuit, except that the input of the charge pump circuit is coupled to the ground, instead of VDD. A two clock scheme using clocks P1 and P3, or P2 and P4, shown in FIG. 8 for the positive charge pump circuit can be used for the negative charge pump circuit. When the charge transfer MOS device Mt in a first pump stage is turned on by a clock signal, a boosted negative charge is created at the output of a first pump stage, which is coupled to the drain nodes of the charge transfer MOS device Mt and auxiliary MOS device Ms. The boosted negative charge is transferred to the input of a second pump stage connected to the output of the first pump stage. The boosted negative charge is coupled to a source of the charge transfer MOS device Mt in the second stage. At the same time, the auxiliary MOS device Ms of the first stage is also turned on so that the boosted negative charge of the output of the first pump stage is coupled to the P-well of the first pump stage. The coupling of the boosted negative charge to the P-well reduces the body effect on the charge transfer MOS device Mt, which results in an increased charge transfer efficiency.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

2[a] The booster circuit of claim 1, wherein

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

2[b] the first boosting cell row includes N stages ($N \geq 1$) of the boosting cells and at least one backflow preventing circuit;

The Omnibus References disclose and/or render obvious the first boosting cell row includes N stages ($N \geq 1$) of the boosting cells and at least one backflow preventing circuit.

See, e.g.:

Hung, col. 3:

It should be noted that a charge pump preferably includes⁵ other associated circuits, e.g., precharge and voltage regulation circuits. These circuits are well known by persons of ordinary skill in the art, and will not be described here.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Lin '129, Fig. 5:

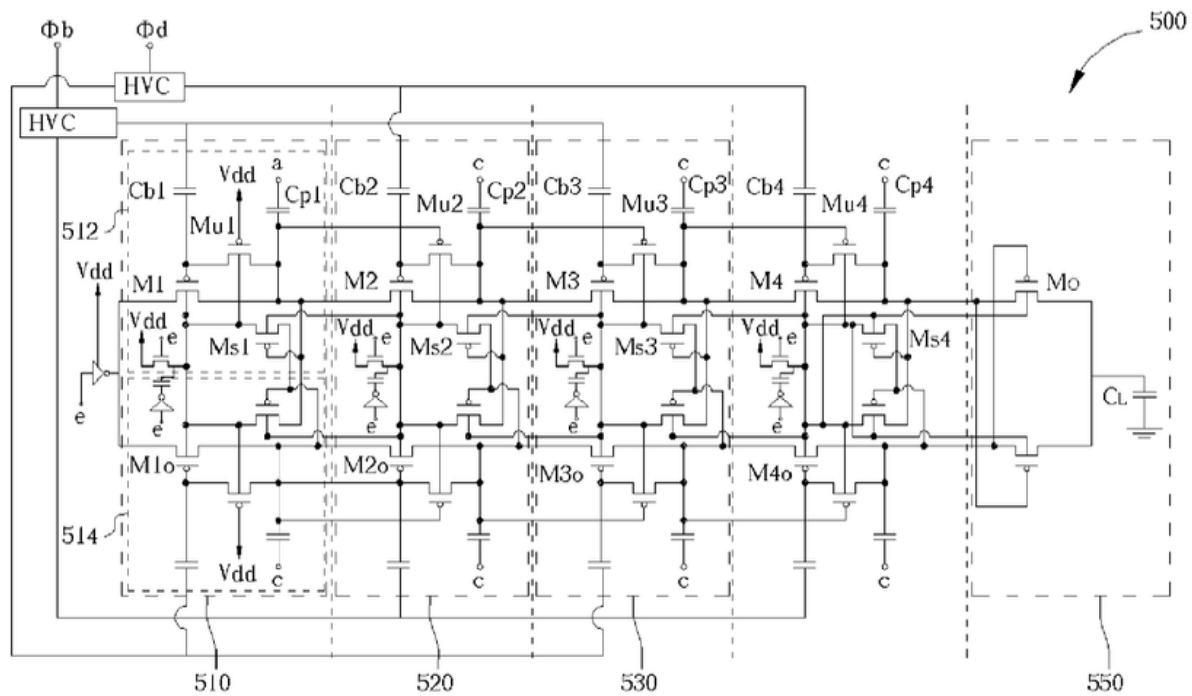


Fig. 5

Lin '129, Fig. 15:

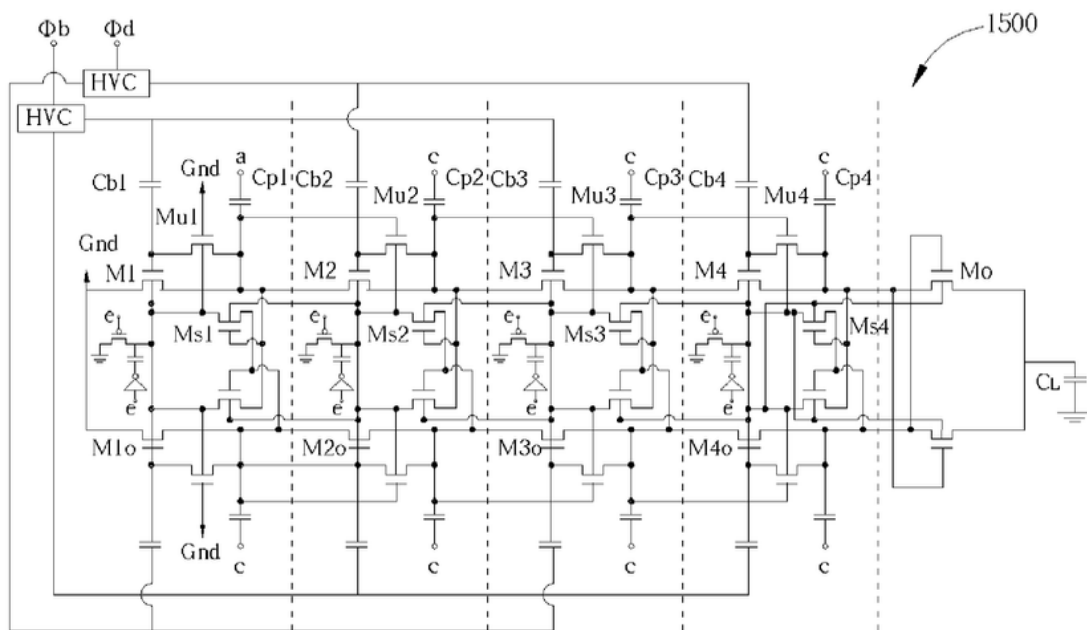


Fig. 15

Park '791, Fig. 11:

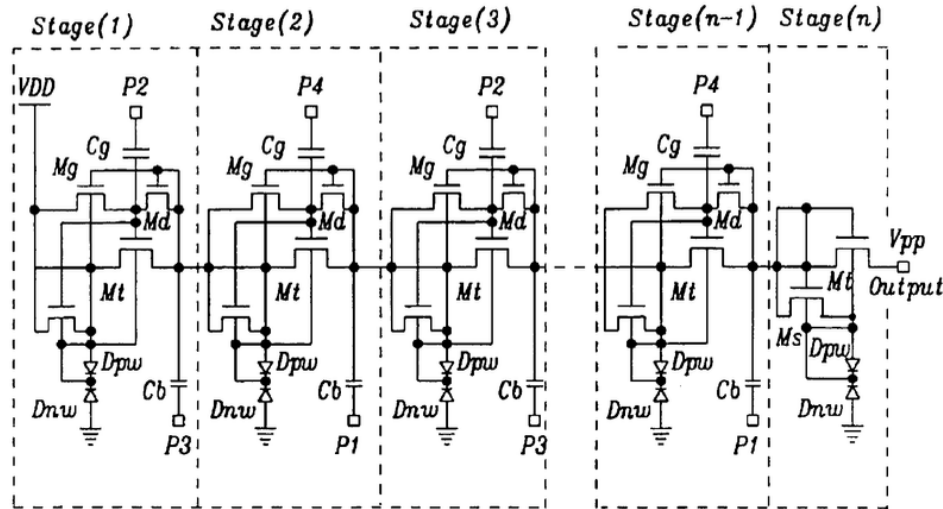


FIG. 11

Park '791, col. 7:

FIG. 11 shows a second embodiment of charge pump circuit diagram of the present invention. The basic components of the charge pump circuit are as same as the first embodiment of the present invention shown in FIG. 7, except that there is a pull-down N-channel MOSFET device Md. The charge pump circuit includes the charge transfer MOS device Mt, the auxiliary MOS device Mg, and auxiliary MOS device Ms contained within the same P-well inside a deep N-well for each stage. The pull-down MOS device Md, however, can be formed either on the same P-well inside a deep N-well or on the P-substrate. The drain and gate of the pull down device Md are connected to the gate of the charge transfer device Mt, and the source of the pull-down device Md is connected to the output of the pumping stage. The pull-down MOS device Md, which is connected as a diode, is used to prevent back flow of charge from the output to the input of the pumping stage in a situation when the gate voltage of charge transfer device Mt becomes high enough to turn on the charge transfer device Mt (even weakly) and when the clock signal coupled to the gate of the charge transfer device Mt changes from high level of VDD to low level of ground. When this situation occurs during operation, the pull-down MOS device Md keeps the charge transfer device Mt turned off which results in preventing the back flow of the charge from the output to the input of the pumping stage.

Campardo at 373-375:

15.4.3 Charge Pump Based on Pass Transistors

The diodes inside the pump are needed to establish the current direction and to prevent any charge from flowing towards the previous stage. The main drawback of the use of such components, apart from the technological complexity to realize them, is their high threshold voltage, i.e. the need of having a consistent voltage difference between drain and source, in order to have a charge transfer. It is clear that under these conditions the charge transfer between one stage and the following one cannot be complete.

The alternative to the diodes to obtain both charge transfer and node connections is represented by transistors used as switches. MOS behavior is involved, i.e.

374 15 Circuits Used in Program and Erase Operations

if the voltage applied to the gate is lower than its V_T the transistor is turned off, therefore there is no charge transfer and it is equivalent to an open switch. On the other hand if the voltage applied to the gate is higher than V_T , then there is a complete current transfer with a minimum voltage drop equal to the turn-on resistance of the transistor R_{ON} , multiplied by the transferred current. In the latter case, the transistor is equivalent to a closed switch

The circuit inevitably gets more complex and it occupies a larger area. In fact, besides the transfer capacitors and the two phases already present in a simple pump circuit, it is necessary to add two boost capacitors and two additional phases to better drive the switches as shown in Fig. 15.15.

Let's suppose to transfer charge from capacitor C_{T-1} to capacitor C_T , and at the same time to block the charge transfer between the two consecutive capacitors (C_T and C_{T+1}).

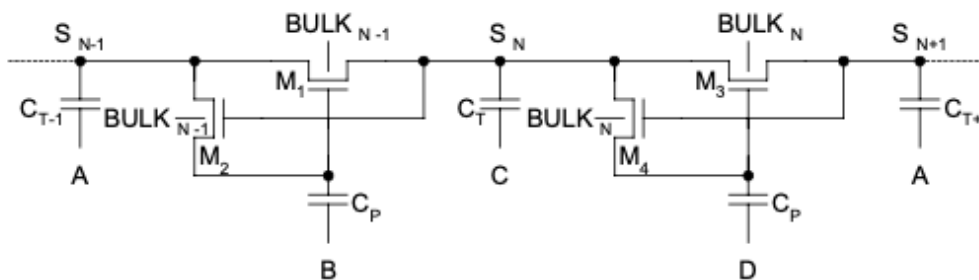


Fig. 15.15. Internal stages for a pump using pass-transistors

Let's start from the condition where no charge transfer occurs, i.e. pass transistors are switched off, and therefore B and D are at GND and C is at VDD. In this case, the gate of transistor M_1 is biased at a low potential (it is difficult to specify the value since it depends on the stage we are looking at and on the amount of discharge on C_p in the meanwhile), while node S_N is biased at VDD.

At this point, as it is possible to see from Fig. 15.16, phase A is triggered, thus applying the bootstrap to node S_{N-1} and transistor M_2 is turned off (C is still active) it is possible to precharge the upper plate of the capacitor C_p which drives the gate of the pass transistor M_1 . Once this phase is over, it is necessary that C returns to GND and that the gate of M_1 reaches a value that allows charge transfer between C_{T-1} and C_T . This condition can be obtained by activating phase B for an interval corresponding to a complete charge transfer between the two capacitors. Once the transfer is over, all the operations are repeated in reverse order: first B is lowered to GND, then phase C rises. Indeed at this point capacitor C_p connected to the gate of transistor M_3 pre-charges as long as A is active. When phase D is activated, charge transfer between C_T and C_{T+1} starts.

The biasing of the bulks of the pass-transistors exhibits the same issues encountered with the pumps where diodes were implemented using transistors (see Sect. 15.4.2).

15.4 Different Types of Charge Pumps 375

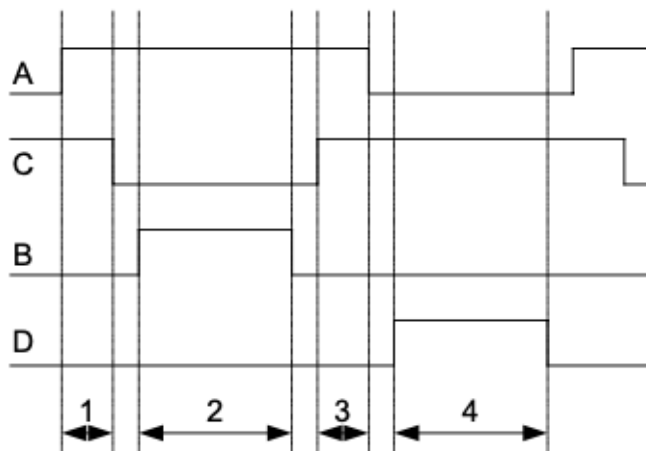


Fig. 15.16. Timing diagram of the phases for the pass-transistor pump: 1) precharge of capacitor C_p of transistor M_1 , 2) charge transfer between capacitors C_{T-1} and C_T , 3) precharge of capacitor C_p of transistor M_3 , 4) charge transfer between capacitors C_T and C_{T+1}

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

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2[c] the second boosting cell row includes M stages ($M \geq 1$) of the boosting cells and at least one backflow preventing circuit; and

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See, e.g.:

Hung, col. 3:

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Lin '129, Fig. 5:

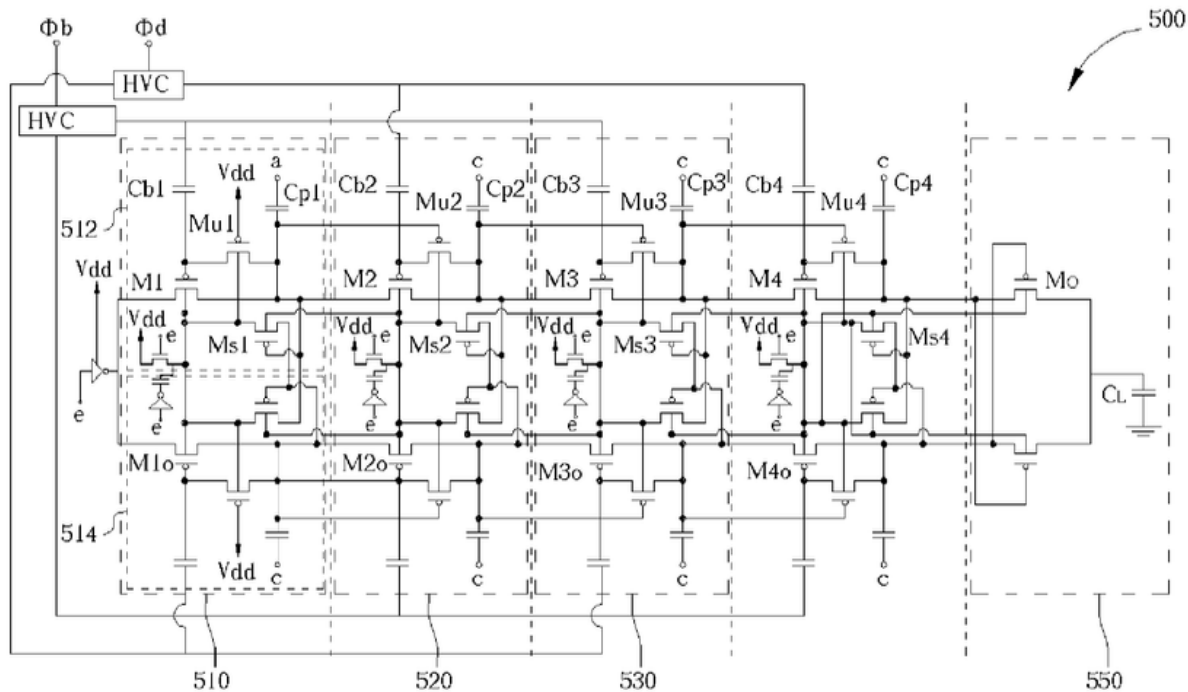


Fig. 5

Lin '129, Fig. 15:

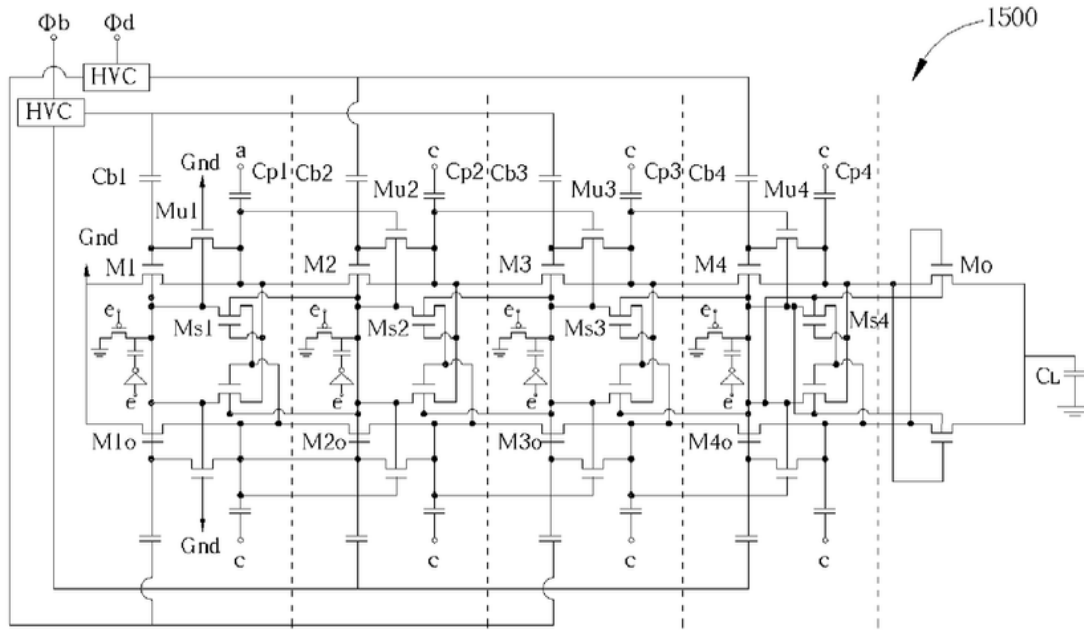


Fig. 15

Park '791, Fig. 11:

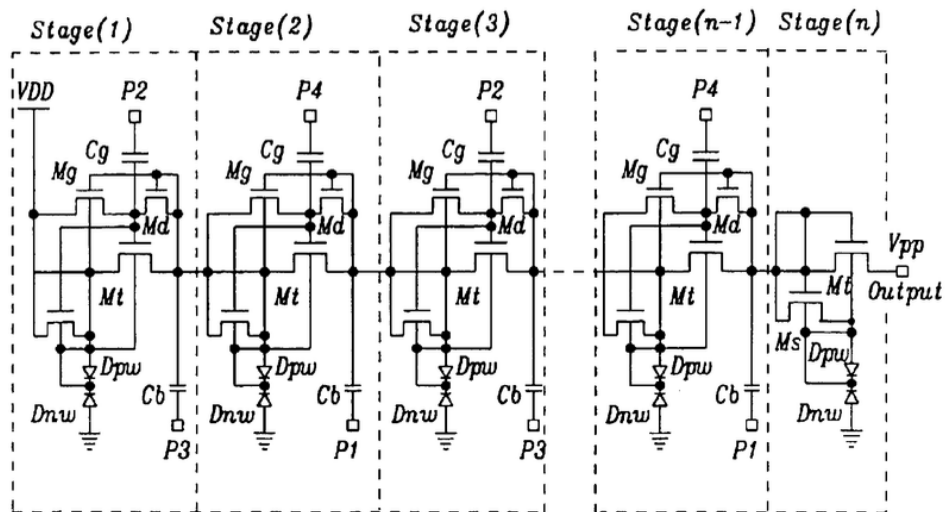


FIG. 11

Park '791, col. 7:

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Campardo at 373-375:

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374 15 Circuits Used in Program and Erase Operations

if the voltage applied to the gate is lower than its V_T the transistor is turned off, therefore there is no charge transfer and it is equivalent to an open switch. On the other hand if the voltage applied to the gate is higher than V_T , then there is a complete current transfer with a minimum voltage drop equal to the turn-on resistance of the transistor R_{ON} , multiplied by the transferred current. In the latter case, the transistor is equivalent to a closed switch

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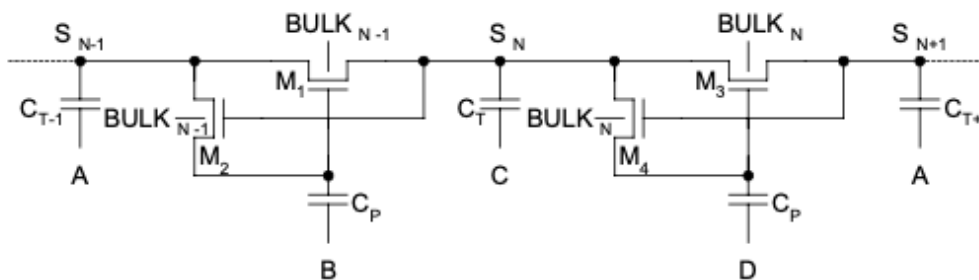


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15.4 Different Types of Charge Pumps 375

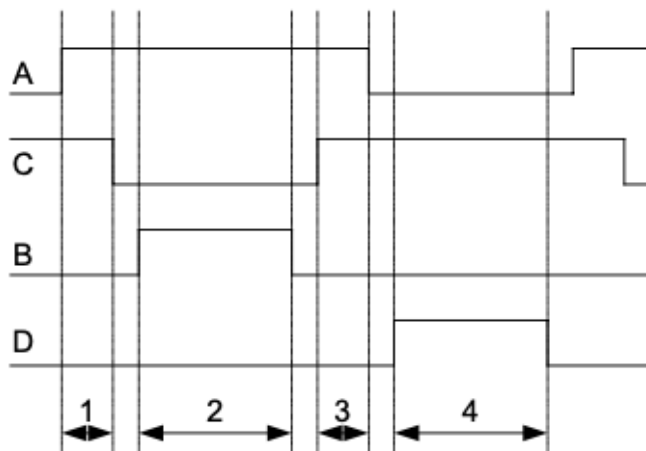


Fig. 15.16. Timing diagram of the phases for the pass-transistor pump: 1) precharge of capacitor C_p of transistor M_1 , 2) charge transfer between capacitors C_{T-1} and C_T , 3) precharge of capacitor C_p of transistor M_3 , 4) charge transfer between capacitors C_T and C_{T+1}

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

2[d] the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.

The Omnibus References disclose and/or render obvious the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one backflow preventing circuit of the first and second boosting cell rows.

See, e.g.:

Hung, Fig. 3:

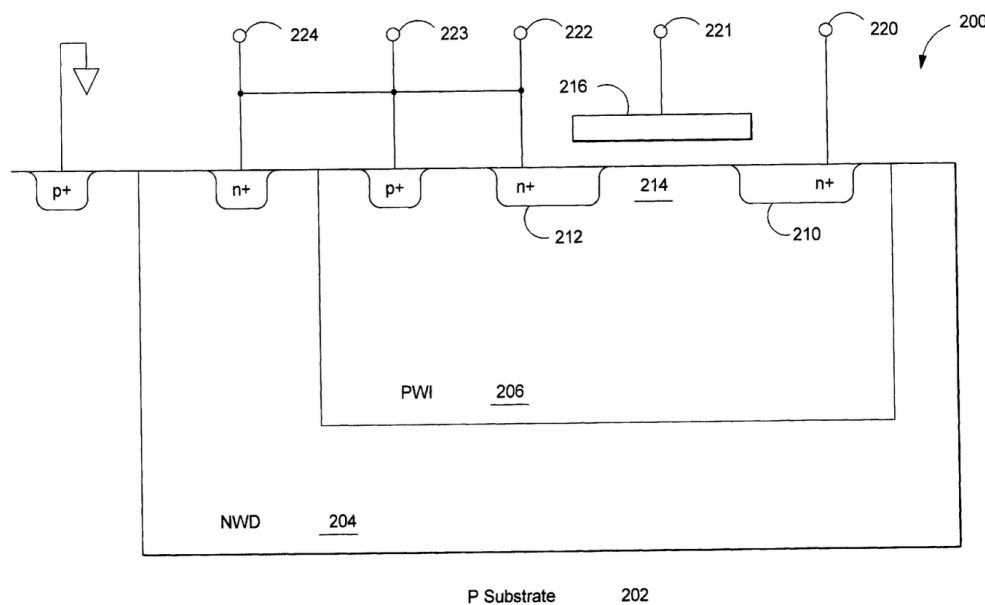


FIG.3

Hung, col. 3:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor **200** that can be used for transistors **102–110** of FIG. 1. Transistor **200** is fabricated on a p-type substrate **202**. An N well **204** is formed in substrate **202**, and a P well **206** is formed in N well **204**. An N+ type drain region **210** is formed in P well **206**, as is an N+ source region **212**. A channel region **214** is defined between source and drain regions in P well **206**. A polysilicon gate **216** is positioned above channel region **214**. A thin gate oxide is deposited between gate **216** and channel region **214**. Drain region **210**, gate **216**, source region **212**, P well **206**, and N well **204** are coupled to individual terminals **220–224**, respectively. Thus, triple well transistor **200** can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Hung, col. 3:

In one embodiment of the present invention, the potential of source region **212**, P well **206** and N well **204** are set to the same value. One way to meet this condition is to electrically connecting terminals **222**, **223** and **224**. The potential of substrate **202** is normally set to ground. This arrangement creates a PN diode between P well **206** and drain region **210**. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an “extra diode.” As explained in more detail below, this extra diode has the following advantageous effects:

Lin '129, Fig. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

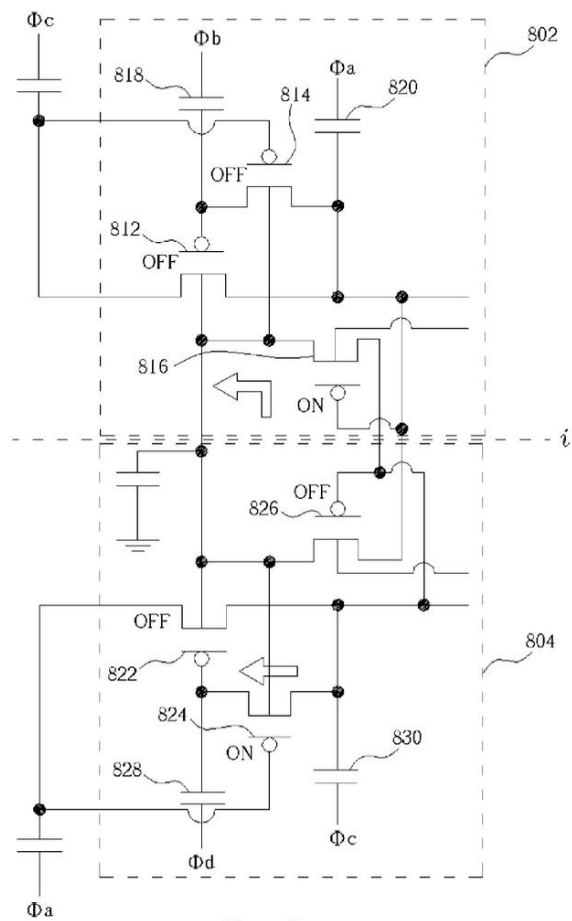


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

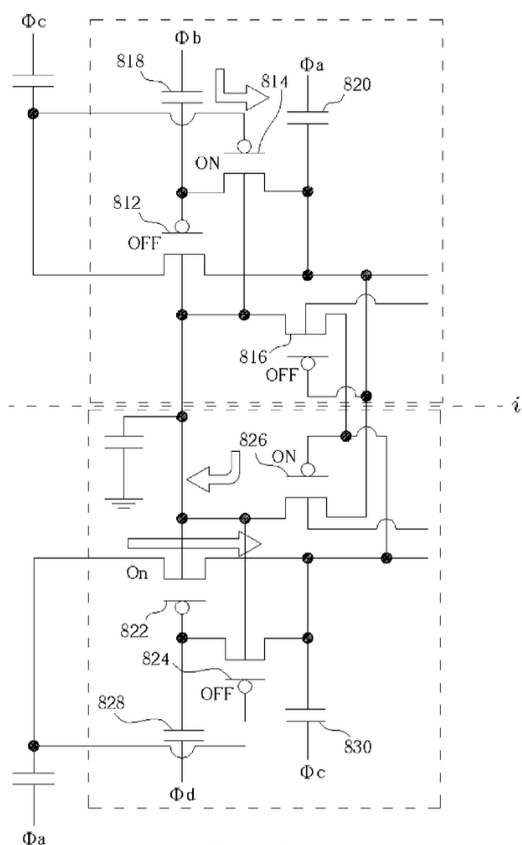


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please refer to FIG. 14 which shows the HVC used for
35 generating high voltage clock pulses from a low input
voltage. The input voltage V_{in} is inputted to a first inverter
1402 and then to a second inverter 1404 where the voltage
signal is transferred to both a first capacitor 1406 to a third
inverter 1408 that is further electrically coupled to a second
40 capacitor 1416. The first capacitor 1406 is electrically
coupled to the source of the first NMOS transistor 1410 and
the gate of the transistor 1412 and the second capacitor 1416
is electrically coupled to the source of the second NMOS
transistor 1412 and the gate of the first NMOS transistor
45 1410. As a result, the two NMOS transistors 1410 and 1412
are cross-coupled to increase the amplitude of the input
voltage V_{in} . To substantially reduce body effects, the body
of the third PMOS transistor 1414 is electrically coupled to
the drain of a fifth NMOS transistor 1424 whose source is
50 electrically coupled to V_{dd} and gate is controlled by clock
pulse ϕ_e which also at the same time control the third
capacitor 1420 through a inverter 1422. The high voltage
clock pulses ϕ_b and ϕ_d can be achieved by such cross-
coupling scheme to increase the pumping gain at low supply
55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 ("Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.").

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50
a dual pumping circuit that can be implemented in either
positive or negative with provides good pumping perfor-
mance at low supply voltage (1V to 2V) using the popular
triple-well technology. The dual pumping circuit uses four-
phase clocks that has one pair of identical but out of phase 55
clocks. The other two of the clocks may be chosen to be
generated by a high voltage circuit to provide better pump-
ing at low voltage. The positive dual pumping circuit uses
PMOS transistors and the negative pumping circuit uses
NMOS transistors where the transistors have special sub- 60
strate connection to avoid body effect and p-n junction
conduction.

Those skilled in the art will readily observe that numerous
modifications and alterations of the device may be made
while retaining the teachings of the invention. Accordingly, 65
that above disclosure should be construed as limited only by
the metes and bounds of the appended

Park '791, Fig. 7:

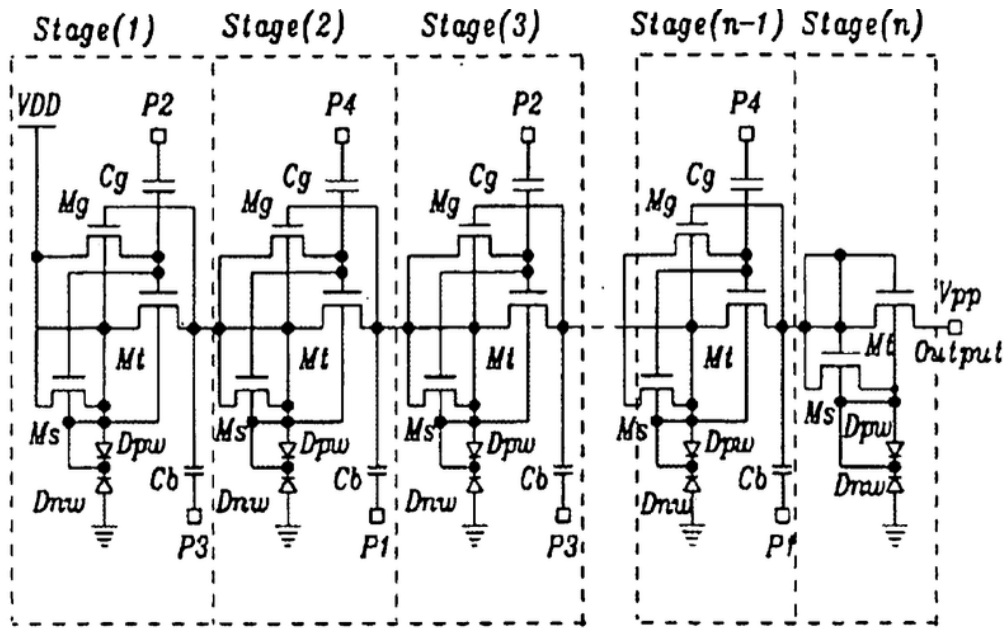


FIG. 7

Park '791, Fig. 13:

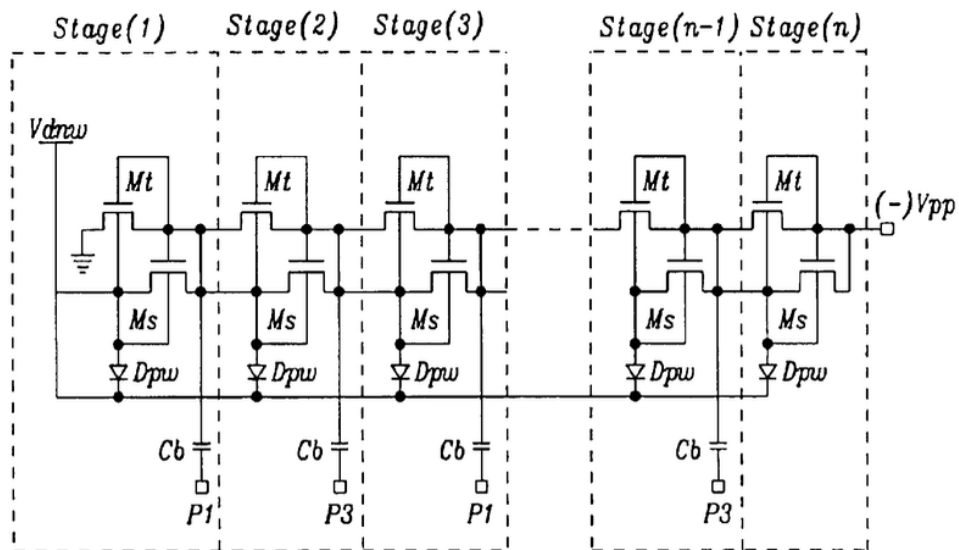


FIG. 13

Park '791, col 4:

25 The auxiliary device, which is used for pre-charging a voltage on the gate of the charge transfer device, couples the input signal of each stage to the gate of the charge transfer device; and therefore, increases the boost coupling effect on the charge transfer MOS device, which results in increasing
30 a signal level at the source (output) of the charge transfer device. The auxiliary device, that is used for buffering the drain of the charge transfer device from the P-well and the N-well, couples the drain voltage of the charge transfer device to the P-well and the deep N-well to reduce the body effect and to improve capacitive coupling effect on the drain of charge transfer MOSFET device by reducing the effects of the P-well and Deep N-well parasitic capacitance.

It should be noted that although the present invention has been oriented to a charge pump circuit formed from
40 N-channel MOSFET devices in a P-well within a deep N-well on a P-substrate, a similar charge pump circuit could be formed from P-channel MOSFET devices in an N-well within a deep P-well residing on an N-substrate.

Park '791, col. 5:

Continuing to refer to FIG. 7, an input voltage of a stage is applied to the drain of the charge transfer MOS device Mt within the stage. This same input voltage is coupled to the gate of the charge transfer MOS device Mt by means of an auxiliary MOS device Mg and clock signal P3 in odd
50 numbered stages and clock signal P1 in even number stages. Similarly, a boosted input signal to a stage is coupled to the P-well Dpw and deep N-well Dnw by the auxiliary MOS device Ms, which is gated by the gate signal of the charge transfer MOS device Mt. Clock P2 for odd numbered stages
55 and clock P4 for even number of stages are applied to the gate of the charge transfer MOS device through capacitor Cg.

Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Park '791, col. 7:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

A negative high voltage output charge pump circuit can also be realized using the same triple-well structure of the present invention, except that deep N-well is connected to 50 V_{dnw}, which is a positive voltage and can be either the power supply VDD, or ground. FIG. 12 shows a cross-sectional view of the charge pump circuit of present invention for a negative high voltage output. The charge transfer MOS device M_t and auxiliary MOS device M_s are formed 55 in their own P-well which act as substrate of the MOS devices. The deep N-well can be shared with other pumping stages and connected to ground or power supply VDD. The source S₂ and drain D₂ of the auxiliary MOS M_s are coupled to the P-well and the drain D₁ of the charge transfer 60 MOS device M_t, respectively. The drains D₁ and D₂ and the gates of the charge transfer device M_t and auxiliary device M_s are coupled together and are further connected to the coupling capacitor C_b.

Park '791, cols. 7-8:

FIG. 13 is a circuit diagram of an embodiment of the 65 present invention of a charge pump for generating a negative voltage output. The circuit uses an N-channel MOSFET as

charge transfer device M_t and an auxiliary device M_s. The pumping stages are connected in series from ground to the negative output voltage (-)V_{pp}. Each pumping stage includes one charge transfer MOS device M_t, one auxiliary 5 MOS device M_s and one coupling capacitor C_b. The P-well within each pump stage, Stage (1), Stage (2), Stage (3), Stage (n-1) and Stage (n), resides within a deep N-well and isolates the circuitry of each stage. The deep N-well can be common for each P-well or separate for each P-well. The 10 auxiliary device M_s couples a boosted voltage to the P-well to reduce body effects on the pumped voltage within each stage. The diode D_{pw} represents the parasitic diode junction between the P-well and the deep N-well. A positive voltage V_{dnw}, which can be either VDD or ground, is applied to the deep N-well to insure that the diode D_{pw} remains back 15 biased throughout the negative charge pump operations.

Park '791, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The circuit operation of the negative charge pump is carried out in the same manner as the positive charge pump circuit, except that the input of the charge pump circuit is coupled to the ground, instead of VDD. A two clock scheme using clocks P1 and P3, or P2 and P4, shown in FIG. 8 for the positive charge pump circuit can be used for the negative charge pump circuit. When the charge transfer MOS device Mt in a first pump stage is turned on by a clock signal, a boosted negative charge is created at the output of a first pump stage, which is coupled to the drain nodes of the charge transfer MOS device Mt and auxiliary MOS device Ms. The boosted negative charge is transferred to the input of a second pump stage connected to the output of the first pump stage. The boosted negative charge is coupled to a source of the charge transfer MOS device Mt in the second stage. At the same time, the auxiliary MOS device Ms of the first stage is also turned on so that the boosted negative charge of the output of the first pump stage is coupled to the P-well of the first pump stage. The coupling of the boosted negative charge to the P-well reduces the body effect on the charge transfer MOS device Mt, which results in an increased charge transfer efficiency.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

4[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

4[b] wherein the well bias potential is the lower potential out of the output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and the output potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row.

The Omnibus References disclose and/or render obvious wherein the well bias potential is the lower potential out of the output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and the output potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) of the second boosting cell row.

See, e.g.:

Hung, Fig. 3:

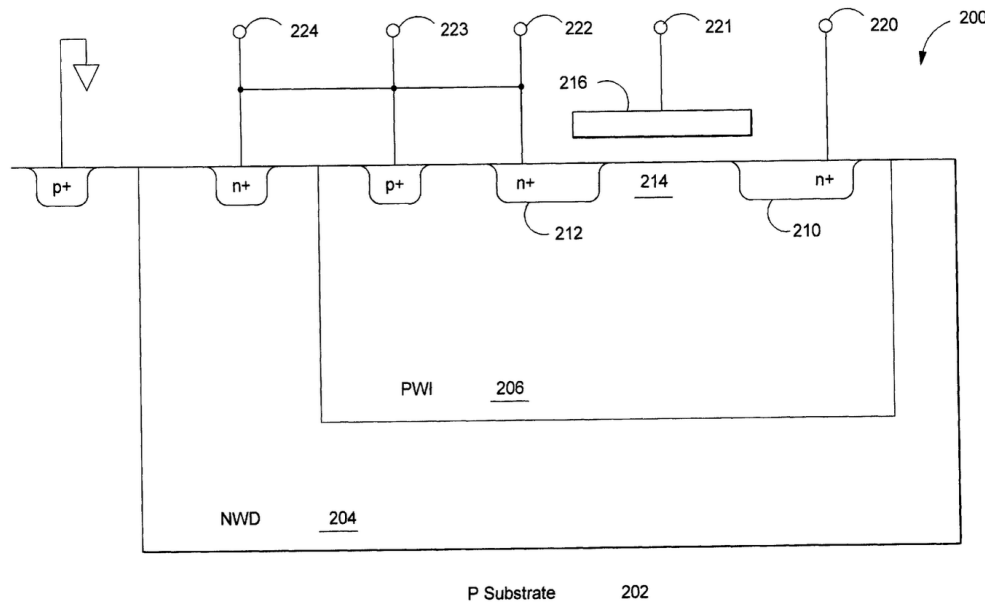


FIG.3

Hung, col. 3:

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor 200 that can be used for transistors 102–110 of FIG. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed in substrate 202, and a P well 206 is formed in N well 204. An N+ type drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220–224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Hung, col. 3:

In one embodiment of the present invention, the potential of source region 212, P well 206 and N well 204 are set to the same value. One way to meet this condition is to electrically connecting terminals 222, 223 and 224. The potential of substrate 202 is normally set to ground. This arrangement creates a PN diode between P well 206 and drain region 210. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an “extra diode.” As explained in more detail below, this extra diode has the following advantageous effects:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Lin '129, Fig. 8:

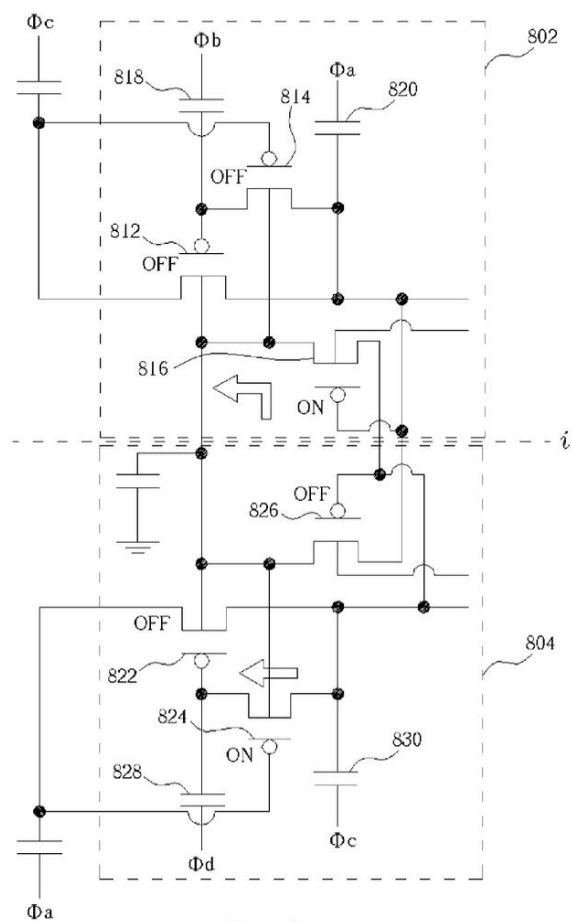


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

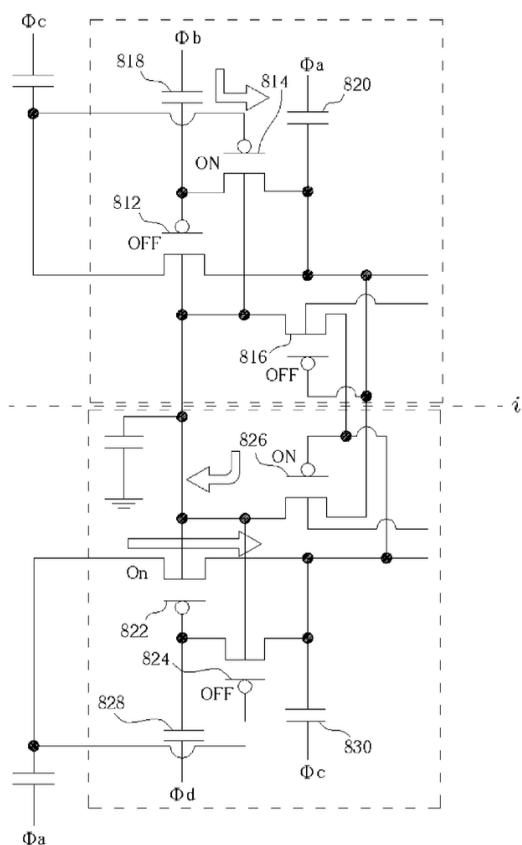


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Please refer to FIG. 14 which shows the HVC used for
35 generating high voltage clock pulses from a low input
voltage. The input voltage V_{in} is inputted to a first inverter
1402 and then to a second inverter 1404 where the voltage
signal is transferred to both a first capacitor 1406 to a third
inverter 1408 that is further electrically coupled to a second
40 capacitor 1416. The first capacitor 1406 is electrically
coupled to the source of the first NMOS transistor 1410 and
the gate of the transistor 1412 and the second capacitor 1416
is electrically coupled to the source of the second NMOS
transistor 1412 and the gate of the first NMOS transistor
45 1410. As a result, the two NMOS transistors 1410 and 1412
are cross-coupled to increase the amplitude of the input
voltage V_{in} . To substantially reduce body effects, the body
of the third PMOS transistor 1414 is electrically coupled to
the drain of a fifth NMOS transistor 1424 whose source is
50 electrically coupled to V_{dd} and gate is controlled by clock
pulse ϕ_e which also at the same time control the third
capacitor 1420 through a inverter 1422. The high voltage
clock pulses ϕ_b and ϕ_d can be achieved by such cross-
coupling scheme to increase the pumping gain at low supply
55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 ("Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.").

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50
a dual pumping circuit that can be implemented in either
positive or negative with provides good pumping perfor-
mance at low supply voltage (1V to 2V) using the popular
triple-well technology. The dual pumping circuit uses four-
phase clocks that has one pair of identical but out of phase 55
clocks. The other two of the clocks may be chosen to be
generated by a high voltage circuit to provide better pump-
ing at low voltage. The positive dual pumping circuit uses
PMOS transistors and the negative pumping circuit uses
NMOS transistors where the transistors have special sub- 60
strate connection to avoid body effect and p-n junction
conduction.

Those skilled in the art will readily observe that numerous
modifications and alterations of the device may be made
while retaining the teachings of the invention. Accordingly, 65
that above disclosure should be construed as limited only by
the metes and bounds of the appended

Park '791, Fig. 7:

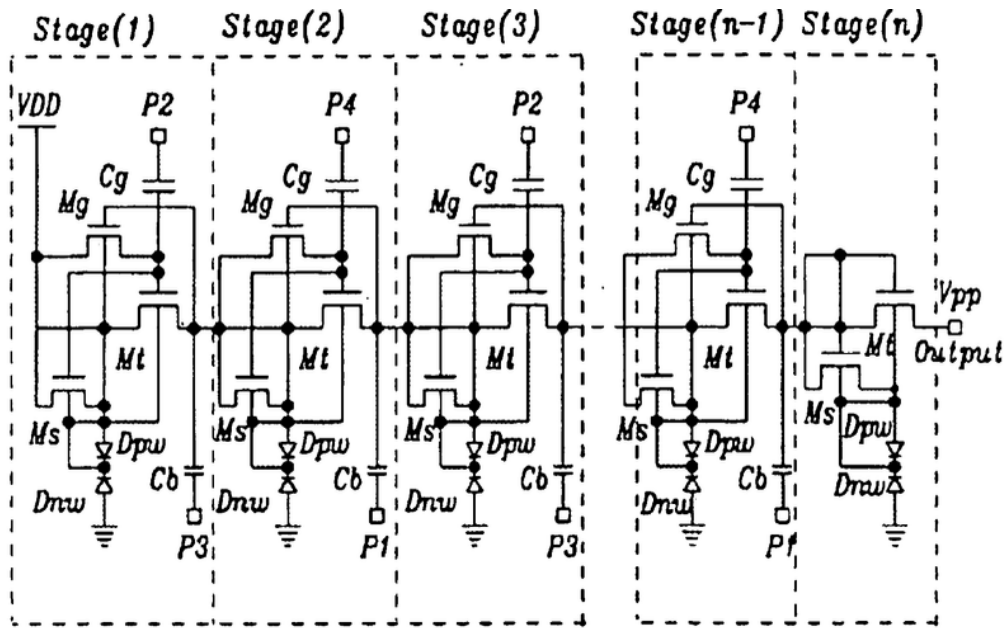


FIG. 7

Park '791, Fig. 13:

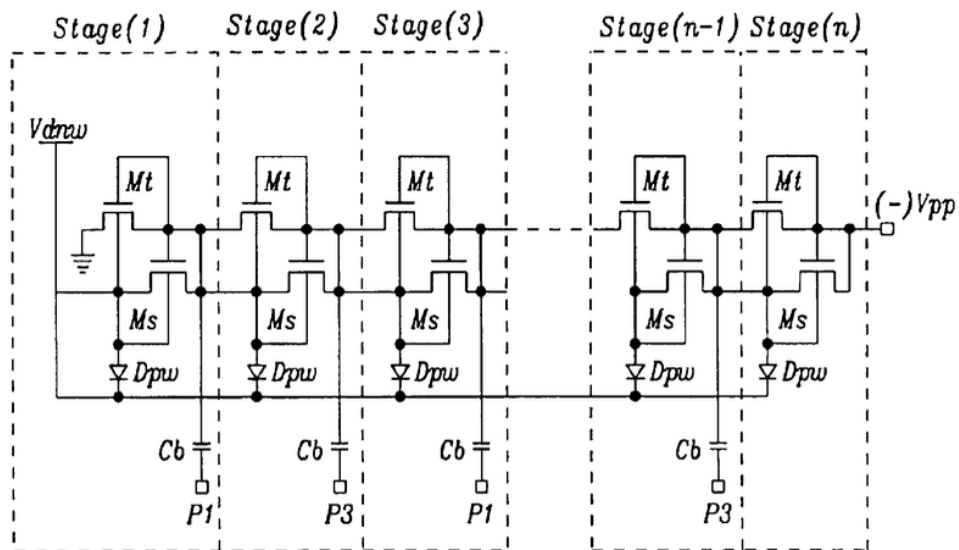


FIG. 13

Park '791, col 4:

25 The auxiliary device, which is used for pre-charging a
voltage on the gate of the charge transfer device, couples the
input signal of each stage to the gate of the charge transfer
device; and therefore, increases the boost coupling effect on
30 the charge transfer MOS device, which results in increasing
a signal level at the source (output) of the charge transfer
device. The auxiliary device, that is used for buffering the
drain of the charge transfer device from the P-well and the
N-well, couples the drain voltage of the charge transfer
35 device to the P-well and the deep N-well to reduce the body
effect and to improve capacitive coupling effect on the drain
of charge transfer MOSFET device by reducing the effects
of the P-well and Deep N-well parasitic capacitance.

It should be noted that although the present invention has
40 been oriented to a charge pump circuit formed from
N-channel MOSFET devices in a P-well within a deep
N-well on a P-substrate, a similar charge pump circuit could
be formed from P-channel MOSFET devices in an N-well
within a deep P-well residing on an N-substrate.

Park '791, col. 5:

Continuing to refer to FIG. 7, an input voltage of a stage
is applied to the drain of the charge transfer MOS device Mt
within the stage. This same input voltage is coupled to the
gate of the charge transfer MOS device Mt by means of an
auxiliary MOS device Mg and clock signal P3 in odd 50
numbered stages and clock signal P1 in even number stages.
Similarly, a boosted input signal to a stage is coupled to the
P-well Dpw and deep N-well Dnw by the auxiliary MOS
device Ms, which is gated by the gate signal of the charge
transfer MOS device Mt. Clock P2 for odd numbered stages 55
and clock P4 for even number of stages are applied to the
gate of the charge transfer MOS device through capacitor
Cg.

Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Park '791, col. 7:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

A negative high voltage output charge pump circuit can also be realized using the same triple-well structure of the present invention, except that deep N-well is connected to 50 V_{dnw} , which is a positive voltage and can be either the power supply VDD, or ground. FIG. 12 shows a cross-sectional view of the charge pump circuit of present invention for a negative high voltage output. The charge transfer MOS device M_t and auxiliary MOS device M_s are formed 55 in their own P-well which act as substrate of the MOS devices. The deep N-well can be shared with other pumping stages and connected to ground or power supply VDD. The source S_2 and drain D_2 of the auxiliary MOS M_s are coupled to the P-well and the drain D_1 of the charge transfer 60 MOS device M_t , respectively. The drains D_1 and D_2 and the gates of the charge transfer device M_t and auxiliary device M_s are coupled together and are further connected to the coupling capacitor C_b .

Park '791, cols. 7-8:

FIG. 13 is a circuit diagram of an embodiment of the 65 present invention of a charge pump for generating a negative voltage output. The circuit uses an N-channel MOSFET as

charge transfer device M_t and an auxiliary device M_s . The pumping stages are connected in series from ground to the negative output voltage $(-V_{pp})$. Each pumping stage includes one charge transfer MOS device M_t , one auxiliary 5 MOS device M_s and one coupling capacitor C_b . The P-well within each pump stage, Stage (1), Stage (2), Stage (3), Stage (n-1) and Stage (n), resides within a deep N-well and isolates the circuitry of each stage. The deep N-well can be common for each P-well or separate for each P-well. The 10 auxiliary device M_s couples a boosted voltage to the P-well to reduce body effects on the pumped voltage within each stage. The diode D_{pw} represents the parasitic diode junction between the P-well and the deep N-well. A positive voltage V_{dnw} , which can be either VDD or ground, is applied to the deep N-well to insure that the diode D_{pw} remains back 15 biased throughout the negative charge pump operations.

Park '791, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The circuit operation of the negative charge pump is carried out in the same manner as the positive charge pump circuit, except that the input of the charge pump circuit is coupled to the ground, instead of VDD. A two clock scheme using clocks P1 and P3, or P2 and P4, shown in FIG. 8 for the positive charge pump circuit can be used for the negative charge pump circuit. When the charge transfer MOS device Mt in a first pump stage is turned on by a clock signal, a boosted negative charge is created at the output of a first pump stage, which is coupled to the drain nodes of the charge transfer MOS device Mt and auxiliary MOS device Ms. The boosted negative charge is transferred to the input of a second pump stage connected to the output of the first pump stage. The boosted negative charge is coupled to a source of the charge transfer MOS device Mt in the second stage. At the same time, the auxiliary MOS device Ms of the first stage is also turned on so that the boosted negative charge of the output of the first pump stage is coupled to the P-well of the first pump stage. The coupling of the boosted negative charge to the P-well reduces the body effect on the charge transfer MOS device Mt, which results in an increased charge transfer efficiency.

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

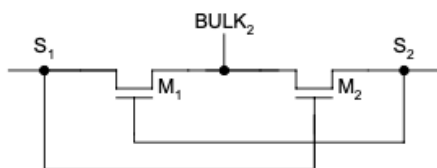


Fig. 15.14. Dynamic biasing of the bulk nodes

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

7[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

7[b] wherein the at least one analog comparison circuit has a first-conductivity type first well region on the substrate,

The Omnibus References disclose and/or render obvious wherein the at least one analog comparison circuit has a first-conductivity type first well region on the substrate.

See, e.g.:

Lin ’129, Fig. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

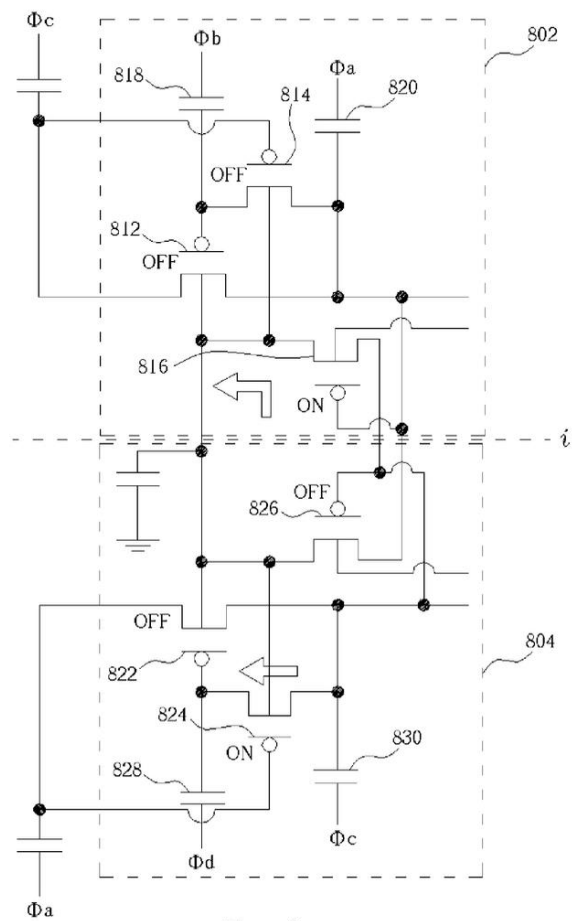


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

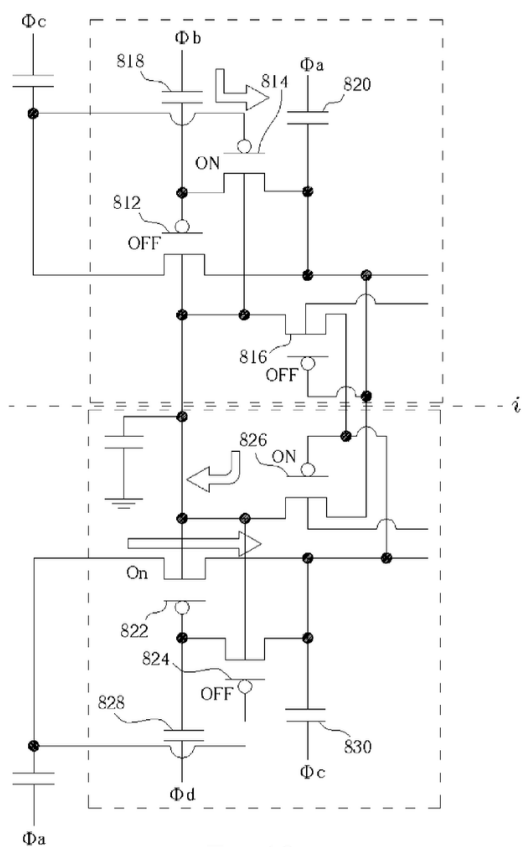


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Please refer to FIG. 14 which shows the HVC used for
 35 generating high voltage clock pulses from a low input
 voltage. The input voltage V_{in} is inputted to a first inverter
 1402 and then to a second inverter 1404 where the voltage
 signal is transferred to both a first capacitor 1406 to a third
 inverter 1408 that is further electrically coupled to a second
 40 capacitor 1416. The first capacitor 1406 is electrically
 coupled to the source of the first NMOS transistor 1410 and
 the gate of the transistor 1412 and the second capacitor 1416
 is electrically coupled to the source of the second NMOS
 transistor 1412 and the gate of the first NMOS transistor
 45 1410. As a result, the two NMOS transistors 1410 and 1412
 are cross-coupled to increase the amplitude of the input
 voltage V_{in} . To substantially reduce body effects, the body
 of the third PMOS transistor 1414 is electrically coupled to
 the drain of a fifth NMOS transistor 1424 whose source is
 50 electrically coupled to V_{dd} and gate is controlled by clock
 pulse ϕ_e which also at the same time control the third
 capacitor 1420 through a inverter 1422. The high voltage
 clock pulses ϕ_b and ϕ_d can be achieved by such cross-
 coupling scheme to increase the pumping gain at low supply
 55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 (“Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.”).

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50 a dual pumping circuit that can be implemented in either positive or negative with provides good pumping performance at low supply voltage (1V to 2V) using the popular triple-well technology. The dual pumping circuit uses four-phase clocks that has one pair of identical but out of phase 55 clocks. The other two of the clocks may be chosen to be generated by a high voltage circuit to provide better pumping at low voltage. The positive dual pumping circuit uses PMOS transistors and the negative pumping circuit uses NMOS transistors where the transistors have special sub- 60 strate connection to avoid body effect and p-n junction conduction.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, 65 that above disclosure should be construed as limited only by the metes and bounds of the appended

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

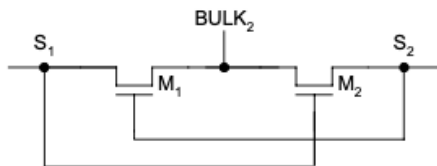


Fig. 15.14. Dynamic biasing of the bulk nodes

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

7[c] a second-conductivity type second well region in the first well region, and

The Omnibus References disclose and/or render obvious a second-conductivity type second well region in the first well region.

See, e.g.:

Claim limitation 1[c], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

7[d] at least one switching element in the first well region or the second well region, and

The Omnibus References disclose and/or render obvious at least one switching element in the first well region or the second well region.

See, e.g.:

Claim limitation 1[d], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading.

7[e] the at least one analog comparison circuit is provided one for each boosting cell stage.

The Omnibus References disclose and/or render obvious the at least one analog comparison circuit is provided one for each boosting cell stage.

See, e.g.:

Lin ’129, Fig. 5:

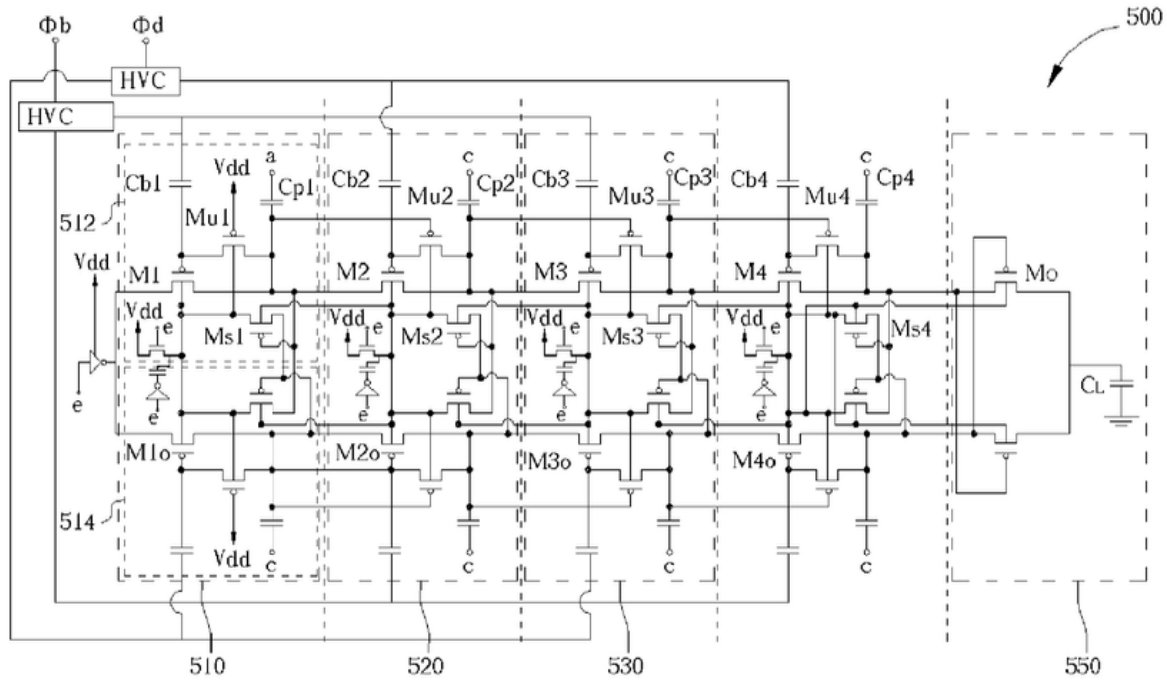


Fig. 5

Lin '129, Fig. 15:

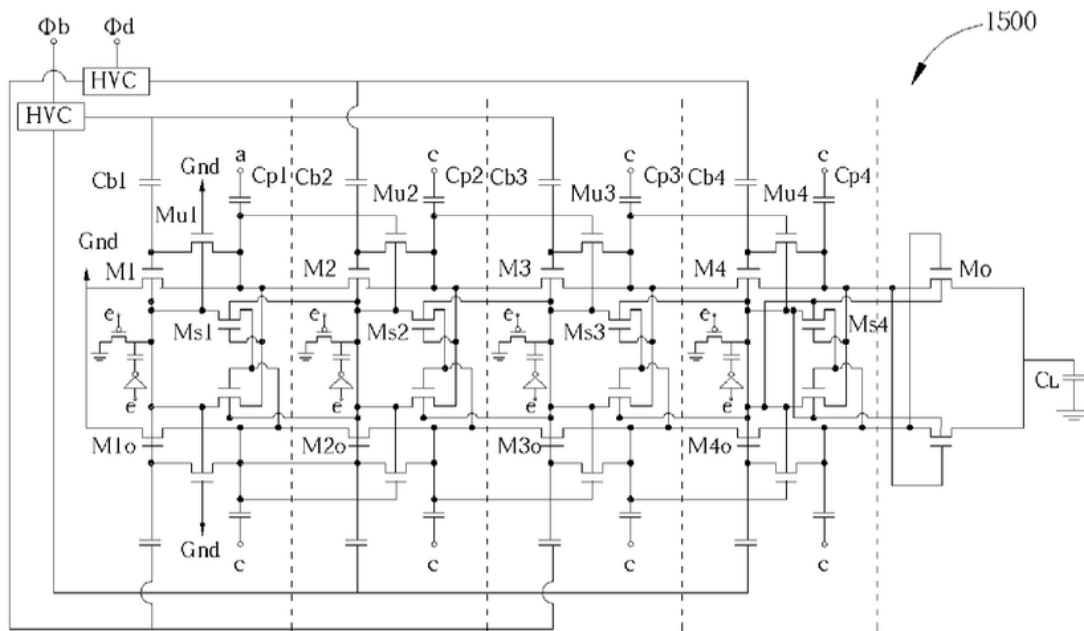


Fig. 15

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

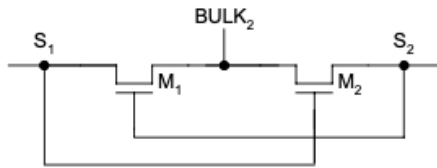


Fig. 15.14. Dynamic biasing of the bulk nodes

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

9[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

9[b] wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

The Omnibus References disclose and/or render obvious wherein a diode element is provided between the first terminal and the first well region of the boosting cell.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

See, e.g.:

Hung, col. 3:

In one embodiment of the present invention, the potential of source region **212**, P well **206** and N well **204** are set to the same value. One way to meet this condition is to electrically connecting terminals **222**, **223** and **224**. The potential of substrate **202** is normally set to ground. This arrangement creates a PN diode between P well **206** and drain region **210**. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an “extra diode.” As explained in more detail below, this extra diode has the following advantageous effects:

Park '791, cols. 2-3:

A prior art charge pump circuit using a floating well is described in U.S. Pat. No. 5,986,947 (Choi et al.). The charge pump circuits using a triple well P-N junction and MOS diodes are disclosed in “A 3.3V only 16 Mb DINOR flash memory”, IEEE International Solid State Circuits Conference, Digest of Technical Papers, 1995, pp 122–123, and in U.S. Pat. No. 6,100,557 (Hung et al.), respectively. The triple well charge pump provides greater efficiency with

increased suppression of the body effect over other prior art. This improvement is due to the extra diode inherently formed between the well and the source of the charge transfer MOS device that can help increase the forward conduction current.

Jinbo, Fig. 7:

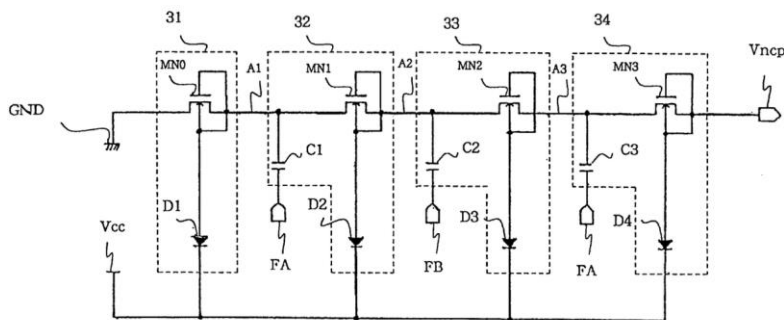


Fig. 7

Jinbo, Fig. 8:

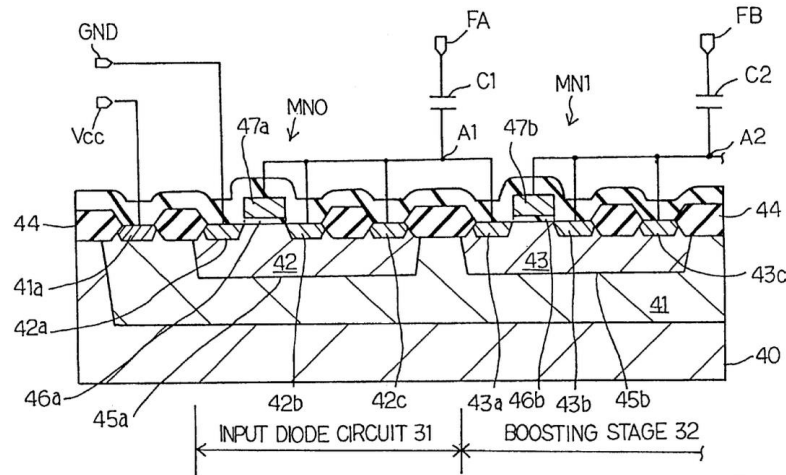


Fig. 8

Jinbo, col. 6:

A p-n junction 45a between the n-type well 41 and the p-type well 42 serves as the diode D1, and the p-type well 42 per se serves as the back gate of the n-channel enhancement type field effect transistor MN0. N-type impurity regions 42a/42b are formed in the p-type well 42, and are spaced from each other. A thin gate insulating layer 46a is grown on the p-type well 42 between the n-type impurity regions 42a/42b, and a conductive line 47a extends over the thin gate insulating layer 46a. The n-type impurity regions 42a/42b and a part of the conductive line 47a serve as the source/drain nodes and the gate electrode of the n-channel enhancement type field effect transistor MN0. The ground line GND is connected to the n-type impurity region 42a.

Jinbo, cols. 6-7:

The p-type well 43 forms another p-n junction 45b together with the n-type well 41, and the p-n junction 45b serves as the diode D2. The p-type well 43 per se serves as the back gate of the n-channel enhancement type field effect transistor MN1. N-type impurity regions 43a/43b are

formed in the p-type well 43, and are spaced from each other. A thin gate insulating layer 46b is grown on the p-type well 43 between the n-type impurity regions 43a/43b, and a conductive line 47b extends over the thin gate insulating layer 46b. The n-type impurity regions 43a/43b and a part of the conductive line 47b serve as the source/drain nodes and the gate electrode of the n-channel enhancement type field effect transistor MN1. The n-type impurity region 42b is further connected to the n-type impurity region 43a.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

10[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

See, e.g., claim limitation 1[a], *supra*.

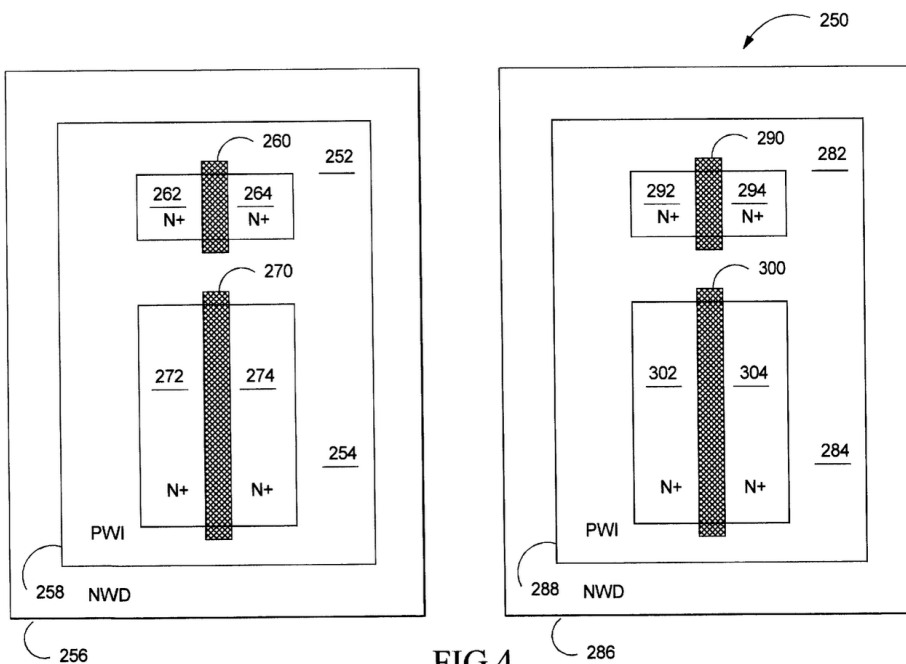
To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

10[b] wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region.

The Omnibus References disclose and/or render obvious wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows share a common first well region.

See, e.g.:

Hung, Fig. 4:



Hung, col. 4:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Referring to both FIGS. 1 and 4, the source terminal 141 of transistor 102 and source terminal 142 of transistor 106 are connected to V_{DD} . Thus, source regions 262 and 272 of transistors 252 and 254, respectively, have the same potential (i.e., V_{DD}). As explained above, P well 258 and N well 256 should have the same potential as source regions 262 and 272. Thus these two wells also have the same potential (V_{DD}).

FIG. 1 shows that the gate terminal 144 of transistor 102 is connected to the drain terminal 145 of transistor 106, the source terminal 146 of transistor 103 and the source terminal 147 of transistor 107. As explained above, P well 288 and N well 286 should have the same potential as source regions 292 and 302 (which are coupled to source terminals 146 and 147). Thus in FIG. 4, gate 260, drain region 274, source regions 292 and 302, N well 286 and P well 288 all have the same potential.

FIG. 1 shows that the drain terminal 150 of transistor 102 is connected to the gate 151 of transistor 106. Thus, in FIG. 4, drain region 264 has the same potential as gate 270.

Hung, col. 5:

FIG. 1 shows that the gate terminal 153 of transistor 103 is connected to the drain terminal 154 of transistor 107 (in addition to the source terminals 155 and 156 of transistors 104 and 108). Thus in FIG. 4, gate 290 has the same potential as drain region 304. FIG. 1 also shows that the drain terminal 158 of transistor 103 is connected to the gate 159 of transistor 107. Thus, in FIG. 4, drain region 294 has the same potential as gate 300.

Park '791, col. 4:

In the present invention a charge pump circuit is disclosed that has multiple stages connected in series. In each stage there are three MOSFET devices residing in a P-well within a deep N-well unique to each stage and on a P-substrate. The three MOSFET devices of each stage comprise one charge transfer device, one auxiliary MOSFET device for pre-charging a voltage on the gate of the charge transfer device and one auxiliary MOSFET device for buffering the drain of the charge transfer device from the P-well and the deep N-well. Each stage also contains two boost capacitors needed to store charge as it is developed. Each stage is clocked by two clock signals that are out of phase with each other. The serial connected stages are clocked such that the corresponding clocks signals for adjacent stages are out of phase with each other. Thus, a four clock system is used; however, with the proper arrangement of two clock signals, a two clock system can also be used. When charge is being clocked into a first stage, pumped charge is being clocked into a third stage from the second stage.

Jinbo, Fig. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

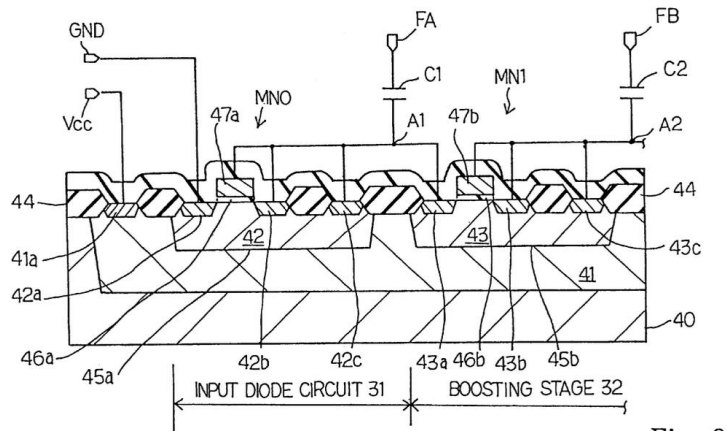


Fig. 8

Jinbo, Fig. 13:

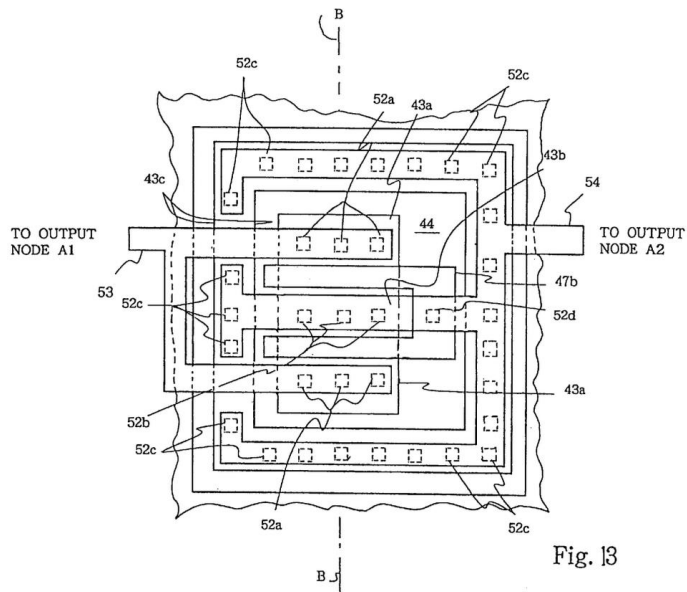


Fig. 13

Jinbo, Fig. 14:

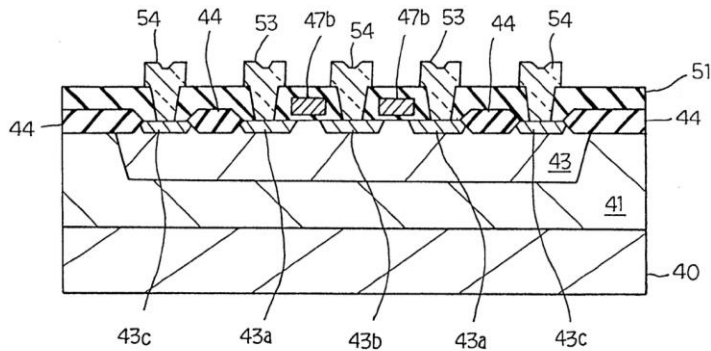


Fig. 14

Jinbo, Fig. 15:

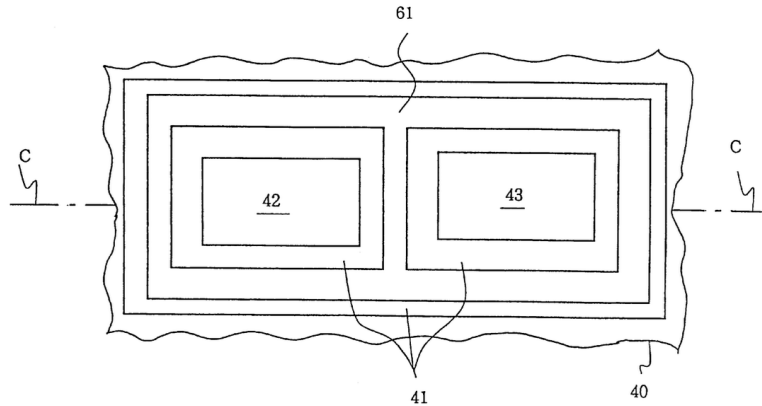


Fig. 15

Jinbo, col. 6:

The p-type wells 42/43 are assigned to the input diode circuit 31 and the boosting stage 32, respectively. Although
 35 other p-type wells are further formed in the n-type well 41 for the other boosting stages 33/34, they are not shown in FIG. 8 for the sake of simplicity. A heavily-doped n-type impurity region 41a is formed in another surface portion of the n-type well 41, and the positive power voltage Vcc is held in contact with the heavily-doped n-type impurity region 41a. The positive power supply voltage Vcc is
 40 supplied through the heavily-doped n-type impurity region 41a to the n-type well 41.

Jinbo, col. 10:

Another alternative layout is shown in FIGS. 13 and 14. The boosting stage 32 shown in FIG. 13 is different from that shown in FIG. 11 in the layout of the n-channel enhancement type field effect transistor MN1. The n-channel enhancement
 10 type field effect transistor MN1 has two n-type impurity regions 43a spaced from the n-type impurity region 43b, and, accordingly, the gate electrode 47b is bifurcated so as to extend over two channel regions between the n-type impurity regions 43a and the n-type impurity region 43b.
 15 Impurity regions, conductive layers and contact holes shown in FIGS. 13 and 14 are labeled with the same references designating corresponding components of the boosting stage 32 shown in FIG. 11 and 12 without detailed description. The two n-type impurity regions 43a widen the current path
 20 from the heavily-doped p-type impurity region 43c, and the resistance is further decreased. As a result, the potential level VA2 is decayed much faster than the potential level VA2 of the charge pump circuit shown in FIG. 8.

Jinbo, col. 10:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

As described hereinbefore, the p-type wells 42/43 are
25 formed in the n-type well 41 at intervals. An n-type channel
stopper 61 may be formed between the p-type wells 42/43a
and the periphery of the n-type well 41. The n-channel
enhancement type field effect transistor MN0/MN1 and the
heavily-doped p-type impurity regions 42c/43c are arranged
30 in the p-type well 42/43 as shown in FIG. 8, 11/12 or 14. The
n-type channel stopper 61 is biased at the same voltage as
the n-type well 41. In this instance, the bias voltage is equal
to the positive power voltage Vcc. The n-type channel
stopper 61 is effective against surface leakage current
35 between the p-type wells 42/43 and the p-type semiconduc-
tor substrate 40.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

11[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

11[b] wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region.

The Omnibus References disclose and/or render obvious wherein the at least one switching elements having the same potential of the first well region of the first and second boosting cell rows and the at least one analog comparison circuit share a common first well region.

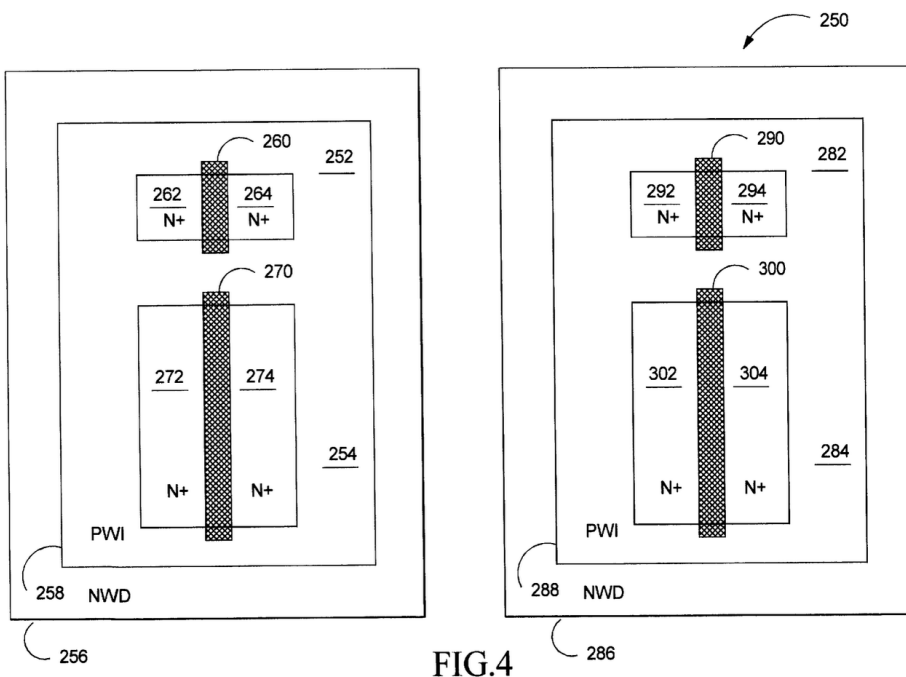
See, e.g.:

Park '791, col. 4:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

In the present invention a charge pump circuit is disclosed that has multiple stages connected in series. In each stage there are three MOSFET devices residing in a P-well within a deep N-well unique to each stage and on a P-substrate. The three MOSFET devices of each stage comprise one charge transfer device, one auxiliary MOSFET device for pre-charging a voltage on the gate of the charge transfer device and one auxiliary MOSFET device for buffering the drain of the charge transfer device from the P-well and the deep N-well. Each stage also contains two boost capacitors needed to store charge as it is developed. Each stage is clocked by two clock signals that are out of phase with each other. The serial connected stages are clocked such that the corresponding clocks signals for adjacent stages are out of phase with each other. Thus, a four clock system is used; however, with the proper arrangement of two clock signals, a two clock system can also be used. When charge is being clocked into a first stage, pumped charge is being clocked into a third stage from the second stage.

Hung, Fig. 4:



Hung, col. 4:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

Referring to both FIGS. 1 and 4, the source terminal 141 of transistor 102 and source terminal 142 of transistor 106 are connected to V_{DD} . Thus, source regions 262 and 272 of transistors 252 and 254, respectively, have the same potential (i.e., V_{DD}). As explained above, P well 258 and N well 256 should have the same potential as source regions 262 and 272. Thus these two wells also have the same potential (V_{DD}).

FIG. 1 shows that the gate terminal 144 of transistor 102 is connected to the drain terminal 145 of transistor 106, the source terminal 146 of transistor 103 and the source terminal 147 of transistor 107. As explained above, P well 288 and N well 286 should have the same potential as source regions 292 and 302 (which are coupled to source terminals 146 and 147). Thus in FIG. 4, gate 260, drain region 274, source regions 292 and 302, N well 286 and P well 288 all have the same potential.

FIG. 1 shows that the drain terminal 150 of transistor 102 is connected to the gate 151 of transistor 106. Thus, in FIG. 4, drain region 264 has the same potential as gate 270.

Hung, col. 5:

FIG. 1 shows that the gate terminal 153 of transistor 103 is connected to the drain terminal 154 of transistor 107 (in addition to the source terminals 155 and 156 of transistors 104 and 108). Thus in FIG. 4, gate 290 has the same potential as drain region 304. FIG. 1 also shows that the drain terminal 158 of transistor 103 is connected to the gate 159 of transistor 107. Thus, in FIG. 4, drain region 294 has the same potential as gate 300.

Park '791, col. 4:

In the present invention a charge pump circuit is disclosed that has multiple stages connected in series. In each stage there are three MOSFET devices residing in a P-well within a deep N-well unique to each stage and on a P-substrate. The three MOSFET devices of each stage comprise one charge transfer device, one auxiliary MOSFET device for pre-charging a voltage on the gate of the charge transfer device and one auxiliary MOSFET device for buffering the drain of the charge transfer device from the P-well and the deep N-well. Each stage also contains two boost capacitors needed to store charge as it is developed. Each stage is clocked by two clock signals that are out of phase with each other. The serial connected stages are clocked such that the corresponding clocks signals for adjacent stages are out of phase with each other. Thus, a four clock system is used; however, with the proper arrangement of two clock signals, a two clock system can also be used. When charge is being clocked into a first stage, pumped charge is being clocked into a third stage from the second stage.

Jinbo, Fig. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

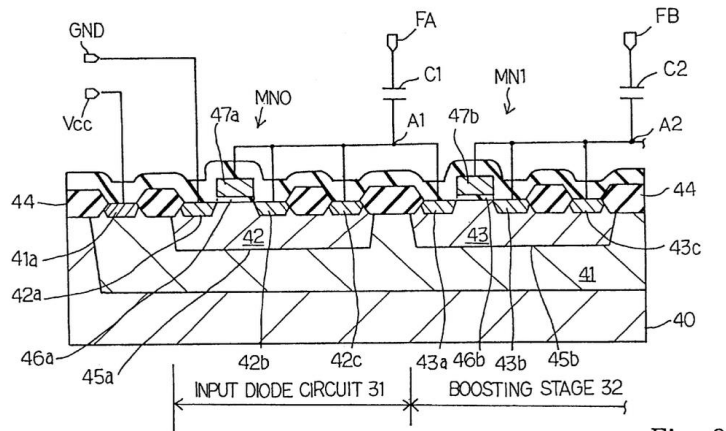


Fig. 8

Jinbo, Fig. 13:

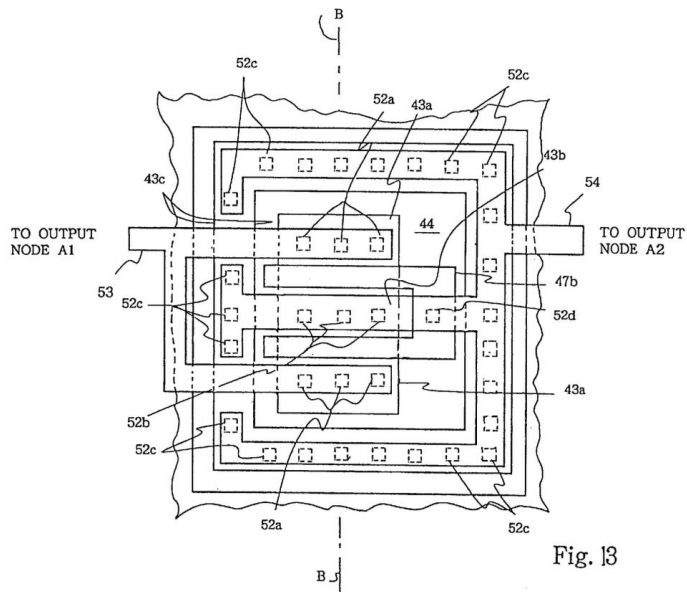


Fig. 13

Jinbo, Fig. 14:

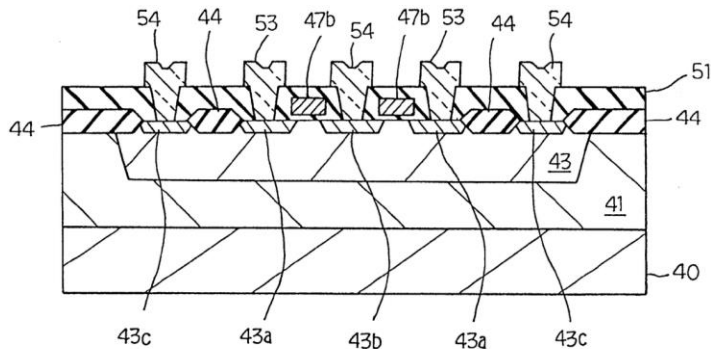


Fig. 14

Jinbo, Fig. 15:

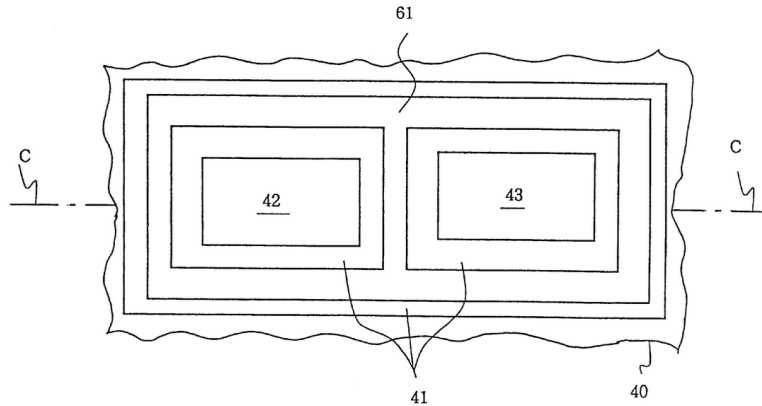


Fig. 15

Jinbo, col. 6:

The p-type wells 42/43 are assigned to the input diode circuit 31 and the boosting stage 32, respectively. Although
 35 other p-type wells are further formed in the n-type well 41 for the other boosting stages 33/34, they are not shown in FIG. 8 for the sake of simplicity. A heavily-doped n-type impurity region 41a is formed in another surface portion of the n-type well 41, and the positive power voltage Vcc is
 40 held in contact with the heavily-doped n-type impurity region 41a. The positive power supply voltage Vcc is supplied through the heavily-doped n-type impurity region 41a to the n-type well 41.

Jinbo, col. 10:

Another alternative layout is shown in FIGS. 13 and 14. The boosting stage 32 shown in FIG. 13 is different from that shown in FIG. 11 in the layout of the n-channel enhancement type field effect transistor MN1. The n-channel enhancement
 10 type field effect transistor MN1 has two n-type impurity regions 43a spaced from the n-type impurity region 43b, and, accordingly, the gate electrode 47b is bifurcated so as to extend over two channel regions between the n-type impurity regions 43a and the n-type impurity region 43b.
 15 Impurity regions, conductive layers and contact holes shown in FIGS. 13 and 14 are labeled with the same references designating corresponding components of the boosting stage 32 shown in FIG. 11 and 12 without detailed description. The two n-type impurity regions 43a widen the current path
 20 from the heavily-doped p-type impurity region 43c, and the resistance is further decreased. As a result, the potential level VA2 is decayed much faster than the potential level VA2 of the charge pump circuit shown in FIG. 8.

Jinbo, col. 10:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

As described hereinbefore, the p-type wells 42/43 are formed in the n-type well 41 at intervals. An n-type channel stopper 61 may be formed between the p-type wells 42/43a and the periphery of the n-type well 41. The n-channel enhancement type field effect transistor MN0/MN1 and the heavily-doped p-type impurity regions 42c/43c are arranged in the p-type well 42/43 as shown in FIG. 8, 11/12 or 14. The n-type channel stopper 61 is biased at the same voltage as the n-type well 41. In this instance, the bias voltage is equal to the positive power voltage Vcc. The n-type channel stopper 61 is effective against surface leakage current between the p-type wells 42/43 and the p-type semiconductor substrate 40.

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

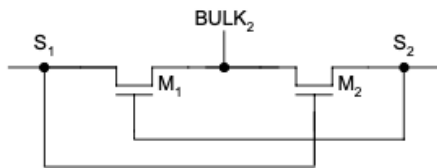


Fig. 15.14. Dynamic biasing of the bulk nodes

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

12[a] The booster circuit of claim 1,

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious the booster circuit of claim 1.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

12[b] wherein the at least one switching circuit of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region, and

The Omnibus References disclose and/or render obvious wherein the at least one switching circuit of the boosting cell on the i-th stage of the first boosting cell row and a first element of the at least one analog comparison circuit share a common first well region.

See, e.g.:

Park '791, col. 4:

10 In the present invention a charge pump circuit is disclosed that has multiple stages connected in series. In each stage there are three MOSFET devices residing in a P-well within a deep N-well unique to each stage and on a P-substrate. The three MOSFET devices of each stage comprise one charge transfer device, one auxiliary MOSFET device for pre-charging a voltage on the gate of the charge transfer device and one auxiliary MOSFET device for buffering the drain of the charge transfer device from the P-well and the deep
15 N-well. Each stage also contains two boost capacitors needed to store charge as it is developed. Each stage is clocked by two clock signals that are out of phase with each other. The serial connected stages are clocked such that the corresponding clocks signals for adjacent stages are out of
20 phase with each other. Thus, a four clock system is used; however, with the proper arrangement of two clock signals, a two clock system can also be used. When charge is being clocked into a first stage, pumped charge is being clocked into a third stage from the second stage.

Hung, Fig. 4:

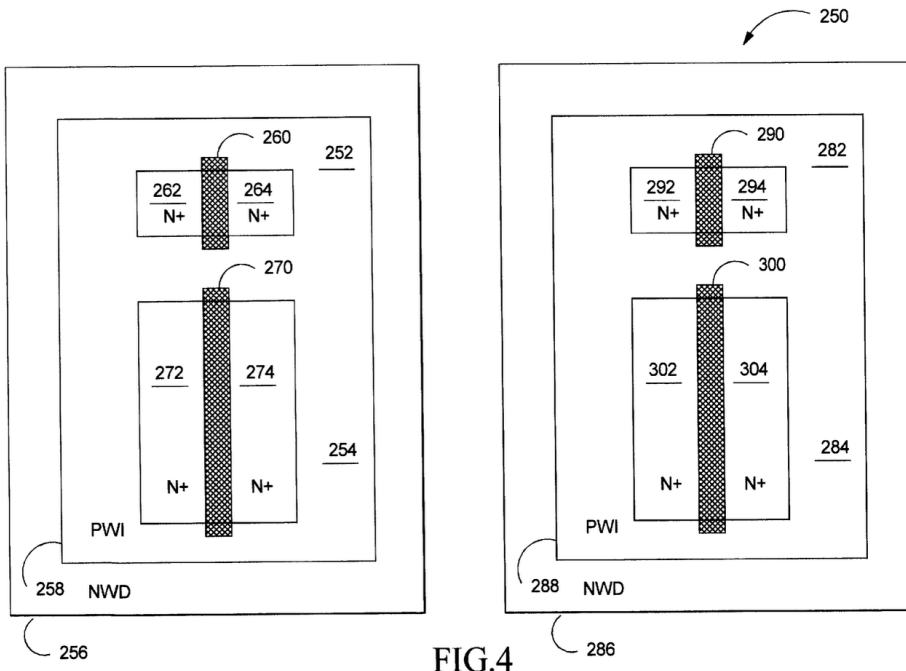


FIG.4

Hung, col. 4:

Referring to both FIGS. 1 and 4, the source terminal 141 of transistor 102 and source terminal 142 of transistor 106 are connected to V_{DD} . Thus, source regions 262 and 272 of transistors 252 and 254, respectively, have the same potential (i.e., V_{DD}). As explained above, P well 258 and N well 256 should have the same potential as source regions 262 and 272. Thus these two wells also have the same potential (V_{DD}).

FIG. 1 shows that the gate terminal 144 of transistor 102 is connected to the drain terminal 145 of transistor 106, the source terminal 146 of transistor 103 and the source terminal 147 of transistor 107. As explained above, P well 288 and N well 286 should have the same potential as source regions 292 and 302 (which are coupled to source terminals 146 and 147). Thus in FIG. 4, gate 260, drain region 274, source regions 292 and 302, N well 286 and P well 288 all have the same potential.

FIG. 1 shows that the drain terminal 150 of transistor 102 is connected to the gate 151 of transistor 106. Thus, in FIG. 4, drain region 264 has the same potential as gate 270.

Hung, col. 5:

FIG. 1 shows that the gate terminal 153 of transistor 103 is connected to the drain terminal 154 of transistor 107 (in addition to the source terminals 155 and 156 of transistors 104 and 108). Thus in FIG. 4, gate 290 has the same potential as drain region 304. FIG. 1 also shows that the drain terminal 158 of transistor 103 is connected to the gate 159 of transistor 107. Thus, in FIG. 4, drain region 294 has the same potential as gate 300.

Park '791, col. 4:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

In the present invention a charge pump circuit is disclosed that has multiple stages connected in series. In each stage there are three MOSFET devices residing in a P-well within a deep N-well unique to each stage and on a P-substrate. The three MOSFET devices of each stage comprise one charge transfer device, one auxiliary MOSFET device for pre-charging a voltage on the gate of the charge transfer device and one auxiliary MOSFET device for buffering the drain of the charge transfer device from the P-well and the deep N-well. Each stage also contains two boost capacitors needed to store charge as it is developed. Each stage is clocked by two clock signals that are out of phase with each other. The serial connected stages are clocked such that the corresponding clocks signals for adjacent stages are out of phase with each other. Thus, a four clock system is used; however, with the proper arrangement of two clock signals, a two clock system can also be used. When charge is being clocked into a first stage, pumped charge is being clocked into a third stage from the second stage.

Jinbo, Fig. 8:

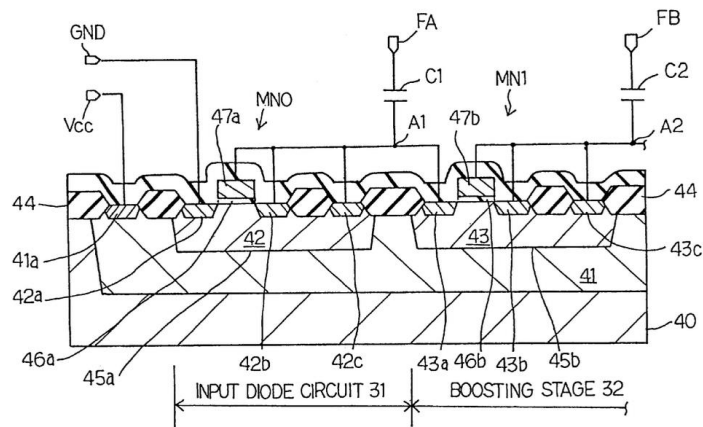
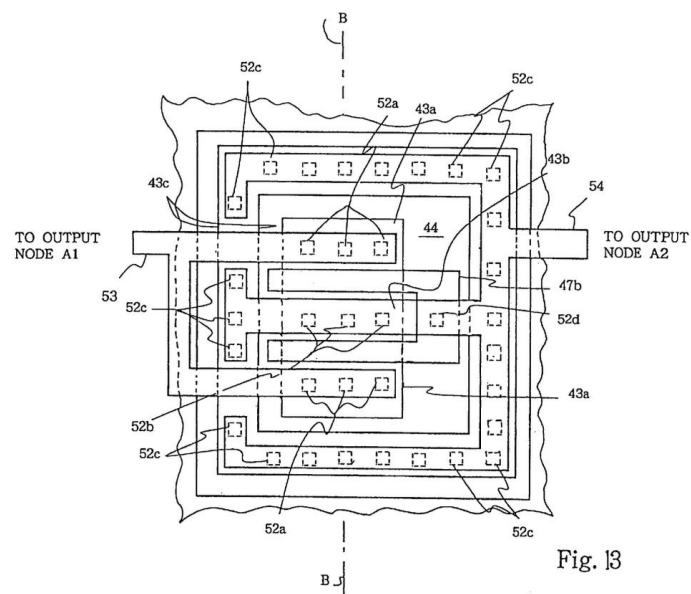


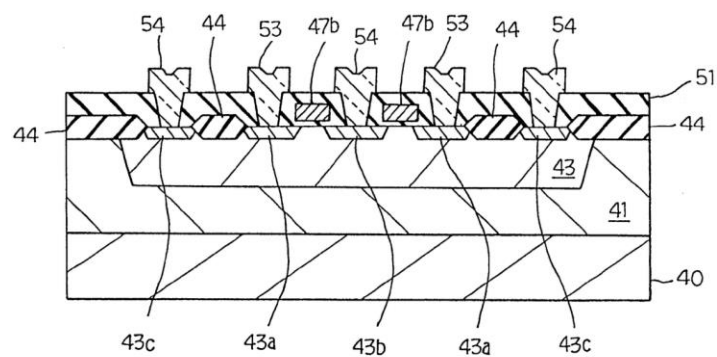
Fig. 8

Jinbo, Fig. 13:

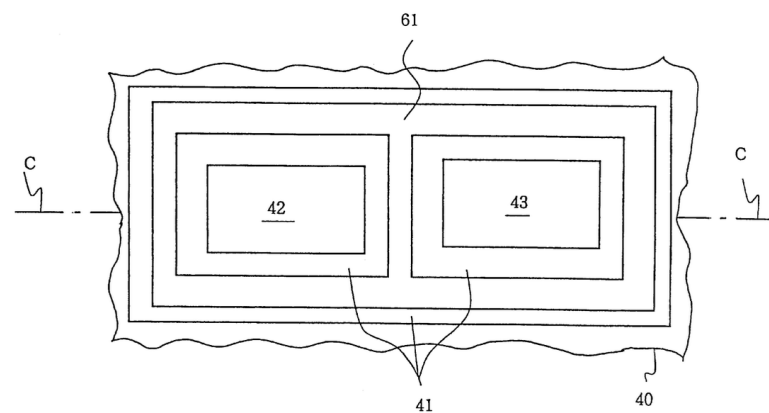
Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart



Jinbo, Fig. 14:



Jinbo, Fig. 15:



Jinbo, col. 6:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The p-type wells 42/43 are assigned to the input diode circuit 31 and the boosting stage 32, respectively. Although other p-type wells are further formed in the n-type well 41 for the other boosting stages 33/34, they are not shown in FIG. 8 for the sake of simplicity. A heavily-doped n-type impurity region 41a is formed in another surface portion of the n-type well 41, and the positive power voltage Vcc is held in contact with the heavily-doped n-type impurity region 41a. The positive power supply voltage Vcc is supplied through the heavily-doped n-type impurity region 41a to the n-type well 41.

Jinbo, col. 10:

Another alternative layout is shown in FIGS. 13 and 14. The boosting stage 32 shown in FIG. 13 is different from that shown in FIG. 11 in the layout of the n-channel enhancement type field effect transistor MN1. The n-channel enhancement type field effect transistor MN1 has two n-type impurity regions 43a spaced from the n-type impurity region 43b, and, accordingly, the gate electrode 47b is bifurcated so as to extend over two channel regions between the n-type impurity regions 43a and the n-type impurity region 43b. Impurity regions, conductive layers and contact holes shown in FIGS. 13 and 14 are labeled with the same references designating corresponding components of the boosting stage 32 shown in FIG. 11 and 12 without detailed description. The two n-type impurity regions 43a widen the current path from the heavily-doped p-type impurity region 43c, and the resistance is further decreased. As a result, the potential level VA2 is decayed much faster than the potential level VA2 of the charge pump circuit shown in FIG. 8.

Jinbo, col. 10:

As described hereinbefore, the p-type wells 42/43 are formed in the n-type well 41 at intervals. An n-type channel stopper 61 may be formed between the p-type wells 42/43a and the periphery of the n-type well 41. The n-channel enhancement type field effect transistor MN0/MN1 and the heavily-doped p-type impurity regions 42c/43c are arranged in the p-type well 42/43 as shown in FIG. 8, 11/12 or 14. The n-type channel stopper 61 is biased at the same voltage as the n-type well 41. In this instance, the bias voltage is equal to the positive power voltage Vcc. The n-type channel stopper 61 is effective against surface leakage current between the p-type wells 42/43 and the p-type semiconductor substrate 40.

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

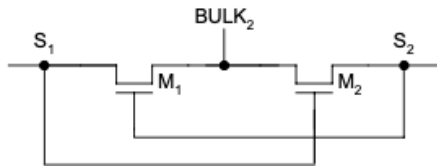


Fig. 15.14. Dynamic biasing of the bulk nodes

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

12[c] the at least one switching circuit of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

The Omnibus References disclose and/or render obvious the at least one switching circuit of the boosting cell on the i-th stage of the second boosting cell row and a second element of the at least one analog comparison circuit share a common first well region.

See, e.g.:

Claim limitation 12[b], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

14[a] A booster circuit comprising:

To the extent the preamble is limiting, the Omnibus References disclose and/or render obvious a booster circuit.

See, e.g., claim limitation 1[a], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[b] boosting cells each having a first-conductivity type first well region on a substrate,

The Omnibus References disclose and/or render obvious boosting cells each having a first-conductivity type first well region on a substrate.

See, e.g.:

Claim limitation 1[b], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[c] a second-conductivity type second well region in the first well region, and

The Omnibus References disclose and/or render obvious a second-conductivity type second well region in the first well region.

See, e.g.:

Claim limitation 1[c], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[d] at least one switching element in either or both of the first well region and the second well region,

The Omnibus References disclose and/or render obvious at least one switching element in either or both of the first well region and the second well region.

See, e.g.:

Claim limitation 1[d], *supra*.

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[e] wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;

The Omnibus References disclose and/or render obvious wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal.

See, e.g.:

Claim limitation 1[e], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[f] a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and

The Omnibus References disclose and/or render obvious a first boosting cell row including N stages ($N \geq 1$) of the boosting cells.

See, e.g.:

Claim limitation 1[f], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[g] a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;

The Omnibus References disclose and/or render obvious a second boosting cell row including M stages ($M \geq 1$) of the boosting cells.

See, e.g.:

Claim limitation 1[g], *supra*.

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant's other invalidity charts and Section II.B.3.a of its cover pleading.

14[h] wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.

The Omnibus References disclose and/or render obvious wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.

See, e.g.:

Hung, Fig. 3:

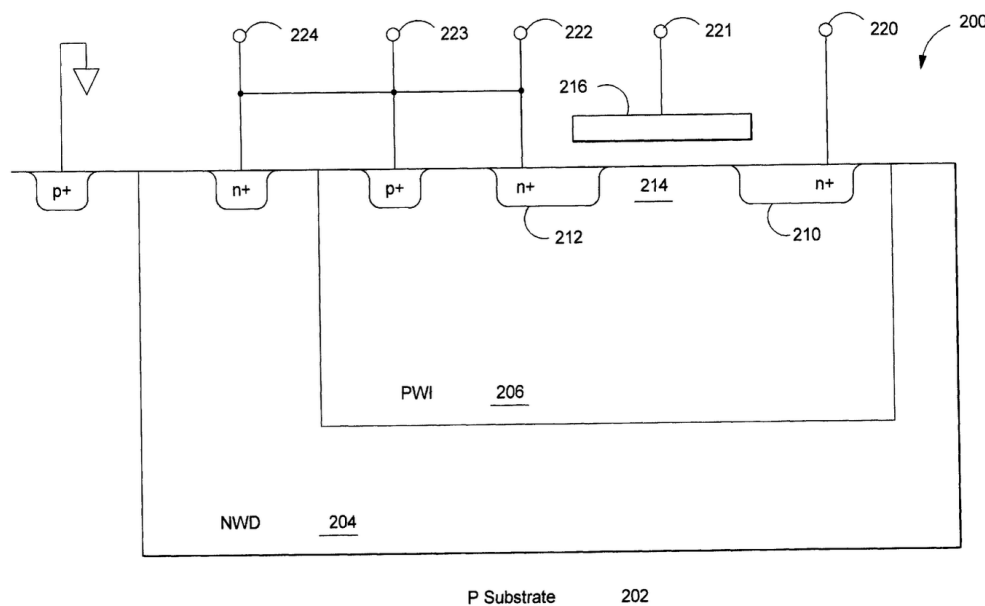


FIG.3

Hung, col. 3:

FIG. 3 shows, schematically, a cross sectional view of a triple well NMOS transistor 200 that can be used for transistors 102–110 of FIG. 1. Transistor 200 is fabricated on a p-type substrate 202. An N well 204 is formed in substrate 202, and a P well 206 is formed in N well 204. An N+ type drain region 210 is formed in P well 206, as is an N+ source region 212. A channel region 214 is defined between source and drain regions in P well 206. A polysilicon gate 216 is positioned above channel region 214. A thin gate oxide is deposited between gate 216 and channel region 214. Drain region 210, gate 216, source region 212, P well 206, and N well 204 are coupled to individual terminals 220–224, respectively. Thus, triple well transistor 200 can be considered a five-terminal device. In one embodiment of the present invention, the N+ source and N+ drain are interchangeable when the charge pump is activated because either terminal may have higher potential than the other.

Hung, col. 3:

In one embodiment of the present invention, the potential of source region 212, P well 206 and N well 204 are set to the same value. One way to meet this condition is to electrically connecting terminals 222, 223 and 224. The potential of substrate 202 is normally set to ground. This arrangement creates a PN diode between P well 206 and drain region 210. The diode is inherent in this triple well construction, and does not occupy any extra silicon area. This diode is able to conduct significant amount of current after it is turned on, and thus adds an extra low resistance path to the NMOS transistor. In this application, this diode is called an "extra diode." As explained in more detail below, this extra diode has the following advantageous effects:

Lin '129, Fig. 8:

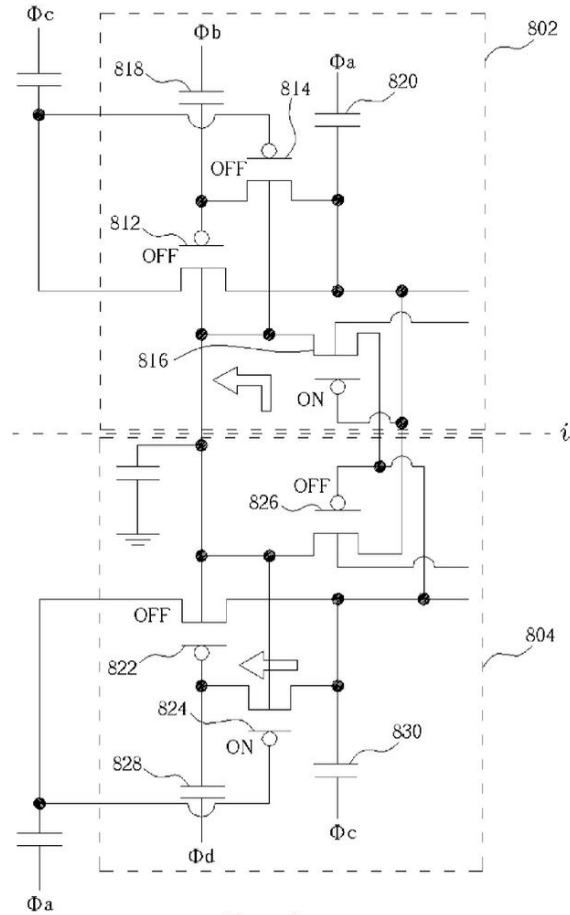


Fig. 8

Lin '129, Fig. 12:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

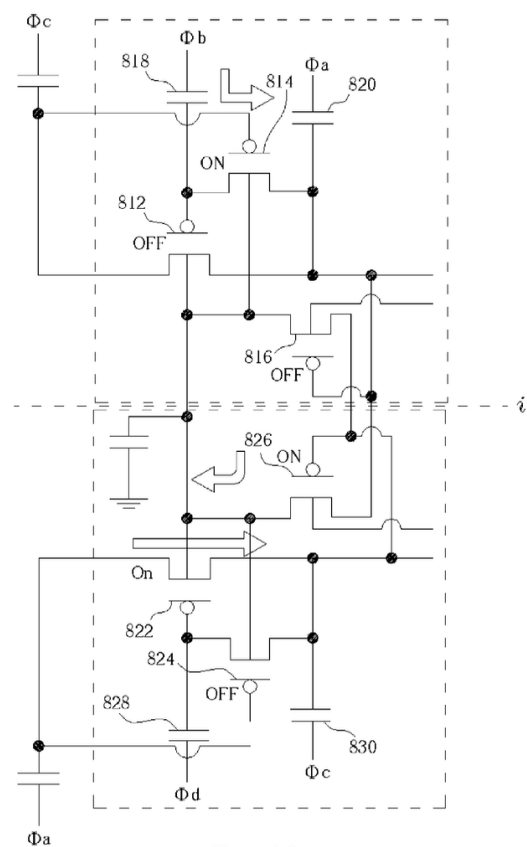


Fig. 12

Lin '129, col. 5:

Please continue to refer to FIG. 6 which shows another 30
embodiment of the present invention with the addition of an
extra voltage controller 601 comprising a NMOS transistor
602, a capacitor 604, and an inverter 606. The NMOS
transistor 602 is controlled by an additional set of control
clock pulses Fe. The additional control clock pulse Fe is set 35
to high before the operation of the dual pumping operation
and is then set to low during the operation of each stage of
the dual pumping operation to prevent any P-N junction
forward conduction. The NMOS transistor 602 is electri-
cally coupled to a common node which is further electrically 40
coupled to the capacitor 604 and the inverter 606 that are
also controlled by the clock pulse Fe. The voltage controller
601 is separately electrically coupled to all stages 510, 520,
530, and 540 to ensure appropriate bias conditions at the
initial pumping operation. Since the voltage controller 601 45
of each stage 510, 520, 530, and 540, are the same, the first
voltage controller 601 of the first stage 510 is chosen to
represent the rest of the duplicated stages. The voltage
controller 601 is electrically coupled to the body of the main
pass transistor of the first pumping unit 512 and the second 50
pumping unit 514 to eliminate any body effect because the
voltage difference of the source/drain and the body is close
to zero. After the input voltage Vdd controlled by clock
pulse ϕ is inputted to the first stage 510 of the dual pumping
circuit 500, the transistor M1 of the first pumping unit 512 55
and M1o of the second pumping unit 514 (either transistor
M1 or M1o being the first to transfer charge depending on
the design of the clock pulses) is ready to transfer the
pre-charge across to the subsequent stage 520. At the
instance when the charge is transferred, the clock pulse ϕ 60
is set to low and the body of the main pass transistor M1 is
at Vdd which minimizes body effects because the voltage
difference of the source/drain and the body is approximately
zero. For the subsequent stages, the output from every stage
is commonly electrically coupled to the voltage controller of 65
the subsequent stages so the partially pumped output voltage
from each stage is used as the voltage to control the main

Lin '129, col. 8:

Please proceed to FIG. 12 which shows the operation of
the stage 530 of the dual pumping circuit 500 in FIG. 5 in
20 interval 5 in FIG. 7 when the clock pulse ϕ_a is high, the clock
pulse ϕ_b is high, the clock pulse ϕ_c is low, and the clock
pulse ϕ_d goes from high to low. Similar to interval 2, the
second pumping unit 804 performs a charge sharing while
the body of the transistors in the second pumping circuit 804
25 are pumped to the highest level to prevent any body effects.

Lin '129, col. 8:

Please refer to FIG. 14 which shows the HVC used for
 35 generating high voltage clock pulses from a low input
 voltage. The input voltage V_{in} is inputted to a first inverter
 1402 and then to a second inverter 1404 where the voltage
 signal is transferred to both a first capacitor 1406 to a third
 inverter 1408 that is further electrically coupled to a second
 40 capacitor 1416. The first capacitor 1406 is electrically
 coupled to the source of the first NMOS transistor 1410 and
 the gate of the transistor 1412 and the second capacitor 1416
 is electrically coupled to the source of the second NMOS
 transistor 1412 and the gate of the first NMOS transistor
 45 1410. As a result, the two NMOS transistors 1410 and 1412
 are cross-coupled to increase the amplitude of the input
 voltage V_{in} . To substantially reduce body effects, the body
 of the third PMOS transistor 1414 is electrically coupled to
 the drain of a fifth NMOS transistor 1424 whose source is
 50 electrically coupled to V_{dd} and gate is controlled by clock
 pulse ϕ_e which also at the same time control the third
 capacitor 1420 through a inverter 1422. The high voltage
 clock pulses ϕ_b and ϕ_d can be achieved by such cross-
 coupling scheme to increase the pumping gain at low supply
 55 voltage and to reduce power consumption and chip area.

Lin '129 at 8:56-9:3 (“Please refer to FIG. 15 which shows the negative dual pumping circuit 1500 according to another embodiment of the present invention. The negative dual pumping circuit 1500 is identical to that in FIG. 5 except for the choice of transistors. The PMOS transistors in the positive dual pumping circuit 500 are replaced by NMOS transistors in the negative dual pumping circuit 1500, and vice versa. The operation and structure of the negative dual pumping circuit 1500 is identical to that of the positive dual pumping circuit 500 so it is therefore purposely omitted. With the popular triple-well CMOS technology, the present invention can achieve both positive pumping for the use of PMOSFETS and NMOSFETS for negative pumping which provides flexibility in design when both positive and negative pumping are required.”).

Lin '129, col. 9:

In contrast to the prior art, the present invention provides 50
 a dual pumping circuit that can be implemented in either
 positive or negative with provides good pumping perfor-
 mance at low supply voltage (1V to 2V) using the popular
 triple-well technology. The dual pumping circuit uses four-
 phase clocks that has one pair of identical but out of phase 55
 clocks. The other two of the clocks may be chosen to be
 generated by a high voltage circuit to provide better pump-
 ing at low voltage. The positive dual pumping circuit uses
 PMOS transistors and the negative pumping circuit uses
 NMOS transistors where the transistors have special sub- 60
 strate connection to avoid body effect and p-n junction
 conduction.

Those skilled in the art will readily observe that numerous
 modifications and alterations of the device may be made
 while retaining the teachings of the invention. Accordingly, 65
 that above disclosure should be construed as limited only by
 the metes and bounds of the appended

Park '791, Fig. 7:

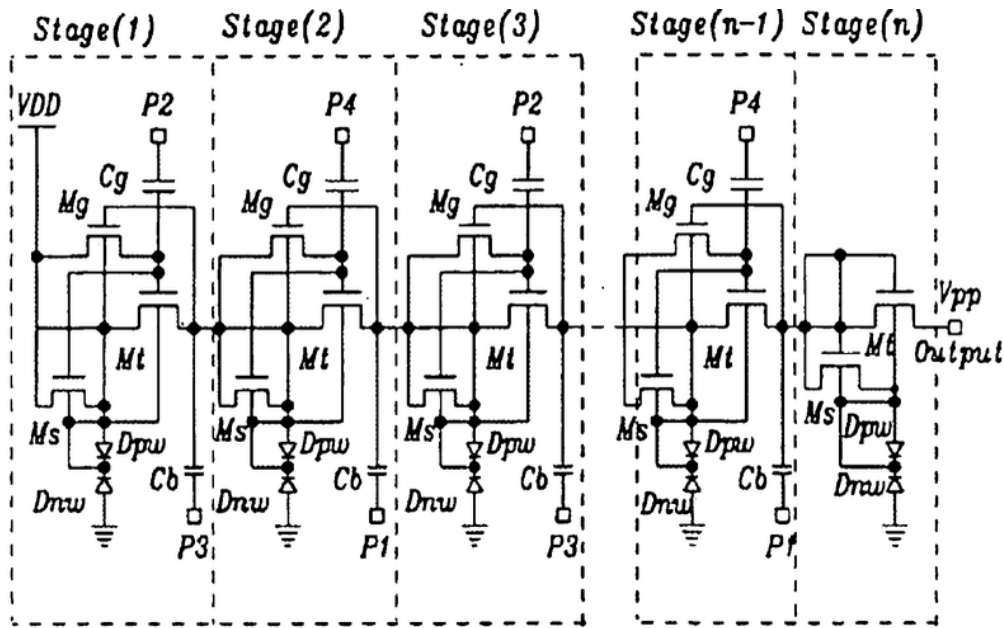


FIG. 7

Park '791, Fig. 13:

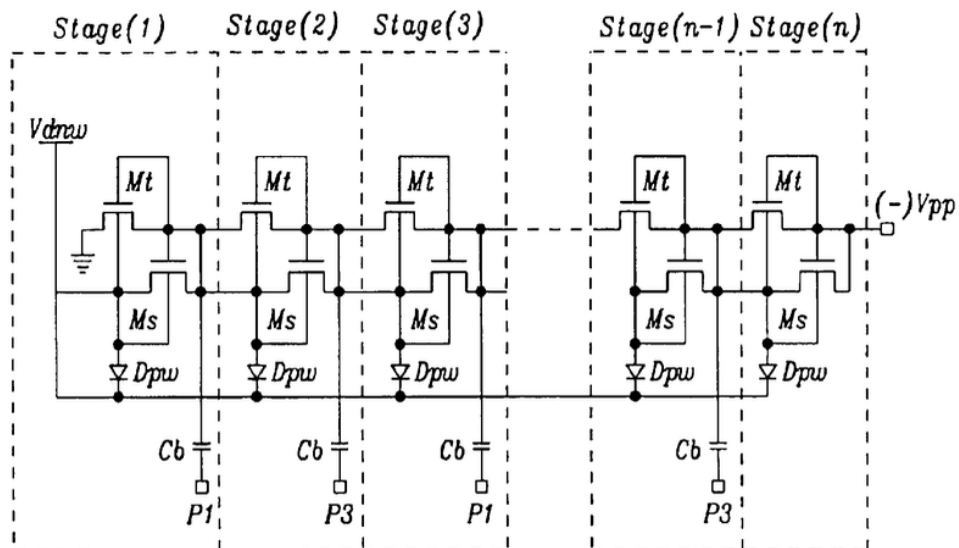


FIG. 13

Park '791, col 4:

25 The auxiliary device, which is used for pre-charging a
voltage on the gate of the charge transfer device, couples the
input signal of each stage to the gate of the charge transfer
device; and therefore, increases the boost coupling effect on
30 the charge transfer MOS device, which results in increasing
a signal level at the source (output) of the charge transfer
device. The auxiliary device, that is used for buffering the
drain of the charge transfer device from the P-well and the
N-well, couples the drain voltage of the charge transfer
35 device to the P-well and the deep N-well to reduce the body
effect and to improve capacitive coupling effect on the drain
of charge transfer MOSFET device by reducing the effects
of the P-well and Deep N-well parasitic capacitance.

40 It should be noted that although the present invention has
been oriented to a charge pump circuit formed from
N-channel MOSFET devices in a P-well within a deep
N-well on a P-substrate, a similar charge pump circuit could
be formed from P-channel MOSFET devices in an N-well
within a deep P-well residing on an N-substrate.

Park '791, col. 5:

Continuing to refer to FIG. 7, an input voltage of a stage
is applied to the drain of the charge transfer MOS device Mt
within the stage. This same input voltage is coupled to the
gate of the charge transfer MOS device Mt by means of an
auxiliary MOS device Mg and clock signal P3 in odd 50
numbered stages and clock signal P1 in even number stages.
Similarly, a boosted input signal to a stage is coupled to the
P-well Dpw and deep N-well Dnw by the auxiliary MOS
device Ms, which is gated by the gate signal of the charge
transfer MOS device Mt. Clock P2 for odd numbered stages 55
and clock P4 for even number of stages are applied to the
gate of the charge transfer MOS device through capacitor
Cg.

Park '791, cols. 6-7:

In FIG. 9 is shown a cross section view of a portion of the circuitry in a stage of the multi-stage charge pump circuit shown in FIG. 7, which includes the charge transfer MOS device Mt and the auxiliary MOS device Ms. Not shown in FIG. 9 is the auxiliary MOS device Mg. The MOS devices Mt and Mg are shown in a P-well within the deep N-well of a stage of the charge pump residing on a P-substrate. An input charge pump voltage from a previous stage is connected to the drain D1 of the charge transfer N-channel MOSFET device Mt and the drain D2 of the auxiliary N-channel MOSFET device Ms. The source S2 of the auxiliary MOSFET device Ms is connected to both the P-well and the deep N-well. A pump clock signal is connected to the gates of the charge transfer MOS device Mt and the auxiliary MOS device Ms through a coupling capacitor Cg (not shown). The output of the stage is taken from the source S1 of the charge transfer MOS device Mt and besides being connected to the next stage, the output is connected to a coupling capacitor Cb (not shown) as well as the gate of the auxiliary MOS device Mg (not shown). The auxiliary MOS device Mg is also located within the same P-well as the charge transfer MOS device Mt and the auxiliary MOS device Ms. From this cross section it is demonstrated how the auxiliary MOS device Ms buffers the drain D1 of the charge transfer MOS device Mt from the P-well and the deep N-well. The input voltage at the drains D1 and D2 of the charge transfer MOS device Mt and the auxiliary MOS device Ms, respectively, is coupled to the P-well and the deep N-well by the auxiliary MOS device Ms controlled by the gate control signal, which is formed from the auxiliary MOS device Mg and the P2 or P4 clock signals at the gate of the charge transfer MOS device Mt schematically shown in FIG. 7. Therefore, the P-well and the deep N-well see a voltage similar to the voltage produced at the input of the charge transfer MOS device Mt when the charge transfer MOS device Mt is turned on. This allows the P-well and the Deep N-well to have a voltage similar to the source S1 of the charge transfer MOS device Mt when it is turned on so that the charge transfer MOS device Mt is able to transfer a boosted high voltage from the input to the output without

any voltage loss caused by the body effect. The silicon area penalty resulting from the auxiliary MOS devices Mg and Ms can be negligible because their area is small compared to the charge transfer MOS device Mt and coupling capacitors Cb and Cg.

5

Park '791, col. 7:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

A negative high voltage output charge pump circuit can also be realized using the same triple-well structure of the present invention, except that deep N-well is connected to 50 V_{dnw} , which is a positive voltage and can be either the power supply VDD, or ground. FIG. 12 shows a cross-sectional view of the charge pump circuit of present invention for a negative high voltage output. The charge transfer MOS device M_t and auxiliary MOS device M_s are formed 55 in their own P-well which act as substrate of the MOS devices. The deep N-well can be shared with other pumping stages and connected to ground or power supply VDD. The source S_2 and drain D_2 of the auxiliary MOS M_s are coupled to the P-well and the drain D_1 of the charge transfer 60 MOS device M_t , respectively. The drains D_1 and D_2 and the gates of the charge transfer device M_t and auxiliary device M_s are coupled together and are further connected to the coupling capacitor C_b .

Park '791, cols. 7-8:

FIG. 13 is a circuit diagram of an embodiment of the 65 present invention of a charge pump for generating a negative voltage output. The circuit uses an N-channel MOSFET as

charge transfer device M_t and an auxiliary device M_s . The pumping stages are connected in series from ground to the negative output voltage $(-V_{pp})$. Each pumping stage includes one charge transfer MOS device M_t , one auxiliary 5 MOS device M_s and one coupling capacitor C_b . The P-well within each pump stage, Stage (1), Stage (2), Stage (3), Stage (n-1) and Stage (n), resides within a deep N-well and isolates the circuitry of each stage. The deep N-well can be common for each P-well or separate for each P-well. The 10 auxiliary device M_s couples a boosted voltage to the P-well to reduce body effects on the pumped voltage within each stage. The diode D_{pw} represents the parasitic diode junction between the P-well and the deep N-well. A positive voltage V_{dnw} , which can be either VDD or ground, is applied to the deep N-well to insure that the diode D_{pw} remains back 15 biased throughout the negative charge pump operations.

Park '791, col. 8:

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

The circuit operation of the negative charge pump is carried out in the same manner as the positive charge pump circuit, except that the input of the charge pump circuit is coupled to the ground, instead of VDD. A two clock scheme using clocks P1 and P3, or P2 and P4, shown in FIG. 8 for the positive charge pump circuit can be used for the negative charge pump circuit. When the charge transfer MOS device Mt in a first pump stage is turned on by a clock signal, a boosted negative charge is created at the output of a first pump stage, which is coupled to the drain nodes of the charge transfer MOS device Mt and auxiliary MOS device Ms. The boosted negative charge is transferred to the input of a second pump stage connected to the output of the first pump stage. The boosted negative charge is coupled to a source of the charge transfer MOS device Mt in the second stage. At the same time, the auxiliary MOS device Ms of the first stage is also turned on so that the boosted negative charge of the output of the first pump stage is coupled to the P-well of the first pump stage. The coupling of the boosted negative charge to the P-well reduces the body effect on the charge transfer MOS device Mt, which results in an increased charge transfer efficiency.

Campardo at 372-373:

Alternatively, a dynamic biasing of the bulk nodes could be devised. The structure shown in Fig. 15.14 allows biasing the bulk nodes of the pump transistors to the lowest voltage between drain and source of the transistor (or the highest one in case the same structure would have been realized using PMOS transistors) exploiting the stages of the pump itself. The disadvantage of this solution is that the bulk nodes of the pump might be not biased during the transient between one semi-

15.4 Different Types of Charge Pumps 373

period and the following one, because of the delay between the turning on of the two transistors M_1 , M_2 . This risk must be carefully evaluated in the design phase taking into account the parasitic capacitances that influence the stages, the tubs of the stages themselves, the commutation time of the phases, etc.

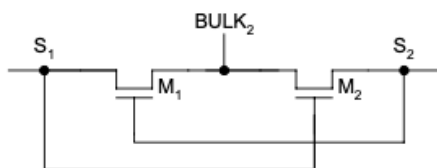


Fig. 15.14. Dynamic biasing of the bulk nodes

Ex. A-OB: Invalidity of U.S. Patent No. 7,777,557 – Omnibus Obviousness Chart

To the extent that AMT contends the Omnibus References do not explicitly or implicitly disclose this limitation, it would have been obvious to a person of ordinary skill in the art based on each of the Omnibus References alone, and/or the teachings with respect to this claim element as detailed in Defendant’s other invalidity charts and Section II.B.3.a of its cover pleading