

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC.,
Petitioner,

v.

ADVANCED MEMORY TECHNOLOGIES, LLC,
Patent Owner.

Case IPR2025-01452
Patent 7,777,557

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107**

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EXHIBIT LIST

Exhibit	Description
2001	Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 1, filed Dec. 30, 2024 (E.D. Tex.)
2002	Amended Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 25, filed April 2, 2025 (E.D. Tex.)
2003	Second Amended Docket Control Order, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 27, filed April 11, 2025 (E.D. Tex.)
2004	RESERVED
2005	Order Denying Motion for Stay Pending <i>Inter Partes</i> Review, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 79, filed Sept. 3, 2025 (E.D. Tex.)
2006	United States District Courts — National Judicial Caseload Profile (including data through June 30, 2025), https://www.uscourts.gov/sites/default/files/document/fcms_na_distprofile0630.2025.pdf (accessed October 10, 2025).
2007	Defendant SH Hynix’s Preliminary Invalidity Contentions Cover Pleading, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)
2008	Omnibus Obviousness Chart A-OB for U.S. Patent No. 7,777,557, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)
2009	February 3, 2022 Non-Final Office Action Concerning Application No. 14/698,542
2010	U.S. Patent No. 11,437,907 to SK Hynix Inc.
2011	Docket Navigator Time To Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025
2012	Lex Machina Time to Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025

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I. INTRODUCTION

Patent Owner Advanced Memory Technologies, LLC (“AMT”) respectfully requests that the Director deny SK Hynix Inc.’s (“Petitioner”) Petition to institute *inter partes* review of U.S. Patent No. 7,777,557 (the “’557 Patent”) because Petitioner has not shown a reasonable likelihood of prevailing on its challenge to any of claims 1–12 and 14. *See* Petition at 2.

The ’557 Patent claims a booster circuit¹ with a two-row structure of booster cells, each with two well regions, the second of which is inside the first. For example, the first well region may be a “deep N-well” within which a second, P-type well region is formed. In the claimed circuits, the output potentials of the booster circuits in both rows are used in biasing the first well region (*e.g.*, the deep N-well). The Examiner found these features distinguished the claims over the prior art, including Meng—the primary reference in two of Petitioner’s three Grounds. The Examiner expressly distinguished Meng as not teaching the limitations on biasing the *first well region*. Petitioner still fails to show that feature in the cited art.

First, Petitioner’s mapping for Ground 1 improperly carves up the booster cell of the allegedly anticipatory Fukushima reference. The portions of the booster cells’

¹ Booster circuits can be used to boost a lower voltage power supply to a higher voltage.

circuit components that Petitioner alleges direct an output potential to the deep N-well are, in fact, the components that generate the output potential. But when generated, Fukushima's output is transmitted to the next stage of the booster circuit, not the deep N-well. Furthermore, Petitioner improperly relies on a combination of distinct embodiments in Fukushima for anticipation without showing that the disclosures regarding one apply to the other.

Second, Meng expressly teaches that its deep N-well is biased using a signal having a constant potential rather than using the output potential of the booster cells, as claimed by the '557 Patent. Petitioner's theory for Ground 2 ignores Meng's express disclosure and relies instead on unsupported assumptions about the relied upon structures in the cited embodiment. Meng therefore does not anticipate any of the challenged claims.

Third, Petitioner's combination of Meng with Park underscores the deficiency of Ground 2 because it does not rely on Meng to teach the biasing of the deep N-well. Moreover, the combination with Park does nothing to cure Meng's deficiencies. Neither Park nor Meng disclose using the output potentials of booster cells in two booster cell rows to bias a deep N-well. Park does not even disclose a two-row booster circuit, let alone any use for outputs from cells in both rows. And Meng teaches an unrelated technique for biasing the deep N-well (as shown for Ground 2).

The Petition thus cannot prevail on any claim and should be denied.

II. BACKGROUND

A. The '557 Patent

The '557 Patent, which is titled “Booster Circuit,” issued on August 17, 2010 to Seiji Yamahira of Panasonic Corporation. EX1001 at (45), (54), (75), (73). It issued from an application filed on January 17, 2008. *Id.* at (22). The '557 Patent generally “relates to a booster circuit employing a switching element having a triple-well structure.” *Id.*, at 1:6–7.

1. Claims

The Petition challenges independent claims 1 and 14, along with dependent claims 2–12. Petition at 2. Independent Claims 1 and 14 are reproduced below, using the same limitation labels as used in the Petition for consistency:

1[pre]	A booster circuit comprising:
1[a]	boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region,
1[b]	and at least one switching element in either or both of the first well region and the second well region, wherein the at least one switching element switches to transfer charges from a first terminal to a second terminal;
1[c]	a first boosting cell row including N stages ($N \geq 1$) of the boosting cells;

	a second boosting cell row including M stages ($M \geq 1$) of the boosting cells; and
1[d]	at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i-th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i-th stage ($1 \leq i \leq M$) ² of the second boosting cell row,
1[e]	wherein the well bias potential of the at least one analog comparison circuit is applied to the first well region of the switching element included in the at least one boosting cell of the first and second boosting cell rows.
14[pre]	A booster circuit comprising:
14[a]	boosting cells each having a first-conductivity type first well region on a substrate, a second-conductivity type second well region in the first well region, and at least one switching element in either or both of the first well region and the second well region,
14[b]	wherein the at least one switching element switches ON/OFF a connection between a first terminal and a second terminal so as to transfer charges from the first terminal to the second terminal;
14[c]	a first boosting cell row including N stages ($N \geq 1$) of the boosting cells; and a second boosting cell row including M stages ($M \geq 1$) of the boosting cells;

² See Certificate of Correction, EX1001 at 30.

14[d]	wherein a potential of the first well region of the at least one switching element included in the boosting cells in the first and second boosting cell rows is controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.
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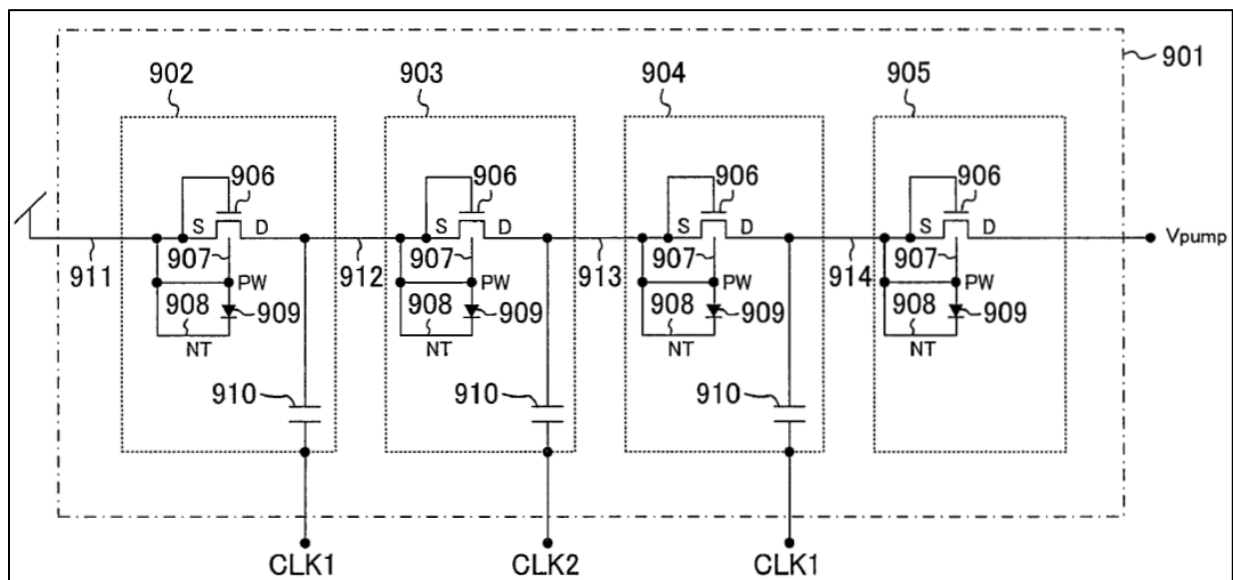
EX1001 at 11:50–12:4 (claim 1), 14:4–23 (claim 14). Claims 2–12 all depend from claim 1. *Id.* at 12:5–13:6.

2. Specification

As noted above, the '557 Patent “relates to a booster circuit employing a switching element having a triple-well structure.” EX1001 at 1:6–7. The '557 Patent observes that “non-volatile semiconductor memory devices” such as “flash memories . . . require data read and data write using a single power supply voltage or low power supply voltages.” *Id.*, at 1:9–14. These “single” or “low power supply voltages” need to be boosted to higher voltages for use in devices such as “non-volatile semiconductor memory devices.” *Id.*

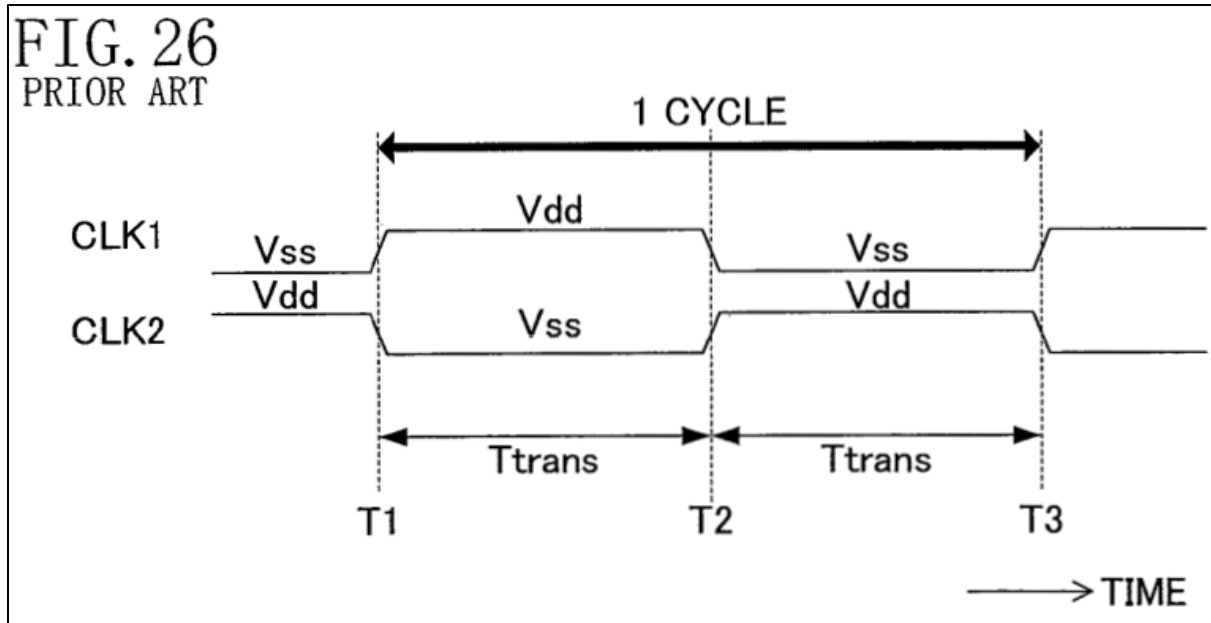
The '557 Patent notes “there is a known booster circuit employing a triple-well structure switching element” that can provide such a boosted voltage, which the Patent discusses in the context of Figures 25 and 26. *See id.* at 1:18–2:11. Figure 25 shows this arrangement with boosting cells 902-904 arranged in “an exemplary three-stage configuration.” *Id.* at 1:22–28. “CLK1 is input to the odd-numbered-stage cells and CLK2 is input to the even-numbered-stage cell” for controlling the

boost operation at the various stages. Furthermore, “the P well 907 and the N well 908 of each charge transfer transistor 906 of the boosting cells 902 to 904 is connected to the source of the charge transfer transistor 906 so that they have the same potential.” *Id.* at 1:38–41. The arrangement shown in Figure 25 suppresses a “substrate biasing effect . . . thereby making it possible to suppress a decrease in charge transfer efficiency during the boosting operation.” *Id.* at 2:8–11.



EX1001, FIG. 25

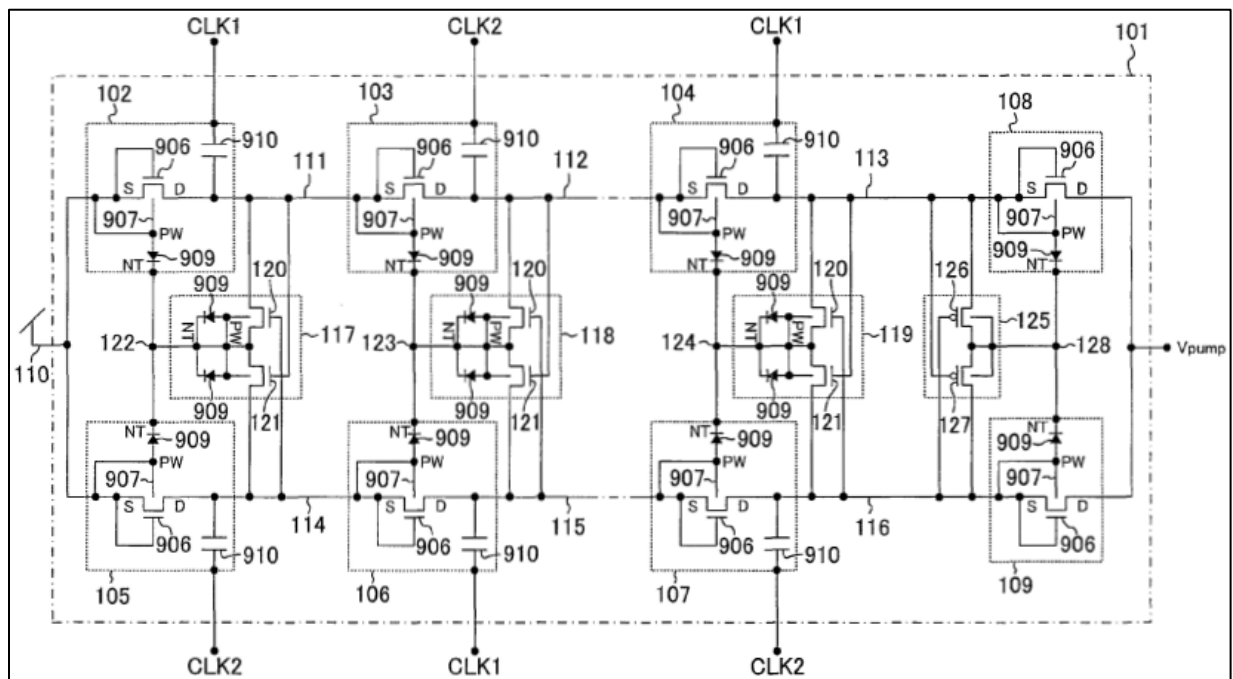
In the example given, the clock signals CLK1 and CLK2 alternate between power supply voltage V_{dd} and ground voltage V_{ss} in order to charge the boosting cells in stages as shown in Figure 26 below. *See id.*, at 1:42–2:11.



EX1001, FIG. 26

The '557 Patent identifies several shortcomings of this conventional booster circuit arrangement. For example, “the source and the N well 908 of the charge transfer transistor 906 are connected to each other, so that a parasitic capacitance formed by the N well 908 is charged and discharged by voltage transition widths of the clock signals CLK1 and CLK2 in response to voltage transitions of the clock signals CLK1 and CLK2.” *Id.* at 2:12–18. The '557 Patent also explains that “charges supplied by the clock signals CLK1 and CLK2 are used to charge and discharge the N well 908, disadvantageous[ly] resulting in a decrease in boost efficiency.” *Id.* at 2:18–21. Furthermore, “since the source and the N well 908 of the charge transfer transistor 906 are connected to each other, it is necessary to separate the N wells 908 of the charge transfer transistors 906 from each other, disadvantageously resulting in an increase in layout area.” *Id.* at 2:22–26.

In response, the '557 Patent teaches solutions to those and other deficiencies in conventional booster circuits. For example, "FIG. 1 shows an exemplary configuration of the booster circuit of the present invention." *Id.* at 7:7–8. "101 indicates a two-parallel booster circuit which receives two-phase clock signals CLK1 and CLK2 and generates an output terminal voltage (boosted voltage) V_{pump} by a boosting operation." *Id.* at 7:8–11. As shown, the Figure 1 embodiment includes boosting cells 102–107, backflow preventing circuits 108–109, low-voltage output analog comparison circuits 117–119, and high-voltage output analog comparison circuit 125.



EX1001, FIG. 1.

The '557 Patent explains that in this arrangement "the potentials of the N wells of the boosting cells 102 to 107 and the backflow preventing circuits 108 and 109

can be fixed to the input potentials or the output potentials of the respective boosting cell stage, so that the amount of charges which are charged and discharged between the N well and the substrate can be reduced, i.e., current consumption can be reduced.” *Id.* at 8:43–49. Furthermore, “by reducing the amount of charges which are charged and discharged between the N well and the substrate, the amount of charges transferred to the next stage can be increased, so that an improvement in boost efficiency can be expected.” *Id.* at 8:50–54.

3. Prosecution History

As Petitioner acknowledges (Petition at 14), Meng (EX1006) was previously considered during prosecution and the Examiner expressly found the issued claims patentable over Meng. EX1002 at 200; *see id.* at 179–80. In doing so, the Examiner withdrew a rejection based on Meng and agreed with the Applicant that “Meng fails to teach that the well potential of the analog comparison circuit is applied to the deep-n well corresponding to the first well region,” as recited in the claims. *Id.* at 192; *see id.* at 200 (“Applicant’s arguments are persuasive.”). As discussed in more detail below, the Examiner was correct that Meng fails to teach or render obvious the ’557 Patent claims as issued, and Petitioner’s arguments to the contrary are incorrect.

B. Petitioner’s Grounds

The Petition asserts the following grounds against the Challenged Claims:

Ground	Basis	References	Claims
1	§ 102 (anticipation)	Fukushima	1, 3, 5, 10–12, 14
2	§ 102 (anticipation)	Meng	1–3, 9, 10, 14
3	§ 103 (obviousness)	Meng, in view of Park	1–12, 14

Petition at 2.

As shown above, independent claims 1 and 14 are challenged as part of Grounds 1–3. Because Grounds 1–3 all fail to teach or render obvious every limitation of Claims 1 and 14, the Petition necessarily fails to present a reasonable likelihood of invalidating any of the challenged claims.

1. Fukushima (EX1005)

Fukushima is U.S. Patent No. 6,107,864 to Kazuhiko Fukushima and Atsuo Yamaguchi, which is titled “Charge Pump Circuit.” EX1005 at (11), (54), (75). Fukushima was filed on February 1, 1999, and claims priority to an Aug. 24, 1998 foreign application; it issued on August 22, 2000. *Id.* at (22), (30), (45). Fukushima “relates to a charge pump circuit with a plurality of booster stages.” *Id.* at 1:4–6.

2. Meng (EX1006)

Meng is U.S. Patent No. 6,501,325 to Anita Meng, which is titled “Low Voltage Supply Higher Efficiency Cross-Coupled High Voltage Charge Pumps.” EX1006 at (10), (54), (75). Meng was filed Jan. 18, 2001 and issued on Dec. 31, 2022. *Id.* at (22), (45). Meng “relates to a method and/or architecture for charge pumps generally and, more particularly, to a method and/or architecture for low

voltage supply high efficiency cross-coupled high voltage charge pumps.” *Id.* at 1:7–10.

As discussed above in Section II.A.3, the Examiner considered Meng during prosecution and allowed the claims of the ’557 Patent after correctly finding them patentable over Meng.

3. Park (EX1007)

Park (EX1007) is U.S. Patent No. 6,914,791 to Ki-Tae Park et al., which is titled “High Efficiency Triple Well Charge Pump Circuit.” EX1007 at (10), (54), (75). Park was filed June 24, 2003 claiming priority to a Nov. 6, 2002 provisional, and issued on July 5, 2005. *Id.* at (22), (45), (60). Park “relates to integrated circuits and more specifically to charge pump circuits providing high output voltage and current at low power supply voltages.” *Id.* at 1:10–12.

III. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner suggests that “[a] person of ordinary skill in the art (‘POSITA’) as of January 17, 2007, would have had a master’s degree in electrical engineering, computer engineering, physics, or a related field, with at least two years of experience in the field of integrated circuits and/or memory devices.” Petition at 2. It is unnecessary for Patent Owner to put forward a different definition at this stage, because the Petition fails to present a reasonable likelihood of success under this (or any other reasonable) definition of a POSITA.

IV. CLAIM CONSTRUCTION

“[A] petition **must** state how a challenged claim is to be construed and how each element of the construed claim is found in prior art patents or printed publications.” *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*, IPR2021-01569, Paper 16, at 5 (citing 37 C.F.R. §§ 42.104(b)(3)–(4)) (emphasis added). Petitioner offered no express constructions, asserting that it “has applied the plain and ordinary meaning understood by a POSITA at the time of the alleged invention.” Petition at 16.

V. LEGAL STANDARDS

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”). To meet this burden, “the petition must specify where **each element of the claim** is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4) (emphasis added). And “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l*

Graphics, Inc., 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, “[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

When an expert declaration is “conclusory and unsupported,” it is “entitled to little weight.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (August 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Upjohn Co. v. Mova Pharm. Corp.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000) (“Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity determination.”) (quoting *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985)); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 138 (Fed. Cir. 1986) (“Although in some circumstances unsupported oral testimony can be sufficient to provide prior knowledge or use, it must be regarded with suspicion and subjected to close scrutiny.”).

VI. PETITIONER FAILS TO SHOW A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CLAIM

The Petition fails to show a reasonable likelihood of prevailing on any claim at least because none of the asserted grounds teaches or renders obvious each

limitation of independent Claims 1 and 14. For example, claim 1 recites in part “at least one analog comparison circuit for outputting a well bias potential generated by an output potential of the boosting cell on the i -th stage ($1 \leq i \leq N$) of the first boosting cell row and an output potential of the boosting cell on the i -th stage ($1 \leq i \leq M$) of the second boosting cell row.” EX1001 at 11:62–67. That *well bias potential* must be “applied to the first well region of the switching element” recited earlier in the claim. *Id.*, at 12:1–4. Claim 14 recites a similar limitation, which requires that “a potential of the first well region” be “controlled according to an output potential of the boosting cells of the first boosting cell row and an output potential of the boosting cells of the second boosting cell row.” *Id.*, at 14:18–23. For each asserted Ground, Petitioner fails to show that the cited art discloses these limitations or (for Ground 3, the sole obviousness Ground) that the combination of Meng and Park renders them obvious.

As discussed below for each Ground, Petitioner identifies a deep N-well as the *first well region* of the claims. But none of the references teach biasing the deep N-well using the *output potentials* of the *booster cells* from two *booster cell rows*, let alone the claimed arrangements for doing so (*e.g.*, using an *analog comparison circuit*).

**A. Fukushima Does Not Anticipate Any Challenged Claim, and
Ground 1 Therefore Fails**

Petitioner’s first Ground—asserting Fukushima anticipates claims 1, 3, 5, 10–12, and 14—fails because Fukushima does not disclose every element of the challenged claims, including at least those discussed above about using the *output potentials* of the *booster cells* to bias the *first well region*.

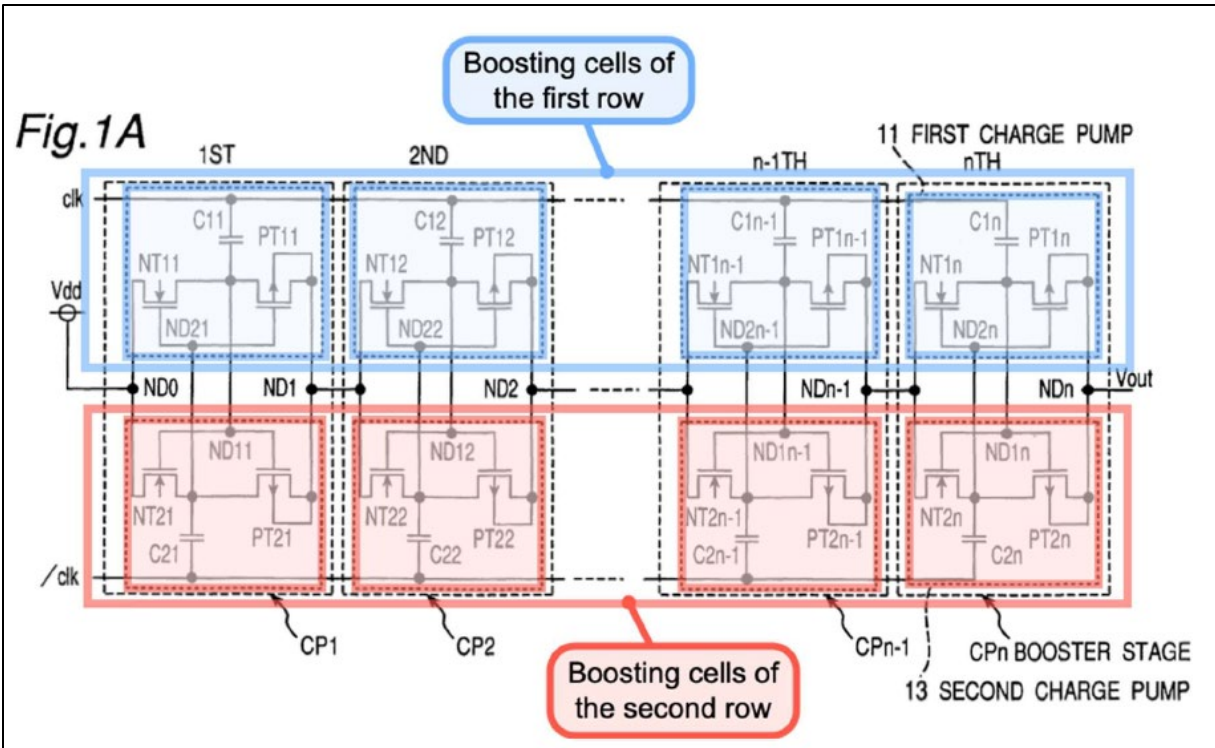
**1. Fukushima Does Not Disclose the Claimed Relationships
Between the *Output Potentials* of the *Booster Cells* and the
*Well Bias Potential***

Fukushima does not anticipate because it does not teach using “an output potential of the boosting cell . . . of the first boosting cell row and an output potential of the boosting cell . . . of the second boosting cell row” to bias the deep N-well identified as the *first well region* of the claims. EX1001 at 11:62–67; *see id.* at 14:20–23 (reciting similar limitation of claim 14). Indeed, as shown below, Petitioner contends that the structure in Fukushima responsible for using the *output potentials* of the *boosting cells* as claimed is the same structure that generates those *output potentials*.³ Petition at 21–24, 33–34. According to Petitioner’s theory, the alleged *analog comparison circuit* uses *output potentials* that ***it has not yet generated*** to

³ The Petition maps this structure to the *analog comparison circuit* of claim 1 (Petition at 21–24) and relies on the same theory for the corresponding limitation of claim 14 (*id.*, at 33–34).

[illegible]

As illustrated in Petitioner’s annotations to Fukushima’s Figure 1A below, Petitioner identifies Fukushima’s first charge pump 11 and second charge pump 13 as the *boosting cells* of the *first* and *second boosting cell rows*, respectively. Petition at 20–21.



Petition at 21 (annotating EX1005 FIG. 1A)

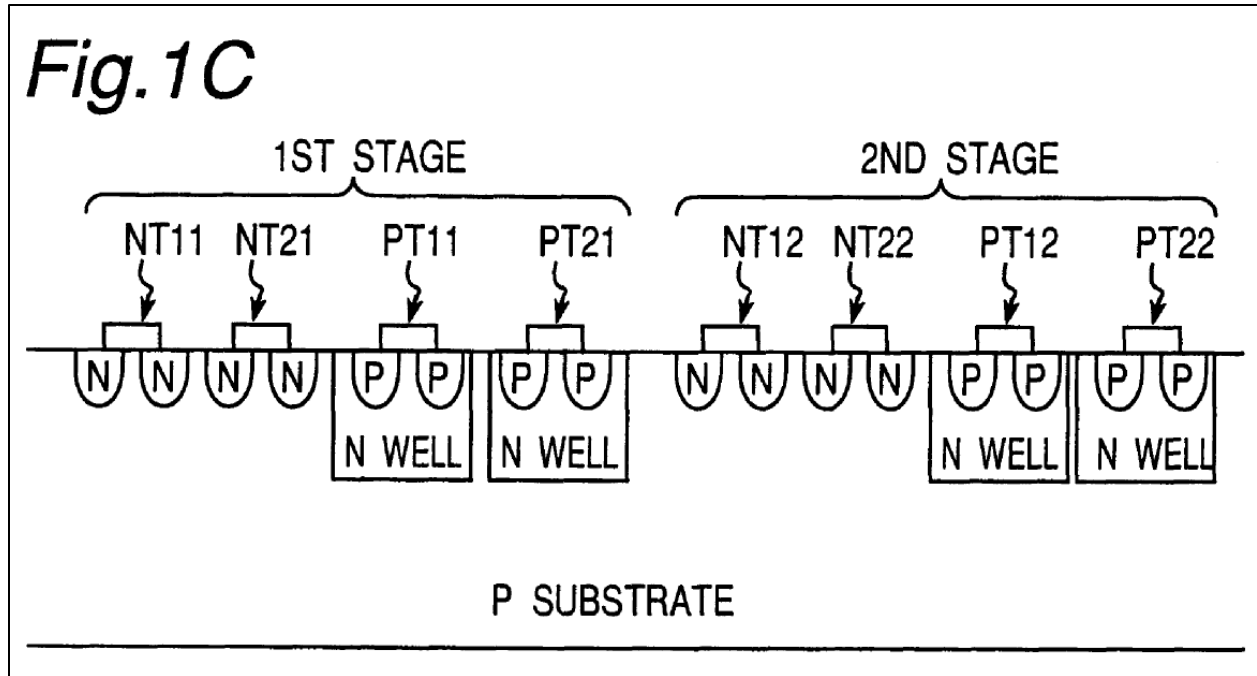
These alleged *boosting cells* are both parts of booster stage CP_n . See EX1005 at 4:66–67 (“Booster stage CP_n further comprises first and second charge pumps 11 and 13. . .”), FIG. 1A. Fukushima teaches that booster stage CP_n has only one output node. See *id.*, at 4:59–64 (“Each booster stage CP_n comprises . . . a node ND_n as an output node from which the charge is supplied to the input node of the next (downstream) booster stage CP_{n+1} .”).

Petitioner’s mapping of the “analog comparison circuit” attempts to carve out the output node (ND_n) and the PMOS transistors ($PT1_n$ or $PT2_n$) from both charge pumps in a given stage. See, e.g., Petition at 22. The remaining portion of the charge pumps (11, 13) cannot function as “boosting cells” because they no longer include

the PMOS transistors that send the accumulated charge from the capacitors to the output node. *See id.*; EX1005 at 5:9–12 (“The PMOS transistor[] PT1_n or PT2_n sends the charge accumulated in the corresponding pumping capacitor C1_n or C2_n to the node ND_n, respectively.”). Accordingly, the “analog voltage levels at nodes ND1_n and ND2_n” (the alleged *output potentials* of the claims), Petition at 22, are not output potentials of “boosting cells” on the first and second row, as the claims require. Petitioner relies on the same alleged *output potentials* for claim 14, *see id.*, at 33, and Ground 1 fails as to claim 14 for the same reasons.

2. Petitioner Relies on Disclosures Pertaining to Different Embodiments for Anticipation but Fails Even to Allege the Necessary Link Between Disclosures

Independent of the foregoing, the Petition cannot prevail because it relies on disclosure pertaining to different embodiments in Fukushima for different elements of the same claims. Anticipation requires “an anticipatory reference to show all of the limitations of the claims arranged or combined in the same way as recited in the claims.” *NetMoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008). Fukushima’s Figure 1A (which Petitioner cites for some claim features) presents “a circuit diagram of a charge pump circuit according to a first preferred embodiment.” EX1005 at 4:5–7. The structure of the semiconductor substrate for that “first preferred embodiment” is depicted in Figure 1C (reproduced below). *Id.*, at 4:10–12.



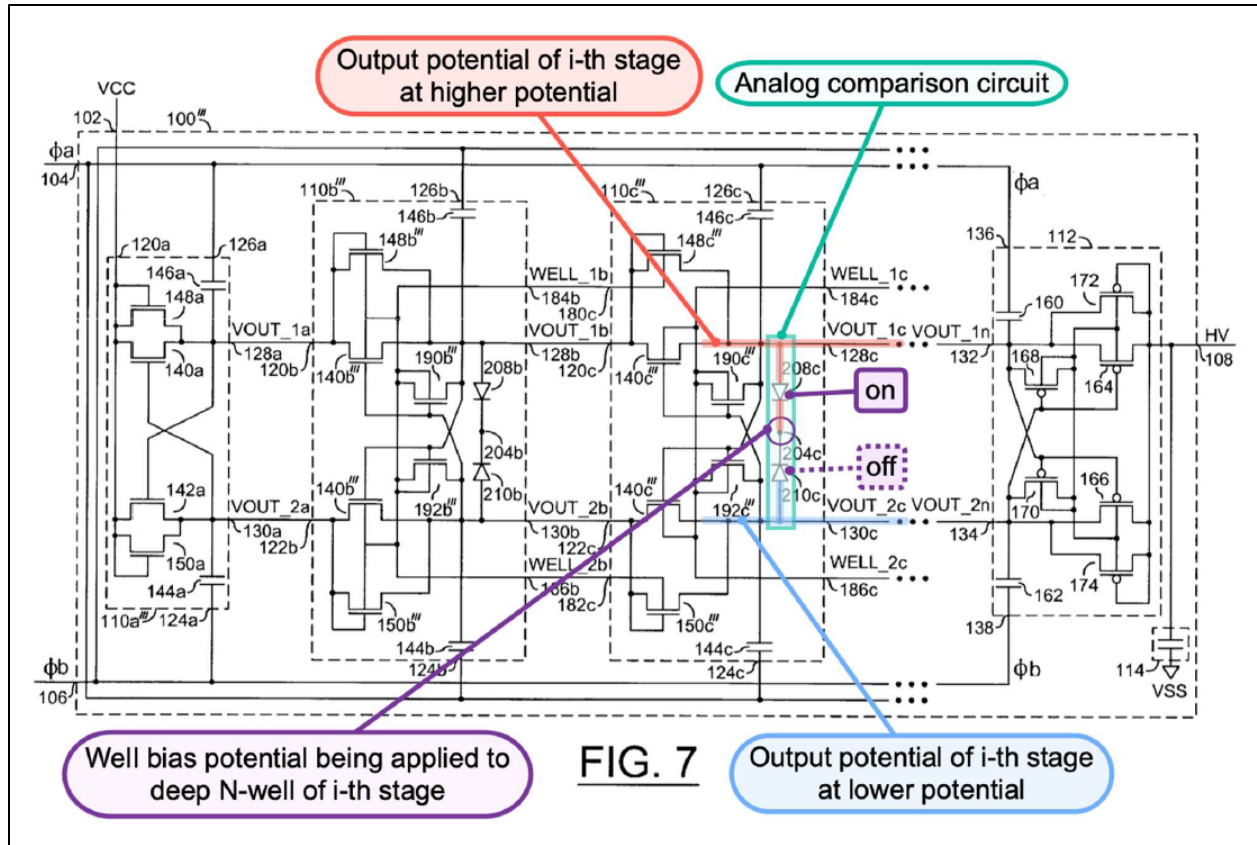
EX1005, Fig. 1C

As shown in Figure 1C, the N-well underlying the PMOS transistors of each stage are not a deep N-well underlying the NMOS transistors. For that, the Petition relies on Figure 3A. *See, e.g.*, Petition at 19. But Fukushima teaches that Figure 3A “is a section view of a semiconductor substrate of a charge pump circuit according to *another* preferred embodiment.” EX1005 at 4:17–19 (emphasis added). The Petition does not even allege that Fukushima discloses using the substrate from this other embodiment in combination with the circuit diagrams of the first embodiment. Petitioner therefore fails to show that Fukushima discloses “all of the limitations of the claims arranged or combined in the same way as recited in the claims,” as required for anticipation. *NetMoneyIN*, 545 F.3d at 1370.

B. Meng Does Not Anticipate Any Challenged Claim, and Ground 2 Therefore Fails

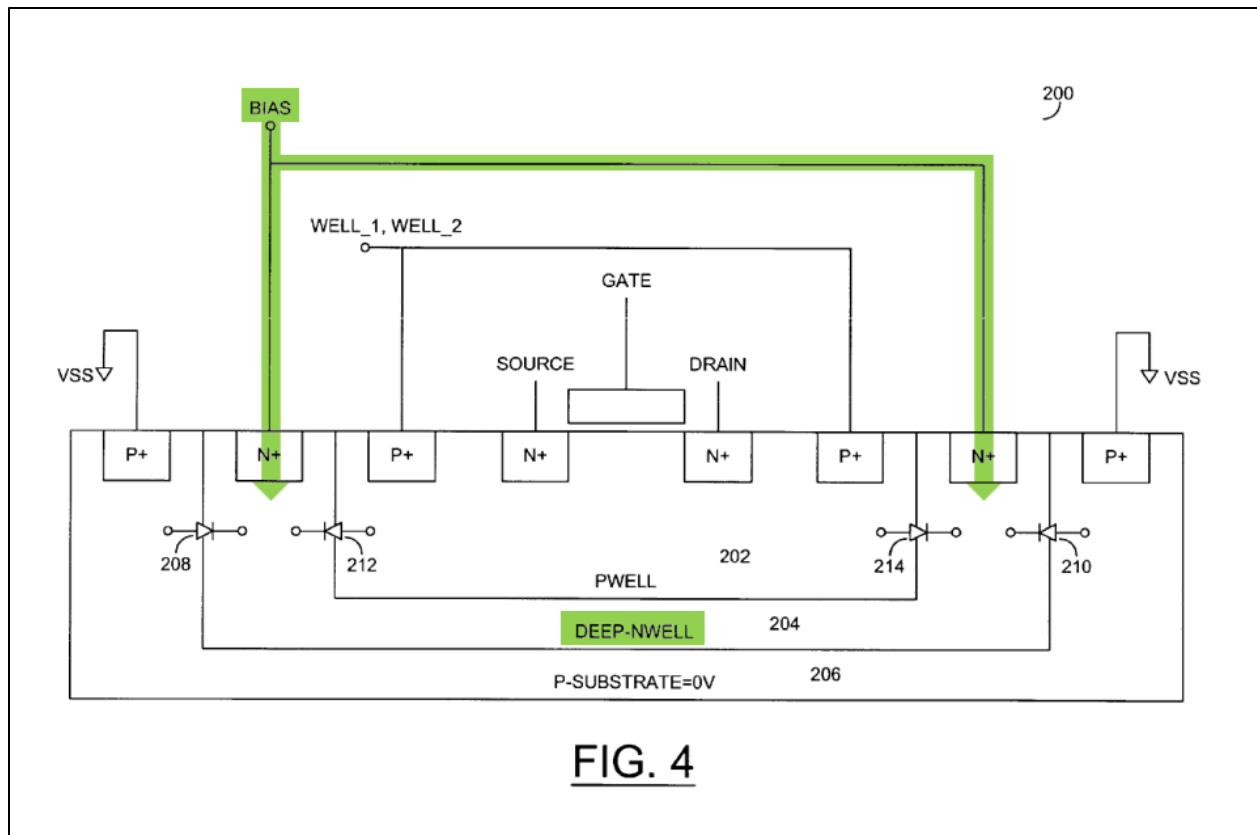
Petitioner's second Ground—asserting anticipation by Meng against claims 1–3, 9, 10, and 14—fails because Meng does not disclose every element of the challenged claims, including at least those reciting the use of *output potentials* of the *booster cells* to bias the *first well region* in both independent claims. Petitioner's anticipation theory rests on a mischaracterization of Meng, which expressly teaches biasing the deep N-well in a manner that contradicts the Petition.

Petitioner relies on the embodiment of Meng's Figure 7 and, more particularly, the annotated portion of that Figure below (reproduced from the Petition) that includes diodes 208c, 210c and node 204c. *See* Petition at 42–44, 55. But Petitioner's arguments ignore Meng's actual description of these structures.



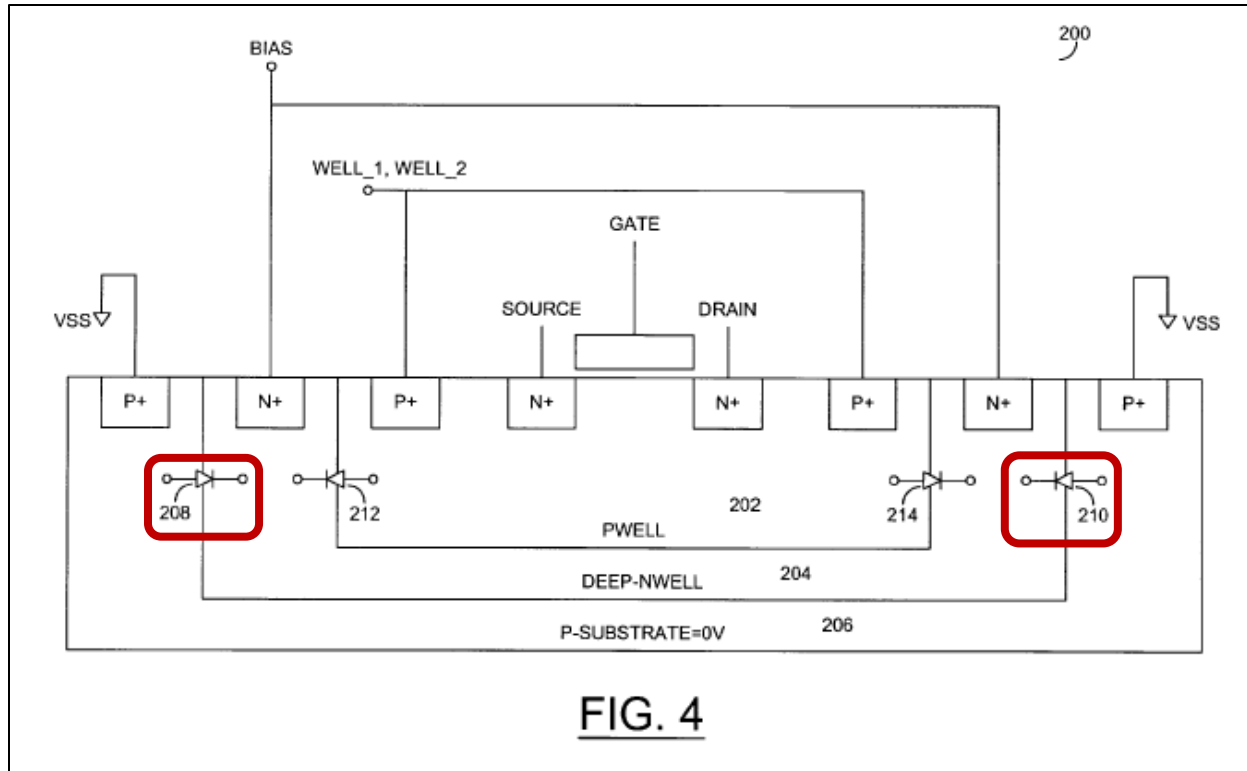
Petition at 43 (annotating EX1006, FIG. 7)

Meng does not disclose that these components operate to bias the deep N-well 204 (the alleged *first well region*) using the alleged *output potentials* (i.e., signals VOUT_1c and VOUT_2c). Rather, the “deep N-well region 204 . . . receives a bias signal” that Meng identifies as “BIAS” in Figure 4 and in the text. EX1006 at 7:8–9, FIG. 4. (This is indicated by the green annotations to Figure 4, below.) Meng further teaches that the “signal BIAS” is greater than the various signals biasing the two P-regions (202, 206). *Id.*, at 7:24–28, 7:29–30, 7:44–47.



EX1006, FIG. 4 (annotated)

Meng's disclosure regarding Figure 4 also applies to the embodiment of Figure 7. In describing the Figure 7 embodiment, Meng states that "diodes 208b–208n[]" and diodes 210b–210n" are "described in more detail in connection with FIG. 4." EX1006 at 8:59–61. In connection with Figure 4, Meng explains that 208 and 210 are the diodes "formed at the junctions between the deep N-well region 204 and the P-substrate region 206," indicated by the red annotations below. *Id.* at 7:11–12. In other words, these diodes are merely an interface between two regions of underlying semiconductor material.



EX1006 FIG. 4 (annotated)

More generally, Meng also does not describe the alleged *output signals* ($VOUT_{1c}$ and $VOUT_{2c}$) being used to bias the deep N-well region 204. Meng discloses that $VOUT_{1c}$ and $VOUT_{2c}$ are each “presented at a [respective] node formed by the connection” of seven different circuit components. EX1006 at 9:17–28. Among these many components, each node is connected to “a P-region terminal of the diode 208 i ” or “a P-region terminal of the diode 210 i .” *Id.* Notably, the “P-region” in question is the *substrate* (206) of the device, which is “connected to the supply ground Vss” or alternatively biased at “0V.” *Id.*, at 7:9–10, 7:29–30, 7:45–47.

Petitioner ignores Meng’s express descriptions of the diodes 208*c*, 210*c* and node (or region) 204*c* in favor of its own speculative interpretation of Figure 7. But, as shown above, the diodes 208*b–n* and 210*b–n* identified by Petitioner as the *analog comparison circuit* are not “NMOS transistors with their drains tied to their gates,” as Petitioner asserts. Petition at 43. The diodes are interfaces between regions of semiconductor material.

Moreover, because 208 and 210 are *diodes* and are not *transistors*, Meng also contradicts Petitioner’s assumption that “V_t” (Meng, Figure 8) is ““the threshold voltage []’ of the diodes . . . 208*i* and 210*i*.” Petition at 46 (quoting EX1006 at 9:47–48) (underline added). Meng refers to voltage “V_t” as “the transistor threshold voltage,” EX1006 at 9:57–58, and describes several elements in Figure 7 as transistors, including 140'''*i*, 142'''*i*, 148'''*i*, 150'''*i*, and 190'''*i*, *id.* at 9:6–8. Meng never suggests that transistor threshold voltage “V_t” applies to diodes 208*i* or 210*i*, nor does Meng describe diodes 208*i* or 210*i* as transistors. Hence, contrary to Petitioner’s suggestion, the alleged relationship between “V_t” and the “DEEP-N WELL REGION 204*i* BIAS” in Meng’s Figure 8 does not teach (nor even suggest) that the bias comes from diodes 208*i* and 210*i* (the alleged comparison circuit). *See* Petition at 46; EX1006, FIG. 8. Rather, Meng teaches that the “BIAS signal” applied to the deep-N well, as depicted in Figure 4 above, could be any “constant positive voltage” within the range provided. EX1006 at 7:19–22.

The Petition therefore fails to identify any evidence linking the alleged *output potential* of the *booster cells* to the “BIAS signal” that Meng expressly discloses applying to the deep-N well. *E.g., id.*, at 7:8–9. The cited passage of the Sechen Declaration does nothing to salvage Petitioner’s theory; Dr. Sechen merely repeats, essentially verbatim, the argument from the Petition without adding any additional facts or analysis. *Compare* EX1003 ¶ 107 *with* Petition at 45–46. Such testimony is entitled to little or no weight and does not support institution. *See, e.g., Xerox*, IPR2022-00624, Paper 9 at 15 (precedential).

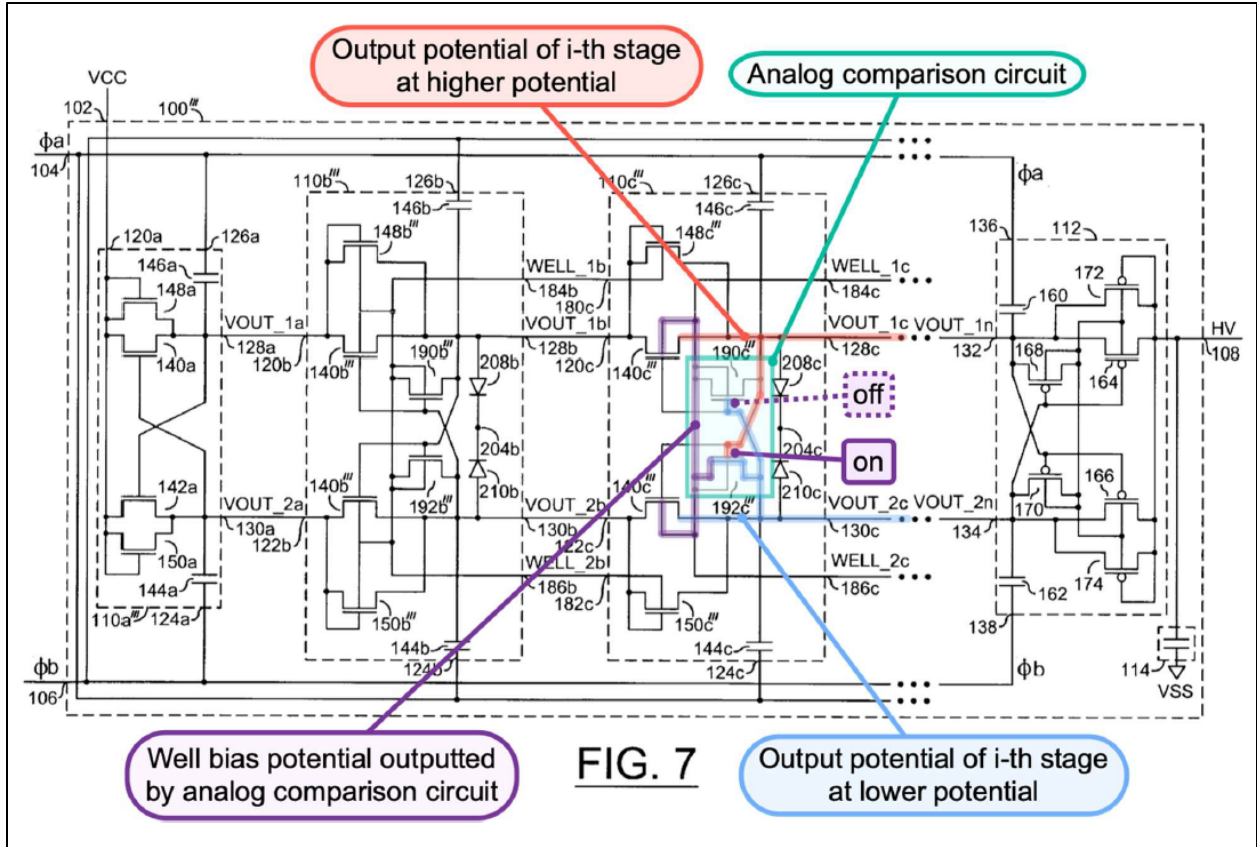
Petitioner therefore fails to show that Meng anticipates either of the independent claims, claims 1 and 14. Because all other challenged claims depend from claim 1, Petitioner’s challenges to those dependent claims necessarily fail as well. The Petition therefore fails to show a reasonable likelihood of prevailing on its Ground asserting that Meng anticipates claims 1–3, 9, 10, and 14.

C. Petitioner Fails to Show that Meng, in view of Park, Renders Obvious the Challenged Claims, and Ground 3 Therefore Fails

Petitioner’s third Ground—asserting that claims 1–12 and 14 would have been obvious—fails because the asserted combination of Meng and Park fares no better than Meng alone. Indeed, for Ground 3, Petitioner does not even allege that Meng teaches or suggests that the alleged *output potentials* of the *booster cells* in the *first* and *second booster cell rows* would be used for the bias potential of the deep N-well (the alleged *first well region* of the claims). Instead, Petitioner relies on Park for

these limitations of the claims, but Park also does not teach the claimed features. Accordingly, these limitations—required by both independent claims—are missing from the cited disclosure of both references. Petitioner therefore fails even to establish a *prima facie* case of obviousness for Ground 3 as to any claim.

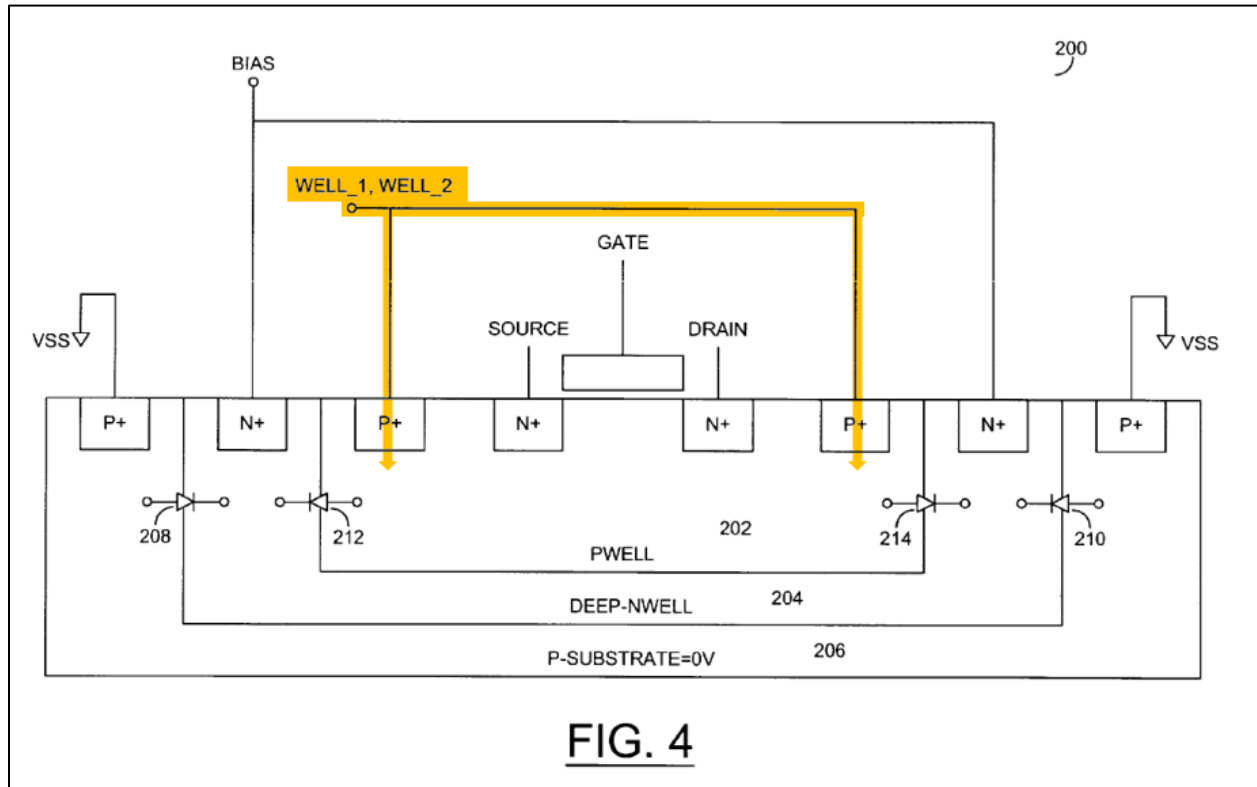
As an initial matter, Petitioner identifies a different set of structures in Meng as the *analog comparison circuit* of the claims in Ground 3 than it did for Ground 2. *Compare* Petition at 69–73 (Ground 3) *with id.* at 42–44 (Ground 2). Neither of these structures applies a well-bias potential to the deep N-well. Petitioner first contends that Meng (in Figure 7) discloses an *analog comparison circuit* that “comprises two cross-coupled NMOS transistors, elements 190'''i and 192'''i.” *Id.*, at 70. This contention is also illustrated by Petitioner’s annotations to Figure 7 (below).



Petition at 70 (annotating EX1006, FIG. 7)

To support its contention that the alleged *analog comparison circuit* outputs a well-bias potential, Petitioner cites Meng as stating: “The ***bias signals*** WELL_1i and WELL_2i may be ***generated by*** the transistors 190'''i and 192'''i [*i.e.*, an ***analog comparison circuit***].” Petition at 71 (quoting EX1006 at 9:9–10) (alteration and emphasis in original). Meng expressly teaches, however, that WELL_1i and WELL_2i are used to bias the ***P-well 202***, not the deep N-well 204, as shown by the orange annotations to Figure 4 (below). *See, e.g.*, EX1006 at 7:15–19, 7:31–36, 9:27–32, FIG. 4. As also shown in Figure 4 (and as explained above for Ground 2), Meng expressly teaches that the deep N-well is biased using the “BIAS” signal,

which “may be a constant positive voltage in the range 0.5V to Vcc.” *Id.*, at 7:20–22; *see also* § VI.B, *supra*. As in Ground 2, Petitioner alleges that the deep N-well is the *first well region* of the claim. *See* Petition at 64 (annotating EX1006, FIG. 4).



EX1006, FIG. 4 (annotated)

Petitioner similarly identifies transistors 190''i and 192''i in Figure 5 as an *analog comparison circuit*. Petition at 72. And, as with the transistors in Figure 7, Petitioner relies on Meng teaching that transistors 190''i and 192''i may generate signals WELL_1i and WELL_2i. *Id.* (citing EX1006 at 8:16–18). Again, Meng teaches that these signals are used to bias the P-well, not the deep N-well.

Accordingly, the output potential of the alleged *analog comparison circuit* is not applied to bias the alleged *first well region*, as recited in claim 1. Indeed, even

Petitioner acknowledges that Meng does not teach applying the well bias potential of this *alleged comparison circuit* to the deep N-well. This is evident from the Petition itself, which asserts that “Meng discloses two analog comparison circuits” and only argues that *one* of them teaches applying a well bias potential to the deep N-well. Petition at 15. Notably, the one that Petitioner refers to is the one cited for Ground 2. *See id.*, at 43–44. And, when addressing limitation 1[e] (which recites this feature), Petitioner relies solely on Park. *Id.*, at 73–78; *see also id.*, at 90–91 (relying on arguments for limitation 1[e] to satisfy corresponding limitation 14[d]).

The combination with Park does not cure Meng’s failure to teach applying the well bias potential of an *analog comparison circuit* to the deep-N well (the alleged “first well region”). Park does not teach an *analog comparison circuit* at all. Nor does it teach using an *output potential of boosting cells* in a *first row* and an *output potential of boosting cells* in a *second row* for any purpose, let alone biasing a deep N-well. Park teaches a single-row boosting circuit. *See* EX1007, FIG. 7. Without a second row, there is nothing for the claimed *analog comparison circuit* to compare. Nor is there any *output potential of boosting cells* in a *second row* to be used for any purpose.

Petitioner relies instead on Park’s disclosure of biasing the “Deep n-well” (Park, Figure 9) using an “input charge pump voltage” from a previous stage. *See* Petition at 73–75. Although this allegedly shows that Park teaches applying some

well-bias potential to the deep N-well, *see* EX1007 at 6:34–40, FIG. 9, Meng already teaches this too. As noted above, Meng describes applying a bias potential (the “BIAS” signal) to deep N-well 204. EX1006 at 7:19–22, FIG. 4. Neither Meng nor Park teaches that the potential being applied to the deep N-well is the well-bias potential of an *analog comparison circuit*. Nor does either reference teach using *output potentials* from both of two rows of *boosting cells* for biasing the deep N-well at all, let alone in the claimed manner. Accordingly, a crucial claim element is missing from both Meng and Park.

Moreover, Petitioner’s proposed motivation for modifying Meng based on Park bears no relationship to the crucial missing limitation. *See* Petition at 57–60. As shown above, Meng and Park both allegedly teach biasing a deep N-well, but they do not teach doing so in the manner claimed. Hence, the respective teachings on this subject (cited by the Petition at 58–59) do not provide any reason “why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*,” as required for obviousness. *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1362 (Fed. Cir. 2019) (quoting *ActiveVideo Networks, Inc. v. Verizon Communc’ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012)) (*italics in original*). Likewise, the more general assertions about the similarities between the references (*see* Petition at 59–60) cannot support a finding of obviousness because they bear no relation to any particular combination of elements.

See ActiveVideo, 694 F.3d at 1328. Petitioner therefore fails to show how or why a POSITA would have arrived at the claimed invention from the combination of Meng and Park.

Accordingly, Petitioner fails to show a reasonable likelihood of prevailing on Ground 3 as to any challenged claim.

VII. CONCLUSION

For at least the reasons stated herein, AMT respectfully requests that the Director deny institution of *inter partes* review in this proceeding.

Dated: December 8, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing was served via email to lead and backup counsel of record for Petitioner as follows:

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24(b)(1) because this brief contains 5,813 words.

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