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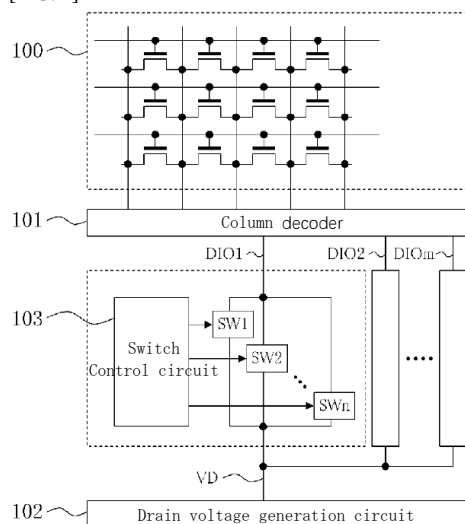
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[Other pages follow]

(54) Title: NONVOLATILE SEMICONDUCTOR MEMORY

(54) Title of invention: Nonvolatile semiconductor memory

[FIG. 1]



101 COLUMN DECODER
103 SWITCH CONTROL CIRCUIT
102 DRAIN VOLTAGE GENERATION CIRCUIT

(57) Abstract: When write is performed simultaneously into a plurality of nonvolatile memory cells in a memory cell array (100), the bit lines of the nonvolatile memory cells are connected to M (M is an integer not smaller than 2) data lines (DIO1 to DIOm) by a column address signal. N (N is an integer not smaller than 1) switches (SW1 to SWn) and a switch control circuit (103) for controlling the N switches are arranged for each of the data lines. M switch control circuits control M × N switches so as to change the voltage level of the drain voltage applied to the memory cell bit lines or the period of the drain voltage application for each of the memory cells.

(57) Summary: When simultaneously writing to a plurality of nonvolatile memory cells in the memory cell array (100), the bit lines of the plurality of nonvolatile memory cells are connected to M data lines (DIO1 to DIOm) (where M is an integer of 2 or more) by a column address signal. Then, for each of the data lines, N switches (SW1 to SWn) (where N is an integer of 1 or more) and a switch control circuit (103) for controlling the N switches are provided; the M switch control circuit controls a total of M×N switches, and thereby vary, for each memory cell, in terms of either the voltage level of the drain voltage applied to the bit lines of the plurality of memory cells or the duration for which drain voltage is applied.



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CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN,
TD, TG).

Attached Publication Documentation:

— International Search Report (Article 21 (3) of the
Treaty)

Specification

Title of invention: Nonvolatile Semiconductor Memory

Technical field

[0001] The present invention relates to nonvolatile semiconductor memory and, in particular, to a technique that suppresses variations in write speed when simultaneously writing a plurality of nonvolatile memory cells at the same threshold level.

Background art

[0002] In general, nonvolatile semiconductor memory, such as flash memory, has memory cells each consisting of a gate electrode connected to a word line, a drain connected to a bit line, a source connected to a source line, and a floating gate or charge trap layer; a memory cell array is provided in which a plurality of these memory cells are arranged in a matrix.

[0003] For example, in nonvolatile semiconductor memory having a trap layer, a charge (electrons or holes) is trapped by injection into a discretized trap layer (a SiN film or a transition region at the SiN film/top SiO₂ film interface) present within an insulating film (SiO₂) between the channel region of the memory cell and the gate electrode; data "0" or "1" is determined based on the threshold level of such memory cell, and information is stored accordingly. Below, electron injection is referred to as writing, and an explanation is given on the principle of writing.

[0004] In FIG. 9, 600 is a semiconductor substrate made of P-type silicon, 601 is a P-type channel region formed on the semiconductor substrate 600, 602 is a first impurity region (e.g., a drain) formed from N-type semiconductor on one side of the channel region 601 on the semiconductor substrate 600, 603 is a second impurity region (e.g., a source) formed of N-type semiconductor on the other side of the channel region 601 on the semiconductor substrate 600, 604 is a bottom insulating film made of silicon oxide formed on the semiconductor substrate 600, 605 is a trap layer made of silicon oxynitride formed on the bottom insulating film 604, 606 is a top insulating film made of silicon oxide formed on the trap layer 605, and 607 is a gate electrode made of N-type polysilicon formed on the top insulating film 606.

[0005] When writing, approximately 9 V is applied to the gate electrode 607, approximately 5 V is applied to the first impurity region (drain) 602, 0 V is applied to the second impurity region (source) 603, and 0 V is applied to the semiconductor substrate 600, respectively. This causes a portion of the electrons heading from the second impurity region 603 to the first impurity region 602 to become heated due to the high electric field in the vicinity of the first impurity region 602, and to be injected locally into the trap layer 605 in the vicinity of the first impurity region 602, causing the threshold level of the memory cell to increase.

[0006] In the write operation for nonvolatile semiconductor memory, it is common practice to shorten the write time by simultaneously applying the aforementioned write voltage to such plurality of memory cells, such as on a byte or word basis, and treating them as a single unit for writing.

[0007] In addition, in nonvolatile semiconductor memory having a trap layer, by reversing the voltages applied to the first impurity region 602 and the second impurity region 603, applying 0V to the first impurity region 602 and approximately 5 V to the second impurity region 603, electrons can be locally injected into the trap layer 605 near the second impurity region 603, making it possible to store two bits of data in a single memory cell.

[0008] However, in recent years, in conjunction with the storage capacity of nonvolatile semiconductor memory having increased, the area of memory cell arrays has also grown, resulting in longer bit lines being formed within the memory cell array. Therefore, when writing, there is a problem in that due to a voltage drop caused by the resistance of the bit lines, the drain voltage varies depending on the location of the memory cells within the memory cell array, resulting in variations in write speed.

[0009] In addition, in nonvolatile semiconductor memory that has a trap layer and which is capable of storing two bits of data in a single memory cell, it is known that the storage state of the first bit affects the write speed of the second bit, which is a factor that contributes to the variation in write speed.

[0010] In order to address these problems, according to one prior art, the level of bit line voltage supplied to the bit line in the memory cell array at the time of writing is varied according to the write address, thereby suppressing the variations in write speed (see Patent Reference 1).

Prior art documents

Patent documents

[0011] Patent document 1: Japanese Unexamined Patent Application Publication 2003-109389

Summary of the invention

Problem to be Solved by the Invention

[0012] However, in the above-described prior art, when a plurality of memory cells are written simultaneously, the write conditions (drain voltage, duration of drain voltage supply) are set commonly. Therefore, variations in write speed between the plurality of memory cells that are being written simultaneously cannot be suppressed, leading to a deterioration in memory cell reliability. In addition, as the write time depends on the memory cell with the slowest write speed, variations in the write speed result in an increase in the overall write time.

Means for Solving the Problem

[0013] According to the present invention, when writing a plurality of nonvolatile memory cells simultaneously, the bit lines of the plurality of nonvolatile memory cells are connected to M data lines (where M is an integer of 2 or more) by a column address signal. In addition, for each of the data lines, N switches (where N is an integer of 1 or more) and a switch control circuit for controlling the N switches are provided; the M switch control circuits control a total of M×N switches, and thereby vary, for each memory cell, either the voltage level of the drain voltage applied to the bit lines of the plurality of memory cells or the duration for which the drain voltage is applied.

Effect of the Invention

[0014] In the nonvolatile semiconductor memory of the present invention, variations in write speed between memory cells when writing a plurality of nonvolatile memory cells simultaneously can be suppressed, variations in post-write threshold levels can

be reduced so as to improve memory cell reliability, and in addition, an increase in write time due to variations in write speed can be suppressed.

Brief Description of the Drawings

[0015] [FIG. 1] A block diagram illustrating a first configuration example of the nonvolatile semiconductor memory according to the present invention.

[FIG. 2] A diagram illustrating a first configuration example of a switch circuit and a switch control circuit according to the present invention.

[FIG. 3] A diagram illustrating a switch control method in a first configuration example of a switch circuit and switch control circuit according to the present invention.

[FIG. 4] A diagram illustrating a second configuration example of a switch circuit and a switch control circuit according to the present invention.

[FIG. 5] A diagram illustrating a switch control method in a second configuration example of a switch circuit and switch control circuit according to the present invention.

[FIG. 6] A diagram illustrating a third configuration example of a switch circuit and a switch control circuit according to the present invention.

[FIG. 7] A diagram illustrating a switch control method in a third configuration example of a switch circuit and switch control circuit according to the present invention.

[FIG. 8] A block diagram illustrating a second configuration example of the nonvolatile semiconductor memory according to the present invention.

[FIG. 9] A cross-sectional view showing the memory cell structure of a conventional nonvolatile semiconductor memory.

Modes for carrying out the invention

[0016] Hereinafter, embodiments of the present invention configured to write a plurality of nonvolatile memory cells simultaneously will be described with reference to the drawings.

[0017] FIG. 1 illustrates an example configuration of a nonvolatile semiconductor memory according to the present invention. 100 is a memory cell array consisting of a plurality of memory cells, 101 is a column decoder that connects a plurality of bit lines to M data lines DIO1 to DIO_M, where M is smaller than the number of bit lines, based on

a column address signal, and 102 is a drain voltage generation circuit that supplies a drain voltage to the bit lines.

[0018] For each data line, the first terminal of each of the N switches SW1 to SWn are commonly connected, and a drain voltage supply line VD, which is the output of the drain voltage generation circuit 102, is commonly connected to the second terminal of each of the N switches SW1 to SWn. In addition, a switch control circuit 103 is provided for each data line to control the N switches SW1 to SWn.

[0019] The M switch control circuit 103 controls M x N switches, and vary, for each data line DIO1 to DIOm, either the drain voltage level supplied or the duration for which the drain voltage is supplied. As a result of this, the write speed of the memory cells connected to M data lines DIO1 to DIOm can be varied for each memory cell, and allows for the write speed variation when writing a plurality of memory cells simultaneously to be suppressed.

[0020] FIG. 2 illustrates a first example configuration of a switch circuit and switch control circuit that varies the voltage level of the drain voltage supplied to the data line. In the switch circuit 200, the first terminals of the two P-type transistors P1 and P2 are commonly connected to the data line DIO, and the second terminals of the P-type transistors P1 and P2 are commonly connected to the drain voltage supply line VD. The switch control circuit 201 receives a data input signal DIN as well as switch control input signals SWIN1 and SWIN2, and outputs switch control output signals SWOUT1 and SWOUT2. The switch control output signals SWOUT1 and SWOUT2 are connected to the gate terminals of the P-type transistors P1 and P2 in the switch circuit 200, respectively.

[0021] FIG. 3 shows the relationship between the data input signal DIN, the switch control input signals SWIN1, SWIN2, and the switch control output signals SWOUT1, SWOUT2 in the switch control circuit 201. The “L” in FIG. 3 represents 0 V and the “H” represents the same level as the drain voltage supply line VD. When SWOUT1 is “L”, the P-type transistor P1 in the switch circuit 200 is turned on, and when SWOUT2 is “L”, the P-type transistor P2 in the switch circuit 200 is turned on. The transistor resistance between the data line DIO and the drain voltage supply line VD varies

depending on the combination in which the P-type transistors P1 and P2 in the switch circuit 200 are turned on, and the amount of voltage drop caused by the transistor resistance changes accordingly. In this way, the voltage level supplied to the data line DIO can be varied depending on the combination by which the P-type transistors P1 and P2 in the switch circuit 200 are turned on.

[0022] FIG. 4 illustrates a second example configuration of a switch circuit and switch control circuit that varies the voltage level of the drain voltage supplied to the data line. In the switch circuit 300, the first terminals of the P-type transistor P1 and the N-type transistor N1 are commonly connected to the data line DIO, and the second terminals of the P-type transistor P1 and the N-type transistor N1 are commonly connected to the drain voltage supply line VD. The switch control circuit 301 receives a data input signal DIN as well as switch control input signal SWIN, and outputs switch control output signals SWOUT1 and SWOUT2. The switch control output signals SWOUT1 and SWOUT2 are connected to the gate terminals of the P-type transistor P1 and the N-type transistor N1 in the switch circuit 300, respectively.

[0023] FIG. 5 shows the relationship between the data input signal DIN, the switch control input signal SWIN, and the switch control output signals SWOUT1, SWOUT2 in the switch control circuit 301. The “L” in FIG. 5 represents 0 V and the “H” represents the same level as the drain voltage supply line VD. When SWOUT1 is “L”, the P-type transistor P1 is turned on, and when SWOUT2 is “L”, the N-type transistor N1 in the N-type transistor is turned on. When the P-type transistor P1 is turned on, the level of the drain voltage supply line VD is supplied to the data line DIO as is, whereas when the N-type transistor N1 is turned on, a voltage level that is lower by exactly the threshold voltage V_{tn} of the N-type transistor N1 than the gate voltage (the level of the drain voltage supply line VD here) is supplied. In this way, the voltage level supplied to the data line DIO can be varied by selectively turning on either the P-type transistor P1 or the N-type transistor N1.

[0024] FIG. 4 illustrates a second example configuration of a switch circuit and switch

control circuit that varies the duration period of the drain voltage supplied to the data line. In the switch circuit 400, the first terminal of the P-type transistor P1 is connected to the data line DIO, and the second terminal of the P-type transistor P1 is connected to the drain voltage supply line VD. The switch control circuit 401 receives a data input signal DIN as well as switch control input signal SWIN, and outputs switch control output signal SWOUT. The switch control output signal SWOUT is connected to the gate terminal of the P-type transistor P1 in the switch circuit 400. The switch control circuit 401 comprises a delay circuit 402 consisting of a resistive element R and a capacitor element C with the ground potential as GND, and can switch the “L” period of the switch control output signal SWOUT in accordance with the switch control input signal SWIN.

[0025] FIG. 7 shows the relationship between the data input signal DIN, the switch control input signal SWIN, and the switch control output signal SWOUT in the switch control circuit 401. The “L” in FIG. 7 represents 0 V and the “H” represents the same level as the drain voltage supply line VD. During the period that the switch control output signal SWOUT is “L”, the P-type transistor P1 is turned on, and the drain voltage is supplied to the data line DIO. In this way, the duration for which voltage is supplied to the data line DIO can be varied by the switch control input signal SWIN.

[0026] FIG. 8 illustrates another example configuration of a nonvolatile semiconductor memory according to the present invention. 500 is a memory cell array consisting of a plurality of memory cells, 501 is a column decoder that connects a plurality of bit lines to M data lines DIO1 to DIOm, with M being smaller than the number of bit lines, based on a column address signal, and 505 is a read circuit for reading data from the memory cell array 500, which receives the M data lines DIO1 to DIOm as inputs and is composed of components such as sense amplifiers, which are not shown in the FIG. 502 is a drain voltage generation circuit that supplies a drain voltage to the bit lines. The memory cell array 500 is composed of a memory cell having a trap layer as shown in FIG. 9, and allows for the storage of two bits of data in a single memory cell.

[0027] For each data line, the first terminal of each of the N switches SW1 to SWn are

commonly connected, and a drain voltage supply line VD, which is the output of the drain voltage generation circuit 502, is commonly connected to the second terminal of each of the N switches SW1 to SWn. In addition, a switch control circuit 503 is provided for each data line to control the N switches SW1 to SWn.

[0028] In addition, a state storage circuit 504 is provided in order to store the storage state (“0” or “1”) of the memory cell as read by the read circuit 505. The state storage circuit 504 outputs state output signals CB1 to CBm in accordance with the stored state of the stored memory cells, and the state output signals CB1 to CBm are connected to M switch control circuits 503.

[0029] Prior to writing the first bit of the memory cell connected to the M data lines DIO1 to DIOm, the storage state of the second bit of the memory cells is read in advance by the read circuit 505 and the read result is stored in the state storage circuit 504. When the first bit of the memory cells is written, the state storage circuit 504 outputs state output signals CB1 to CBm in accordance with the stored storage states, and based on these state output signals CB1 to CBm, either the voltage level supplied to each of the M data lines DIO1 to DIOm or the duration for which the voltage is supplied is varied for each data line. In this way, the write speed of the first bit of the memory cells connected to the M data lines DIO1 to DIOm can be varied for each memory cell in accordance with the storage state of the second bit of the memory cell, allowing for the write speed variation when writing a plurality of memory cells simultaneously to be suppressed.

[0030] In addition, as a modification to the configuration example shown in FIG. 8, the threshold level state of the memory cells to be written is read in advance by the read circuit 505, prior to writing to the memory cell connected to the M data lines DIO1 to DIOm, and the read result is stored in the state storage circuit 504. When the memory cells are written, the state storage circuit 504 outputs state output signals CB1 to CBm in accordance with the stored threshold level states, and based on these state output signals CB1 to CBm, either the voltage level supplied to each of the M data lines DIO1 to DIOm or the duration for which the voltage is supplied is varied for each data line. In this way, the write speed of the memory cells connected to the M data lines DIO1

to DIOm can be varied for each memory cell in accordance with the threshold level state of the memory cell to be written, allowing for the write speed variation when writing a plurality of memory cells simultaneously to be suppressed.

[0031] Although the above embodiments have described cases in which one or two switches are connected to one data line, the present invention is also applicable to configurations in which three or more switches are provided. In addition, although the above description of a nonvolatile semiconductor memory having a trap layer has been given for a case in which each memory cell stores two bits, the present invention is also applicable to configurations with memory cells capable of writing by reversing the voltage relationship between the first and second impurity regions, even when storing three or more bits per memory cell.

Industrial applicability

[0032] As explained above, the nonvolatile semiconductor memory according to the present invention can improve memory cell reliability by suppressing variations in write speed between memory cells, and can also suppress increases in write time caused by such variations in write speed. In particular, it is useful as a nonvolatile semiconductor memory having a trap layer and which is capable of storing a plurality of bits in a single memory cell.

Explanation of References

[0033] 100, 500 Memory cell arrays
101, 501 Column decoders
102, 502 Drain voltage generation circuits
103, 503 Switch control circuits
200, 300, 400 Switch circuits
201, 301, 401 Switch control circuits
402 Delay circuit
504 State storage circuit
505 Read circuit
600 Semiconductor substrate
601 Channel area

602 First impurity region (drain)
603 Second impurity region (source)
604 Bottom insulation film
605 Trap layer
606 Top insulation film
607 Gate electrode
C Capacitor element
CB1 - CBm State output signal
DIN Data entry signal
DIO, DIO1 - DIOm Data lines
GND Ground potential
N1 N-type transistor
P1, P2 P-type transistors
R Resistive element
SW1 - SWn Switches
SWIN, SWIN1, SWIN2 Switch control input signals
SWOUT, SWOUT1, SWOUT2 Switch control output signals
VD Drain voltage supply line

Scope of Patent Claims

[Claim 1] A nonvolatile semiconductor memory capable of simultaneously writing a plurality of nonvolatile memory cells through a plurality of bit lines, with the memory comprising:

M data lines (where M is an integer of 2 or more), which are fewer in number than the number of bit lines and are connected to the plurality of bit lines in accordance with the column address signal;

a drain voltage generation circuit configured to generate a voltage that serves as the source of drain voltage for each of the plurality of nonvolatile memory cells;

a drain voltage supply line connected to the output of the drain voltage generation circuit;

M switch circuits and M switch control circuits interposed between the M data lines and the drain voltage supply line;

wherein each of the M switch circuits has N switches (where N is an integer of 1 or more), and

each of the M×N switches has a first terminal which is commonly connected to one corresponding data line out of the M data lines, and a second terminal that is commonly connected to the drain voltage supply line;

the drain voltage supply line is connected to the M data lines via the M×N switches, and the M×N switches are controlled by the M switch control circuits.

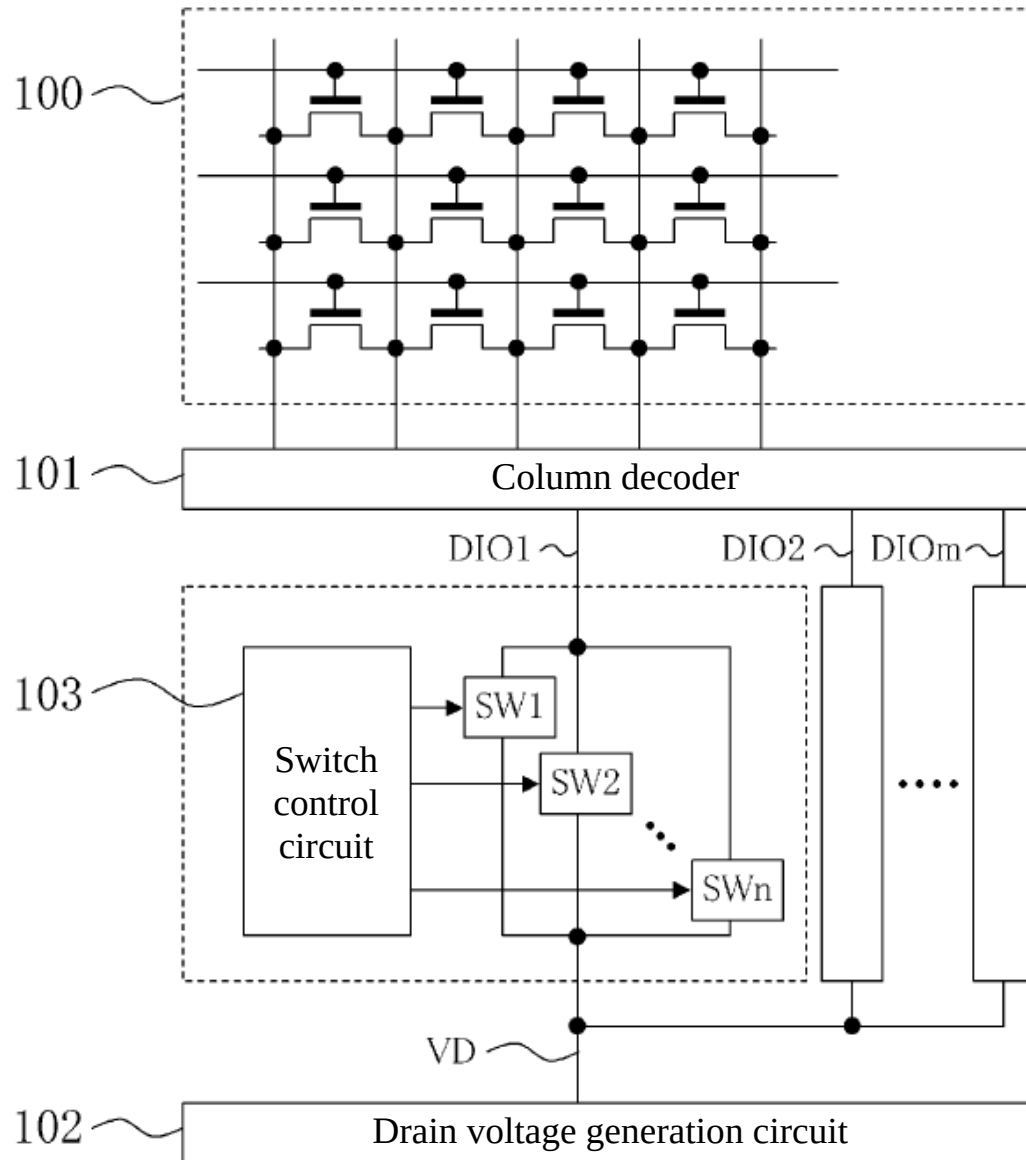
[Claim 2] The nonvolatile semiconductor memory according to claim 1, wherein each of the N switches included in any one of the M switch circuits are composed of one-conductivity-type transistors connected in parallel with one another,

and when drain voltage is to be supplied to the corresponding one data line out of the M data lines, at least one of the N transistors is turned on through the control of the corresponding switch control circuit.

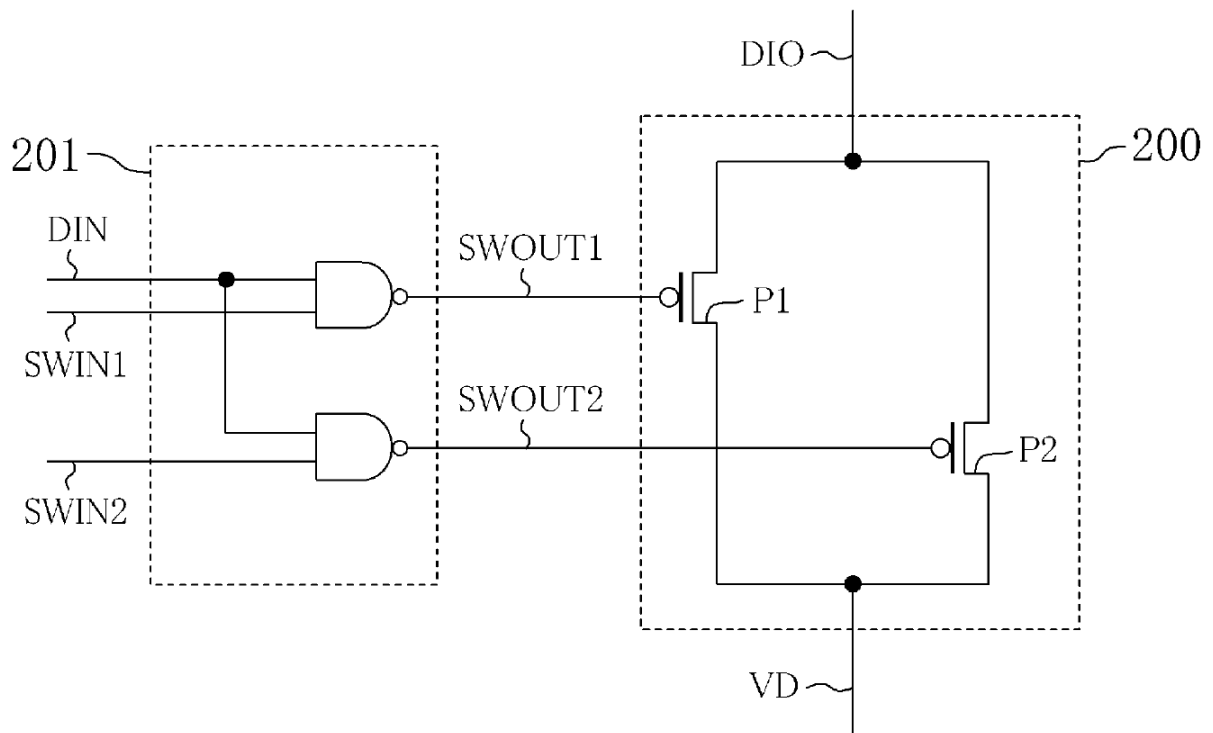
- [Claim 3] The nonvolatile semiconductor memory according to claim 1, wherein each of the N switches included in any one of the M switch circuits are composed of P-type and N-type transistors connected in parallel, and when drain voltage is to be supplied to the corresponding one data line out of the M data lines, either the P-type transistor or the N-type transistor is turned on through the control of the corresponding switch control circuit.
- [Claim 4] The nonvolatile semiconductor memory according to claim 1, wherein the M switch control circuits are capable of controlling, for each of the M data lines, a combination in which the N switches connected to the corresponding one out of the M data lines are turned on.
- [Claim 5] The nonvolatile semiconductor memory according to claim 1, wherein the M switch control circuits are capable of controlling, for each of the M data lines, the period during which the N switches connected to the corresponding one out of the M data lines are turned on.
- [Claim 6] The nonvolatile semiconductor memory according to claim 1, wherein a read circuit that receives the M data lines as inputs, and a state storage circuit to which M read signals output from the read circuit are input, wherein the M switch circuits are controlled in accordance with the M state output signals that are output from the state storage circuit.
- [Claim 7] The nonvolatile semiconductor memory according to claim 6, wherein each of the plurality of nonvolatile memory cells is capable of storing multi-bit data that can be written by reversing the source drain voltage relationship, and during writing of a first bit using source drain voltage applied in one direction, the storage state of a second bit, which is written by applying source drain voltage in the opposite direction, is read, the read storage state is stored in the state storage circuit, and the control method of the M switch control circuits is changed in accordance with the storage state stored to the state storage circuit.

[Claim 8] The nonvolatile semiconductor memory according to claim 6, wherein
 during writing of the plurality of non-volatile memory cells, the threshold
 level states of the memory cells to be written are read, the read threshold level
 states are stored to the state storage circuit,
 and the control method of the M switch control circuits is changed in
 accordance with the threshold level state stored to the state storage circuit.

[FIG. 1]



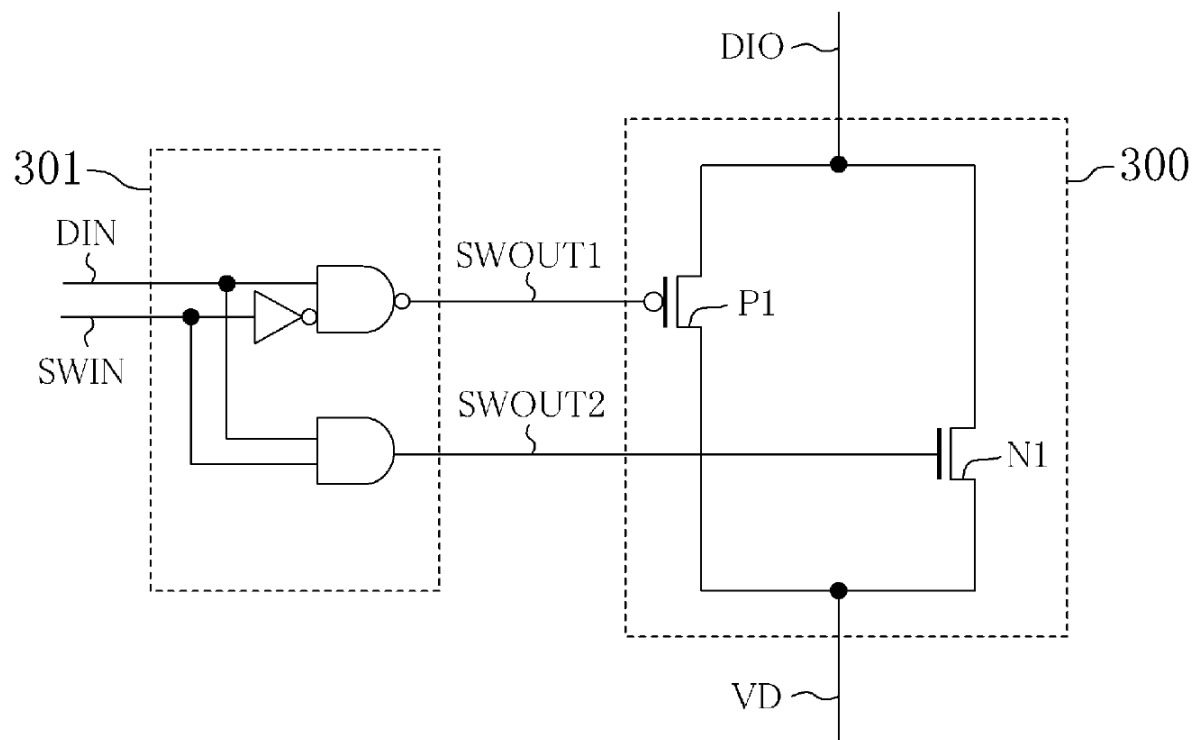
[FIG. 2]



[FIG. 3]

DIN	SWIN1	SWIN2	SWOUT1	SWOUT2	Transistor that is turned on
L	—	—	H	H	None
H	L	L	H	H	None
H	H	L	L	H	P 1
H	L	H	H	L	P 2
H	H	H	L	L	P 1 、 P 2

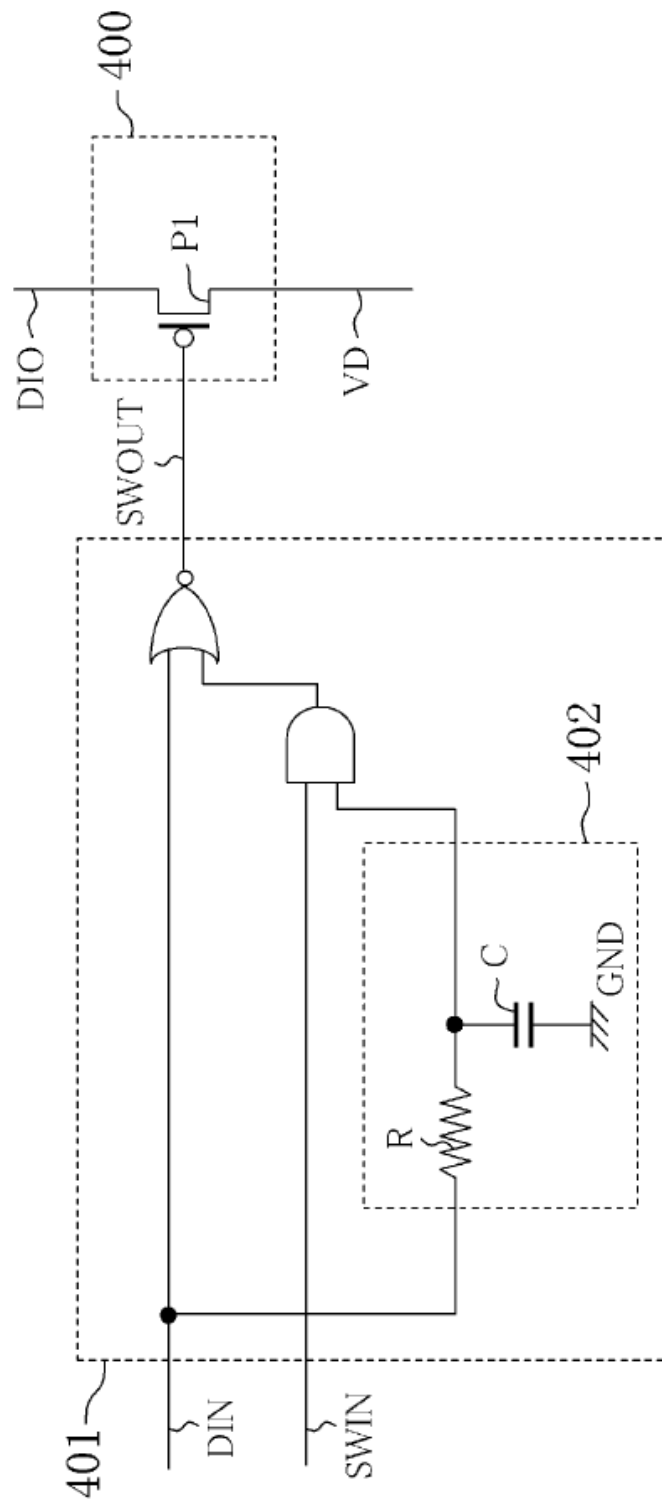
[FIG. 4]



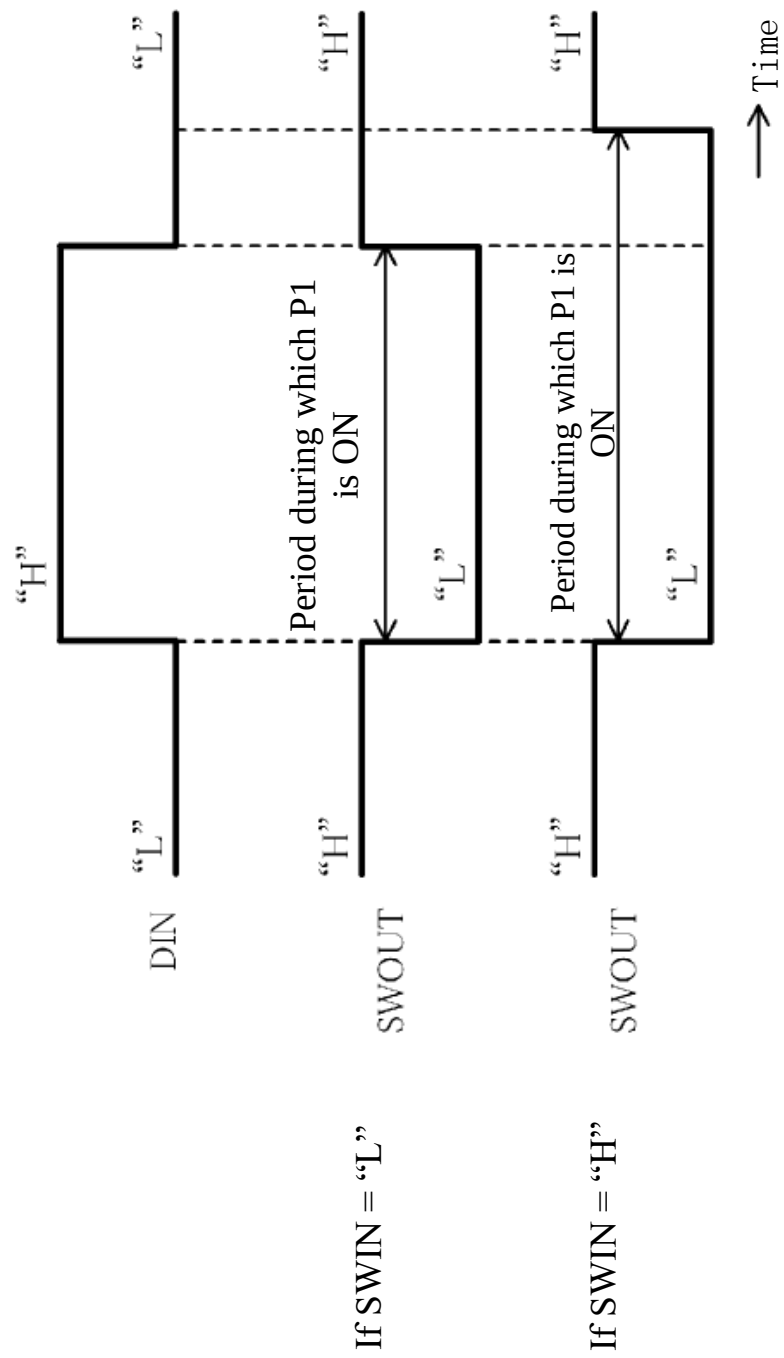
[FIG. 5]

DIN	SWIN	SWOUT1	SWOUT2	Transistor that is turned on
L	—	H	L	None
H	L	L	L	P 1
H	H	H	H	N 1

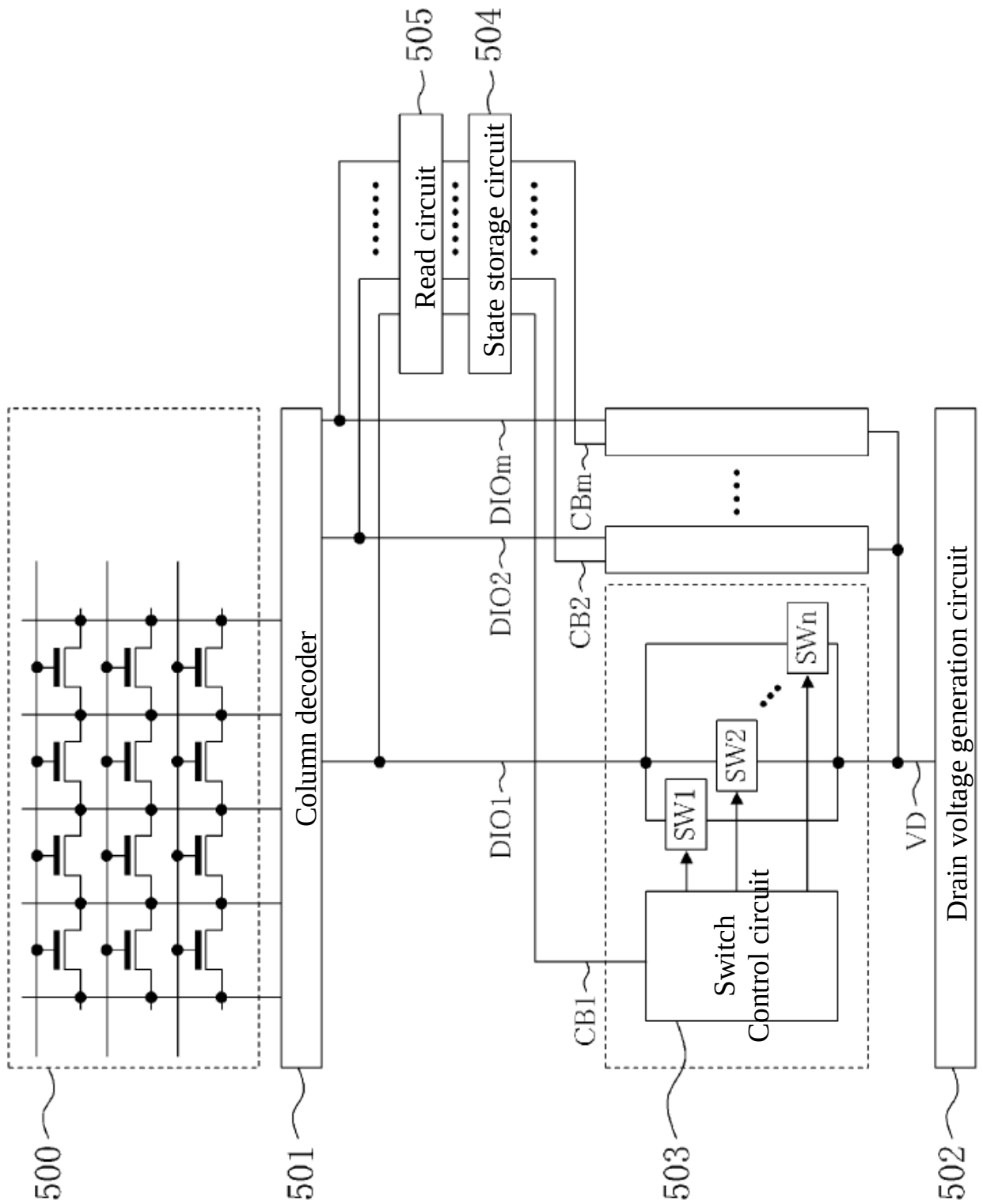
[FIG. 6]



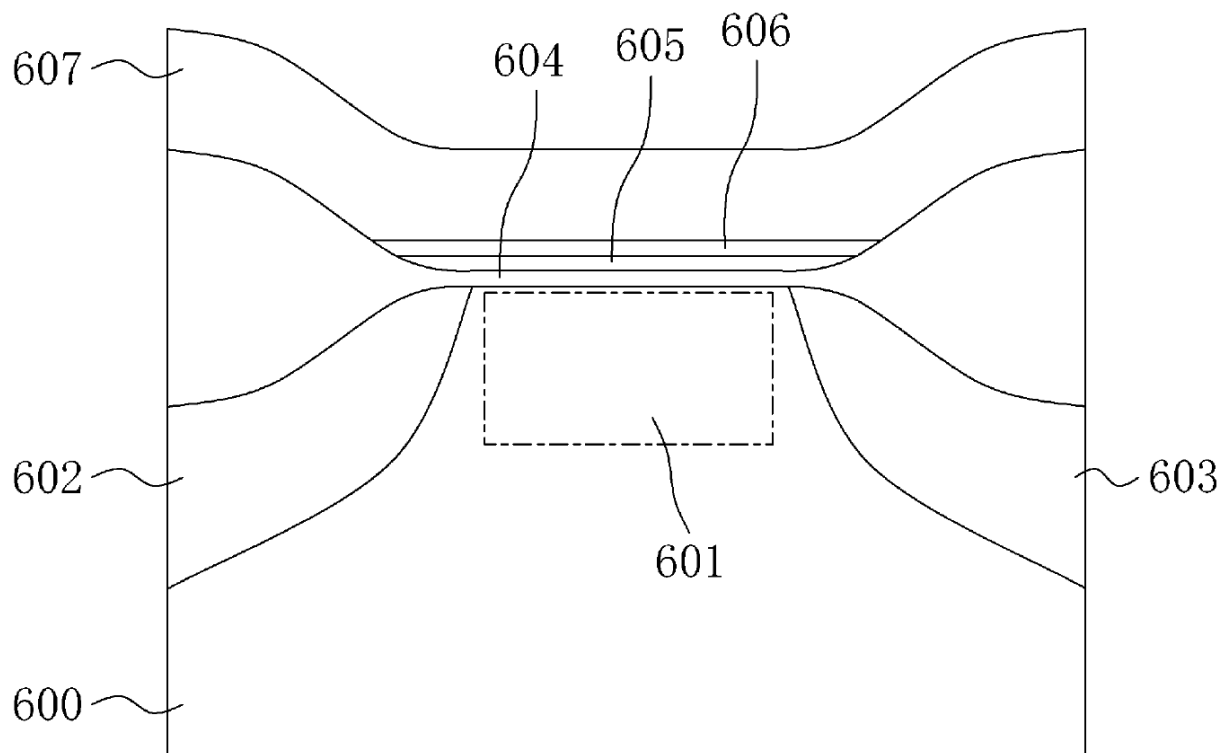
[FIG. 7]



[FIG. 8]



[FIG. 9]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/004737

A. CLASSIFICATION OF SUBJECT MATTER

G11C16/06(2006.01)i, G11C16/02(2006.01)i, G11C16/04(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C16/06, G11C16/02, G11C16/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2009

Kokai Jitsuyo Shinan Koho 1971-2009 Toroku Jitsuyo Shinan Koho 1994-2009

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 06-150670 A (Hitachi, Ltd., Hitachi Tohbu Semiconductor, Ltd.), 31 May 1994 (31.05.1994), paragraphs [0008] to [0045]; fig. 1 to 3 (Family: none)	1, 2, 4-8 3
Y	WO 2002/097821 A1 (Fujitsu Ltd.), 05 December 2002 (05.12.2002), page 3, line 15 to page 8, line 7; fig. 1 to 4 & US 2004/0100825 A1	1, 2, 4-8
Y	JP 2004-273096 A (Hynix Semiconductor Inc.), 30 September 2004 (30.09.2004), paragraphs [0008] to [0009]; fig. 1 & US 2004/0174745 A1 & DE 10361719 A1 & KR 2004-0079464 A & TW 239011 B	1, 2, 4-8

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search
20 October, 2009 (20.10.09)Date of mailing of the international search report
02 November, 2009 (02.11.09)Name and mailing address of the ISA/
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Authorized officer

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2009/004737

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 05-062484 A (Mitsubishi Electric Corp.), 12 March 1993 (12.03.1993), paragraphs [0041] to [0043]; fig. 1 to 3 (Family: none)	5
Y	JP 2003-346484 A (Mitsubishi Electric Corp.), 05 December 2003 (05.12.2003), paragraphs [0168] to [0178]; fig. 15 & US 2003/0218897 A1 & CN 1459863 A & TW 575879 B	6-8

A. Classification of the Field to Which the Invention Belongs (International Patent Classification (IPC)) Int.Cl.G11C16/06(01.2006)i, G11C16/02(01.2006)i, G11C16/04(01.2006)i			
B. Areas Investigated			
Minimal Materials Investigated (International Patent Classification (IPC)) Int.Cl.G11C16/06, G11C16/02, G11C16/04			
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Japanese Unexamined Utility Model Application Publication 1922-1996 Japanese Unexamined Utility Model Application Publication 1971-2009 Japanese Unexamined Utility Model Application Publication 1996-2009 Japanese Registered Utility Model Application Publication 1994-2009			
Electronic data bases consulted during the international investigation (name of database and search terms used)			
C. Literature Considered to be Relevant			
Cited Literature Category*	Title of the cited literature and, if relevant, indication of the relevant passages	Relevant to claim No.	
Y	JP 06-150670 A(Hitachi, Ltd., Hitachi Tobu Semiconductor K.K)	1,2,4-8	
A	05.31.1994, paragraph [0008]—[0045], FIGs. 1 — 3 (without family)	3	
Y	WO 2002/097821 A1 (Fujitsu Corporation) 12.05.2002, p. 3, p. 15-8, line 7, FIGs. 1-4 & US 2004/0100825 A1	1,2,4-8	
Y	JP 2004-273096 A (Hynix Semiconductor Inc.) 09.30.2004, paragraphs [0008]—[0009], Figure 1,	1,2,4-8	
Further cited literature are listed in the continuation of Box ☒ C. ☐ See patent family attachment.			
* Cited literature category "A" Literature defining the general state of the art which is not considered to be of particular relevance "E" Earlier application or patent but published on or after the international filing date "L" Literature which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" Literature referring to an oral disclosure, use, exhibition or other means "P" Literature published prior to the international filing date but later than the priority date claimed		"T" Literature published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" Literature of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" Literature of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more such documents, such combination being obvious to a person skilled in the art "&" Same patent family literature	
Date of actual completion of the international search 20.10.2009		Date of mailing of the international search report 02.11.2009	
Name and mailing address of the ISA Japan Patent Office (ISA/JP) Postal code 100-8915 3-4-3 Kasumigaseki, Chiyoda-ku, Tokyo		Patent Office Examiner (Authorized officer) Takeshi Toyama Phone 03—3581—1101	5N 3982 Extension 3585

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Cited Literature Category*	Title of the cited literature and, if relevant, indication of the relevant passages	Relevant to claim No.
	& US 2004/0174745 A1 & DE 10361719 A1 & KR 2004-0079464 A & TW 239011 B	
Y	JP 05-062484 A (Mitsubishi Electric Corporation) March 12, 1993, Paragraphs [0041]—[0043], FIGs. 1-3 (without family)	5
Y	JP 2003-346484 A (Mitsubishi Electric Corporation) 12.05.2003, Paragraphs [0168]—[0178], FIG. 15, & US 2003/0218897 A1 & CN 1459863 A & TW 575879 B	6-8

I, Simon Edmunds, hereby certify that I am competent to translate from Japanese to English and that the attached translations are, to the best of my knowledge and belief, a true and accurate translation of the documents entitled below from Japanese to English.

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

- WO2010089815A1



Simon Edmunds

07/31/2025
