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(54) [Title of invention]	Semiconductor memory device					

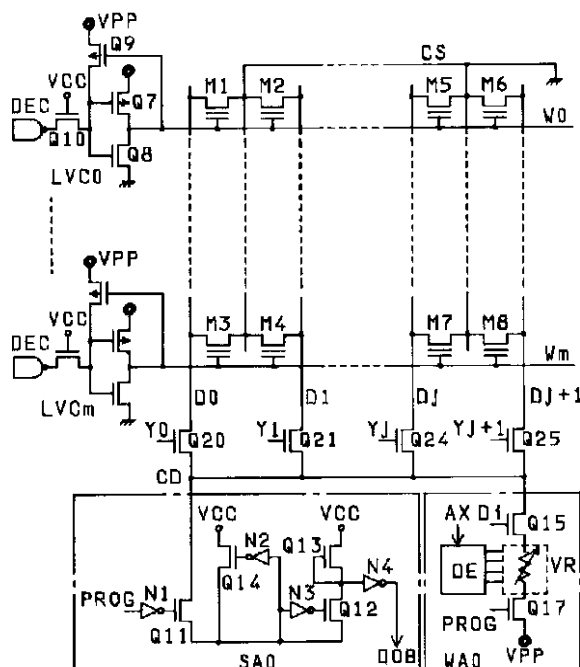
(57) (ABSTRACT)

(Objective) To provide a semiconductor memory device with improved writing characteristics.

(Configuration) A memory element in which a write operation is performed by injecting an information charge into a floating gate, comprising a matrix arrangement at the intersection point of word lines and data lines, and the output voltage of a writing load circuit provided via a Y gate that performs a data line selection operation is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines.

(Effects) Because the voltage drop caused by the resistance component of the data line is compensated for on the writing load circuit side, it is possible to improve the writing characteristics of the memory element.

FIG. 1



(SCOPE OF PATENT CLAIMS)

(Claim 1) A semiconductor memory device characterized in that a memory array in which memory elements to which write operations are performed by injecting an information charge into the floating gate are arranged in a matrix at the intersection of word lines and the data lines, and a write load circuit provided via a Y gate, which performs a data line selection operation, wherein the output voltage of the write load circuit is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines.

(Claim 2) The semiconductor memory device of Claim 1, characterized in that the aforementioned write load circuit comprises a plurality of MOSFETs in parallel form, and is switched by adjusting the number of MOSFETs comprising the aforementioned plurality that are turned on by control signals formed by decoding an X-system address signal that divides the aforementioned memory array into multiple blocks relative to the data line direction, thereby switching the combined resistance value.

(Claim 3) The semiconductor memory device of Claim 1 or Claim 2, characterized in that the above data lines are made to have a relatively large resistance value by increasing their length.

(Detailed description of the invention)

[0001]

(Industrial Field of Use) This invention relates to a semiconductor memory device, and more particularly to a technique that is effective when used for a non-volatile semiconductor memory device such as an EPROM (erasable programmable read-only memory).

[0002]

(Prior Art) There are EPROMs from which stored information can be erased by ultraviolet light, and EEPROMs (Electrical erasable programmable read-only memory) that can be electrically erased. Although EEPROMs can be rewritten electrically, the size of the memory cells is approximately 2.5 to 5 times that of EPROMs, making them unsuitable for achieving large storage capacities. Thus, recently, a device called an electrically mass-erasable EEPROM has been developed as an intermediate non-volatile memory device between the two. An electrically mass-erasable EEPROM is a nonvolatile memory device that has the function of electrically erasing a chip as a whole or a group of memory cells as a whole. It can have memory cells that are as small as those of EPROM. For the mass-erasable EEPROM, see page 152 of the International Solid-State Circuits Conference (ISSCC) 1980 and page 76 of the International Solid-State Circuits Conference (ISSCC) 1987, and IEEE Journal of Solid-State Circuits, Vol. 23, No. 5 (1988) pp.1157-1163 (IEEE J. Solid-State Circuits, vol. 23 (1988) pp. 1157-1163).

[0003]

(Problem to be Solved by the Invention) As storage capacity becomes larger, the number of memory elements connected to a single data line increases. Therefore, the length of the data line also increases, and the resistance component cannot be ignored. From the perspective of a write load circuit provided

via a Y-gate that performs data line selection, a relatively large difference in the voltage applied to the drain of the memory element at the time of writing occurs between the memory element at the near end of the data line and the memory element at the far end due to a voltage drop due to the resistance component contained in the data line.

[0004] In other words, in the current-voltage characteristic diagram of the memory element as shown in FIG. 4, because the resistance component of the data line is not included at the near end of the data line, its partial load resistance value decreases, and a drain voltage such as at intersection point a with the load characteristic A indicated by the dashed line is given. In contrast, at the far end of the data line, the resistance component of the data line is included in the load, resulting in a substantial load resistance value, and a drain voltage such as intersection point b with the load characteristic B indicated by the dashed line is given. As a result, the write depth is deep at the near end of the data line, and the write depth is shallow at the far end of the data line.

[0005] The purpose of this invention is to provide a semiconductor memory device with improved write characteristics. The foregoing and other objects and novel features of the invention will become apparent from the description of this specification and the accompanying drawings.

[0006]

[Means for Solving the Problem] The representative inventions disclosed in this application will be briefly outlined below. That is, a memory element in which a write operation is performed by injecting an information charge into a floating gate, comprising a matrix arrangement at the intersection point of word lines and data lines, and the output voltage of a write load circuit provided via a Y gate, which performs a data line selection operation, is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines.

[0007]

[Operation] According to the aforementioned means, because the voltage drop caused by the resistance component of the data line is compensated for on the write load circuit side, it is possible to improve the write characteristics of the memory element.

[0008]

[Example] FIG. 2 shows a block diagram of one embodiment of an EPROM to which the present invention has been applied. Although not limited to this, each circuit block shown in the drawing is formed on a single semiconductor substrate using well-known semiconductor integrated circuit technology. In the drawing, a memory array (or memory mat) is formed by a plurality of word lines, a plurality of data lines arranged to intersect with these word lines, and non-volatile memory elements (hereinafter referred to as memory cells) provided at each intersection of the word lines and data lines, arranged in a matrix. In the memory array, the word lines are arranged to extend laterally, and the word lines are coupled to the control gates of the memory cells. Data lines (which may also be

referred to as bit lines or digit lines) and source lines are arranged to extend in the longitudinal direction. The drains and sources of the memory cells are connected in common to these data lines and source lines.

[0009] ADB is an address buffer that receives external address signals A0 to Ai supplied via an external terminal, and forms an internal address signal ay corresponding to the X-system address signal and an internal address signal ax corresponding to the Y-system address signal. XDC is an X-system decoder that receives an internal address signal ax formed by the address buffer ADB described above and decodes this internal address signal ax.

[0010] YDC is a Y-system decoder, and decodes the internal address signal ay formed by the address buffer ADB described above to form a data line selection signal according to the internal address signal ay. A Y-gate YG is provided that combines a data line indicated by the internal address signal ay above among the plurality of data lines provided in each memory block MB0-MBn of the memory array with a common data line. This Y-gate YG receives a data line selection signal formed by the Y-system decoder YDC described above, and connects the above one data line to a common data line corresponding thereto.

[0011] In this way, in the memory array, one word line and one data line are selected according to the internal address signal ax of the X system corresponding to address signals A0 to Ai and the internal address signal ay of the Y system, and a memory cell is selected at the intersection of this selected word line and the data line. That is, the selected word line and the memory cell coupled to the data line are selected from a plurality of memory cells in the memory array.

[0012] When a plurality of memory cells are to be selected in a single memory access, in other words, when writing/reading multiple bits of data, a plurality of memory arrays as described above are provided. Although not particularly limited, in this example, data is written/read in units of 8 bits. In this case, there are eight memory arrays as described above.

[0013] In this embodiment, write and read operations are performed almost simultaneously on the memory cells selected from each of the eight memory arrays as described above. In other words, information is written or read in 8-bit units. To this end, the EPROM of this embodiment is provided with eight external input/output terminals D0 to D7, and between the eight memory arrays and the corresponding external input/output terminals D0 to D7, there are provided an input/output circuit IOB consisting of a data input buffer and a data output buffer, sense amplifiers SA as read-out circuits, and a write-load circuits WA as write-out circuits. Eight of each of these sense amplifiers SA and write load circuits WA are provided in accordance with the eight memory arrays described above, each corresponding to external input/output terminals D0 to D7.

[0014] In the same figure, CLG is a control circuit which generates timing signals required for a series of operations in response to external signals or voltages supplied to external terminals CEB, OEB, and WEB and high voltage VPP, and signals from the internal circuits. For example, control circuit CLG provides control signal PROG to sense amplifier SA and write load circuit WA in addition to sending control signals through signal line IOC to the input/output circuit IOB to control write and read operations.

[0015] Terminal CEB is a control input terminal to which a chip enabled signal is input, OEB is a control input terminal to which an output enabled signal is input, and WEB is a control input terminal to which a write enable signal is input. Also, VCC is an external terminal for supplying a power supply voltage VCC such as about 5V to each circuit, and GND is an external terminal for supplying a ground potential of 0V of the circuit to each circuit block. VPP is a high voltage terminal to which a high voltage such as 12V is input when writing.

[0016] In this embodiment, in order to homogenize the overall write depth of the memory cell due to the resistance component of the data line, in other words, in order to improve the write characteristics for the memory cell at the far end of the data line, write load circuit WA is provided with a function to adjust the write output voltage. That is, the write load circuit WA outputs a relatively low voltage when writing to a memory cell on the near end of the data line, and outputs a relatively high voltage after writing to a memory cell on the far end of the data line.

[0017] To identify the location relationship of the memory cell to such a data line, the memory array is divided into four blocks, such as blocks MAT0 to MAT3, relative to the data line direction. That is, for write load circuit WA, the nearest block is MAT0, followed by MAT1, TMAT2, and MAT3 in that order. The write operation to a memory cell belonging to a block as described above, with the word line address being physically assigned in order starting from the Y-gate YG side, can identify whether a memory cell belonging to any of the above blocks MAT0-MAT3 has been selected by decoding the address signal AX consisting of the top two bits of the X system. That is, the write load circuit WA recognizes the block in which the selected memory cell is provided upon receiving the address signal AX described above, adjusts the load resistance value in response, and forms an output voltage that compensates for the voltage drop caused by the resistance component of the data line.

[0018] FIG. 1 shows a schematic diagram of a memory array portion and major peripheral circuits, which is one embodiment of an EPROM to which this invention was applied. Although not particularly limited, each circuit element in the drawing is formed on a semiconductor substrate such as monocrystalline silicon by known techniques for manufacturing complementary MOS (CMOS) integrated circuits. In the drawing, a P-channel MOSFET is distinguished from an N-channel MOSFET by the addition of arrows to the channel (backgate). This is the same in the other drawings.

[0019] Although not particularly limited, an integrated circuit is formed into a semiconductor substrate consisting of monocrystalline P-type silicon. An N-channel MOSFET is composed of a source region, a drain region formed on the surface of the semiconductor substrate, and a gate electrode made of polysilicon that is formed on the surface of the semiconductor substrate between the source region and the drain region, with a thin gate insulating film interposed therebetween. A P-channel MOSFET is formed in the N-shaped well region formed on the semiconductor substrate surface. As a result, the semiconductor substrate constitutes a common substrate gate for the multiple N-channel MOSFETs formed thereon, and is supplied with the ground potential of the circuit. The N-well region constitutes the substrate gate of the P-channel MOSFET formed thereon. The board gate or N-well area of the P-channel MOSFET is coupled to the supply voltage VCC. However, in the case of high voltage circuits, the N-shaped well region in which the corresponding P-channel MOSFET is formed is connected to the external high voltage VPP, internally generated high voltage, etc.

[0020] The integrated circuit may be formed on a semiconductor substrate composed of monocrystalline N-type silicon. In this case, the N-channel MOSFET and the non-volatile memory elements are formed in the P-shaped well region, and the P-channel MOSFET is formed on the N-shaped substrate. In this invention, MOSFET is used to mean an insulated-gate field effect transistor (IGFET).

[0021] As the memory array described above, eight memory cells M1 to M8 are illustratively shown as representative. That is, the memory array is constituted by memory cells (non-volatile memory elements... MOSFETs M1 to M8) of a stacked gate structure having a control gate and a floating gate as shown by way of example, word lines W0 to Wm, and data lines D0, D1 to Dj, and Dj+1.

[0022] In the memory array illustrated above, the control gates of the memory cells M1, M2, M5, and M6 (M3, M4, M7, and M8) arranged in the same row are connected to the corresponding word line W0 (Wm). The word lines W0 and Wm are driven by level conversion circuits LVC0 and LVCm that make up the word driver. When the output of the address decoder circuit DEC is set to a low level, the low level is communicated through the cut-off MOSFET Q10, the N-channel MOSFET Q8 is turned off, the P-channel MOSFET Q7 is turned on, and the high voltage VPP is communicated to the word line W0. When the output signal of the above address

decoder circuit DEC is at a high level, the N-channel type MOSFET Q8 is turned on through the cut-off MOSFET Q10, and the word line W0 is reduced to a lower level such as the ground potential of the circuit. This low level causes the return P-channel MOSFET Q9 to be turned on, and the input signal is raised to high voltage VPP, and therefore the P-channel MOSFET Q7 is turned off. Because the cut-off MOSFET Q10 goes to the OFF state due to such an increase in the input signal, DC current flow is prevented towards the decoder circuit DEC, which operates from the high voltage VPP at the supply voltage VCC to form a high level output signal. During the read operation, VPP is switched to VCC.

[0023] The drains of memory cells M1, M3, M2, and M4 arranged in the same column are connected to corresponding data lines D0 and D1, respectively, and the drains of memory cells M5, M7, M6, and M8 are connected to corresponding data lines Dj and Dj+1, respectively. The sources of the memory cells M1-M8 are connected to the common source line CS.

[0024] Although not particularly limited, in order to write/read in multiple bit units such as 8 bits (or 16 bits, etc.), the memory array described above is configured to be provided in multiple sets such as 8 sets (or 16 sets, etc.) in total. The drawing shows one bit of the circuit.

[0025] Each data line D0 to Dj+1 comprising the one memory array described above is connected to a common data line CD via a column selection switch MOSFETs Q20, Q21 to Q24, Q25 constituting a Y-gate YG that receives selection signals Y0, Y1 to Yj, Yj+1 formed by the Y-system decoder YDC. Common data line CD is connected to the output terminal of write load circuit WA0. This write load circuit WA0 consists of a series circuit consisting of a MOSFET Q15 receiving an output signal Di of a data input buffer for writing that receives a write signal input from a corresponding D0 terminal D0 to D7, a MOSFET Q17 receiving a variable resistance circuit VR, and a control signal PROG, and conveys the voltage of the high voltage terminal VPP to the common data line CD.

[0026] The other side of the common data line CD is coupled to the input terminal of the input stage circuit of sense amplifier SA0 via switch MOSFET Q11. The circuit consisting of MOSFET Q12 to Q14, which performs the amplification operation of the input stage, control inverter circuits N2 and N3, and CMOS inverter circuit N4 will be referred to as sense amplifier SA0. The MOSFET Q11 is controlled by the output signal of inverter circuit N1 that receives the control signal PROG and is turned off during write operation. Therefore, the relatively high potential of the common data line CD during writing is not supplied to the input of sense amplifier SA0.

[0027] The memory level of the memory cell read out onto the common data line CD is connected to the source of the N-channel type amplifying MOSFET Q12 to which the source is connected through the MOSFET Q11 which is turned on during readout. Between the drain of this amplifying MOSFET Q12 and the power supply voltage terminal VCC is a P-channel load MOSFET Q13, the gate and source of which are connected. The above load MOSFET Q13 operates such that a precharge current flows to the common data line CD for read operation.

[0028] In order to increase the sensitivity of the amplifying MOSFET Q12 described above, the voltage of the common data line CD is supplied via the switch MOSFET Q11 to the input of inverter circuits N2 and N3 which act as inverting amplifier circuits. The output signal of inverter circuit N3 as an inverting amplifier circuit is supplied to the gate of the amplifying MOSFET Q12 described above. In addition, the source input is charged up from the power terminal VCC via MOSFET Q14, which acts as a limiter. The gate of this MOSFET Q14 is supplied with the output signal of inverter circuit N2 as an inverting amplifier circuit.

[0029] When reading the memory cell, the memory cell has a high threshold voltage or a low threshold voltage for the word line selection level depending on the information charge accumulated in the floating gate. If the memory cell selected by the X-system and Y-system decoders XDC, YDC is turned off despite the word line being set to the selection level, the common data line CD is made relatively high by the current supply from MOSFETs Q12 and Q14. On the other hand, if the selected memory cell is turned on by the word line selection level, the common data line CD is relatively low-level.

[0030] In this case, the high level of the common data line CD is limited to a relatively low potential by supplying to the gate of MOSFET Q14 a relatively low level output voltage formed by the inverting amplifier circuit which receives this high level potential. On the other hand, the low level of the common data line CD is limited to a relatively high potential by supplying to the gate of the MOSFET Q14 a relatively high level voltage formed by the inverting amplifier circuit that receives this low level potential. Such a level limiting action of the common data line CD allows the signal change rate to be substantially faster when the memory information read sequentially from the memory cell changes from level 1 to level 0, or from level 0 to level 1.

[0031] The amplifying MOSFET Q12 amplifies the gate-grounded source input, and transmits the output signal to the input of CMOS inverter circuit N4. CMOS inverter circuit N4 shapes the waveform of the drain output signal of the amplifying MOSFET Q12 and transmits it to the input of the corresponding data output buffer DOB. Data output buffer DOB amplifies the signal from the sense amplifier SA0 above and outputs it from the corresponding external terminal D0. Also, although omitted in the drawing, the write signal supplied from the above external terminal D0 is input to the data input buffer, and its output signal Di is supplied to the gate of MOSFET Q15 of the write load circuit WA0.

[0032] In this embodiment, in order to prevent the write depth from differing between the memory cells at the near end of the data line and the memory cells at the far end, a memory block as in FIG. 1 is assumed, and the selected address AX is input into the block decoder circuit DE, and the block to which the selected memory cell belongs is identified, and the resistance value of the variable resistance VR is adjusted accordingly. This increases the write voltage output to the common data line CD to compensate for the voltage drop caused by the resistance component of the data line that is larger in proportion to the length of the data line between the memory cell and the Y gate.

[0033] FIG. 3 shows a schematic diagram of one embodiment of the block decoder circuit DE and variable resistance circuit VR described above. The block decoder circuit DE forms three select signals S0-S2 based on two-bit address signal A8B and A9B for identifying blocks MAT0-MAT3 as described above. For example, block MAT0 close to Y-gate YG is specified when address signals A8 and A9 are both high-level. The next closest block, MAT1, is specified when address signals A8B and A9 are both high-level. The next closest block, MAT2, is specified when address signals A8 and A9B are both high-level. The farthest block, MAT3, is specified when address signals A8B and A9B are both high-level. In this configuration, as shown in FIG. 1, the memory cell that is farthest from Y gate YG (write load circuit WA) side is assigned address 0, and physical addresses are assigned in increasing order toward the Y gate. Note that signals with B added, such as address signals A8B and A9B, are address signals in reverse phase with respect to that of address signals input from an external source. In contrast, address signals A8 and A9 are address signals that are in phase with externally input address signals.

[0034] The above address signals A8B and A9B are supplied to the inputs of NAND gate circuit G1. The output signal of this NAND gate circuit G1 is reversed by inverter circuit N1 to be selection signal S0. The address signal A9B is used as selection signal S1. The address signal A8B and the address signal A9B are supplied through inverter circuit N2 to NAND gate circuit G2. The output signal of this NAND gate circuit G2 and the output signal of the inverter circuit N2 are input to the NAND gate circuit G3, and a select signal S2 is formed from the output of this NAND gate circuit G3.

[0035] Variable resistance circuit VR consists of MOSFETs Q1 to Q4 in parallel form. The gate of MOSFET Q1 is constantly supplied with a bias voltage VP. This MOSFET Q1 sets the maximum resistance value of the variable resistance circuit VR. In other words, when a write operation is performed on the memory cell in block MAT0, the address signals A8B and A9B are both at the low level, so that the selected signals S0 to S2 are all at the low level, and the other MOSFETs Q2 to Q4 are turned off, and only MOSFET Q1 is turned on to output a write voltage.

[0036] When a write operation is performed to the memory cell in block MAT1, the address signal A8B is set to high level and A9B is set to low level. This causes the selection signal S2 to be high and MOSFET Q4 to be turned on. This reduces the combined resistance values from the parallel MOSFETs Q1 and Q4 to form an output voltage that compensates for the voltage drop due to the resistance component of the data line from Y-gate YG to block MAT1.

[0037] When a write operation is performed to the memory cell of block MAT2, the address signal A8B is set to low level and A9B is set to high level. This causes the selection signals S2 and S1 to be high and MOSFETs Q4 and Q3 to be turned on. This further reduces the combined resistance values by parallel MOSFETs Q1, Q4 and Q3 to form an output voltage that compensates for the voltage drop due to the resistance component of the data line from Y-gate YG to block MAT2.

[0038] When a write operation is performed to the memory cell of the farthest block MAT3, both address signals A8B and A9B are set to high level. As a result, in addition to the selection signals S2 and S1, S0 also becomes high level, and all MOSFETs Q1 to Q4 are turned on, and their combined resistance value is set to the minimum value to form an output voltage that compensates for the voltage drop caused by the resistance component of the data line from Y-gate YG to block MAT3.

[0039] The actual load characteristic consisting of the resistance component of the data line as seen from the memory cell, the MOSFET constituting the Y gate, and the load circuit described above, if the resistance value in the write load circuit is constant, as in the prior art, the resistance component of the data line will be added on the far end side of the data line to become the load characteristic B as shown in FIG. 4, but in this embodiment, compensation is made to maintain characteristic A in any block by adjusting the resistance on the load circuit side.

[0040] In a write operation, the write voltage transmitted to the common data line CD requires a higher voltage than the supply voltage VCC. Therefore, the high level of the selection signals S0-S2 given to the gates of MOSFETs Q1-Q4 needs to be matched to the bias voltage VP higher than the supply voltage VCC. Therefore, gate circuits G1 to G3 and inverter circuits N1, N2, etc., which comprise block decoder circuit DE, are composed of circuits with bias voltage VP as the operating voltage as described above. In addition, a level conversion circuit may be provided in the output part of the circuit operated

by VCC to output a signal at the level described above.

[0041] When a write operation is performed, MOSFET Q17 is turned on due to the high level of the control signal PROG, and switch MOSFET Q15 is turned on/off according to write data Di. When this MOSFET Q15 is turned on, a relatively high voltage is supplied to the drain of the selected memory cell, so that hot electrons generated in the vicinity of the drain are taken into the floating gate, thereby carrying out a charge write operation. The occurrence of these hot electrons is affected by the drain-to-source voltage of the memory cell, so the write depth per unit time varies depending on the size of the drain voltage.

[0042] The effect obtained from the above embodiment is as follows. That is,

(1) In a memory element in which a write operation is performed by injecting an information charge into a floating gate, comprising a matrix arrangement at the intersection point of word lines and data lines, and the output voltage of a write load circuit provided via a Y gate which performs a data line selection operation is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines, the effect is achieved that improvement in the characteristics of the memory element is thereby made possible.

[0043] (2) In accordance with (1) above, since the influence of the resistive component of the data lines can be reduced, the length of the data lines can be increased, and thus the number of memory cells connected to one data line can be increased, and the effect is achieved of realizing increased storage capacity. Incidentally, if resistance adjustment is not performed in the write load circuit, the length of the data lines is limited because the write depth varies greatly due to the resistance component as the length of the data lines increases. Consequently, as the number of memory arrays or memory mats increases, such as by dividing data lines, the number of Y gates and decoders increases accordingly, which is a major obstacle to achieving a large storage capacity.

[0044] (3) The effect is obtained that, assuming the memory array is divided in the direction of the data lines to create memory blocks, it is possible to generate control signals for a variable resistance circuit made up of MOSFETs in a parallel configuration by means of a simple configuration that decodes the X-system address signal to identify the position of the memory cell to be written.

[0045] While the invention made by the present inventor has been specifically described above based on the embodiments, this invention is not limited to the above embodiments, and can be modified in various ways to the extent that it does not deviate from the summary. For example, when configuring a variable resistance circuit with MOSFETs connected in parallel, the data lines are divided according to the number. Alternatively, one MOSFET may be used as a variable resistive element. As a gate control voltage in this case, for example, an X-system address signal can be input into a digital/analog conversion circuit to form a control voltage that is proportionally greater than the physical distance between the write load circuit and the selected memory cell. As the memory element, in addition to a MOS transistor with a stacked gate structure as used in EPROM, the write operation may also use a FLOTOX-type non-volatile memory element that uses a tunneling phenomenon. High voltage VPPs for write/erase are not limited to those that use externally supplied high voltages. That is, if the current flowing during write/erase is small, a voltage boosted from a low voltage VCC by a known charge pump circuit, etc. inside the EPROM or EEPROM may be used. This internally boosted power supply may also be used in combination with an external high voltage VPP.

[0046] The erasing operation may be performed electrically using tunnel current. If such an erasing operation is also performed electrically, the corresponding erase circuit and erase control circuit are added. The circuit portion for controlling writing/reading and the circuit portion for controlling the erase algorithm as described above may be configured using a random logic circuit, or may be configured to incorporate a programmable logic array (PLA), microcomputer and software. Semiconductor memory devices,

such as EPROMs and EEPROMs, may be integrated into digital semiconductor integrated circuit devices, such as microcomputers, etc.

[0047]

[Effects of Inventions] The effects obtained by the representative inventions disclosed in this application are briefly outlined below. That is, a memory element in which a write operation is performed by injecting an information charge into a floating gate, comprising a matrix arrangement at the intersection point of word lines and data lines, and the output voltage of a write load circuit provided via a Y gate which performs a data line selection operation is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines, thereby allowing improvement in the characteristics of the memory element.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1] A circuit diagram of a memory array portion and major peripheral circuits showing one embodiment of the EPROM according to the invention.

[FIG. 2] A block diagram showing one embodiment of an EPROM in which this invention is applied.

[FIG. 3] A circuit diagram showing one embodiment of a block decoder and a variable resistance circuit.

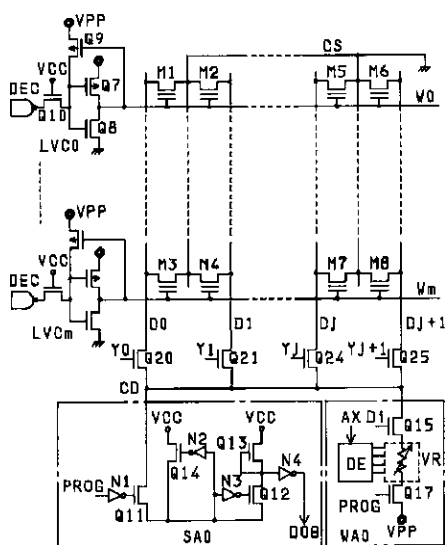
[FIG. 4] A characteristic diagram for describing the write characteristics of a memory cell.

[EXPLANATION OF REFERENCES]

ADB ... address buffer, XDC ... X-system decoder, YDC ... Y-system decoder, MAT0-MAT3 ... block, YG ... Y gate, SA ... sense amplifier, WA ... write load circuit, IOB ... input/output circuit, CLG ... control circuit, DEC ... address decoder circuit, DE ... block decoder, VR ... variable resistance circuit.

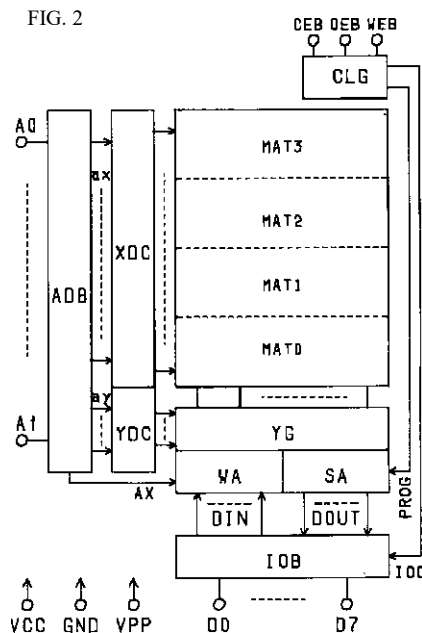
[FIG. 1]

FIG. 1



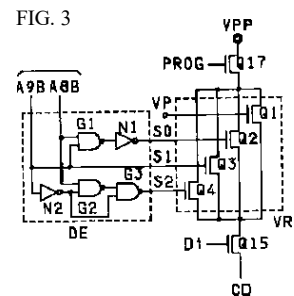
[FIG. 2]

FIG. 2



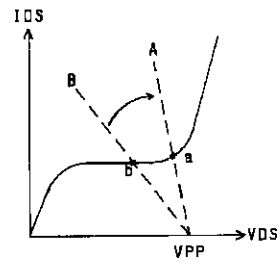
[FIG. 3]

FIG. 3



[FIG. 4]

FIG. 4



I, Matthew Francis, hereby certify that I am competent to translate from Japanese to English and that the attached translations are, to the best of my knowledge and belief, a true and accurate translation of the documents entitled below from Japanese to English.

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

- JP_H06150670_A



Matthew Francis

Linguist Name

May 23, 2025

Date