

H05-062484

(43) Publication date March 12, 1993

(51) Int. Cl. ⁵	Identification codes	JPO file number	FI	Technical indications
G11C	16/06			
G06F	1/32			
		9191-5L	G11C	17/00
		7832-5B	G06F	1/00
				309 A
				332 A
Request for examination Not yet requested			Number of claims 3 OL (Total of 15 pages)	

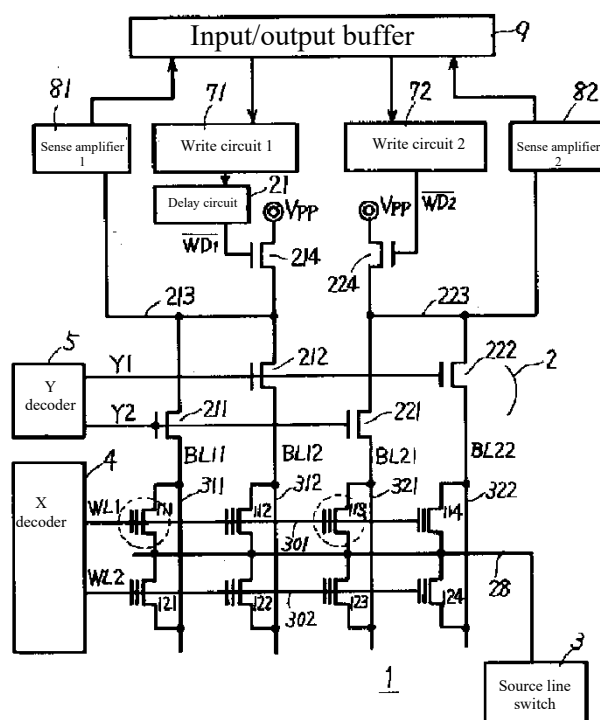
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(54)[TITLE OF THE INVENTION] Non-volatile semiconductor storage device

(57) [ABSTRACT]

[PURPOSE] To achieve the suppression of peaks of write current and current during write operations.

[CONSTITUTION]A non-volatile semiconductor storage device that is characterized by the fact that a plurality of non-volatile memory cells are arranged in an array, and there are X and Y decoders to select each memory cell, a plurality of write transistors to apply a write voltage to the memory cells that were selected, and a delay circuit to differentiate the timing at which the write transistor begins to turn ON.



[SCOPE OF PATENT CLAIMS]

[CLAIM 1] A non-volatile semiconductor storage device with a multi-bit structure that is provided with a memory cell array having a plurality of memory cells that can each store information in a non-volatile manner, wherein this non-volatile semiconductor storage device is characterized by the fact that it includes

a means to select said multi-bit memory cell in response to an address signal that may be provided;

a plurality of write voltage supply means to supply the write voltage for writing information to said multi-bit memory cell that was selected, and a write timing control means to differentiate the supply timing for the write voltage between a predetermined number of write voltage supply means and the remaining write voltage supply means of said plurality of write voltage supply means.

[CLAIM 2] The non-volatile semiconductor storage device as described in Claim 1 above, wherein said write timing control means includes delay means to delay the write timing of a predetermined number of write means amongst said plurality of write voltage supply means.

[CLAIM 3] The non-volatile semiconductor storage device as described in Claim 1 above, wherein said write timing control means includes a first clock signal to control the write voltage supply timing of a predetermined number of write voltage supply means of said plurality of write voltage supply means, and a second clock signal to control the write voltage supply timing of the remaining write voltage supply means of said plurality of write voltage supply means, and said first clock signal and said second clock signal are prevented from overlapping one another.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF INDUSTRIAL APPLICATION] The present invention relates to a non-volatile semiconductor storage device, and in particular, it relates to flash EEPROM (Electrically Erasable and Programmable Read Only Memory).

[0002]

[PRIOR ART] One type of semiconductor storage device that stores information is a non-volatile semiconductor storage device that stores information in a non-volatile manner. One such non-volatile semiconductor storage device is a semiconductor storage device called EEPROM that is capable of electrically erasing and writing information. One of these EEPROMs is a flash EEPROM (flash-type nonvolatile semiconductor storage), which performs electrical writing (programming) of information in bytes (eight bits) and electrically deletes (erases) all of the bytes of information at the same time.

[0003] Figure 9 is a diagram that schematically illustrates the cross-sectional structure of a memory cell of the conventional commonly-used flash EEPROM. In Figure 9, the memory cell includes floating gate 16 that may be formed on semiconductor substrate 15, control gate 17 that may be formed on floating gate 16, and source diffusion region 18 and drain diffusion region 19 that may be formed on the surface of semiconductor

substrate 15.

[0004] A thin insulating film (such as an oxide film) with a film thickness of approximately 100 Å may be formed between floating gate 16 and semiconductor substrate 15, for example. This thin insulating film allows for the movement of electrons by utilizing the tunneling phenomenon between floating gate 16 and source diffusion region 18. The writing (programming) of data into memory cells and the erasing of data from memory cells may be performed as described below.

[0005] At the time of programming, drain diffusion region 19 will receive the application of a program voltage of approximately 6.5 V, while a high pressure V_{pp} of 12 V will be applied to control gate 17, and source diffusion area 18 will be grounded. A channel region is formed on the surface of semiconductor substrate 15 in response to the high pressure V_{pp} that may be applied to control gate 17, which causes the memory cell to enter the ON state, and as a result, current will flow from drain diffusion region 19 to source diffusion region 18. At that time, an avalanche breakdown occurs in the vicinity of drain diffusion region 19, generating an electron hole pair. The holes flow towards the ground potential via semiconductor substrate 15, while the electrons flow along this channel direction to drain diffusion region 19. Some of the electrons generated by the avalanche breakdown are accelerated by the high electric field formed between floating gate 16 and drain diffusion region 19 to become hot electrons, which will be injected into floating gate 16. The electrons will be injected into floating gate 16, which increases the threshold voltage of the memory cell. This state is defined as the state in which information "0" may be stored.

[0006] Erasing may be performed by setting drain diffusion region 19 to the open state, setting control gate 17 to the ground potential, and applying high pressure V_{pp} to source diffusion region 18. Between source diffusion region 18 and floating gate 16, a voltage may be applied by performing capacity partitioning of the voltage between this control gate 17 and source diffusion region 18. The potential difference between source diffusion region 18 and floating gate 16 (approximately 2 MV) results in a Fowler-Nordheim tunneling phenomenon in which the electrons of floating gate 16 are drawn into source diffusion region 18. As a result, the threshold voltage of the memory cell is reduced. This condition is defined as the state in which the information "1" may be stored.

[0007] The normal "H" level voltage may be applied to control gate 17 when the data is read. If the memory cell stores information "0", its threshold voltage will be high, while if it stores information "1", its threshold voltage will be low. The ON/OFF state of the memory cell may be determined according to this threshold voltage. In the ON state of the memory cell, a channel is formed on the surface of semiconductor substrate 15 and current flows between drain diffusion region 19 and source diffusion region 18. On the other hand, when the memory cell is in the OFF state, no channels are formed on the surface of semiconductor substrate 15, and therefore, no current flows between drain diffusion region 19 and source diffusion region

18. Data may be read out by detecting the presence or absence of this current.

[0008] As described above, a memory cell that is a component of a flash EEPROM is a transistor that stores information according to the amount of electrons stored in the floating gate.

[0009] Figure 10 is a diagram that schematically illustrates the overall configuration of the flash EEPROM using the memory cell shown in Figure 9. The flash EEPROM shown in this Figure 10 was disclosed by V.N. Kynett in the IEEE Journal of Solid State Circuits, Vol. 23 No. 5, October 1998, on pages 1157 through 1163 (V. N. KYNETT).

[0010] Referring to Figure 10, the flash EEPROM includes memory cell array 1 in which the memory cells shown in Figure 9 are arranged in a matrix shape, X decoder 4 to select a row of memory cell array 1, and Y-gate 2 and Y-decoder 5 to select a column of memory cell array 1. X decoder 4 and Y decoder 5 are latched onto addresses that may be provided from an external source, and will be provided with internal row and column addresses from address register 6, which generates the internal addresses, respectively. X decoder 4 decodes the internal row address and selects the corresponding row in memory cell array 1. Y decoder 5 decodes the given internal column address and gives the decode results to Y-gate 2. Y-gate 2 connects a corresponding column of memory cell array 1 to write circuit 7 or sense amplifier 8 in response to this decode result (row selection signal).

[0011] In flash EEPROM, data input/output may be performed in units of one byte, so Y decoder 5 sets eight selected gates in Y gate 2 to the ON state so as to select one byte of memory cell (8-bit memory cell) of memory cell array 1.

[0012] Source line switch 3 is provided to set the source potential of each memory cell for memory cell array 1. This source line switch 3 applies high pressure V_{pp} to the source area of each memory cell in the erasing mode, while during writing (programming), the source of each memory cell is set to the ground potential V_{ss} .

[0013] Write circuit 7 and sense amplifier 8 perform the input/output of one byte of data VO_0 to VO_7 externally via input/output buffer 9. In other words, input/output buffer 9 receives external write data VO_0 to VO_7 during data writing, generates the internal write data, and provides it to write circuit 7. During data reading, input/output buffer 9 receives the read data from a 1-byte memory cell via sense amplifier 8 and generates external read data VO_0 to VO_7 .

[0014] Flash EEPROM further includes program voltage generation circuit 10, verification voltage generation circuit 11, command register 12, command decoder 13, and control circuit

14 as the peripheral circuits. Program voltage generation circuit 10 generates a high voltage V_{pp} for the program during programming, and provides the program high voltage V_{pp} to X decoder 4. Also, program voltage generation circuit 10 provides a high voltage of approximately 6.5 V to Y decoder 5 during programming, while during erasing, it will provide a high pressure V_{pp} to source line switch 3.

[0015] Verification voltage generation circuit 11 generates a verification voltage to verify whether or not the data of the memory cell has been erased reliably during the erasing operation. In the erase verification mode and programming mode, a verification voltage is generated to verify whether or not the predetermined data has been written to the corresponding memory cell, and it is provided to X decoder 4 and program voltage generation circuit 10, etc.

[0016] Command register 12 receives data from input/output buffer 9 that sets the operation mode of this EEPROM in response to the control signal from control circuit 14. Command decoder 13 decodes the command set in this command register 12 and controls operations such as of source line switch 3 and verification voltage generation circuit 11 according to the decode results.

[0017] By establishing command register 12 and command decoder 13, etc., it will be possible to easily configure the erase, erase verification, program, program verification, and read (data read) modes using an external microprocessor. A high voltage V_{pp} of approximately 12 V, a voltage of approximately 5 V (operating power supply voltage) V_{cc} and the ground potential V_{ss} may be provided from the outside.

[0018] Control circuit 14 generates various internal control signals in response to the external control signals, such as write enable signal/WE, chip enable signal/CE and output enable signal/OE. This flash EEPROM is set to data read mode when the read code is loaded into command register 12 or when the high pressure V_{pp} drops to 5V or less.

[0019] Write enable signal/WE and chip enable signal/CE set each operating mode of this flash EEPROM. The contents of address register 6 are updated at the falling edge of write enable signal/WE. In other words, the address that may be provided from the external source is captured at the falling edge of write enable signal/WE and is latched onto address register 6. At the rising edge of write enable signal/WE, command register 12 and write circuit 7 are in a latched state. The operating mode of this flash EEPROM is set according to the command provided to input/output buffer 9 when write enable signal/WE rises.

[0020] Figure 11 is a diagram showing the configuration of the memory cell array shown in Figure 10 in more detail. This

memory cell array has a word structure of 4X2 bits. Referring to Figure 11, memory cell array 1 includes eight bits of memory cells 111 to 114 and 121 to 124, which are arranged in a matrix. Each memory cell is provided with one floating gate memory transistor. The control gates of memory cells 111 to 114 that are arranged in one row are connected to word line 301. Memory cells 121 to 124 that are arranged in the other row are connected to word line 302. Word line drive signal WL1 is transmitted from X decoder 4 to word line 301, while word line drive signal WL2 is transmitted from X decoder 4 to word line 302.

[0021] The drain of memory cells 111 and 121 is connected to bit line 311, while the drain of memory cells 112 and 122 is connected to bit line 312, the drain of memory cells 113 and 123 is connected to bit line 321, and memory cells 114 and 124 are connected to bit line 322. Bit lines 311 to 312 are connected to internal data transmission line (IO line) 213 via the corresponding Y-gate transistors 211 and 212. Bit lines 321 and 322 are connected to internal data transfer line 223 via Y-gate transistors 221 and 222. Row selection signal Y2 from Y-decoder 5 will be transmitted to the gates of Y-gate transistors 221 and 222, while row selection signal Y1 from Y-decoder 5 will be transmitted to Y-gate transistors 212 and 222.

[0022] The source of each memory cell is connected to source line 28 in common. Source line 28 is connected to source line switch 3.

[0023] Sense amplifier 81 and write transistor 214 are connected to internal data transmission line 213. Write transistor 214 is connected to write circuit 71, while its drain is connected to high pressure Vpp, and its source is connected to internal data line 213. Write transistor 224 is also connected to write circuit 72, while the drain is connected to high pressure Vpp, and the source is connected to internal data transmission line 223.

[0024] Source line 28 is commonly connected to the source of all memory cells in Figure 11, but it is also acceptable to have a configuration in which the memory cells are grouped and source line 28 is provided for each group.

[0025] Figure 12 is a diagram showing the timing of the operation when writing to the EEPROM shown in Figures 9 through 11.

[0026] The operation of the conventional flash EEPROM will now be described with reference to Figures 9 through 12.

[0027] First, the operation of selecting memory cells 111 and 113, which are enclosed by the dotted lines shown in Figure 11, to write data "0" to memory cell 111 and data "1" to memory cell 113 will be described. The data write operation is set by providing a program command to command register 12 when a

write cycle is set by write enable signal/WE and chip enable signal/CE.

[0028] In other words, in response to the control signal from control circuit 14 to command register 12 in the first write cycle, the program mode is set by providing the program command via input/output buffer 9. In the next write cycle, address register 6 and input/output buffer 9 latch the address and write the data of memory cells 111 and 113, respectively. Command decoder 13 controls the generated voltage of source line switch 3 and program voltage generating circuit 10 according to the decode results of the program command set in this command register 12. Program voltage generating circuit 10, in response to the control signal from command decoder 13, will generate program voltage high voltage Vpp and a high voltage of 6.5 V, after which these voltages will be transmitted to the drain of X decoder 4, Y decoder 5, and the write transistor, respectively. Source line switch 3 will set source line 28 to the ground potential in response to a control signal from command decoder 13.

[0029] X decoder 4 and Y decoder 5 will set word line drive signal WL1 and bit line selection signal Y2 to "H" in the active state according to the address latched onto address register 6. Write circuit 71 will be activated, while write circuit 72 remains inactive. Therefore, write transistor 214 is turned ON, write transistor 224 remains OFF, and write high voltage Vpp will be applied to data transmission line 213 only. At the same time, Y gates 211 and 221 and word line 301 are selected via Y decoder 5 and X decoder 4 based on the address signal. High voltage Vpp will then be applied to memory cell 111. Because write transistor 224 is OFF at this time, no high pressure Vpp will be applied to the drain of memory cell 113. Source wire 28 is also grounded by source wire switch 3 during programming. In this way, current flows only to memory cell 111, causing hot electrons to be generated, and the threshold voltage will increase. Because no current flows to memory cell 113, its threshold voltage will not change. At this time, the current due to high voltage Vpp forms a peak due to significant flow before the threshold voltage shifts, as shown in Figure 12.

[0030] On the other hand, erasing may be performed as described below. First, the X and Y decoders 4 and 5 are deactivated. All of the memory cells are deselected. In other words, word lines 301 and 302 of each memory cell are grounded and the drain is opened. Source line 28 is supplied with high voltage by source line switch 3. In this way, the tunneling phenomenon shifts the threshold voltage of memory cells 111 to 114 and 121 to 124 to be lower. Because source line 28 is common across all of the memory cells, erasing may be performed collectively across all of the memory cells.

[0031] Next, the reading operation will be described. As is the case with the writing operation, the reading of the memory cell enclosed by the dotted lines in Figure 11 will be described. The address signal is first decoded by Y decoder 5 and X decoder 4, and Y-gate transistors 211 and 221 that were selected as well as word line 301 will enter the "H" level. At this time, source line 28 will be grounded by source line switch 3. If the data is written to the memory cell and its threshold voltage is high (in the case of memory cell 111), even if the control gate is provided a "H" level, the memory cell will not turn ON and no current will flow from bit line 311 to source line 28. On the other hand, in the case in which data "0" is not written to the memory cell (in the case of memory cell 113), the memory cell will be turned ON, and current will flow from bit line 321 to source line 28. By detecting whether current flows through the memory cell using sense amplifiers 215 and 225, read data "1" and "0" may be obtained.

[0032] In this way, data of the flash EEPROM may be written, deleted, and read.

[0033]

[PROBLEM TO BE SOLVED BY THE INVENTION] The conventional EEPROM is configured as described above, so when writing data "0" to multiple bit memory cells simultaneously, peak current will flow through the memory cell where data "0" is written at the start of writing to the source line (see V_{pp} current in Figure 12). In other words, the current will increase proportionally to the number of memory cells to which data "0" is written. Therefore, if the power consumed by the resistive component of the source line becomes larger and the system is driven by a battery, etc., there may be a problem of the acceleration of battery depletion.

[0034] As a result, the purpose of the present invention is to reduce the peak of write current when writing data to multiple bit memory cells in a non-volatile semiconductor storage device.

[0035]

[MEANS FOR SOLVING THE PROBLEM] In order to achieve the purpose described above, the non-volatile semiconductor storage device according to the present invention is a non-volatile semiconductor storage device with a multi-bit structure that is provided with a memory cell array having a plurality of memory cells that can each store information in a non-volatile manner, and that boasts the following characteristics. In other words, the non-volatile semiconductor storage device includes a means to select said multi-bit memory cell in response to an address signal that may be provide, a plurality of write voltage supply means to supply the write voltage for writing information to said multi-bit memory cell that was selected, and a write timing control means to differentiate the supply timing for the write voltage between a predetermined number of write voltage supply means and the remaining write voltage supply means of said plurality of write voltage supply means.

[0036] Also, the present invention is characterized by the fact that said write timing control means includes a delay means to

delay the write timing of a predetermined number of write means among said plurality of write voltage supply means.

[0037] Further, said write timing control means is characterized by the fact that it includes a first clock signal to control the write voltage supply timing of a predetermined number of write voltage supply means of said plurality of write voltage supply means, and a second clock signal to control the write voltage supply timing of the remaining write voltage supply means of said plurality of write voltage supply means, and said first clock signal and said second clock signal are prevented from overlapping one another.

[0038]

[OPERATION] In the present invention as described above, peaks of the write current flowing to the source line can be suppressed by differentiating between the write voltage supply timing of the write voltage supply means of a predetermined number of write voltage supply means and the write voltage supply timing of the remaining write voltage supply means.

[0039] In addition, if the writing timing control means includes a delay means that delays the writing timing of a predetermined number of writing control means, the current flowing to the source line at the time of the writing start can be suppressed.

[0040] If the write timing control means further includes a means for generating a first write clock signal for controlling the write voltage supply timing of the specified number of write voltage supply means and a second write clock signal for controlling the write voltage supply timing of the remaining write voltage supply means, ensuring that the first clock signal and the second clock signal do not overlap each other, the write current during the program period can be reduced because the specified number of write voltage supply means and the remaining write voltage supply means will alternately turn ON and OFF.

[0041]

[EXAMPLES OF EMBODIMENT] Figure 1 is a circuit diagram showing one example of embodiment of the present invention. The parts that correspond to the conventional flash EEPROM as shown in Figure 11 are marked with the same reference symbols. In Figure 1, the flash EEPROM according to the present invention is equipped with delay circuit 21 that may be provided between write circuit 214 and write transistor 214. Delay circuit 21 will delay the write control signal from write circuit 71, converting the write control signal to a level of V_{pp} . In response to the V_{pp} level write control signal, write transistor 214 will switch ON and will output the high pressure V_{pp} to data transmission line 213. On the other hand, there is no delay circuit provided between the gates of write transistor 224 in direction write circuit 70, and write transistor 224 communicates the high voltage V_{pp} to data transmission line 223 in response to the write control signal from write circuit 72. As a result, the high pressure V_{pp} that may be outputted from write transistor 71 is slower in timing than the high pressure V_{pp} that may be outputted from write transistor 72. As a result,

even if data “0” is written to two or more memory cells, no high pressure V_{pp} will be applied to the two memory cells at the same time, making it possible to suppress the current flowing to the source line.

[0042] Figure 2 is a schematic diagram showing the details of the delay circuit shown in Figure 1. In Figure 1, delay circuit 21 includes delay inverters 22 and 23, NAND gate 24, transistor 25 for high voltage cutting, P-channel transistors 26 and 27, and N-channel transistor 28. After delaying the write data/WD from write circuit 71, delay inverters 22 and 23 will provide it to NAND gate 24. NAND gate 24 is provided with the output of delay inverter 23 into one input terminal and the write data/WD into the other input terminal. NAND gate 24 will output a signal that has delayed the write data/WD rise. High voltage cutting transistor 25 cuts the high voltage coming back from P-channel transistor 26 because the gate is being provided with a supply voltage V_{cc} . P-channel transistors 26 and 27 and N-channel transistor 28 configure a level conversion circuit, and convert the output of NAND gate 24 to a high voltage V_{pp} level to generate write control signal/WD1.

[0043] Figure 3 is a timing chart showing the operation of the flash EEPROM shown in Figures 1 and 2. Referring to Figures 1 through 3, the operation of the EEPROM in this example will be described. The read and erase operation is the same as in the conventional case, so an explanation of this will be omitted. The operation of writing data “0” to memory cells 111 and 113 will be described. First, in response to write control signal/WE, command decoder 13 will output program control signal/PRC (“L” level). Also, in response to data that has been inputted from the outside, input/output buffer 9 will activate write circuits 71 and 72. The activated write circuit 71 will output a signal at the supply voltage V_{cc} level. On the other hand, write circuit 72 will output a signal at the high voltage V_{pp} level. Output/WD of write circuit 71 will be delayed by delay circuit 21 and will be subjected to a high pressure V_{pp} level over the delay period. Output/WD1 of delay circuit 21 will be at the V_{pp} level and will be later than output/WD2 of delay circuit 72. On the other hand, at the same time as the rise of output/WD2 of write circuit 72, the address signal selects Y gates 211 and 221 and word line 301 via Y decoder 5 and X decoder 4. As a result, memory cells 111 and 113 will be selected. A high voltage V_{pp} will be applied to the selected memory cell 113 through write transistor 224. Memory cell 111 will be subjected to high voltage V_{pp} over a relay period by delay circuit 21. In this way, the write current to the memory cell that was selected during the initial write can be suppressed.

[0044] Figure 4 is a schematic diagram that illustrates another example of embodiment of the present invention, while Figure 5 is a timing chart illustrating the operation of the EEPROM shown in Figure 4.

[0045] In Figure 4, the EEPROM includes resistance 29 and capacitance 31 to delay the rise of the output of writing circuit

71, and resistance 30 and capacitance 31 to delay the rise of the output of writing circuit 72.

[0046] The operation of the EEPROM of Figure 4 will be described next with reference to Figure 5. The output of writing circuits 71 and 72 rises slowly according to the respective time constants determined by resistance 29 and capacitance 31, and resistance 30 and capacitance 32. Therefore, the output voltages of write transistors 214 and 224 also gradually increase to V_{pp} levels. This slow rising high voltage V_{pp} can be applied to multiple memory cells in order to suppress the current flowing at the start of the programming.

[0047] In the example of Figure 4, the rise time of write transistors 214 and 224 was increased, but the rise time of the output of Y decoder may also be increased.

[0048] Figure 6 is a schematic diagram illustrating the third example of embodiment of the present invention. In Figure 6, the EEPROM is provided with oscillator 33, first control circuit 34, and second control circuit 35. Oscillator 33 generates clock signal S in response to program control signal/PRC. First control circuit 34 is activated by an output (“H” level) of write circuit 71 in order to generate first control signal S1 for controlling write transistor 214 in response to clock signal S that was generated by oscillator 33. Second control circuit 35 is activated by the output of write circuit 72 and generates second control signal S2 for controlling write transistor 224 in response to clock signal S that was generated by the oscillator. The first and second control circuits 34 and 35 are configured such that the periods for outputting the V_{pp} levels will not overlap each other. As a result, it will be possible prevent the high pressure V_{pp} from being applied to multiple memory cells simultaneously.

[0049] Figure 7 is a detailed circuit diagram of oscillator 33, first control circuit 34, and second control circuit 35 as shown in Figure 6. In Figure 7, oscillator 33 includes N-channel transistor 38, inverters 39 to 42, P-channel transistor 43, P-channel transistor 44, and N-channel transistor 45. N-channel transistor 38 and P-channel transistor 43 are connected such that each gate receives program control signal/PRC and will activate the oscillator only during writing. Program control signal/PRC that passed through N-channel transistor 38 is delayed by inverters 39 to 42, and is then provided to inverter 100, which is constructed of P-channel transistor 44 and N-channel transistor 45. Because the output of inverter 100 is returned to the input of inverter 39, clock signal S is oscillated at this return loop and oscillates at a predetermined frequency.

[0050] First control circuit 34 includes delay circuit 101 that delays the clock signal from oscillator 33, NAND gate 50 that receives the output of delay circuit 101 and the output of write

circuit 71, transistor 51 for high voltage cutting, and level conversion circuit 102. Delay circuit 101 includes series-connected inverters 46 and 47, NAND gate 48, and inverter 49. One input of NAND gate 48 is provided with a delayed clock signal and the other input is provided with a non-delayed clock signal. Level conversion circuit 102 includes P-channel transistors 52 and 53, and N-channel transistor 54, similar to the level conversion circuit described in Figure 2.

[0051] Second control circuit 35 includes inverter 55 that reverses the clock signal from oscillator 33, delay circuit 103 that delays the output of inverter 55, NAND gate 60 that receives the output of delay circuit 103 and the output of write circuit 72, transistor 61 for high pressure cutting, and level conversion circuit 104. In other words, the difference between second control circuit 35 and first control circuit 34 is the fact that the clock signal is inverted by inverter 55.

[0052] Figure 8 is a timing chart of the EEPROM shown in Figures 6 and 7. While referring to Figures 6 through 8, the operation of the third example of embodiment will be described. The operation of writing data "0" to memory cells 111 and 113 will be described in this case as well. First, in response to the write control signal/WE input from the outside, internal program control signal/PRC will fall. As a result of the falling of program control signal/PRC, transistor 38 will be turned OFF and transistor 39 will be turned ON. As a result, oscillator 33 will be activated, generating clock signal S. The generated clock signal S will be provided to first control circuit 34 and second control circuit 35. The clock signal that was provided to first control circuit 34 will be applied to one input terminal of NAND gate 50 after being delayed by delay circuit 101. The clock signal that was provided to second control circuit 35 will be applied to delay circuit 103 after being reversed by inverter 55. Delay circuit 103 delays the inverted clock signal and then provides it to one input terminal of NAND gate 60. The other input terminals of NAND gates 50 and 60 will be provided "H"-level signals from write circuits 71 and 72, and output "H"-level signals if one input terminal is given an H-level clock signal. The signals output from NAND gates 50 and 60 are converted to Vpp level control signals S1 and S2 by level conversion circuits 102 and 104. Also, depending on the address that was entered at the same time, output Y2 of the Y decoder and output WL1 of the X decoder will also be at the Vpp level. In this way, signal BL11 that may be provided to bit line 311 and signal BL21 that may be provided to bit line 321 will be controlled by

a clock that does not overlap each other. Thereafter, with the end of the write cycle, program control signal/PRC becomes the "H" level, oscillator 33 will be deactivated, and the output of the write pulse will stop.

[0053]

[EFFECT OF THE INVENTION] As described above, according to the present invention, by varying the timing of the write voltage supply of multiple write voltage supply means, it will be possible to suppress the peaks of write current flowing to the source line, making it possible to reduce power consumption.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIGURE 1] This is a schematic diagram showing an example of embodiment of the present invention.

[FIGURE 2] This is a circuit diagram showing the details of the delay circuit in Figure 1.

[FIGURE 3] This is timing chart of the EEPROM shown in Figure 1.

[FIGURE 4] This is a schematic diagram showing another example of embodiment of the present invention.

[FIGURE 5] This is a timing chart of the EEPROM shown in Figure 4.

[FIGURE 6] This is a schematic diagram showing the third example of embodiment of the present invention.

[FIGURE 7] This is a circuit diagram showing details of the oscillator, first control circuit, and second control circuit shown in Figure 6.

[FIGURE 8] This is a timing chart of the third example of embodiment.

[FIGURE 9] This is a cross-sectional view of a memory cell that may be used in the EEPROM.

[FIGURE 10] This is an overall block diagram of EEPROM.

[FIGURE 11] This is a circuit diagram of the area surrounding the conventional memory cell array.

[FIGURE 12] This is a timing chart showing the operation of the circuit in Figure 11.

[EXPLANATION OF REFERENCES]

101 Memory cell array

4 X decoder

5 Y decoder

21 Delay circuit

214, 224 Transistor

71, 72 Write circuit

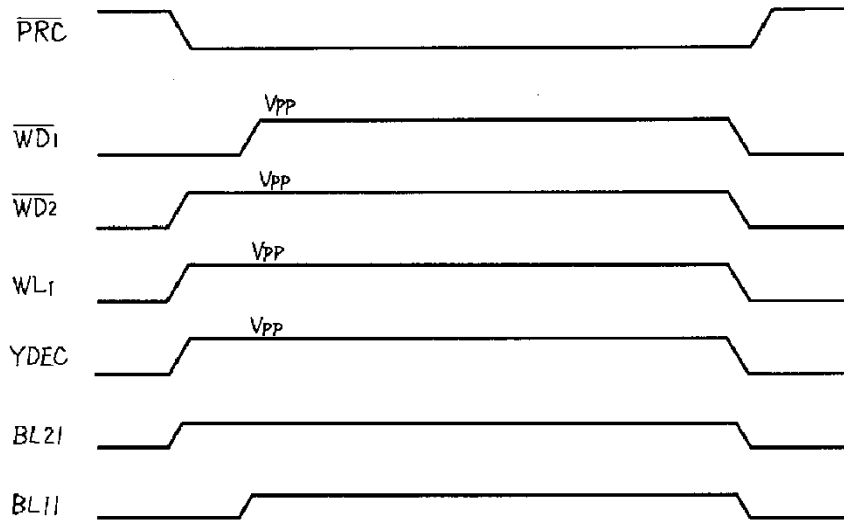
33 Oscillator

34 First control circuit

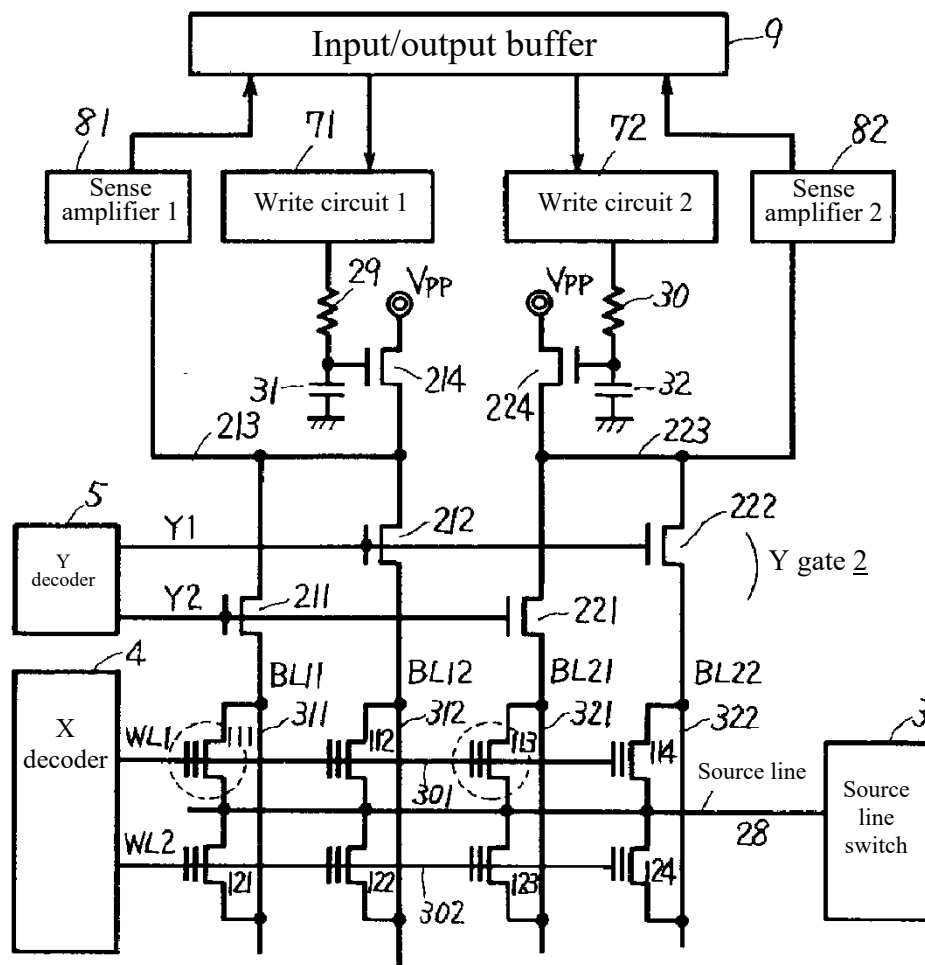
35 Second control circuit

The diagram illustrates a memory array (1) with two columns of memory cells. Each column contains two memory cells, BL11 and BL12 in the first column, and BL21 and BL22 in the second column. The array is connected to an input/output buffer (9) via sense amplifiers (81, 82) and write circuits (71, 72). The sense amplifiers are connected to the bit lines (BL11, BL12, BL21, BL22) and the source line switch (3). The write circuits are connected to the word lines (WL1, WL2) and the source line switch (3). The array is also connected to a Y decoder (5) and an X decoder (4). The Y decoder is connected to the bit lines (BL11, BL12, BL21, BL22) and the source line switch (3). The X decoder is connected to the word lines (WL1, WL2) and the source line switch (3). The array is connected to a source line switch (3) which is connected to a source line (28). The array is also connected to a source line switch (3) which is connected to a source line (28). The array is connected to a source line switch (3) which is connected to a source line (28). The array is connected to a source line switch (3) which is connected to a source line (28).

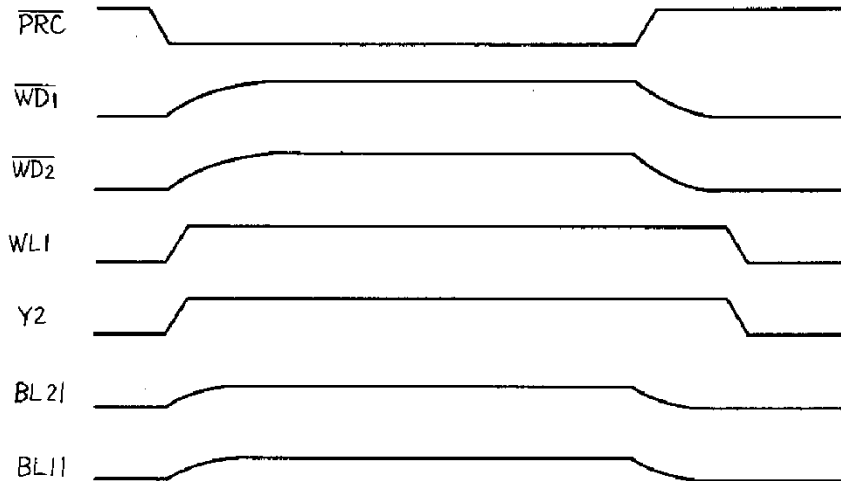
[FIGURE 3]



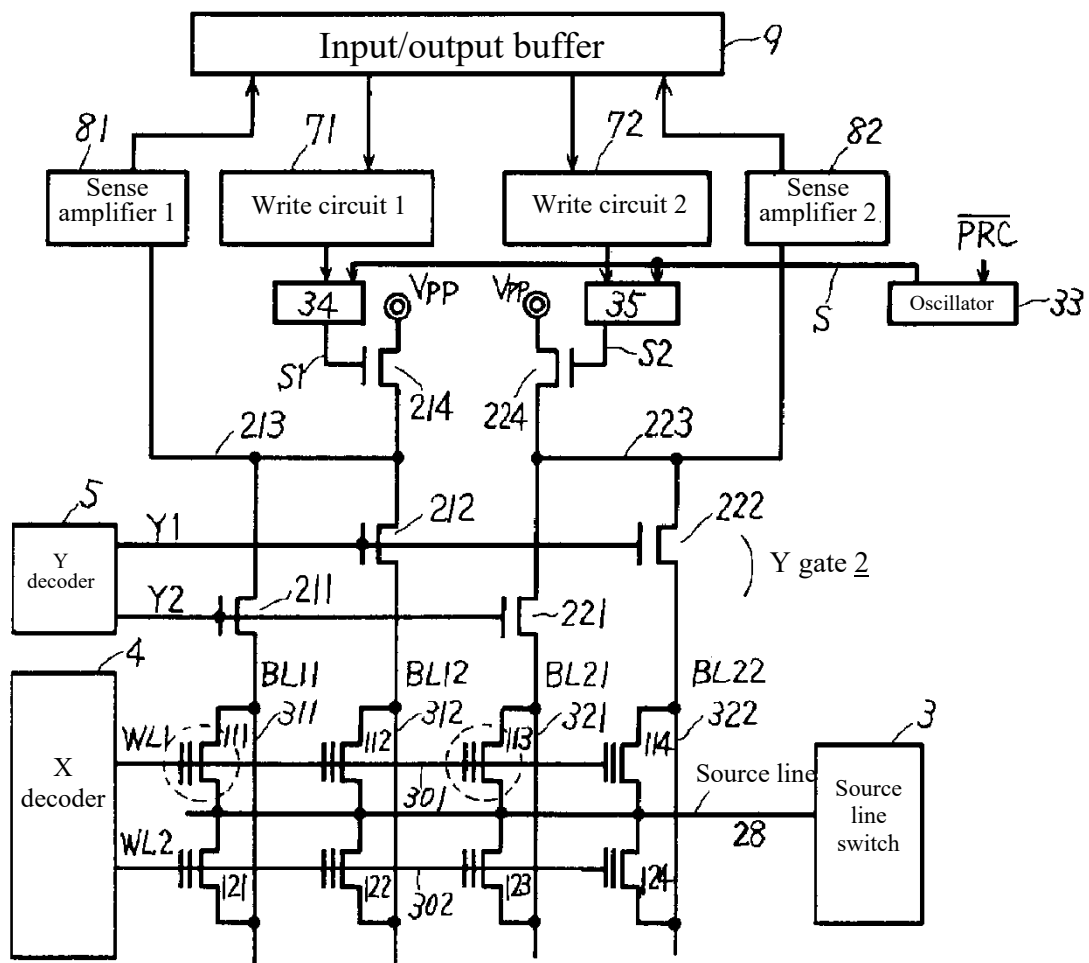
[FIGURE 4]



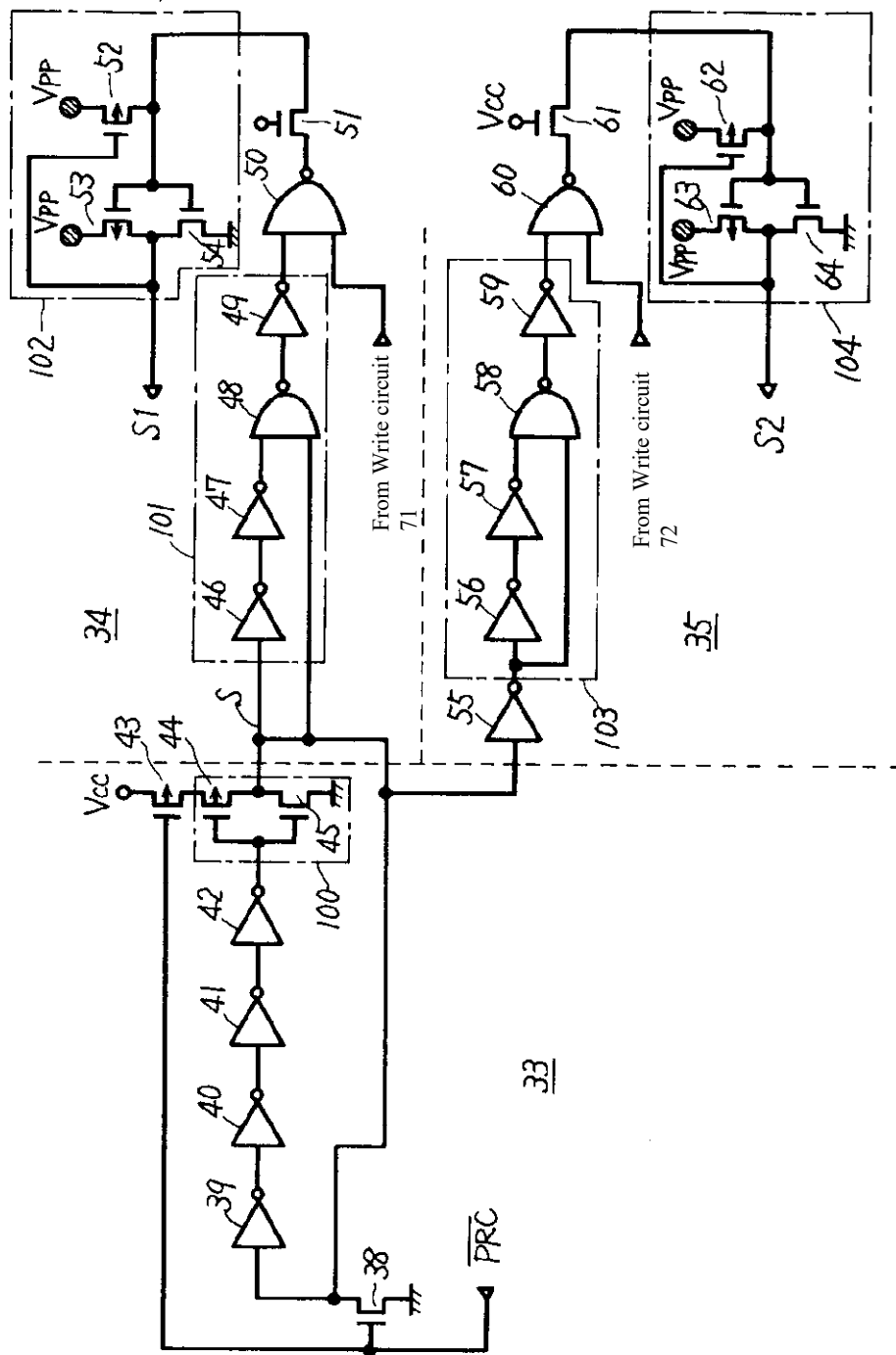
[FIGURE 5]



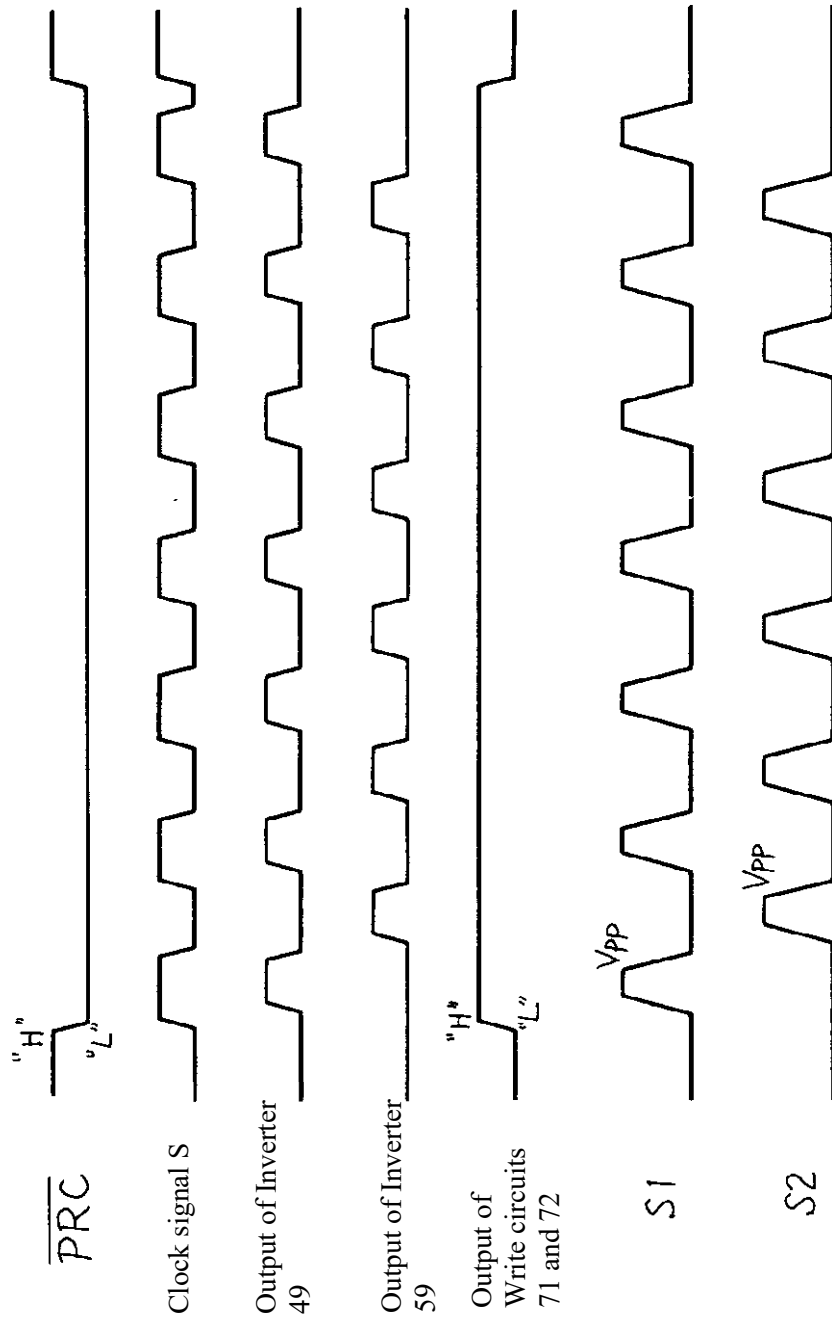
[FIGURE 6]



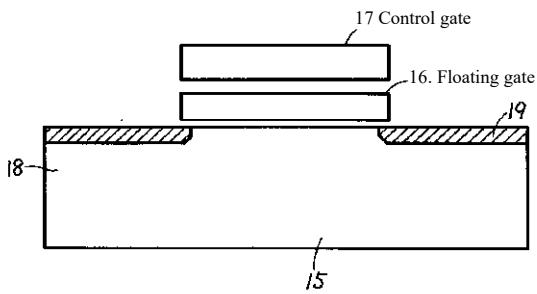
[FIGURE 7]



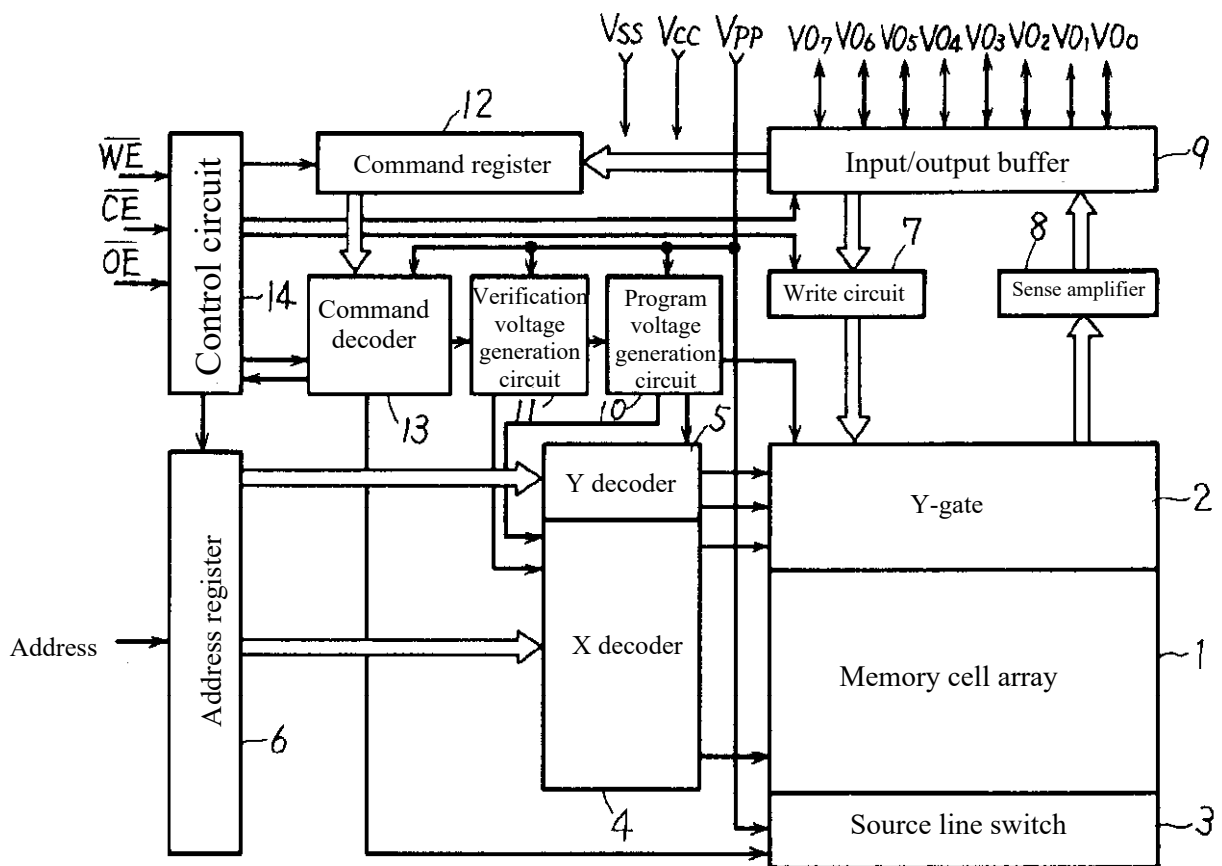
[FIGURE 8]



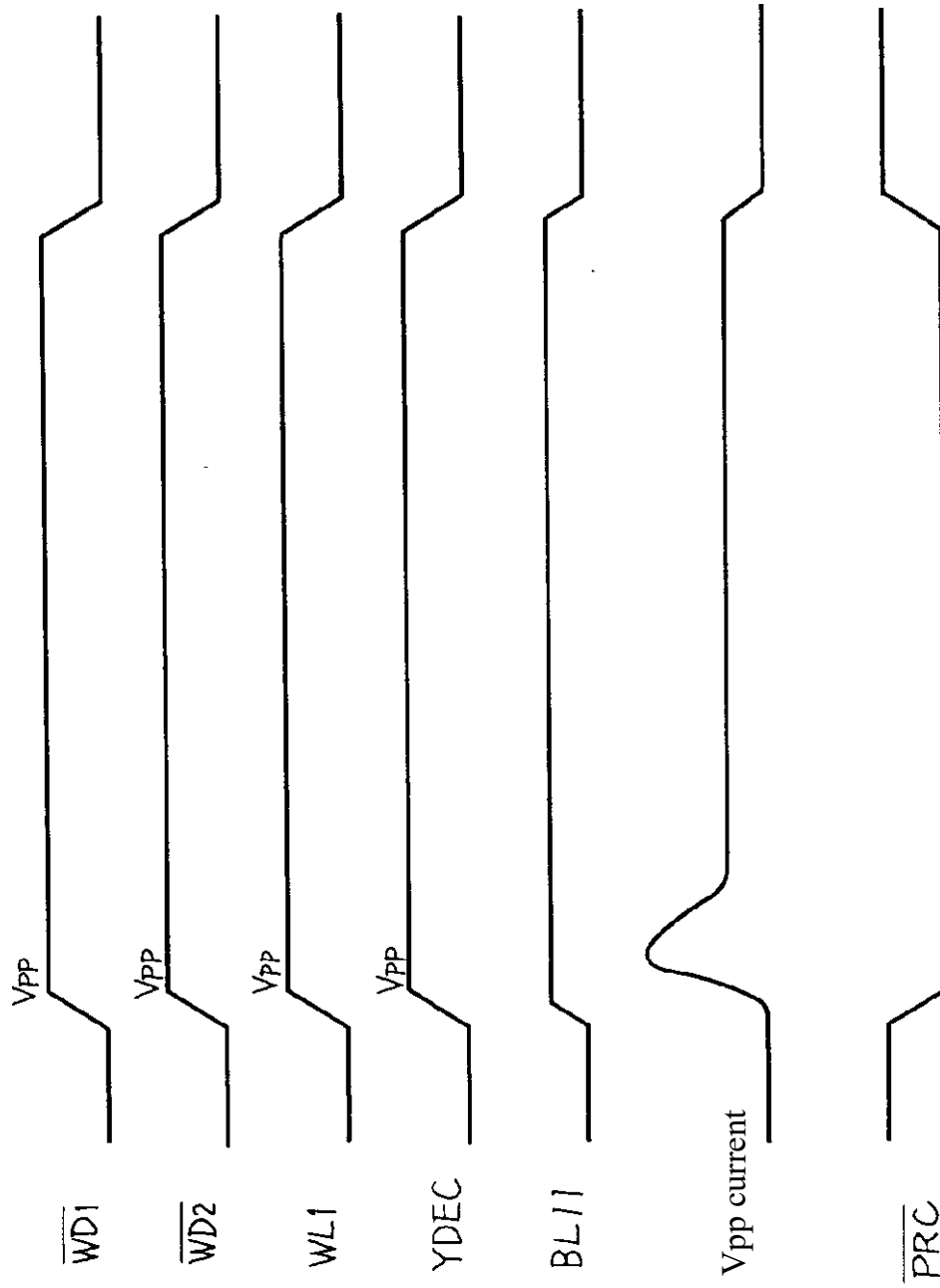
[FIGURE 9]



[FIGURE 10]



[FIGURE 12]





TRANSPERFECT

I, STEPHANIE BOX, hereby certify that I am competent to translate from Japanese to English and that the attached translations are, to the best of my knowledge and belief, a true and accurate translation of the documents entitled below from Japanese to English.

I hereby further declare that all statements made herein of my own knowledge are true and that all statements made on the information and belief are believed to be true; I declare under penalty of perjury that the foregoing is true and correct, and understand that willful false statements and the like are punishable by fine or imprisonment, or both pursuant to 18 U.S.C. 1001.

- JP_H0562484_A

Stephanie Box

June 4, 2025
Date