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To cite this version:

Sehmi Saad, Fayrouz. Haddad, Aymen Ben Hammadi. Impact of multi-finger MOSFET geometry on the electrical performance of RF circuits. Microelectronics Reliability, 2022, 129, pp.114445. 10.1016/j.microrel.2021.114445 . hal-03604352

HAL Id: hal-03604352

https://hal.science/hal-03604352v1

Submitted on 7 Mar 2023

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Impact of multi-finger MOSFET geometry on the electrical performance of RF circuits

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***Abstract*—The increasing demand of low-cost, low-power and high-efficiency integrated systems is making more complex to design radiofrequency (RF) analog circuits. Using multi-finger MOSFETs is an attractive technique to optimize the circuit performances. It reduces the silicon area, the gate resistance and parasitic capacitances compared to the single finger MOSFET, which mainly impact the high frequency and noise performances. However, selecting the optimal number of fingers remains a challenging issue. This paper investigates the number of fingers (*nf*) influence on the transistor parameters and assesses its effect on several key functions in RF transceivers. The study focuses specially on the obtained performances of civil RF circuits, implemented in 130 nm CMOS technology, as a function of *nf*. First, design of a differential RF bandpass filter is presented. The results show that using multi-finger MOSFETs leads to reductions in chip area by 66.5%, in power consumption by 15% and in noise figure by 43% with an improvement in linearity and frequency range compared to the conventional approach. Then, an inductorless LC-VCO and an LNA operating around 2.4 GHz have been designed using three different configurations depending on *nf*. Obtained results display an improvement in the area, power gain, frequency and noise performances by applying the multi-finger optimization, and show that keep increasing *nf* can degrade the stability, linearity and power consumption. The proposed circuits are also tested through Monte Carlo simulations confirming their robustness to process and mismatch variations. Detailed analytical comparison between the different proposed circuits and configurations of *nf* proves that the MF technique is reliable when *nf* is inferior to 5.**

Keywords*— *Multi-finger; MOSFET, RFIC; noise; power consumption; area.

1. INTRODUCTION

In the last decades, CMOS integrated circuit (IC) design has known several technological advances conducted with a constant technology downscaling [1]. Size of transistors have been shrinking exponentially and subsequently the continuous miniaturization of devices enters the nanoscale regime. Notably, the challenges associated with using conventional Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) have increased. Because of performance limitation and parameter variation due to gate leakage (GL) and short-channel effects (SCEs), new materials, structures and manufacturing techniques against electrical performance effects as well as reliability characterization have been vastly investigated in literature [2-5].

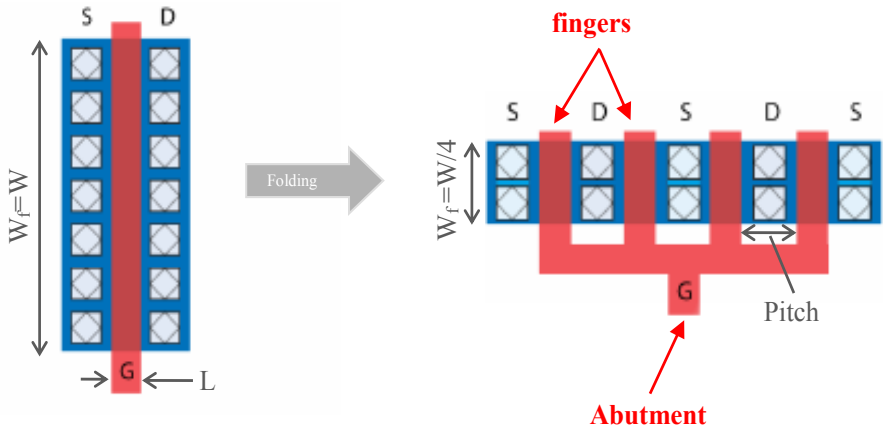
Modifications of subtract profiles and usage of different insulator materials, i.e. Silicon-On-Insulator (SOI) [6], Silicon Carbide (SiC) [7], Silicon-On-Sapphire (SOS) [8], Carbon Nanotube [9,10], Germanium [11], Silicon-Germanium [12] High-k material [13], are examples of well-known optimization transistor techniques. However, besides its high fabrication cost, this technique leads to high-grade electrical performance, in the production of multi-function MMICs for space and aerospace applications, where low voltage and high frequencies are required.

On the other hand, new possible fabrication structures of transistor's gate such as FinFET [14,15], Double Gate (DGFET) [16], Multi Gate (MuGFET) [17], Ion Sensitive Field Effect (ISFET) [18], Gate-All Around (GAA) [19], Ultra-Thin Body (UTB) [20], Ultra-Thin Body and Buried oxide (UTBB) [21], Multi-Bridge Channel FET (MBCFET) [22], Junction less MOSFET [23], Tunnel Field-Effect Transistor (TFET) [24,25], Organic Thin-Film transistors [26], Nanowires transistors [27] are eminently pertinent to the development and realization of the new RF transistor generation for communication device. The general goal of each technique

is to enhance gate control of the channel charge and to reduce leakage current. For the instance, majority of these techniques have been shown to be effective as a promising technology to mitigate degradation due to short-channel effects (SCEs) and gate leakage [28]. New manufacturing processes such as plasma [29] and photolithograph [30] are other approaches to implement high performant MOSFET. They offer many advantages, including low thermal budget, low fringing gate capacitances and simplified processing. Nevertheless, further study is needed on variability and reliability characterization, for instance. For example, in plasma process, silicon or other material surfaces of transistor is induced by high-energy ion bombardment incident [31]. Hence, a lot of effort has been made by researchers in the recent years to experience new materiel on emergent structures, such as GaN SOI FinFET [32], high-k gate SOI FET [33], S/D junction less SiNW MOSFET [34], etc. to boost the IC electrical performance.

Drawing layout techniques for an efficient IC design is another promise solution still unexplored by the semiconductor foundries [2]. Namely, PN Junctions Engineering between the Drain/Source and the Channel Regions, the technique consists on changing the classical rectangular form of the gate to non-standard geometries such as ellipsoidal, circular, hexagonal, octagonal, fish and wave style [2]. In contrast to traditional transistors gate placement approaches, more geometrical design variables concerning longitudinal corner and parallel connection of transistors are added to other unknown electrical effects: new parasitics elements, leakage current pattern… Then, despite the cost manufacturing process still unchanged compared to the current planer transistor, the problem's complexity is raised and analog/RF designer becomes aware of the design tradeoffs.

Other design strategies have been expanded to maximize the RF characteristics of CMOS transistor as well as the noise reduction among series connections and multi-gate stacked transistors [35,36]. In this latter, connecting transistors in series with multiple gates allows a high breakdown voltage and a compact unit cell, but needs a careful implementation to avoid extra parasitic elements that can cause problems in matching and stability. An alternative approach consists in using multi-finger (MF) transistors that can simultaneously decrease the gate resistance and the capacitance parasitics, which directly affect the RF circuit performances [37,38]. In fact, reducing the gate series resistance impacts the device's figure-of-merit such as noise figure, maximum oscillation frequency, cut-off frequency, etc. [39-41]. However, the transistor properties can change depending on the current direction [42]. Therefore, extra care must be taken when trying to achieve good matching [43]. The multi-finger layout of an RF transistor consists in splitting the gate into multiple fingers in parallel, as shown in Fig. 1. The width of the transistor is divided by the number of fingers (*nf*) inducing a smaller area occupation and a better matching compared to the single-finger (*SF*) configuration.



(a) (b)

Fig. 1. Example of (a) a single-finger (SF), and (b) a multi-finger (MF) transistor layouts

In this work, the impact of number of fingers on the transistor parameters (R_g, f_{max}, f_T, g_m) and performances (noise, area, power consumption) is investigated on 130 nm CMOS technology. Afterward, MF transistors have been applied to implement the essential functions of the RF front-end receiver. Such an ample study of the effect of MF MOSFETs is first time proposed as the known of authors, determining the trade-offs to be considered on

the design optimization of several main RF circuits (RF filter, Voltage-Controlled Oscillator VCO, Low-Noise Amplifier LNA).

The paper is organized as follows. Section II investigates the influence of multi-fingers on a single MOSFET features. Its application on the design of a differential RF bandpass filter is presented in section III. Then, implementations of an inductorless LC-VCO and an LNA using the multi-finger technique are presented in section IV and V, respectively. The obtained results are discussed for each RF circuit exploring the effect of multi-finger MOSFET on the design optimization. Also, Monte Carlo analysis has been conducted to consider the robustness and reliability of the circuits. Conclusions are drawn in Section VI.

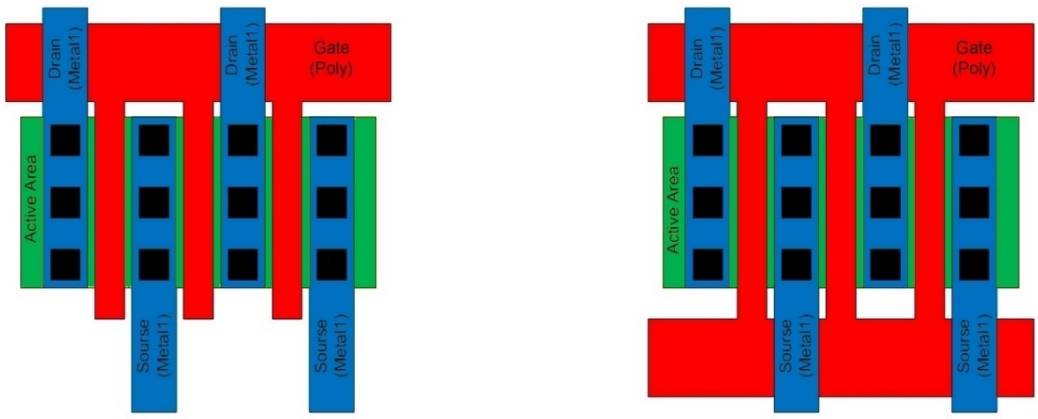
2. Multi-finger impact on a single MOSFET

In this section, a brief study on the straightforward concept of multi-gate stacked MOSFET, is presented followed by impact of the number of fingers on different electrical parameters for conventional MF layout.

2.1. Basic concept of multi-gate MOSFET

In CMOS integrated circuit (IC) design, the gate layout is an essential feature that should be considered. For RF applications, MOS transistor with large gate dimensions is needed to meet the required transconductance together with high frequency, low power and low noise. But, large transistor cannot be arranged with simple gate because of performance degradation and technological restrictions [44]. Therefore, special layout approaches have to be deployed.

The most effective technique in RF IC design is the multi-finger gate layout [44,45] (See Fig. 2).



(a) (b)

Fig. 2. Single connection (a) and double connection (b) gate layout for MOSFET transistor

Transistors are designed in an interdigitated configuration in which the total channel width (W) is divided by the number of fingers, as illustrated in Fig. 3. All the gates, sources and drains are connected among themselves to make a single transistor. Thus, W can be expressed as follows [46]:

$$W = W_f . n_f \tag{1}$$

where W_f is the channel width of the transistor after division and n_f is the number of fingers.

This results in a reduction of the effective area of the multi-finger transistor, as depicted in Fig. 4. For example, the area of a transistor with 2 fingers is lower by 22% than a single-finger one. Also, area diminution is about 35% for $nf = 7$.

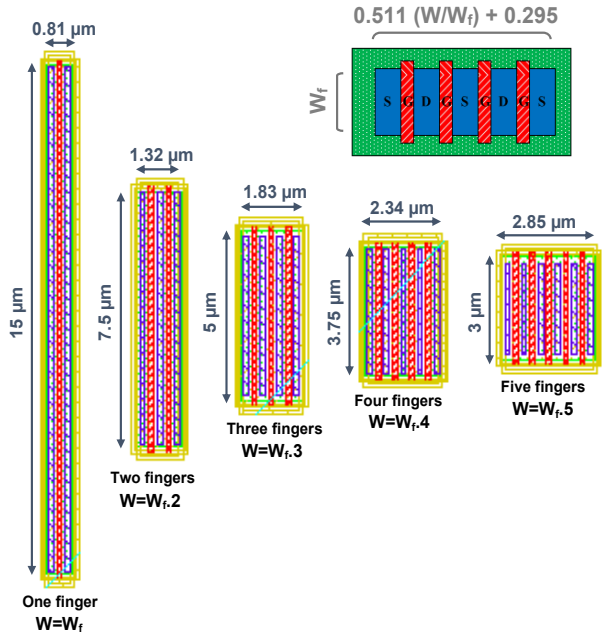


Fig. 3. Variation of *W* versus the number of fingers: W=15 µm.

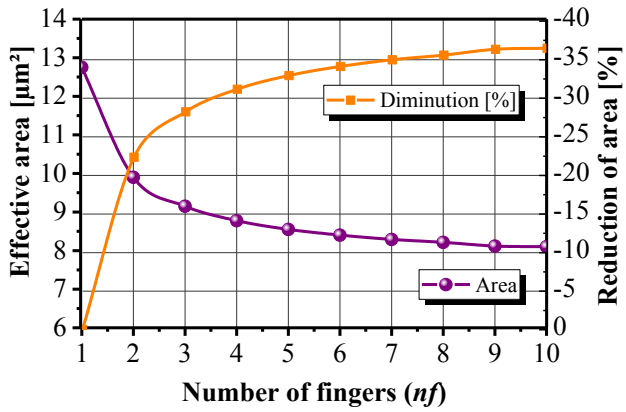
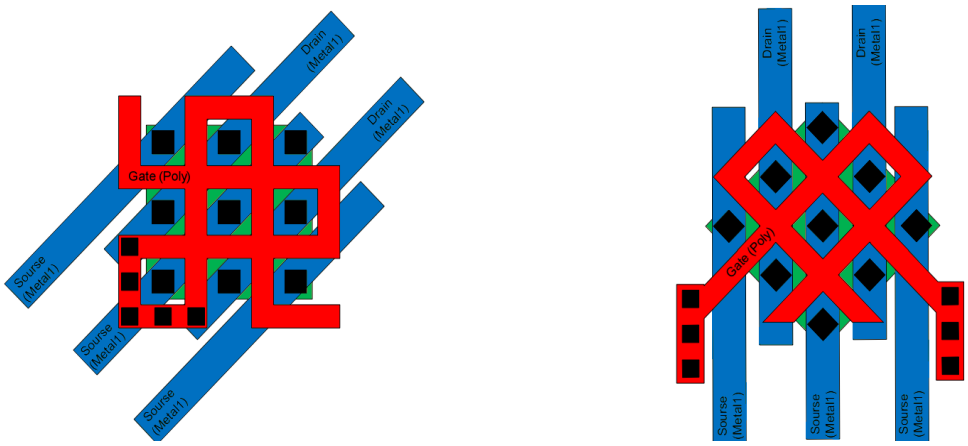


Fig. 4. Area variation versus the number of fingers

Another interesting layout structure, known as Waffle (WF) structure, has been presented in [47] and [48]. It consists in arranging the MOSFET gate fingers in a square grid topology. Two implementation style of the WF structure, called Manhattan Gate (MG-WF) and Manhattan Interconnect (MI-WF) are depicted in Fig. 5. Each square contains a single contact, while drain and source metallization is a series of diagonal stripes [49].



(a) (b)

Fig. 5. Manhattan Gate (a) and Manhattan Interconnect (b) implementation for MOSFET transistor layout.

In [50], a comparative analysis between the WF and MF layout structures, achieved for a given device area, is discussed. It shows that the waffle layout has a better packing density and a smaller parasitic capacitance than the MF layout. Although the compactness of the WF layout, it is not a known gate structure in CMOS RF design and has complex modeling issues especially in high frequencies [51]. Besides, using the multi-finger technique results in the gate resistance reduction [52] and offers a simple design. But, even though access resistances are reduced, the coupling between the relatively wide metal lines leads to capacitive coupling effects and high parasitic capacitances [45,48,53-54]. Hence, a judicious trade-off between the transistor parameters and number of fingers should be considered in RF circuit design.

2.2. Multi-finger effects on the MOSFET parameters

In the following, impacts of the number of fingers on high frequency and noise parameters on a single transistor are investigated. The next extracted parameters are derived through simulations of an NMOS transistor in 130 nm CMOS technology, at the biasing conditions $V_{gs}=V_{dd}/2=0.6$ V and $V_{ds}=1.2$ V. The transistor channel length (L) is set constant to 0.13 µm.

- **f_T and f_{max}**

It is known that, as the operating frequency is high, intrinsic components, such as capacitances, of the transistor become significant leading to a limit of operation. The most important frequencies characterizing the RF performance of MOSFETs are f_T, the cut-off frequency of unity current gain, and f_{max}, the maximum oscillation frequency or frequency of unity power-gain [55]. Assuming that the drain-bulk capacitance C_{db} is neglected, the f_T and f_{max} can be estimated as [56]:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{2}$$

$$f_{max} \approx \frac{1}{2\sqrt{2\pi}}\sqrt{\frac{f_T}{R_g C_{gd}}} \approx \frac{1}{4\pi}\sqrt{\frac{g_m}{R_g C_{gd}(C_{gs}+C_{gd})}} \tag{3}$$

where C_{gs} and C_{gd} are the gate-source and gate-drain capacitances, respectively, g_m is the intrinsic transconductance and R_g is the gate resistance.

Both f_T and f_{max} depend on bias conditions and device geometry (nf and W/L). To validate this, an NMOS transistor has been simulated while varying its width and number of fingers. Fig. 6 shows the obtained f_T and f_{max} characteristics versus nf, and their evolution relative to the initial value with single finger (dotted curves). As it can be noted, both f_T and f_{max} increase when decreasing W, for a fixed nf value. For example, when using two fingers, f_T is equal to 60 GHz and 75 GHz, for W = 120 µm and 15 µm, respectively. In fact, considering the velocity saturation region, and assuming that the short-channel effect does not change much the total capacitance ($C_{gs}+C_{gd}$), it can be derived that this latter is proportional to the gate width and length of the transistor [56]. Hence, f_T, and so on f_{max}, is inversely proportional to W.

Besides, both f_T and f_{max} increase when increasing nf. For example, for W = 15 µm, using 10 fingers have a higher f_T and f_{max} by 39% and 42%, respectively, compared to the single finger configuration. But, the percentage of evolution of each frequency value is higher when using narrow transistor widths. Also, the variation of the number of fingers has a bigger impact on f_T and f_{max} for the smallest values of nf, essentially $nf \leq 10$. After this value, increasing nf does not change the frequencies which remain almost constant around their maximal values.

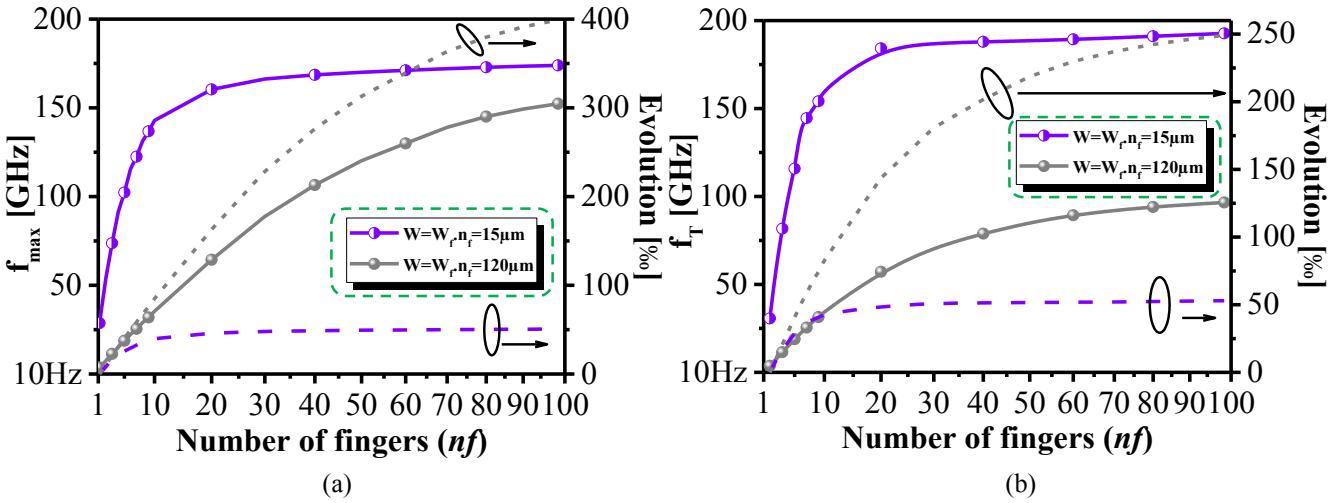


Fig. 6. Effect of nf on (a) f_{max} and (b) f_T characteristics for different widths

- ***R_g, noise and g_m***

There is a trade-off in the layout of RF MOSFETs between the values of R_g and intrinsic capacitances [57,58]. R_g can be approximately modelled by:

$$R_g \approx R_{sch}\frac{W}{L}\frac{1}{3.N_{con}^2.nf} = R_{sch}\frac{Wf}{L}\frac{1}{3.N_{con}^2} \tag{4}$$

where R_{sch} is the resistance of poly layer (gate layer) and N_{con} is the gate contact number (either 1 or 2) [59-61]. Since R_g is inversely proportional to *nf*, increasing *nf* will result in a reduction of the gate resistance for a constant *W/L*. The extracted result, given in Fig. 7(a), illustrates the influence of the number of fingers on R_g for different width values. For example, for W = 15 µm, it shows that resistance R_g decreases from 360 Ω to 19 Ω as the number of fingers increases from 1 to 6. Also, increasing W leads to an increase of R_g as given by Eq. (4). It can be noted that the variation of R_g versus the number of fingers has the same evolution when changing W, and that it is more important for small *nf* values.

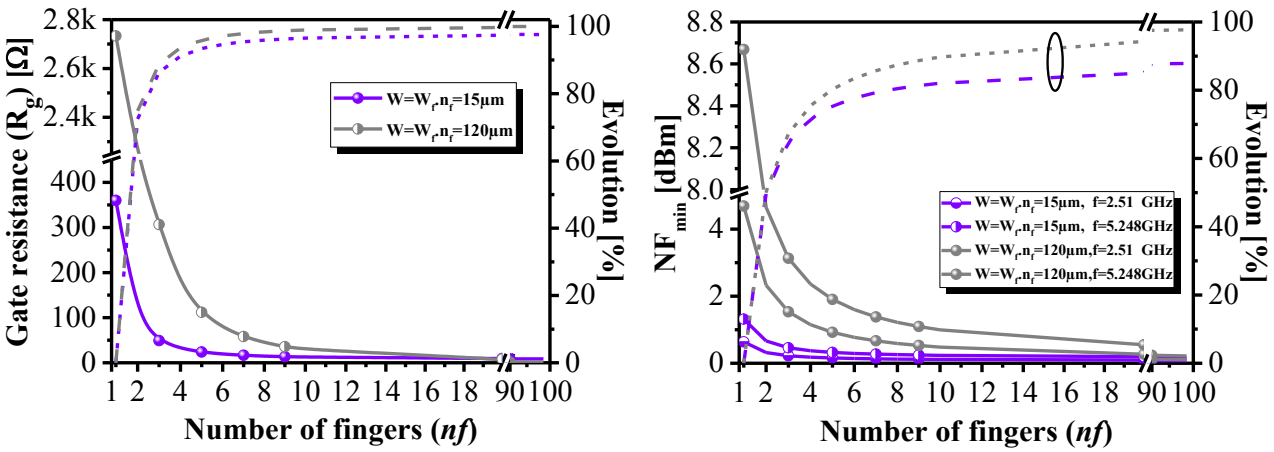
Therefore, the current distribution in multi-finger transistors makes it possible to decrease the gate resistance, which is valuable for RF and noise performance [62]. In order to evaluate the noise of a MOSFET, the function derived from the small signal model is determined by integrating all the sources of noise. The minimum noise factor can be expressed by:

$$NF_{min} = 1 + K_f\frac{f_{max}}{f_T}\sqrt{(R_g + R_s)g_m} \tag{5}$$

where K_f is the Fukui coefficient and R_s is the substrate resistance [63].
The obtained equations Eq. (2) and Eq. (5) give:

$$(NF_{min} - 1) = 1 + K_f\omega_{max}C_{gs}\sqrt{\frac{R_g+R_s}{g_m}} \tag{6}$$

Accordingly, the minimum noise factor *NF* can be improved by decreasing R_g. This latter is possible by decreasing the number of fingers as derived previously. Fig. 7(b) presents the variation of NF_{min} versus *nf* for different sets of W and frequencies of operation. The larger number of fingers yield to a lower noise factor. For example, as determined from Fig. 7(b), an NMOS with W = 15µm and operating at 2.51 GHz offers 77% improvement in NF_{min} when increasing *nf* from 1 to 6. Also, the narrower width will engender a lower noise factor. As it can be observed from Fig. 7(b), a 2.51 GHz NMOS using 3 fingers ensures an NF_{min} of 0.22 dB and 1.54 dB when W equals to 15 µm and 120 µm, respectively. Note that, by changing the frequency of operation, the same NF_{min} evolution versus the number of fingers is obtained when using the same width.



(a) (b)

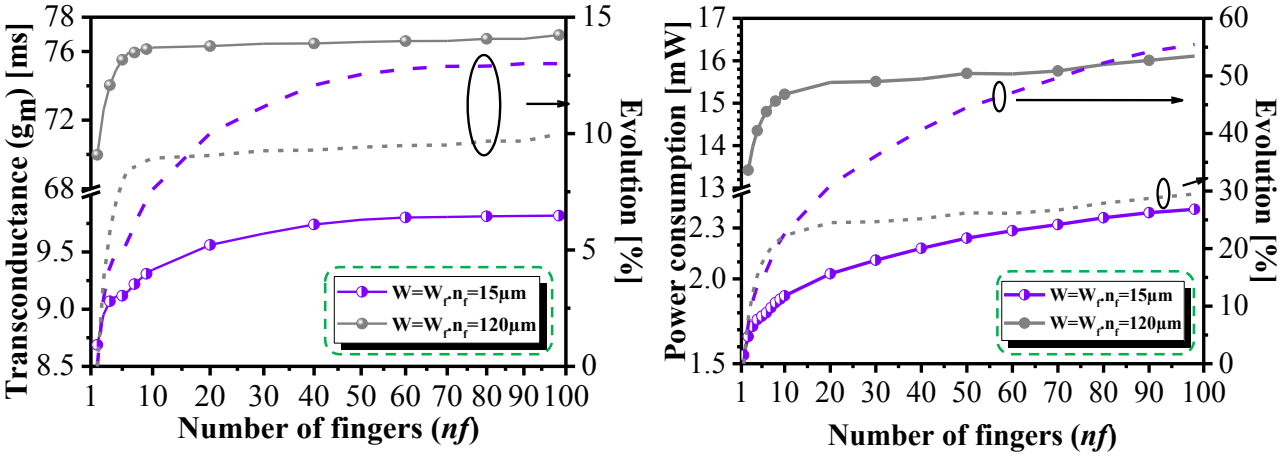
Fig. 7. Effect of *nf* on (a) the gate resistance and (b) the noise figure

In addition, increasing the transconductance g_m can further improve NF_{min} as derived in Eq. (6). Fig. 8(a) depicts the impact of varying *nf* on g_m. It is evident that increasing the number of fingers enhances the transconductance, and subsequently the minimum noise factor is reduced.

Furthermore, power consumption is another important parameter that should be analyzed. Its dependence on the number of fingers is shown in Fig. 8(b) for different *W*. Since the drain current I_D is directly proportional to g_m, which is also dependent on *nf*, I_D should have the same variation as g_m versus *nf*. As suspected, it was found that I_D, and thus the power consumption, increases when increasing the number of fingers (cf. Fig. 8(b)).

Note that large transistors with fixed *nf* provide a higher consumption, as obviously known. Fig. 8(b) indicates an increase of the DC power from 1.9 mW to 15 mW for *W* equals to 15 µm and 120 µm, respectively, for fixed *nf* equals to 10.

It can be concluded that a trade-off is needed during *nf* selection between the power consumption, the noise and high frequency parameters of MOSFETs. Also, this MF approach is not so simple since it presents additional interferences with losses in silicon substrates, which can degrade the RF circuit performances.



(a) (b)

Fig. 8. Effect of *nf* on (a) the transconductance and (b) the power consumption of an NMOS

2.3. Multi-finger effects on the MOSFET self-heating

Electro-thermal analysis is an important issue when multi-finger gate is used in design. Generally, to evaluate the temperature reached inside the junction, Foser model and Cauer model with the physic characteristics of the device are always used to predict thermal stress inside transistor devices [64,66]. To provide a detailed dynamic of the time-dependent current distribution, TCAD simulations, i.e. 2D numerical simulations and 3D finites elements, are recommended for microscopic analysis behavior and heatsink.

In [67], a reliable study for 130 nm MOSFET was proposed by *Meng* et al through an empirical ionization model. Fig. 9 shows a 2D schematic of the architecture of 8-fingers transistor, and its thermal characteristic as a function of current input [67]. The study results show that the lattice temperature is highest near to the central fingers than that outside. At high current levels, the current per each finger consistently decreases as one moves to the outer fingers. Obviously, the thermal effect can be shrunken by increasing the lateral distance between fingers (Finger pitch) [68] and hence a new attention to the influence of transistor geometry and layout on RF transistor becomes important.

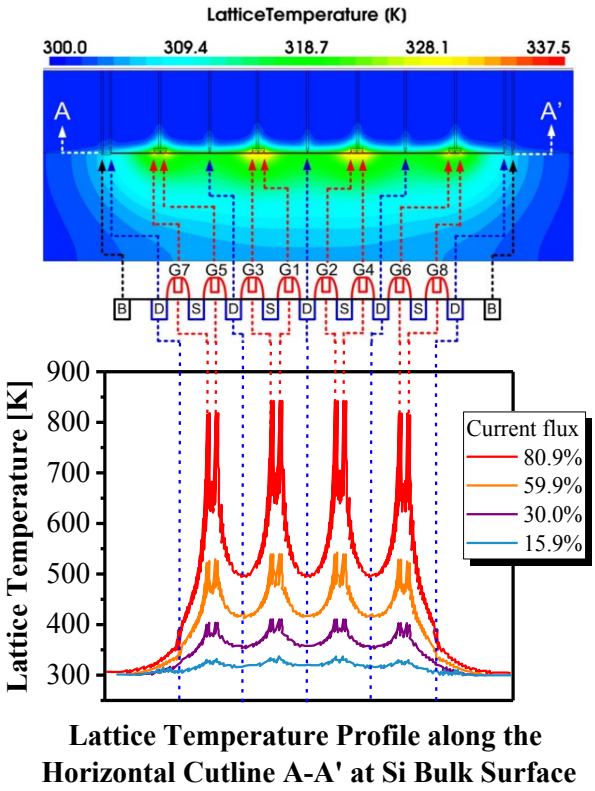


Fig. 9. Temperature distribution profile of an 8-fingers NMOS [67]

In Table 1, we regroup and focus on the impacts of the finger pitch (*P*), the finger width (*W*), and the poly number of fingers (*nf*) on the transistor parameters and its corresponding parasitic resistances and capacitances.

Tab. 1. Summary on the geometry of the finger impact on parasitic elements

Increased parameter	Fixed parameter	R_g	g_m	C_{gd}/C_{gs}	f_T	f_{max}
***nf* (↑)**	***W*, *P***	**Decrease (↓)**	**Increase (↑)**	**High increase (↑↑)**	**Decrease (↓)**	**Decrease (↓)**
***W* (↑)**	***nf*, *P***	**Increase (↑)**	**Increase (↑)**	**Increase (↑)**	**Slightly Increase (↑)**	**Decrease (↓)**
***P* (↑)**	***nf*, *W***	**Increase (↑)**	**Increase (↑)**	**Increase (↑)**	**Slightly decrease (↓)**	**Slightly decrease (↓)**

Based on relations (2) and (3), f_{max} is dominated by resistance R_g and the gate capacitance C_{gd}/C_{gs}, and f_T is dominated by transconductance g_m and C_{gd}/C_{gs}. Thus, under a fixed *W* and *P*, increasing *nf* will reduce R_g and increase C_{gd}/C_{gs}. As a result, f_T decreases with increasing *nf* and this particularly for a large *nf*. The effect on f_{max} becomes more complicated due to the parallel effect of R_g and C_{gs}/C_{gd} which play a conflicting action on f_{max} and hence the maximal frequency will be dependent to the dominant parameter. For example, for a small *W*, the influence of gate capacitance has a higher change than that of the gate resistance, thus resulting in f_{max} decreasing with increasing the number of finger *nf*

On the other hand, under a fixed *nf* and *P*, increasing *W* will increase both the resistance and the capacitance gate to decrease f_{max}. Transconductance g_m is also affected, which increases with *W,* leads to a slightly increase of f_T. Furthermore, under a fixed *nf* and *W*, increasing the distance of the finger pitch *P*, decreases slightly f_T and f_{max}.

3. APPLICATION ON THE DESIGN OF A MF-BASED RF BANDPASS FILTER

After investigating the impact of multi-finger technique on single MOSFET parameters, this approach will be applied to optimize the design of a tunable RF bandpass filter (BPF). Fig. 10 depicts the implemented RF BPF topology along with the dimensions of the components. The circuit is based on a differential tunable active inductor (DTAI) composed of an active part comprising (M_1-M_8 and M_9-M_{16}) and a cross-coupled pair (M_{17}-M_{18}) for loss compensation. The analytical study of such tunable active inductor is detailed in [69,70]. The BPF consists also of a differential input stage (M_{19} and M_{20}) used to deliver the current applied to the DTAI, and a differential output stage (M_{21}-M_{22} and M_{23}-M_{24}) utilized for matching and buffering. Note that the tuning of the center frequency of the filter is ensured through voltages V_{ctr1} and V_{ctr2}, while the quality factor (Q) control is done by V_{bias1}.

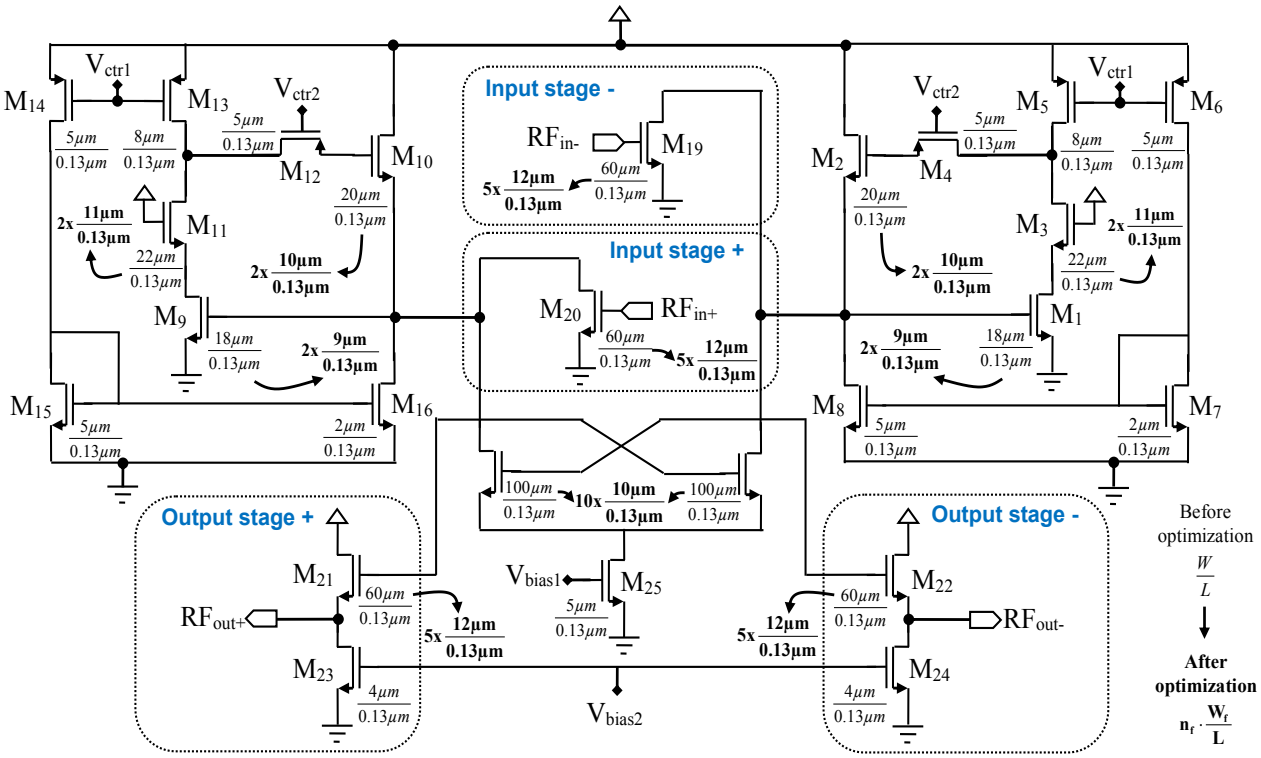


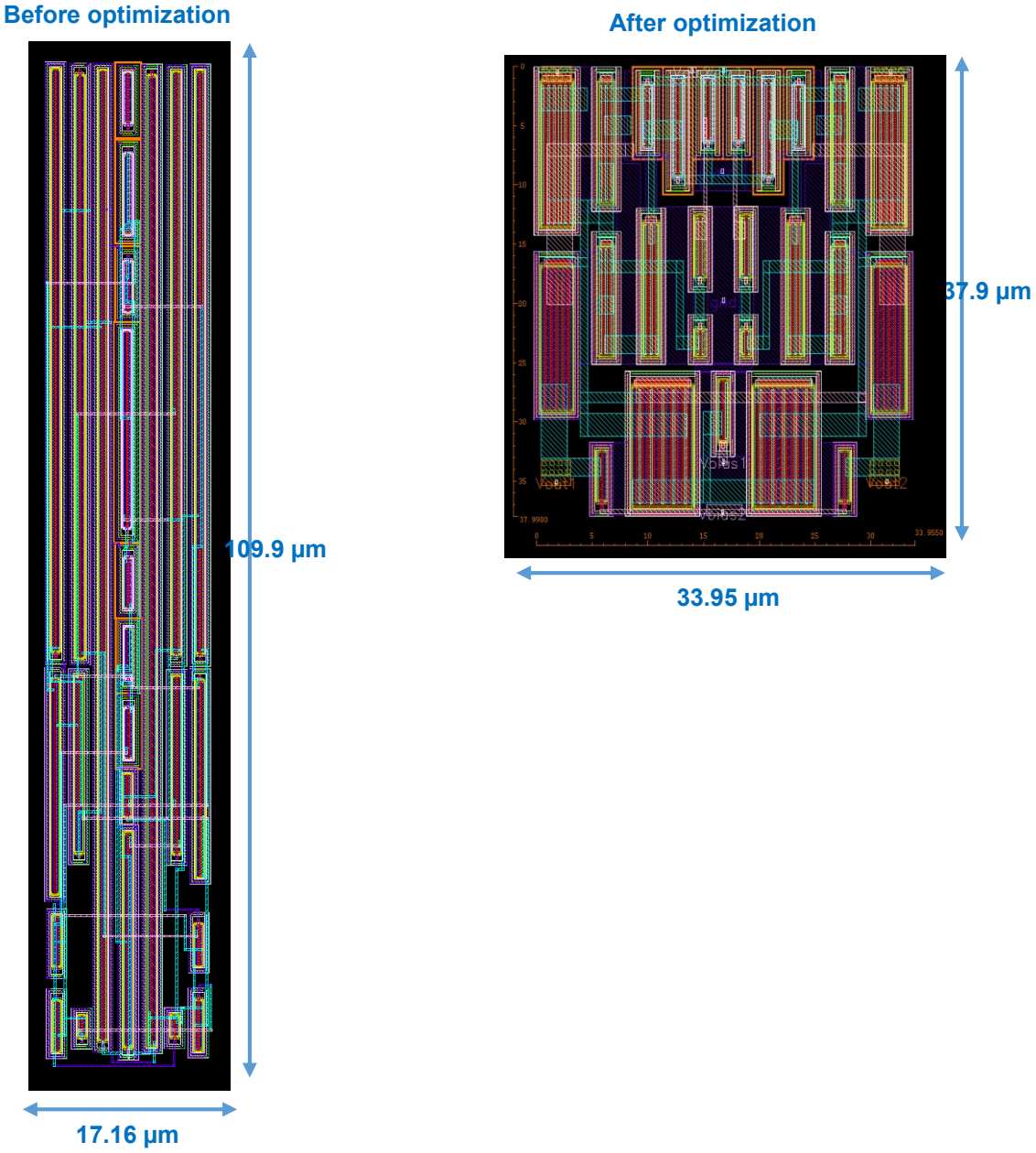
Fig. 10. RF differential bandpass filter using MF transistors

The proposed RF bandpass filter using single-finger and multi-finger MOSFETs has been simulated using Spectre-RF® of Cadence® considering the parasitic elements of the circuit. Hence, the impact of the MF optimization approach on the filter performances could be clearly assessed. The assessment focuses essentially on the area, voltage gain, noise figure, frequency tuning band, linearity and power consumption.

Implemented in 130 nm CMOS technology, distinct layouts of the BPF have been drawn with different aspect ratios. Fig. 11 depicts both optimized and not optimized layouts of the circuit. It is clear that using the multi-finger technique allows a higher layout density by almost 66.5% than that with single finger MOSFETs: 1934 µm² for conventional transistor and 1287 µm² for MF one. In addition to the area enhancement, the arrangement of MF transistors avoids unnecessary parasitic elements.

Furthermore, impact of the MF technique on the filter characteristics has been considered through post-layout simulations. Fig. 12 shows the transmission coefficient S21 response of the reconfigurable BPF with and without the multi-finger optimization. Note that as the control voltages V_{ctr1} and V_{ctr2} change, it is possible to tune the center frequency of the filter. The obtained frequency tuning band (FTB) varies from 0.62 to 5.67 GHz when using SF transistors, while it varies from 1.17 GHz to 3.28 GHz in the MF configuration. Despite the FTB reduction in the latter case, the simulated gain (S21) of the filter remains almost constant around 29 dB with the multi-finger optimization, as shown in Fig. 12(b). Also, a high power gain is achieved in the whole covered frequency band when using MF transistors. Such characteristic is important in reconfigurable circuits, which drives the use of this multi-finger optimization, maintaining a high and constant gain in the entire FTB. Due to

the higher BPF gain with MF compared to SF configuration, the maximal quality factor is also increased and a Q_{max} of 107 is attained at 1.85 GHz when using MF transistors.



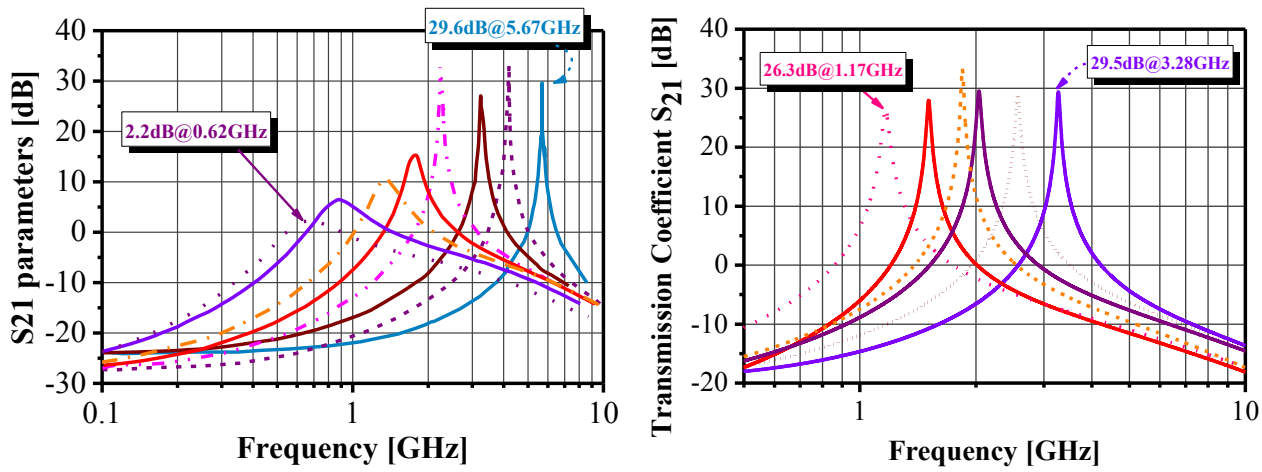
(a) (b)

Fig. 11. Layouts of the differential BPF: (a) without and (b) with multi-finger optimization

Concerning the DC power consumption of the BPF, it is increased when increasing the number of fingers, as suspected from Fig. 8. An optimal choice of *nf* in the used MOSFETs gives an appropriate power consumption to the RF filter. It varies from 3.58 mW to 6.44 mW, from 1.2 V supply voltage, in the MF configuration when increasing the BPF center frequency. Whereas, it varies from 0.96 mW to 7.55 mW by using SF transistors.

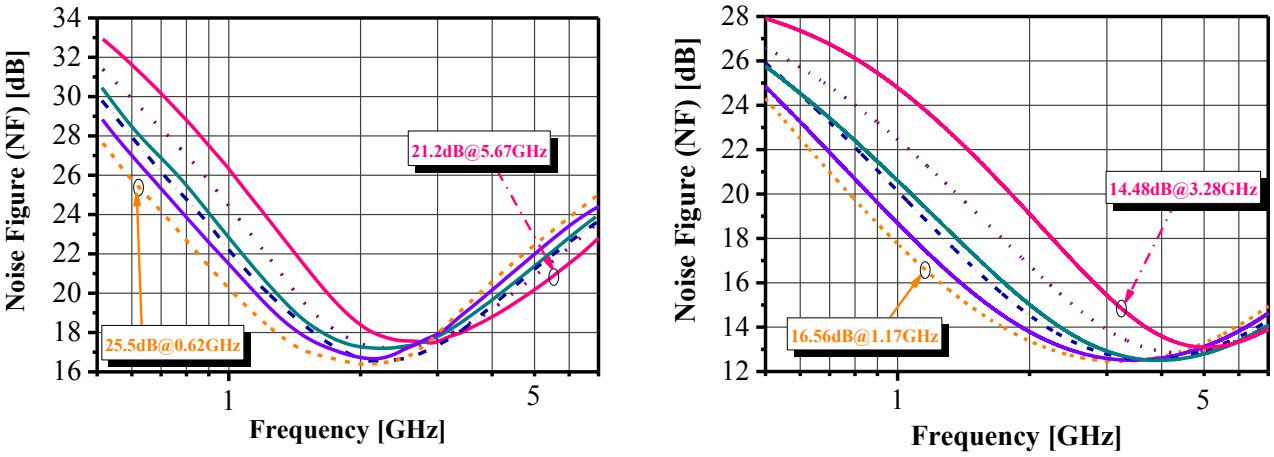
Besides, the noise characteristic of the designed differential BPF with its dynamic range has been examined depending on the MF approach. Fig. 13 shows the obtained noise figure responses versus the frequency for some selected control voltage combinations. It can be observed that the *NF* is 21.2 dB at 5.67GHz, with SF transistors, while it varies from 16.56 dB at 1.17 GHz to 14.48 dB at 3.28 GHz with MF MOSFETs.

Analysis of the BPF linearity has been investigated through the input third-order intercept point (*IIP3*) and the input referred 1 dB compression point ($P_{in,1dB}$). A great improvement has been achieved when applying the MF technique. In fact, by rising the number of fingers, the *IIP3* and $P_{in,1dB}$ increase from -8.3 dBm to 8.43 dBm, and from -7.57 dBm to 2.72 dBm, respectively.



(a) (b)

Fig. 12. Transmission coefficient S21 versus frequency of the differential BPF: (a) without and (b) with multi-finger optimization



(a) (b)

Fig. 13. Noise figure responses of the differential BPF: (a) without and (b) with multi-finger optimization

For reliability concerns, it is necessary to analyze the tolerance to Monte Carlo variations in RF circuit design. Indeed, Monte Carlo simulations allow the designer to consider the possible effects of a random variation of circuit's parameters over its performance. Monte Carlo analysis of the BPF has been carried out through both process and mismatch deviations over 100 runs. The obtained histogram and probability distribution of the filter's ($S21_{max}$) gain is shown in Fig. 14. The obtained result demonstrates that the gain has a mean value of 21.5 dB and a standard variation of 6.57 dB with MF technique.

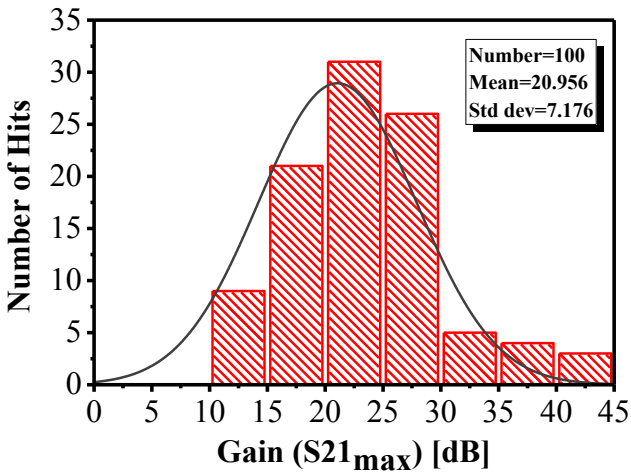


Fig. 14. Monte Carlo analysis of the differential BPF: Statistical distribution of the gain ($S21_{max}$) with MF optimization

Table 2 summarizes the performances of the designed differential bandpass filter with and without the multi-finger optimization. It illustrates that this MF technique allows a high gain, low noise figure, good linearity with suitable frequency tuning range and power consumption. A good robustness to Monte Carlo variations is also observed.

Tab. 2. Summary of the RF differential BPF performances

		Without optimization	With optimization	Gain (↑), Loss (↓)		
Tuning frequency	**[GHz]**	0.62 - 5.67	1.17 – 3.28	**Δf**	- 58.21%	↓
Gain (S21)	**[dB]**	0.9 – 37	13.56 – 33.45	**$S21_{max}$**	- 9.6%	↓
NF	**[dB]**	21.2-25.5	14.48-16.58	**NF_{max}**	- 43.21%	↑
$P_{in,1dB}$	**[dBm]**	-7.57	+2.72		+135.93%	↑
IIP3	**[dBm]**	-8.3	+8.43		+200.56%	↑
Q_{max} @ frequency	**-**	30@2.5GHz	107@5.4GHz	**Q_{max}**	+256.66%	↑
Power	**[mW]**	0.96 – 7.55	3.58 – 6.44	**P_{max}**	-14.7%	↑

4. Application on the design of oscillator

Generally, characteristics of the voltage-controlled oscillator (VCO) in terms of phase noise and frequency tuning range impacts the whole transceiver performance. Accordingly, judicious design considerations have to be assessed to ensure high performance VCOs. In this section, the basic idea of NMOS cross-coupled LC-VCO [71] has been exploited in an alternative topology in which the spiral inductor is replaced by a novel tunable active inductor (TAI). This latter is based on the Gyrator-C principle, often convenient to recognize the impact of multi-finger configurations.

The architecture of the proposed inductorless LC-VCO is shown in Fig. 15 with a focus on the tunable active inductor structure. To simplify the circuit presentation, it is reported that the oscillator is biased using a tail current source M_{bias}. By adjusting V_{ctrl}, the resulting control current is applied to the cross-coupled $M_{1,2}$ transistor sources to assure a reliable startup, perpetuate the oscillation and alter the output voltage swing, i.e. the voltage headroom.

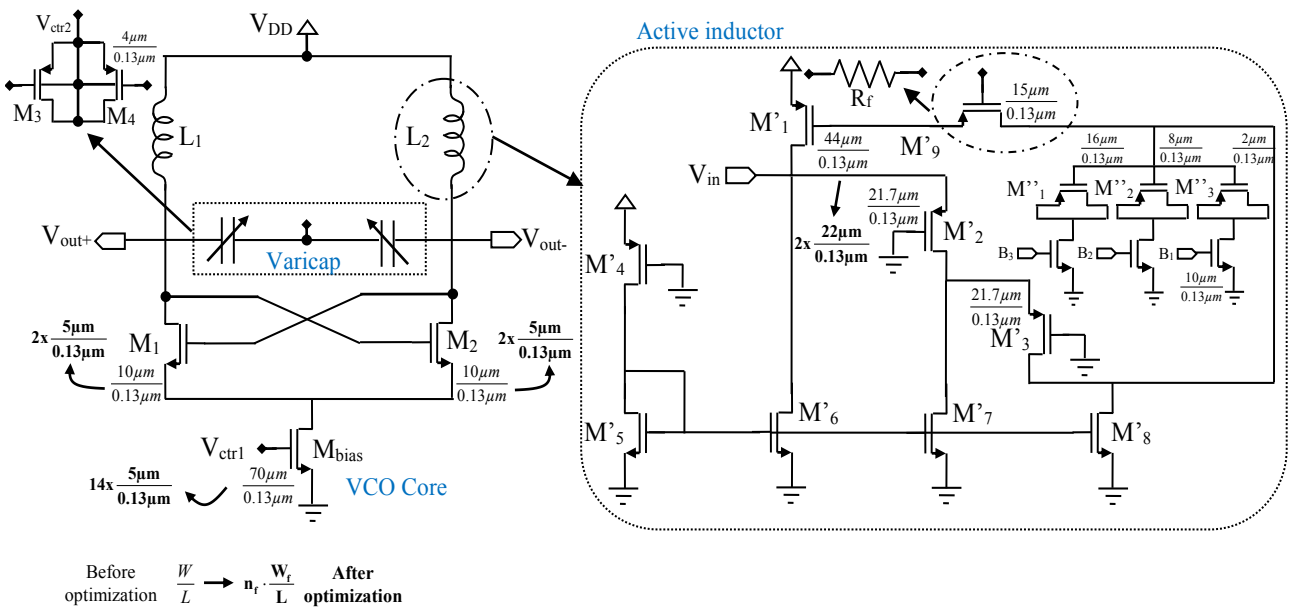


Fig. 15. Architecture of the LC-VCO and its tunable active inductor

The LC-tank consists of a PMOS varactor for continuous tuning and two TAIs determining the oscillation frequencies. The topology of the proposed inductor is different from that used in the bandpass filter discussed in the previous section. It consists of three PMOS transistors to emulate the inductive behavior. The presence

of an active feedback resistance (R_f) introduces an additional impedance to enhance the quality factor. Furthermore, a network of switched capacitors is added to adjust the inductance value independently. Thus, the circuit is designed to operate as a high impedance at 2.4 GHz to prevent the 2nd order harmonic, meanwhile the maximum Q-factor of the TAI is 612 at 1.27 GHz. Deeper insight with detailed implementation and results of the TAI in 90nm CMOS process are given in [72-74].

In order to investigate the effect of MF technique, a comparison between two separate layouts using conventional gate-above-device (CGAD) and MF technique is given, as shown in Fig. 16. The area occupation of the VCO presents a reduction about 6% when applying the multi-finger approach. In the optimized MF-based circuit, the layout has a total area of 1772 µm², while the original one occupies a size of 1882 µm².

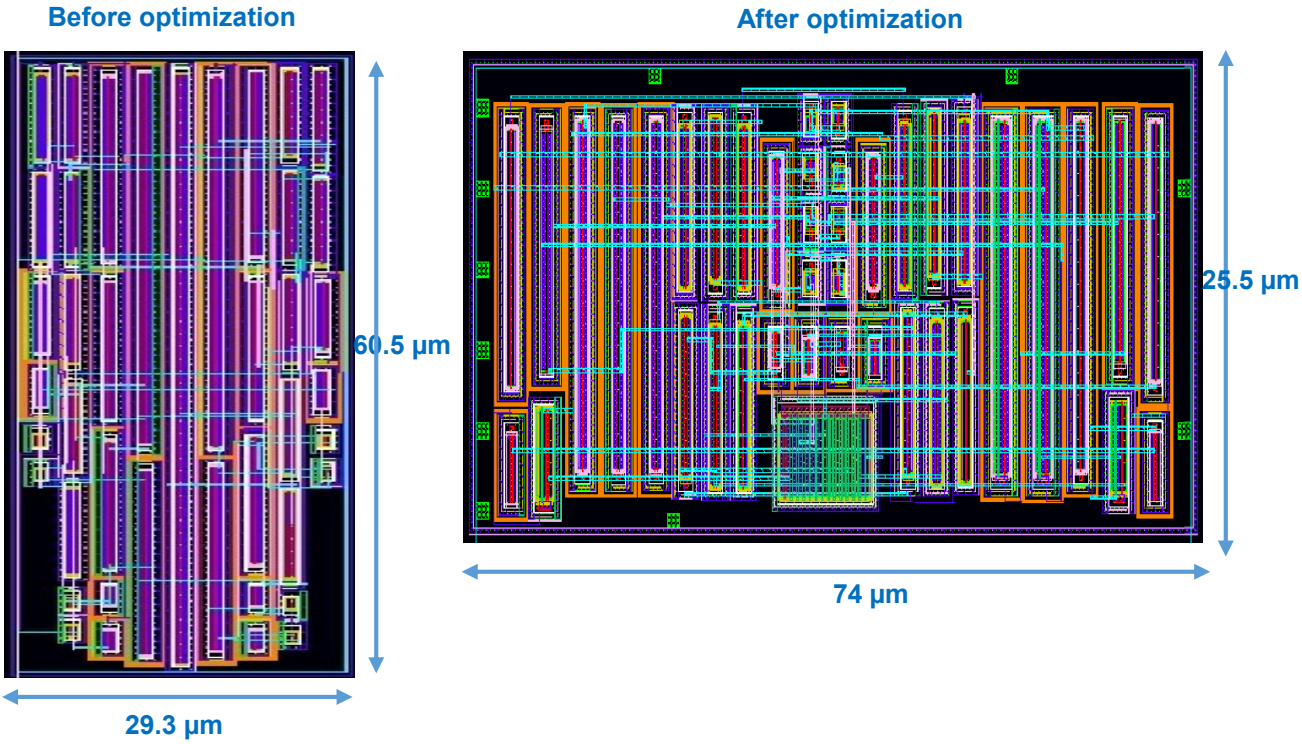


Fig. 16. Layouts of the inductorless LC-VCO without and with multi-finger optimization

In the following study, the obtained results are provided through three different configurations.

- Configuration I: using the conventional SF MOSFETs.
- Configuration II: using the optimized MF technique, with $nf = 2$ for some transistors.
- Configuration III: using MF transistors too, with $nf > 2$ to demonstrate the MF technique limits.

Fig. 17 depicts the frequency tuning characteristic of the VCO for the different configurations. A narrow frequency tuning range of 0.75% is achieved while changing the control voltage from -1.2 V to 0 V. In configurations I and II, the obtained frequency range is [2.4, 2.418] GHz with a tuning sensitivity of 18 MHz/V. In configuration III, the frequency band increases slightly at the cost of an undesired nonlinear zone. Fig. 18 illustrates the output waveforms of the differential outputs at 2.4 GHz, showing that the voltage magnitude rises from 0.49 V to 0.67 V when changing the MF configurations.

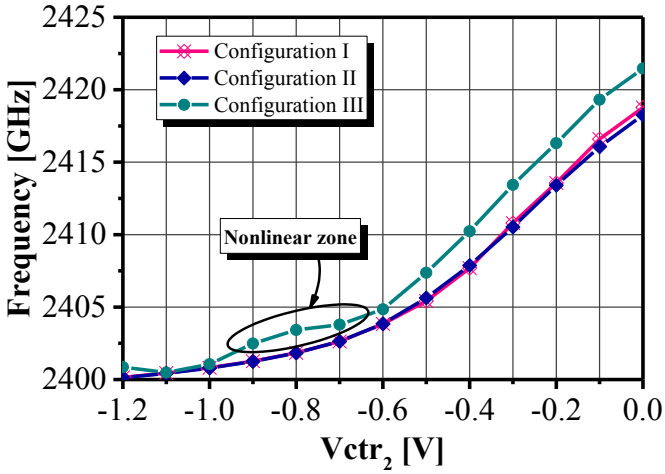


Fig. 17. Comparison of the frequency tuning characteristics of the VCO for different configurations

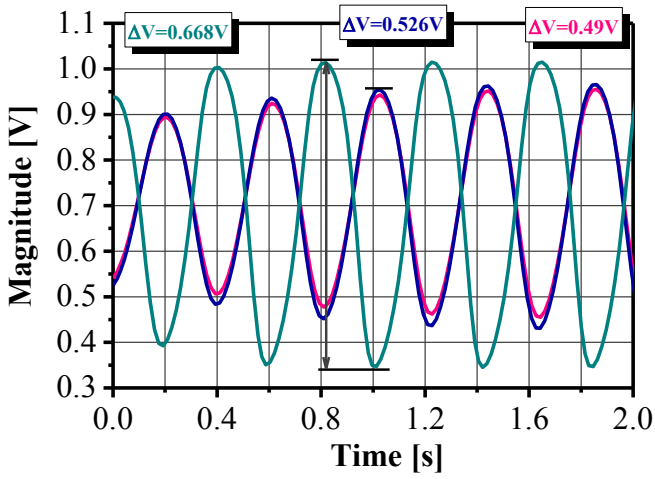


Fig. 18. VCO differential output waveforms at 2.4 GHz for different configurations

Fig. 19 plots the phase noise (PN) profile of the proposed oscillator. Using single finger transistor, the VCO achieves a PN of -107.3 dBc/Hz. In the optimized implementation, i.e. configuration II, the PN is still unchanged, while it lowers to -108.6 dBc/Hz for configuration III. Note that these values are normalized at 10 MHz offset from the 2.4 GHz carrier.

Unfortunately, the total harmonic distortion (THD) results show a degradation especially for the multi-finger device when *nf* is superior to 2. The THD can be defined as follows [75]:

$$THD = \sqrt{\sum_{n=2}^{\infty} I_n^2 / I_1^2} \tag{8}$$

where I_1 and I_n are fundamental and *n*th harmonic current of the oscillator, respectively.

In fact, due to the increased g_m compared to conventional device, the quantity of drain current has a main impact on the total unwanted harmonic current, which also affects the fundamental current, and thus influences the oscillation. Regarding Fig. 20, the THD improvement is more significant while using single finger device (configuration I) or bi-finger transistor (configuration II). For fair comparison, at 2.4 GHz, the THD of the VCO with $nf = 1$ and $nf = 2$ is 3.4% and 3.76%, respectively, whereas the THD of the VCO with $nf > 2$ sharing is 8.21%.

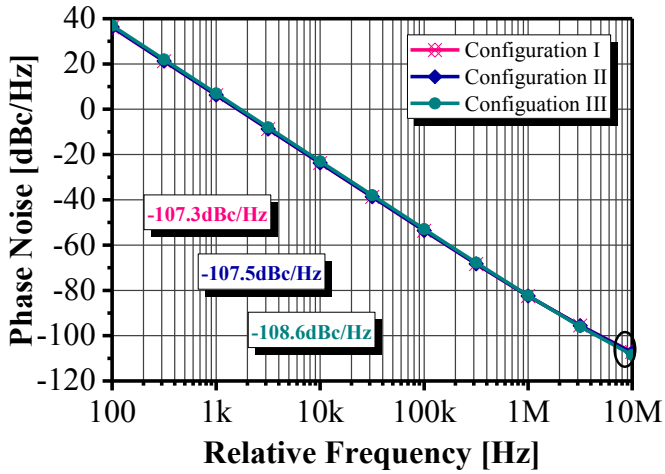


Fig. 19. Evaluated Phase Noise (PN) at 2.4 GHz of the VCO for different configurations

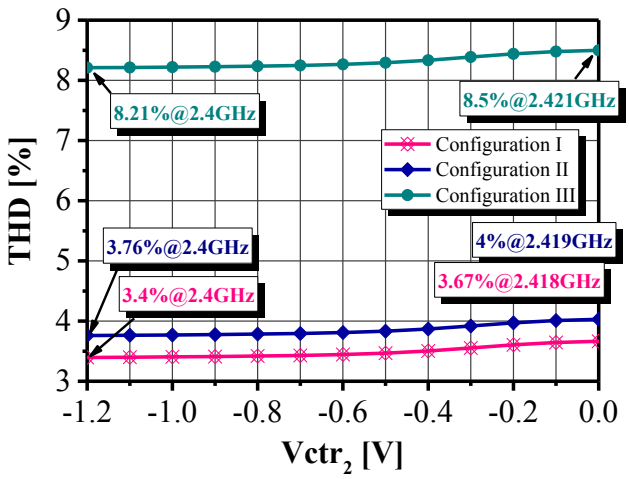


Fig. 20. Total Harmonic Distortion (THD) of the VCO for different configurations

Besides, the VCO core dissipates about 5 mW half of which is consumed by the tunable active inductors. Fig. 21 provides an overview of the power consumption in the VCO and TAI, for the different configurations. As suspected, the power consumption increases with the number of fingers in the MOSFET.

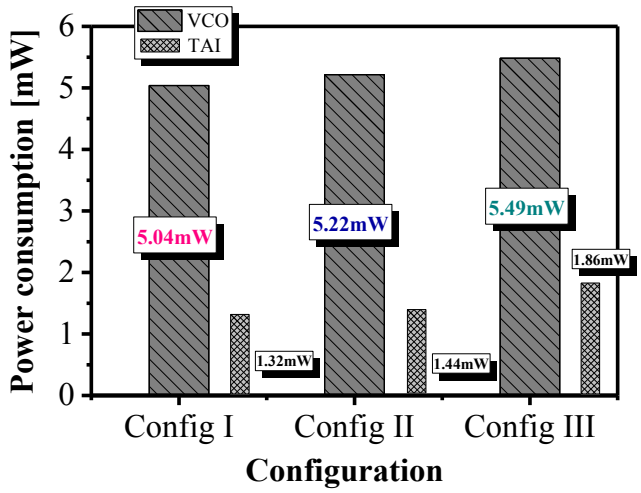


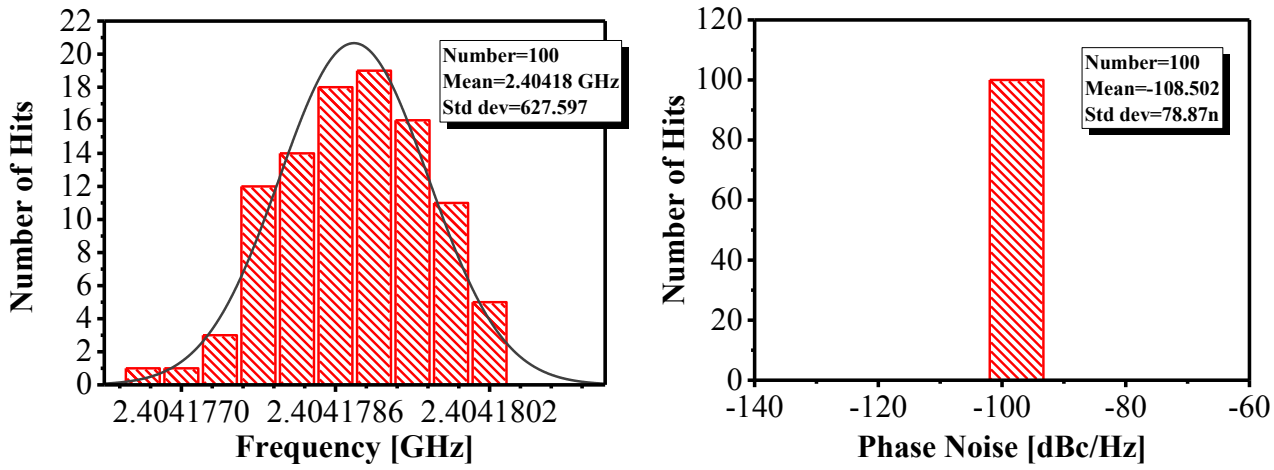
Fig. 21. Comparison of the power consumption of the VCO for different configurations

Table. 3 recapitulates the obtained performances of the three designed oscillators. To summarize, the use of multi-finger transistors provides a certain level of enhancements that results in area reduction, but a deliberate $nf > 2$ would further degrade the K_{VCO} linearity and also the THD, which degrades the performances and limits the reliability of the circuit.

Tab. 3. Performances summary of the VCO for the different configurations

		Configuration I	Configuration II	Configuration III	Config. I vs Config. II Gain (↑), Loss (↓)	
V_{pp} (ΔV)	**[mV]**	490	526	668	+7.3%	↑
K_{VCO}	**[MHz/V]**	17.9	17.4	20.6	- 2.8%	↓
FTR	**[%]**	0.747	0.722	0.855	- 3.4%	↓
THD	**[%]**	3.395	3.76	8.21	+10.8%	↑
PN@10MHz	**[dBc/Hz]**	-107.3@2.4GHz	-107.5@2.4GHz	-108.6@2.4GHz	- 0.2%	↑
Power	**[mW]**	5.04	5.22	5.49	+3.6%	↓
Area	**[µm²]**	1887	1772	Not released	- 6.1%	↑
FoM	**[dBc/Hz]**	-147.88	-147.93	-148.8	- 0.04%	↑
FoM_T	**[dBc/Hz]**	-170.4	-170.7	-170.1	- 0.18%	↑
FoM_A	**[dBc/Hz]**	-175.2	-175.5	Not released	- 0.17%	↑

Monte Carlo analysis is also achieved to assess the robustness of the optimized VCO to process and mismatch uncertainties. Monte Carlo simulations are performed with 100 runs for random values. Fig. 22, depicts the results for the two fundamental parameters of an oscillator: natural free-running frequency and phase noise. As depicted in Fig. 22(a), the oscillator frequency shows a robustness to process and mismatch variations with 98% of samples between 2404.17 and 2404.18 MHz in distribution of the mean value, i.e. 2404.18 MHz. In addition, a steady PN at 108.5 dBc/Hz has been obtained as shown in Fig. 22(b). These results demonstrate the reliability of the designed oscillator and its stability versus process and mismatch variations.



(a) (b)

Fig. 22. Monte Carlo analysis of the VCO: (a) central frequency (2.4GHz), (b) Phase Noise@10MHz

5. Application on the design of Low Noise Amplifier

The LNA is one of the most important blocks in RF receivers, since it is the first building block so that its characteristics influence the whole reception chain. To investigate the effect of MF technique on the performances, two principal considerations have been applied to design RF LNAs [76]:

- Determine the circuit topology and it is matching network,
- Select the bias point of transistors and hence their topology.

In most cases of circuit design, few numbers of transistors are preferred to realize a straightforward core. In LNAs, the design challenge is to ensure a good agreement between wide band gain flatness, low noise figure, high linearity and broadband impedance matching [77]. In the studied application, a common gate (CG) topology has been used as illustrated in Fig. 23. This cascode structure provides a better isolation between input/output, where M_2 assures the isolation of Miller capacitance. The input matching network includes the capacitor C_{in} and the inductor L_g, inductor L_s operates as the resonant frequency. Inductor L_d with capacitors C_d and C_{out} determine the resonant frequency and form the output matching network.

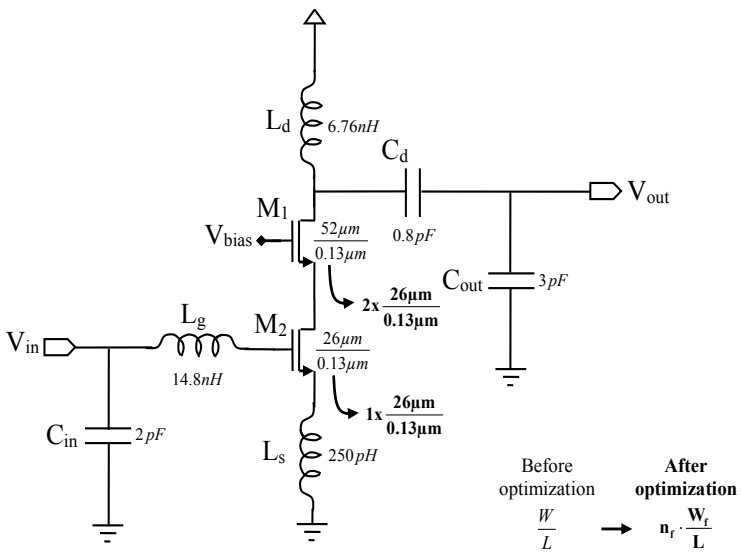


Fig. 23. Schematic of the Low Noise Amplifier (LNA)

This CG-LNA operates at 2.4 GHz with drain current I_D around 5 mA under a $W_{M1} = 2.W_{M2}$. Analyses of the LNA have been mainly attributed to the following configurations:

- Configuration (I): one finger device W_{M1} = 52 µm (nf = 1), W_{M2} = 26 µm (nf=1).
- Configuration (II): double finger device W_{M1} = 52 µm (nf = 2), W_{M2} = 26µm (nf=1).
- Configuration (III): multi-finger device W_{M1} = 52 µm (nf = 4), W_{M2} = 26µm (nf=2).

The LNA has been implemented in 130 nm CMOS technology. The total area of LNA is approximately (658 x 435) µm², as shown in Fig. 24. In presence of many passive components, i.e. three spiral inductors and three MIM capacitors, which dominates the space, the MF technique is not beneficial to optimize the surface. As an indication, Fig. 24(b), shows that using two-finger based transistor M_1 can reduce the area from 255µm² to 144µm², which is an important feature in inductorless designs.

Fig. 25 depicts the variations of S11 and S22 parameters for the different configurations mentioned above. In Fig. 25(a), the maximum input-return loss S11 is -44.17 dB in design (II), which is 2.5 dB higher than the obtained results from designs (I) and (III). The measured S22 gives values under -17.4 dB, -23 dB and -24.8 dB for configurations (I), (II) and (III) respectively. Moreover, the LNA achieves a high-power gain ($S21_{max}$) that varies between 19 dB and 22 dB at 2.4GHz over the three designs, as illustrated in Fig. 26(a). It can be noted that the gain performance is slightly sensitive to MF technique.

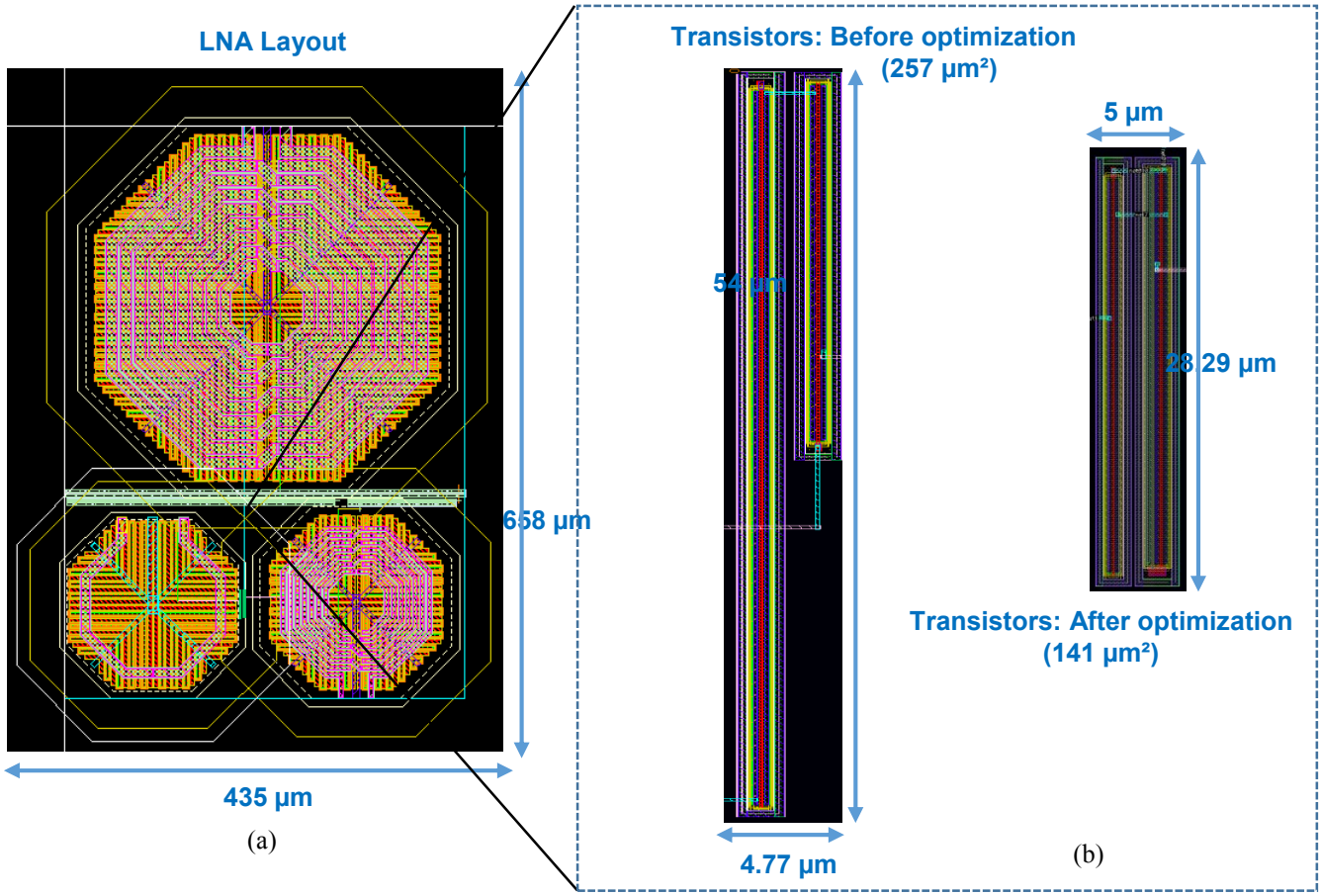
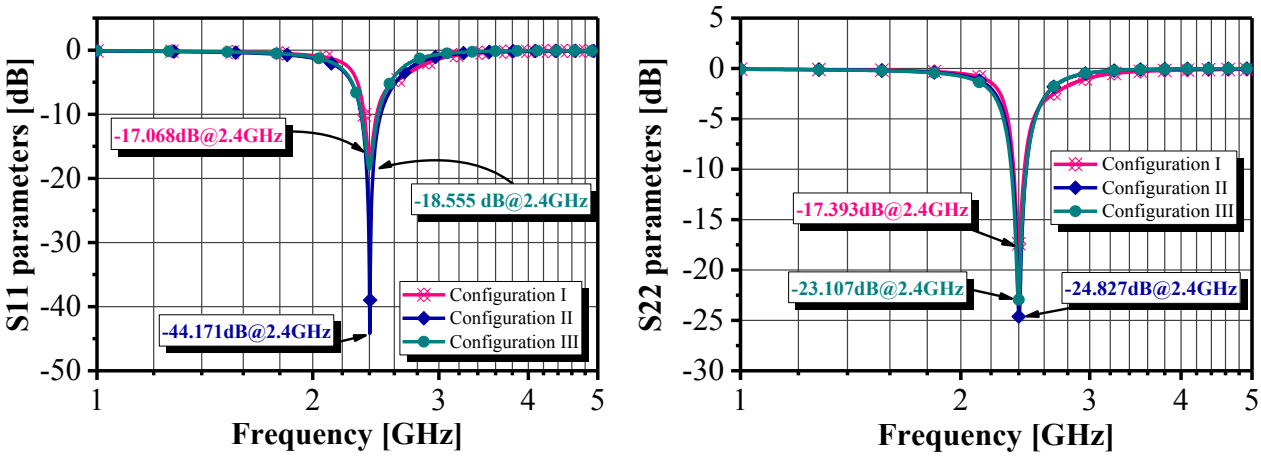


Fig. 24. (a) Layout of the LNA with and without multi-finger optimization, and a zoom on the (b) transistors: before and after optimization

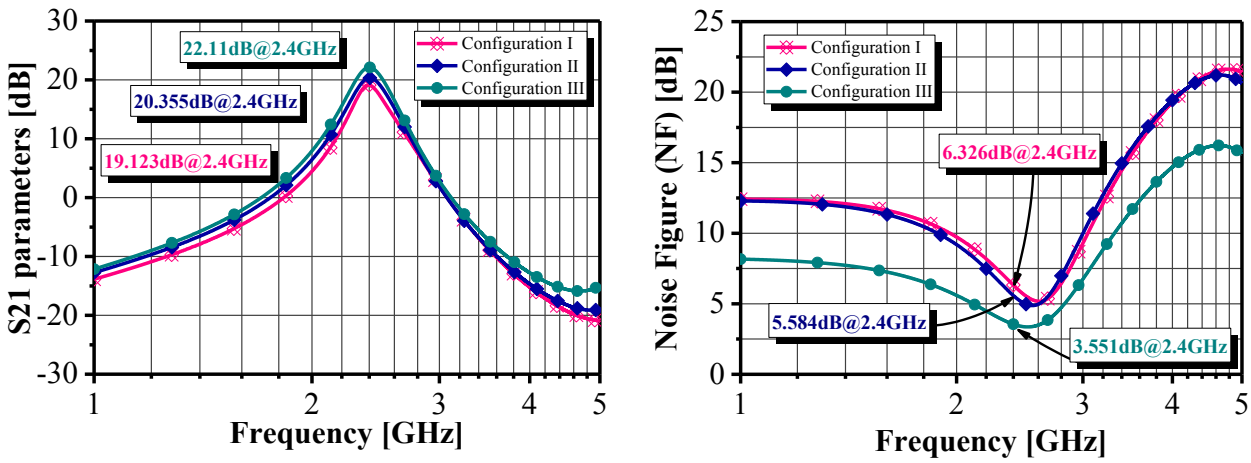


(a) (b)

Fig. 25. (a) Input return loss (S11), (b) output return loss (S22), versus frequency of the LNA, for different configurations

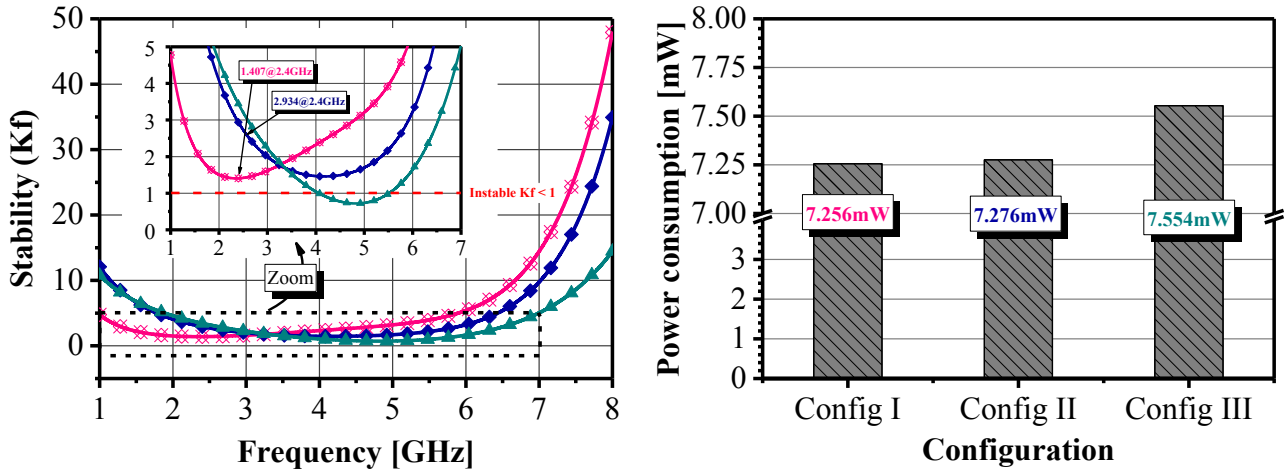
The obtained noise figure is also depicted in Fig. 26(b) showing that it is improved while increasing the number of fingers, as already discussed in section 2. Fig. 27(a) gives an important information about the LNA stability by plotting the K_f parameter. It indicates a stable operation in configurations (I) and (II), while an instability occurs when the number of fingers is superior to 2, i.e. in configuration (III). Thus, although its good output-return loss (S22) of -34.8 dB, peak gain ($S21_{max}$) of 22.1 dB and minimum NF of 3.55 dB, the configuration (III) is instable. This limitation could be avoided through a resizing of the transistors. With the new optimal sizing of the LNA components, it become unconditionally stable (K_f>1) over high frequencies, together with a good power gain of 20.35 dB after matching proof.

Under a supply voltage of 1.2 V and a bias current of 5.83 mA, the power consumption of the core circuit is around 7.27 mW as demonstrated in Fig. 27(b). This result is in correlation with the previous study of the *nf* impact on MOSFETs.



(a) (b)

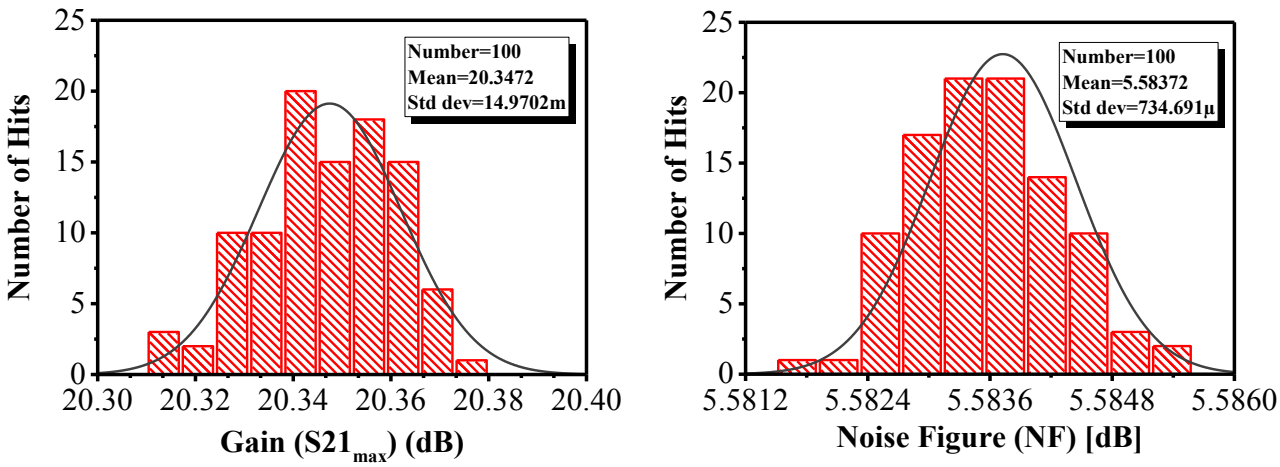
Fig. 26. (a) Transmission coefficient (S21) and (b) Noise Figure versus frequency of the LNA, for different configurations



(a) (b)

Fig. 27. (a) Stability versus frequency of the LNA and (b) power consumption: with and without multi-finger optimization

To qualify the effect of process and mismatch variations after MF optimization, Monte Carlo simulations have been performed with 100 iterations. They are performed for the principal performances of the LNA, i.e. the gain and noise figure. Fig. 28 depicts the obtained results as statistical histograms. The Gaussian distributions at ± 3δ level show that 98.5% of the total samples of $S21_{max}$ occurs with bound between 20.302 and 20.392 dB, while 93% samples lead to be between 5.582 and 5.585 dB in distribution of NF. Thus, the gain and NF of the LNA are robust to mismatch with only 0.073% and 0.13% deviation, referring to their respective mean values.



(a) (b)

Fig. 28. Monte Carlo analysis of the LNA: (a) Gain ($S21_{max}$) and (b) Noise Figure (NF) after optimization

Table 4 Summaries the LNA's design performances. The figure of Merit defines as follows [78,79] is also compared:

$$FoM = \frac{S21[dB].BW[GHz]}{(NF[dB]-1).P_{DC}[mW]} \tag{9}$$

It can be seen that the bi-finger structure (Configuration II) gives the best tradeoffs. It achieves a good input matching (S11 < -10 dB) in the desired frequency range with the lowest noise figure of 5.58 dB at 2.4 GHz, a valid stability condition (K_f> 1 ∀ frequency) and a suitable power consumption.

Tab. 4. Summary of LNA performances for the different configurations

		Configuration I	Configuration II	Configuration III
S11	**[dB]**	-17.068	-44.171	-18.555
S21	**[dB]**	19.123	20.355	22.11
S22	**[dB]**	-17.393	-24.827	-23.107
NF	**[dBm]**	6.326	5.584	3.551
Power	**[mW]**	7.256	7.276	7.554
$P_{in,1dB}$	**[dBm]**	-18.635	-18.665	-18.742
IIP3	**[dBm]**	-23.55	-24.11	-24.44
THD	**[%]**	10.5	14	15.6
Gain/P_{DC}	**[dB/mW]**	2.63	2.8	2.92
BW	**[MHz]**	228	256	304
K_f @ 2.4GHz	**-**	1.407	2.934	3.456
K_f along frequency	**-**	>1 ∀ [frequency]	>1 ∀ [frequency]	< 1 [4 GHz ; 5.2 GHz]
FoM	**-**	0.142	0.156	0.349
Area	**[mm²]**	0.286		

Note that there is a severe tradeoff between input impedance matching and noise figure. For CG-LNA keeping a good S11 with a noise figure lower than 4 dB is very difficult [77]. By additional optimization effort in configuration (III), the noise performance of the LNA can be further improved at a cost of decreasing the input impedance matching and affecting the linearity. For instance, the geometry of transistor M_1 has been adjusted to be 26 µm for an $nf = 4$. In this case, the LNA returns stable with a new NF of 3.63 dB (< 4 dB). In the present optimization, the circuit requires a careful re-sizing of the components, as changing L_d and L_s in order to maintain input/output matching without sacrificing the gain. But, keeping the increase of nf may destroy the input matching and hence break the stability. Table 5 gives an overview of the obtained results after the final optimization.

Tab. 5. Summary of different performances of the LNA after final optimization

		W_{M1}=26 µm (nf=4) **W_{M2}=26 µm (nf=2)**	**Gain (↑), Loss (↓)**	
S11	**[dB]**	-25.37	+48.68%	↑
S21	**[dB]**	20.86	+9.08%	↑
S22	**[dB]**	-19.45	+11.83%	↑
NF	**[dBm]**	3.63	- 42.62%	↑
Power	**[mW]**	7.22	-0.5%	↑
$P_{in,1dB}$	**[dBm]**	-18.71	+0.4%	↓
IIP3	**[dBm]**	-24.02	+2%	↓
THD	**[%]**	14.5	+38.1%	↑
Gain/P_{DC}	**[dB/mW]**	2.89	+9.89%	↑
BW	**[MHz]**	266	+16.67%	↑
K_f @ 2.4GHz	**-**	4.64	+229.78%	↑
K_f along frequency	**-**	>1 ∀ [frequency]	-	-
FoM	**-**	0.292	+105.64%	↑
Area	**[mm²]**	Not realized	-	-

6. CONCLUSION

The effects of the Multi-finger gate on area, power consumption, noise, maximum oscillation frequency f_{max} and cutoff frequency f_T of the 130 nm CMOS MOSFETs has been systematically investigated by Virtuoso® simulation and compared to the conventional one. Both R_g and NF_{min} decrease with increasing the number of finger. Moreover, the finger width W, pitch P and number nf modulate the gate capacitance C_g and resistance R_g, and thus, in turn, f_{max}, f_T.

An implementation to a reconfigurable RF differential bandpass filter, inductorless LC-VCO and LNA has been also developed with and without using the MF optimization, showing significant improvements in RF characteristics depending on the number of fingers. Overall, based on design trade-offs required to achieve the best RF performance (stability, noise and gain), MF optimization technique reveals that the influences are more obvious in the finger range of less than 5, thus implying that the MF design is reliable for CMOS technology in RF applications. With suggested configurations, proposed circuits present robustness to Monto Carlo statistical analyses, random process and mismatch, as well as environmental variations when using multi-finger MOSFETs.

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