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Review

Architecture and Process Integration Overview of 3D NAND Flash Technologies

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Abstract: In the past few decades, NAND flash memory has been one of the most successful non-volatile storage technologies, and it is commonly used in electronic devices because of its high scalability and reliable switching properties. To overcome the scaling limit of planar NAND flash arrays, various three-dimensional (3D) architectures of NAND flash memory and their process integration methods have been investigated in both industry and academia and adopted in commercial mass production. In this paper, 3D NAND flash technologies are reviewed in terms of their architecture and fabrication methods, and the advantages and disadvantages of the architectures are compared.

Keywords: NAND flash memory; three-dimensional architecture; process integration

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1. Introduction

Recently, the demand for mobile electronic devices has been increasing owing to a no-contact lifestyle. This is leading to an enormous market growth in storage memory, particularly NAND flash, because the technology transformation from hard-disk drives to solid-state drives has already been established, owing to the requirements for a faster operation speed and a lower power consumption. Since NAND flash was commercialized for mass production in the early 1990s, reducing the cost per bit has been one of the most important approaches for NAND flash memory, and there have been efforts to scale down the effective cell size. Interestingly, NAND flash cells have been integrated into three-dimensional (3D) NAND flash architectures for further scaling down, unlike logic devices.

The 3D NAND flash architectures have been realized in various structures and can be categorized into two types based on the stacking direction: channel and gate stacks. Figure 1 shows the structure–year classification of 3D NAND flash. Toshiba announced the first 3D stack flash based on a gate stacked structure, such as bit cost scalable (BiCS) [1], pipe-shaped BiCS (PBiCS) [2] with charge trapping layers and a horizontal-channel-type floating gate (HC-FG) [3] with a floating gate. In addition, Samsung has developed various 3D structures based on both stack methods. Examples are the terabit cell array transistor (TCAT) flash [4], vertical recess array transistor (VRAT) flash, vertical stacked array transistor (VSAT) flash [5] structure for efficient connection of peripheral circuits, vertical gate (VG) NAND [6] with a vertical gate and channel stacked structure, and V-NAND, which was the first 3D NAND product commercialized by Samsung [7]. SK Hynix has also developed several 3D architectures based on both methods: a dual control gate with a surrounding floating-gate (DC-SF) [8] structure, a hybrid 3D NAND structure [9] with mixed gate and channel stacks, a stacked memory array transistor (SMArT) [10] using an oxide–nitride–oxide (ONO) film to minimize the stack height, and a metal control gate past process (MCGL process) [11] using a metal gate based on the DC-SF structure. Channel-stacked 3D architectures have been investigated, including the dual-channel 3D

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NAND structure [12–16] from Macronix and a single crystalline Si-stacked array (STAR) structure [17] from Seoul National University.

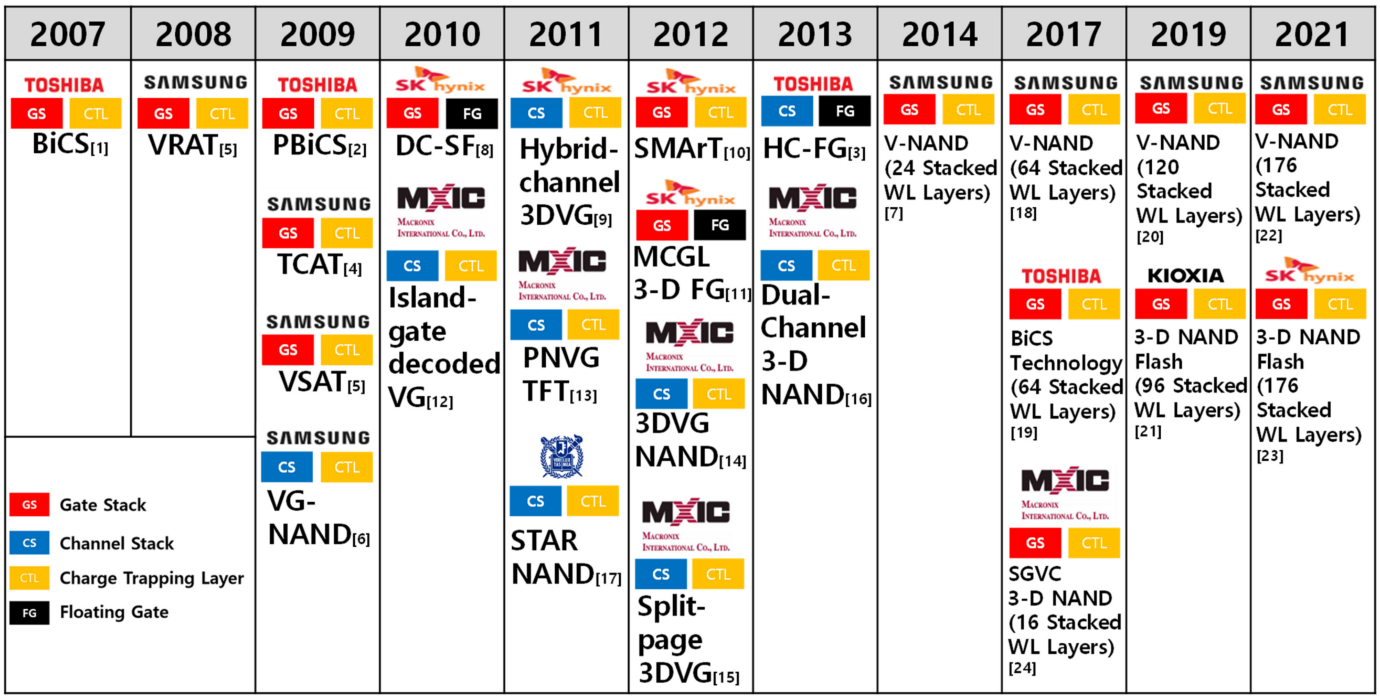
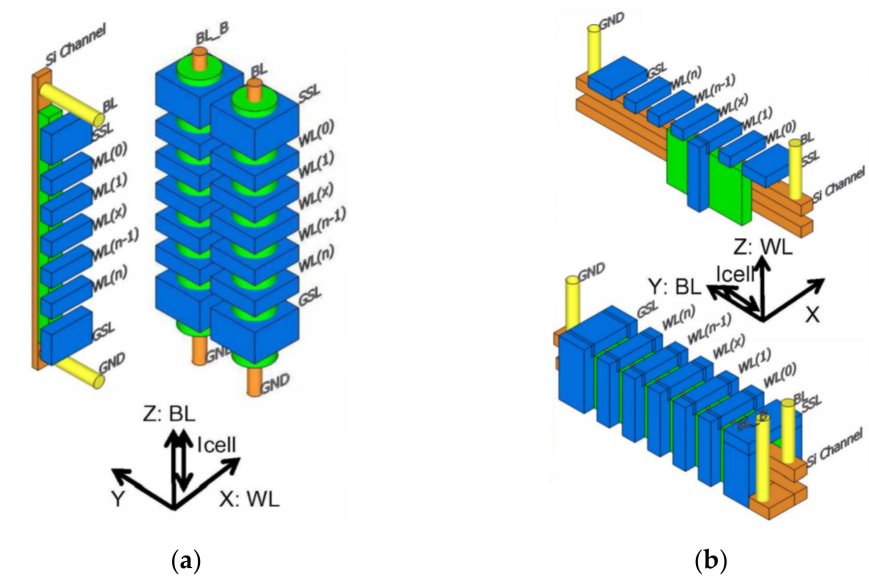


Figure 1. Chronological development of 3D NAND flash technologies.

In this study, all 3D NAND architectures are analyzed and compared from a structural perspective. First, in Section 2, the 3D NAND flash architectures are discussed based on the stack method and their operational characteristics. Section 3 compares and analyzes the fabrication methods of all structures based on the gate fabrication method.

2. Three-Dimensional NAND Flash Architectures

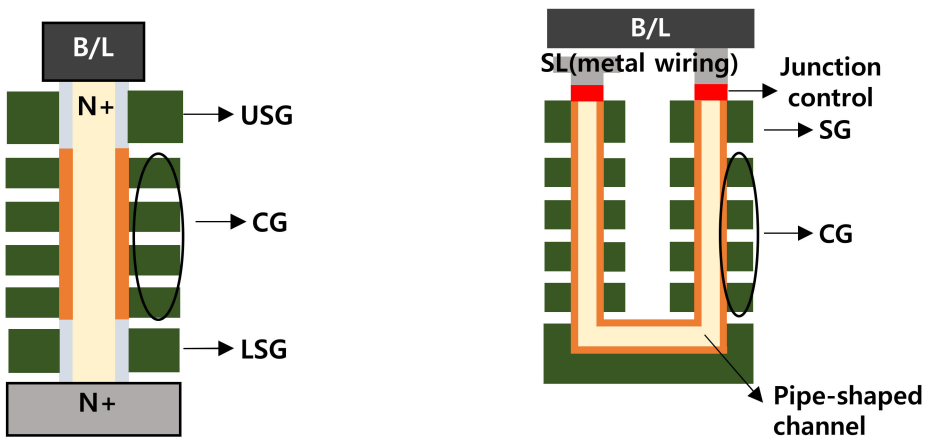
The architectures of 3D NAND flash can be typically classified into gate-stacked structure [1,2,4,5,7,8,10,11,18–24] and channel-stacked structure [3,6,9,12–17], which are illustrated in Figure 2. In the gate-stacked structure, a channel is formed after stacking gate layers, and the current flows in the vertical direction. The cell structure is mostly based on gate-all-around (GAA), because a channel hole is filled with polycrystalline silicon (poly-Si) and a gate dielectric stack; inherently, this structure has several issues arising from the hole diameter. In contrast, in a conventional planar NAND array in a channel-stacked architecture, the current flows in the lateral direction. Although the scaling of a channel-stacked structure is limited by the ONO thickness in the bit line (BL) pitch, it is necessary to maintain the word line (WL) channel length to maintain an effective memory window. Moreover, it is difficult to connect the BLs with each layer, owing to their horizontal and parallel orientations. Currently, most commercialized 3D NAND architectures use the gate-stacked structure, owing to the abovementioned problems in the channel-stacked structure [25,26].



(**a**) (**b**)

Figure 2. (**a**) Gate-stacked (vertical channel) and (**b**) channel-stacked (vertical gate) 3D NAND architectures [26], Copyright IEEE, 2014.

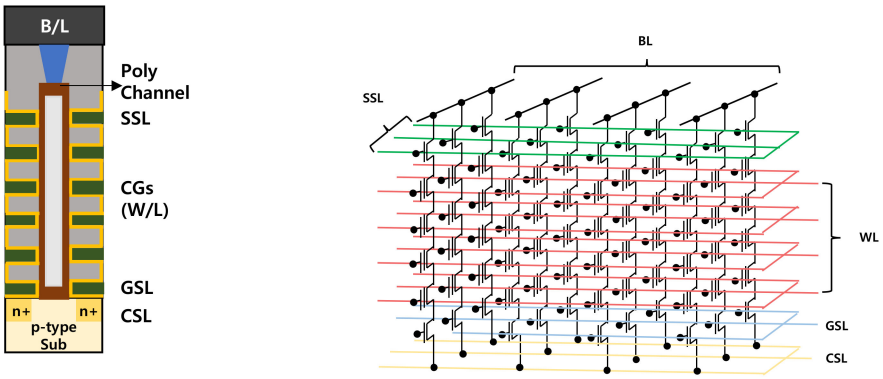
Figure 3a,b compare the cross-sectional views of the BiCS and PBiCS flash structures, respectively, based on the gate-stacked structure and gate-first fabrication method. The BiCS flash structure was the first proposed 3D NAND architecture with a high density and cost per bit. In the BiCS structure, the vertically stacked gates are composed of a lower select gate (LSG), an upper select gate (USG), and control gates (CGs), as shown in Figure 3a. Because the channel pillars are not directly connected to the p-well in this structure, gate-induced drain lowering (GIDL) is used as the erase mechanism [1,27–30]. The PBiCS architecture improves the limitations of the BiCS flash, including the program/erase window, retention properties, high resistance of the source line (SL), and multibit operation. PBiCS flash has a U-shaped string structure, instead of a straight shape, and a pipe connection (PC) is formed at the bottom between two adjacent gates. This structural difference lowers the SL resistance because it can be accessed by the first and second metal layers, similar to a conventional planar NAND flash array. In terms of reliability, the PBiCS flash has better retention characteristics thanks to less damage to the trapping layer during the fabrication process, and the low resistance of metal wiring and steeply controlled diffusion profile at the SL allows the PBiCs to have better cut-off characteristics [2,31,32].



(**a**) (**b**)

Figure 3. Cross-sectional views of (**a**) BiCS structure and (**b**) PBiCS structure.

Figure 4a shows a cross-sectional view of the TCAT architecture. The TCAT uses metal CGs, owing to the use of the gate-last fabrication method. Poly-Si channel holes are formed using the punched-through method like that in the BiCS structure; however, a notable difference is that the TCAT is connected to a p-type substrate, which allows the bulk erase operation. The two poly-Si channels in the structure share a common source line (CSL) formed by the WL cut. Figure 4b shows that the circuit diagram of the TCAT cell array is equivalent to that of a 90°-rotated planar flash array per string layer, and its bottom end is connected to the CSL. The ground selection line (GSL) and string selection line (SSL) transistors are at the top and bottom of a string, respectively, and flash cells are placed between them in series [4,33].



(**a**) (**b**)

Figure 4. (**a**) Cross-section view and (**b**) equivalent circuit diagram of TCAT flash array structure.

Figure 5a shows the VRAT architecture containing a planarized-integration-on-the-same-plane (PIPE) structure for effective vertical interconnection [5]. All the WLs are exposed on the same plane simultaneously during the chemical-mechanical planarization (CMP) process. The WLs do not need to be etched consecutively for each layer, unlike in a stair-like method, which implies that the PIPE structure increases the efficiency of the WL interconnection without an additional lithography step after stacking. The VSAT is aimed at solving the difficulties in the fabrication of the VRAT structure, as shown in Figure 5b. Instead of the gate-last process, in which an undercut region is formed and filled, the VSAT structure is fabricated using the gate-first method with doped poly-Si. Because the undercut process is not required for the VSAT structure, it is easy to realize vertical strings along with the stacked WLs, which are similar to the currently commercialized 3D NAND flash string. In addition, the dual-gate structure of the VSAT architecture effectively elongates the channel length without cell density loss, leading to a reduction in the off-current [5,33–35].

A schematic and unit cell diagram of the VG NAND structure are illustrated in Figure 6 [6]. Here, the channels are horizontally stacked, unlike in the BiCS and TCAT structures, and it has an almost identical structure to that of a planar flash array, except for the SSL, which means that the effective cell size per layer is maintained as $4F^2$. The source and the active body (V_{bb}) are connected to the CSL, enabling the body erase operation, and the required number of SSLs depends on the number of active layers. Common BLs and WLs are used between the stacked active channel layers, and a string needs to be selected to program a specific target cell by SSL biasing.

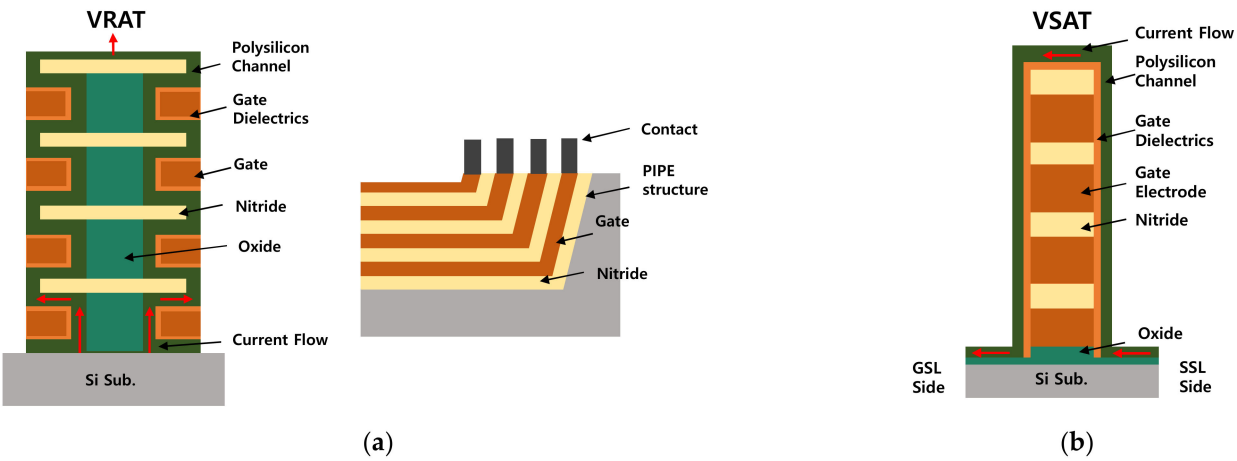


Figure 5. Schematics of (**a**) VRAT and (**b**) VSAT with PIPE structure.

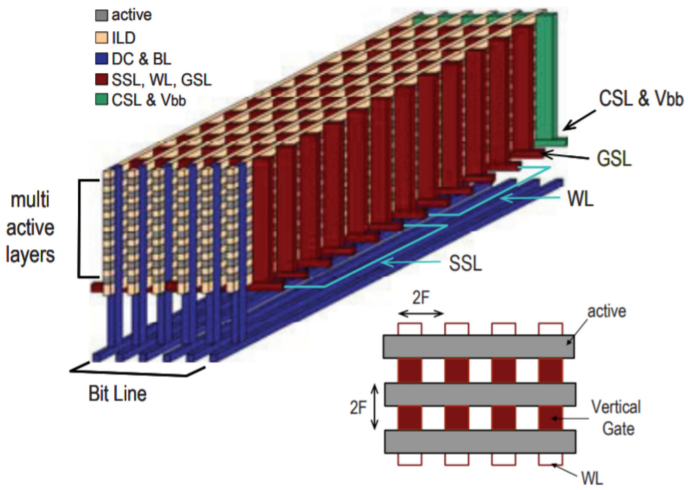


Figure 6. Schematic of VG NAND flash array [6], Copyright IEEE, 2009.

Unlike the above-mentioned approaches, a floating gate is used as the charge storage layer in the DC-SF structure, as shown in Figure 7a [8]. In this structure, an FG is surrounded by two CGs and covered by an inter-poly dielectric (IPD) and a tunneling oxide. It consists of two CGs and presents a vertical direction. Owing to the thick IPD layer, no tunneling occurs in the CG direction. In addition, a charge spreading phenomenon rarely occurs thanks to the isolated charge in the FG, unlike in the BiCS, as shown in Figure 7b. In the case of the BiCS, charge spreading occurs because the CTL is connected successively to the adjacent cells, while it does not occur in the DC-SF, because the FG is separated and isolated from each cell. Moreover, cell-to-cell interference is negligible, owing to the shielding effect of the two CGs. It also has a wide program/erase window, low operating voltage, and high coupling ratio. The DC-SF can have good retention characteristics by using the FG; however, it is not advantageous for 3D stacking due to a thicker memory film than CTL, which limits the scaling of channel hole dimension.

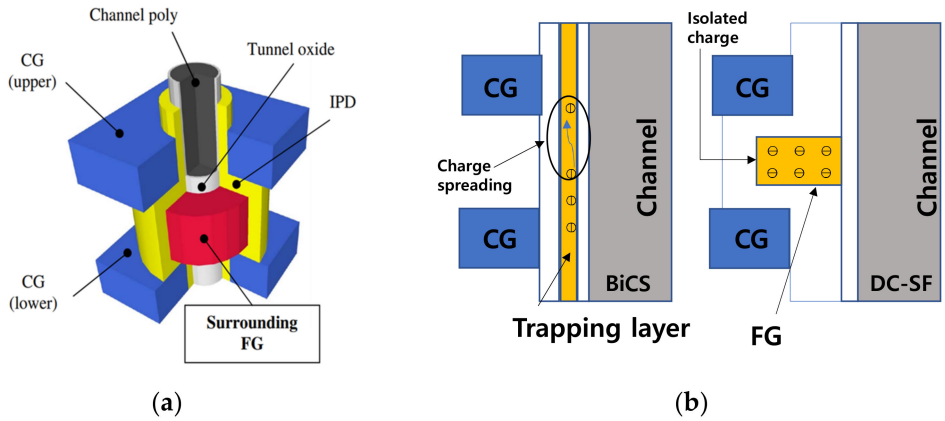


Figure 7. (**a**) Aerial view of DC-SF structure [8], Copyright IEEE, 2010. (**b**) Charge spreading in BiCS and DC-SF structures.

Another 3D NAND structure with an FG is the HC-FG structure, as shown in Figure 8a [3]. Unlike in the DC-SF structure, horizontal channels are stacked in the HC-FG architecture; however, the unit cell is not surrounded by CGs. Consequently, the FG cells can be stacked by the channel-first process, similar to that in a conventional 2D planar flash array, and a 3D structure can be implemented at a low cost. In addition, the HC-FG structure is combined with a layer select transistor (LST), as shown in Figure 8b, to enable additional bit cost scaling. The HC-FG and LST structures are connected via an SSL and share the gate electrodes. The LST structure requires a simple and low-cost process, because impurity regions can be incorporated simultaneously using a self-aligned method, owing to a stair-like structure.

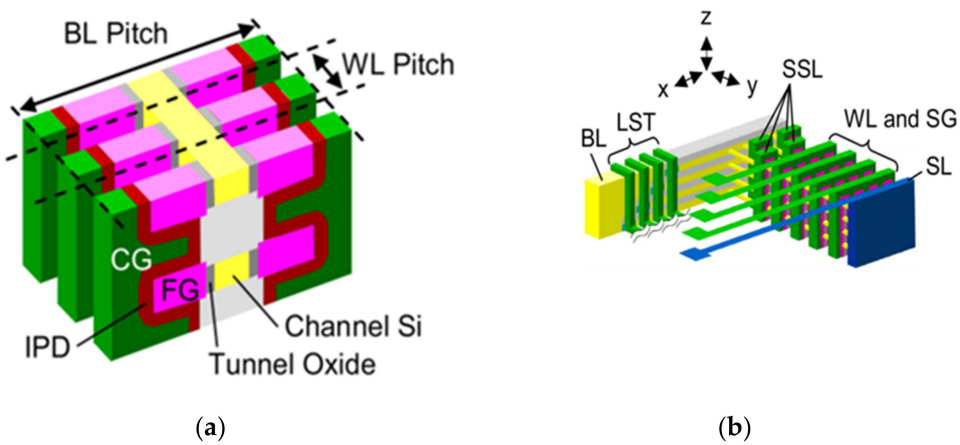
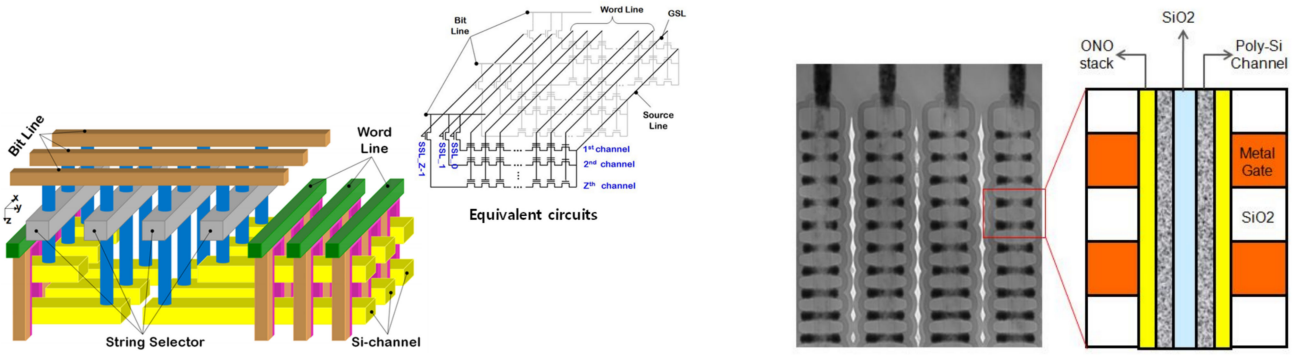


Figure 8. (**a**) Cell structure and (**b**) schematic of HC-FG NAND flash structure [3], Copyright IEEE, 2013.

The VG NAND architecture has both WL and SSL in the same active layer; therefore, the cell density becomes worse as the stack layer increases. This is improved in a hybrid 3D NAND flash, in which the density is increased by placing the WL and the SSL in the same string, as shown in Figure 9a [9]. In this hybrid structure, the GAA string selector and the metal-alumina–nitride-oxide–silicon (MANOS) cells form string lines, and each channel layer is connected to the BL through the SSL. This structure allows both a vertical channel of the GAA string selectors and horizontal channels of the MANOS cells. The cell string exhibits high channel controllability, owing to GAA structure, and the double-gate memory cell provides a sufficient threshold voltage (V_T) window for multibit operation. Figure 9b shows the SMArT structure [10], which minimizes the stack height using the ONO layer and employs the low-resistance of the metal gate by employing the gate-last

process method. The SMArT structure shows superior V_T distribution and endurance compared to planar FG cells; however, the retention characteristics need to be improved.



(**a**) (**b**)

Figure 9. (**a**) Aerial view of a hybrid 3D NAND flash cell with equivalent circuits [9], Copyright IEEE, 2011. (**b**) Cross-section view of a SMArT structure [10], Copyright IEEE, 2012.

In general, the channel-stacked method can have the same pitch size as a 2D NAND architecture; however, it has an issue that the SSL for the target cell access (decoding) increases as the stack layer increases. To address this issue, Macronix proposed several structures for decoding the SSL [12–16,36]. Figure 10 shows the architecture of an island-gate decoded VG structure with channel-stacked BE-SONOS (bandgap engineered SONOS) [37], containing an island gate for the SSL selection [12]. Unlike the VG NAND structure, the presence of an n-type doped poly-Si buried channel allows a junction-free structure, and no additional junction implantation is required. In the island-gate decoded VG structure, the intercepts of the WL, BL, and SSL planes are used for cell decoding, and the WLs and BL are grouped into planes.

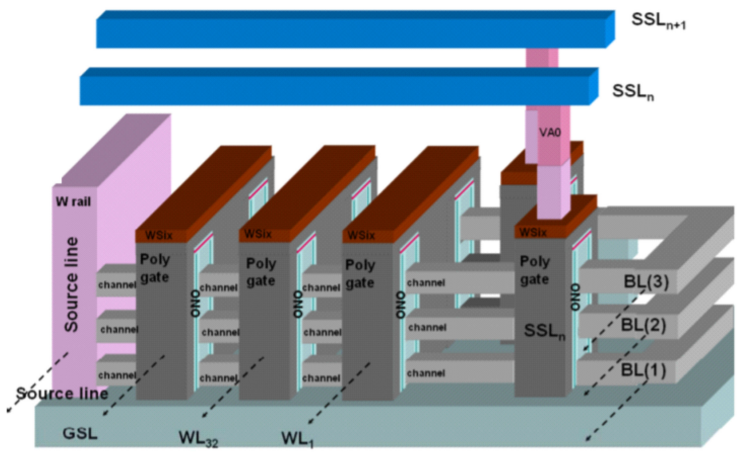
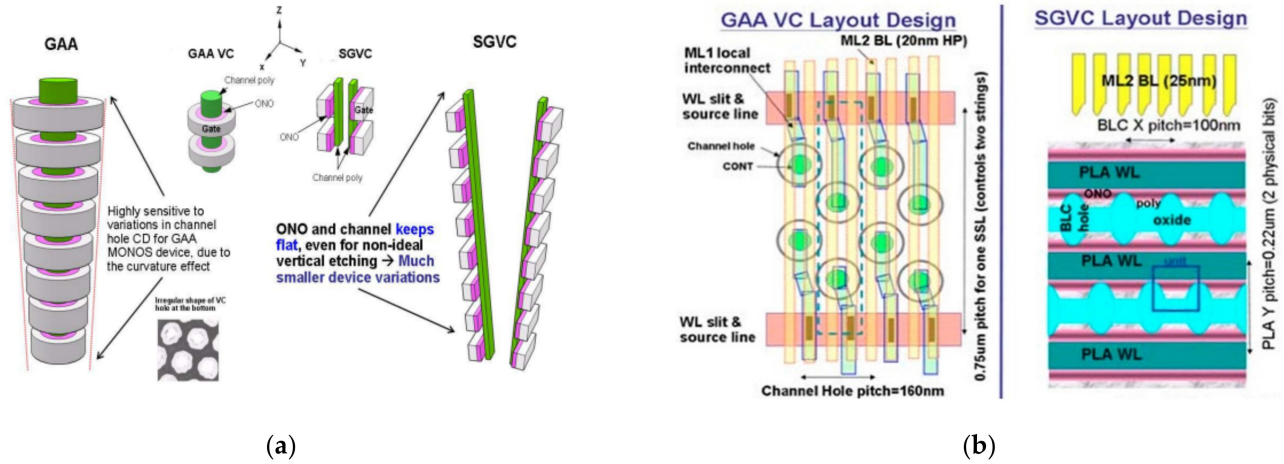


Figure 10. Schematic of island-gate decoded VG structure [12], Copyright IEEE, 2010.

Another type of gate-stacked 3D NAND structure of Macronix is a single-gate vertical channel (SGVC) [38]. In the SGVC structure, the cell transistor is not based on a nanowire channel of a GAA structure but instead on a flat channel in the WL trench. Figure 11a presents a comparison of GAA and the SGVC cell structure. The SGVC structure is a flat channel-based charge trapping device and has an initial V_T distribution and short channel effect similar to that of GAA structure, owing to the ultra-thin body. Compared to the curvature-shaped GAA structure, the SGVC cell structure advantages are in the formation of the critical dimension and channel hole etching. Figure 11b shows the layouts

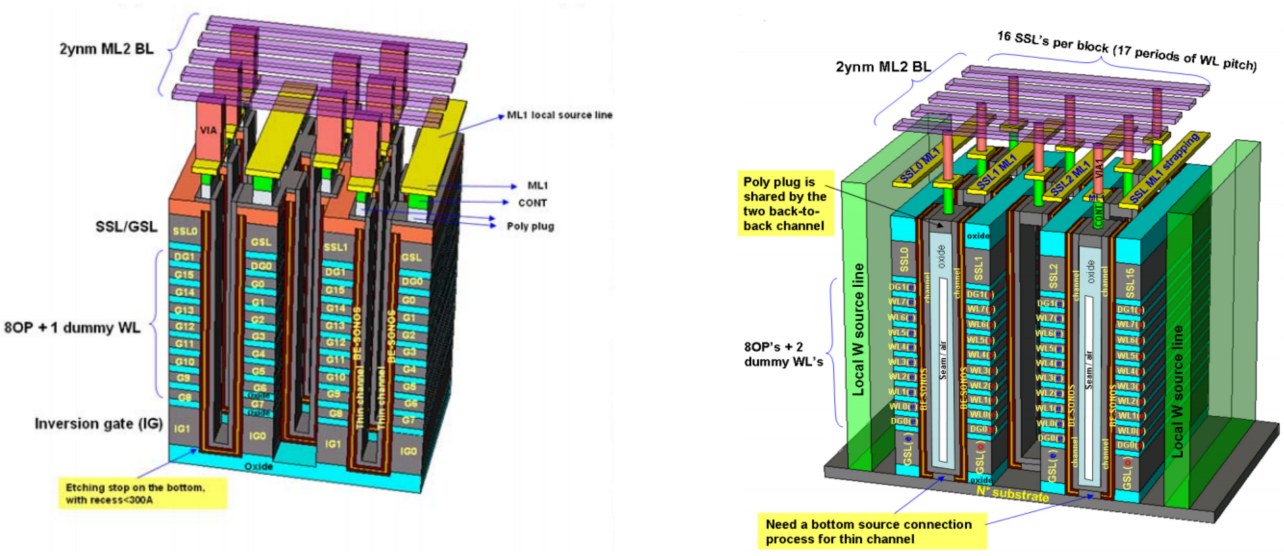
of the GAA VC and SGVC structures. Compared to the GAA VC structure, the SGVC has approximately 2.4 times the memory density in the same stack layer [38–41].



(**a**) (**b**)

Figure 11. (**a**) Structural and (**b**) layout comparison of GAA and SGVC 3D NAND flash [41], Copyright IEEE, 2015.

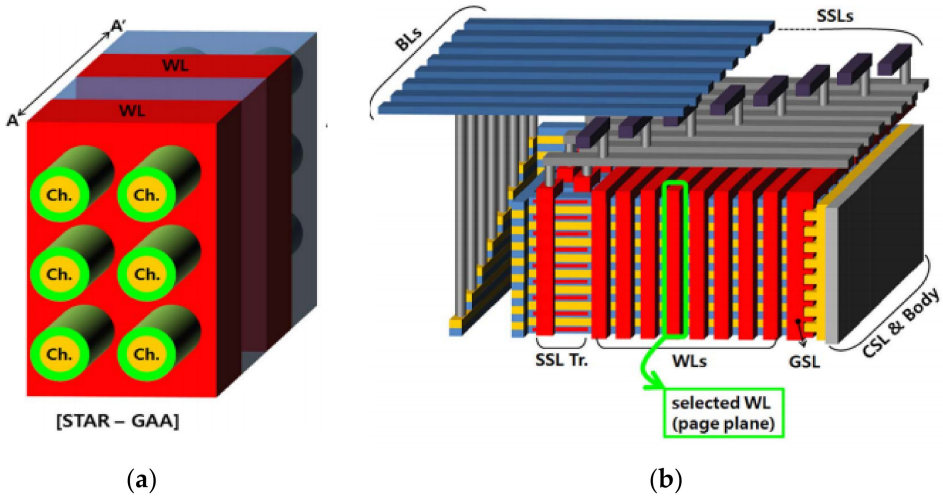
Figure 12a,b show the U-turn and bottom-source SGVC architectures, respectively [39,40]. In the former, an ONO CTL and poly channels are deposited on the WL trench. The thin poly channel layers are separated by the BL cut process, and the CTL and channel are controlled by independent WLs. Owing to the use of a flat channel cell transistor, the scalability of the U-turn SGVC structure is comparable to that of 2D NAND flash, and its etching controllability is better than that of a GAA structure. The bottom-source structure has almost the same characteristics as the U-turn structure, except thin poly channels are connected to the bottom n^+ substrate. The gate-first process for the bottom-source SGVC fabrication, similar to the BiCS, causes ONO layer damage, and a two-step poly channel process is required to protect the ONO layer. However, the U-turn structure produced by a one-step poly channel process has an extremely thin body structure and a better subthreshold swing distribution [38–42].



(**a**) (**b**)

Figure 12. Schematics of (**a**) U-turn string and (**b**) bottom-source SGVC 3D NAND architecture [41], Copyright IEEE, 2016.

Figure 13a shows the STAR NAND flash architecture with a GAA unit cell structure [17]. Because the STAR NAND flash is based on the channel-stacked method, it can have the same minimum cell size as the conventional 2D planar NAND flash structure. Single-crystalline Si nanowire channels are stacked by employing a Si/SiGe epitaxial growth process. However, SiGe-selective etching is required for nanowire channel formation and isolation after the multistacking of the Si/SiGe layers. In the gate-stacked method, poly-Si is generally used as the channel material, because epitaxial growth is difficult, due to narrow and deep channel holes. Since single-crystalline Si is used as a channel layer in this structure, the STAR NAND flash can have a relatively uniform V_T and stable BL current distributions. Compared to the VG NAND architecture, the single-crystalline Si channel solves the uniformity issues caused by the defects and the grain boundaries of the poly-Si channel, and it exhibits a better performance with the GAA cell structure. Figure 13b shows the unit structure of the STAR NAND flash [43]. The channel-stacked 3D NAND flash structure requires SSLs for additional address access, unlike a 2D planar NAND flash, and the number of SSLs increases as the stack layer increases.

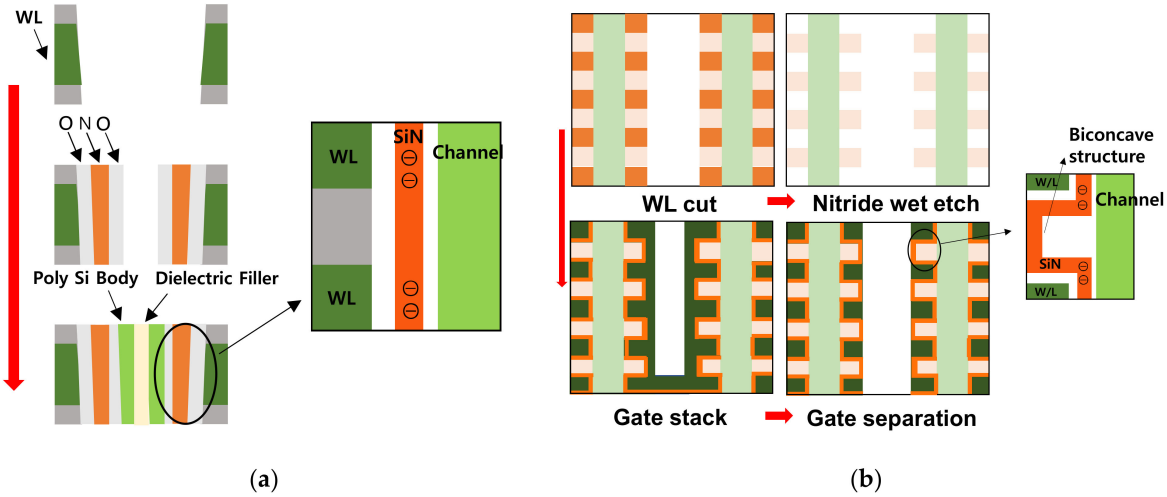


(**a**) (**b**)

Figure 13. (**a**) Aerial view of and (**b**) unit structure of STAR NAND flash [43], Copyright IEEE, 2012.

3. Fabrication Methods of 3D NAND Flash

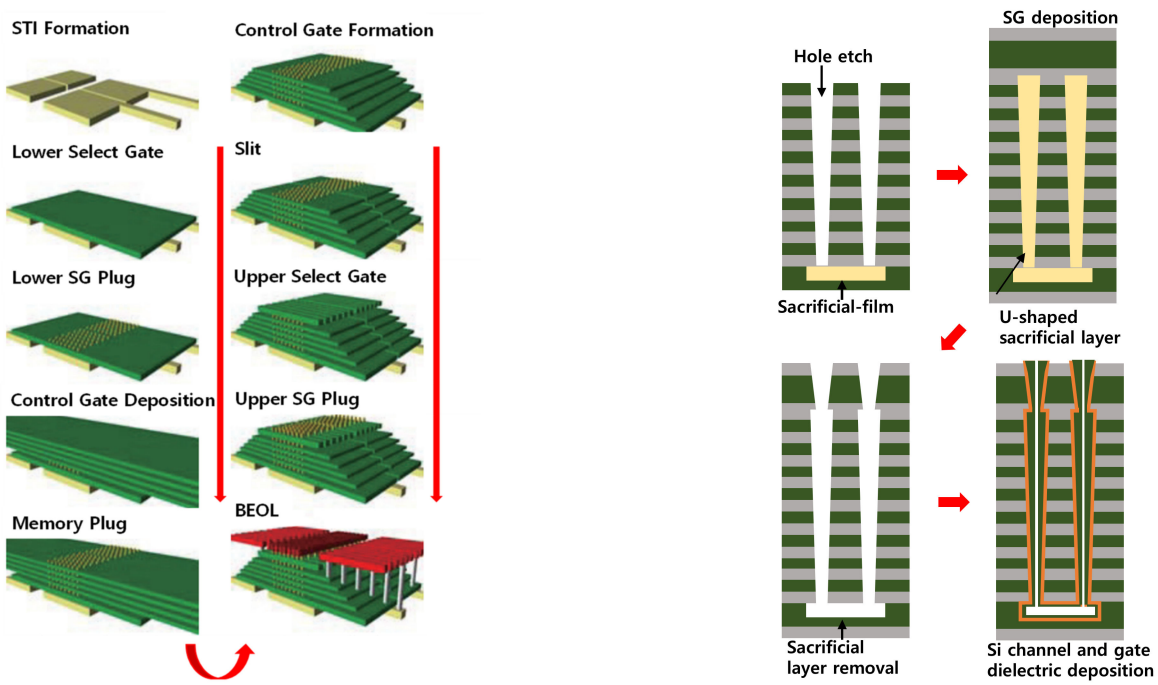
Gate-stacked 3D NAND architectures can be fabricated using two methods: gate-first and -last, and the most representative structures fabricated by the gate-first and -last methods are BiCS [1] and TCAT [4], respectively. Figure 14a shows the gate-first process, in which WLs are stacked first, and subsequently, channel holes are etched. The channel holes are filled with a charge-trapping dielectric and poly-Si channel layers [31]. Figure 14b shows the gate-last (gate replacement) process, in which oxide/nitride multilayers are deposited, which is followed by hole etching and channel poly-Si deposition. An additional process step, called the WL cut, is performed between the channel poly plugs. The WL cut is performed by dry etching; the nitride layer is removed, and the gate dielectric layers and metal gate are deposited. In general, the use of metal gate provides a faster erase speed, lower program/erase voltage, and a wider V_T margin by suppressing unwanted backward Fowler–Nordheim tunneling current [44]. The gate-first method of the BiCS [1] structure has a problem in that the hole-etch size is affected by the gate dielectric layers. In contrast, the biconcave produced by the WL cut process of the gate-last method prevents lateral charge loss [45] but increases a process difficulty [4].



(**a**) (**b**)

Figure 14. (**a**) Gate-first method of BiCS flash and (**b**) gate-last method of TCAT with a WL cut process.

Figure 15a shows the fabrication process of the BiCS structure. LSG, memory string, and USG transistors are fabricated separately, and poly-Si is used as the gate material. A transistor channel and a memory plug are formed by hole etching, using a punch-through method. Silicon nitride and tetraethoxysilane (TEOS) layers are formed by low-pressure chemical vapor deposition (LPCVD) for an ONO stack in the etched hole. Arsenic ions are implanted and activated in the LSG source and drain. The CG formation proceeds in the reverse order of the conventional SONOS deposition. The edge of the CG is etched in the form of stair-like steps by reactive ion etching. The entire layers are separated into two blocks through a slit to minimize disturbance. The USG operates as a row address selector using a line pattern and is simultaneously connected to the via hole, BL, and peripheral circuit [29].



(**a**) (**b**)

Figure 15. Process flow of (**a**) a BiCS structure [29], Copyright IEEE, 2007, and (**b**) a PBiCS structure with a pipe connection.

Figure 15b shows the process flow of the PBiCS structure string and the PC formation. A memory hole is formed by hole etching, and a sacrificial film is deposited. A PC is formed on the sacrificial film, which is followed by memory layer deposition. After the SG formation, the U-shaped sacrificial layer is removed and the memory films and silicon-body layer are deposited for CG formation on the memory hole, which allows for the pipe-shaped NAND string structure with better reliability characteristics [2].

Figure 16a shows the process flow of the VRAT structure. Firstly, oxide-nitride stacks are deposited on the Si mesa in order, and an active region is defined by patterning and etching. An undercut is created in each oxide layer by wet etching using a buffered oxide etchant (BOE), where each flash cell would be placed. All the gate stacks, including oxide-nitride-oxide and the poly-Si gate are sequentially deposited by LPCVD, with an improved step coverage. Subsequently, only the WL electrodes remain in the undercut region by the etch-back process, and they are separated from each other. The exposed part of the multi-stacked layers on the formed Si mesa is flattened by the CMP process, and the WL electrode is exposed. Then, each string is isolated by a poly-Si etch, followed by the contact process for WLs and BLs [35]. The VSAT structure simplifies the overall process compared with the VRAT by adopting a gate-first method, as shown in Figure 16b. Gate electrodes and isolating films (nitride) are sequentially deposited on a Si mesa. Subsequently, an active region is formed, and the CMP process is conducted immediately without the VRAT undercut process, leading each WL to be exposed on the same plane. Subsequently, gate dielectric layers and a poly-Si layer as the channel materials are deposited, and each vertical string is separated by lithography and etching [5].

(**a**)

(**b**)

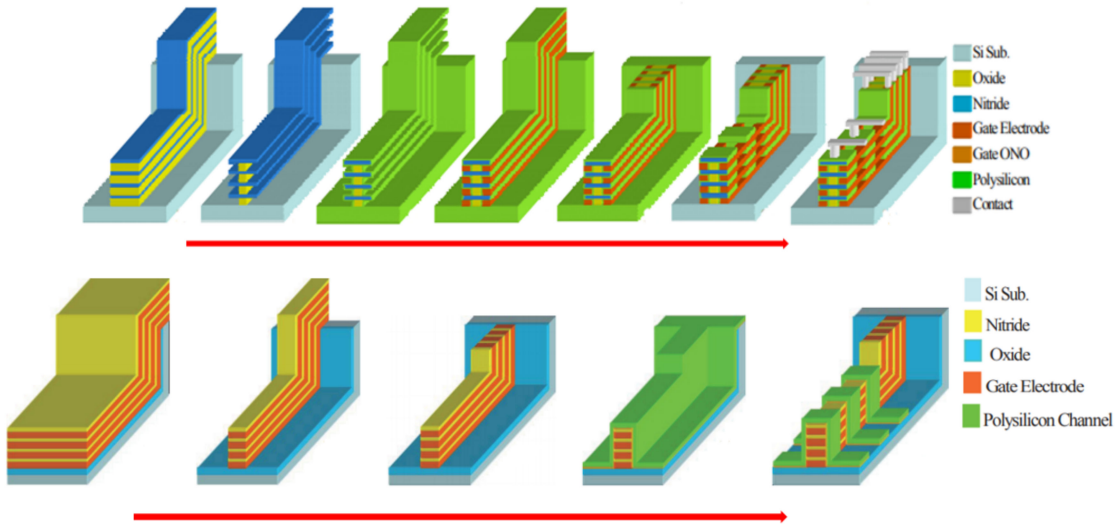


Figure 16. Process flow of (**a**) VRAT [35], Copyright IEEE, 2008, and (**b**) a VSAT structure [5], Copyright IEEE, 2009.

The direction of WL and BL for the VG NAND structure is changed in a channel-stacked structure for simple WL interconnection, as shown in Figure 17. An n^+ poly-Si BL is formed first, then n^+ poly-Si WLs are formed on the top of it in a crossing direction. Subsequently, p-type poly-Si multi-active layers are deposited, and n-type ion implantation is performed to form an SSL layer. After the deposition of an interlayer dielectric between the multi-active layers, an ONO stack is deposited over the active regions, and the gate is formed vertically. Thanks to the buried BLs and WLs formed at the early stage of the process flow, the interconnection to them can be easily accomplished [6].

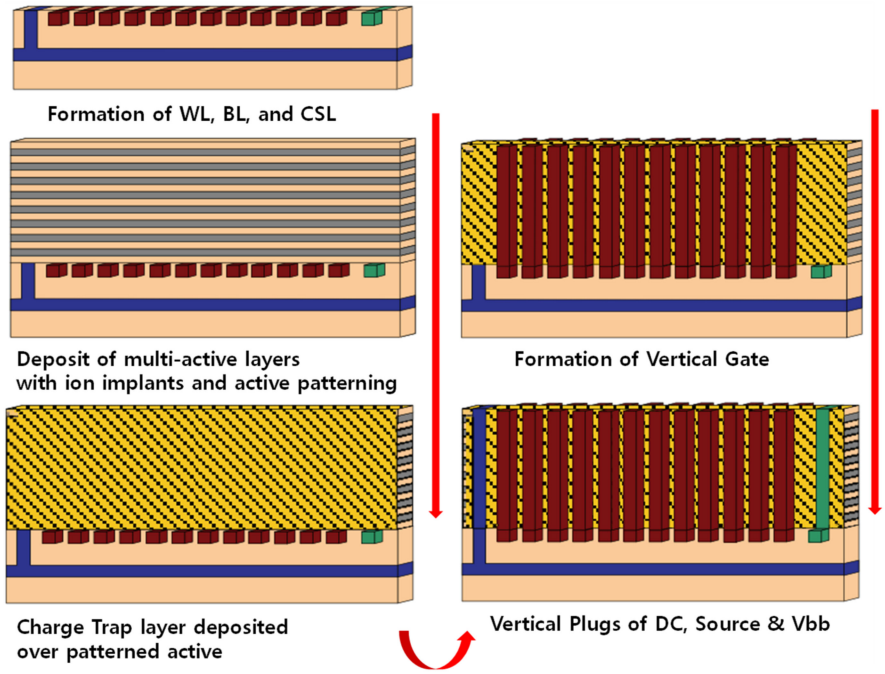


Figure 17. Process flow of a VG NAND structure [6], Copyright IEEE, 2009.

The DC-SF NAND flash structure utilizes a surrounding floating gate as a charge storage layer instead of a CTL, as shown in Figure 18a. Oxide and poly-Si layers are deposited first. Subsequently, a hole etch is done for channel region, and the oxide layer is recessed to form FG regions, respectively. The IPD and FG layers are deposited in order as a blocking oxide and charge storage layer, respectively, and each FG is isolated by wet etching. Lastly, a tunnel oxide and poly-Si layers are deposited in the hole channel [8]. Thanks to the FG structure, the DC-SF boasts better retention characteristics than other 3D SONOS flash architectures; however, the use of the DC-SF poly-Si gate causes several issues, including a high gate resistance, the IPD damage during the FG separation process, field confinement due to the horn-shaped FG, and GIDL during erasing due to the floating channel.

In order to ease them, the MCGL process is demonstrated as shown in Figure 18b. First, oxide and nitride layers are deposited on n^+/p-Si substrate. Subsequently, a channel hole is etched, and FGs for individual flash cells are formed at the recessed region after isotropic oxide etching. Then, a tunnel oxide is deposited, and a hole is etched on the Si substrate for channel contact. The poly-Si layer is filled in the channel hole and directly connected to the substrate. Following this, the nitride is removed, and the gate stack, including a high-k IPD film and a tungsten metal gate, is deposited on the FG. In this structure, the tungsten metal gate gives a low WL resistance compared to a poly-Si gate, and the bulk erase operation becomes possible thanks to the direct connection between the substrate and the poly-Si channel [11].

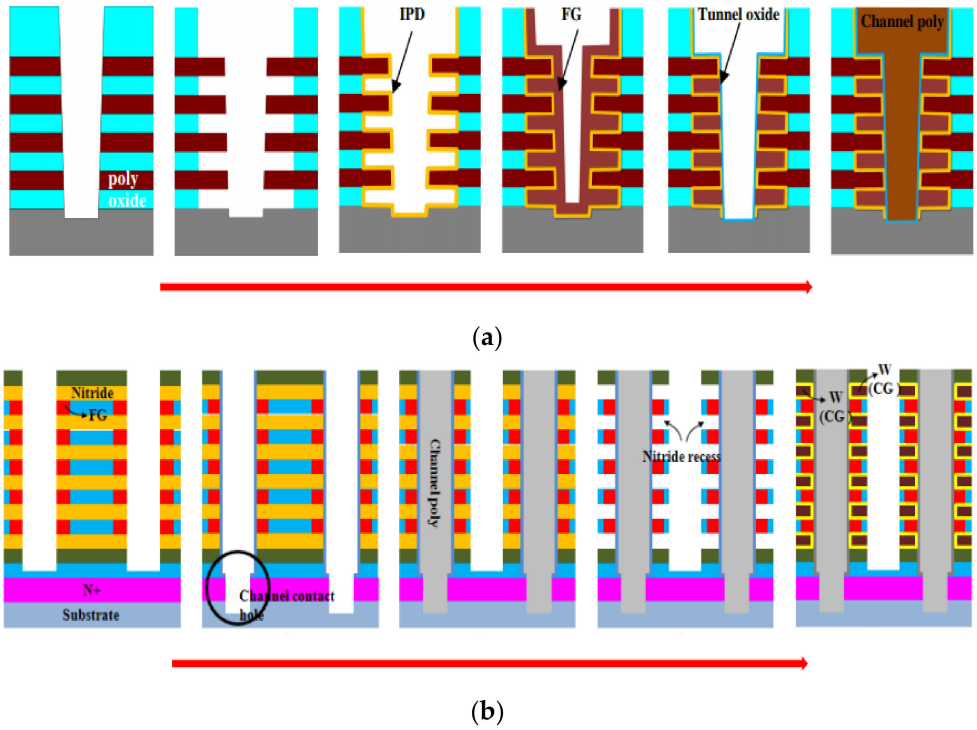


Figure 18. Process flow of (**a**) DC-SF [8], Copyright IEEE, 2010, and (**b**) MCGL [11], Copyright IEEE, 2012.

The STAR NAND flash has a unique feature of single crystalline Si nanowire channels, and its fabrications method is described in Figure 19. Initially, Si/SiGe layers are epitaxially grown, and an active region is formed by using oxide/poly-Si/oxide layers as an etching hard mask. Subsequently, n-type and p-type ions are implanted in the left BL region and the right body region, respectively. Then, an additional oxide layer is deposited and etched as a buttress to prevent the collapse of long Si channels during the selective SiGe layer etch. After the selective SiGe etching is carried out, an oxide layer is re-deposited to fill the gap between the Si channels. Oxide patterning for the WL region is followed by isotropic etching of oxide to expose the Si channels and make a gate stack. The width of the buttress oxide (B) should be greater than the width of the oxide (A) of the channel region to be removed so that the buttress oxide can remain with the reduced width (B→C). Subsequently, the gate stacks, including ONO dielectrics and tungsten, are deposited, and planarization is performed to form WL, SSL, and GSL gates. The flash cell, SSL, and GSL transistors are self-aligned using the damascene gate process. Since the STAR architecture is based on the channel-stacked structure, a stair-shaped BL contact is needed [43]. Thanks to the single crystalline Si channel, the STAR can feature better electrical characteristics compared with poly-Si channel flash structures, but it has a difficult fabrication method. In addition, it is hard to increase the number of stacked layers, considering Si/SiGe sequential epitaxial growth.

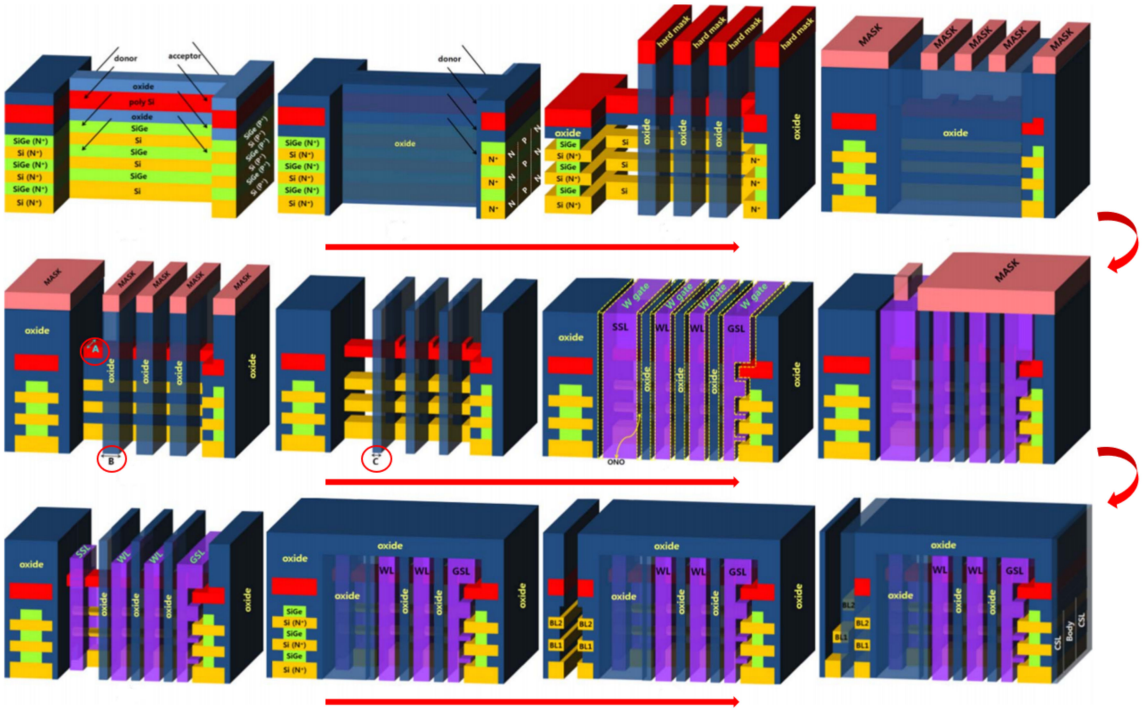


Figure 19. Process flow of STAR NAND flash [43], Copyright IEEE, 2012.

4. Conclusions

Currently, the demand for NAND flash memory continues to grow. It has various applications, such as in solid-state drives, and it is widely used in mobile devices requiring data storage. Over time, the planar flash array has evolved into a 3D integrated architecture to increase memory capacity and overcome scaling issues. With over 10 years of development, there has been a significant reduction in the cost per bit of 3D NAND flash. As the number of stack layers increases, a high aspect-ratio etching technology is required for hole formation, considering the fact that it is hard to reduce the hole critical dimension due to gate dielectric stacks, and there is a problem with peripheral circuits and WL thickness. Several efforts have been made to solve these issues, including etching technology with an extremely high aspect-ratio and a so-called four-dimensional NAND flash technology with peripheral circuit under a flash cell array. In addition, program methods have been proposed to reduce the cost per bit of flash instead of stacking layers and conducted to obtain the distribution margin of V_T for quadruple level cell (QLC) implementation [20,22,46–49]. Starting with the BiCS structure, we have reviewed various kinds of 3D NAND flash structures by classifying and comparing their structures and fabrication methods. Depending on the channel direction and gate formation, their fabrication methods and consequential electrical characteristics significantly differ, and vertical NAND structures with a charge trapping layer have been commercialized, thanks to their easy integration method and high stackablity. In addition, it is believed that etching technology with a high aspect-ratio and programming scheme for accurate multi-level operations should be further improved for the bit cost scaling of 3D NAND flash technologies. However, it is expected that there would be a physical limitation to increase the number of stack layers infinitely, even assuming excellent hole etching technology, and it is necessary to investigate how to solve this through structural changes or emerging memories. Various emerging memories, including resistive random access memory (RRAM) [50–59] and phase-change random access memory (PCRAM) [60–67], have been widely investigated for faster speed and lower operating voltage, but the reliability is still considered one of the most important factors to be solved for the competition with mainstream memories. The 3D integration of emerging memory devices should also be investigated to replace 3D NAND flash, and it can be inspired by

the architectures and fabrication methods of 3D NAND flash technologies. In addition, we believe that it is important to investigate memory computing applications, including neuromorphic systems and processing-in-memory using flash technology, in order to expand the function and capability of 3D NAND flash beyond data storage [68–77].

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Komori, Y.; Kido, M.; Kito, M.; Katsumata, R.; Fukuzumi, Y.; Tanaka, H.; Nagata, Y.; Ishiduki, M.; Aochi, H.; Nitayama, A. Disturbless flash memory due to high boost efficiency on BiCS structure and optimal memory film stack for ultra high density storage device. In Proceedings of the 2008 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 15–17 December 2008; pp. 851–854.
2. Katsumata, R.; Kito, M.; Fukuzumi, Y.; Kido, M.; Tanaka, H.; Komori, Y.; Ishiduki, M.; Matsunami, J.; Fujiwara, T.; Nagata, Y.; et al. Pipe-shaped BiCS flash memory with 16 stacked layers and multi-level-cell operation for ultra high density storage devices. In Proceedings of the 2009 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2009; pp. 136–137.
3. Sakuma, K.; Kusai, H.; Fujii, S.; Koyama, M. Highly Scalable Horizontal Channel 3-D NAND Memory Excellent in Compatibility with Conventional Fabrication Technology. *IEEE Electron. Device Lett.* **2013**, *34*, 1142–1144. [CrossRef]
4. Jang, J.; Kim, H.-S.; Cho, W.; Cho, H.; Kim, J.; Shim, S.I.; Jang, Y.; Jeong, J.-H.; Son, B.-K.; Kim, D.W.; et al. Vertical cell array using TCAT (Terabit Cell Array Transistor) technology for ultra high density NAND flash memory. In Proceedings of the 2009 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2009; pp. 192–193.
5. Kim, J.; Hong, A.J.; Kim, S.M.; Song, E.B.; Park, J.H.; Han, J.; Choi, S.; Jang, D.; Moon, J.-T.; Wang, K.L. Novel Vertical-Stacked-Array-Transistor (VSAT) for ultra-high-density and cost-effective NAND flash memory devices and SSD (Solid State Drive). In Proceedings of the 2009 Symposium on VLSI Technology, Kyoto, Japan, 15–17 June 2009; pp. 186–187.
6. Kim, W.; Choi, S.; Sung, J.; Lee, T.; Park, C.; Ko, H.; Jung, J.; Yoo, I.; Park, Y. Multi-layered vertical gate NAND flash overcoming stacking limit for terabit density storage. In Proceedings of the 2009 Symposium on VLSI Technology, Kyoto, Japan, 15–17 June 2009; pp. 188–189.
7. Park, K.-T.; Nam, S.; Kim, D.; Kwak, P.; Lee, D.; Choi, Y.-H.; Choi, M.-H.; Kwak, D.-H.; Kim, D.-H.; Kim, M.-S.; et al. Three-Dimensional 128 Gb MLC Vertical nand Flash Memory With 24-WL Stacked Layers and 50 MB/s High-Speed Programming. *IEEE J. Solid State Circuits* **2015**, *50*, 204–213. [CrossRef]
8. Whang, S.; Lee, K.; Shin, D.; Kim, B.Y.; Kim, M.; Bin, J.; Han, J.; Kim, S.; Lee, B.; Jung, Y.; et al. Novel 3-dimensional Dual Control-gate with Surrounding Floating-gate (DC-SF) NAND flash cell for 1Tb file storage application. In Proceedings of the 2010 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 6–8 December 2010; pp. 29.7.1–29.7.4.
9. Choi, E.-S.; Yoo, H.-S.; Joo, H.-S.; Cho, G.-S.; Park, S.-K.; Lee, S.-K. A Novel 3D Cell Array Architecture for Terra-bit NAND Flash Memory. In Proceedings of the IEEE International Memory Workshop (IMW), Monterey, CA, USA, 22–25 May 2011; pp. 1–4.
10. Choi, E.-S.; Park, S.-K. Device considerations for high density and highly reliable 3D NAND flash cell in near future. In Proceedings of the 2012 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 10–13 December 2012; pp. 9.4.1–9.4.4.
11. Noh, Y.; Ahn, Y.; Yoo, H.; Han, B.; Chung, S.; Shim, K.; Lee, K.; Kwak, S.; Shin, S.; Choi, I.; et al. A New Metal Control Gate Last process (MCGL process) for high performance DC-SF (Dual Control gate with Surrounding Floating gate) 3D NAND flash memory. In Proceedings of the 2012 Symposium on VLSI Technology, Honolulu, HI, USA, 12–14 June 2012; pp. 19–20.
12. Lue, H.-T.; Hsu, T.-H.; Hsiao, Y.-H.; Hong, S.P.; Wu, M.T.; Hsu, F.H.; Lien, N.Z.; Wang, S.-Y.; Hsieh, J.-Y.; Yang, L.-W.; et al. A highly scalable 8-layer 3D vertical-gate (VG) TFT NAND Flash using junction-free buried channel BE-SONOS device. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 131–132.
13. Hung, C.-H.; Lue, H.-T.; Chang, K.-P.; Chen, C.-P.; Hsiao, Y.-H.; Chen, S.-H.; Shih, Y.-H.; Hsieh, K.-Y.; Yang, M.; Lee, J.; et al. A highly scalable vertical gate (VG) 3D NAND Flash with robust program disturb immunity using a novel PN diode decoding structure. In Proceedings of the 2011 Symposium on VLSI Technology, Kyoto, Japan, 14–16 June 2011; pp. 68–69.

14. Chang, K.-P.; Lue, H.-T.; Chen, C.-P.; Chen, C.-F.; Chen, Y.-R.; Hsiao, Y.-H.; Hsieh, C.-C.; Shih, Y.-H.; Yang, T.; Chen, K.-C.; et al. Memory Architecture of 3D Vertical Gate (3DVG) NAND Flash Using Plural Island-Gate SSL Decoding Method and Study of It's Program Inhibit Characteristics. In Proceedings of the IEEE International Memory Workshop (IMW), Milan, Italy, 20–23 May 2012; pp. 1–4.
15. Chen, S.H.; Lue, H.T.; Shih, Y.H.; Chen, C.F.; Hsu, T.H.; Chen, Y.R.; Hsiao, Y.H.; Huang, S.C.; Chang, K.P.; Hsieh, C.C.; et al. A highly scalable 8-layer Vertical Gate 3D NAND with split-page bit line layout and efficient binary-sum MiLC (Minimal Incremental Layer Cost) staircase contacts. In Proceedings of the 2012 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 10–13 December 2012; pp. 2.3.1–2.3.4.
16. Lue, H.-T.; Du, P.-Y.; Chen, W.-C.; Yeh, T.-H.; Chang, K.-P.; Hsiao, Y.-H.; Shih, Y.-H.; Hung, C.-H.; Lu, C.-Y. A novel dual-channel 3D NAND flash featuring both N-channel and P-channel NAND characteristics for bit-alterable Flash memory and a new opportunity in sensing the stored charge in the WL space. In Proceedings of the 2013 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 9–11 December 2013; pp. 3.7.1–3.7.4.
17. Yun, J.-G.; Kim, G.; Lee, J.-E.; Kim, Y.; Shim, W.B.; Lee, J.-H.; Shin, H.; Lee, J.D.; Park, B.-G. Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. *IEEE Trans. Electron. Devices* **2011**, *58*, 1006–1014.
18. Kim, C.; Kim, D.-H.; Jeong, W.; Kim, H.-J.; Park, I.H.; Park, H.-W.; Lee, J.; Park, J.; Ahn, Y.-L.; Lee, J.Y.; et al. A 512-Gb 3-b/Cell 64-Stacked WL 3-D-NAND Flash Memory. *IEEE J. Solid State Circuits* **2018**, *53*, 124–133. [CrossRef]
19. Yamashita, R.; Magia, S.; Higuchi, T.; Yoneya, K.; Yamamura, T.; Mizukoshi, H.; Zaitsu, S.; Yamashita, M.; Toyama, S.; Kamae, N.; et al. A 512 Gb 3b/cell flash memory on 64-word-line-layer BiCS technology. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 196–197.
20. Kang, D.; Kim, M.; Jeon, S.C.; Jung, W.; Park, J.; Choo, G.; Shim, D.-K.; Kavala, A.; Kim, S.-B.; Kang, K.-M.; et al. A 512 Gb 3-bit/Cell 3D 6th-Generation V-NAND Flash Memory with 82 MB/s Write Throughput and 1.2 Gb/s Interface. In Proceedings of the 2019 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 17–21 February 2019; pp. 216–217.
21. Shibata, N.; Kanda, K.; Shimizu, T.; Nakai, J.; Nagao, O.; Kobayashi, N.; Miakashi, M.; Nagadomi, Y.; Nakano, T.; Kawabe, T.; et al. A 1.33-Tb 4-Bit/Cell 3-D Flash Memory on a 96-Word-Line-Layer Technology. *IEEE J. Solid State Circuits* **2019**, *55*, 178–188. [CrossRef]
22. Cho, J.; Kang, D.C.; Park, J.; Nam, S.-W.; Song, J.-H.; Jung, B.-K.; Lyu, J.; Lee, H.; Kim, W.-T.; Jeon, H.; et al. A 512 Gb 3b/Cell 7th-Generation 3D-NAND Flash Memory with 184 MB/s Write Throughput and 2.0 Gb/s Interface. In Proceedings of the 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 13–22 February 2021; pp. 426–427.
23. Park, J.-W.; Kim, D.; Ok, S.; Park, J.; Kwon, T.; Lee, H.; Lim, S.; Jung, S.-Y.; Choi, H.; Kang, T.; et al. A 176-Stacked 512 Gb 3b/Cell 3D-NAND Flash with 10.8 Gb/mm^2 Density with a Peripheral Circuit Under Cell Array Architecture. In Proceedings of the 2021 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 13–22 February 2021; pp. 422–423.
24. Lue, H.-T.; Du, P.-Y.; Chen, W.-C.; Lee, Y.-C.; Hsu, T.-H.; Yeh, T.-H.; Chang, K.-P.; Hsieh, C.-C.; Huang, C.; Lee, G.-R.; et al. A 128 Gb (MLC)/192 Gb (TLC) single-gate vertical channel (SGVC) architecture 3D NAND using only 16 layers with robust read disturb, long-retention and excellent scaling capability. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 19.1.1–19.1.4.
25. Lue, H.-T.; Chen, S.-H.; Shih, Y.-H.; Hsieh, K.-Y.; Lu, C.-Y. Overview of 3D NAND Flash and progress of vertical gate (VG) architecture. In Proceedings of the IEEE International Conference on Solid-State and Integrated Circuit Technology, Xi'an, China, 29 October–1 November 2012; pp. 1–4.
26. Du, P.-Y.; Lue, H.-T.; Shih, Y.-H.; Hsieh, K.-Y.; Lu, C.-Y. Overview of 3D NAND Flash and progress of split-page 3D vertical gate (3DVG) NAND architecture. In Proceedings of the IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Guilin, China, 28–31 October 2014; pp. 1–4.
27. Nitayama, A.; Aochi, H. Bit Cost Scalable (BiCS) technology for future ultra high density storage memories. In Proceedings of the 2013 Symposium on VLSI Technology, Kyoto, Japan, 11–13 June 2013; pp. 60–61.
28. Fukuzumi, Y.; Katsumata, R.; Kito, M.; Kido, M.; Sato, M.; Tanaka, H.; Nagata, Y.; Matsuoka, Y.; Iwata, Y.; Aochi, H.; et al. Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory. In Proceedings of the 2007 IEEE International Conference on Electron Devices Meeting (IEDM), Washington, DC, USA, 10–12 December 2007; pp. 449–452.
29. Tanaka, H.; Kido, M.; Yahashi, K.; Oomura, M.; Katsumata, R.; Kito, M.; Fukuzumi, Y.; Sato, M.; Nagata, Y.; Matsuoka, Y.; et al. Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory. In Proceedings of the 2007 Symposium on VLSI Technology, Kyoto, Japan, 12–14 June 2007; pp. 14–15.
30. Aochi, H. BiCS Flash as a Future 3D Non-Volatile Memory Technology for Ultra High Density Storage Devices. In Proceedings of the IEEE International Memory Workshop (IMW), Monterey, CA, USA, 10–14 May 2009; pp. 1–2.
31. Ishiduki, M.; Fukuzumi, Y.; Katsumata, R.; Kito, M.; Kido, M.; Tanaka, H.; Komori, Y.; Nagata, Y.; Fujiwara, T.; Maeda, T.; et al. Optimal device structure for Pipe-shaped BiCS Flash memory for ultra high density storage device with excellent performance and reliability. In Proceedings of the 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 7–9 December 2009; pp. 27.3.1–27.3.4.
32. Maeda, T.; Itagaki, K.; Hishida, T.; Katsumata, R.; Kito, M.; Fukuzumi, Y.; Kido, M.; Tanaka, H.; Komori, Y.; Ishiduki, M.; et al. Multi-stacked 1G cell/layer Pipe-shaped BiCS flash memory. In Proceedings of the 2009 Symposium on VLSI Circuits, Kyoto, Japan, 16–18 August 2009; pp. 22–23.

33. Micheloni, R.; Crippa, L.; Zambelli, C.; Olivo, P. Architectural and Integration Options for 3D NAND Flash Memories. *Computers* **2017**, *6*, 27. [CrossRef]
34. Kim, J.; Hong, A.J.; Kim, S.M.; Shin, K.-S.; Song, E.B.; Hwang, Y.; Xiu, F.; Galatsis, K.; Chui, C.O.; Candler, R.N.; et al. A stacked memory device on logic 3D technology for ultra-high-density data storage. *Nanotechnology* **2011**, *22*, 254006. [CrossRef]
35. Kim, J.; Hong, A.J.; Ogawa, M.; Ma, S.; Song, E.B.; Lin, Y.-S.; Han, J.; Chung, U.-I.; Wang, K.L. Novel 3-D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE). In Proceedings of the 2008 Symposium on VLSI Technology, Honolulu, HI, USA, 17–19 June 2008; pp. 122–123.
36. Chen, C.-P.; Lue, H.-T.; Chang, K.-P.; Hsiao, Y.-H.; Hsieh, C.-C.; Chen, S.-H.; Shih, Y.-H.; Hsieh, K.-Y.; Yang, T.; Chen, K.C.; et al. A highly pitch scalable 3D vertical gate (VG) NAND flash decoded by a novel self-aligned independently controlled double gate (IDG) string select transistor (SSL). In Proceedings of the 2012 Symposium on VLSI Technology, Honolulu, HI, USA, 12–14 June 2012; pp. 91–92.
37. Lue, H.-T.; Wang, S.-Y.; Lai, E.-K.; Shih, Y.-H.; Lai, S.-C.; Yang, L.-W.; Chen, K.-C.; Ku, J.; Hsieh, K.-Y.; Liu, R.; et al. BE-SONOS: A bandgap engineered SONOS with excellent performance and reliability. In Proceedings of the IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 5 December 2005; pp. 547–550.
38. Lue, H.-T.; Hsu, T.-H.; Wu, C.-J.; Chen, W.-C.; Yeh, T.-H.; Chang, K.-P.; Hsieh, C.-C.; Du, P.-Y.; Hsiao, Y.-H.; Jiang, Y.-W.; et al. A novel double-density, single-gate vertical channel (SGVC) 3D NAND Flash that is tolerant to deep vertical etching CD variation and possesses robust read-disturb immunity. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015; pp. 3.2.1–3.2.4.
39. Wu, C.-J.; Lue, H.-T.; Hsu, T.-H.; Hsieh, C.-C.; Chen, W.-C.; Du, P.-Y.; Chiu, C.-J.; Lu, C.-Y. Device Characteristics of Single-Gate Vertical Channel (SGVC) 3D NAND Flash Architecture. In Proceedings of the IEEE International Memory Workshop (IMW), Paris, France, 15–18 May 2016; pp. 1–4.
40. Lai, S.-C.; Lue, H.-T.; Hsu, T.-H.; Wu, C.-J.; Liang, L.-Y.; Du, P.-Y.; Chiu, C.-J.; Lu, C.-Y. A Bottom-Source Single-Gate Vertical Channel (BS-SGVC) 3D NAND Flash Architecture and Studies of Bottom Source Engineering. In Proceedings of the IEEE International Memory Workshop (IMW), Paris, France, 15–18 May 2016; pp. 1–4.
41. Chiu, C.-J.; Lue, H.-T.; Hsieh, K.-Y.; Lu, C.-Y. A novel double-density single-gate vertical-channel (SGVC) 3D NAND flash utilizing a flat-channel thin-body device. In Proceedings of the IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, 25–28 October 2016; pp. 1–4.
42. Lue, H.-T.; Chiu, C.-J.; Lu, C.-Y. A novel double-density single-gate vertical-channel (SGVC) 3D NAND flash featuring a flat-channel device with excellent layer uniformity. In Proceedings of the 2016 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), Hsinchu, Taiwan, 25–27 April 2016; pp. 1–4.
43. Kim, Y.; Yun, J.-G.; Park, S.H.; Kim, W.; Seo, J.Y.; Kang, M.; Ryoo, K.-C.; Oh, J.-H.; Lee, J.-H.; Shin, H.; et al. Three-Dimensional nand Flash Architecture Design Based on Single-Crystalline STacked ARray. *IEEE Trans. Electron. Devices* **2012**, *59*, 35–45. [CrossRef]
44. Lee, C.H.; Choi, K.I.; Cho, M.K.; Song, Y.H.; Park, K.C.; Kim, K. A Novel SONOS structure of $SiO_2/SiN/Al_2O_3$ with TaN Metal Gate for Multi-Giga Bit Flash Memories. In Proceedings of the 2003 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 8–10 December 2003; pp. 26.5.1–26.5.4.
45. Cho, W.-S.; Shim, S.I.; Jang, J.; Cho, H.-S.; You, B.-K.; Son, B.-K.; Kim, K.-H.; Shim, J.-J.; Park, C.-M.; Lim, J.-S.; et al. Highly reliable vertical NAND technology with biconcave shaped storage layer and leakage controllable offset structure. In Proceedings of the 2010 Symposium on VLSI Technology, Honolulu, HI, USA, 15–17 June 2010; pp. 173–174.
46. Park, K.-T.; Byeon, D.-S.; Kim, D.-H. A world's first product of three-dimensional vertical NAND Flash memory and beyond. In Proceedings of the 2014 14th Annual Non-Volatile Memory Technology Symposium (NVMTS), Jeju Island, Korea, 27–29 October 2014; pp. 1–5.
47. Jeong, W.; Im, J.-W.; Kim, D.-H.; Nam, S.-W.; Shim, D.-K.; Choi, M.-H.; Yoon, H.-J.; Kim, D.-H.; Kim, Y.-S.; Park, H.-W.; et al. A 128 Gb 3b/cell V-NAND Flash Memory With 1 Gb/s I/O Rate. *IEEE J. Solid State Circuits* **2016**, *51*, 204–212.
48. Kang, D.; Jeong, W.; Kim, C.; Kim, D.-H.; Cho, Y.S.; Kang, K.-T.; Ryu, J.; Kang, K.-M.; Lee, S.; Kim, W.; et al. 256 Gb 3 b/Cell V-nand Flash Memory With 48 Stacked WL Layers. *IEEE J. Solid State Circuits* **2017**, *52*, 210–217. [CrossRef]
49. Lee, S.; Kim, C.; Kim, M.; Joe, S.-M.; Jang, J.; Kim, S.; Lee, K.; Kim, J.; Park, J.; Lee, H.-J.; et al. A 1 Tb 4b/cell 64-stacked-WL 3D NAND flash memory with 12 MB/s program throughput. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 11–15 February 2018; pp. 340–341.
50. Ielmini, D.; Ambrogio, S. Emerging neuromorphic devices. *Nanotechnology* **2019**, *31*, 092001. [CrossRef] [PubMed]
51. Kim, H.; Nili, H.; Mahmoodi, M.; Strukov, D. 4K-memristor analog-grade passive crossbar circuit. *arXiv* **2019**, arXiv:1906.12045.
52. Qi, M.; Cao, S.; Yang, L.; You, Q.; Shi, L.; Wu, Z. Uniform multilevel switching of graphene oxide-based RRAM achieved by embedding with gold nanoparticles for image pattern recognition. *Appl. Phys. Lett.* **2020**, *116*, 163503. [CrossRef]
53. Chen, J.; Wu, H.; Gao, B.; Tang, J.; Hu, X.S.; Qian, H. A parallel multibit programing scheme with high precision for RRAM-based neuromorphic systems. *IEEE Trans. Electron. Devices* **2020**, *67*, 2213–2217. [CrossRef]
54. Kim, T.-H.; Nili, H.; Kim, M.-H.; Min, K.K.; Park, B.-G.; Kim, H. Reset-voltage-dependent precise tuning operation of TiO_x/Al_2O_3 memristive crossbar array. *Appl. Phys. Lett.* **2020**, *117*, 152103. [CrossRef]
55. Kim, S.; Kim, T.-H.; Kim, H.; Park, B.-G. Current suppressed self-compliance characteristics of oxygen rich TiO_y inserted Al_2O_3/TiO_x based RRAM. *Appl. Phys. Lett.* **2020**, *117*, 202106. [CrossRef]

56. Wang, Y.; Liu, X.; Chen, Y.; Xu, W.; Liang, D.; Gao, F.; Zhang, M.; Samanta, S.; Gong, X.; Lian, X. Manipulation of the electrical behaviors of Cu/MXene/SiO_2/W memristor. *Appl. Phys. Express* **2019**, *12*, 106504. [CrossRef]
57. Kim, T.-H.; Lee, J.; Kim, S.; Park, J.; Park, B.-G.; Kim, H. 3-bit multilevel operation with accurate programming scheme in TiO_x/Al_2O_3 memristor crossbar array for quantized neuromorphic system. *Nanotechnology* **2021**, *32*, 295201. [CrossRef] [PubMed]
58. Jang, J.T.; Min, J.; Hwang, Y.; Choi, S.-J.; Kim, D.M.; Kim, H.; Kim, D.H. Digital and analog switching characteristics of InGaZnO memristor depending on top electrode material for neuromorphic system. *IEEE Access* **2020**, *8*, 192304–192311. [CrossRef]
59. Mahmoodi, M.; Kim, H.; Fahimi, Z.; Nili, H.; Sedov, L.; Polishchuk, V.; Strukov, D. An Analog Neuro-Optimizer with Adaptable Annealing Based on 64 × 64 0T1R Crossbar Circuit. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 14.7.1–14.7.4.
60. Joshi, V.; Le Gallo, M.; Haefeli, S.; Boybat, I.; Nandakumar, S.R.; Piveteau, C.; Dazzi, M.; Rajendran, B.; Sebastian, A.; Eleftheriou, E. Accurate deep neural network inference using computational phase-change memory. *Nat. Commun.* **2020**, *11*, 2473. [CrossRef] [PubMed]
61. Saito, Y.; Kolobov, A.V.; Fons, P.; Mitrofanov, K.V.; Makino, K.; Tominaga, J.; Robertson, J. Origin of resistivity contrast in interfacial phase-change memory: The crucial role of Ge/Sb intermixing. *Appl. Phys. Lett.* **2019**, *114*, 132102. [CrossRef]
62. Neumann, C.M.; Okabe, K.L.; Yalon, E.; Grady, R.W.; Wong, H.-S.P.; Pop, E. Engineering thermal and electrical interface properties of phase change memory with monolayer MoS_2. *Appl. Phys. Lett.* **2019**, *114*, 082103. [CrossRef]
63. Raeis-Hosseini, N.; Rho, J. Dual-functional nanoscale devices using phase-change materials: A reconfigurable perfect absorber with nonvolatile resistance-change memory characteristics. *Appl. Sci.* **2019**, *9*, 564. [CrossRef]
64. Yin, Q.; Chen, L. Crystallization behavior and electrical characteristics of Ga–Sb thin films for phase change memory. *Nanotechnology* **2020**, *31*, 215709. [CrossRef] [PubMed]
65. Anam, M.K.; Ahn, E.C. Understanding the effect of dry etching on nanoscale phase-change memory. *Nanotechnology* **2019**, *30*, 495202. [CrossRef] [PubMed]
66. Oh, S.; Huang, Z.; Shi, Y.; Kuzum, D. The impact of resistance drift of phase change memory (PCM) synaptic devices on artificial neural network performance. *IEEE Electron. Device Lett.* **2019**, *40*, 1325–1328. [CrossRef]
67. Shin, M.; Min, K.; Shim, H.; Kwon, Y. Investigation on phase-change synapse devices for more gradual switching. *J. Semicond. Technol. Sci.* **2019**, *19*, 8–17. [CrossRef]
68. Kim, H.; Hwang, S.; Park, J.; Yun, S.; Lee, J.-H.; Park, B.-G. Spiking neural network using synaptic transistors and neuron circuits for pattern recognition with noisy images. *IEEE Electron. Device Lett.* **2018**, *39*, 630–633. [CrossRef]
69. Shim, W.; Yu, S. Technological design of 3D NAND-based compute-in-memory architecture for GB-scale deep neural network. *IEEE Electron. Device Lett.* **2021**, *42*, 160–163. [CrossRef]
70. Oh, S.; Kim, C.-H.; Lee, S.; Kim, J.S.; Lee, J.-H. Unsupervised online learning of temporal information in spiking neural network using thin-film transistor-type NOR flash memory devices. *Nanotechnology* **2019**, *30*, 435206. [CrossRef] [PubMed]
71. Kim, H.; Hwang, S.; Park, J.; Park, B.-G. Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic system. *Nanotechnology* **2017**, *28*, 405202. [CrossRef] [PubMed]
72. Hwang, S.; Kim, H.; Park, J.; Kwon, M.-W.; Baek, M.-H.; Lee, J.-J.; Park, B.-G. System-level simulation of hardware spiking neural network based on synaptic transistors and I&F neuron circuits. *IEEE Electron. Device Lett.* **2018**, *39*, 1441–1444.
73. Malavena, G.; Filippi, M.; Spinelli, A.S.; Compagnoni, C.M. Unsupervised learning by spike-timing-dependent plasticity in a mainstream NOR flash memory array—Part I: Cell operation. *IEEE Trans. Electron. Devices* **2019**, *66*, 4727–4732. [CrossRef]
74. Kim, H.; Park, J.; Kwon, M.-W.; Lee, J.-H.; Park, B.-G. Silicon-based floating-body synaptic transistor with frequency dependent short-and long-term memories. *IEEE Electron. Device Lett.* **2016**, *37*, 249–252. [CrossRef]
75. Choi, H.-S.; Kim, H.; Lee, J.-H.; Park, B.-G.; Kim, Y. AND flash array based on charge trap flash for implementation of convolutional neural networks. *IEEE Electron. Device Lett.* **2020**, *41*, 1653–1656. [CrossRef]
76. Kim, S.; Baek, M.-H.; Hwang, S.; Jang, T.; Park, K.; Park, B.-G. A novel vector-matrix multiplication (VMM) architecture based on NAND memory array. *J. Semicond. Technol. Sci.* **2020**, *20*, 242–248. [CrossRef]
77. Lee, S.-T.; Kwon, D.; Kim, H.; Yoo, H.; Lee, J.-H. NAND flash based novel synaptic architecture for highly robust and high-density quantized neural networks with binary neuron activation of (1, 0). *IEEE Access* **2020**, *8*, 114330–114339. [CrossRef]