

aUNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC.,
Petitioner,

v.

ADVANCED MEMORY TECHNOLOGIES, LLC,
Patent Owner.

Case IPR2025-01453
Patent 8,400,835

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107**

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EXHIBIT LIST

Exhibit	Description
2001	Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 1, filed Dec. 30, 2024 (E.D. Tex.)
2002	Amended Complaint for Patent Infringement, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 25, filed April 2, 2025 (E.D. Tex.)
2003	Second Amended Docket Control Order, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 27, filed April 11, 2025 (E.D. Tex.)
2004	RESERVED
2005	Order Denying Motion for Stay Pending <i>Inter Partes</i> Review, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, Dkt. No. 79, filed Sept. 3, 2025 (E.D. Tex.)
2006	United States District Courts — National Judicial Caseload Profile (including data through June 30, 2025), https://www.uscourts.gov/sites/default/files/document/fcms_na_distprofile0630.2025.pdf (accessed October 10, 2025).
2007	Defendant SH Hynix’s Preliminary Invalidity Contentions Cover Pleading, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)
2008	Omnibus Obviousness Chart E-OB for U.S. Patent No. 8,400,835, <i>Advanced Memory Techs., LLC v. SK Hynix Inc.</i> , No. 2-24-cv-01078, served June 25, 2025 (E.D. Tex.)
2009	RESERVED
2010	RESERVED
2011	Docket Navigator Time To Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025
2012	Lex Machina Time to Trial Statistics for Judge Rodney Gilstrap for October 20, 2024 through October 20, 2025

I. INTRODUCTION

Patent Owner Advanced Memory Technologies, LLC (“AMT”) respectfully requests that the Director deny SK Hynix Inc.’s (“Petitioner” or “Hynix”) Petition to institute *inter partes* review of U.S. Patent No. 8,400,835 (the “’835 Patent”) because Petitioner has not shown a reasonable likelihood of prevailing on its challenge to any of claims 1, 2, 4, or 5 (the “Challenged Claims”). *See* Petition at 1–2.

Hynix fails even to address a requirement, present in every claim, that *the second terminals* of the recited switches be “connected ***at a common point*** to the drain voltage supply line.” Instead, Hynix relies on an implied claim construction that reads out the requirement of a common point entirely, assuming that “connected at a common point” has the same meaning as “connected.” That implied construction cannot be supported by law or fact. Neither of the references cited for the “connected at a common point” limitation—Murakami and Kobayashi—disclose anything more than a “connection,” and Hynix makes no attempt to show otherwise. Petitioner relies on these two references for this limitation in every Ground, and the Petition therefore fails in its entirety.

II. BACKGROUND

A. The '835 Patent

The '835 Patent, which is titled “Non-Volatile Semiconductor Memory,” issued on March 19, 2013 to Yukimasa Hamamoto and Masahiro Toki of Panasonic Corporation. EX1001 at (45), (54), (75), (73). The patent issued from an application filed on July 25, 2011. *Id.* at (22).

1. Claims

The Petition challenges independent claim 1 and dependent claims 2, 4, and 5 of the '835 Patent. Petition at 1. The Petition grounds fail to present a reasonable likelihood of invalidating independent claim 1, and therefore the grounds fail for dependent claims 2, 4, and 5 as well. Independent claim 1 is reproduced below, using the same limitation labels as used in the Petition for consistency (*see* Petition at v):

1[pre]	A non-volatile semiconductor memory in which a plurality of non-volatile memory cells can be simultaneously written using a plurality of bit lines, the device comprising:
1[a]	M data lines connected to the plurality of bit lines based on a column address signal, where M is an integer of two or more and is smaller than the number of the bit lines;
1[b]	a drain voltage generation circuit configured to generate a voltage which is a source of a drain voltage of each of the plurality of non-volatile memory cells;

1[c]	a drain voltage supply line connected to an output of the drain voltage generation circuit; and
1[d]	M switch circuits and M switch control circuits provided between the M data lines and the drain voltage supply line,
1[e]	wherein each of the M switch circuits includes N switches, where N is an integer of one or more,
1[f]	each of the M×N switches includes a first and a second terminal, and the first terminals of the N switches of each of the M switch circuits are connected at a common point to a corresponding one of the M data lines, and the second terminals of the N switches of each of the M switch circuits are connected at a common point to the drain voltage supply line, and
1[g]	the drain voltage supply line is connected to the M data lines via the M×N switches, and the M×N switches are controlled by the M switch control circuits.

EX1001 at 6:32–58.

2. Specification

The '835 patent “relates to non-volatile semiconductor memories, and more particularly, techniques of reducing variations in write speed when a plurality of non-volatile memory cells are simultaneously written to the same threshold level.”

EX1001 at 1:16–20. Non-volatile semiconductor memory is a type of memory that can generally retain stored information even after power is removed. *See, e.g.*, EX1002 ¶ 44. In contrast, volatile semiconductor memory (such as RAM) generally

needs constant power in order to store information. *See, e.g., id.* The '835 Patent gives examples of non-volatile information storage designs, such as those using “a floating gate or a charge trapping layer.” EX1001 at 1:26.

The '835 Patent describes several shortcomings that can occur in conventional non-volatile semiconductor memory designs. The Patent gives the conventional example of “non-volatile semiconductor memory, such as a flash memory [that] typically includes a memory cell array including a plurality of memory cells arranged in a matrix, where each memory cell includes a gate electrode connected to a word line, a drain connected to a bit line, a source connected to a source line, and a floating gate or a charge trapping layer.” *Id.*, at 1:22–26.

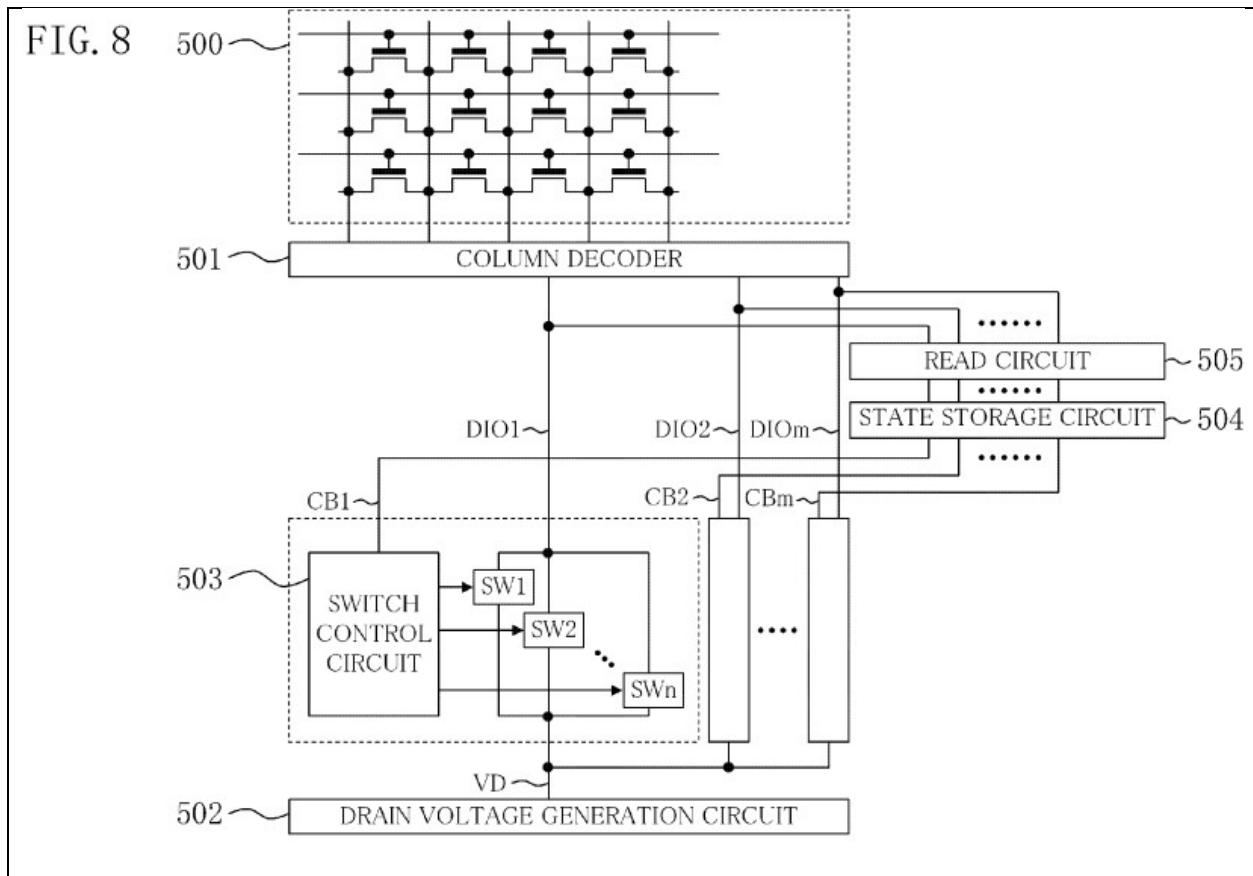
The '835 Patent notes that “[i]n recent years, [] as the capacity of non-volatile semiconductor memories has increased, the area of the memory cell array has also increased, and therefore, the length of bit lines provided in the memory cell array has also increased.” *Id.*, at 2:12–16. Those longer bit lines caused additional resistance and voltage drop, “resulting in variations in write speed” because “the drain voltage varies depending on the position of the memory cell in the memory array” and different voltages applied to the drain can result in different write speeds. *Id.*, at 2:16–19.

Further compounding problems with variations in write speed, the '835 Patent explains that “in the non-volatile semiconductor memory which includes the

trapping layer and can store two bits of data in each memory cell, it is known that the memory state of a first bit has an influence on the write speed of a second bit, leading to variations in write speed.” *Id.*, at 2:20–24.

The ’835 Patent observes that the “conventional technique of reducing variations in write speed” was to “chang[e] the level of a bit line voltage supplied to a bit line in a memory cell array, depending on a write address, during write operation.” *Id.*, at 2:25–29. But that technique could not be used when writing to a plurality of memory cells simultaneously because the voltages required by different memory cells to optimize write speed would have been independent from one another and thus may differ. Thus, conventional techniques attempting to write to multiple memory cells simultaneously still resulted in more variability in write speed and/or increased degradation of the individual memory cells if unnecessarily high voltages were used on certain memory cells while trying to reduce variability in write speed. *Id.*, at 2:33–40.

The ’835 Patent teaches specific arrangements wherein “the write speeds of memory cells . . . can be changed on a memory cell-by-memory cell basis, whereby variations in write speed which occur when a plurality of memory cells are simultaneously written can be reduced or prevented.” *Id.*, at 3:53–58. The ’835 Patent teaches an example embodiment as shown in Figure 8.



EX1001, Fig. 8

This embodiment includes “a memory cell array 500 including a plurality of memory cells, a column decoder 501 which connects a plurality of bit lines and M data lines DIO1-DIOm together using a column address signal.” *Id.*, at 5:15–20. “[A] read circuit 505 [] reads data from the memory cell array 500, and a drain voltage generation circuit 502 [] supplies a drain voltage to the bit lines.” *Id.*, at 5:22–24. As the ’835 Patent further explains, “[t]he second terminals of the N switches SW1–SWn for each data line are connected at a common point to a drain voltage supply line VD[,] which is an output of the drain voltage generation circuit 502.” *Id.*, at 5:32–35.

3. Prosecution History

The '835 Patent is a continuation of PCT Application No. PCT/JP2009/004737 and claims priority to a Feb. 6, 2009 foreign application priority date. EX1001 at 1:7–12. When the application for the '835 Patent was filed, the Applicant simultaneously filed an information disclosure statement (“IDS”) and the international search report (“ISR”) for the PCT application. *See* EX1006 at 54–61. Both the IDS and ISR identified the Murakami and Kobayashi references upon which Petitioner relies for all of its Petition grounds. *See id.* (identifying “JP 06-150670” and “JP 05-062484”); Petition at 2.

The Examiner considered both Murakami and Kobayashi (among others), EX1006 at 24, and subsequently issued a Notice of Allowance on January 10, 2013, *id.* at 14–20. The Examiner noted that the closest art failed to “show or suggest” the claimed combination of limitations in claim 1, specifically identifying limitations 1[d] through 1[g]. *Id.* at 19. As discussed below, the Examiner was correct, and the references considered during prosecution (including Murakami and Kobayashi) fail to teach or render obvious the limitations of any Challenged Claims. AMT addresses

the deficiencies of Murakami and Kobayashi in more detail below, especially regarding limitation 1[f].¹

As Petitioner admits, the Applicant submitted the Japanese language versions of Murakami and Kobayashi, together with the English translations of their abstracts. Petition at 13. Petitioner's suggestion that the Applicant was required to do more, *i.e.*, to submit "full English language translations of Murakami and Kobayashi," *id.*, is baseless. There is no requirement for a patent applicant to submit such translations, and their absence would not have prevented the Examiner from considering the references.

For example, MPEP § 609 instructs that "[t]ranslations are not required to be filed unless they have been reduced to writing and are actually translations of what is contained in the non-English language information." Furthermore, "[i]f no translation is submitted, the examiner will consider the information in view of the concise explanation and insofar as it is understood on its face, e.g., *drawings*." *Id.*

¹ For purposes of this Preliminary Response, Patent Owner has limited its analysis to certain limitations for which the Petition clearly fails to show any reasonable likelihood of success. If the proceeding is instituted then Patent Owner reserves the right to address additional limitations, including the other limitations the examiner identified that the prior art failed to "show or suggest." *See* EX1006 at 19.

(emphasis added). The Petition relies heavily on the Figures from both references, including circuit diagrams that convey structure even without the need for translation. *See generally id.* at 17–43, 58–74. The Examiner therefore considered at least a substantial portion of Murakami’s and Kobayashi’s respective disclosures on which the Petition relies. *See* EX1006 at 24 (initialing to indicate consideration of “JP 06-150670” and “JP 05-062484”). As discussed in more detail below, the deficiencies in the asserted references (including, e.g., the absence of a common connection point to a drain voltage supply line) is evident from the figures themselves and thus would have been apparent to an examiner considering the figures.

Even if the shortcomings of Murakami and Kobayashi had not already been clear from the figures alone, the examiner also had access to translation services if they had been needed to further confirm the deficiencies in Murakami and Kobayashi. *See, e.g.,* MPEP § 901.05(d) (noting “Examiners may request human (written) translations at any point in the examination process” and “Examiners may also contact in-house translators for on-the-spot oral translations”). This further confirms that the examiner was correct that Murakami and Kobayashi fail to teach or render obvious any Challenged Claims.

B. Petitioner’s Grounds

The Petition asserts the following grounds against the Challenged Claims:

Ground	Basis	References	Claims
1	§102 (anticipation)	Murakami (JP Pat. Appl. Pub. No. JPH06150670A)	1, 2, 4
2	§103 (obviousness)	Murakami in view of Yu (U.S. Pat. Pub. No. 2007/0263449A1)	5
3	§102 (anticipation)	Kobayashi (JP Pat. Appl. Pub. No. JPH0562484A)	1, 4, 5
4	§103 (obviousness)	Kobayashi in view of the knowledge of a POSITA	2

Petition at 2.

As shown above, Petitioner’s Grounds challenging independent claim 1 are based only on theories that the asserted reference—Murakami (Ground 1) or Kobayashi (Ground 3)—anticipates claim 1. All the other challenged claims depend from claim 1 and incorporate its limitations. Grounds 2 and 4 are based on obviousness, but each relies on the theories asserted in Ground 1 or 3, respectively, for the limitations of the independent claim. Because Murakami and Kobayashi both fail to teach every limitation of claim 1, the Petition necessarily fails to present a reasonable likelihood of invalidating any of the challenged claims.

1. Murakami (EX1008)

Petitioner identifies Murakami (EX1008) as JP Patent Publication No. JPH06150670A. Petition at iii. Exhibit 1009 purports to be an English translation of Murakami and states that Murakami is a Japanese Unexamined Patent Application

Publication published on May 31, 1994. EX1009 at 1. Murakami (as translated) purports “[t]o provide a semiconductor memory device with improved writing characteristics” by “perform[ing] a data line selection operation [that] is adjustable to compensate for the voltage drop caused by the resistance component contained in the data lines.” *Id.* at (57), (Abstract).

2. Kobayashi (EX1010)

Petitioner identifies Kobayashi (EX1010) as JP Pat. Pub. No. JPH0562484A. Petition at iii. Exhibit 1011 purports to be an English translation of Kobayashi and states that Kobayashi is a Japanese Unexamined Patent Application Publication published on March 12, 1993. Kobayashi (as translated) purports to teach how to “achieve the suppression of peaks of write current and current during write operations.” *Id.* at (57), (Abstract). It suggests that “peaks of the write current flowing to the source line can be suppressed by differentiating between the write voltage supply timing of the write voltage supply means of a predetermined number of write voltage supply means and the write voltage supply timing of the remaining write voltage supply means.” *Id.* ¶ [0038].

III. LEVEL OF ORDINARY SKILL IN THE ART

Petitioner suggests that “[a] person of ordinary skill in the art at the time of the ’835 patent (‘POSITA’) had at least a Bachelor of Science in electrical engineering, computer engineering, or similar fields and at least two years of

experience in the field of computer memory technology.” Petition at 14. It is unnecessary for Patent Owner to put forward a different definition at this stage because the Petition fails to present a reasonable likelihood of success under this (or any other reasonable) definition of a POSITA.

IV. CLAIM CONSTRUCTION

“[A] petition **must** state how a challenged claim is to be construed and how each element of the construed claim is found in prior art patents or printed publications.” *Samsung Electronics Co., Ltd. v. Blaze Mobile, Inc.*, IPR2021-01569, Paper 16, at 5 (citing 37 C.F.R. § 42.104(b)(3)–(4)) (emphasis added). Petitioner failed to do so, asserting that “[n]o express constructions are required to find the ’835 patent claims invalid.” Petition at 14. Despite this, Petitioner applied an implicit construction for the term “connected **at a common point**” that reads out the “**at a common point**” limitation altogether. *See id.* at 41 n.3, 72. As discussed in more detail below, the Petition grounds fail to address the limitations as claimed, and the Petition should therefore be denied.

V. LEGAL STANDARDS

“In an IPR, the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (noting 35 U.S.C. § 312(a)(3) requires that petitions must identify “with particularity . . . the evidence that supports

the grounds for the challenge to each claim”). To meet this burden, “the petition must specify where *each element of the claim* is found in the prior art patents or printed publications relied upon.” 37 C.F.R. § 42.104(b)(4) (emphasis added). And “the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016). The burden of persuasion on the petitioner never shifts to the patent owner. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Applying the foregoing substantive standards and burdens, “[t]he Director may not authorize an *inter partes* review to be instituted unless the Director determines . . . that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

When an expert declaration is “conclusory and unsupported,” it is “entitled to little weight.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (August 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”); *Upjohn Co. v. Mova Pharm. Corp.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000) (“Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity determination.”) (quoting *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776

F.2d 281, 294 (Fed. Cir. 1985)); *Carella v. Starlight Archery & Pro Line Co.*, 804 F.2d 135, 138 (Fed. Cir. 1986) (“Although in some circumstances unsupported oral testimony can be sufficient to provide prior knowledge or use, it must be regarded with suspicion and subjected to close scrutiny.”).

“A party must [] meet a high standard in order to rely on inherency.” *Par Pharm., Inc. v. TWi Pharm., Inc.*, 773 F.3d 1186, 1195 (Fed. Cir. 2014). “Inherency [] may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981); *see also In re Rijckaert*, 9 F.3d 1531, 1533-34 (Fed. Cir. 1993) (“The mere fact that a certain thing may result from a given set of circumstances is not sufficient [to establish inherency].” (internal quotation omitted)).

VI. PETITIONER FAILS TO SHOW A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CLAIM

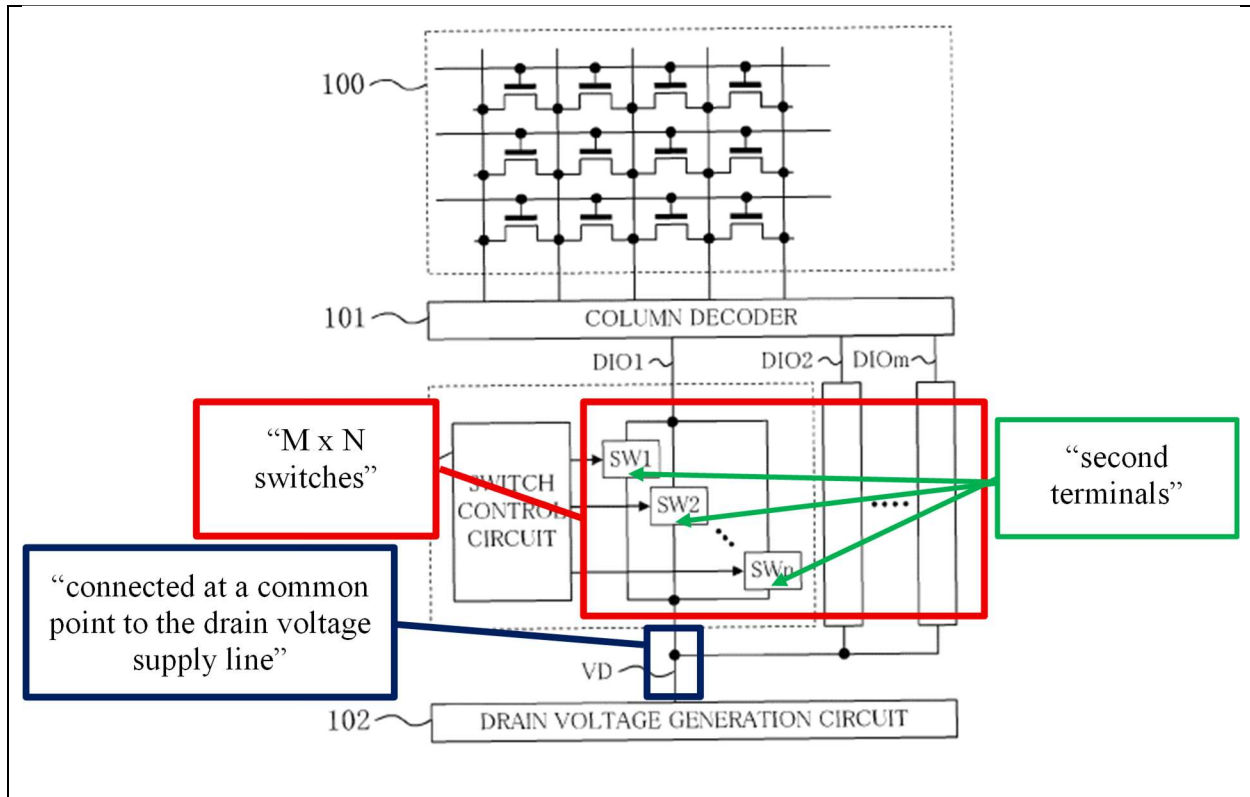
The Petition fails to show a reasonable likelihood of prevailing on any claim because none of the cited references teaches the claim 1 limitation reciting “the second terminals of the N switches of each of the M Switch circuits are connected *at a common point* to the drain voltage supply line.” EX1001 at 6:52–55 (emphasis added). The Petition Grounds fail even to address the requirement that the claimed terminals are connected “at a common point.” Instead, Hynix relies on an implied claim construction that reads out the requirement of a common point entirely.

A. Claim 1 Recites the Switch Terminals Being *Connected at a Common Point to the Drain Voltage Supply*

Claim 1 (the sole independent claim of the '835 Patent) recites in part “M”² number of “switch circuits . . . wherein each of the M switch circuits includes N switches, where N is an integer of one or more.” EX1001 at 6:43–48. The claim further recites that “each of the M x N switches includes a first and a second terminal,” and “the second terminals of the N switches of each of the M switch circuits are connected at a common point to the drain voltage supply line.” *Id.*, at 6:49–55.

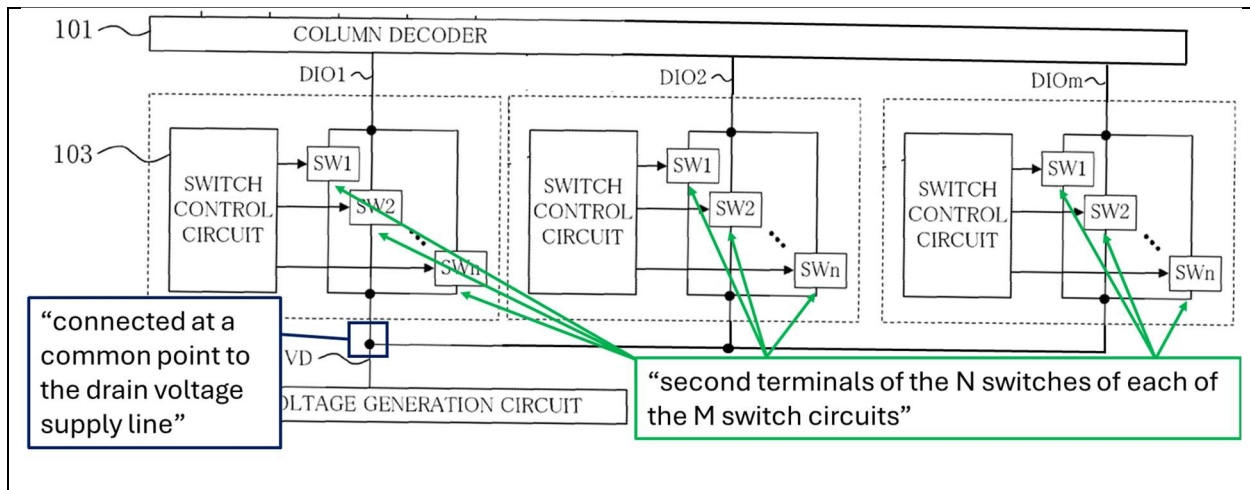
A “common point” of connection to a “drain voltage supply line,” as recited, is illustrated by Figure 1 of the '835 Patent, reproduced below (with annotations). As shown below, the second terminals of the N switches (SW1, SW2, . . . SWn) for each of the M switch circuits (DIO1, DIO2, . . . DIOm) are “connected *at a common point* to a drain voltage supply line VD.” *Id.*, at 3:44–47 (emphasis added).

² Claim 1 recites that “M is an integer of two or more and is smaller than the number of the [plurality of bit lines recited in the preamble].” EX1001 at 6:32–37.



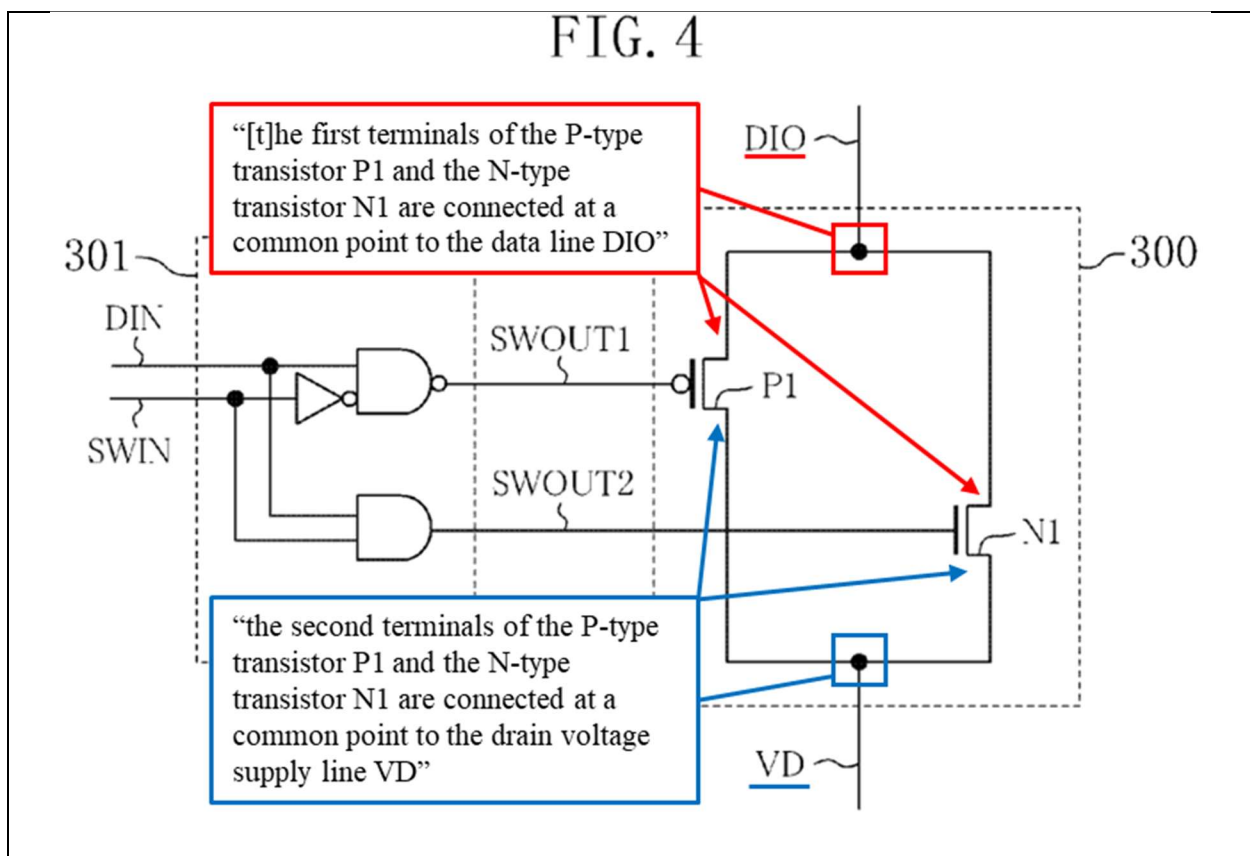
EX1001, Fig. 1 (annotated).

A version of Figure 1, modified to show the additional switch control circuits and switch circuits, is shown below.



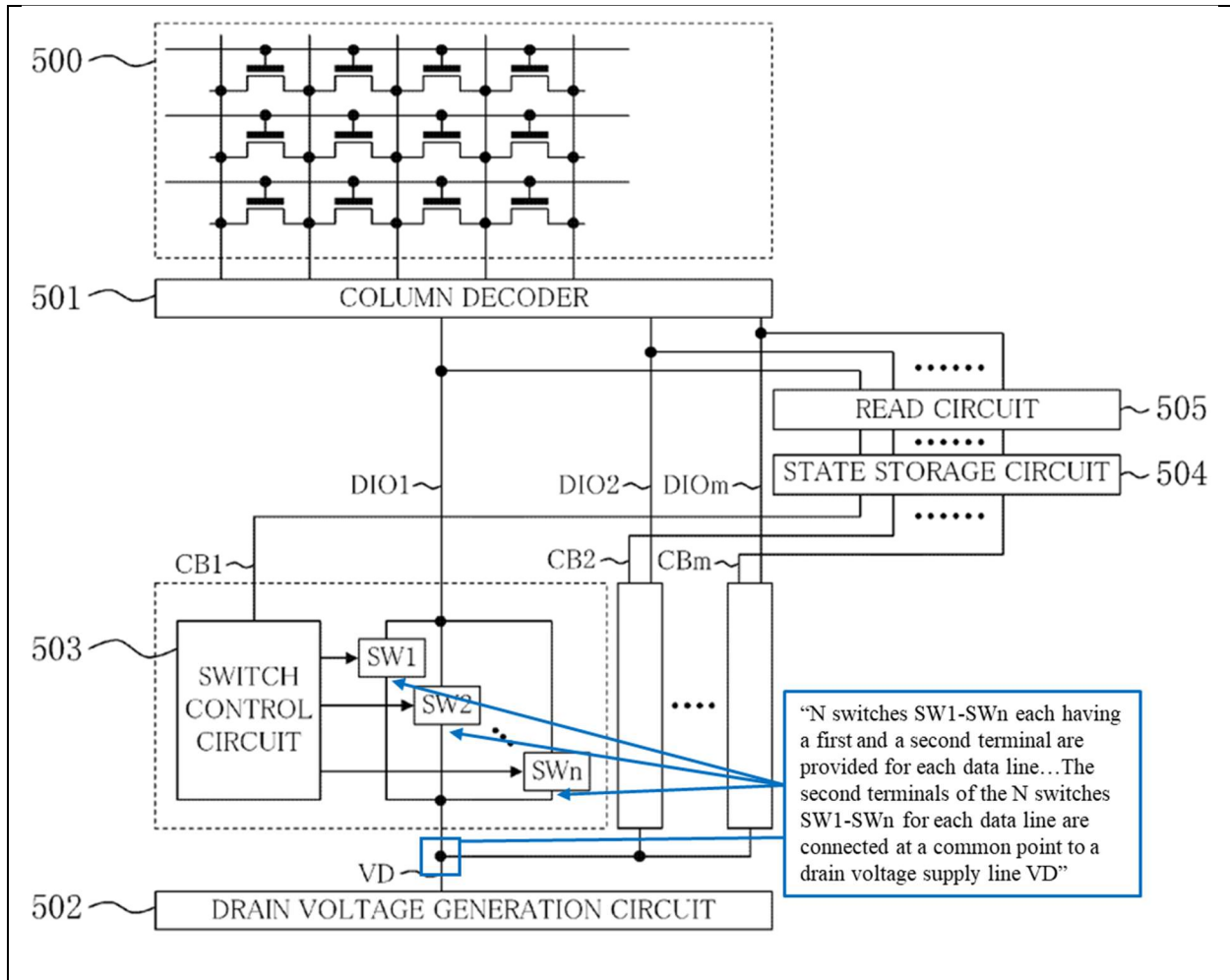
See EX1001, Fig. 1 (modified and annotated).

The '835 Patent uses similar “connected at a common point” language consistently throughout the disclosure. For example, when discussing Figure 4 it notes “[t]he first terminals of the P-type transistor P1 and the N-type transistor N1 are connected *at a common point* to the data line DIO, and the second terminals of the P-type transistor P1 and the N-type transistor N1 are connected *at a common point* to the drain voltage supply line VD.” *Id.* at 4:28–33 (emphasis added).



EX1001, Fig. 4 (annotated).

The '835 Patent uses similar language yet again when describing Figure 8:



EX1001, Fig. 8 (annotated, quotes from EX1001 at 5:30–35).

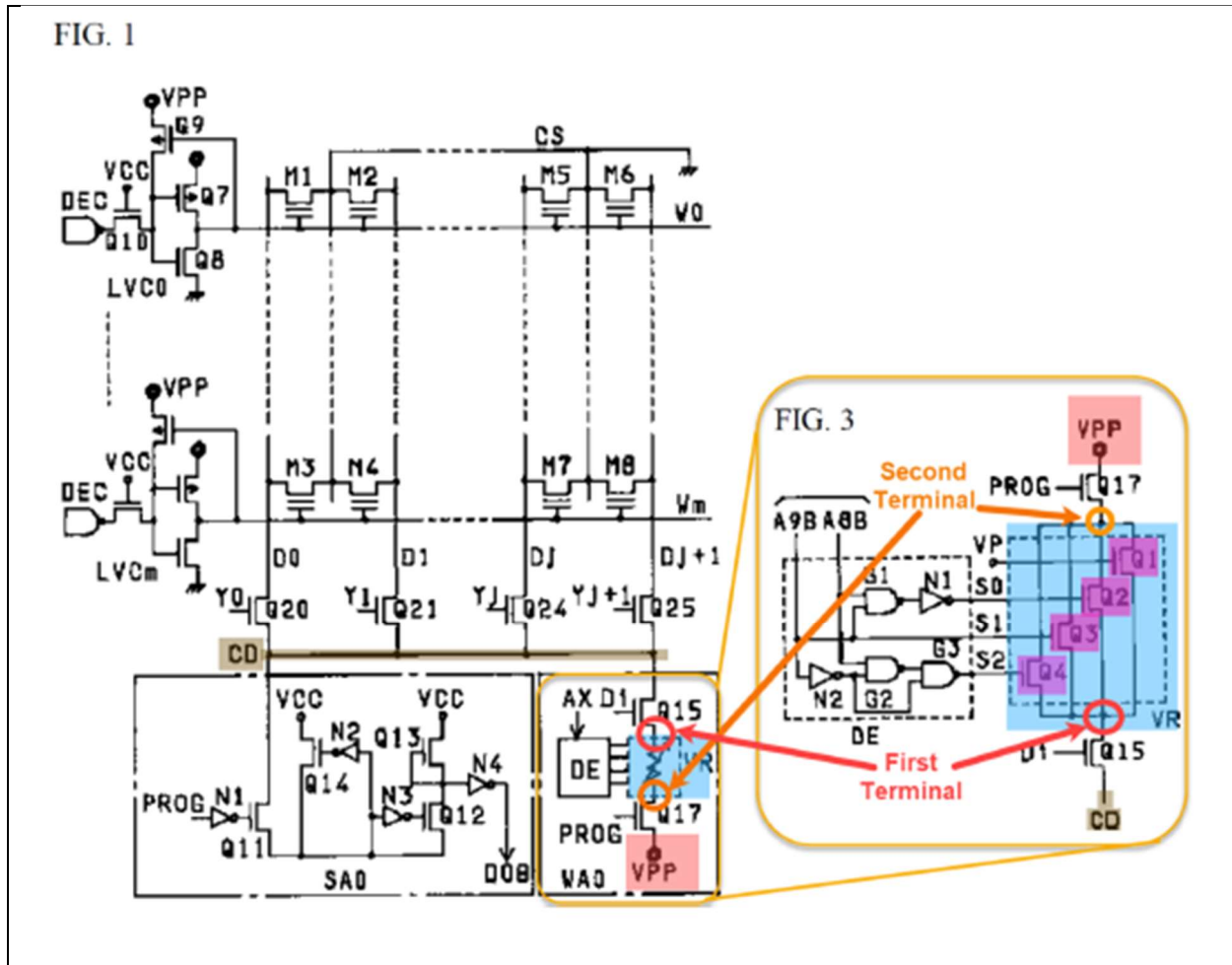
B. Petitioner Fails to Show That Either of Its Primary References Disclose the *Connected at a Common Point* Limitation

Neither Murakami nor Kobayashi discloses the second terminals being connected to the drain voltage supply line *at a common point*, as discussed below. Indeed, the Petition fails even to address the requirement that the connection be “at a common point.” Instead, Petitioner attempts to read that requirement out of the claim, asserting that the phrase “connected at a common point” should be construed to have the same meaning as the word “connected,” by itself. *See* Petition at 40 n.3

(quoting from the “Merriam-Webster definition of ‘connected,’” EX1013). The phrase “connected at a common point” cannot reasonably be given the same scope as the unqualified term “connected” because it would render the words “at a common point” meaningless. *See Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”). Petitioner also attempts to bury this unsupported construction in a footnote, *see* Petition at 40 n.3, and neither Petitioner nor its expert provides any explanation or justification for ignoring a distinct requirement of claim 1. *See id.*; EX1002 ¶ 101 n.12.

1. Murakami Does Not Teach the Switch Terminals Being Connected at a Common Point to the Drain Voltage Supply and Thus Cannot Anticipate Claim 1

In Murakami, Petitioner identifies the line connected to “VPP” as the drain voltage supply line. Petition at 38–41, 43. The Petition only identifies one alleged “second terminal” of one switch, as shown in Petitioner’s (heavily annotated and modified) figure below, being connected to the VPP. *See id.*, at 40–41. Murakami does not disclose that any other second terminals (*i.e.*, for the N switches of other switch circuits, M) are also connected to “VPP” at a “common point,” and the Petition does not demonstrate otherwise.



Petition at 40 (annotating and modifying EX1009 Figs. 1 & 3)

Petitioner asserts (1) that “the MxN switches include first and second terminals, serving as respective ‘common point[s]’ for other components connected together on the circuit schematic,” and (2) that “a second terminal (orange circle O) [is] at a common point shared between the collective ‘N switches’ (pink) of each of the M write load circuits and the ‘drain voltage supply line.’” *Id.*, at 40–41 (emphasis added, color in original). Both theories fail to anticipate the claimed “second terminals of the N switches of each of the M Switch circuits [] connected at a common point to the drain voltage supply line,” as addressed below.

Petitioner’s first assertion—that each terminal is somehow a common point for all other components—is completely unsupported and would render the “at a common point” limitation meaningless because every circuit component would always be connected at a common point to every other circuit component.

Petitioner’s second assertion—that the purported orange “second terminal” can be the claimed common point—is equally deficient. As an initial matter, claim 1 recites that each of the switches includes a first and a second terminal, not that multiple switches share a single terminal. Even looking past that deficiency, the Challenged Claims recite that “each of the MxN switches includes a first and a second terminal” and that “the second terminals of the N switches of each of the M switch circuits are connected at a common point to the drain voltage supply line.” EX1001 at 6:49–55 (emphasis added). Petitioner made no attempt to demonstrate that each of the MxN switches are connected at a common point to the drain voltage supply line. At best, Petitioner has shown that each of the N switches in a single switch circuit M are connected to a common point. That showing is wholly insufficient, especially for a theory based on anticipation. *See Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (“[T]o demonstrate anticipation, the proponent must show that the four corners of a single, prior art document describe every element of the claimed invention.” (internal quotes and citations omitted)); *see also id.* (noting that the prior-art document “must not only

disclose all elements of the claim within the four corners of the document, but must also disclose those elements arranged as in the claim.” (internal quotes and citations omitted)).

Petitioner cites Murakami (¶ [0025]) and the Khatri Declaration (EX1002 ¶ 102) for support, Petition at 41–42, however neither one provides any support for its theory. The cited portion of Murakami does not address connecting multiple switch circuits to a drain voltage supply line at a common point, and in paragraph 102 of his declaration, Dr. Khatri merely parrots the same conclusory analysis from the Petition that this limitation is met simply because all circuit components are “joined or linked together” in some capacity. *See* EX1002 ¶ 102 n.12. This confirms that Petitioner’s anticipation theory depends entirely on ignoring the “at a common point” limitation. The Grounds citing Murakami therefore fail.

**2. Kobayashi Does Not Teach the Switch Terminals Being
Connected at a Common Point to the Drain Voltage Supply and
Thus Cannot Anticipate Claim 1**

In Kobayashi, Petitioner identifies a component labeled “ V_{PP} ” as the drain voltage supply line to which the second terminals must be connected. Petition at 69, 71–72. As shown in the annotated figure below, the two alleged second terminals are connected to V_{PP} at two different points, not “at a common point.”



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Petitioner's diagram that Kobayashi teaches two separate connections to V_{PP} , rather than a connection to V_{PP} "at a common point," as claimed.

3. All Asserted Grounds Fail as to All Claims

As discussed above, Petitioner's challenges to claim 1 in Grounds 1 (Murakami) and 3 (Kobayashi) fail. Petitioner's Ground 2 and 4 challenge only dependent claims and expressly rely on Petitioner's contentions regarding claim 1. Petition at 52, 74. These Grounds therefore fail for the same reasons as Petitioner's challenges to claim 1. The Petition thus fails to present a reasonable likelihood of prevailing as to any challenged claims.

VII. CONCLUSION

For at least the reasons stated herein, AMT respectfully requests that the Director deny institution of *inter partes* review in this proceeding.

Dated: December 1, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 TO PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,400,835 was served to the following counsel of record for SK Hynix as follows:

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), the undersigned hereby certifies that this brief complies with the type-volume limitation of 37 C.F.R. § 42.24 because this brief contains 4,497 words.

Dated: December 1, 2025

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