Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 4418I-2
	Application Number	
Title of Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM	

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Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Peter	B.	GILLINGHAM	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Ottawa	Country of Residence i	CA

Mailing Address of Inventor:

Address 1	43 Slade Crescent		
Address 2			
City	Ottawa	State/Province	OT
Postal Code	K2K 2K9	Country i	CA

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Graham		ALLAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Stittsville	Country of Residence i	CA

Mailing Address of Inventor:

Address 1	10 Carbery Drive		
Address 2			
City	Stittsville	State/Province	OT
Postal Code	K2S 1E4	Country i	CA

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Application Information:

Title of the Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM		
Attorney Docket Number	PAT 4418I-2	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	2

Filing By Reference:

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15655336	2017-07-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15655336	Continuation of	15378650	2016-12-14	9740407	2017-08-22

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15378650	Continuation of	15183162	2016-06-15	9552889	2017-01-24

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15183162	Continuation of	14720317	2015-05-22	9384847	2016-07-05

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Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14720317	Continuation of	14491440	2014-09-19	9042199	2015-05-26

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14491440	Continuation of	14158215	2014-01-17	8854915	2014-10-07

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14158215	Continuation of	13871487	2013-04-26	8644108	2014-02-04

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13871487	Continuation of	13006005	2011-01-13	8432767	2013-04-30

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13006005	Division of	12032249	2008-02-15	7885140	2011-02-08

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12032249	Claims benefit of provisional	60902003	2007-02-16

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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	Application Number	
Title of Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	PAT 4418I-2
	Application Number	
Title of Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	
If the Applicant is an Organization check here.	☒
Organization Name	Conversant Intellectual Property Management Inc.

Mailing Address Information For Applicant:

Address 1	515 Legget Drive		
Address 2	Suite 704		
City	Ottawa	**State/Province**	OT
Country[i]	CA	Postal Code	K2K 3G4
Phone Number		Fax Number	
Email Address			

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Address 1			
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City		**State/Province**	
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Signature:

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Shin Hung/			Date (YYYY-MM-DD)	
First Name	Shin	Last Name	Hung	Registration Number	55497

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CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation application of U.S. Patent Application No. 15/655,336, filed on July 20, 2017, which is a Continuation application of U.S. Patent Application No. 15/378,650, filed on December 14, 2016, now issued as U.S. Patent No. 9,740,407 on August 22, 2017, which is a Continuation application of U.S. Patent Application No. 15/183,162, filed on June 15, 2016, now issued as U.S. Patent No. 9,552,889 on January 24, 2017, which is a Continuation application of U.S. Patent Application 14/720,317, filed on May 22, 2015, now issued as U.S. Patent No. 9, 384,847 on July 5, 2016, which is a continuation application of U.S. Patent Application Serial No. 14/491,440, filed on September 19, 2014, now issued as U.S. Patent No. 9,042,199 on May 26, 2015, which is a Continuation application of U.S. Patent Application Serial No. 14/158,215, filed on January 17, 2014, now issued as U.S. Patent No. 8,854,915 on October 7, 2014, which is a Continuation application of U.S. Patent Application Serial No. 13/871,487 filed on April 26, 2013, now issued as U.S. Patent No. 8,644,108 on February 4, 2014, which is a Continuation application of U.S. Patent Application Serial No. 13/006,005 filed on January 13, 2011, now issued as U.S. Patent No. 8,432,767 on April 30, 2013, which is a Divisional application of U.S. patent application Serial No. 12/032,249 filed on February 15, 2008, now issued as U.S. Patent No. 7,885,140 on February 8, 2011, which claims the benefit of U.S. Provisional Patent Application Serial No. 60/902,003 filed on February 16, 2007, which are hereby incorporated by reference.

BACKGROUND

[0002] Flash memory is a commonly used type of non-volatile memory in widespread use as mass storage for consumer electronics, such as digital cameras and portable digital music players for example. The density of a presently available Flash memory component, consisting of 2 stacked dies, can be up to 32Gbits (4GB), which is suitable for use in popular USB Flash drives, since the size of one Flash component is small.

[0003] The advent of 8 mega pixel digital cameras and portable digital entertainment devices with music and video capabilities has spurred demand for ultra-high capacities to store the large amounts of data, which cannot be met by the single Flash memory device. Therefore, multiple Flash memory devices are combined together into a memory system to effectively increase the available storage capacity. For example, Flash storage densities of 20GB may be required for such applications.

[0004] Figure 1 is a block diagram of a prior art flash memory system **10** integrated with a host system **12**. Flash memory system **10** includes a memory controller **14** in communication with host system **12**, and multiple non-volatile memory devices **16**. The host system **12** includes a processing device such as a microcontroller, microprocessor, or a computer system. The Flash memory system **10** of Figure 1 is configured to include one channel **18**, where memory devices **16** are connected in parallel to channel **18**. Those skilled in the art will understand that the memory system **10** can have more or less than four memory devices connected to it.

[0005] Channel **18** includes a set of common buses, which include data and control lines that are connected to all its corresponding memory devices. Each memory device is enabled/disabled with respective chip select signals CE#1, CE#2, CE#3 and CE#4, provided by memory controller **14**. The "#" indicates that the signal is an active low logic level signal. The memory controller **14** is responsible for issuing commands and data, via the channel **18**, to a selected memory device based on the operation of the host system **12**. Data read from the memory devices is transferred via the channel **18** back to the memory controller **14** and host system **12**. Operation of flash memory system **10** can be asynchronous or synchronous. Figure 1 illustrates an example of a synchronous system that uses a clock CLK, which is provided in parallel to each memory device **16**. Flash memory system **10** is generally referred to as a multi-drop configuration, in which the memory devices **16** are connected in parallel with respect to channel **18**.

[0006] In Flash memory system **10**, non-volatile memory devices **16** may be (but not necessarily) substantially identical to each other, and are typically implemented as NAND flash memory devices. Those skilled in the art will understand that flash memory is organized into banks, and each bank is organized into blocks to facilitate block erasure. Most commercially available NAND flash memory devices are configured to have two banks of memory.

[0007] There are specific issues that will adversely impact performance of the system. The configuration of Flash memory system **10** imposes physical performance limitations. With the large number of parallel signals extending across the system, the signal integrity of the signals they carry will be degraded by crosstalk, signal skew, and simultaneous switching noise (SSN). Power consumption in such a configuration becomes an issue as each signal track between the flash controller and flash memory devices is frequently charged and discharged for signaling. With increasing system clock frequencies, the power consumption will increase.

[0008] There is also a practical limit to the number of memory devices which can be connected in parallel to the channel since the drive capability of a single memory device is small relative to the loading of the long signal tracks. Furthermore, as the number of memory devices increase, more chip enable signals (CE#) are required, and the clock signal CLK will need to be routed to the additional memory devices. Clock performance issues due to extensive clock distribution are well known in the art, which would need to be addressed. Therefore, in order to accommodate a memory system having a large number of memory devices, either a controller having more channels must be used, or and/or the system will need to be clocked at a lower frequency. A controller configured to have multiple channels and additional chip enable signals increases the cost of the memory system. Otherwise, the memory system is limited to a small number of memory devices.

[0009] Therefore, it is desirable to provide a memory system device architecture capable of high speed operation while overcoming issues associated with the prior art memory system having memory devices connected in parallel to each other.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Embodiments of the clock mode circuits will now be described, by way of example only, with reference to the attached Figures, wherein:

[0011] Fig. 1 is a block diagram of a prior art Flash memory system;

[0012] Fig. 2A is a general block diagram of a serial memory system receiving a clock signal in parallel;

[0013] Fig. 2B is a general block diagram of a serial memory system receiving a clock signal serially;

[0014] Fig. 3A is a block diagram of a serial memory system receiving clock signals serially, according to one embodiment;

[0015] Fig. 3B is a timing diagram showing the operation of the memory system of Figure 3A;

[0016] Fig. 3C is a block diagram of a serial memory system receiving clock signals in parallel, according to another embodiment;

[0017] Fig. 3D is a timing diagram showing the operation of the memory system of Figure 3C;

[0018] Fig. 4 is a block diagram of a memory device having a native core and a serial input/output interface suitable for use in the serial memory systems of Figures 3A and B;

[0019] Fig. 5 is a block diagram illustrating a configurable input circuit embodiment usable in the serial memory systems of Figures 3A and 3C;

[0020] Fig. 6 is a circuit schematic embodiment of the mode setter of Figure 5;

[0021] Fig. 7 is a sequence diagram illustrating the operation of the mode setter of Figure 6;

[0022] Fig. 8A is a schematic embodiment of the configurable input circuit shown in Figure 5;

[0023] Fig. 8B is a timing diagram showing the operation of the circuits of Figure 8A;

[0024] Fig. 9 is a block diagram of an embodiment of a dynamically configurable serial memory system;

[0025] Fig. 10 is a schematic embodiment of an alternate clock switch circuit embodiment used in the memory devices shown in Figure 9; and,

[0026] Fig. 11 is a flow chart of a method for configuring an clock operating mode of a memory device.

DETAILED DESCRIPTION

[0027] In a first aspect, there is provided a semiconductor device for receiving a clock and input data. The semiconductor device includes a configurable input circuit operable in a first mode for receiving coincident edges of the clock and the input data, and for providing

shifted clock edges positioned within a data valid window for sampling the input data. The configurable input circuit is operable in a second mode for receiving non-coincident edges of the clock and the input data for sampling the input data. In an embodiment of the present aspect, the semiconductor device further includes an input pin for providing a voltage to the configurable input circuit for setting the first mode and the second mode. The input pin includes a reference voltage pin set to one of low and high power supply levels for setting the second mode, and a reference voltage level for setting the first mode. The reference voltage level can be between the low and high power supply levels, and is used by the configurable input circuit to sense logic levels of the input data.

[0028] In further embodiments of the present aspect, the configurable input circuit includes a single ended input buffer and a differential input buffer. The single ended input buffer is coupled to a data input pin for receiving the input data, and is enabled in the second mode and disabled in the first mode. The differential input buffer is coupled to the data input pin for receiving the input data, and is enabled in the first mode for sensing logic levels of the input data relative to the voltage. Alternately, the configurable input circuit includes a clock synthesizer for providing the shifted clock edges in response to the clock. The clock synthesizer includes one of a delay locked loop and a phase locked loop, or the clock synthesizer can be disabled in the second mode.

[0029] In a second aspect, the present invention provides a configurable memory device. The configurable memory device includes a mode setter, a clock switch, and a configurable data input/output buffer. The mode setter senses a voltage level of a reference voltage input port and provides a mode selection signal corresponding to the sensed voltage level. The clock switch is coupled to a clock input port for receiving at least one of parallel complementary clock signals and serial complementary clock signals. The clock switch generates complementary internal clock signals corresponding to the parallel complementary clock signals in response to a first logic state of the mode selection signal, or the serial complementary clock signals in response to a second logic state of the mode selection signal. The configurable data input/output buffer is coupled to a data input port and the reference voltage input port for sensing data received on the data input port relative to the voltage level in response to the second logic state of the mode selection signal. In an embodiment of the present aspect, the mode setter includes a sense circuit and a latch. The sense circuit compares the voltage level to a preset reference voltage, and provides a sense

output corresponding to the voltage level relative to the preset reference voltage. The latch latches the sense output and provides the mode selection signal having one of the first logic state and the second logic state.

[0030] In the current embodiment, the sense circuit includes a reference voltage circuit and a comparator. The reference voltage circuit provides the preset reference voltage and the comparator provides the sense output in response to the voltage level and the preset reference voltage. The reference voltage circuit includes a voltage divider coupled between VDD and VSS, and a power shut-off device for cutting off current through the voltage divider after a predetermined period of time. The mode setter includes a delay circuit for turning off the power shut-off device after the predetermined period of time when a reset signal is driven to an inactive logic state. The delay circuit includes an n-bit counter enabled when the reset signal is at the inactive logic state for driving a most significant bit to an active logic state. The most significant bit is driven to the active logic state when 2^n active edges of a clock signal are counted, where n is an integer value greater than 1, such that the delay circuit generates a disable signal corresponding to the most significant bit being at the active logic state for turning off the power shut-off device.

[0031] In yet another embodiment of the present aspect, the clock switch includes a clock input buffer, a clock generator and a clock output buffer. The clock input buffer provides the buffered parallel complementary clock signals in response to the first logic state of the mode selection signal, and provides a sensed clock signal corresponding to the serial complementary clock signals in response to the second logic state of the mode selection signal. The clock generator generates the complementary internal clock signals in response to either the buffered parallel complementary clock signals when the mode selection signal is at the first logic state, or the sensed clock signal when the mode selection signal is at the second logic state. The clock output buffer drives the complementary internal clock signals through clock output ports when the mode selection signal is at the second logic state. The clock input buffer includes a comparator and a pair of buffers. The comparator is enabled in response to the mode selection signal at the second logic state for providing the sensed clock signal in response to the serial complementary clock signals. The pair of buffers are enabled in response to the mode selection signal at the second logic state for providing the buffered parallel complementary clock signals in response to the parallel complementary clock signals. The clock output buffer includes a pair of drivers enabled in response to the

mode selection signal at the second logic state for driving the complementary internal clock signals through the clock output ports.

[0032] In a further embodiment, the clock generator includes a clock synthesizer and a switch circuit. The clock synthesizer provides a first clock signal and a second clock signal shifted 180 degrees relative to the first clock signal, in response to the sensed clock signal. The switch circuit passes the first clock signal and the second clock signal as the complementary internal clock signals when the mode selection circuit is at the second logic state. The switch circuit passes the buffered parallel complementary clock signals as the complementary internal clock signals when the mode selection circuit is at the second logic state. The clock synthesizer can be one of a phase locked loop and a delay locked loop. The clock synthesizer provides a third clock signal and a fourth clock signal, where the third clock signal is shifted 90 degrees relative to the first clock signal and the fourth clock signal is shifted 180 degrees relative to the third clock signal. The clock generator further includes a phase selector circuit for selectively passing either the complementary internal clock signals or the third and fourth clock signals to the clock output buffer.

[0033] According to another embodiment, the configurable data input/output buffer includes a data input buffer for selectively providing input data corresponding to either sensed data resulting from a comparison between the data and the voltage level, or buffered data corresponding to the data, in response to the mode selection signal. The data input buffer includes a comparator and a buffer. The comparator is enabled when the mode selection signal is at the second logic state for providing the input data in response to the voltage level and a voltage of the data. The buffer is enabled when the mode selection signal is at the first logic state for providing the buffered data. The configurable data input/output buffer can further include a data switch for selectively passing one of the input data and local read data to a data output buffer.

[0034] In a third aspect, the present invention provides a method for configuring a clock operating mode of a memory device that receives a reference voltage for sensing input data. The method includes setting the reference voltage level; comparing the reference voltage to a preset reference voltage for generating a mode selection signal corresponding to the reference voltage relative to the preset reference voltage; and configuring a clock input buffer to receive either parallel complementary clock signals or serial complementary clock signals in response to the mode selection signal. In embodiments of the present aspect, the

step of comparing includes latching the mode selection signal, and the step of comparing includes disabling a sense circuit used for comparing the reference voltage to the preset reference voltage after a predetermined delay. The predetermined delay is determined by counting 2^n clock edges after deasserting a reset signal, and the preset reference voltage floats to a voltage supply while the reset signal is asserted.

[0035] In yet another embodiment of the present aspect, the step of configuring includes enabling a comparator receiving serial complementary clock signals and disabling buffers receiving parallel complementary clock signals in response to a first logic state of the mode selection signal. The step of enabling includes enabling a clock synthesizer for generating a first clock signal and a second clock signal shifted 180 degrees relative to the first clock signal, in response to a sensed clock signal from the comparator. The step of enabling a clock synthesizer includes providing as internal clock signals one of the first clock signal and the second clock signal and buffered parallel complementary clock signals corresponding to the parallel complementary clock signals, in response to the mode selection signal. The clock synthesizer generates a third clock signal and a fourth clock signal, where the third clock signal is shifted 90 degrees relative to the first clock signal and the fourth clock signal is shifted 180 degrees relative to the third clock signal. The step of configuring includes selectively passing one of the internal clock signals and the third and fourth clock signals in response to a phase selection signal.

[0036] In a fourth aspect, the present invention provides a memory system configurable to operate with one of parallel clock signals and serial clock signals. The memory system includes a memory controller and at least one serially connected memory device. The at least one memory device has clock input ports, a reference voltage input port, a mode setter, and a clock switch circuit. The clock input ports receive one of the parallel clock signals and the serial clock signals. The reference voltage input port receives a reference voltage set to one of a predetermined voltage level and a voltage supply level. The mode setter compares the reference voltage to the predetermined voltage level, and generates a mode selection signal corresponding to a result of the comparison. The clock switch circuit is coupled to the clock input ports for generating complementary internal clock signals corresponding to one of the parallel clock signals and the serial complementary clock signals, in response to the mode selection signal.

[0037] A memory system that resolves many performance issues of the Flash memory system **10** of Figure 1 is a serially connected memory system in which the memory devices are serially connected with each other and the memory controller in a ring topology configuration. Figures 2A and 2B are block diagrams illustrating the conceptual nature of a serial memory system. Figure 2A is a block diagram of a serial memory system receiving a parallel clock signal while Figure 2B is a block diagram of the same serial memory system of Figure 2A receiving a source synchronous clock signal.

[0038] In Figure 2A, the serial memory system **20** includes a memory controller **22** having at least one serial channel output port Sout and a serial channel input port Sin, and memory devices **24**, **26**, **28** and **30** that are connected in series. Input and output ports correspond to physical pins or connections interfacing the memory device to the system it is integrated with. In one embodiment, the memory devices can be flash memory devices. Alternately, the memory devices can be DRAM, SRAM or any other type of memory device provided it has a serial input/output interface compatible with a specific command structure, for executing commands or for passing through commands and data to the next memory device. The current example of Figure 2A includes four memory devices, but alternate embodiments can include a single memory device, or any number of memory devices. Accordingly, if memory device **24** is the first device of serial memory system **100** as it is connected to Sout, then memory device **30** is the Nth or last device as it is connected to Sin, where N is an integer number greater than zero. Memory devices **26** to **28** are then intervening serially connected memory devices between the first and last memory devices. Each memory device can assume a distinct identification (ID) number, or device address (DA) upon power up initialization of the system, so that they are individually addressable. Commonly owned U.S. Patent Application Serial No. 11/622,828 titled “APPARATUS AND METHOD FOR PRODUCING IDS FOR INTERCONNECTED DEVICES OF MIXED TYPE”, U.S. Patent Application Serial No. 11/750,649 titled “APPARATUS AND METHOD FOR ESTABLISHING DEVICE IDENTIFIERS FOR SERIALLY INTERCONNECTED DEVICES”, U.S. Patent Application Serial No. 11/692,452 titled “APPARATUS AND METHOD FOR PRODUCING DEVICE IDENTIFIERS FOR SERIALLY INTERCONNECTED DEVICES OF MIXED TYPE”, U.S. Patent Application Serial No. 11/692,446 titled “APPARATUS AND METHOD FOR PRODUCING IDENTIFIERS REGARDLESS OF MIXED DEVICE TYPE IN A SERIAL INTERCONNECTION”, U.S. Patent Application Serial No. 11/692,326 titled

"APPARATUS AND METHOD FOR IDENTIFYING DEVICE TYPE OF SERIALLY INTERCONNECTED DEVICES" and U.S. Patent Application Serial No. 11/771,023 titled "ADDRESS ASSIGNMENT AND TYPE RECOGNITION OF SERIALLY INTERCONNECTED MEMORY DEVICES OF MIXED TYPE" describe methods for generating device addresses for serially connected memory devices of a memory system, the contents of which are incorporated by reference in its entirety.

[0039] Memory devices **24** to **30** are considered serially connected because the data input of one memory device is connected to the data output of a previous memory device, thereby forming a series-connection configuration, with the exception of the first and last memory devices in the chain. The channel of memory controller **22** includes data, address, command, and control information provided by separate pins or the same pins. For example, a data channel of any suitable data width will carry command, data and address information, while a control channel will carry control signal data. The embodiment of Figure 2A includes one channel, where the one channel includes Sout and corresponding Sin ports. However, memory controller **22** can include any number of channels for accommodating separate memory device chains. In the example of Figure 2A, the memory controller **22** provides a clock signal CLK, which is connected in parallel to all the memory devices.

[0040] In general operation, the memory controller **22** issues a command through its Sout port, which includes an operational code (op code), a device address, address information for reading or programming, and data for programming. The command is issued as a serial bitstream packet, where the packet can be logically subdivided into predetermined size segments, such as a byte for example. A bitstream is a sequence or series of bits provided over time. The command is received by the first memory device **24**, which compares the device address to its assigned address. If the addresses match, then memory device **24** executes the command. Otherwise, the command is passed through its own output port to the next memory device **26**, where the same procedure is repeated. Eventually, the memory device having the matching device address, referred to as a selected memory device, will execute the operation dictated by the command. If the command is to read data, the selected memory device will output the read data through its output port, which is serially passed through intervening memory devices until it reaches the Sin port of the memory controller **22**. Since the commands and data are provided in a serial bitstream, the clock is used by each memory device for clocking in/out the serial bits and for synchronizing internal

memory device operations. This clock is used by all the memory devices in the serial memory system **20**.

[0041] The performance of serial memory system **20** is superior to that of the parallel memory system **10** shown in Figure 10. The parallel distributed clock lines can provide a relatively relaxed clock frequency, thereby allowing memory system **20** to use low voltage CMOS unterminated full swing signaling to provide robust data communication. This is also referred to as LVTTL signaling. For example, assuming a 66 MHz clock is used and the serial memory system **20** includes four memory devices, the data rate per pin of one of the serially connected memory devices employing double data rate (DDR) signaling will be about 133 Mbps.

[0042] Serial memory system **40** of Figure 2B is similar to serial memory system **20** of Figure 2A, except that the clock signal CLK is provided serially to each memory device from an alternate memory controller **42** configured for providing the source synchronous clock signal CLK. Each memory device **44**, **46**, **48** and **50** will be configured to receive and pass the source synchronous clock CLK. In a practical implementation of serial memory system **40**, the clock signal CLK is passed from one memory device to another via short signal lines. Therefore none of the clock performance issues related to the parallel clock distribution scheme are present, and CLK can operate at high frequencies. Accordingly, the serial memory system **40** can operate with greater speed than serial memory system **20** of Figure 2A. For example, high speed transceiver logic (HSTL) signaling can be used to provide high performance data communication. In the HSTL signaling format, each memory device will receive a reference voltage that is used for determining a logic state of the incoming data signals. Another similar signaling format is the SSTL signaling format. Accordingly, the data and clock input circuits in the memory devices of serial memory systems **20** and **40** will be configured differently from each other.

[0043] While high speed serial memory systems are suitable for newer computing devices, there may be existing computing systems that do not require high speed operation, but can still benefit from the high memory capacity of a serial memory system. For example, the serial memory system can be modular, as disclosed in commonly owned U.S. Patent Application No. 11/843,440, where additional memory devices can be added to the memory system in order to expand the total memory capacity. On the other hand, it may not be cost effective to replace existing slower speed serial memory systems with the high speed

memory systems. Therefore, both types of memory devices would have to be available for upgrading or assembling of both types of serial memory systems. However, persons skilled in the art will understand that it is not cost effective to manufacture two different types of memory devices, where one type is configured for interfacing with memory controller **22** while another type is configured for interfacing with memory controller **42**.

[0044] Therefore, a clock mode configuration circuit for a configurable memory device is provided for allowing the configurable memory device to be used in both a parallel clocked memory system and a serially clocked memory system. Such a memory system includes any number of configurable memory devices serially connected to each other, where each configurable memory device receives a clock signal. The clock signal can be provided either in parallel to all the configurable memory devices or serially from one memory device to another through the same clock input. The clock mode configuration circuit in each configurable memory device is set to a parallel mode for receiving the parallel clock signal, and to a serial mode for receiving a source synchronous clock signal from a prior memory device or memory controller. Depending on the set operating mode, the data input circuits will be configured for a corresponding data signal format, and the corresponding clock input circuits will be either enabled or disabled. The parallel mode and the serial mode is set by sensing a reference voltage level provided to each memory device.

[0045] Figures 3A and 3C are block diagrams of serial memory systems using the same type of memory device that includes embodiments of the clock mode configuration circuit, the details of which will be described later. The memory devices of the serial memory system of Figure 3A receive the clock serially while the memory devices of the serial memory system of Figure 3C receive the clock in parallel. In the memory system embodiments of Figures 3A and 3C, four memory devices are shown connected in series in a ring topology configuration with the memory controller, however any number of memory devices can be included in either serial memory system. The serial memory systems of Figures 3A and 3C illustrate that the same type of memory device can be used for both a parallel clocked system and a serially source synchronous clocked system, provided the memory devices have the clock mode configuration circuit.

[0046] In Figure 3A, serial memory system **100** includes a memory controller **102** and four memory devices **104**, **106**, **108** and **110**. The memory controller **102** provides control signals in parallel to the memory devices. These include the chip enable signal CE# and the

reset signal RST#. In one example use of CE#, the device is enabled when CE# is at the low logic level. Once the memory device starts a program or erase operation, CE# can be de-asserted, or driven to a high logic level. In one example use of RST#, the memory device is set to a reset mode when RST# is at the low logic level. In the reset mode, the power is allowed to stabilize and the device prepares itself for operation by initializing all finite state machines and resetting any configuration and status registers to their default states. The memory controller **102** includes clock output ports CKO# and CKO for providing complementary clock signals CK and CK#, and clock input ports CKI# and CKI for receiving the complementary clock signals from the last memory device of the system. Each memory device will include a clock synthesizer, such as a DLL or a PLL for generating phases of the received clocks. Certain phases will be used to center the clock edges within the input data valid window internally to ensure reliable operation. Each memory device has clock output ports CKO# and CKO for passing the complementary clock signals to the clock input ports of the next memory device, and clock input ports CKI and CKI# for receiving the complementary clock signals from either the memory controller **102** or a previous memory device. The last memory device **110** provides the clock signals back to the memory controller **102**.

[0047] The channel of memory controller **102** includes a data channel consisting of data output port Qn and data input port Dn, and a control channel consisting of a command strobe input CSI, a command strobe output CSO (echo of CSI), data strobe input DSI, and a data strobe output DSO (echo of DSI). Output port Qn and input port Dn can be one bit in width, or n bits in width where n is a non-zero integer, depending on the desired configuration. For example, if n is 1 then one byte of data is received after eight data latching edges of the clock. A data latching clock edge can be a rising clock edge for example in single data rate (SDR) operation, or both rising and falling edges of the clock for example in double data rate (DDR) operation. If n is 2 then one byte of data is received after four latching edges of the clock. If n is 4 then one byte of data is received after two latching edges of the clock. The memory device can be statically configured or dynamically configured for any width of Qn and Dn. Hence, in a configuration where n is greater than 1, the memory controller provides data in parallel bitstreams. CSI is used for latching command and write data appearing on the input port Dn, and has a pulse duration corresponding to the length of the command data received. More specifically, the command and write data will have a

duration measured by a number of clock cycles, and the pulse duration of the CSI signal will have a corresponding duration. DSI is used for enabling the output port Qn buffer to output read data, and has a pulse duration corresponding to the length of the read data being requested.

[0048] Since the present embodiment of Figure 3A is intended for high speed operation, a high speed signaling format, such as the HSTL signaling format by example, will be used. Accordingly, a reference voltage VREF is provided to each memory device which is used by each memory device to determine the logic level of the signals received at the Dn, CSI and DSI input ports. The reference voltage VREF may be generated by another circuit on the printed circuit board, for example, and is set to a predetermined voltage level based on the voltage swing of the HSTL signal. By example, VREF can be set to a mid-point voltage of the maximum voltage level of the HSTL signal. According to the present embodiment, setting VREF to the aforementioned predetermined voltage level will set the clock mode configuration circuit in a first operating mode in which the input circuits are set to receive HSTL input signals and the appropriate internal clock circuits will be generated. The first operating mode can be referred to as a high speed operating mode.

[0049] In a practical implementation of the embodiment of Figure 3A, each memory device is positioned on a printed circuit board such that the distance and signal track between input and output ports is minimized. Alternately, the four memory devices can be implemented in a system in package module (SIP) which further minimizes signal track lengths. The memory devices can also be implemented as multiple SIP modules. Memory controller **102** and memory devices **104** to **110** are serially connected to form a ring topology, meaning that the last memory device **110** provides its outputs back to the memory controller **102**. As such, those skilled in the art will understand that the distance between memory device **110** and memory controller **102** is easily minimized.

[0050] Figure 3B is a timing diagram showing the general timing relationship between the input signals and output signals for each memory device in serial memory system **100** with some internal signals shown as well. In this diagram internal gate delays are assumed to be minimal, although in an actual system significant delays can be accommodated and will not affect functionality. Signal traces for received input clocks CKI and CKI#, input data Dn, output clocks CKO and CKO#, and output data Qn are shown in Figure 3B, as are internally generated 90, 180, 270 and 360 degree phases of the received input clocks. Since each

memory device operates at the double data rate, received data is buffered into an internal single data rate even data stream D_E and an internal single data rate odd data stream D_O. In the example of Figure 3B, data “A”, “B”, “C”, “D” and “E” are provided serially on the Dn input of the memory device, where each has a data input valid window corresponding to a rising and falling edge of CKI or CKI#. In other words, the input data and the clock edges are coincident with each other. Data “A”, “C” and “E” are latched on each rising edge of the internal 90 degree clock and provided on the D_E data stream. Data “B” and “D” are latched on each rising edge of the internal 270 degree clock and provided on the D_O data stream. Assuming that the received input data on Dn is simply passed through to its Qn output, the double data rate output data Qn is generated from the even D_E data latched on each rising edge of the 270 degree clock output and the odd D_O data latched on each rising edge of the 90 degree clock output. As shown in Figure 3B, CKO corresponds to the 270 degree clock output while CKO# corresponds to the 90 degree clock output.

[0051] In the presently shown embodiment of Figure 3C, each memory device has the same serial input/output interface, which includes RST#, CE#, CKI# and CKI input ports for receiving the corresponding signals from the memory controller **202**. The serial input/output interface further includes a data input port Dn, a data output port Qn, CSI, DSI, CSO and DSO ports. As shown in Figure 3C, the Dn, CSI and DSI input ports for each memory device are connected to the Qn, CSO and DSO output ports respectively, of a previous memory device. Accordingly, the memory devices are considered serially connected to each other as each can pass command and read data to the next memory device in the chain.

[0052] In Figure 3C, serial memory system **200** includes a memory controller **202** and the same memory devices **104**, **106**, **108** and **110** of Figure 3A. The memory controller **202** will be configured to provide the same functionality as memory controller **102** of Figure 3A except that the clock signals are provided in parallel, therefore the clock output ports CKO# and CKO of each memory device are unconnected. Furthermore, the signaling format for the data and the strobe signals will be different, such as the full swing un-terminated LVTTL signaling format by example. At lower clock frequencies, the LVTTL signaling format does not require the use of reference voltage VREF, thus VREF can be set to a voltage level other than the predetermined level used in the embodiment of Figure 3A. For example, VREF can be set to either VDD or VSS. According to the present embodiment, setting VREF to VSS or

some voltage other than the aforementioned predetermined voltage level will set the clock mode configuration circuit in a second operating mode in which the input circuits are set to receive LVTTL input signals and the appropriate internal clock circuits will be generated. The second operating mode can be referred to as a low speed operating mode. Accordingly, an advantage of using the existing VREF input of the memory devices to set the operating mode of the clock mode configuration circuit is that no additional pin and corresponding logic in the memory controllers is required for configuring the memory devices. Each memory device self-configures based on the voltage level of VREF, thereby reducing any design overhead in the memory controller. Furthermore, the same clock input ports CKI and CKI# can receive either the parallel clock signals or the serial clock signals, which minimizes the pin count of the memory device.

[0053] Figure 3D is a timing diagram showing the general timing relationship between the input signals and output signals for each memory device in serial memory system **200** with some internal signals shown as well. In this diagram internal gate delays are assumed to be minimal, although in an actual system significant delays can be accommodated and will not affect functionality. Signal traces for received input clocks CKI and CKI#, input data Dn and output data Qn are shown in Figure 3B. The memory devices do not have an internal clock synthesizer, and no output clocks CKO and CKO# are provided. Each memory device operates at the double data rate, hence received data is buffered into a single data rate even data stream D_E and a single data rate odd data stream D_O. In the example of Figure 3D, data “A”, “B”, “C”, “D” and “E” are provided serially on the Dn input of the memory device, and the rising and falling edges of CKI and CKI# are centered within each data input valid window. In the present example, internal read data “Ci” and “Di” will be provided to the output circuits of the memory device via RD_E and RD_O, in response to a read command received by the memory device. Accordingly, there is an even output data stream Q_E and an odd output data stream Q_O that will provide either the internal read data from RD_E and RD_O or external data from the D_E and D_O on the Qn output. More specifically, data from RD_E and RD_O will be provided on Q_E and Q_O in response to enable signals EN_E and EN_O at the high logic level.

[0054] Data “A”, “C” and “E” are latched on each rising edge of CKI and provided on the D_E data stream. Data “B” and “D” are latched on each rising edge of CKI# and provided on the D_O data stream. While EN_E and EN_O are at the inactive low logic level, data “A”

and “B” will be latched on the rising edges of CKI and CKI# and provided on D_E and D_O respectively. On the rising edge of CKI#, data “A” on D_E is latched and provided on Q_E, while data “B” on D_O is latched on the rising edge of CK and provided on Q_O. Data “A” and “B” are then provided on the Qn output on the rising edges of CKI# and CKI respectively. When EN_E is high, data “Ci” on RD_E is latched and provided on Q_E on the rising edge of CKI#. Subsequently, while EN_O is high, data “Di” on RD_O is latched and provided on Q_O on the rising edge of CKI. Data “Ci” and “Di” are then provided on the Qn output on the rising edges of CKI# and CKI respectively. When EN_E and EN_O fall to the low logic level, external data “E” will be latched onto Q_E and passed onto Qn. Delay through the output path of the device, the interconnection to the following device, and the input path of the following device will shift the Qn data stream so that the rising edge of CKI in the following device falls within the received Dn data stream bits A, Ci, and E, and the rising edge of CKI# in the following device falls within the received Dn data stream bits B and Di. Persons skilled in the art will ensure that the delay path from serial output Qn to serial input Dn is less than half a clock period.

[0055] According to an example embodiment, memory devices **104**, **106**, **108** and **110** can be any type of memory device having a serial input/output interface designed for serial interconnection with other memory devices. While memory devices **104**, **106**, **108** and **110** can be implemented as Flash memory devices, they can also be implemented as DRAM, SRAM or any other suitable type of volatile or non-volatile memory device. More specifically, other memory types can be adapted to operate with the serial input/output interface and configured to receive LVTTL input signals or HSTL input signals.

[0056] Figure 4 is a block diagram illustrating the conceptual organization of a generic memory device having a native core and a serial input/output interface suitable for use in the serial memory systems of Figures 3A and 3C. Memory device **300** includes a native memory core, which includes memory array banks **302** and **304**, and native control and I/O circuits **306** for accessing the memory array banks **302** and **304**. Those skilled in the art will understand that the memory array can be organized as a single memory bank or more than two memory banks. The native memory core can be DRAM, SRAM, NAND flash, or NOR flash memory based for example. Of course, any suitable emerging memory and its corresponding control circuits can be used. Accordingly, depending on the type of native memory core, circuit block **306** can include error correction logic, high voltage generators,

refresh logic and any other circuit blocks that are required for executing the operations native to the memory type.

[0057] Typically, memory devices use command decoders for initializing the relevant circuits in response to a received command by asserting internal control signals. They will also include well known I/O circuitry for receiving and latching data, commands and addresses. According to the present embodiment, the existing I/O circuits are replaced with the serial interface and control logic block **308**. In the present example, the serial interface and control logic block **308** receives RST#, CE#, CK#, CK, CSI, DSI and Dn inputs, and provides Qn, CSO, DSO, CKO and CKO# outputs.

[0058] The serial interface and control logic block **308** is responsible for various functions, as discussed in U.S. Patent Application No. 11/324,023. Example functions of serial interface and control logic block **308** include setting a device identifier number, passing data through to the next serially connected memory device, and decoding a received command for executing native operations. This circuit will be configured to receive commands serially, and will be configured to include additional commands specific to serial operation of the memory device, in addition to existing native commands specific for controlling core circuits. The command set can be expanded to execute features usable by the memory controller when the memory devices are serially connected. For example, status register information can be requested to assess the status of the memory device.

[0059] Therefore, the serial memory systems of Figures 3A and 3C can include a mix of memory device types, each providing different advantages for the greater system. Such a configuration having memory devices of mixed types is disclosed in U.S. Provisional Patent Application No. 60/868,773 filed December 6, 2006, the disclosure of which is incorporated herein by reference in its entirety. Further details are such configurations are disclosed in U.S. Patent Application Serial No. 11/771,023 titled ""ADDRESS ASSIGNMENT AND TYPE RECOGNITION OF SERIALLY INTERCONNECTED MEMORY DEVICES OF MIXED TYPE", and in U.S. Patent Application Serial No. 11/771,241 titled "SYSTEM AND METHOD OF OPERATING MEMORY DEVICES OF MIXED TYPE". For example, the high speed of DRAM memory can be used for caching operations while the non-volatility of flash memory can be used for low power mass data storage. Regardless of the type of memory device being used, each memory device is individually addressable to act upon a command because the serial interface and control logic block **306** is configured to receive commands

according to a predetermined protocol. According to one embodiment, the previously discussed clock mode configuration circuit is implemented in the serial interface and control logic block **308**.

[0060] Figure 5 is a block diagram illustrating a clock mode configuration circuit according to one embodiment, which generates signals to be used by an embodiment of a configurable input/output buffer. Both the clock mode configuration circuit and the configurable input buffer can be used in the previously described serial interface and control logic block **308**. The clock mode configuration circuit includes a mode setter **400** and a clock switch circuit **402**. The mode setter **400** generates a mode signal MODE having either a high logic level or a low logic level in response to a voltage level of a reference voltage VREF. As previously noted by example, VREF is used by the memory device to determine the logic level of high speed input signals, such as those using the HSTL signaling format. In the present embodiment, VREF will be set to some predetermined voltage level between the high and low voltage supply levels, such as VDD/2 for HSTL signaling for example. If lower speed input signals are to be used, such as those using the LVTTL signaling format, then the VREF voltage is not required, and the VREF pin can be connected to either supply voltage level (VDD or VSS). From this point on, the HSTL and LVTTL signaling formats will be used to describe the operation of the embodiments, and VREF will be set to VSS when the memory device is to receive LVTTL signals. The clock switch circuit **402** is responsible for enabling generation of internal clock signals based on one of a parallel clock signal or a source synchronous serial clock signal, in response to the mode signal MODE provided by the mode setter **400**. A further discussion of the components of the clock switch circuit **402** will follow later.

[0061] The configurable input/output buffer of Figure 5 is implemented as a configurable data input/output buffer **404** that will sense HSTL or LVTTL input signals and pass either the received input signals or internal data from the memory device, to the output port Qn. The configurable data input/output buffer **404** will use the internally generated clock signals provided by clock switch circuit **402** in order to maintain synchronous operation in accordance with the selected input signaling format. While only one configurable input/output buffer is shown in Figure 5, persons of skill in the art will understand that there is one configurable input/output buffer for input signals DSI and CSI as well.

[0062] In the present example embodiments, VREF at the predetermined voltage level, typically VDD/2, will correspond to a serial clock mode of operation, while VREF at the VSS voltage level will correspond to a parallel clock mode of operation. This means that during assembly of the memory system, if each memory device receives the clock signal in series as in Figure 3A, then VREF will be set to the predetermined voltage level. Accordingly, the HSTL signaling format will be used. On the other hand, if each memory device receives the clock signal in parallel as in Figure 3C, then VREF will be set to VSS. Then the LVTTL signaling format will be used instead. Therefore, VREF is sensed by mode setter **400** to set signal MODE to a first logic state corresponding to a serial clock mode of operation or to a second logic state corresponding to a parallel clock mode of operation.

[0063] Returning to the clock switch circuit **402** with this understanding of the MODE signal, clock switch circuit **402** includes a clock input buffer **406**, a clock generator **408**, and a clock output buffer **410**. The clock input buffer **406** is connected to the clock input ports CK and CK#, and generates either a single ended clock signal based on two differential clock inputs CK and CK#, or separate buffered versions of CK and CK# in response to the logic state of the mode signal MODE. For example, the single ended clock signal is generated when MODE is at the first logic state. The clock generator **408** receives either the single ended clock signal or the buffered versions of CK and CK# to provide two internal clock phases used for internal operation and generating the proper output timing. The internal clock signals CKI and CKI# are distributed to the internal circuits of the memory device, and to the configurable input/output buffers. The clock output buffer **410** receives the internal clock signals CKI and CKI#, and drives them through the CKO and CKO# output port when MODE is at the first logic state. When MODE is at the second logic state corresponding to a parallel mode of operation, the clock output buffer **410** is disabled since there is no need to provide the serial clock to the next memory device.

[0064] The configurable data input/output buffer **404** includes a data input buffer **412**, a data switch **414**, and a data output buffer **416**. The data input buffer **412** receives input data Dn and the reference voltage VREF, which is used when MODE is at the first logic level. A buffered input signal Din is then provided to the data switch **414**, which passes either Din or native data from the memory device, to the data output buffer **416**. The native data in the present example includes even data RD_e and odd data RD_o, because data is provided on both the rising and falling edge of the clock signal. Signals EN_o and EN_e are used to

select Din or both RD_e and RD_o to pass to the data output buffer **416**. Furthermore, it is noted that the serial data of Dn is provided on both the rising and falling edge of the clock signal. The selection of which data to pass will depend on the command received by the memory device. In either case, the data is synchronized to the internal clock signals CKI and CKI# and passed to the data output buffer as even and odd data Dout_e and Dout_o respectively. The data output buffer **416** will then interleave the Dout_e and Dout_o bits of data in response to the clock and drive it through the Qn data output port.

[0065] An advantage provided by the clock mode configuration circuit of Figure 5 is that no additional package pin is required because VREF is now used for two different purposes. If each memory device is individually packaged, then the package size is thereby minimized by reducing the number of pins that are required. Those skilled in the art will understand that smaller package sizes minimize required printed circuit board area upon which the memory system is integrated upon. Alternately, the memory devices of the serial memory systems shown in Figures 3A and 3C can be packaged together as a system in package (SIP). Once again, a reduced pin count will minimize the package size. The mode setter **400** being connected to the VREF input port provides this advantage. A further advantage is that a single memory component can operate correctly in high performance source synchronous clocking configurations, and in lower performance parallel clocking configurations with reduced power consumption, as will be further explained as follows.

[0066] Figure 6 is a circuit schematic of the mode setter **400**, according to one embodiment. Mode setter **400** will sense the voltage level of VREF and drive signal MODE to either a first logic level or a second logic level. In this particular example, the first and second logic levels can correspond to VDD and VSS respectively. Mode setter **400** includes a sense circuit **500**, a latch **502**, and a digital delay circuit **504**. The sense circuit **500** includes resistor elements **506**, **508**, a power shut-off device **510** connected in series between VDD and VSS, and a comparator **512**. In the present embodiment, power shut-off device **510** is implemented as an n-channel transistor having a gate terminal receiving an enable signal EN. The shared terminal of resistor elements **506** and **508** is connected to one input of comparator **512**, while a second input of comparator **512** receives the reference voltage VREF. Resistor elements **506** ad **508** form a reference voltage circuit. The ratio of resistor elements **506** and **508** can be set depending on the value of VREF to be detected. For example, if the stable voltage level of VREF is to be VDD/2, then resistor element **506** can be

set to 3R while resistor element **508** can be set to R. Accordingly, the shared terminal "x" will be at approximately VDD/4. The comparator **512** can be implemented with any known circuit, and in the present example, includes an optional enable input for receiving the enable signal EN.

[0067] The latch **502** can be implemented with any known circuit, and in the present example optionally receives enable signal EN. When the latch enable input is high the signal appearing on the D input is provided at the Q output. When the latch enable input transitions from high to low, the state of the D input is latched and provided to the output Q. The digital delay circuit **504** includes a counter **514**, a NOR logic gate **516**, and an inverter **518**. The counter **514** is an n-bit counter, where n can be any integer number greater than 1, having only its most significant bit output (MSB) connected to the input of inverter **518**. The counter is reset such that all bits, including the MSB output, are set to 0 (VSS) when RST# is at the low logic level. MSB is also connected to one input of NOR logic gate **516**, while its other input receives clock signal CK. Therefore, when reset, MSB is at VSS in the present example. When RST# is released by setting it to the high logic level, the counter is permitted to increment the count with each rising or falling edge of the clock CK. When the MSB is toggled to 1 (VDD), then power shut-off device **510** is turned off via inverter **518**, the comparator **512** is turned off to save power, the MODE output is latched, and the clock input of the counter **514** is disabled via the NOR gate to freeze the counter **514**. After the delay provided by the counter, MODE will be stably set to either VDD or VSS.

[0068] The operation of mode setter **400** is now described with reference to the sequence diagram of Figure 7. At time t1, RST# is at VDD, which results in counter **514** driving MSB to VDD. EN is then driven to VSS by inverter **518**, which turns off power shut-off device **510** to allow node "x" to float to VDD. The advantage of having node "x" float to VDD while the circuit is disabled is that regardless of the value of VREF, MODE will immediately default to VSS when comparator **512** and latch **502** are enabled, because node "x" will always be greater than VREF. This immediately sets the memory device to the parallel clock mode of operation so that normal memory operations can begin without delay. At time t2, RST# is pulsed to VSS to reset MSB to VSS. RST# returning high releases counter **514** to count a predetermined number of edges of clock signal CK to allow the analog portions of the circuit sufficient time to settle and properly determine the level on the VREF pin, even if the RST# low level pulse is short. When MSB drops to VSS, EN is driven to VDD by inverter

518 to enable the resistor divider, comparator **512**, and latch **502** to evaluate the level on the VREF pin and determine the MODE of operation. Because node "x" is currently floating at VDD, the enabled comparator **512** will drive a low logic output which is then passed through latch **502** for setting MODE to the low logic level.

[0069] In the present example, it is assumed that VREF is configured to be approximately VDD/2, and the ratio of resistor elements **506**/**508** is 3R/R. While the circuit is enabled, the voltage at node "x" will therefore settle to a level of approximately VDD/4. Eventually, the voltage on node "x" will be established at a steady VDD/4 level as shown in Figure 7 at time t3. If VREF is set to VSS, then no change will occur in comparator **512** to keep MODE at VSS. On the other hand, if VREF is set to VDD/2, comparator **512** will then drive its output to VDD which causes latch **502** to drive MODE to VDD around time t3. Eventually, counter **514** will set MSB to VDD at time t4 to drive EN to VSS. MSB at VDD will cause NOR logic gate **516** to output a low logic level signal to effectively terminate counting by counter **514**, thereby "freezing" the counter **514**. Once EN drops to VSS, power shut-off device **510** is turned off and node "x" will eventually float to VDD. However, EN at VSS will now disable comparator **512**, and latch **502** is prevented from latching any changing output signal on its D input. Therefore, power is saved by turning off sense circuit **500**. In the source synchronous mode of operation, normal memory operations can begin only after PLL or DLL synchronization. This time is not wasted since the voltage at node "x" will settle to the correct value during this synchronization period.

[0070] Therefore, the time delay corresponding to the time for counter **514** to toggle MSB to VDD will be sufficiently long to ensure that node "x" and VREF have stabilized for sensing by comparator **512**. By example only, a 1ms time delay may be a sufficient time delay provided by digital delay circuit **504**. Hence by turning off power shut-off device **510** after MSB is toggled to VDD, the current path from VDD through the resistor elements **506** and **508** to VSS is cut off, thereby conserving power during operation of the memory device. This time delay can be selected based on the clock frequency being applied and the number of bits in the counter **514**.

[0071] Figure 8A is a schematic embodiment of the clock switch circuit **402** and the configurable data input/output buffer **404** of Figure 5. Both circuits can be referred to as a configurable input circuit, since one receives an input clock and the other receives input data from at least one input data port. The clock switch circuit **402** is configurable to operate in the

parallel or serial clock modes in response to a logic state of the mode signal MODE, while the configurable data input/output buffer **404** is configurable to receive input data in either the HSTL or LVTTL signaling format in response to the logic state of MODE. It is noted that this Dn input can receive both write data and commands from a memory controller. In order to simplify the circuit schematic of Figure 8A, the command data path and the input write data path are not shown. The same numbered reference numbers appearing in Figure 8A have been generally described in Figure 5.

[0072] The details of the clock switch circuit **402** now follows. The clock input buffer **406** includes a comparator **700** for receiving complementary clock signals from clock input ports CKI and CKI#, a first buffer circuit **702** receiving a clock signal from clock input port CKI and a second buffer circuit **704** receiving a complementary clock signal from clock input port CKI#. Comparator **700** is enabled by one state of MODE while the first and second buffers **702** and **704** are both enabled by an opposite state of MODE. Thus, only one of the comparator **700** and the buffers **702** and **704** will be active for any single logic state of MODE. However, the outputs of comparator **700** and buffers **702** and **704** are coupled to clock generator **408** in parallel. For the presently described example where mode setter **400** sets MODE to the first logic state corresponding to the serial clock mode of operation and to a second logic state corresponding to the parallel clock mode of operation, MODE at the first logic state will enable comparator **700**. Accordingly, MODE at the second logic state will enable first and second buffers **702** and **704**.

[0073] Clock generator **408** includes a phase locked loop (PLL) circuit **706** that is enabled when MODE is at the first logic state. When enabled, PLL circuit **706** will generate clock outputs shifted by 90, 180, 270 and 360 degrees relative to the clock signal received at its REF input, which is connected to the output of comparator **700**. These shifted clock outputs are provided from the terminals labeled 90, 180, 270 and 360. In the serial clock mode of operation, received input clock transitions and received input data transitions are coincident. The PLL circuit **706** is used to place the edges of the internal clock signals within the input data valid window, for reliable data capture. A feedback input FB receives the 360 degree shifted clock output to facilitate locking of the clock signals. Those skilled in the art should be familiar with PLL circuit operation, and that the clock will be locked after several clock cycles to ensure stable operation. Instead of a PLL, a delayed lock loop (DLL) circuit can be used in place of the PLL circuit **706**. A PLL and a DLL are both examples of clock

synthesizers which can be used in the disclosed embodiments. The 90 and 270 degree clock outputs are provided to first inputs of 2-1 multiplexors **708** and **710**, both being controlled by MODE. The second inputs of multiplexors **708** and **710** receive the outputs of buffers **702** and **704** respectively. In the parallel clock mode of operation, the received input clock transitions will be within the input data valid window so that no phase shifted clocks are required. Therefore, multiplexors **708** and **710** collectively form a switch circuit for selectively passing one of the 90 and 270 degree clock outputs from PLL circuit **706** and the buffered clock signals from buffers **702** and **704** in response to MODE. In the present example when MODE is at the first logic level, PLL circuit **706** is enabled and multiplexors **708** and **710** will be controlled to pass the 90 and 270 degree clock outputs as internal clock signals CK and CK#. On the other hand, when MODE is at the second logic level, PLL circuit **706** is disabled and multiplexors **708** and **710** will be controlled to pass the clock signals from buffers **702** and **704** as the internal clock signals CK and CK#. Accordingly, turning off the PLL that is not being used will reduce power consumption.

[0074] While not explicitly shown in Figure 8A, complementary internal clock signals CK and CK# are distributed to other circuits within the memory device. An optional feature of clock generator **408** is the phase selector circuit that includes multiplexors **712** and **714**. First inputs of multiplexors **712** and **714** receives the internal clock signals CK# and CK respectively, while second inputs receive the 360 and 180 degree clock outputs from PLL circuit **706**. Both multiplexors **712** and **714** are controlled by signal PHASE, which is provided by the command decoder of the memory device. The purpose of the phase selector circuit is to centre the output clock signals provided on output ports CKO and CKO# with the output data provided on the output port Qn. In a serially connected memory system, this feature is enabled in the last memory device of the system. The advantage is that the memory controller design can be simplified as it will not require a PLL or DLL to reliably receive the data from the last memory device in the ring. Further details of the application of this feature in a memory system will be described later. The clock output buffer **410** includes a pair of drivers **716** and **718** for driving the clock signals provided by multiplexors **712** and **714** onto output ports CKO and CKO#. Both drivers **716** and **718** are enabled by MODE, when it is at the first logic level representing the serial clock mode for example.

[0075] Therefore, in response to MODE, clock switch circuit **402** is configured to generate internal clock signals corresponding to a serially provided source synchronous

clock signal or to a parallel clock signal. Because the memory devices will operate at high speeds in response to a high speed source synchronous clock signal, this mode can be referred to as a high speed mode of operation. On the other hand, because the parallel clock signals will be at a lower frequency than the source synchronous clock, the other mode can be referred to as a low power mode of operation since circuits such as the comparator **700**, PLL **706**, and drivers **716** and **718** will be turned off, and the lower frequency operation reduces overall power consumption relative to when the memory device operates at high frequencies. In either mode of operation, the internal clock signals CK and CK# will be generated for use by other circuits of the memory device, such as the configurable data input/output buffer consisting of data input buffer **412**, data switch **414** and data output buffer **416**.

[0076] The data input buffer **412** includes a comparator **720**, a buffer circuit **722** and a data input selector **724**, where the data input selector **724** is implemented as a 2-1 multiplexor. Comparator **720** has one input connected to input port Dn, and a second input connected to the reference voltage input port VREF. The buffer circuit **722** is also connected to input port Dn. Comparator **720** generates a logic output corresponding to the voltage level of Dn relative to VREF, while buffer circuit **722** drives a logic level corresponding to what it receives. All three circuits are controlled by MODE, and in the presently described example where MODE being at the first logic level corresponds to a high speed mode of operation, comparator **720** is enabled, buffer **722** is disabled, and data input selector **724** is controlled to pass the output of comparator **720**. The output of data input selector **724** is referred to as Din.

[0077] Since the memory devices of the present embodiments are to be serially connected to each other, external data arriving at the Dn input port can be selectively passed through a memory device to the designated, or addressed, memory device. However, each memory device can also provide local read data that is to be passed on to the memory controller through any intervening memory devices. The purpose of data switch **414** is to selectively pass either external Dn data or local read data to the output port Qn. The data switch **414** includes external data input latches **726** and **728**, data output selectors **730** and **732**, and output latches **734** and **736**. In the present embodiment, data is latched on both edges of the internal clock CK. Therefore, latches **726** and **728** receive CK and CK# respectively. Data output selector **730** passes one of latched external data from data input

latch **726** or local even read data RD_e in response to select signal EN_e. Similarly, data output selector **732** passes one of latched external data from data input latch **728** or local odd read data RD_o in response to select signal EN_o. Select signals EN_e and EN_o are provided by the command decoder of the memory device.

[0078] The data output latches **734** and **736** latch the outputs of output selectors **730** and **732** in response to active edges of the internal clock signals CK# and CK respectively. The operation of the data switch **414** is well understood by those of skill in the art familiar with double data rate operation. The data output buffer **416** includes a data output selector **738** implemented as a 2-1 multiplexor, and a driver **740**. Data output selector **738** alternately passes the outputs of data output latches **734** and **736** in response to CK, which is then provided onto output port Qn by driver **740**. In summary, when MODE is set, the data input buffer **412** is automatically configured to receive a corresponding data signal format, and the appropriate internal clock signals are automatically generated by clock switch circuit **402** for use by data switch **414** and data output buffer **416**.

[0079] Therefore, the same memory devices connected in series in a ring topology with a memory controller can be configured to receive either a parallel clock or a source synchronous clock in series in response to a reference voltage that is used for sensing data signal voltage levels, as shown in Figues 3A and 3C. Furthermore, data input circuits are automatically configured to receive data signals having a signaling format that corresponds with the parallel clock and the source synchronous clock. Although not shown, the output buffer drive strength can also be configured based on the MODE setting, to optimize performance and power in the multi-drop bus and point-to-point ring topologies.

[0080] As previously discussed, each memory device can include the optional phase selector circuit that includes multiplexors **712** and **714** shown in Figure 8A. In use with the memory system of Figure 3A for example, only the last memory device **110** will have PHASE set to a logic level for passing the 180 and 360 degree clock outputs from PLL **706**. For example, all memory devices except the last memory device in the ring will output the 90 and 270 degree clocks, which are the same clocks used to generate output data transitions. Therefore, output clock edges and output data edges are co-incident and fully compatible with the input sampling stages of the next memory device. If the controller does not have a PLL or DLL to shift the input clock edges to the middle of the input data valid window, the PHASE bit can be set to provide output clock transitions already positioned in the middle of

the data valid window, so that the controller can sample received data directly with the received clock signal. In the present examples, these would be the 180 and 360 degree degree clock outputs. Signal PHASE can be set by loading a single bit register from a command received by the memory device. This would be set during a power up sequence of the memory system, which would start with the memory controller **202** executing an algorithm for assigning addresses to each memory device. Such algorithms can include the ones disclosed in the previously mentioned commonly owned U.S. Patent Applications which are directed to generating ID numbers for memory devices in the memory system.

[0081] During ID number assignment, all memory devices will have the PHASE bit set to output co-incident clock and data edges. In the present embodiments for example, this can correspond to a default state of PHASE in which the 90 and 180 degree clocks are output. If the memory controller does not have a PLL or DLL, then it will not be able to properly receive data until PHASE of the last memory device has been properly programmed. However, since devices will not output any data transitions at all until their device addresses have been assigned, the memory controller will recognize transitions on its data input as an indication that the last memory device has been programmed with a device address. Once the last memory device in the system is known by the memory controller, a command is issued to set the aforementioned single bit register that changes the default state of PHASE to one for passing the 180 and 360 degree clock outputs. After this setting has taken effect full communication around the ring can occur.

[0082] Figure 8B is a timing diagram showing the operation of the circuits of Figure 8A. In particular, the timing diagram of Figure 8B shows the internally generated clock signals in response to different settings of MODE and PHASE during a continuous sequence of CKI and CKI# clock transitions. At the same time, hypothetical data on the Qn output port is shown to contrast timing differences relative to the output data valid windows in response to different logic levels of MODE and PHASE. This timing diagram is merely illustrative of the behaviour of the circuits of Figure 8A. Those skilled in the art will understand that data would not be provided proximate to transitions of MODE and PHASE during actual use. Dynamic transitions of MODE and PHASE would be done during an initialization or reset period of the memory system. Figure 8B includes signal traces for MODE, PHASE, CKI and CKI#, the internally generated 90, 180, 270 and 360 degree clock signals from the clock synthesizer, CK and CK# and CKO and CKO#.

[0083] In the time period between time t1 and t2, the circuit is operating in the parallel clock mode when MODE is at a low logic level. Because MODE is at the low logic level, PLL circuit 706 is turned off resulting in its 90, 180, 270 and 360 clock outputs being set to the low logic level. The internal clocks CK and CK# are therefore buffered versions of CKI and CKI# respectively. Using the circuits shown in Figure 8A, the data transfer operation between the input Dn (not shown) and Qn will follow the same sequence as shown in Figure 3D, except that the latching operations are now responsive to CK and CK# instead of directly to CKI and CKI#. With MODE at the low logic level, the clock output buffer 410 is disabled to keep CKO and CKO# at the low logic level.

[0084] In the time period between time t2 and t4, the circuit is operating in the serial clock mode when MODE is at a high logic level. Because MODE is at the high logic level, PLL circuit 706 is turned on to generate the 90, 180, 270 and 360 clock outputs. The current timing diagram assumes that mode reset and PLL locking is immediate. With MODE at the high logic level, internal clocks CK and CK# will correspond to the 90 and 270 degree clock outputs, and the clock output buffer 410 is enabled to drive CKO and CKO# with the CK and CK# clocks. Using the circuits shown in Figure 8A, the data transfer operation between the input Dn (not shown) and Qn will follow the same sequence as shown in Figure 3B, except that the latching operations are now responsive to CK and CK# instead of directly to the 90 and 270 degee clock outputs.

[0085] At time t3 PHASE is at the high logic level, but in actual use PHASE is set to either the high or low logic level before normal operations of the memory device. The transition shown in Figure 8B merely contrasts the relationship between rising and falling edges of CKO and CKO# relative to the output data of Qn between different logic levels of PHASE. With PHASE set to the high logic level, multiplexors 712 and 714 will pass the 180 and 360 degree clock outputs to the clock output buffer 410. Accordingly, CKO and CKO# will correspond to the 180 and 360 degree clock outputs, thereby centering the clock edges within the data valid windows.

[0086] The system embodiments of Figures 3A and 3C are static, meaning that once manufactured or assembled for use, they cannot be changed. According to another embodiment, the memory system can be dynamically changed such that the memory devices receive either a parallel clock or a source synchronous clock in series. Figure 9 is a an embodiment of a dynamically configurable serial memory system where the memory

controller provides both parallel and source synchronous clocks, and data signals in signaling formats corresponding to the type of clocks. The memory devices will include the same circuits shown in Figure 8A, with a minor modification to receive both parallel and source synchronous clock signals.

[0087] In Figure 9, configurable serial memory system **800** includes a memory controller **802**, and four dynamically clock configurable memory devices **804**, **806**, **808** and **810**. Memory controller **802** provides the same control and data signals as memory controller **102** or **202**, but now provides parallel complementary clocks through clock output ports CK1 and CK1#, and complementary source synchronous clocks through clock output ports CK2 and CK2#. Memory controller **802** is further configured to dynamically provide data and the strobe signals through its Qn, CSO and DSO output ports in one signaling format corresponding to the parallel clock, and another signaling format corresponding to the source synchronous clock. For example, LVTTL signaling can be used with the parallel clock while HSTL signaling can be used with the source synchronous clock. Memory controller **802** further includes serial clock input ports CKI and CKI# for receiving the source synchronous clocks from the last memory device. Each memory device is similarly configured to the memory devices shown in Figures 3A and 3C, except that each now includes a parallel input clock ports CK1 and CK1# and serial input clock ports CKI and CKI#. Depending on the level of VREF, each memory device will selectively use either the parallel clocks or the source synchronous clocks.

[0088] Figure 10 is a schematic showing details of a clock switch circuit **402** according to an alternate embodiment. This clock switch circuit shows a modification to the clock switch circuit shown in Figure 8A, where elements that are the same share the same reference numerals. The only difference over the embodiment of Figure 8A is that clock input buffer **406** now includes comparator **900**, first buffer circuit **902** and second buffer circuit **904** that replace comparator **700**, first buffer circuit **702** and second buffer circuit **704** of Figure 8A. Comparator **900** has its inputs connected to clock input ports CKI and CKI# that are dedicated to receiving complementary source synchronous clock signals. The first buffer circuit **902** and second buffer circuit **904** are connected to clock input ports CK1# and CK1 that are dedicated to receiving complementary parallel clock signals. Now each memory device can be physically connected to both parallel and source synchronous clocks at the same time. The voltage level of VREF will then determine which of the clock inputs are to be

used. In the memory system embodiment of Figures 9 and 10, VREF can now be controlled by the memory controller, or alternatively by some suitable circuit separate from the memory controller that is controllable to drive VREF to the predetermined voltage level, or to either supply voltage. Therefore, the memory system illustrated in Figures 9 and 10 can be dynamically switched to operate with the source synchronous clocks for high speed operation, or with the parallel clocks if low power consumption operation is desired.

[0089] Figure 11 is a flow chart summarizing the general algorithm executed by both the memory controller and the memory devices of the memory systems shown in Figures 3A, 3C and 9 for setting an operating mode. The method begins at step **1000** where the memory system is powered up, or reset by asserting the reset signal RST#. At step **1002** the memory controller will execute start-up algorithms, such as an algorithm to assign device ID numbers to each memory device in the memory system. At power up or reset, VREF will be set to a power supply voltage or to a predetermined voltage level. It should be understood to those skilled in the art that other start-up algorithms can be executed by the memory controller and the memory devices themselves. Each memory device will then sense the level of VREF at step **1004**, via their respective clock input buffers, such as the clock input buffer **406** shown in Figure 8A. The level of VREF is then determined at step **1006**, and if it is not a reference voltage, then it should be either the VDD or VSS voltage supply, and MODE is set to a first logic level at step **1008**. Otherwise, VREF is the predetermined reference voltage level and MODE is set to a second logic level at step **1010**.

[0090] Once MODE has been set, then all the memory devices will automatically configure their clock switch circuits and configurable data input/output buffers, such as clock switch circuit **402** and configurable data input/output buffer **404**, in the manner previously described at step **1012**. Once the memory devices have been configured to receive clock and data signals corresponding to MODE, then as an optional step, the memory controller can issue a command to switch PHASE of the last memory device from a default value to an active level. With reference to Figure 8A, the default value of PHASE at start-up or reset of the memory device can be a low logic level to pass CKI and CKI#, while an active value can be VDD for passing the 180 and 360 degree clock outputs of PLL **706**.

[0091] While the previously described embodiments are directed to serial memory devices, they can be applied to any semiconductor device that operates with a clock provided in parallel or in series.

[0092] In the preceding description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the embodiments of the invention. However, it will be apparent to one skilled in the art that for any particular embodiment of the invention, not all described details are required in order to practice that embodiment of the invention. In some instances, well-known electrical structures and circuits are shown in block diagram form in order not to obscure the invention. For example, specific details are not provided as to whether the embodiments of the invention described herein are implemented as a software routine, hardware circuit, firmware, or a combination thereof.

[0093] Certain adaptations and modifications of the described embodiments can be made. Therefore, the above discussed embodiments are considered to be illustrative and not restrictive.

WHAT IS CLAIMED IS:

1. A system comprising:

a memory controller; and

at least one non-volatile memory device communicatively coupled to the memory controller, the at least one non-volatile memory device comprising:

at least two non-volatile memory banks;

a chip enable input port to receive a chip enable signal for enabling the at least one non-volatile memory device;

first and second input ports to receive first and second input signals respectively, wherein the second input signal is a complementary signal to the first input signal;

a reference voltage input port to receive an external reference voltage;

n-bit-wide common data ports to receive common data signals carrying command data, address data and/or write data, wherein the write data to be latched in synchronization with both rising and falling edges of at least the first input signal and to be programmed into one of the at least two non-volatile memory banks addressable by the address data, and wherein n is an integer number greater than zero;

a first configurable input buffer being able to be configured to utilize the first input signal and the second input signal as a differential signaling configuration;

a second configurable input buffer being able to be configured to utilize the external reference voltage in order to determine logic level of the common data signal; and

a configurable output buffer being able to be configured to set an output drive strength.

ABSTRACT

A clock mode configuration circuit for a memory device is described. A memory system includes any number of memory devices serially connected to each other, where each memory device receives a clock signal. The clock signal can be provided either in parallel to all the memory devices or serially from memory device to memory device through a common clock input. The clock mode configuration circuit in each memory device is set to a parallel mode for receiving the parallel clock signal, and to a serial mode for receiving a source synchronous clock signal from a prior memory device. Depending on the set operating mode, the data input circuits will be configured for the corresponding data signal format, and the corresponding clock input circuits will be either enabled or disabled. The parallel mode and the serial mode is set by sensing a voltage level of a reference voltage provided to each memory device.

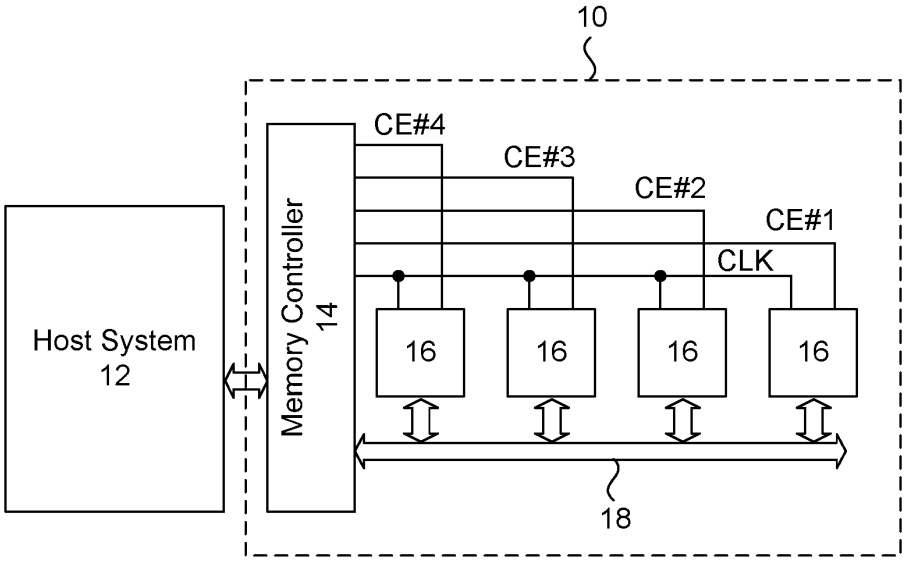


Fig. 1 (Prior Art)

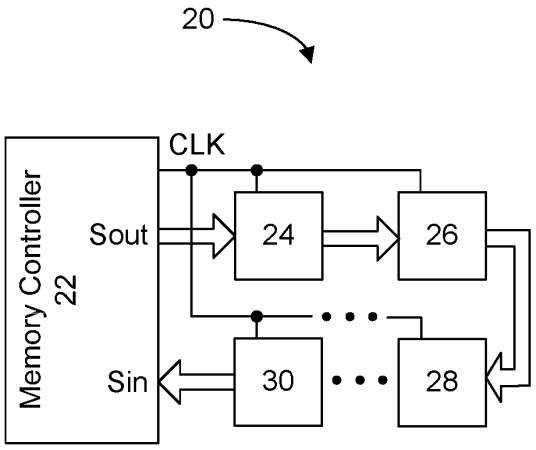

20
CLK
Memory Controller
22
Sout
Sin
24
26
30
28

Fig. 2A

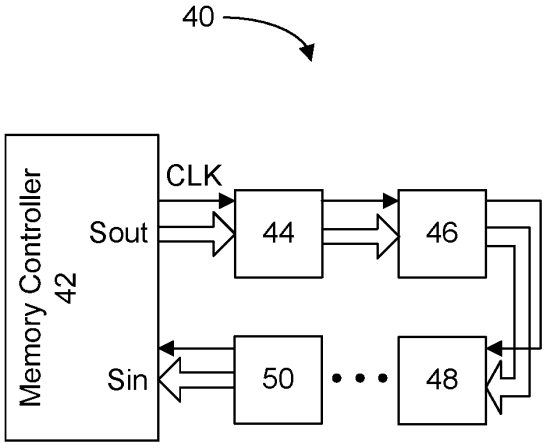

40
CLK
Memory Controller
42
Sout
Sin
44
46
50
48

Fig. 2B

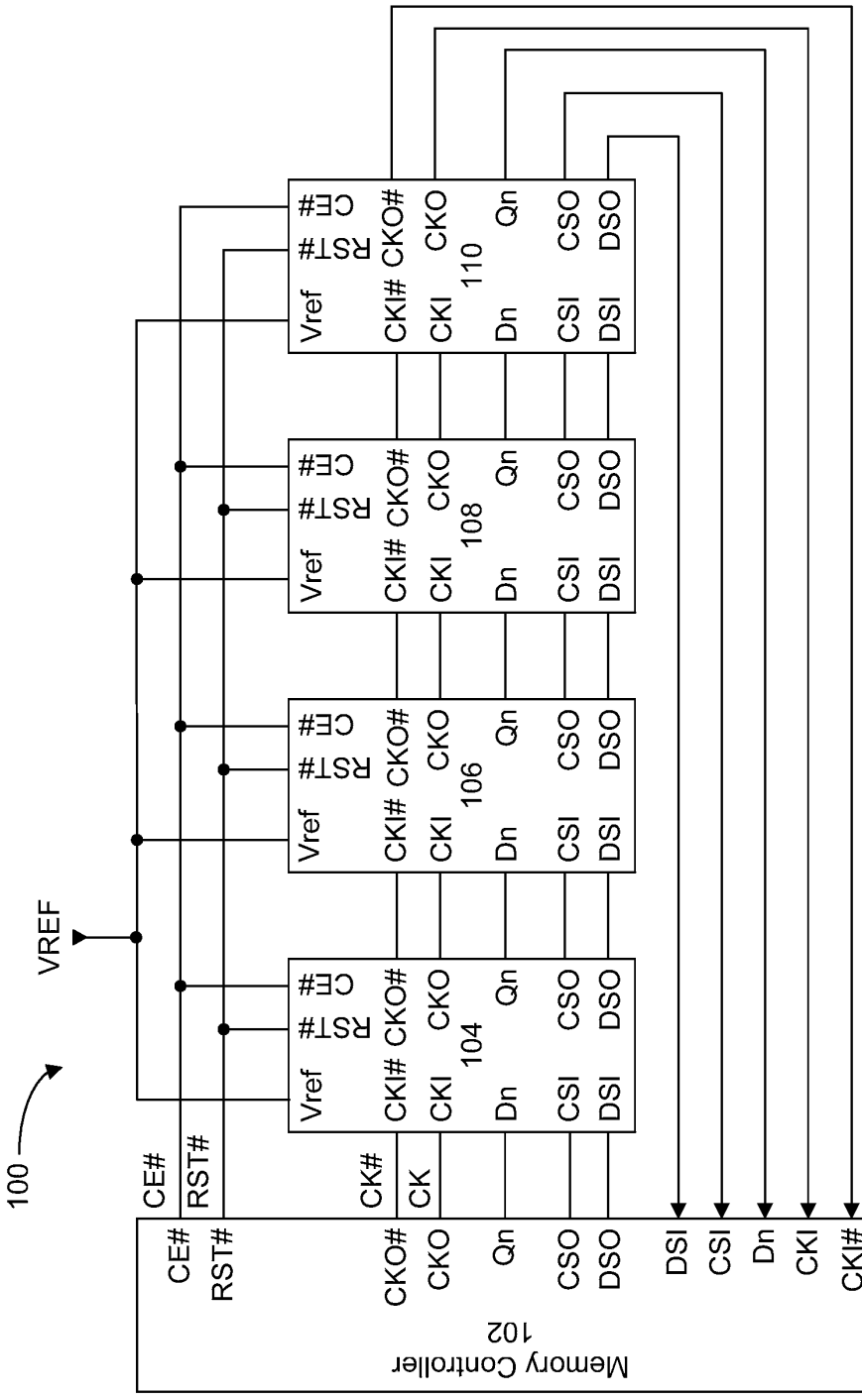

100
VREF
CE#
RST#
CK#
CK
Memory Controller
102
CKO#
CKO
Qn
CSO
DSO
DSI
CSI
Dn
CKI
CKI#
Vref
CKI#
CKI
Dn
CSI
DSI
CE#
RST#
CKO#
CKO
Qn
CSO
DSO
104
106
108
110

Fig. 3A

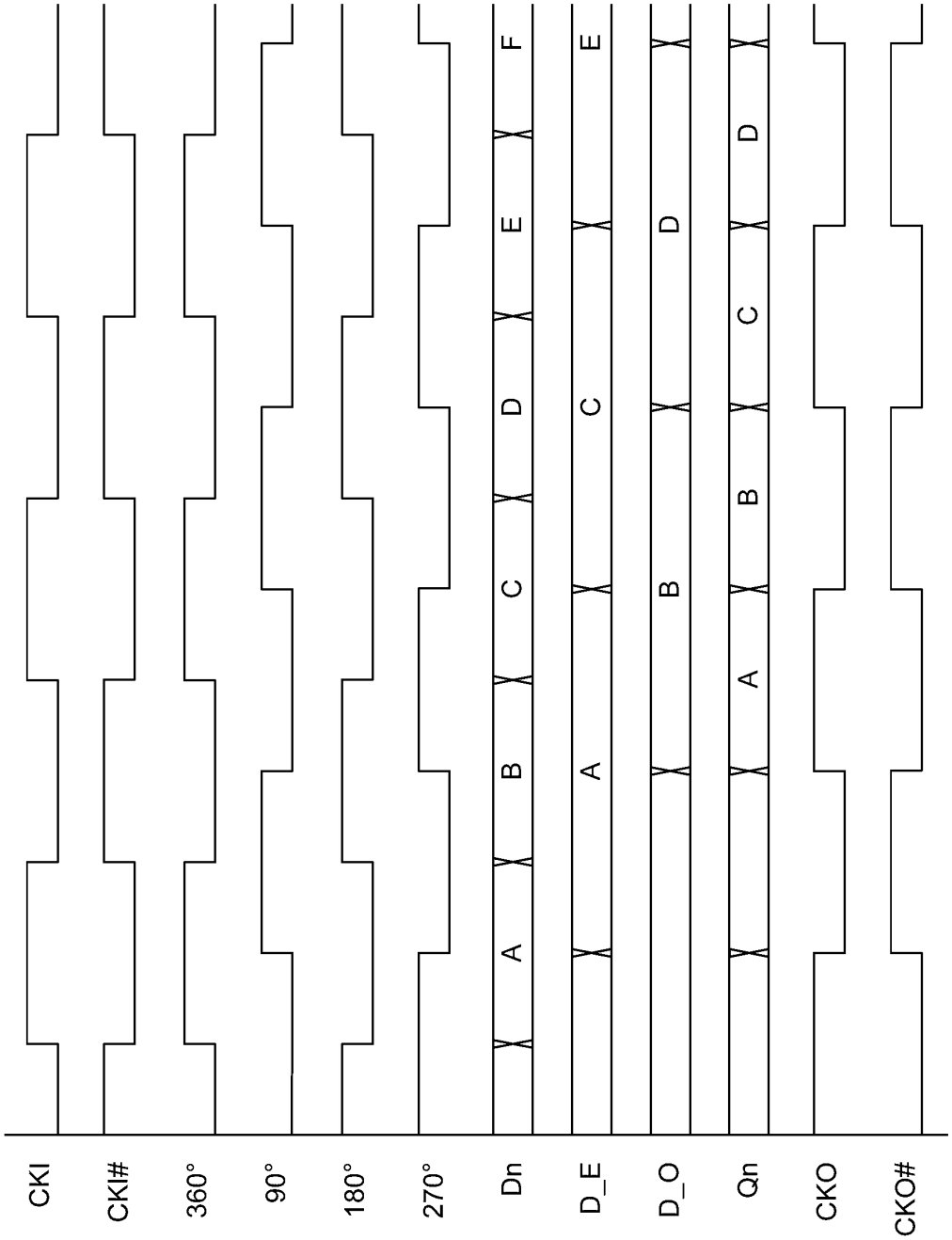


Fig. 3B

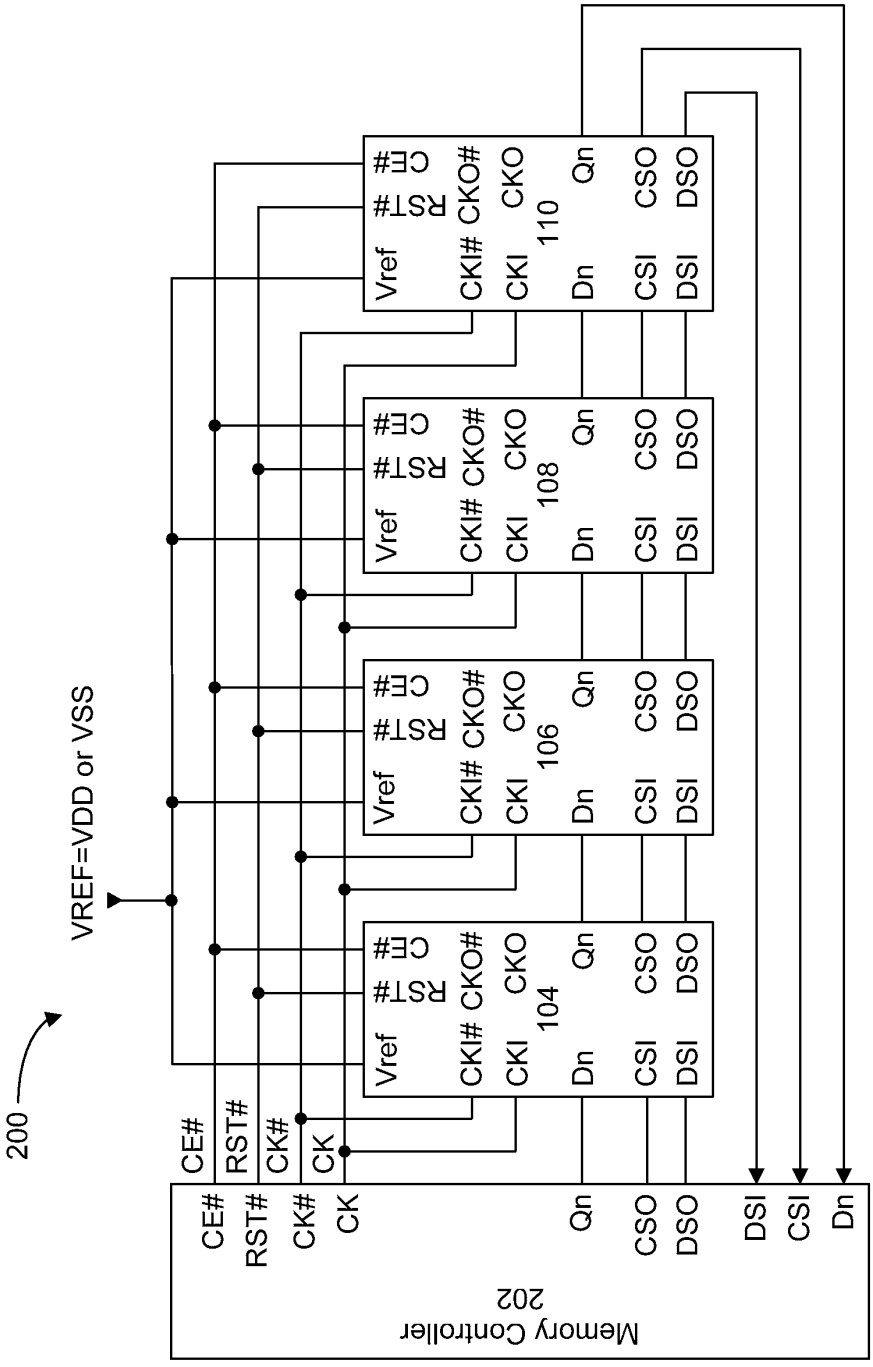

200
VREF=VDD or VSS
CE#
RST#
CK#
CK
Memory Controller
202
Qn
CSO
DSO
DSI
CSI
Dn
Vref
CE#
RST#
CKI#
CKO#
CKI
CKO
Dn
Qn
CSI
CSO
DSI
DSO
104
106
108
110

Fig. 3C

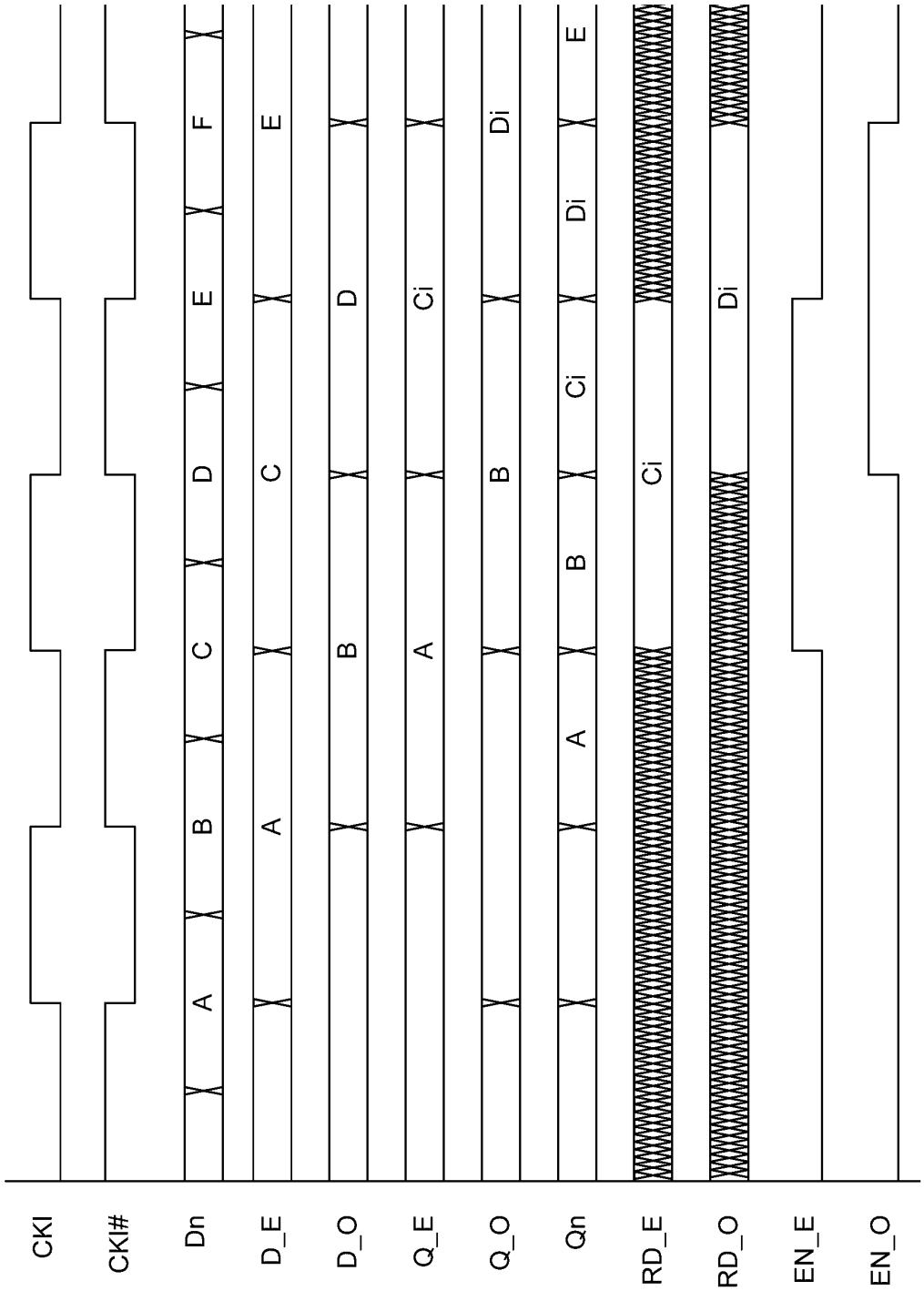


Fig. 3D

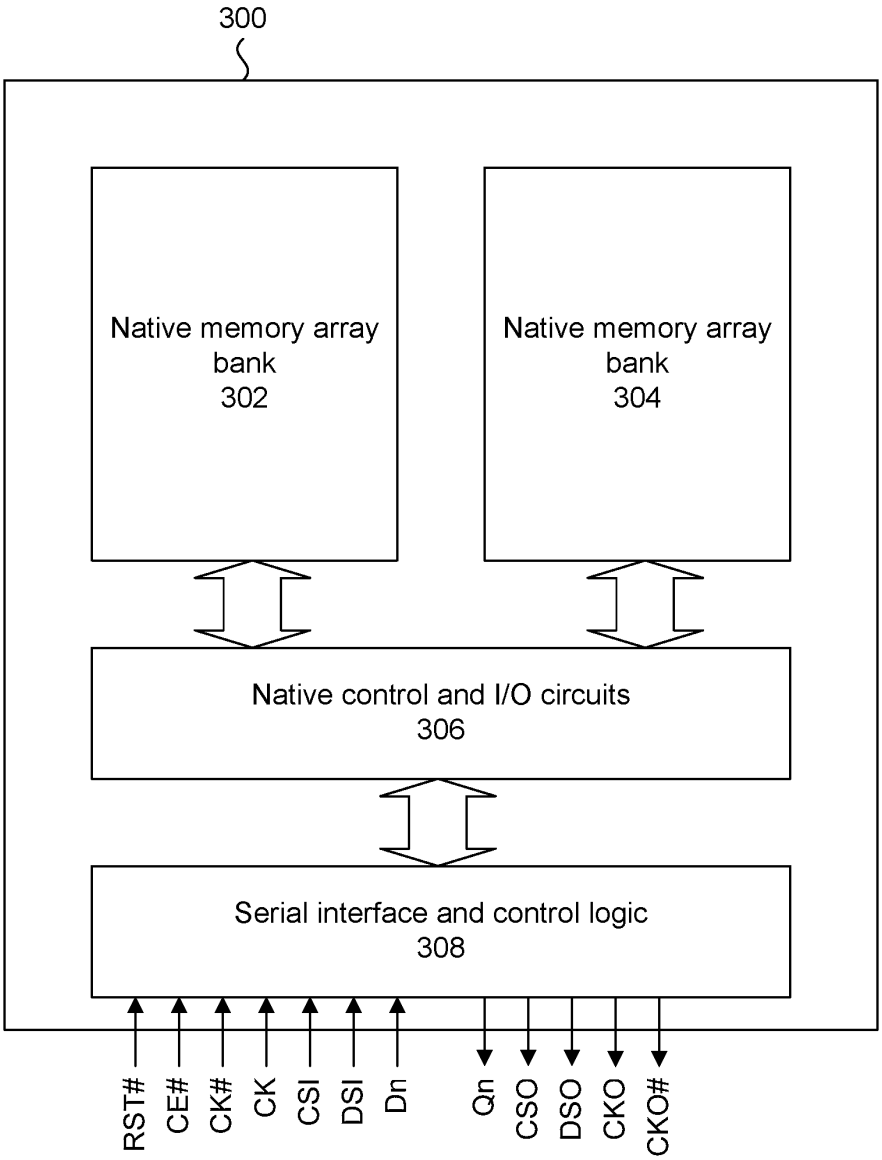

300
Native memory array bank 302
Native memory array bank 304
Native control and I/O circuits 306
Serial interface and control logic 308
RST#
CE#
CK#
CK
CSI
DSI
Dn
Qn
CSO
DSO
CKO
CKO#

Fig. 4

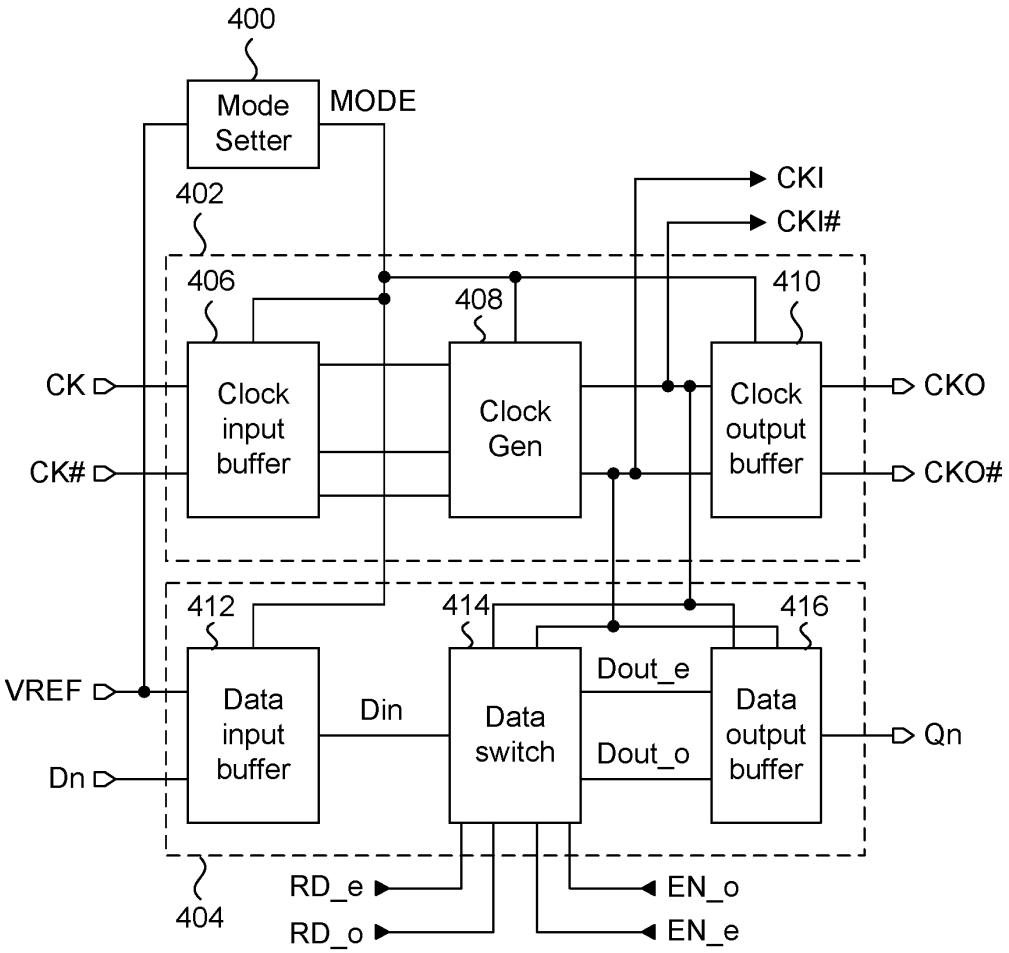

400
Mode Setter
MODE
402
CKI
CKI#
406
408
410
CK
CK#
Clock input buffer
Clock Gen
Clock output buffer
CKO
CKO#
412
414
416
VREF
Dn
Data input buffer
Din
Data switch
Dout_e
Dout_o
Data output buffer
Qn
404
RD_e
RD_o
EN_o
EN_e

Fig. 5

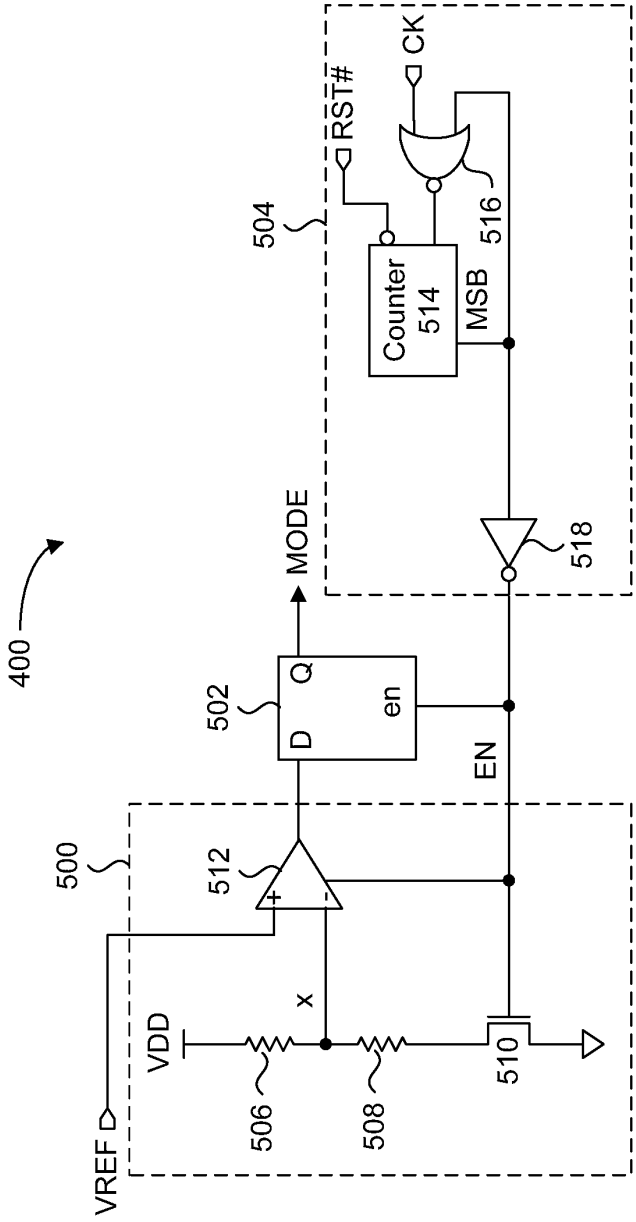

400
500
VREF
VDD
506
508
x
512
510
EN
502
D
Q
en
MODE
504
RST#
CK
Counter
514
MSB
516
518

Fig. 6

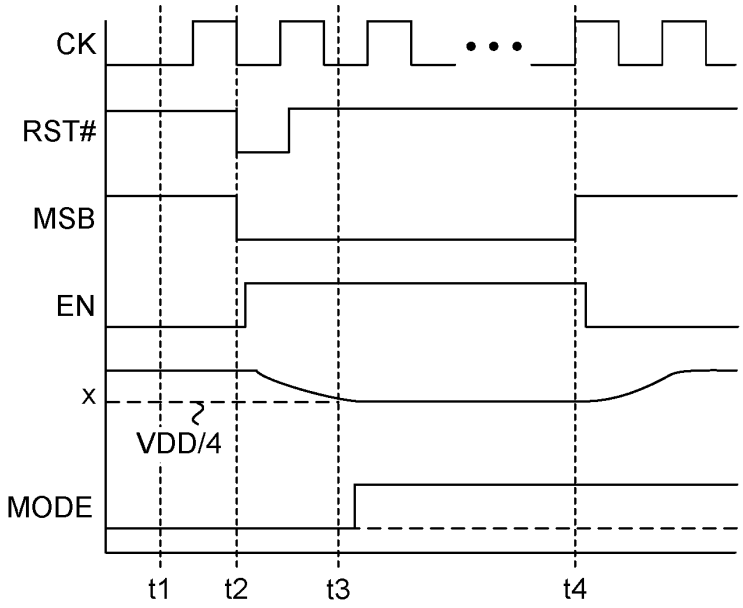


Fig. 7

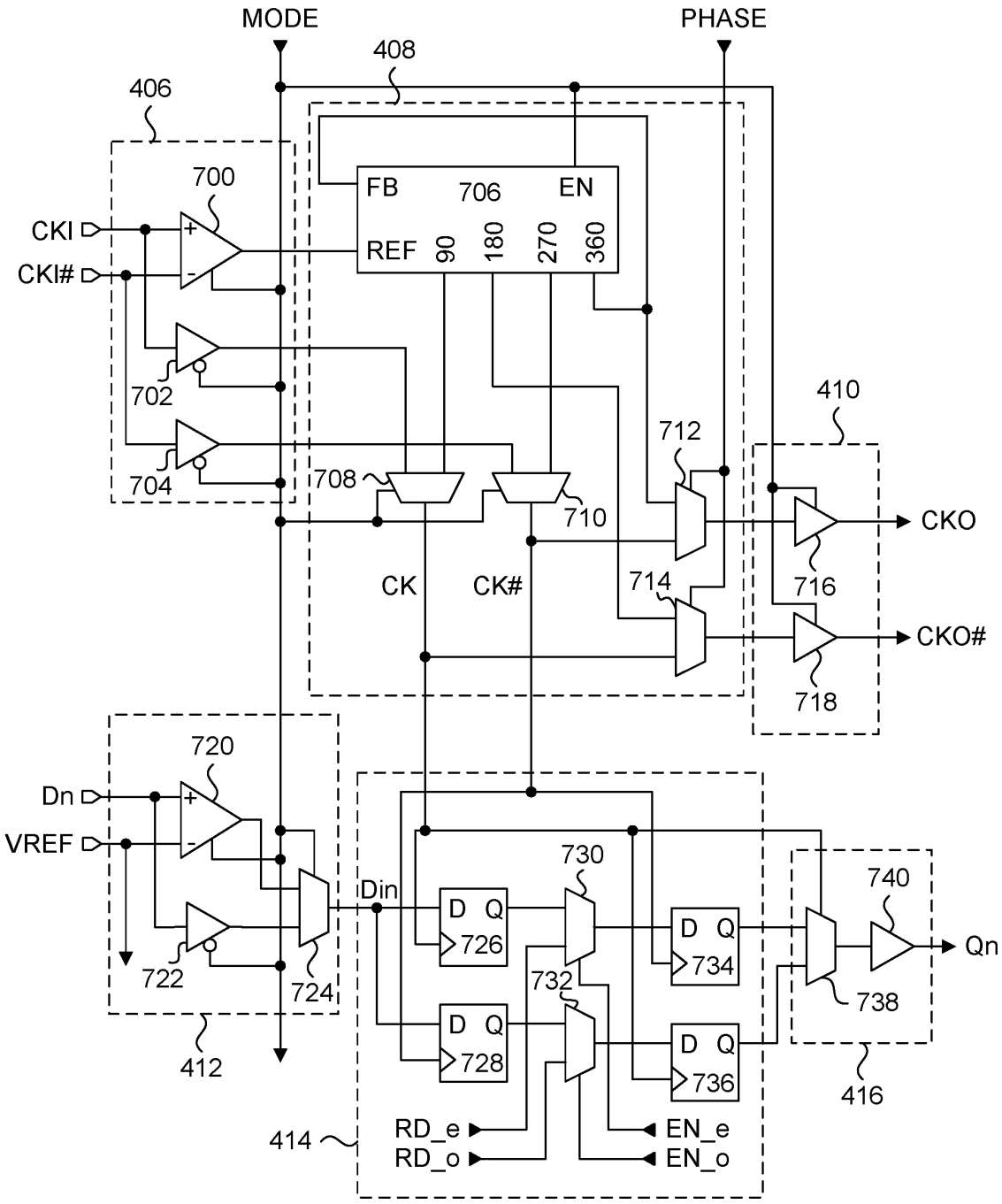

MODE
PHASE
408
406
700
FB
706
EN
REF
90
180
270
360
CKI
CKI#
702
704
708
710
712
410
CKO
716
CK
CK#
714
CKO#
718
720
Dn
VREF
722
724
412
Din
730
740
D Q
726
734
732
D Q
728
736
738
Qn
416
414
RD_e
RD_o
EN_e
EN_o

Fig. 8A

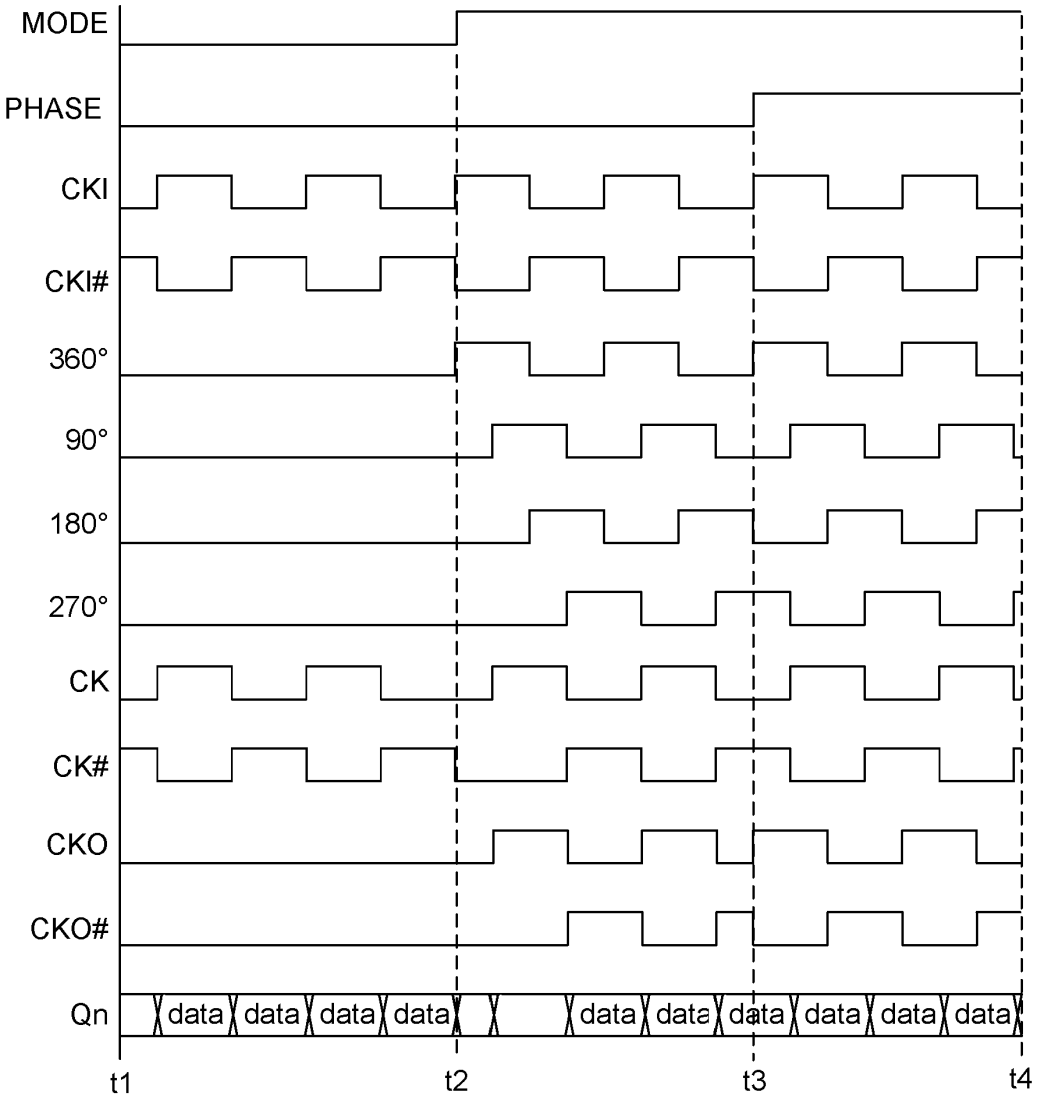

MODE
PHASE
CKI
CKI#
360°
90°
180°
270°
CK
CK#
CKO
CKO#
Qn
data
data
data
data
data
data
data
data
data
data
t1
t2
t3
t4

Fig. 8B

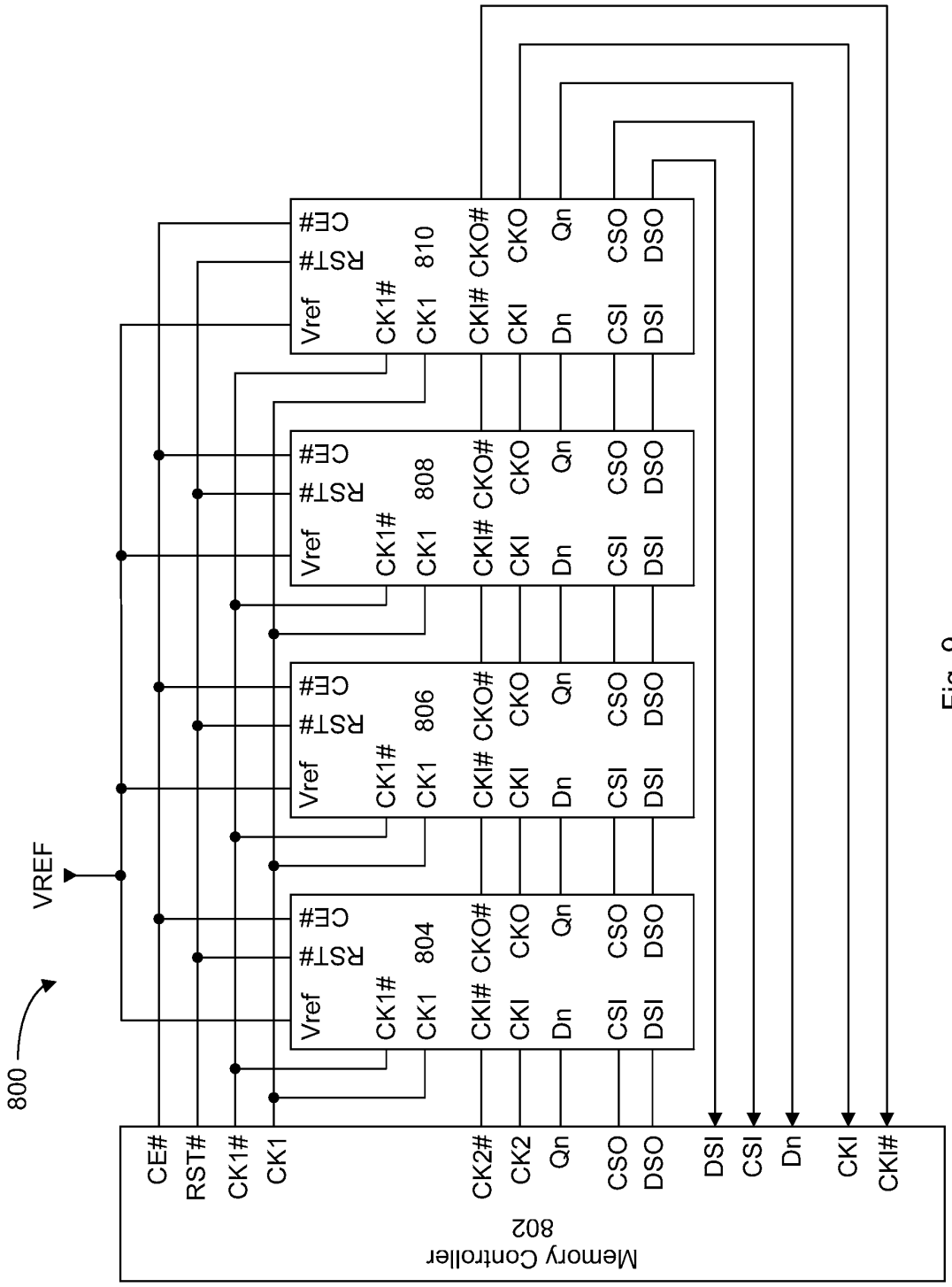

800
VREF
Memory Controller
802
CE#
RST#
CK1#
CK1
CK2#
CK2
Qn
CSO
DSO
DSI
CSI
Dn
CKI
CKI#
804
806
808
810
Vref
CK1#
CK1
CKI#
CKO#
CKI
CKO
Dn
Qn
CSI
CSO
DSI
DSO
RST#
CE#

Fig. 9

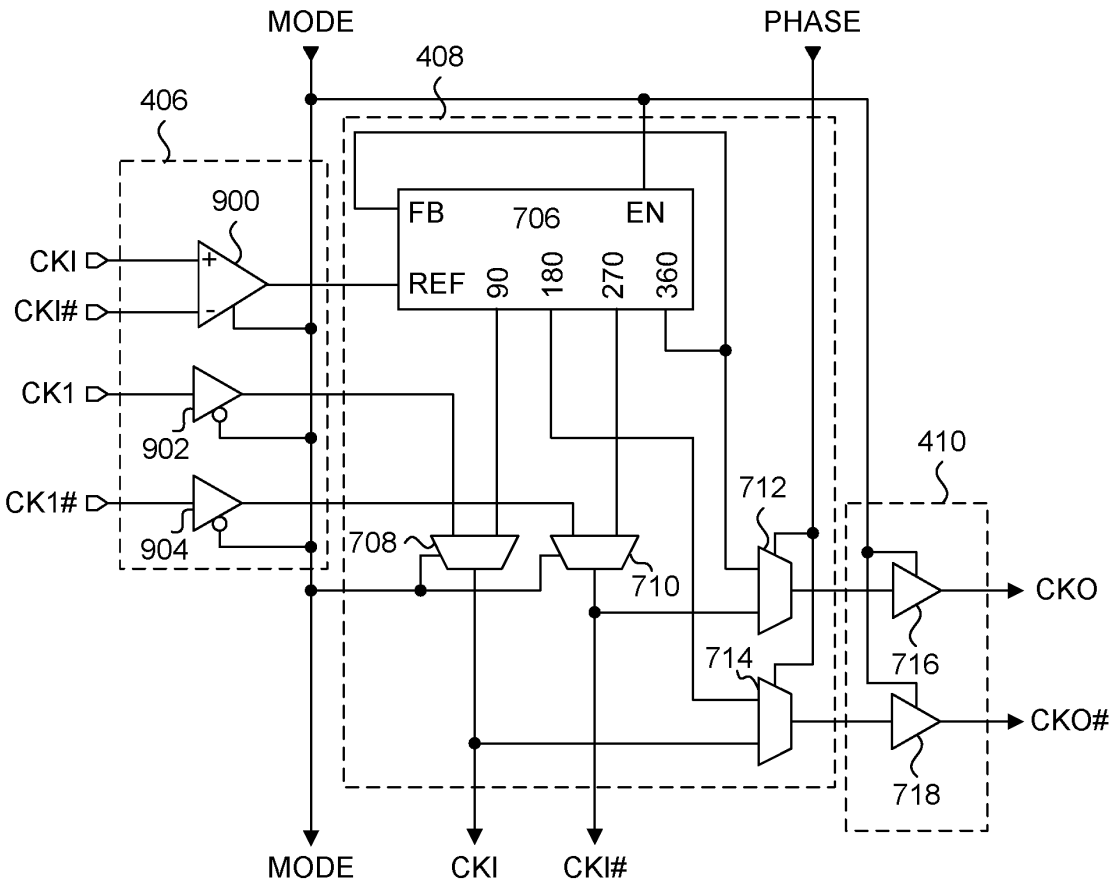

MODE
PHASE
408
406
900
FB
706
EN
CKI
CKI#
REF
90
180
270
360
CK1
902
CK1#
904
410
712
708
710
CKO
714
716
CKO#
718
MODE
CKI
CKI#

Fig. 10

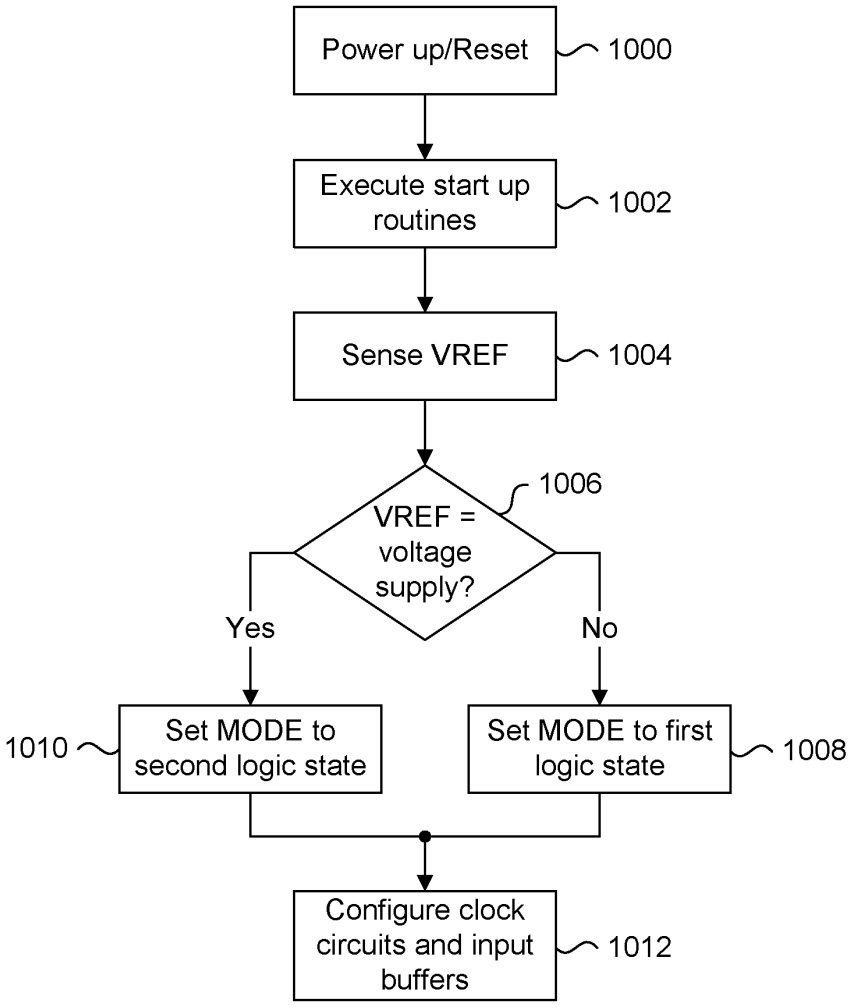

Power up/Reset
1000
Execute start up routines
1002
Sense VREF
1004
VREF = voltage supply?
1006
Yes
No
Set MODE to second logic state
1010
Set MODE to first logic state
1008
Configure clock circuits and input buffers
1012

Fig. 11

Doc code: Oath
Document Description: Oath or declaration filed

PTO/AIA/02 (07-13)
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SUBSTITUTE STATEMENT IN LIEU OF AN OATH OR DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (35 U.S.C. 115(d) AND 37 CFR 1.64)

Title of Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

This statement is directed to:

☐ The attached application,

OR

☒ United States application or PCT international application number 14/491,440 filed on September 19, 2014.

LEGAL NAME of inventor to whom this substitute statement applies:

(*E.g.*, Given Name (first and middle (if any)) and Family Name or Surname)

Graham ALLAN

Residence (except for a deceased or legally incapacitated inventor):

City	State	Country
Stittsville	Ontario	CANADA

Mailing Address (except for a deceased or legally incapacitated inventor):

10 Carberry Drive

City	State	Zip	Country
Stittsville	Ontario	K2S 1E4	CANADA

I believe the above-named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application.

The above-identified application was made or authorized to be made by me.

I hereby acknowledge that any willful false statement made in this statement is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Relationship to the inventor to whom this substitute statement applies:

- ☐ Legal Representative (for deceased or legally incapacitated inventor only),
- ☒ Assignee,
- ☐ Person to whom the inventor is under an obligation to assign,
- ☐ Person who otherwise shows a sufficient proprietary interest in the matter (petition under 37 CFR 1.46 is required), or
- ☐ Joint Inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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SUBSTITUTE STATEMENT

Circumstances permitting execution of this substitute statement:

- ☐ Inventor is deceased,
- ☐ Inventor is under legal incapacity,
- ☐ Inventor cannot be found or reached after diligent effort, or
- ■ Inventor has refused to execute the oath or declaration under 37 CFR 1.63.

If there are joint inventors, please check the appropriate box below:

- ■ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) naming the entire inventive entity has been or is currently submitted.

OR

- ☐ An application data sheet under 37 CFR 1.76 (PTO/AIA/14 or equivalent) has not been submitted. Thus, a Substitute Statement Supplemental Sheet (PTO/AIA/11 or equivalent) naming the entire inventive entity and providing inventor information is attached. See 37 CFR 1.64(b).

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

Name: Phillip Sheer | Date (Optional):

Signature:

APPLICANT NAME AND TITLE OF PERSON EXECUTING THIS SUBSTITUTE STATEMENT:

If the applicant is a juristic entity, list the applicant name and the title of the signer:

Applicant Name: Conversant Intellectual Property Management Inc.

Title of Person Executing This Substitute Statement: Sr. VP, Chief Licensing Officer

The signer, whose title is supplied above, is authorized to act on behalf of the applicant.

Residence of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent):

City Ottawa | State Ontario | Country CANADA

Mailing Address of the signer (unless provided in an application data sheet, PTO/AIA/14 or equivalent)

390 March Road, Suite 100

City Ottawa | State Ontario | Zip K2K 0G7 | Country CANADA

Note: Use an additional PTO/AIA/02 form for each inventor who is deceased, legally incapacitated, cannot be found or reached after diligent effort, or has refused to execute the oath or declaration under 37 CFR 1.63.

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

  filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Peter B. GILLINGHAM Date (Optional): 26 April 2013

Signature: Peter Gillingham

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt	
EFS ID:	32383021
Application Number:	15957120
International Application Number:	
Confirmation Number:	5375
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Customer Number:	108927
Filer:	Shin Hung/Barb MacDonald
Filer Authorized By:	Shin Hung
Attorney Docket Number:	PAT 4418I-2
Receipt Date:	19-APR-2018
Filing Date:	
Time Stamp:	14:02:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	160302 3f8ea9ec627bf2dcf40c725c4a20e574fab6bf8c	no	9

Warnings:

Information:					
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	Specification		1	32	
	Claims		33	34	
	Abstract		35	35	
	Drawings-only black and white line drawings		36	50	
Warnings:					
Information:					
3	Oath or Declaration filed	PAT_4418I_2_ALLAN_Statement_In_lieu_of_Declaration.PDF	255840 dc524c9b6a0e587ed059e038aee4f646d644fb22	no	2
Warnings:					
Information:					
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The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
		Total Files Size (in bytes):	782047		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 108927

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	FEBRUARY 6, 2017
Name	Scott Bell		
Title	SVP, Chief Intellectual Property Officer and General Counsel, Patent Licensing		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt	
EFS ID:	32393460
Application Number:	15957120
International Application Number:	
Confirmation Number:	5375
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Customer Number:	108927
Filer:	Shin Hung/Barb MacDonald
Filer Authorized By:	Shin Hung
Attorney Docket Number:	PAT 4418I-2
Receipt Date:	25-APR-2018
Filing Date:	
Time Stamp:	11:49:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		PAT_4418I_2_Transmittal_and_POA.pdf	249765 8c4f9df7974598cb67791b12c2aef26bb331528d	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Power of Attorney	2	2

Warnings:	
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Information:	
Total Files Size (in bytes):	249765

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
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Application Number	15/957,120
Filing Date	April 19, 2018
First Named Inventor	Peter B. GILLINGHAM
Title	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
Art Unit	
Examiner Name	
Attorney Docket Number	PAT 4418I-2

SIGNATURE of Applicant or Patent Practitioner

Signature	/Shin Hung/	Date (Optional)	
Name	Shin Hung	Registration Number	55497
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: May 4, 2018
Electronic Signature for: /Shin HUNG/

Docket No.: PAT 4418I-2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Peter B. GILLINGHAM et. al.

Application No.: 15/957,120 Confirmation No.: 5375

Filed: April 19, 2018 Art Unit: 2827

Title: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM Examiner: <unknown>

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to MPEP 609.02, Applicant(s) expect the Examiner to consider all the references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet of the present application. The Applicant(s) do not plan to resubmit a listing of those references unless the Examiner explicitly requests.

May 4, 2018

Respectfully submitted,
HakJune OH et al.

/Shin HUNG/
By: _____
Shin HUNG
Reg. No. 55,497
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1300
Ottawa, ON K1P 1J9
CANADA
Tel: (613) 237-5160
Fax: (613) 787-3558
E-mail: ipinfo@blg.com

Electronic Acknowledgement Receipt

EFS ID:	32526543
Application Number:	15957120
International Application Number:	
Confirmation Number:	5375
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Customer Number:	108927
Filer:	Shin Hung/Edgar AGUHAR
Filer Authorized By:	Shin Hung
Attorney Docket Number:	PAT 4418I-2
Receipt Date:	04-MAY-2018
Filing Date:	
Time Stamp:	11:51:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_Letter.pdf	71092 ed791571af1761dc04cb62d5d8558e3a73eb6517	no	1

Warnings:

Information:	
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/957,120

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/957,120	04/19/2018	Peter B. GILLINGHAM	PAT 4418I-2

CONFIRMATION NO. 5375

108927
Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

FORMALITIES LETTER

OC000000099647409

Date Mailed: 05/22/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

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Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/mhaile/

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/957,120	04/19/2018	2827	0.00	PAT 4418I-2	1	1

CONFIRMATION NO. 5375

FILING RECEIPT

108927
Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

OC000000099647408

Date Mailed: 05/22/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Peter B. GILLINGHAM, Ottawa, CANADA;
Graham ALLAN, Stittsville, CANADA;

Applicant(s)

Conversant Intellectual Property Management Inc., Ottawa, CANADA;

Power of Attorney: The patent practitioners associated with Customer Number 108927

Domestic Priority data as claimed by applicant

This application is a CON of 15/655,336 07/20/2017 PAT 9971518
which is a CON of 15/378,650 12/14/2016 PAT 9740407
which is a CON of 15/183,162 06/15/2016 PAT 9552889
which is a CON of 14/720,317 05/22/2015 PAT 9384847
which is a CON of 14/491,440 09/19/2014 PAT 9042199
which is a CON of 14/158,215 01/17/2014 PAT 8854915
which is a CON of 13/871,487 04/26/2013 PAT 8644108
which is a CON of 13/006,005 01/13/2011 PAT 8432767
which is a DIV of 12/032,249 02/15/2008 PAT 7885140
which claims benefit of 60/902,003 02/16/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/18/2018
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/957,120**
Projected Publication Date: To Be Determined - pending completion of Missing Parts
Non-Publication Request: No
Early Publication Request: No
Title

CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	GILLINGHAM, Peter, B.; ALLAN, Graham
Serial No.:	15/957,120
Filed:	February 15, 2008
Title:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
Group:	2827
Examiner:	
Attorney Ref.:	PAT 4418I-2 US

July 20, 2018

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria VA 22314-1450
USA

PRELIMINARY AMENDMENT

Amendments to the Claims begin on page **2** of this document.

Remarks begin on page **5** of this document.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (New) A configurable non-volatile memory device comprising:

plurality of non-volatile memory blocks;

a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;

a first clock input port configured to receive a first clock input signal;

a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;

a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;

one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;

a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-

volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

3. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively.

4. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the first clock input signal and the second clock input signal are data latching clock signals.

5. (New) The configurable non-volatile memory device as claimed in claim 2, wherein each of the one or more common data ports comprises 1 bit.

6. (New) The configurable non-volatile memory device as claimed in claim 2, further comprising one or more configurable data input buffers configured to utilize a reference voltage for determining logic levels of the common data signals.

7. (New) The configurable non-volatile memory device as claimed in claim 6, wherein the reference voltage is set to a predetermined voltage level.

8. (New) The configurable non-volatile memory device as claimed in claim 6, wherein the reference voltage is set to half of the common data signal's high logic level.

9. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the first clock input signal, the second clock input signal and the common data signal are terminated signals.

10. (New) The configurable non-volatile memory device as claimed in claim 9, wherein the first clock input signal, the second clock input signal and the common data signals are SSTL signals.

11. (New) The configurable non-volatile memory device as claimed in claim 2, further comprising a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration.

12. (New) The configurable non-volatile memory device as claimed in claim 2, further comprising a configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers.

13. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the output data is edge aligned with the clock output signal.

14. (New) The configurable non-volatile memory device as claimed in claim 2, further comprising a reset port configured to receive a reset signal for resetting the configurable non-volatile memory device to a default configuration.

15. (New) The configurable non-volatile memory device as claimed in claim 14, wherein the default configuration comprises the single ended signaling configuration.

16. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the configurable non-volatile memory device is a flash memory device.

17. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the configurable non-volatile memory device is a NOR flash memory device.

18. (New) The configurable non-volatile memory device as claimed in claim 2, wherein the configurable non-volatile memory device is a NAND flash memory device.

REMARKS/ARGUMENTS

This continuation application was filed on April 19, 2018. Applicant respectfully requests entry of the above noted amendments.

Entry of this Preliminary Amendment should not be disapproved as it is filed no later than 3 months from the filing date of the application (37 CFR 1.115 (b)(3)(i)).

Applicant notes no Examiner has been assigned to this application as of the date of this submission. Therefore this Preliminary Amendment does not interfere with examination of the application.

Claim 1 has been cancelled and new claims 2 to 18 have been added.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments, to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

/Shin Hung/
By: _____
Shin Hung
Reg. No. 55,497
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1300
Ottawa, ON K1P 1J9
CANADA
Tel:(613) 237-5160
Fax:(613) 787-3558
E-mail: ipinfo@blg.com

Electronic Patent Application Fee Transmittal

Application Number:	15957120
Filing Date:	19-Apr-2018
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Filer:	Shin Hung/Ruth Murphy
Attorney Docket Number:	PAT 4418I-2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1880**

Electronic Acknowledgement Receipt	
EFS ID:	33239538
Application Number:	15957120
International Application Number:	
Confirmation Number:	5375
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Customer Number:	108927
Filer:	Shin Hung/Ruth Murphy
Filer Authorized By:	Shin Hung
Attorney Docket Number:	PAT 4418I-2
Receipt Date:	20-JUL-2018
Filing Date:	19-APR-2018
Time Stamp:	15:02:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1880
RAM confirmation Number	072318INTEFSW00001467501593
Deposit Account	501593
Authorized User	Shin Hung
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	PAT_4418I-2_Letter_to_USPTO_-_Response_to_Missing_Parts.pdf	61754 203ce816cc95cb68e7871643c69ffc4d235b3f8a	no	1
Warnings:					
Information:					
2		PAT_4418I-2_Letter_to_USPTO_-_Preliminary_Amendment.pdf	76657 8abcfd9f561b9655c2ea42c43ca1766d6df7d995	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	36971 4ff52eb8a28958935e5c65e907fdd5b801f2a659	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	175382		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	GILLINGHAM, Peter, B.; ALLAN, Graham
Serial No.:	15/957,120
Filed:	February 15, 2008
Title:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
Group:	2827
Examiner:	<unknown>
Attorney Ref.:	PAT 4418I-2 US

July 20, 2018

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria VA 22314-1450
USA

RESPONSE TO NOTICE TO FILE MISSING PARTS

In response to the Notice to File Missing Parts dated May 22, 2018, for which a response is due by **July 22, 2018**, Applicant submits the outstanding basic filing, search and examination fees, along with a late payment surcharge fee, in compliance with 37 CFR 1.16(f).

The Applicant has also concurrently submitted a Preliminary Amendment.

The Commissioner is hereby authorized to debit $1880.00 from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP. The Commissioner is hereby authorized to charge any additional fees, and credit any over payments, to Deposit Account No. 501593.

Respectfully submitted,

/Shin Hung/

Shin Hung
Reg. No. 55,497
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1300
Ottawa, ON K1P 1J9
CANADA
Tel:(613) 237-5160
Fax:(613) 787-3558
E-mail: ipinfo@blg.com

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/957,120

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/957,120	04/19/2018	2827	1880	PAT 4418I-2	1	1

CONFIRMATION NO. 5375

UPDATED FILING RECEIPT

108927
Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

OC000000101182873

Date Mailed: 07/26/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Peter B. GILLINGHAM, Ottawa, CANADA;
Graham ALLAN, Stittsville, CANADA;

Applicant(s)

Conversant Intellectual Property Management Inc., Ottawa, CANADA;

Power of Attorney: The patent practitioners associated with Customer Number 108927

Domestic Priority data as claimed by applicant

This application is a CON of 15/655,336 07/20/2017 PAT 9971518
which is a CON of 15/378,650 12/14/2016 PAT 9740407
which is a CON of 15/183,162 06/15/2016 PAT 9552889
which is a CON of 14/720,317 05/22/2015 PAT 9384847
which is a CON of 14/491,440 09/19/2014 PAT 9042199
which is a CON of 14/158,215 01/17/2014 PAT 8854915
which is a CON of 13/871,487 04/26/2013 PAT 8644108
which is a CON of 13/006,005 01/13/2011 PAT 8432767
which is a DIV of 12/032,249 02/15/2008 PAT 7885140
which claims benefit of 60/902,003 02/16/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/18/2018
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/957,120**
Projected Publication Date: 11/01/2018
Non-Publication Request: No
Early Publication Request: No
Title

CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

108927 7590 10/01/2018

Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

EXAMINER	
LE, VU ANH	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/01/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/957,120	04/19/2018	Peter B. GILLINGHAM	PAT 4418I-2	5375

TITLE OF INVENTION: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	01/02/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

108927 7590 10/01/2018
Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/957,120	04/19/2018	Peter B. GILLINGHAM	PAT 4418I-2	5375

TITLE OF INVENTION: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	01/02/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, VU ANH	2825	365-233100

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/957,120	04/19/2018	Peter B. GILLINGHAM	PAT 4418I-2	5375

108927 7590 10/01/2018

Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/01/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/957,120	Applicant(s) GILLINGHAM ET AL.	
	Examiner VU LE	Art Unit 2825	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/20/2018*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *2-18*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/04/2018
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/VU LE/
Primary Examiner, Art Unit 2825

The present application is being examined under the pre-AIA first to invent provisions.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: the present invention relates to clock mode determination in a memory system. The independent claim 2 recites a configurable non-volatile memory device comprising: plurality of non-volatile memory blocks; a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device; a first clock input port configured to receive a first clock input signal; a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal; a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal; one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks; a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second

clock input signal as a single ended signal; and one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

The prior art fails to disclose or suggest “a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration” as recited in the independent claim 2. Therefore, claims 2-18 are in condition for allowance.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Any inquiry concerning this communication or earlier communications from the examiner should be directed to VU LE whose telephone number is (571)272-1871. The examiner can normally be reached on Monday to Friday.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ALEXANDER SOFOCLEOUS can be reached on (571)272-0635. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VU LE/
Primary Examiner, Art Unit 2825

09/04/2018

Notice of References Cited	Application/Control No. 15/957,120	Applicant(s)/Patent Under Reexamination GILLINGHAM ET AL.	
	Examiner VU LE	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-5,880,998 A	03-1999	Tanimura; Masaaki	G11C7/1072	365/189.05
*	B	US-6,636,110 B1	10-2003	Ooishi; Tsukasa	G06F1/10	327/295
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"9971518".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:22
L2	5	"9740407".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:24
L3	2	"9552889".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:24
L4	2	"9384847".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:25
L5	2	"9042199".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:26
L6	2	"8854915".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:26
L7	2	"8644108".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:26
L8	4	"8432767".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/03 21:27

9/3/2018 9:28:13 PM
C:\Users\vle1\Documents\EAST\Workspaces\~auto.11122017.194632.wsp

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4).

Dated: May 4, 2018
Electronic Signature for: /Shin HUNG/

Docket No.: PAT 4418I-2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Peter B. GILLINGHAM et. al.

Application No.: 15/957,120 Confirmation No.: 5375

Filed: April 19, 2018 Art Unit: 2827

Title: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM Examiner: <unknown>

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to MPEP 609.02, Applicant(s) expect the Examiner to consider all the references submitted, cited, or otherwise considered during the prosecution of all the ancestor applications listed on the application data sheet of the present application. The Applicant(s) do not plan to resubmit a listing of those references unless the Examiner explicitly requests.

May 4, 2018

Respectfully submitted,
HakJune OH et al.

/Shin HUNG/
By: _____
Shin HUNG
Reg. No. 55,497
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1300
Ottawa, ON K1P 1J9
CANADA
Tel: (613) 237-5160
Fax: (613) 787-3558
E-mail: ipinfo@blg.com

/VU A LE/

09/04/2018

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.A.L/

Bibliographic Data

Application No: 15/957,120

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /VU A LE/ Examiner's Signature | Initials

Title: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/19/2018	365	2825	PAT 4418I-2
RULE			

APPLICANTS

Conversant Intellectual Property Management Inc., Ottawa, CANADA

INVENTORS

Peter B. GILLINGHAM Ottawa, CANADA

Graham ALLAN Stittsville, CANADA

CONTINUING DATA

This application is a CON of 15655336 07/20/2017 PAT 9971518

15655336 is a CON of 15378650 12/14/2016 PAT 9740407

15378650 is a CON of 15183162 06/15/2016 PAT 9552889

15183162 is a CON of 14720317 05/22/2015 PAT 9384847

14720317 is a CON of 14491440 09/19/2014 PAT 9042199

14491440 is a CON of 14158215 01/17/2014 PAT 8854915

14158215 is a CON of 13871487 04/26/2013 PAT 8644108

13871487 is a CON of 13006005 01/13/2011 PAT 8432767

13006005 is a DIV of 12032249 02/15/2008 PAT 7885140

12032249 has PRO of 60902003 02/16/2007

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/18/2018

STATE OR COUNTRY

CANADA

ADDRESS

Borden Ladner Gervais LLP (BLG/Conversant - 8021)

1300-100 Queen Street

Ottawa, ON K19 1J9
CANADA

FILING FEE RECEIVED

$1,880

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	(clock adj input adj buffer) and (common adj data adj port)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/04 09:07
L2	35	(clock adj input adj buffer) and (clock adj mode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/04 09:42
L3	1	"20050140416".PN.	US-PGPUB	OR	OFF	2018/09/04 10:11
L4	1	"7391246".PN.	USPAT; USOCR	OR	OFF	2018/09/04 10:29
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L8	24	(differential near signal$3) and (clock adj mode) and synchroniz$3 and (double same rate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/09/04 10:34
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L10	1	"6259288".PN.	USPAT; USOCR	OR	OFF	2018/09/04 10:36

9/4/2018 10:39:39 AM
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15957120	GILLINGHAM ET AL.
	Examiner	**Art Unit**
	VU LE	2825

CPC						
Symbol					**Type**	**Version**
G06F		3	/	061	F	2013-01-01
G11C		7	/	22	I	2013-01-01
H03K		2005	/	00247	A	2013-01-01
G11C		7	/	1078	I	2013-01-01
G11C		7	/	1045	I	2013-01-01
G11C		14	/	0018	I	2013-01-01
Y02D		10	/	14	A	2018-01-01
G06F		13	/	1694	I	2013-01-01
G06F		3	/	0688	I	2013-01-01
G06F		3	/	0655	I	2013-01-01
G11C		16	/	0483	I	2013-01-01
G11C		16	/	32	I	2013-01-01
G11C		16	/	28	I	2013-01-01
G11C		16	/	10	I	2013-01-01
G11C		7	/	1093	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 17	
/VU LE/ Primary Examiner.Art Unit 2825 (Primary Examiner)	09/04/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

U.S. Patent and Trademark Office

Part of Paper No. 20180904

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15957120	GILLINGHAM ET AL.
	Examiner	Art Unit
	VU LE	2825

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
365	230.08	G	1	1	C	8 / 00 (2006.0)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											
365	233.1											

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 17	
/VU LE/ Primary Examiner.Art Unit 2825 (Primary Examiner)	09/04/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15957120	GILLINGHAM ET AL.
	Examiner	**Art Unit**
	VU LE	2825

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 17	
/VU LE/ Primary Examiner.Art Unit 2825 (Primary Examiner)	09/04/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5

U.S. Patent and Trademark Office Part of Paper No. 20180904

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15957120	GILLINGHAM ET AL.
	Examiner	Art Unit
	VU LE	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/04/2018								
	1	-								
	2	=								
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	4	=								
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	16	=								
	17	=								
	18	=								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15957120	GILLINGHAM ET AL.
	Examiner	Art Unit
	VU LE	2825

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 3/061, G06F 3/0655, G06F 3/0688, G06F 13,1694	09/04/2018	VL

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	230.08, 233.1, 233.5	09/04/2018	VL

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
East	09/04/2018	VL
Inventorship search	09/04/2018	VL

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
365	230.08, 233.1	09/04/2018	VL

Doc Code: MFEE.C.AD PTO/SB/47-EFS

Document Description: Maintenance Fee Address Change

FEE ADDRESS INDICATION FORM			
Application Number	15957120	Art Unit	2825
Filing Date	19-Apr-2018	Examiner Name	VU LE
First Name Inventor	Peter GILLINGHAM	Attorney Doc. Number	PAT 4418I-2

INSTRUCTIONS: In order for the fee address identified on this form to be effective, the issue fee must have been paid for the application listed on this form. Only an address represented by a customer number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. For more information on customer numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

Please recognize as the Fee Address under the provisions of 37 CFR 1.363 the address associated with:

Customer Number:	68256 Conversant Intellectual Property Management Inc. 5601 Granite Parkway Suite 1300 Plano TX 75024 UNITED STATES 214-494-4800 ipadmin@conversantip.com

Signature :

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application.

Signature	/Jeffrey J. Coghlan/	**Date**	10-24-2018
Name	Jeffrey J. Coghlan	**Registration Number**	73451

Electronic Patent Application Fee Transmittal

Application Number:	15957120
Filing Date:	19-Apr-2018
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Filer:	Jeffrey J. Coghlan/Trisha Williams
Attorney Docket Number:	PAT 4418I-2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	34092704
Application Number:	15957120
International Application Number:	
Confirmation Number:	5375
Title of Invention:	CLOCK MODE DETERMINATION IN A MEMORY SYSTEM
First Named Inventor/Applicant Name:	Peter B. GILLINGHAM
Customer Number:	108927
Filer:	Jeffrey J. Coghlan/Trisha Williams
Filer Authorized By:	Jeffrey J. Coghlan
Attorney Docket Number:	PAT 4418I-2
Receipt Date:	24-OCT-2018
Filing Date:	19-APR-2018
Time Stamp:	15:55:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	102518INTEFSW00002610501593
Deposit Account	501593
Authorized User	Jeffrey Coghlan
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46117 8b6bb37f254d4bce8b779af0a583e47d00ac00c1	no	2
Warnings:					
Information:					
2	Maintenance Fee Address Change	web85feeaddress.pdf	32862 c3d02757c8752baef971aca9b160e5bca05cbb41	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31989 b98d0cdfe153739f79a26eea4141c41853962719	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	110968		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
15957120	19-Apr-2018	Peter GILLINGHAM	PAT 4418I-2	5375

TITLE OF INVENTION :

CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2825	233100	VU LE

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1000	$0	$1000	02-Jan-2019	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
108927 Borden Ladner Gervais LLP (BLG/Conversant - 8021) 1300-100 Queen Street Ottawa ON K19 1J9 CANADA 6132375160 ipinfo@blg.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☒ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency, or credit any overpayment, to Deposit Account Number 501593 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. BORDEN LADNER GERVAIS LLP
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Conversant Intellectual Property Management Inc.	Ottawa		canada	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Jeffrey J. Coghlan/	**Date**	10-24-2018
Name	Jeffrey J. Coghlan	**Registration Number**	73451

WEB IFEE 1.0

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/957,120	04/19/2018	Peter B. GILLINGHAM	PAT 4418I-2

CONFIRMATION NO. 5375

108927
Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ON K19 1J9
CANADA

PUBLICATION NOTICE

OC000000103526602

Title:CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

Publication No.US-2018-0314424-A1
Publication Date:11/01/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/957,120	11/27/2018	10140028	PAT 4418I-2	5375

108927 7590 11/07/2018

Borden Ladner Gervais LLP (BLG/Conversant - 8021)
1300-100 Queen Street
Ottawa, ONTARIO K19 1J9
CANADA

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Peter B. GILLINGHAM, Ottawa, CANADA;
Conversant Intellectual Property Management Inc., Ottawa, CANADA;
Graham ALLAN, Stittsville, CANADA;

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
15/957,120	10140028	2825	96827

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 68256 on 10/01/2019 via Private PAIR in view of the certification copied below that authorized the change.

- Correspondence Address

The address for Customer Number 68256 is:
68256
Conversant Intellectual Property Management Corp
5830 Granite Parkway #100-247
Suite 247
Plano, TX 75024

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/Rodney M Anderson/
Name:	Rodney M. Anderson
Registration Number:	66487

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APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	REQUEST ID
15/957,120	10140028	2825	96827

PAIR Correspondence Address/Fee Address Change

The following fields have been changed to Customer Number 68256 on 10/01/2019 via Private PAIR in view of the certification copied below that authorized the change.

- Maintenance Fee Address

The address for Customer Number 68256 is:
68256
Conversant Intellectual Property Management Corp
5830 Granite Parkway #100-247
Suite 247
Plano, TX 75024

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

An attorney or Agent of Record registered to practice before the Patent and Trademark Office who has been given power of attorney in this application

Signature:	/Rodney M Anderson/
Name:	Rodney M. Anderson
Registration Number:	66487