

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Peter B. Gillingham et al.
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Issue Date: November 27, 2018
Appl. Serial No.: 15/957,120
Filing Date: April 19, 2018
Title: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 10,140,028 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

EX1001	U.S. Patent No. 10,140,028 to Gillingham (“the ’028 Patent”)
EX1002	Excerpts from the Prosecution History of the ’028 Patent (“the Prosecution History”)
EX1003	Expert Declaration and Curriculum Vitae of Carl Sechen, Ph.D.
EX1004	U.S. Publication No. 2006/0023499 (“Ryu”)
EX1005	U.S. Publication No. 2005/0141666 (“Cole”)
EX1006	U.S. Patent No. 5,864,506 (“Arcoleo”)
EX1007	U.S. Patent No. 6,337,832 (“Ooishi”)
EX1008	U.S. Patent No. 5,917,759 (“Akashi”)
EX1009	U.S. Publication No. 2004/0148482 (“Grundy”)
EX1010	U.S. Patent No. 5,206,831 (“Wakamatsu”)
EX1011	U.S. Patent No. 6,304,497 (“Roohparvar”)
EX1012	Wu, <i>eNVy: A Non-Volatile, Main Memory Storage System</i> (1994), available at https://dl.acm.org/doi/pdf/10.1145/381792.195506
EX1013	U.S. Patent No. 6,026,465 (“Mills”)
EX1014	U.S. Patent No. 4,970,694 (“Tanaka”)
EX1015	Maksimovic, <i>Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply</i> (2000), available at https://www.acsel-lab.com/Publications/Papers/102-IEEE-TVLSI-CAL.pdf

- EX1016 U.S. Patent No. 6,943,604 (“Minzoni”)
- EX1017 U.S. Patent No. 6,972,993 (“Conley”)
- EX1018 Lee, *Low-Energy Heterogeneous Non-Volatile Memory Systems for Mobile Systems* (2005), available at <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e1f287fa9e15bd88cb14574c4802fd7a6017c449>
- EX1019 Crisp, *Direct Rambus Technology: The New Main Memory Standard* (1997), available at <https://www.ardent-tool.com/CPU/docs/AMD/anatomy/misc/articles/m6crisp.pdf>
- EX1020 U.S. Patent No. 7,486,104 (“Oh”)
- EX1021 U.S. Patent No. 6,937,513 (“Desai”)
- EX1022 U.S. Patent No. 7,177,190 (“Lee”)
- EX1023 Yeh, *Flash Memory Built-In Self-Test Using March-Like Algorithms* (2002), available at https://www.researchgate.net/profile/Jen-Chieh-Yeh-2/publication/3943092_Flash_memory_built-in_self-test_using_March-like_algorithms/links/0c9605187311b4193a000000/Flash-memory-built-in-self-test-using-March-like-algorithms.pdf
- EX1024 U.S. Patent No. 7,804,176 (“Hanawa”)
- EX1025 U.S. Patent No. 8,085,574 (“Kang”)
- EX1026 U.S. Publication No. 2008/0016306 (“Min”)
- EX1027 Palanisamy, *Interfacing Spartan—3 Devices with 166 MHz or 3333 Mb/s DDR SRAM Memories* (2004), available at https://my.eng.utah.edu/~cs3710/xilinx-docs/examples/s3e_starter_revD_mig_ddr/docs/XAPP768c.pdf

EX1028	U.S. Patent No. 6,442,644 (“Gustavson”)
EX1029	U.S. Patent No. 6,560,669 (“Ryan”)
EX1030	U.S. Patent No. 6,240,040 (“Akaogi”)
EX1031	Pon, <i>Technology Scaling Impact on NOR and NAND Flash Memories and Their Applications</i> (2006), available at https://web.archive.org/web/20080225091210id_/http://www.pentium.pt/design/flcomp/papers/tech_scaling.pdf
EX1032	U.S. Patent No. 7,499,323 (“Park”)
EX1033	U.S. Patent No. 6,178,518 (“Toda”)
EX1034	U.S. Patent No. 6,272,064 (“Wilford”)
EX1035	U.S. Patent No. 6,286,077 (“Choi”)
EX1036-1099	RESERVED
EX1100	Complaint, <i>Mosaid Techs. Inc. v. Infineon Techs. AG et al.</i> , 1-25-cv-00436 (W.D. Tex.) (Mar. 25, 2025)
EX1101	Mosaid Technologies Inc.’s Preliminary Infringement Contentions, Exhibit 028-A <i>MOSAID Technologies, Inc. v. Infineon Technologies AG, et al.</i> , 1-25-cv-00436 (W.D. Tex.) (Jun. 20, 2025)
EX1102	Mosaid Technologies Inc.’s Preliminary Infringement Contentions, Exhibit 028-B <i>MOSAID Technologies, Inc. v. Infineon Technologies AG, et al.</i> , 1-25-cv-00436 (W.D. Tex.) (Jun. 20, 2025)

LIST OF CHALLENGED CLAIM ELEMENTS

Claim 1	
[1pre]	A configurable non-volatile memory device comprising:
[1a]	plurality of non-volatile memory blocks;
[1b]	a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;
[1c]	a first clock input port configured to receive a first clock input signal; a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;
[1d]	a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;
[1e]	one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;
[1f]	a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and
[1g]	one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

Claim 2	
[2]	The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively.
Claim 3	
[3]	The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal and the second clock input signal are data latching clock signals.
Claim 4	
[4]	The configurable non-volatile memory device as claimed in claim 1, wherein each of the one or more common data ports comprises 1 bit.
Claim 5	
[5]	The configurable non-volatile memory device as claimed in claim 1, further comprising one or more configurable data input buffers configured to utilize a reference voltage for determining logic levels of the common data signals.
Claim 6	
[6]	The configurable non-volatile memory device as claimed in claim 5, wherein the reference voltage is set to a predetermined voltage level.
Claim 7	
[7]	The configurable non-volatile memory device as claimed in claim 5, wherein the reference voltage is set to half of the common data signal's high logic level.
Claim 8	
[8]	The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal, the second clock input signal and the common data signal are terminated signals.

Claim 9	
[9]	The configurable non-volatile memory device as claimed in claim 8, wherein the first clock input signal, the second clock input signal and the common data signals are SSTL signals.
Claim 10	
[10]	The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration.
Claim 11	
[11]	The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers.
Claim 12	
[12]	The configurable non-volatile memory device as claimed in claim 1, wherein the output data is edge aligned with the clock output signal.
Claim 13	
[13]	The configurable non-volatile memory device as claimed in claim 1, further comprising a reset port configured to receive a reset signal for resetting the configurable non-volatile memory device to a default configuration.
Claim 14	
[14]	The configurable non-volatile memory device as claimed in claim 13, wherein the default configuration comprises the single ended signaling configuration.
Claim 15	
[15]	The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a flash memory device.

Claim 16	
[16]	The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NOR flash memory device.
Claim 17	
[17]	The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NAND flash memory device.

Infineon Technologies Americas Corp. (“Infineon” or “Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-17 (“the Challenged Claims”) of U.S. Patent No. 10,140,028 (“the ’028 Patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’028 Patent is available for IPR. This Petition is being filed within one year of service of a complaint against Infineon. *See* EX1100. Infineon is not barred or estopped from requesting review of the Challenged Claims on the grounds identified below.

B. Challenge and Relief Requested

Infineon requests institution of IPR and cancellation of the Challenged Claims based on the following grounds:

<u>Ground</u>	<u>Claims</u>	<u>Basis</u>
1A	1-4, 10-17	§103 – Obvious based on Ryu (EX1004) in view of Cole (EX1005) and Arcoleo (EX1006)
1B	1-4, 10-17	§103 – Obvious based on Ryu, in view of Cole, Grundy (EX1009), and Arcoleo,
1C	5-9	§103 – Obvious based on Ryu in view of Cole, Arcoleo, and Akashi (EX1008)
1D	5-9	§103 – Obvious based on Ryu in view of Cole, Grundy, Arcoleo, and Akashi

Grounds 1A-1D are further supported by the expert declaration of Dr. Carl Sechen, Ph.D. (EX1003) and additional evidence cited throughout this Petition and Dr. Sechen's declaration. *See* EX1001-EX1035 and EX1100-EX1102.

The '028 Patent issued from a continuation application filed on April 19, 2018 and claims priority through a chain of intervening applications to U.S. Provisional Application No. 60/902,003, filed on February 16, 2007. Petitioner does not concede that the '028 Patent is entitled to the benefit of the filing date of any of the alleged priority applications. Nonetheless, for purposes of the analysis herein, Petitioner treats February 16, 2007 as the date of the alleged invention of ("Critical Date") of the Challenged Claims. Grounds 1A-1D are each based on prior art patents or printed publications that published more than one year before the Critical Date:¹

<u>Reference</u>	<u>Pre-AIA Prior Art Status</u>
Ryu	pre-AIA §102(b) – Published on Feb. 2, 2006
Cole	pre-AIA §102(b) – Published on Jun. 30, 2005
Grundy	pre-AIA §102(b) – Published on Jul. 9, 2004
Arcoleo	pre-AIA §102(b) – Patented on Jan. 26, 1999
Akashi	pre-AIA §102(b) – Patented on Jun. 29, 1999

¹ Each of Ryu, Cole, Grundy, Arcoleo, and Akashi, further qualify as prior art under pre-AIA 35 U.S.C. §§102(a) and 102(e).

II. SUMMARY OF THE '028 PATENT

A. Brief Description

The '028 Patent describes a memory system comprising a memory controller and a set of non-volatile memory devices arranged in a series configuration.

EX1001, 1:37-2:57, 3:37-6:30, 9:3-12:49, FIG. 3A, FIG. 3C; EX1003, ¶36. Each non-volatile memory device receives, among other inputs, a chip enable signal CE#, complementary clock signals CK and CK#, and a data input Dn. EX1001, 2:37-5:58, 9:3-10:41, 11:19-12:49, FIG. 3A, FIG. 3C. The '028 Patent explains that an example non-volatile memory device can include one or more memory banks, and control circuitry for managing data stored in the memory banks.

EX1001, 12:50-13:49, FIG. 4.

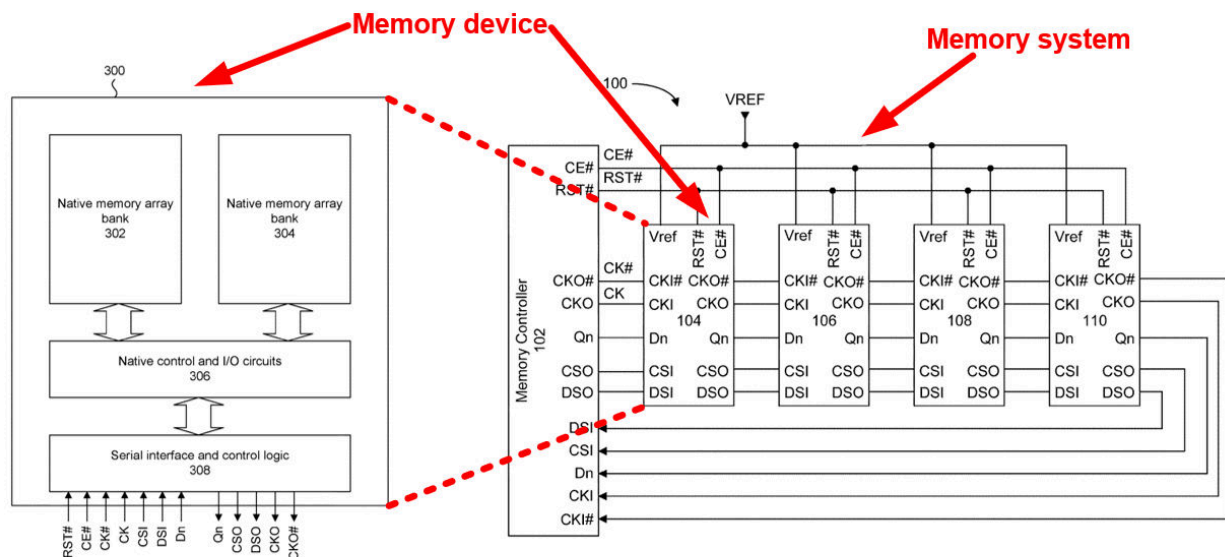
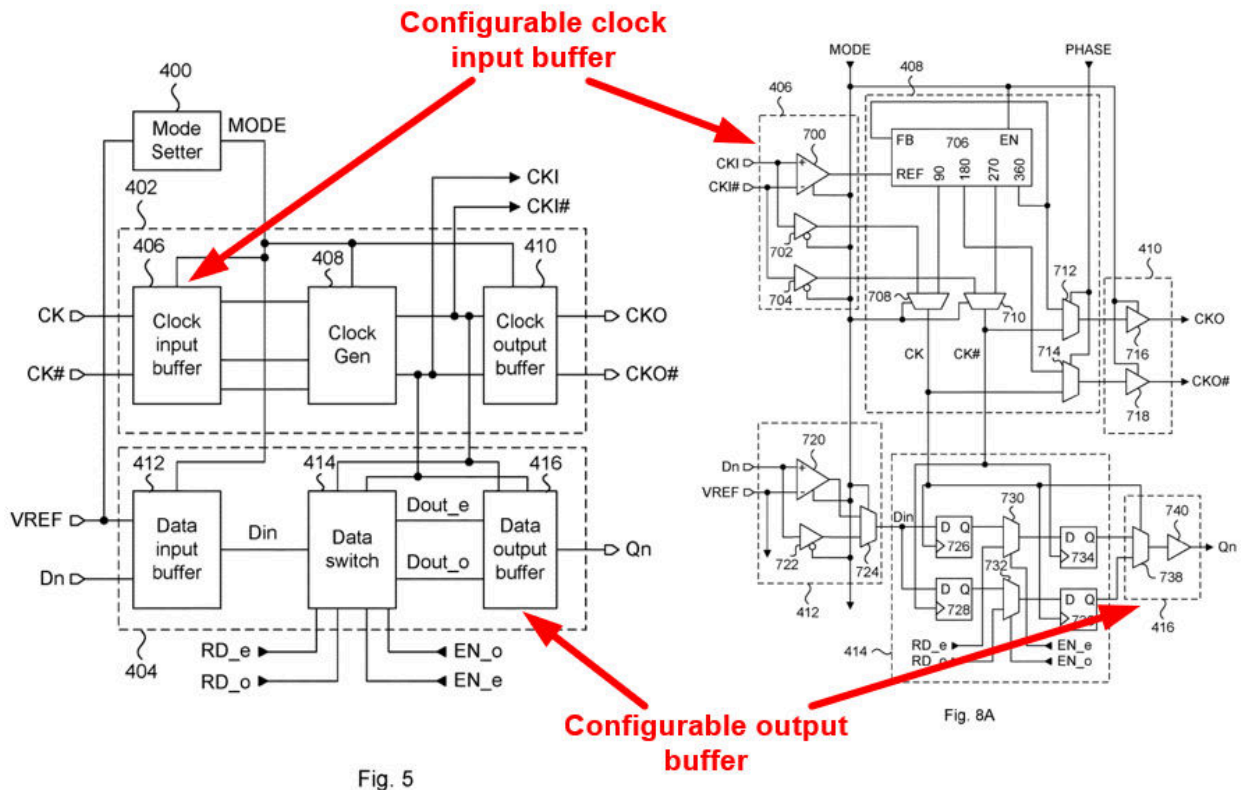


Fig. 4

Fig. 3A

EX1001, FIG. 4, FIG. 3A (annotated).

As noted above, the non-volatile memory device includes a clock input buffer that receives complementary clock input signals CK and CK#. EX1001, 4:46-5:5, 14:41-63, 17:32-51, FIG. 5, FIG. 8A; EX1003, ¶37. The clock input buffer is configurable based on a mode signal (MODE) that indicates either of two logic states. EX1001, 4:1-25, 4:46-5:5, 14:25-63, 15:38-62, 17:32-51, 18:26-51, 22:36-56, FIG. 5, FIG. 8A. When the MODE signal indicates one logic state, the clock input buffer is configured to generate “a single ended clock signal based on [the] two differential clock inputs CK and CK#.” *Id.*, 14:41-49. When the MODE signal indicates the other logic state, the clock input buffer is configured to generate “separate buffered versions of CK and CK#.” *Id.*



EX1001, FIG. 5, FIG. 8A (annotated).

The '028 Patent explains that the “clock mode configuration circuit ... is provided for allowing the configurable memory device to be used in both a parallel clocked memory system and a serially clocked memory system.” EX1001, 8:31-9:3. Noticeably, however, the claims of the '028 Patent do not describe the use of parallel and serial clock signal modes. The claims instead refer to the clock input buffer as being configurable “to one of a *single ended signaling configuration* and a *differential signaling configuration*”—i.e., terms that appear nowhere in the specification of the '028 Patent. EX1001, 23:26-61. Nonetheless, as described

below (*infra*, §V), clock input buffers that achieved the claimed configurability were well known before the Critical Date. EX1003, ¶38.

The disclosed non-volatile memory device also includes an input buffer (e.g., data input buffer 412) and output buffer (e.g., data output buffer 416) that are connected to one or more common data lines. EX1001, 5:26-40, 14:64-15:18, 19:4-67, FIG. 5, FIG. 8A. A drive strength of the output buffer is configurable. EX1001, 19:56-67. A clock output buffer of the non-volatile memory device provides a clock output signal synchronized in a double data rate configuration with output data produced at the output buffer. EX1001, 4:46-5:5, 14:41-63, 18:26-51, 20:47-21:37, FIGs. 5, 8A-8B; EX1003, ¶39. According to the '028 Patent, the configurable output buffer can “optimize performance and power in the multi-drop bus and point-to-point ring topologies.” EX1001, 19:56-67.

B. Prosecution History

The Examiner issued no prior art rejections before allowing the application that issued as the '028 Patent. *See generally*, EX1002. In the reasons for allowance, the Examiner stated that “[t]he prior art fails to disclose or suggest ‘a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration...” and “one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths.” EX1002, 102. Despite the Examiner’s assertions, however, the features of a

“configurable clock input buffer” and “one or more configurable output buffers” as claimed were well-known in the art as demonstrated by references like Cole and Arcoleo. *Infra*, §V; EX1003, ¶40. The file history contains no indication that the Examiner had ever considered these references or the prior art combinations advanced in Grounds 1A-1D of this Petition before the application that issued as the '028 Patent was allowed. *See generally*, EX1002.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the Critical Date of the '028 Patent (“POSITA”) would have had a bachelor of science degree in electrical engineering, computer engineering, or a related field, and three years of experience in the research, design, or development of electronic memory circuits. Additional education could substitute for experience and vice versa. EX1003, ¶¶29-34.

IV. CLAIM CONSTRUCTION

Claim terms in an IPR are generally given their ordinary and customary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Considering the noticeable overlap between the preferred embodiments of the '028 Patent and the prior art/predictable combinations articulated in Grounds 1A-1D, Petitioner submits that no claim terms presently require a formal construction for purposes of addressing the grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Google Inc. v.*

Intellectual Ventures II LLC, 701 Fed. Appx. 946, 956 (Fed. Cir. 2017) (“do not require construction” for purposes of “resolv[ing] the parties’ patentability arguments”); EX1003, ¶35.

This Petition maps the prior art based on two interpretations of “clock” signal. The first interpretation, applied in Ground 1A, is based on Patent Owner’s infringement theories in district court and treats a “clock” signal as encompassing discontinuous “strobe” timing signals. EX1100, 52-53; EX1101, 21-28; EX1102, 17-21; EX1003, ¶36. However, the term “clock” signal is distinguished from a “strobe” signal, and Ground 1B applies this understanding that a clock and a strobe are not the same. *Infra*, Footnote 3.

V. THE CHALLENGED CLAIMS ARE UNPATENTABLE

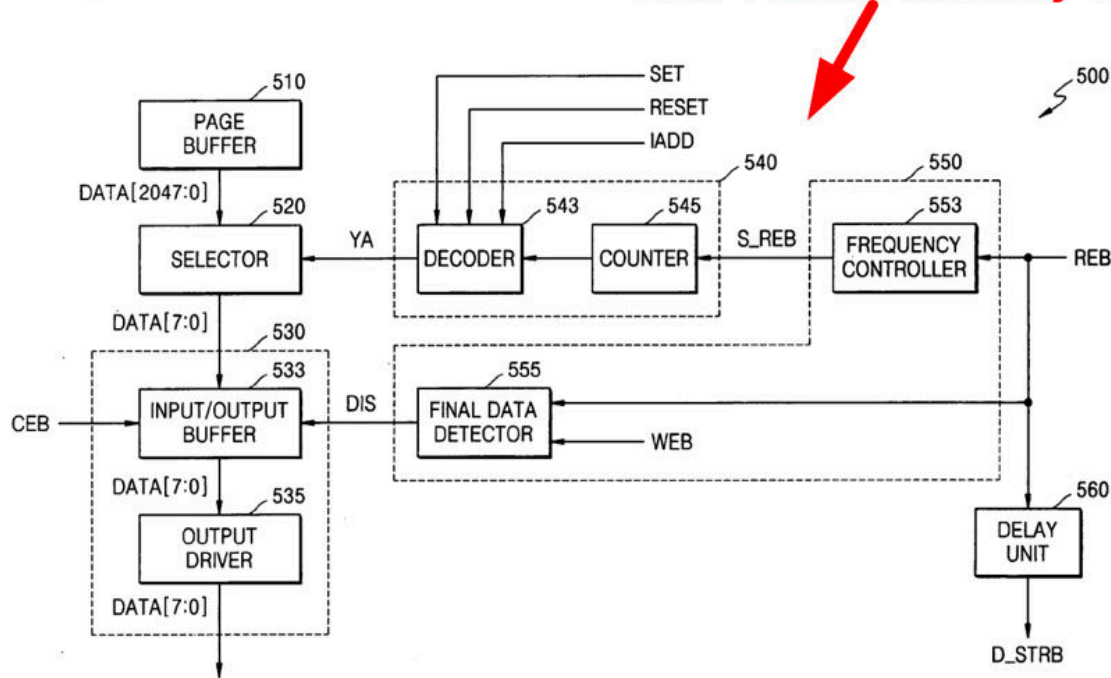
A. GROUND 1A: Obviousness Based on Ryu-Cole-Arcoleo (Claims 1-4 and 10-17)

1. Ryu

Ryu describes a “non-volatile memory device” that “receive[s] or output[s] data through an input/output pin...when reading or writing data.” EX1004, [0003], *see also id.*, [0005], [0041]-[0043], [0059], [0060], [0076], FIG. 5, FIG. 11; EX1003, ¶41. The non-volatile memory device includes “a non-volatile memory array” that stores data, a “page buffer” that receives a portion of this data, and a “selector” that selects data for sending to an “output unit” based on address data. EX1004, [0041]-[0043], [0058]-[0060], [0076]-[0078], FIG. 5, FIG. 11. The output

unit includes an input/output buffer that controls the input and output of data from the non-volatile memory device based on an enable signal (CEB) and a disable signal (DIS). EX1004, [0043], [0059]-[0061], [0063], [0078], FIG. 5, FIG. 11.

FIG. 5 **Non-volatile memory device**



EX1004, FIG. 5 (annotated).

Ryu explains that the non-volatile memory device includes a “system clock” and that the device receives a read control signal (REB) and a write control signal (WEB) for controlling read and write operations of the device. EX1004, [0003]-[0008], [0045], [0047]-[0049] [0051], [0061]-[0064], [0066]-[0070], FIG. 5, FIG. 7. The non-volatile memory device includes a “delay unit” that generates a D_STRB signal for output from the device, the D_STRB signal indicating a timing of the data output from the input/output pin of the device. EX1004, [0064], [0067]-

[0068], [0092], [0095], FIGs. 5, 7, 11, 12; EX1003, ¶42. The D_STRB signal is synchronized with the data output in a double data rate configuration. *Id.*

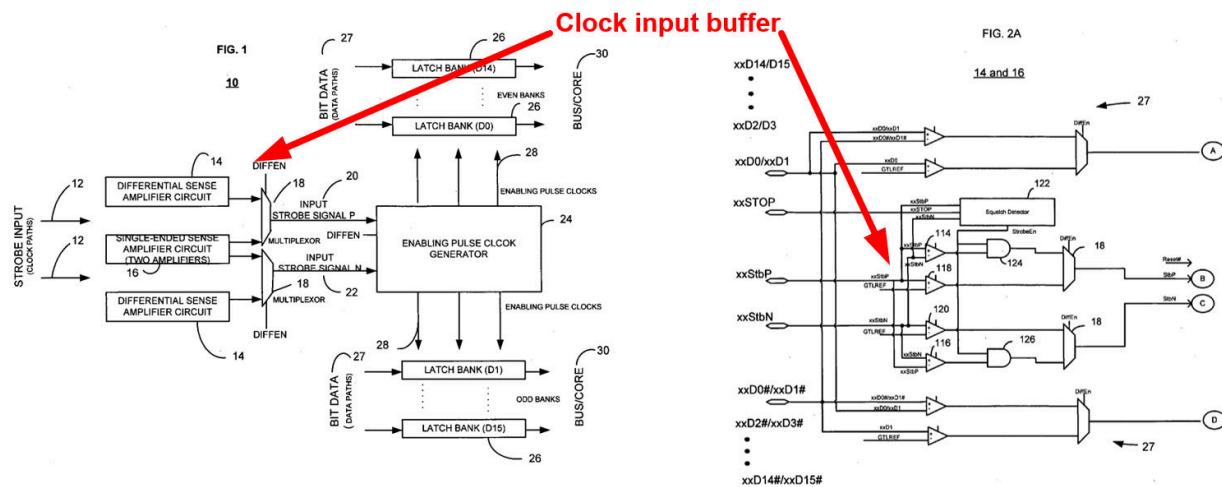
2. Cole

Cole describes “a micro-architecture for an input section of an integrated circuit (IC)[] ... that may be configured to support either differential or single-ended signaling mode of source synchronous data transfer/signaling. EX1005, [0013]; EX1003, ¶43. According to Cole, “there are at least two types of data input signaling modes, single-ended signaling mode and differential signaling mode.” EX1005, [0002]. “Currently, for a variety of reasons, the former [signaling mode] tends to be favored by the lower speed, higher voltage integrated circuits, while the later [*sic*] tends to be favored by the higher speed, lower voltage integrated circuits.” *Id.* “The differences between the two signaling modes create[s] difficulties for designing the Input sections of the integrated circuits of the different types, especially since they often have to co-exist and co-operate with each other in the same system” *Id.* Like the '028 Patent, Cole proposes solutions to address these problems through a configurable IC that supports different signaling modes.

In more detail, Cole discloses an input section of an IC configured to control latching operations based on complementary strobe input signals including a first strobe input signal (xxStbP) and a second strobe input signal (xxStbN). EX1005,

[0013]-[0020], [0023]-[0028], FIGS. 1 (disclosing strobe input “CLOCK PATHS” 12), 2A-2C. Using these complementary strobe input signals, the input section generates two internal strobe signals (sometimes referred to as “StbP” and “StbN”) for controlling data flow through latch banks 26 in a plurality of data paths.

EX1005, [0017], [0019]-[0021], [0026], [0027], FIG. 1, FIG. 2A; EX1003, ¶44.



EX1005, FIG. 1 (annotated).

Cole’s input section further includes a configurable clock input buffer that controls the integrated circuit to operate in a “differential signaling mode” or a “single-ended signaling mode” based on a control signal (DIFFEN). EX1005, [0018], [0022]-[0023], [0034]; *see also* [0013], [0017]-[0019], [0021], [0025], [0028], FIGs. 1, 2A; EX1003, ¶45. The clock input buffer includes “sense amplifiers 114 and 116” that each receive the complementary strobe input signals xxStbP and xxStbN as differential signals and “sense amplifiers 118 and 120” that

each receive one of the complementary strobe input signals as a single ended signal. EX1005, [0026], [0028], *see also id.*, [0019], [0021], [0021], FIGs. 1, 2A.

When the DIFFEN control signal has a value “1,” the sense amplifiers 114 and 116 are activated thereby causing the integrated circuit to operate in the differential signaling mode, and when the DIFFEN control signal has a value “0,” the sense amplifiers 118 and 120 are activated, thereby causing the integrated circuit to operate in the single ended signaling mode. *Id.*, [0023].

3. Arcoleo

Arcoleo describes a memory device including an output buffer that manages data output from a memory chip. EX1006, 1:6-10, 2:66-3:6, 3:43-4:28, 6:10-65, 8:1-46, 8:47-10:5, FIGs. 4-6; EX1003, ¶46. The output buffer is controlled by a “drive strength selector (*sic*)” that “enables control of the operation of the output buffer” to select “one of a set of possible output buffer drive strengths.” EX1006, 6:10-7:23, FIG. 4. Arcoleo therefore includes a configurable output buffer that is configurable to one of a plurality of drive strengths. *Id.*

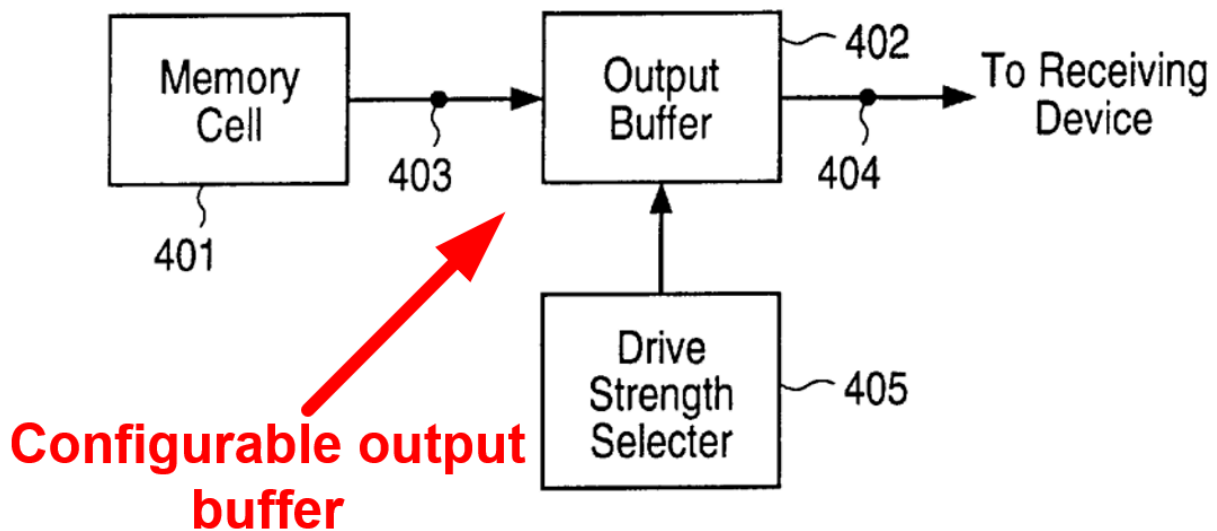


FIG. 4

EX1005, FIG. 4 (annotated).

Arcoleo explains that the drive strength from the output buffer is configurable so that “the drive strength of the output buffers of a memory device” is “appropriately matched” with the electrical load at an output of the output buffer. EX1006, 1:37-51. For example, when the output drive strength is too strong, this can cause “an impedance mismatch between the output buffer and the transmission line electrical load” and when the output drive strength is too weak, “the data can be supplied from the memory device to the receiving device more slowly than desired.” EX1006, 1:52-2:11. Using a configurable output buffer can prevent these issues from occurring. EX1003, ¶47.

4. The Ryu-Cole-Arcoleo Combination

Combining Ryu with Cole

As discussed above, Ryu discloses a non-volatile memory device that controls operations to read and write data from a non-volatile memory array in a synchronous fashion. EX1004, [0003], [0005], [0041]-[0043], [0059], [0060], [0066]-[0070], [0076], [0094], [0095], FIGs. 5, 7, 11, 12; *supra*, §V.A.1; EX1003, ¶48. Although Ryu's device incorporates use of a system clock signal, Ryu nonetheless describes few details about the clock signal or the particular type of signaling configuration implemented on the device. For example, although a POSITA would have known that ICs commonly employed either a single-ended signaling configuration or a differential signaling configuration, Ryu does not expressly address which configuration its device employs or how its device would communicate with other devices that use different signaling configurations. EX1003, ¶48. A POSITA therefore would have turned to Cole for details of a known and beneficial technique for implementing a configurable input section of an IC capable of selectively switching between a single ended signaling configuration and a differential signaling configuration. *Supra*, §V.A.2. Multiple reasons would have prompted a POSITA to integrate a configurable input section that can be selectively configured to a single ended signal mode or a differential

signaling mode as suggested by Cole in the non-volatile memory device of Ryu.

EX1003, ¶48.

First, a POSITA would have pursued the combination to achieve interoperability between Ryu's device and other devices regardless of the type of signaling employed (e.g., single ended signaling or differential signaling). EX1003, ¶49. For example, Cole discloses that the single ended signaling mode "tends to be favored by lower speed, higher voltage integrated circuits" and the differential signaling mode "tends to be favored by higher speed, lower voltage integrated circuits." EX1005, [0002]; EX1003, ¶49. A configurable clock input buffer like that taught in Cole would have been beneficial to allow Ryu's non-volatile memory device to toggle between the single ended signaling mode and the differential signaling mode so that these modes "co-exist and co-operate with each other in the same system." EX1005, [0002]; *see also id.*, [0001], [0013], [0043], FIG. 8, Abstract; EX1003, ¶49. This enables the system to operate in a variety of different environments. EX1003, ¶49.

Second, a POSITA would have implemented Ryu's non-volatile memory device to include a configurable input section as suggested by Cole to allow the memory device to receive data signals according to either a single-ended or differential mode signaling configuration in an efficient manner using common circuit components that were well known before the Critical Date. EX1003, ¶50.

For example, Cole explains that the input section 10 includes two multiplexors 18, each receiving a respective input from one of the differential sense amplifier circuits 14 and one of the single-ended sense amplifier circuits 16. EX1005, [0019]-[0022], [0026], FIGs. 1, 2A; EX1003, ¶50. The multiplexors 18 each receive a control signal “Diffen” that controls whether the multiplexor passes the output from the differential sense amplifier circuit according to the differential signaling mode or the single ended sense amplifier circuit in the single-ended signaling mode. *Id.* Thus, a POSITA would have understood that multiplexors can readily select outputs from appropriate amplifiers to provide configurability between modes in an efficient manner based on a single “Diffen” control signal. *Id.*

Third, a POSITA would have implemented Ryu’s memory device with a configurable input section as suggested by Cole to allow the memory device to efficiently latch received data regardless of whether the received data is signaled using either a single-ended or differential signaling scheme. EX1003, ¶51. Doing so would allow the non-volatile memory device to more efficiently receive data through I/O pins of the device using either single-ended or differential signaling. EX1005, [0025] (“[T]o achieve at least the same data transfer rate for a given set of pins ..., the embodiment is designed to allow the data to be transmitted on each data path at twice the speed while operating in a differential signaling mode (as compared to the speed of transmission while operating in the single-ended

mode).”); EX1003, ¶51. Indeed, Cole explains that “[l]atch banks 26 may be employed to latch and temporarily store the data being transferred,” and “[t]he latch banks 26 may operate in accordance with enabling pulse clocks 28” that are generated based on complementary clock signals, and “[a]n enabling pulse clock generator 24 may be employed to provide latch banks 26 with enabling pulse clocks 28 to control their operations.” EX1005, [0016], [0017]; *see also id.*, [0015]-[0018], [0023]-[0025], FIGS. 1, 2B; EX1003, ¶51.

Fourth, a POSITA would have been motivated to implement the memory device of Ryu with a configurable input section that receives two complementary strobe input signals as taught by Cole (e.g., xxStbP, xxStbN) to enable generation of internal strobe signals according to either of a single-ended or differential signaling mode. EX1003, ¶52. In the differential signaling mode, for example, Cole’s input section 10 generates internal strobes based on the complementary strobe inputs. EX1005, [0026] (“each of sense amplifiers 114 and 116 receives both two strobe signals and generates StbP/StbN based on the received signals”); EX1003, ¶52. In the single ended signaling mode, Cole’s input section 10 likewise generates internal strobes, but each of the internal strobes is generated based on a respective one of the complementary strobe inputs. EX1005, [0026] (“each of sense amplifiers 118/120 receives one of the two strobe signals...and generates StbP/StbN based on the received signals”); EX1003, ¶52.

Fifth, a POSITA would have found it obvious to combine the teachings of Ryu with Cole because the combination merely involves the application of a known technique to a known system to achieve predictable results. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious). “It’s enough... to show that there was a known problem... in the art, that [another known teaching] ... helped address that issue, and that combining the teachings of ... wasn’t beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81, (Fed. Cir. 2023). Here, Cole recognized a problem in reconciling speed and power requirement tradeoffs between ICs that implement differential or single-ended signaling modes, and Cole described a straightforward solution to address it. EX1003, ¶53.

A POSITA would have reasonably expected success implementing Ryu with Cole, especially since the combination involves well known data transfer techniques and conventional logic circuitry that was also well known before the Critical Date. *KSR* at 401; EX1003, ¶53. The configurable IC input section suggested by Cole would be compatible with the non-volatile memory device of Ryu, especially as Ryu and Cole describe similar techniques for controlling data outputs based on one or more clock signals. EX1004, [0003] (“SCLK represents a

system clock”); EX1005, FIG. 2A (depicting “clock paths”); EX1003, ¶53. Cole also expressly confirms that its configurable input section can be implemented in a wide range of ICs including memory devices like those disclosed in Ryu. EX1005, [0043]-[0044], [0046]-[0047], [0045] (“system 800 may include other components, including but [] not limited to non-volatile memory” and “[o]ne or more of these components may also include input section 10”), FIG. 8.

Combining Ryu-Cole with Arcoleo

As described above, it would have been obvious to implement Ryu’s memory device to include an input section configurable between a single ended signaling configuration and a differential signaling configuration as taught in Cole. EX1003, ¶54. Ryu further explains that an “input/output buffer 533 outputs or blocks the data DATA[7:0]” and “output driver 535 outputs the data DATA[7:0] from the input/output buffer 533 to the external source through [an] input/output pin.” EX1005, [0060]. Neither Ryu nor Cole describes in detail the electrical requirements of devices coupled to an input/output pin of the memory device, however. EX1003, ¶54. A POSITA therefore would have turned to Arcoleo for additional guidance on implementing an output driver for outputting data from the memory device. EX1003, ¶54. For example, Arcoleo discloses that “[a]n output buffer drive strength selector [*sic*] 405 enables control of the operation of the output buffer 402 so that the output buffer 402 has a selected one of a set of

possible output buffer drive strengths...”, thus providing a solution to configure an output drive strength based on the electrical load of the outputs. EX1006, 6:19-65, 14:10-21, FIG. 4; §V.A.3; EX1003, ¶54. A POSITA would have been motivated to further augment the Ryu-Cole memory device with the features disclosed in Arcoleo for multiple reasons. EX1003, ¶54.

First, a POSITA would have implemented Ryu-Cole’s non-volatile memory device with a configurable output buffer as taught by Arcoleo because it was known to be beneficial to tailor the drive strength of the output buffer to the needs of the system. EX1003, ¶55. Indeed, more than eight years before the Critical Date of the ’028 Patent, Arcoleo explained that “[i]n many current electronic [s]ystems...SRAMs must drive and switch electrical loads that are more accurately modelled as distributed capacitive loads (i.e., as transmission lines), rather than as lumped capacitive loads, thus *necessitating output buffers having different drive characteristics.*” EX1006, 1:45-51; EX1003, ¶55. Arcoleo also confirms that its techniques can be applied to a range of different memories including non-volatile memory devices like those described in Ryu. EX1006, 5:30-33 (“The invention can be implemented with any type of memory device, such as, for example, SRAM, ... flash memory ...”), 5:22-29.

Second, Arcoleo explains that the output buffer can be implemented simply using two inverters connected in parallel, where one of the inverters can be

connected and disconnected via a switch to control the drive strength. EX1006, 6:37-65; FIGs. 5A-5B. A POSITA would have understood that this configuration is a straightforward and effective way to control drive strength, because connecting and disconnecting an inverter using a switch can be done using well-known components that are easy to control. EX1003, ¶56. Thus, a POSITA would have been motivated to modify the non-volatile memory device of Ryu-Cole with the output buffer of Arcoleo. *Id.*

Third, implementing the non-volatile memory device of Ryu with an output buffer having a user-selectable drive strength, as taught by Arcoleo, would have been obvious and beneficial to promote use of the non-volatile memory devices in a wider range of systems while allowing a system designer to more flexibly incorporate the device in a larger computer/memory system. EX1003, ¶57. Arcoleo explains that “[w]hile output buffers having selectable drive strength have previously been used with other devices...selectable drive strength output buffers that allow a user to adjust the output buffer drive strength have not heretofore been used with...memory devices.” EX1006, 3:7-40; EX1003, ¶57. This allows “the output buffer drive strength to be easily selected by a user of the memory device...from the multiple possible drive strengths.” EX1006, 3:43-65; EX1003, ¶57. A POSITA would have understood that allowing a user to configure the

output drive strength would be beneficial to permit a user to integrate a memory device in a custom system having other components. EX1003, ¶57.

Fourth, because the configurable output buffer of Arcoleo receives a bit stream of output data from a single memory cell, a POSITA would have found it obvious to implement the memory device of the Ryu-Cole combination with a configurable output buffer for each common data signal that is output by the memory device. EX1003, ¶58.

Fifth, a POSITA would have found it obvious to further combine the teachings of Ryu-Cole with Arcoleo because the combination merely involves the application of a known technique to a conventional system to achieve predictable results. *KSR*, 550 U.S. at 417; *Intel*, 61 F.4th at 1380-81. Here, Arcoleo recognized a problem with existing output buffers and described a straightforward method to address it. In this context, combining the teachings of Ryu-Cole with Arcoleo would have been obvious, and a POSITA would have reasonably expected success, especially considering that the combination merely implicates conventional techniques for transmitting common data and conventional circuitry. *KSR* at 401; EX1003, ¶59. The Ryu-Cole memory device would be fully compatible with a configurable output buffer as taught in Arcoleo. For example, both provide memory devices outputting data stored by memory cells via an output buffer. EX1004, [0060], [0061]; EX006, 6:10-36; EX1003, ¶59.

5. Application to Challenged Claims

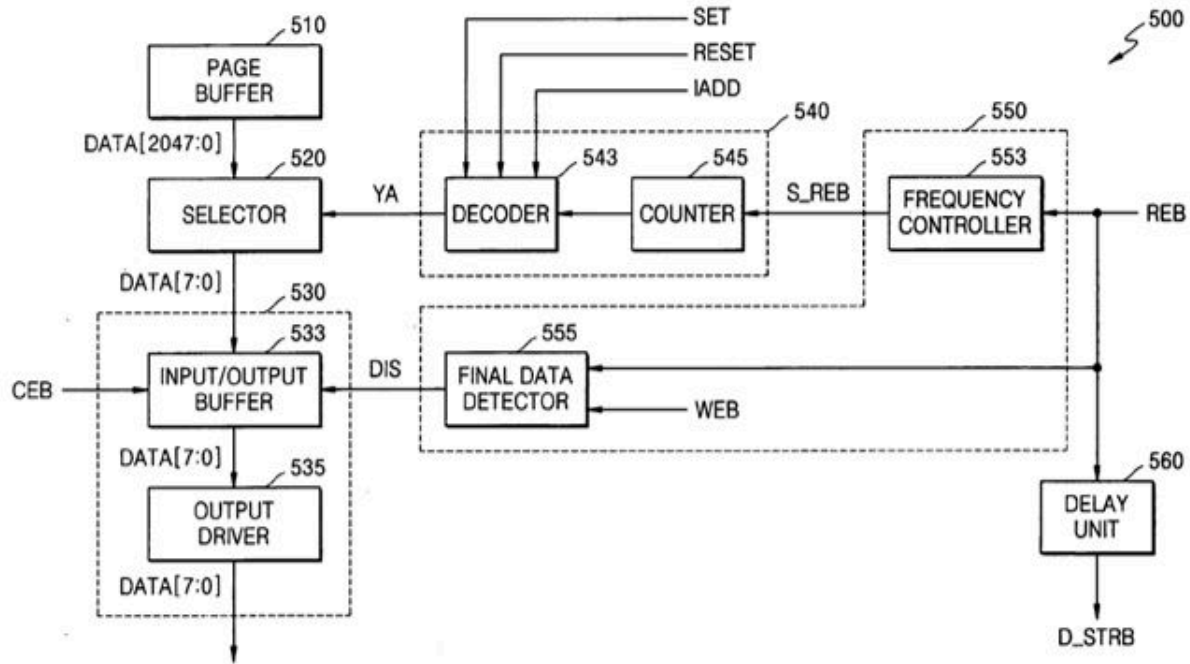
Element [1pre]

To the extent the preamble is a limitation, the Ryu-Cole-Arcoleo combination renders obvious the claimed “configurable non-volatile memory device.” EX1003, ¶83. For example, Ryu expressly discloses a “***non-volatile memory device***.” EX1004, [0009] (“According to some embodiments of the present invention, a non-volatile memory device is operated by ...”), [0036] (“the present invention can be embodied in various nonvolatile memory devices ...”); *see also id.*, [0002]-[0005], [0007], [0009], [0012]-[0014], [0042], [0046], [0047], [0062], [0064], [0065], [0069], [0070], [0072], [0076], [0077], FIGs. 5, 11.

The ***non-volatile memory device*** is also ***configurable***. EX1003, ¶84. For example, Ryu discloses that an output unit of the memory device can be “activated in response to an enable signal (CEB) and deactivated in response to a disable signal (DIS). EX1004, [0043], [0059]-[0061], [0078], FIGs. 5, 11. Further, the memory device includes a ***configurable*** input section as taught in Cole and a ***configurable*** output buffer as taught in Arcoleo. *Supra*, §V.A.1-4.

**Non-volatile
memory device**

FIG. 5

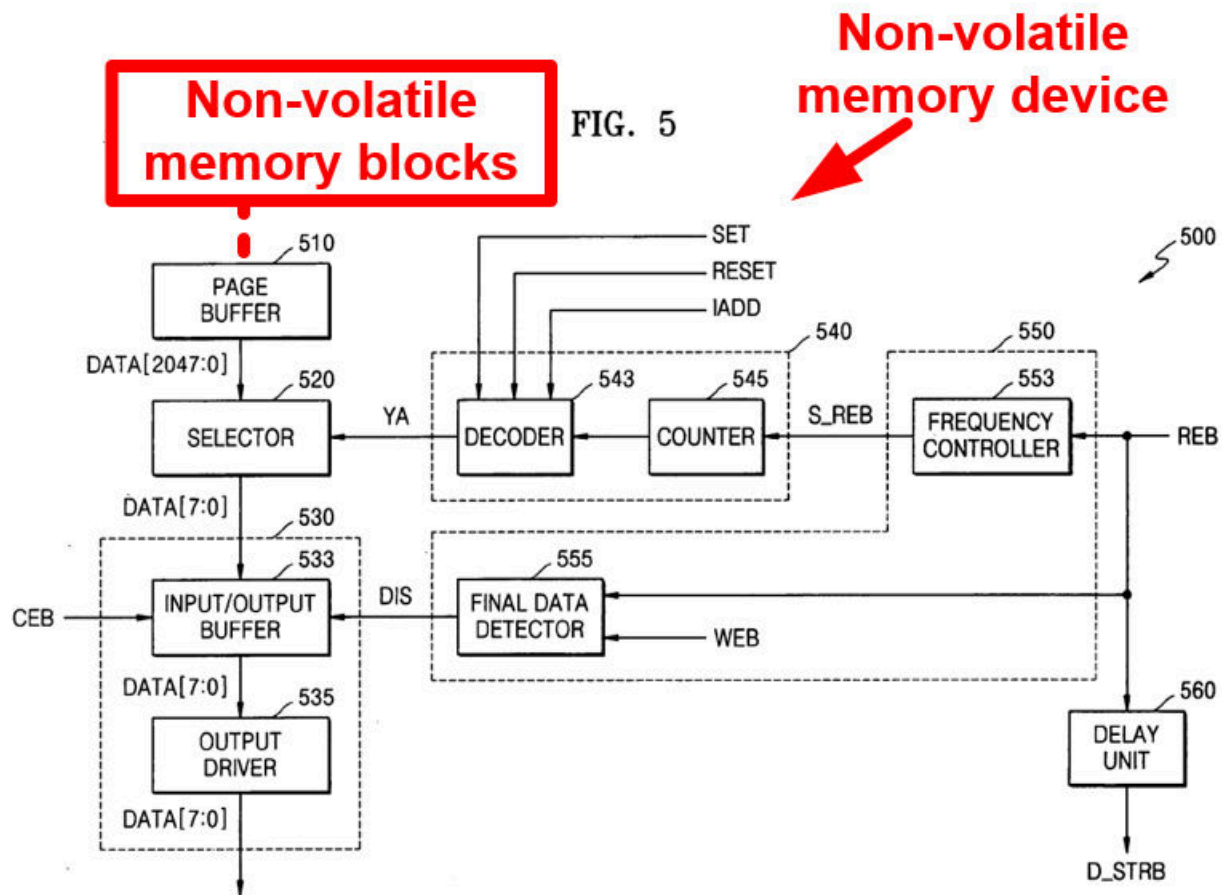


EX1004, FIG. 5 (annotated).

Element [1a]

The Ryu-Cole-Arcoleo combination renders obvious [1a]. EX1003, ¶¶85-87. Ryu explains that the non-volatile memory device includes a “page buffer” that “stores a portion of data stored in a non-volatile memory array (not shown).” EX1005, [0042]; *see also id.*, [0046] (“page buffer... receives and stores data from a non-volatile memory array”), [0077], Cls. 5, 17; EX1003, ¶85. According to Ryu, the non-volatile memory array can be implemented “in the context of a NAND flash memory,” which includes a *plurality of non-volatile memory blocks*.

EX1004, [0036]; cf. EX1001, 2:17-24 (“organized into blocks to facilitate block erasure”), FIG. 4; see also EX1003, ¶¶86-87 (citing corroboration EX1010, 15:15-34; EX1011, 1:45-54; EX1012, 4).



EX1004, FIG. 5 (annotated).

Element [1b]

The Ryu-Cole-Arcoleo combination renders obvious [1b]. EX1003, ¶¶88-91. Ryu explains that the *non-volatile memory device* includes an “output unit,” e.g.,

EX1004, FIG. 5 (annotated).

The '028 Patent also admits that chip enable signals were known in “*prior art* flash memory system[s]” and explains that such prior art memories commonly included a ***plurality of memory devices*** that each receive a chip enable signal (CE#). EX1001, 1:54-2:52, FIG. 1; EX1003, ¶91.

Element [1c]

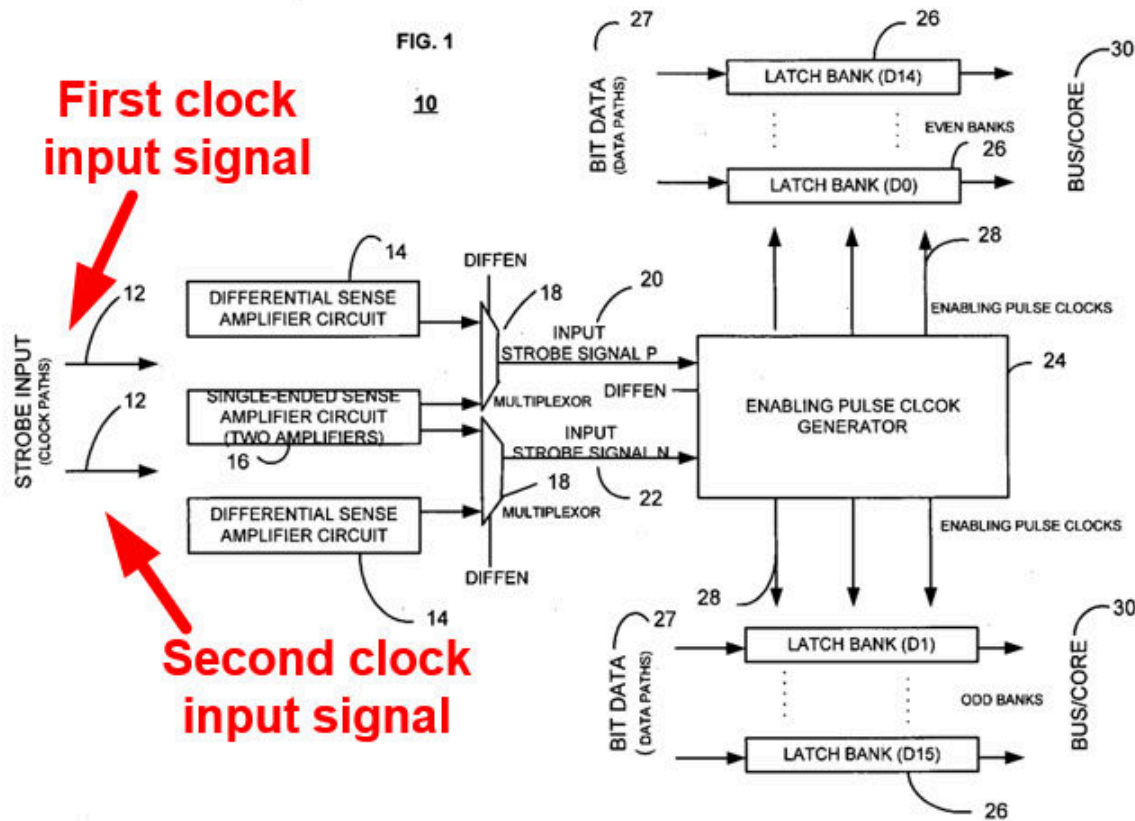
The Ryu-Cole-Arcoleo combination renders obvious [1c]. EX1003, ¶¶92-101. As an initial matter, Ryu’s ***non-volatile memory device*** discloses a system clock that aids in synchronizing operations of the memory device. EX1004, [0003] (“SCLK represents a system clock”), [0062], [0063], FIGs. 1A-1B, FIG. 7. Ryu also discloses a read control signal (REB) as a timing signal that synchronizes read operations on the device. *Id.* REB is exactly half the frequency of the system clock such that one cycle of the system clock is equal to one half cycle of the read control signal. *Id.* In another embodiment, Ryu discloses a flash clock signal (F_CLK) that is also exactly half the frequency of the system clock and that synchronizes read operations by the memory device. EX1004, [0080], [0083]-[0088], [0091], [0092], [0094], FIGs. 11, 12; EX1003, ¶92.

Ryu’s non-volatile memory device is modified in the combination based on Cole to include an “input section” that receives “strobe inputs” for controlling “latch banks” to cycle data through one or more “input data paths.” EX1005,

[0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, §V.A.2, V.A.4; EX1003, ¶93. For example, Cole explains that the “strobe inputs 12 are provided by the source of the data being transferred” such that “the data may be transferred source synchronously.” EX1005, [0020]; *see also id.*, (“strobe inputs 12 may be provided in parallel with the data”), [0019], FIGs. 1, 2A, 2C.

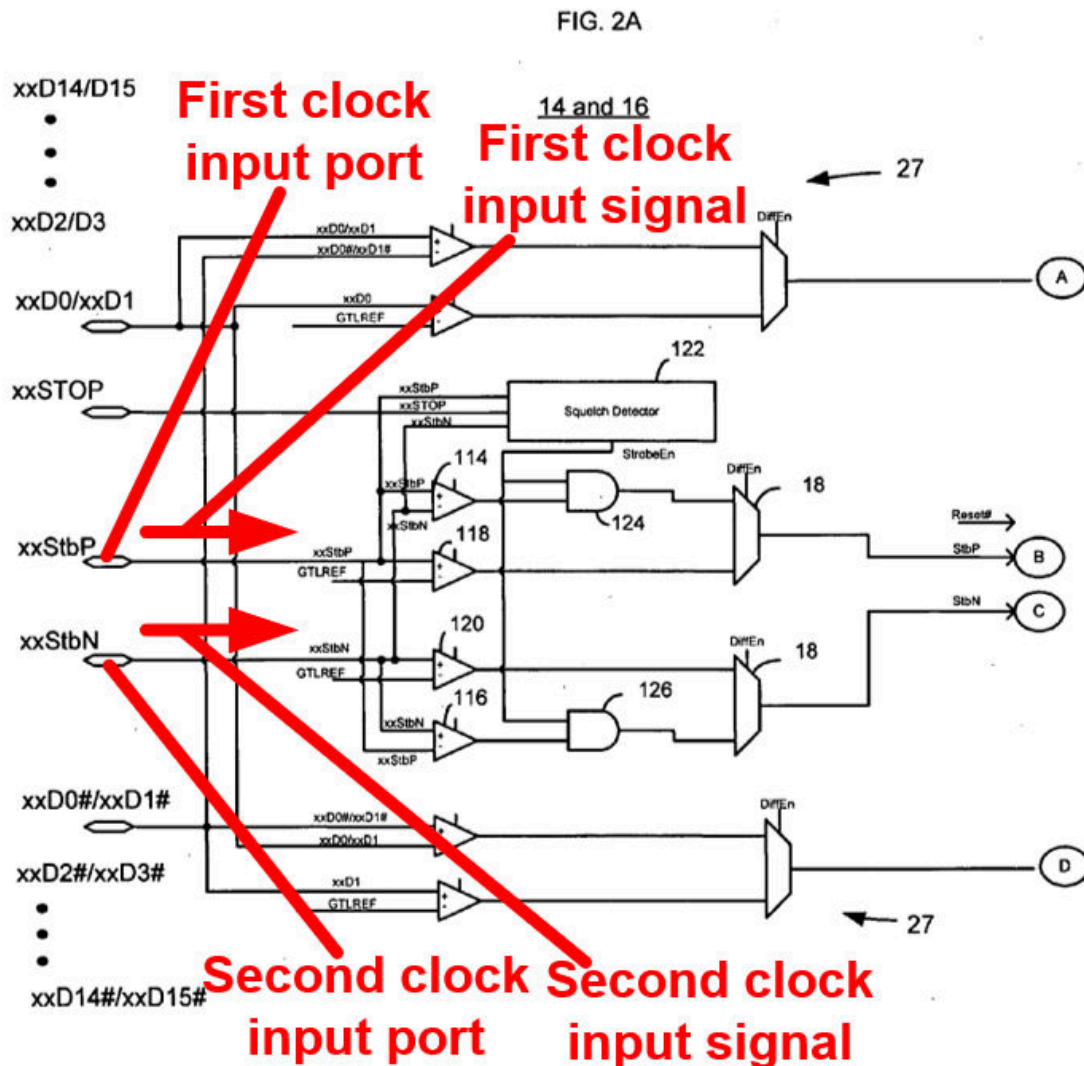
Notably, while Cole sometimes refers to inputs 12 as “strobe inputs,” Cole also refers to them as “CLOCK PATHS.” EX1005, FIG. 1 (“STROBE INPUT (CLOCK PATHS)”). A first of these strobe inputs or clock paths 12 is the “xxStbP” signal that provides a ***first clock input signal***. EX1005, [0026], FIG. 2A, FIG. 2C; EX1003, ¶94. A second of these strobe inputs or clock paths 12 is the “xxStbN” signal that provides a ***second clock input signal***.³ *Id.*

³ Patent Owner’s district court infringement allegations equate a strobe signal with a clock signal. *See* EX1100, 52-53; EX1101, 21-28; EX1102, 17-21. Petitioner’s mapping of data strobe inputs to clock input signals in this ground is based on Patent Owner’s interpretation of clock signals as encompassing data strobes, which Petitioner does not concede. Nonetheless, Patent Owner cannot credibly challenge this mapping that aligns with its own district court infringement theories. Ground 1B provides additional obviousness arguments addressing another interpretation of the claimed clock signals. *Infra*, §V.B; EX1003, ¶94.



EX1005, FIG. 1 (annotated).

Based on Cole's teachings, the input section of the Ryu-Cole-Arcoleo memory device predictably includes a *first clock input port* for receiving the *first clock input signal* "xxStbP" and a *second clock input port* for receiving the *second clock input signal* "xxStbN" as signified by the port symbols on the left-hand side of FIG. 2A. EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, §V.A.4; EX1003, ¶95.



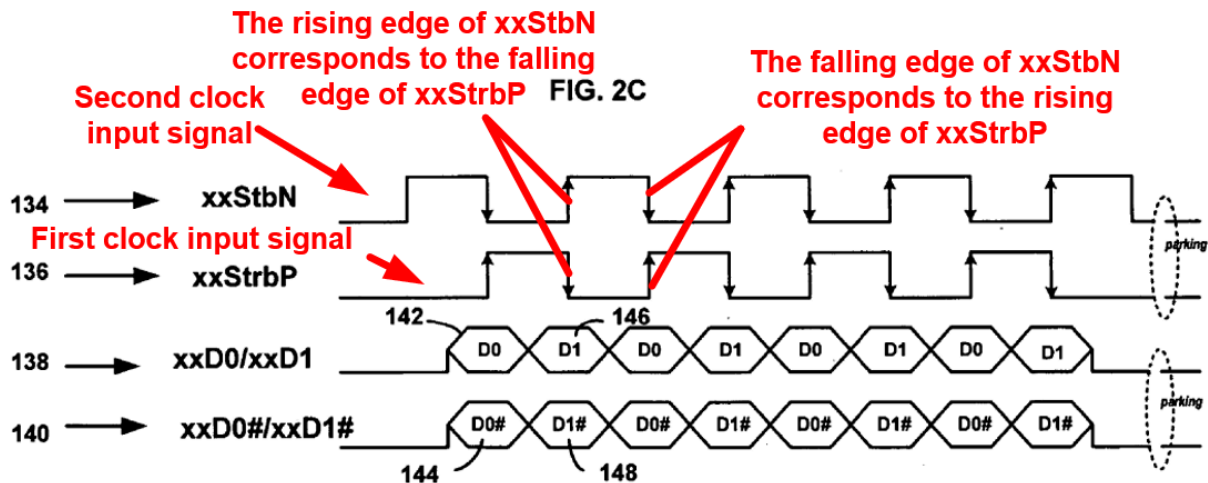
EX1005, FIG. 2A (annotated).

In the context of the data paths, Cole explains that “to achieve at least the same data transfer rate for a given *set of pins* (16 for the embodiment), the embodiment is designed to allow data to be transmitted on each data path.”

EX1005, [0025], FIG. 2A; EX1003, ¶¶96-98. These pins include two pins for each pair of “data paths” (i.e., $xxD0$, $xxD1$, and so on), and each of these pins represents a *port* for receiving input data. *Id.* Cole uses the same symbol to depict the inputs

for the *first clock input signal* (xxStbP) and the *second clock input signal* (xxStbN) as Cole uses for the data input pins. *Id.* This confirms that Cole’s pin for receiving xxStbP represents a *first clock input port* and the pin for receiving xxStbN represents a *second clock input port*. *Id.*

A POSITA would have understood the *first clock input signal* (xxStbP) and the *second clock input signal* (xxStbN) to be *complementary*. EX1003, ¶¶99. For example, the rising edges of xxStbN are aligned with falling edges of xxStbP and falling edges of xxStbN are aligned with rising edges of xxStbP such that the signals are the inverse of each other. EX1005, [0019], [0020], [0026], [0027], FIGs. 2A, 2C; cf. EX1001, 9:19-48, 10:42-11:18, 17:32-51, 20:47-64, FIGs. 3B, 3D, 8B EX1003, ¶¶100-101 (citing corroboration EX1015, 2; EX1016, FIG. 3A).



EX1005, FIG. 2C (annotated).

Element [1d]

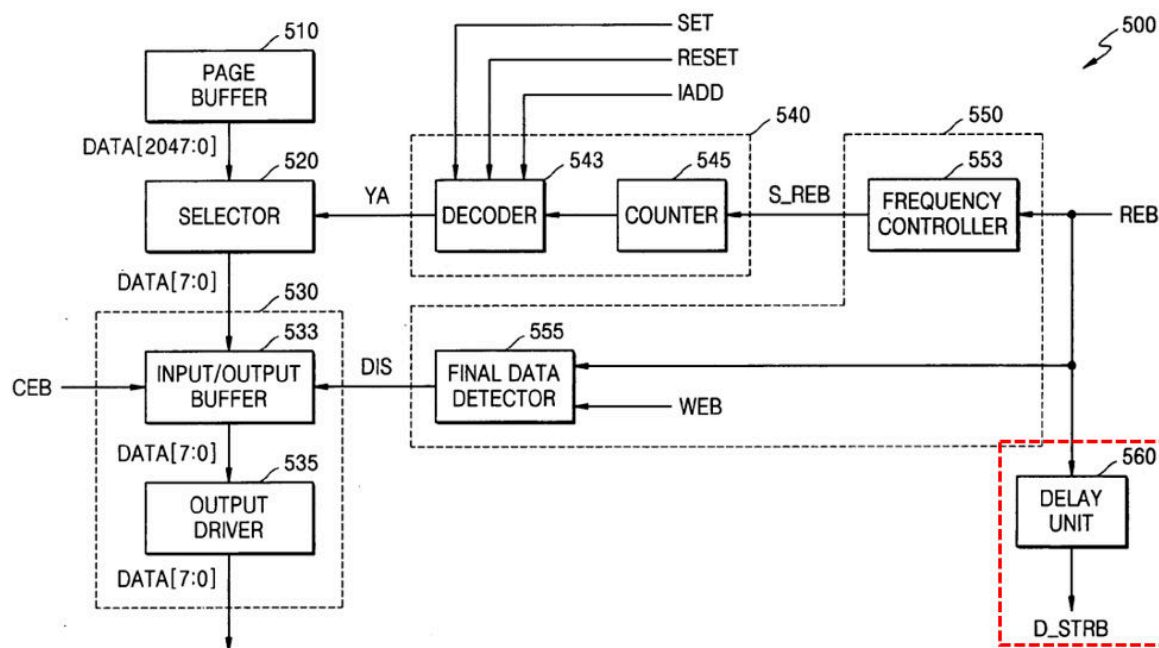
The Ryu-Cole-Arcoleo combination renders obvious [1d]. EX1003, ¶¶102-106. For example, Ryu explains that the ***non-volatile memory device*** includes a “delay unit” that generates a D_STRB signal to be “output at the same time with the data DATA[7:0] to the external source.” EX1004, [0064], *see also id.*, [0065]-[0070], [0092], [0095], FIGs. 5, 7, 11, 12, Cls. 10, 22; EX1003, ¶102. In some examples, the D_STRB signal “is generated by delaying the read control signal by a predetermined delay time” and the D_STRB signal “is output with the data concurrently to an external source.” EX1004, [0011], [0016]. In other examples, the D_STRB signal “is created by delaying the flash clock signal F_CLK by a predetermined time and [is] output at the same time with the data DATA[7:0] to an external source.” *Id.*, [0091]-[0095]. Ryu’s D_STRB is an output that indicates the exact timing of output data presented at the input/output pin (IOP) of the device. EX1003, ¶103. Based on the interpretation of “clock signal” underlying Patent Owner’s infringement allegations, Ryu’s D_STRB signal provides a ***clock output signal*** as claimed. *See* EX1100, 52-53; *supra*, Footnote 3; EX1101, 21-28; EX1102, 17-21; *see also infra*, Ground 1B at [1d].

Ryu’s explanation that D_STRB is “output” from the ***non-volatile memory device*** confirms that the ***non-volatile memory device*** comprises an ***output port*** configured to transmit D_STRB to a downstream device. *See* EX1004, [0064]-

[0070], [0091]-[0095] (data “is transmitted from the non-volatile memory device 1100 to the external controller” and the non-volatile memory device 1100 outputs a D-STRB signal “for indicating the time when the controller fetches the data”).

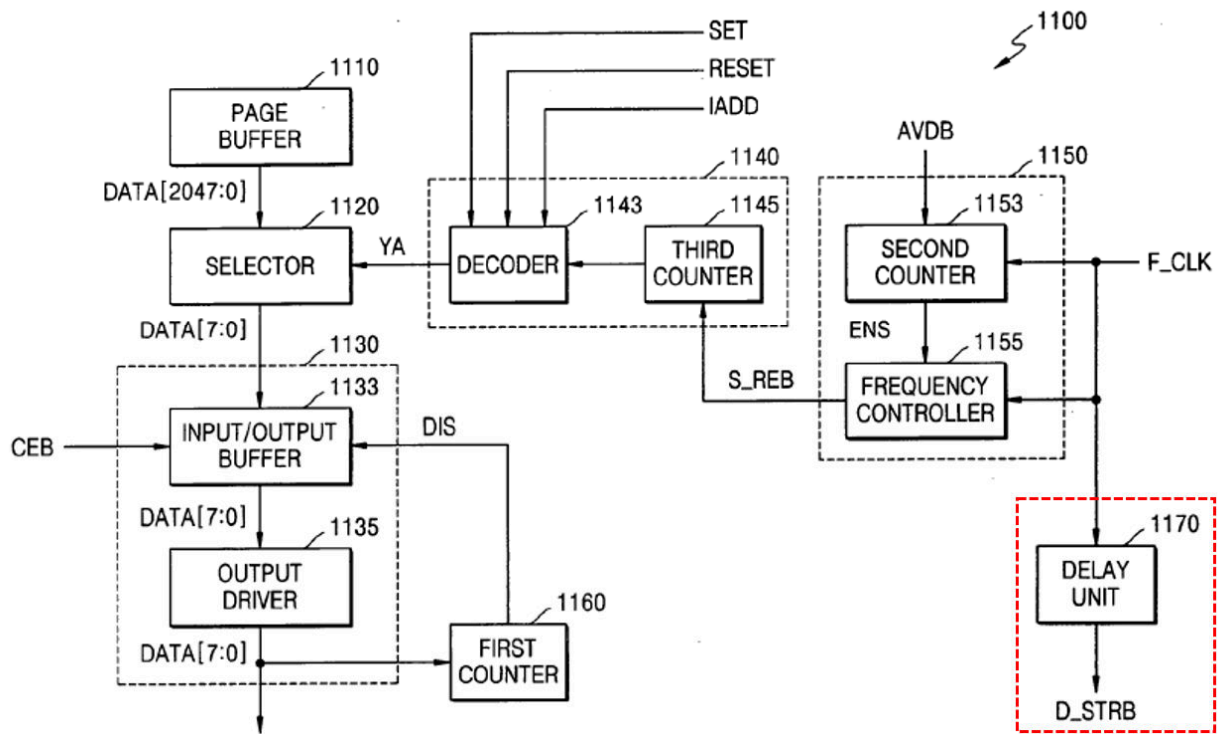
Indeed, Cole explains that strobe signals like Ryu’s D_STRB are transmitted synchronously and in parallel with data transmitted on a different line. EX1005, [0022] (“[s]trobe ... provided in parallel with the data”). A POSITA thus would have understood that D-STRB would be transmitted in parallel with the output data from an *output port* distinct from the data input/output pin (IOP), which is consistent with the separate D_STRB and data output arrows depicted in FIGs. 5 and 11 of Ryu. EX1004, [0011], FIGs. 5, 11; EX1003, ¶104 (citing corroboration EX1007, 7:18-9:34; EX1009, [0084]-[0091]). Transmitting D_STRB in parallel with the data on a distinct output port also would have been obvious to eliminate the need for D_STRB to be extracted from the data by the downstream device that receives the signals. EX1005, [0020]; EX1003, ¶104.

FIG. 5



EX1004, FIG. 5 (annotated).

FIG. 11



EX1004, FIG. 11 (annotated).

A POSITA would have found it obvious to implement the D_STRB signal (*clock output signal*⁴) in the Ryu-Cole-Arcoleo memory device to be referenced to a *first clock input signal*. EX1003, ¶105. Indeed, Ryu expressly discloses that D_STRB is generated by “delaying the flash *clock signal* F_CLK by a predetermined time,” meaning that Ryu specifically contemplates D_STRB being referenced to a flash clock signal. EX1004, [0094], FIG. 11; *see also id.*, [0091]-

⁴ *Supra*, Footnote 3.

[0095], [0064] (“D_STRB may [be] created by delaying the read control signal REB”).

Furthermore, in the combination, and based on Cole’s teachings, the input section of the memory device receives complementary input signals xxStbP and xxStbN, where xxStbP provides another example of a first clock input signal consistent with Patent Owner’s infringement theories.⁵ *Supra*, [1c]; EX1003, ¶106. A POSITA would have found it obvious to reference Ryu’s D_STRB signal (***clock output signal***⁶) to one of Cole’s complementary strobe input signals, such as xxStbP, so that the D_STRB signal can be used by external device(s) as an indication of the exact timing of values in the output data presented at the input-output pin (IOP). EX1003, ¶106 (citing corroboration EX1009, [0047]-[0048]). For example, a POSITA would have appreciated that memory devices like Ryu’s are commonly chained together and configured to pass data/commands from one device to another until the data/commands reach a target memory device in the chain where the data/commands are to be processed. EX1003, ¶106 (citing corroboration EX1009, [0030] (“memory devices are chained to one another” and “[c]ommands and data received within a given memory device are retransmitted to

⁵ *Supra*, Footnote 3.

⁶ *Supra*, Footnote 3.

a subsequent memory device ... By this operation, commands and data propagate rapidly through the chain...”), FIG. 3 (depicting chained memory devices), FIG. 5A (same), FIG. 17 (depicting clock output signal referenced to clock input signal used in passing data/commands from one device to another)). To pass input data and timing information (e.g., xxStbP) received from a prior memory device to a next device in the chain, it was known and obvious for output timing information (e.g., D_STRB) to be referenced to the input timing information (e.g., xxStbP) so that the output timing information (e.g., D_STRB) would match the input timing information (e.g., xxStbP) for the same data, but delayed by an amount corresponding to the propagation delay of the input data. EX1003, ¶106 (citing corroboration EX1009, [0048] (“each of the signals retransmitted by the initial memory device 155₁ is delayed by the same (or substantially the same) propagation delay, t_p”). This would have been obvious to ensure the output timing information (e.g., D_STRB) was synchronized with the data being passed to the next device in the chain. *Id.*

Element [1e]

The Ryu-Cole-Arcoleo combination renders obvious Element [1e]. EX1003, ¶¶107-117. As an initial matter, the '028 Patent concedes that the features recited in [1e] were known in the prior art. EX1001, 1:53-2:16, 2:20-22, FIG. 1.

Additionally, Ryu explains that ***non-volatile memory device*** can “receive or output

data through an input/output pin in synchronization with rising edges and/or falling edges of a read control signal and/or write control signal when reading or writing **data.**” EX1004, [0003], *see also id.*, [0005]-[0007], [0009], [0037], [0038], [0041]-[0043], [0045], [0059], [0060]-[0062], [0067], [0069], [0072], [0078], FIGs. 5, 7, 11, 12; EX1003, ¶¶107-108. The data that is received by the “input/output pin” and written to the non-volatile memory array represents **common data signals** carrying **input data** while the data that is read from the non-volatile memory and output from the “input/output pin” represents **common data signals** carrying **output data**. *Id.* In the combination, Cole likewise discloses I/O ports for the input section of the IC to receive data from a bus and to transmit data over the bus. EX1005, [0016], [0023], FIGS. 1, 2A-2B (disclosing data paths 27 and corresponding data ports), [0043]-[0044], FIG. 8 (bus 808); EX1003, ¶109 (citing corroboration EX1009, [0030], FIGS. 3, 5A, 17).

Ryu also discloses that “REB_CTRL is a read control signal generated from the controller...and is applied to the nonvolatile memory device” and that “WEB_CTRL is a write control signal generated from the controller...and is applied to the nonvolatile memory device,” which means that the non-volatile memory device further includes a port for transferring data signals carrying **command data** to control read and write operations. EX1004, [0005], *see also id.*, [0066], FIG. 5, FIG. 7; EX1003, ¶110. SET, RESET, CEB, WEB, and AVDB are

additional **command data** applied to the memory device via one or more ports.

EX1004, [0055], [0083], FIGs. 5, 11.

Furthermore, Ryu explains that the non-volatile memory device receives an initial address (IADD) and “generates an address signal YA,” and explains that a selector “outputs data corresponding to an address value of an address signal YA.” EX1004, [0042], [0044], *see also id.*, [0054], [0055] (“[t]he initial address IADD can be set by a designer through an external source”), [0057], [0058], [0077], [0079], [0087], [0088], FIGs., 5, 11; EX1003, ¶111. Thus, the non-volatile memory device also includes a data port for receiving data signals carrying **address data**. *Id.*

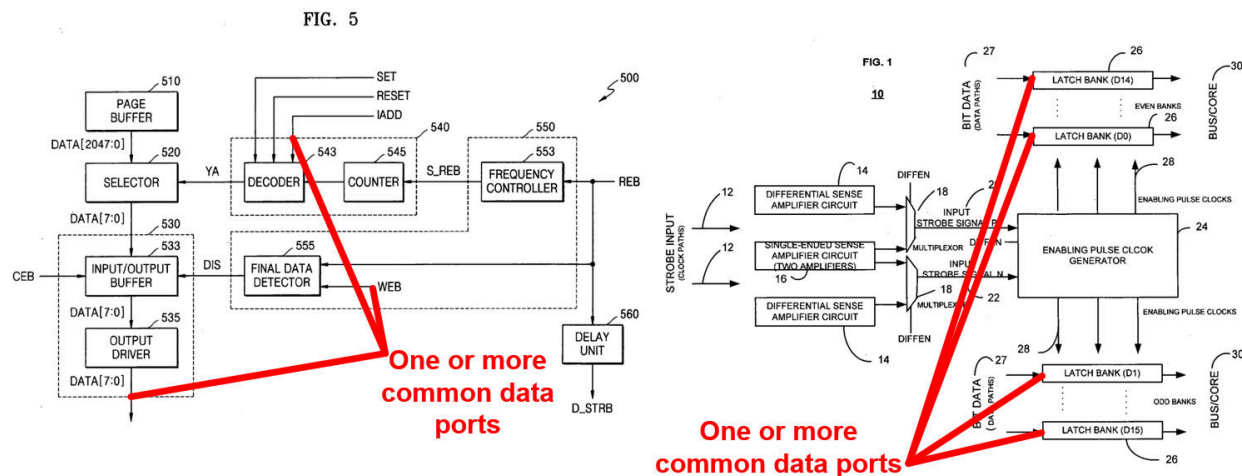
During a read operation, **command data** and **address data** received by the **non-volatile memory device** are used to access data stored in the non-volatile memory array. EX1004, [0042]-[0046], [0053]-[0062], FIG. 5. For example, Ryu discloses that “[t]he data is output in response to the first and second edges of the read control signal REB for controlling the output of the data. EX1004, [0048], *see also id.*, [0044], [0045], [0049], [0051], [0057], [0061], [0067], FIG. 5. Ryu also explains that the data output from the **non-volatile memory device** is selected based on **address data**. EX1004, [0042], [0043], [0060], FIG. 5; EX1003, ¶112. These teachings indicate that the **output data** is **retrievable** from the **non-volatile memory blocks** of the **non-volatile memory device**. *Id.*; *supra*, Element [1a];

EX1003, ¶¶112-114. For example, because “page buffer 510 stores a portion of data in a non-volatile memory array” and Ryu’s *non-volatile memory device* outputs data from the page buffer during a read operation, a POSITA would have understood and found obvious that the *output data* is retrievable from the *plurality of non-volatile memory blocks* because the page buffer itself retrieves data from the non-volatile memory array. EX1004, [0042], [0046], [0077]; *supra*, Element [1a].

A POSITA would have understood and found obvious that the *input data* to be stored according to a write operation would be programmed into one of the *plurality of non-volatile memory blocks* in a memory array like Ryu’s and accessible based on *command data* and *address data* as claimed. EX1003, ¶115 (citing corroboration EX1028, 4:59-6:56; EX1029, 1:24-35; EX1030, 4:50-5:5). For example, the command data such as a write control signal would indicate that the input data is to be written to memory and the address data would specify the location in memory where the input data is to be programmed and thus stored. This is also corroborated by a reference that describes address data. EX1009, [0068] (“memory addresses are typically provided with such commands”), [0071] (“write address”), [0072]-[0073]). A POSITA would have reasonably expected success implementing these features in the non-volatile memory device of the Ryu-Cole-Arcoleo combination because the use of command and address data was commonly

implemented in similar memory devices before the alleged invention of the '028 Patent. EX1003, ¶115 (citing corroboration EX1028, 4:59-6:56; EX1029, 1:24-35; EX1030, 4:50-5:5).

In the combination, Ryu's input/output pin, Ryu's ports for receiving *address data* and *command data* (e.g., IADD, SET, RESET, CEB, WEB, AVDB signals), and/or Cole's data bus ports provide *one or more common data ports* configured to transfer *common data signals* carrying at least one of *command data*, *address data*, *input data* and *output data*, as recited in Element [1e]. EX1005, [0016], [0023], [0043]-[0044], FIGS. 1, 2A-2B, 8; EX1003, ¶¶116-117.



EX1004, FIG. 5 and EX1005, FIG. 1 (annotated).

Element [1f]

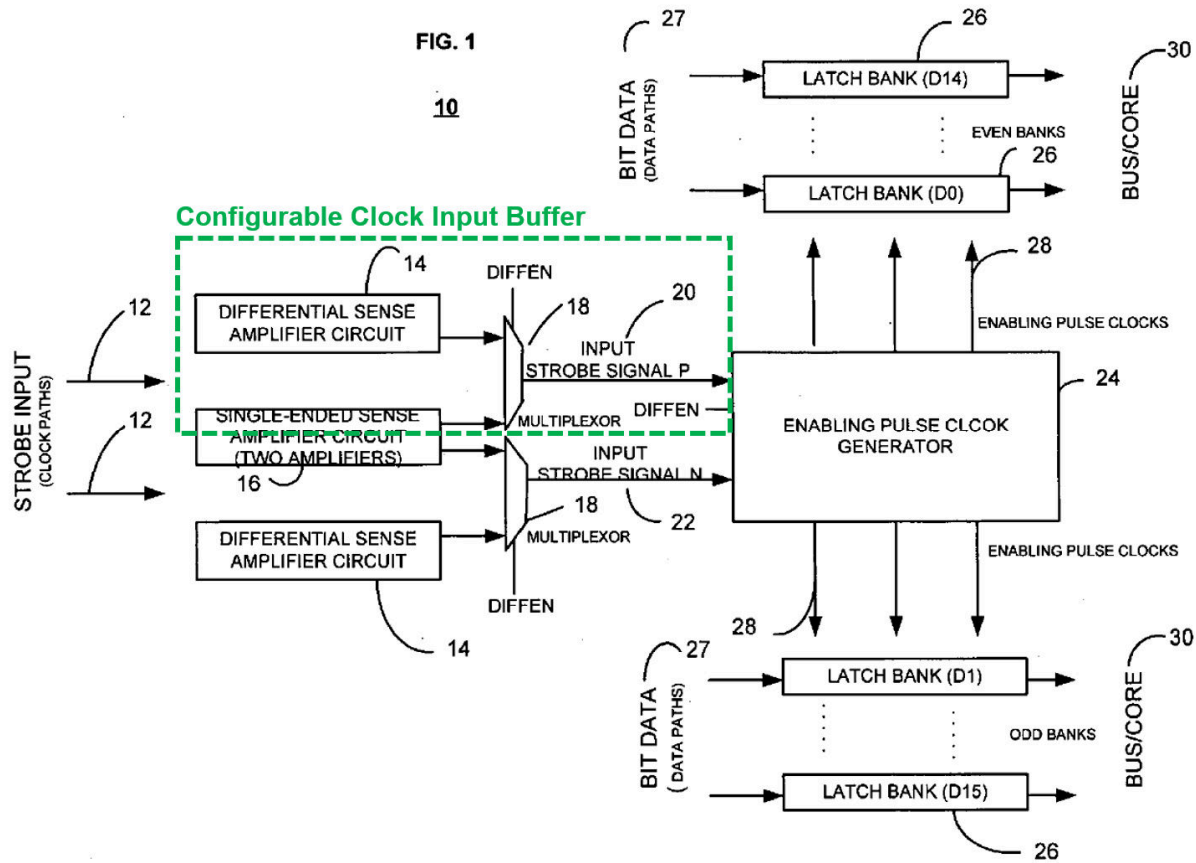
The Ryu-Cole-Arcoleo combination renders obvious [1f]. EX1003, ¶¶118-123. As described above, it would have been obvious to implement Ryu's non-

volatile memory device to include a configurable as taught in Cole. *Supra*, §V.A.2, §V.A.4. Cole's input section includes a **clock input buffer** including the **first clock input port** configured to receive the **first clock input signal** (sometimes referred to as a "strobe input" or "xxStrbP") and the **second clock input port** configured to receive the **second clock input signal** (referred to as a first "strobe input," "clock path," or "xxStrbP").⁷ EX1005, [0019], [0020], [0026], FIG. 1, FIG. 2A; *supra*, [1c]; EX1003, ¶118. For example, the **clock input buffer** includes a "differential sense amplifier" circuit 14 (including amplifier 114) and a first single-ended sense amplifier 118 (part of "single-ended sense amplifier circuit 16"), the **clock input buffer** receiving the first and second clock input signals, including xxStrbP and xxStrbN.⁸ EX1005, [0019], [0020], FIG. 1. Sense amplifier circuits 14 and 16 are coupled to a first multiplexor 18, which selectively passes the output of either

⁷ *Supra*, Footnote 3.

⁸ Alternatively, sense amplifiers 116 and 120 and the second multiplexor 18 can provide the claimed "**clock input buffer**," or both differential sense amplifier circuits 14 (including amplifiers 114 and 116), single-ended sense amplifier circuit 16 (including both amplifiers 118 and 120), and both multiplexors 18 collectively provide the claimed "**clock input buffer**." EX1003, ¶118.

sense amplifier 114 or 118 depending on the configuration mode. EX1005, [0021],
see also id., [0015], FIG. 1.



EX1005, FIG. 1 (annotated).

The *clock input buffer* of Cole’s configurable input section is *configurable* to operate in a “*single-ended signaling mode*” (*configuration*) or a “*differential signaling mode*” (*configuration*) based on a control signal (DIFFEN). EX1005, [0002] (“[s]ingle-ended signaling mode and differential signaling mode”), [0017], [0018] (“input section 10 may...be configurable to support either single-ended or differential signaling”), [0019], [0021]-[0023], [0028], FIGs. 1, 2A. Cole also

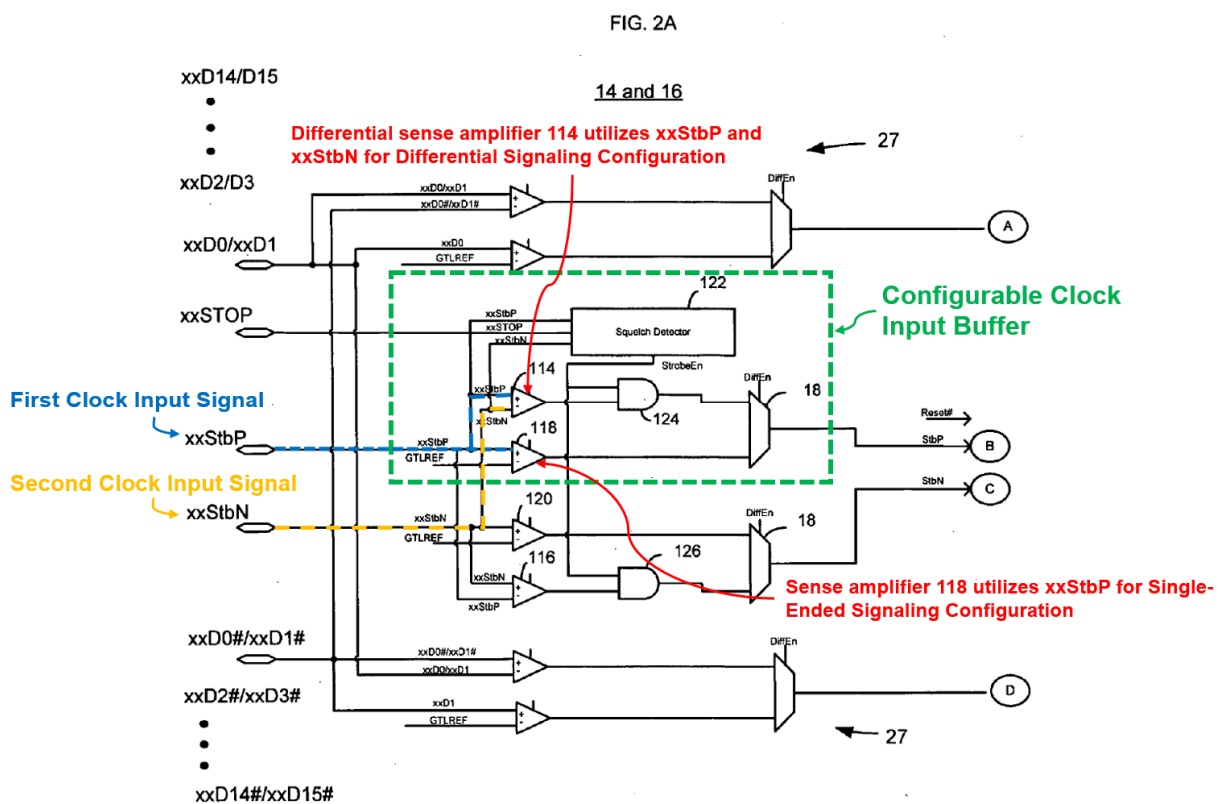
explains that multiplexors 18 use DIFFEN “to configurably select...the outputs of sense amplifier circuits 14 and 16...for the differential signaling mode and the single-ended signaling mode respectively,” and explains that the *differential signaling mode* is enabled when DIFFEN has a value “1” and the *single ended signaling mode* is enabled when DIFFEN has a value “0.” EX1005, [0021], [0022], FIG. 1; EX1003, ¶119.

In the *differential signaling configuration*, the differential sense amplifier circuit 14 utilizes both of the input signals 12 as *differential signals*. EX1005, [0015], [0019], [0021]-[0022], [0040]-[0041], FIGs. 1, 7. For example, Cole explains that the first differential sense amplifier circuit 14 includes a sense amplifier 114 that receives both of the *first clock input signal* “xxStrbP” and the *second clock input signal* “xxStrbN.”⁹ EX1005, [0023], [0026], [0028], FIG. 2A; EX1003, ¶120. Sense amplifier 114 produces a first timing signal based on comparison of the input signals xxStrbP and xxStrbN. EX1005, [0026], [0028], FIG. 2A, FIG. 2C.

In the *single ended signaling configuration*, the single-ended sense amplifier circuits 16 each utilize one of the input signals 12 as a *single ended signal*. EX1005, [0015], [0019], [0021]-[0022], [0040]-[0041], FIGs. 1, 7. For

⁹ *Supra*, Footnote 3.

example, Cole explains that the single-ended sense amplifier circuit 16 includes a sense amplifier 118 that receives the *first clock input signal* xxStbP.¹⁰ EX1005, [0023], [0026], [0028], FIG. 2A; EX1003, ¶121. Sense amplifier 118 produces a first timing signal based on xxStbP as a single-ended signal. EX1005, [0026], [0028], FIG. 2A, FIG. 2C.



EX1005, FIG. 2A (annotated).

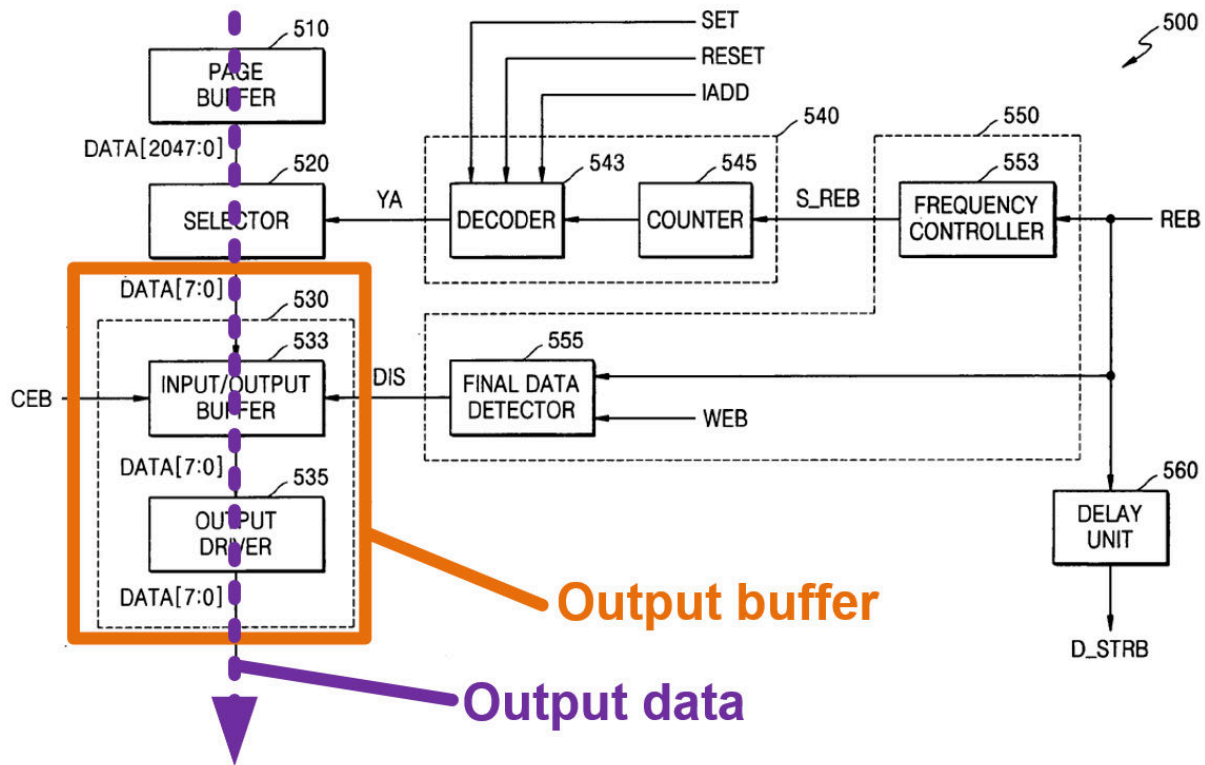
The fact that Cole's configurable clock input buffer circuitry is strikingly similar to the circuitry for the configurable clock input buffer disclosed in the '028

¹⁰ *Supra*, Footnote 3.

Patent supports that the limitations of Element [1e] would be rendered obvious by the Ryu-Cole-Arcoleo combination. *Cf.* EX1001, 17:32-51, FIG. 8A; EX1003, ¶¶122-123.

Element [1g]

The Ryu-Cole-Arcoleo combination renders obvious [1g]. EX1003, ¶¶124-127. For example, Ryu discloses that the output unit of the non-volatile memory device includes an “input/output buffer” and an “output driver” that collectively provide an ***output buffer*** as claimed. EX1004, [0060], [0061], [0078], [0090], FIG. 5, FIG. 11, Cls. 9, 21; *supra*, Element [1e]; EX1003, ¶124. Ryu’s ***output buffer*** receives an enable signal CEB and a disable signal DIS for controlling transfer of ***output data*** (“Data[7:0]”) to be outputted via the input/output pin (IOP). *Id.* For example, a selector retrieves ***output data*** from data in a page buffer, which represents a portion of data stored in Ryu’s non-volatile memory array (***non-volatile memory blocks***) and sends the output data to Ryu’s output unit for transfer via the input-output pin. EX1004, [0042], [0043], [0046], [0060], [0061], [0076]-[0078], [0090], FIG. 5, FIG. 11.



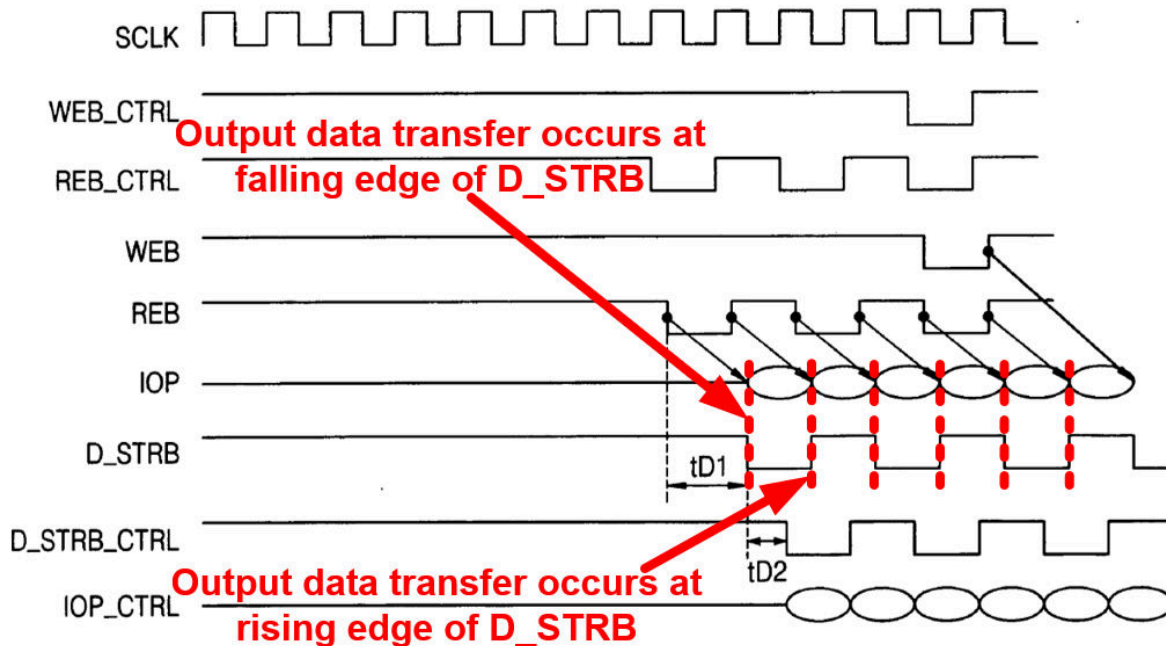
EX1004, FIG. 5 (annotated).

The *output data* (“Data[7:0]”) from Ryu’s *output buffer* is transferred “at the same time” as the *clock output signal* (“D_STRB”) from the *clock output port*. EX1004, [0064]-[0071], [0091]-[0095], FIGs. 5, 7, 11, 12; *supra*, Element [1d]; EX1003, ¶125. Ryu explains that “[t]he present invention relates generally to...*double data rate (DDR)* integrated circuit memory devices.” EX1004, [0002]; *see also* Title (“USING DOUBLE DATA RATE”). A POSITA would have recognized that Ryu’s *output data* is both edge aligned and *synchronized* with the *clock output signal* (“D_STRB”) ¹¹ in a *double data rate* configuration given that

¹¹ *Supra*, Footnote 3, Element [1d].

each half-cycle of the *clock output signal* corresponds to one output data unit at the input output pin (IOP). EX1004, [0066], [0067], [0094], [0095], FIGs. 7, 12.

FIG. 7



EX1004, FIG. 7 (annotated).

To the extent Ryu does not expressly disclose that the *output buffer* is *configurable* to one of a *plurality of output buffer drive strengths*, this feature would have been obvious and provided in the Ryu-Cole-Arcoleo combination. EX1006, 1:12-25, 1:37-2:11, 3:43-4:28, 6:10-65, 7:24-8:46, FIG. 4; *supra*, §§V.A.3-4; EX1003, ¶126. For example, Arcoleo discloses a “memory device” that includes a “memory cell” and an “output buffer circuit.” EX1006, 6:10-36, *see also id.*, 3:43-4:28, FIG. 4. Arcoleo discloses that the output buffer circuit includes

an “output buffer 402” and an “output buffer drive strength selector (*sic*) 405” that “enables control of the operation of the output buffer 402 so that the output buffer 402 has a selected one of a set of possible output buffer drive strengths.” EX1006, 6:10-65, *see also id.*, 8:1-10:5, FIG. 4.

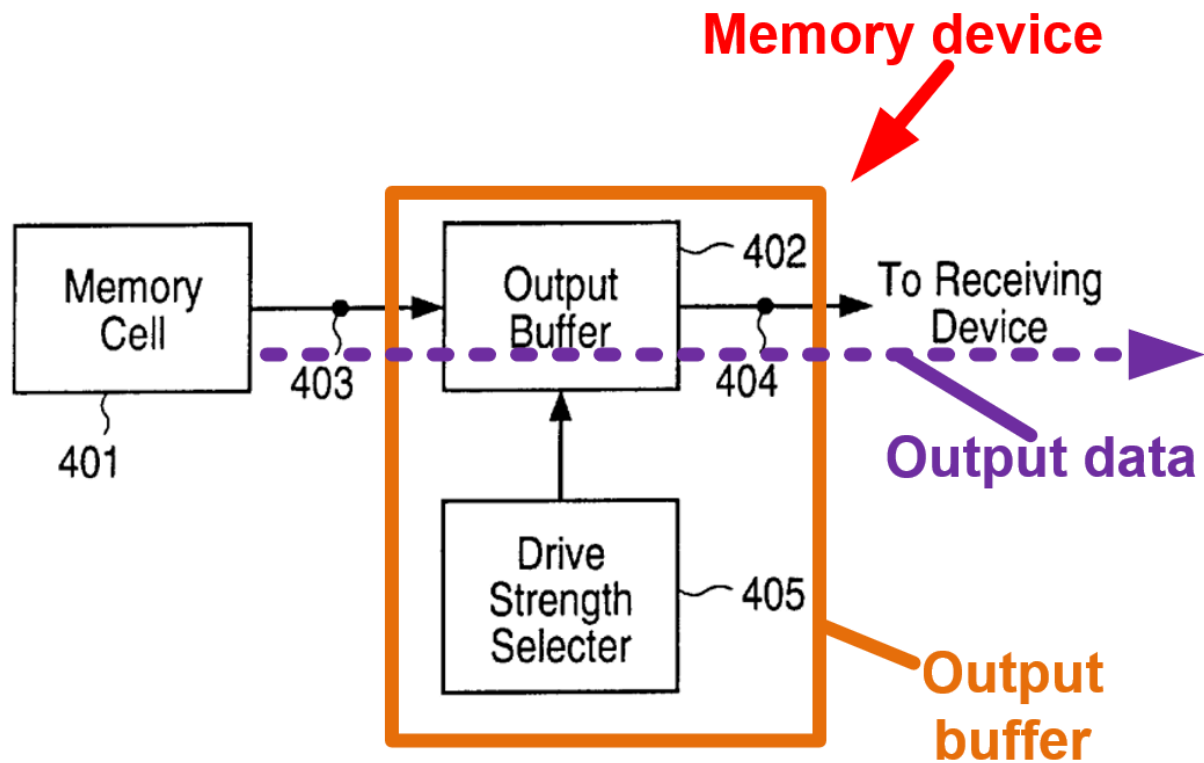


FIG. 4

EX1006, FIG. 4 (annotated).

Because the “drive strength selector (*sic*) 405” controls “output buffer 402” to operate at one of a set of possible output buffer drive strengths, Arcoleo describes a *configurable output buffer* that is configurable to one of a *plurality of*

output buffer drive strengths. EX1006, 6:10-65, FIG. 4; *cf.* EX1001, 19:64-67; EX1003, ¶127.

Claim [2]

The Ryu-Cole-Arcoleo combination renders obvious Claim [2]. EX1003, ¶128. As described above for Element [1c], *supra*, Cole describes an IC input section having a *configurable clock input buffer* that receives two strobe inputs 12 representing a *first clock input signal* (“xxStbP”) and a *second clock input signal* (“xxStbN”).¹² EX1005, [0019], [0020], [0026], FIGs. 1, 2A, 2C. Cole generally refers to *positive* signals using the letter “P” and *negative* signals using the letter “N,” including the *first clock input signal* “xxStbP” that represents a *positive clock input signal* and the *second clock input signal* “xxStbN” which represents a *negative clock input signal*. EX1005, [0017], [0019], [0026], [0027], FIGs. 2A, 2C; EX1003, ¶128.

Claim [3]

The Ryu-Cole-Arcoleo combination renders obvious Claim [3]. EX1003, ¶¶129-132. To the extent Ryu does not disclose a *first clock input signal* and a *second clock input signal* that represent *data latching clock signals*, the teachings of Cole demonstrate that such features were known and would have been obvious

¹² *Supra*, Footnote 3.

before the Critical Date of the '028 Patent. EX1004, [0003]-[0008], [0038], [0041]-[0045], [0059]-[0065], [0076]-[0079], FIGs. 4A-4B, 7, 12; EX1005, [0015]-[0028], FIGs. 1, 2A, 2C. For example, Cole explains that the input section 10 includes “latch banks 26” which “may be employed to latch and temporarily store the data being transferred to the IC.” EX1005, [0016]-[0020], [0023], [0024], [0029], FIGs. 1, 2B, 3; EX1003, ¶¶129-130. Cole’s *first clock input signal* (“xxStbP”) and *second clock input signal* (“xxStbN”) represent *data latching clock signals*, because xxStbP and xxStbN indicate the timing of signals received through data paths 27, thereby ensuring the data can be properly latched in latch banks 26.¹³ *Id*; EX1003, ¶¶130-131. For example, Cole’s input section 10 generates “strobe signals P and N 20 and 22” for output to pulse clock generator 24, which provides “latch banks 26 with enabling pulse clocks 28 to control their operations...in accordance with at least strobe signals P and N 20 and 22.” EX1005, [0017], [0019]; *see also id.*, [0015]-[0018], [0023], [0026], [0027], [0036], [0037], [0038], [0039], FIGs. 1-2B, 3.

Claim [4]

The Ryu-Cole-Arcoleo combination renders obvious [4]. EX1003, ¶¶133-135. For example, Ryu discloses that “output unit 530 is activated in response to an

¹³ *Supra*, Footnote 3.

enable signal CEB” and “outputs DATA[7:0] received from the selector 520 through an input/output pin.” EX1004, [0043], FIGS. 4A, 5, 7, 10B, 11. Because Ryu’s DATA[7:0] includes eight bits of data, it is apparent that the input/output pin (IOP) of Ryu includes at least eight ***common data ports*** each comprising ***1 bit*** so that the bits of DATA[7:0] can be output simultaneously. EX1003, ¶133. Ryu’s timing diagrams confirm that one data transfer of DATA[7:0] occurs at the IOP at a given time, meaning that a POSITA would have understood the IOP to include at least eight ***1 bit common data ports***. EX1003, ¶134. A POSITA also would have recognized that each of the other common data ports for receiving input data, command data, and address data (e.g., including IADD, SET, RESET, REB, CEB) would likewise comprise ***1 bit*** since Ryu’s timing diagrams consistently depict signaling in which 1 bit of data is transmitted per line at a time. *See e.g.*, EX1004, FIGS. 4A, 7, 10B, 12. Cole similarly describes common data input ports 27 that each comprise 1 bit. EX1005, [0016] (“latch bit data off input data paths 27”), [0023] (“capturing bit data received via data paths 27”), FIGs. 1, 2A-2C, 4; EX1003, ¶135.

Claim [10]

The Ryu-Cole-Arcoleo combination renders obvious Claim [10]. EX1003, ¶¶136-137. For example, in the combination, Ryu’s non-volatile memory device is modified to include an IC input section as described in Cole, and Cole explains that

the input section includes a “**configuration register**” that stores **configuration information** “one or more control bits.” EX1005, [0022] (“Configuration of input section 10 may be effectuated in any one of a number of manners, including but [] not limited to the setting of one or more control bits in a configuration register...”); *see also* EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, Elements [1c] and [1e]; *supra* §V.A.4. These one or more control bits can “cause the control signal Diffen to assume a value of ‘1’” to configure input section 10 to operate in the **differential signaling configuration**, and cause the control signal to assume “a value of ‘0’” to configure input section 10 to operate in the **single ended signaling configuration**. *Id.* EX1003, ¶¶136-137.

Claim [11]

The Ryu-Cole-Arcoleo combination renders obvious Claim [11]. EX1003, ¶¶138-139. For example, the Ryu-Cole-Arcoleo combination provides a **non-volatile memory device** including an **output buffer** configurable to one of a plurality of **output buffer drive strengths** to transfer output data. EX1006, 1:12-25, 1:37-2:11, 3:43-4:28, 6:10-65, 7:24-8:46, FIG. 4; *supra*, §V.A.4; EX1003, ¶138. This combination also provides a **configuration register** configured to store the **plurality of output buffer drive strengths** to be utilized by the **output buffer**. EX1006, 11:3-17 (“[e]ach possible drive strength can be associated with a

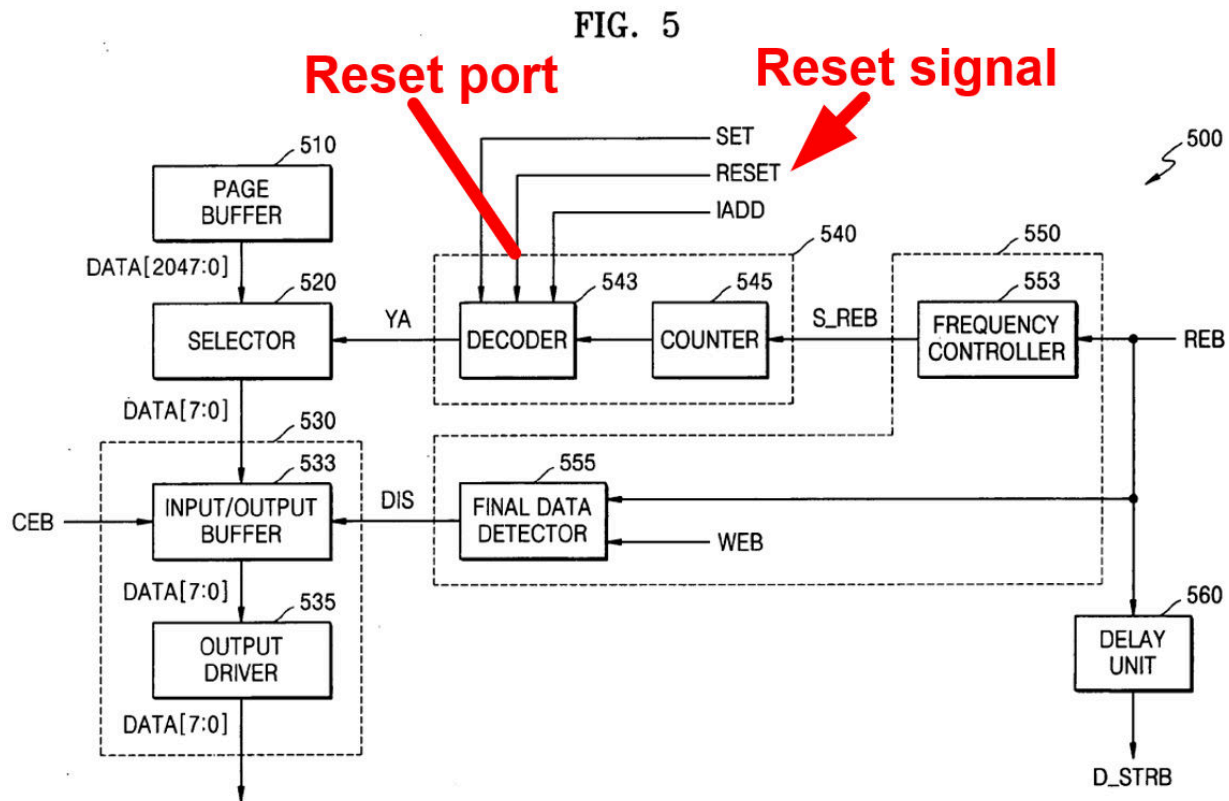
particular series of signals so that...a **register** or registers can be set, for example, in the memory device to identify a specified drive strength.” EX1003, ¶139.

Claim [12]

The Ryu-Cole-Arcoleo combination renders obvious Claim [12] for the reasons discussed above with respect to Element [1g]. *Supra*, Element [1g]; EX1003, ¶¶140-142.

Claim [13]

The Ryu-Cole-Arcoleo combination renders obvious Claim [13]. EX1003, ¶¶143-145. The ***non-volatile memory device*** of Ryu includes a ***reset port*** configured to receive a “***reset signal***” (RESET). EX1004, [0055], FIGs. 5, 11; EX1003, ¶143. This ***reset signal*** is input to a decoder 543, which also receives a “set signal” (SET). *Id.* Ryu expressly discloses that “[t]he decoder 453 is set or reset by a set signal SET or a reset signal RESET.” *Id.* The “decoder” of Ryu is part of the ***non-volatile memory device***. EX1004, [0054], [0055], [0057], FIGs. 5, 11. Accordingly, the “***reset signal***” is for resetting the ***configurable non-volatile memory device*** to a ***default configuration***. *Supra*, §V.A.4; EX1003, ¶143.



EX1005, FIG. 5 (annotated).

As another example, Cole explains that “the configuration register or the fuses may be configured to cause the control signal Diffen to assume a value of ‘1’ to configure input section 10 to operate in a differential signaling mode, and a value of ‘0’ to configure input section 10 to operate in a single-ended signaling mode.” EX1006, [0022]. EX1003, ¶144. If the device is initially set to the single-ended signaling configuration (Diffen=0) but has been subsequently changed to the differential-ended signaling configuration (Diffen=1), a POSITA would have understood a received signal that causes Diffen to revert to 0 for the single-ended signaling configuration to be a “*reset signal*” that resets the non-volatile memory

device to a default single-ended signaling configuration, for example. EX1003, ¶145; *supra*, §V.A.4.

Claim [14]

Supra, Element [13]; §V.A.4; EX1003, ¶146.

Claim [15]

The Ryu-Cole-Arcoleo combination renders obvious Claim [15]. EX1003, ¶147. Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of...***flash memory***,” which means that Ryu discloses that the ***non-volatile memory device*** can be a ***flash memory device***. EX1006, [0036]; *Supra*, §V.A.4; EX1003, ¶147 (citing corroboration EX1012, 2; EX1017, 17:4-17; EX1018, 1).

Claim [16]

The Ryu-Cole-Arcoleo combination renders obvious Claim [16]. EX1003, ¶¶148-149. Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of a...***flash memory***” and “the present invention can be embodied in various ***nonvolatile memory devices*** including, but not limited to, a ***NOR device***.” EX1004, [0036]. EX1003, ¶148. Ryu thus discloses or plainly suggests implementations of the configurable ***non-volatile memory device*** as a ***NOR flash memory device***. *Supra*, §V.A.4; EX1003, ¶149 (citing corroboration EX1031, 1; EX1021, 3:20-3; EX1022, 5:18-30).

Claim [17]

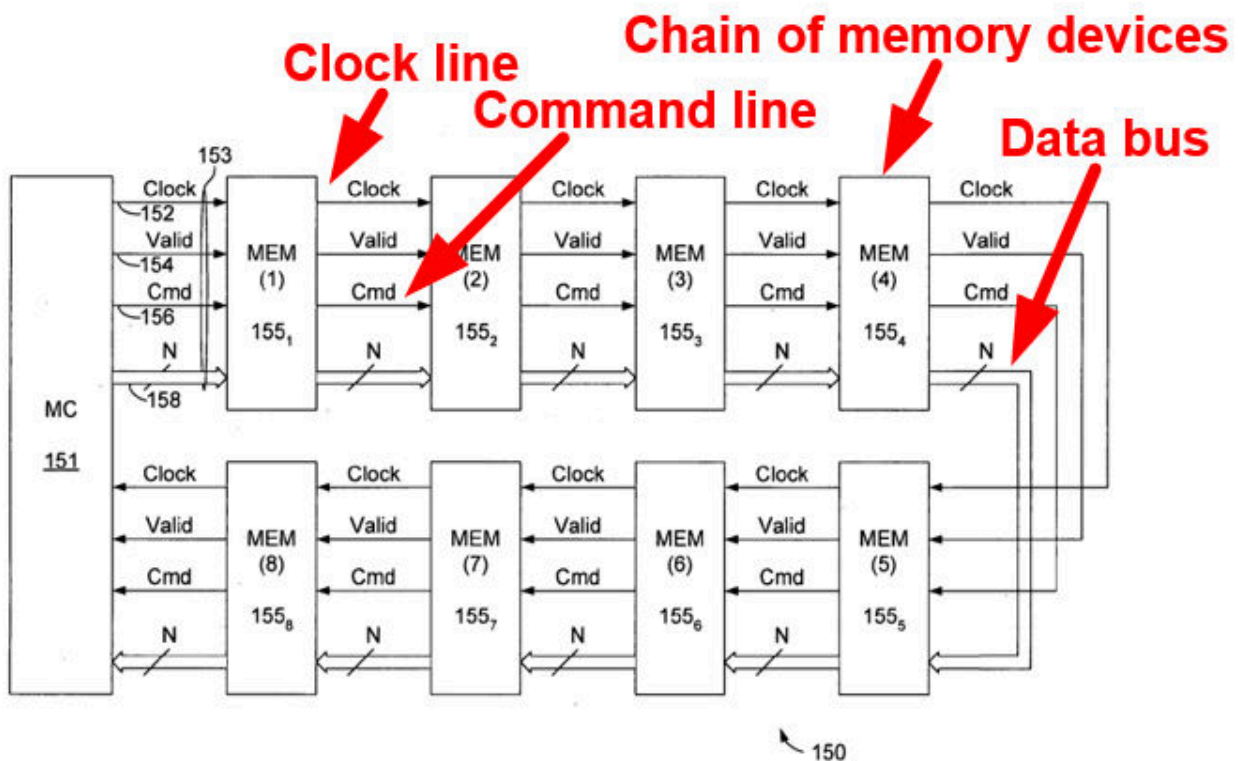
The Ryu-Cole-Arcoleo combination renders obvious Claim [17]. EX1003, ¶150. Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of a *NAND flash memory*” and “the present invention can be embodied in various *nonvolatile memory devices*,” meaning that Ryu discloses or plainly suggests implementations of the configurable *non-volatile memory device* as a *NAND flash memory device*. EX1004, [0036]. EX1003, ¶150 (citing corroboration EX1021, 3:20-31; EX1022, 5:18-30).

B. GROUND 1B: Obviousness Based on Ryu-Cole-Grundy-Arcoleo (Claims 1-4 and 10-17)

1. Grundy

Grundy discloses a “memory system” that includes a “set of memory devices” that are “coupled to one another in chain.” EX1009, [0035], *see also id.*, [0030], [0036]-[0059], FIGs. 3-7E; EX1003, ¶60. Each memory device in the chain includes a “signaling interface” and a “storage array,” the signaling interface “being used to receive and transmit data and commands propagating through the chain of memory devices.” *Id.* The storage arrays can include “nonvolatile storage arrays.” *Id.* Grundy explains that the chain of memory devices communicate by “signaling links” that connect each memory device to other memory devices and a memory controller. EX1009, [0043], *see also id.*, [0030], [0044], [0047]-[0059],

[0084], [0085], FIGs. 5A-7E, 17. These signaling links include a “clock line” that carries clock signals, a “command line” that carries command signals, “multi-purpose lines” that carry data is stored by the storage arrays, and a “valid line” indicating whether a valid command or data signal is being transmitted. *Id.*



EX1009, FIG. 1 (annotated).

Every memory device in Grundy’s chain includes a clock input (“Clock In”) that receives a clock signal from a prior device in the chain and a clock output (“Clock Out”) that forwards clock signals to the next device in the chain. EX1009, [0084]-[0091], FIG. 17; EX1003, ¶61. This clock signal is used to control latching

operations in the command lines and data lines, which likewise have inputs and outputs on each memory device. *Id.*

2. The Ryu-Cole-Grundy-Arcoleo Combination

As described above, it would have been obvious to implement Ryu's memory device to include an input section that receives complementary strobe input signals as taught by Cole. EX1003, ¶62; *supra*, §V.A. Ryu further explains that "[a] controller...for controlling the non-volatile memory device applies a read control signal REB to the non-volatile memory device to receive data during a read operation" and "a D_STRB signal may be created by delaying the read control signal REB by a predetermined delay time and output at the same time with the data DATA[7:0] to the external source." EX1009, [0005], [0064], FIG. 5.

In co-pending litigation involving the '028 Patent, the Patent Owner has pointed to a "strobe" signal as a "clock" signal in its infringement contentions against Petitioner. *See* EX1100, 52-53; EX1101, 21-28; EX1102, 17-21; *supra*, Footnote, 3. However, the term "clock" signal is distinguished from a "strobe" signal in that a "clock" signal, for example, represents a *continuous* periodic signal for synchronizing timing. EX1003, ¶63. Because the periodic behavior of conventional "strobe" signals is not continuous, they are not "clock" signals under this interpretation. *Id.* In particular, a "strobe" signal toggles only when data is present on a corresponding input or output line to which the strobe signal is

synchronized. *Id.* However, during times when no data is transferred, the periodic strobe signal is discontinued (e.g., it is held at a constant signal level). *Id.*

Even under this interpretation of “clock” signal, the claimed clock input and output signals still would have been obvious to a POSITA when the Ryu-Cole-Arcoleo combination is further considered in view of Grundy. EX1003, ¶64. This is because Grundy teaches the conventional alternative option of synchronizing data input to and outputted by a memory device to a continuous clock signal in lieu of a discontinuous strobe signal. EX1003, ¶64. For example, Grundy disclose the following:

[T]he memory controller 151 outputs a **free-running clock signal** 172₁ on the clock line 152 coupled between the memory controller 151 and the initial memory device 155₁. **The clock signal 172₁ may also be a strobe signal that is toggled only when data and/or commands are being transmitted on the point-to-point link 153.** When command or data values are to be transmitted on the signaling queue ..., the memory controller 151 simultaneously asserts a valid signal 174₁ on the valid line 154 (and a command signal 176₁ on command line 156 if a command is being transmitted) and drives a first value, A, onto the bus 158, both in response to an edge 167 of the clock signal 172₁. The memory controller 151 continues to assert the valid signal 174₁ (and command signal if appropriate) as subsequent values B, C, D, E, and F are transmitted on to the bus 158 in successive transmit intervals.

EX1009, [0047].

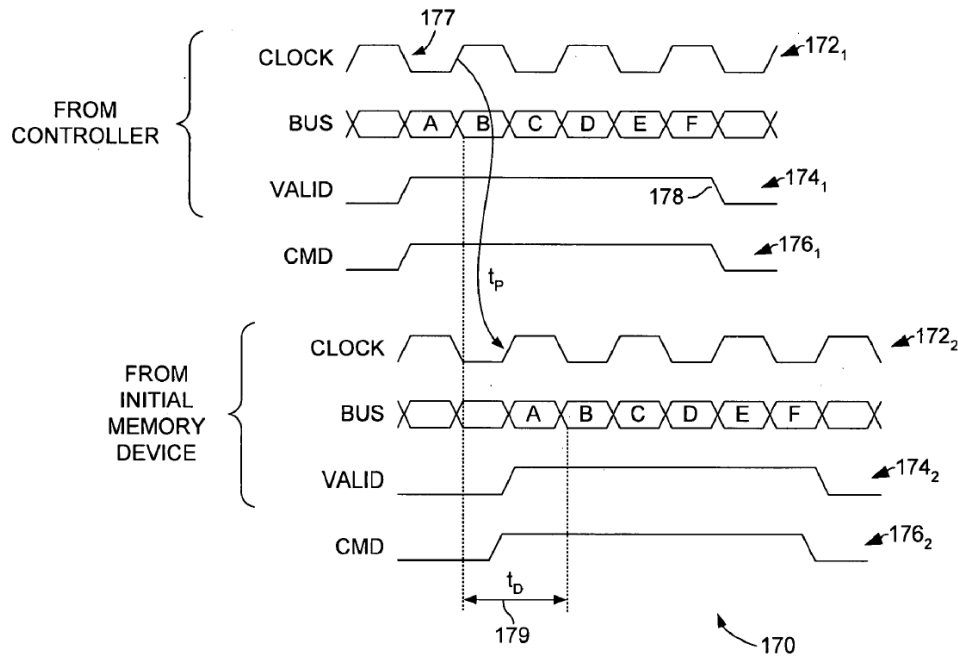


FIG. 6

EX1009, FIG. 6.

In other words, Grundy teaches that a free-running clock signal can be used in place of a discontinuous strobe signal if separate control lines (such as the VALID or CMD lines) are provided to indicate when data is and is not present on the bus. EX1003, ¶66. A POSITA would have found it obvious and would have been motivated to further modify the Ryu-Cole-Arcoleo combination to implement a timing scheme for data transfers using continuous clock signals rather than discontinuous probe signals for multiple reasons. In the resulting Ryu-Cole-Arcoleo-Grundy combination, the discontinuous strobe inputs (e.g., xxStbP and

xxStbN) and strobe output signal (e.g., D_STRB) in the resulting combination would be implemented as continuous clock signals where the presence/absence of data is separately indicated on separate control lines (e.g., VALID and/or COMMAND lines). EX1003, ¶¶66-67.

First, a POSITA would have considered the option of implementing either continuous clock signals (with corresponding control lines) or discontinuous strobe signals to be an obvious design choice and simple substitution. EX1003, ¶68. As Grundy explains, there were primarily just two known, predictable alternatives for signaling data timing information, and a POSITA would have selected one alternative or the other to meet the demands of a given application or design, as both were obvious to try. *Id.*, EX1009, [0047], FIG. 6. For example, a POSITA would have appreciated that a continuous clock signal is often beneficial when the memory device is already configured to receive and transfer the clock signal as part of a serially chained memory system like Grundy's, as this scheme obviates the need for separate (semi) periodic strobe signals, which can reduce cost and complexity in the circuitry. EX1003, ¶68. Discontinuous strobe signals, on the other hand, are often preferable to reduce the number of signaling lines needed for timing data transfers since strobe signals do not require separate control signal lines (e.g., VALID, COMMAND signals) to indicate when data is being transferred. *Id.*

Second, a POSITA would have found it obvious to implement continuous clock signals for data timing according to Grundy's suggestion because Ryu and Cole invite alternative timing schemes. EX1003, ¶69. For example, Ryu discloses alternative embodiments in which D_STRB is already a delayed version of a "flash clock signal" rather than the discontinuous REB signal. EX1004, [0072]-[0082], FIGs. 9-11. Cole likewise describes alternatives for the strobe inputs 12 to be provided "in parallel with the data (requiring no extraction) or interleaved with the data (requiring extraction)." EX1006, [0020]. These examples indicate that the substitution of discontinuous strobe signals for a continuous clock is fully compatible with the range of timing schemes contemplated by each of Ryu and Cole. EX1003, ¶69.

Third, because Grundy discloses a memory system having a chain of serially connected memory devices, a POSITA would have been motivated to implement Ryu's non-volatile memory device with clock input ports and clock output ports as taught by Grundy so every memory device in a chain receives a clock signal to govern internal latching operations. EX1003, ¶70.

Fourth, a POSITA would have understood that implementing Ryu's non-volatile memory device as one of a chain of memory devices connected to a controller as taught by Grundy would improve a processing speed and scalability of the memory system. EX1003, ¶71.

Fifth, a POSITA would have been motivated to implement the non-volatile memory device of Ryu-Cole-Arcoleo with multiple common data ports as taught by Grundy, because this would result in the non-volatile memory device processing data at a higher rate. EX1003, ¶72.

Sixth, a POSITA would have found it obvious to combine the teachings of Ryu-Cole-Arcoleo with Grundy because the combination merely involves the application of a known technique to a known system to achieve predictable results. *KSR* at 417; *Intel Corp* at 1380-81. A POSITA would have reasonably expected success in making this combination. EX1003, ¶73.

3. Application to Challenged Claims

Element [1pre]

Supra, Ground 1A (§V.A.5) at Element [1pre]. EX1003, ¶151.

Element [1a]

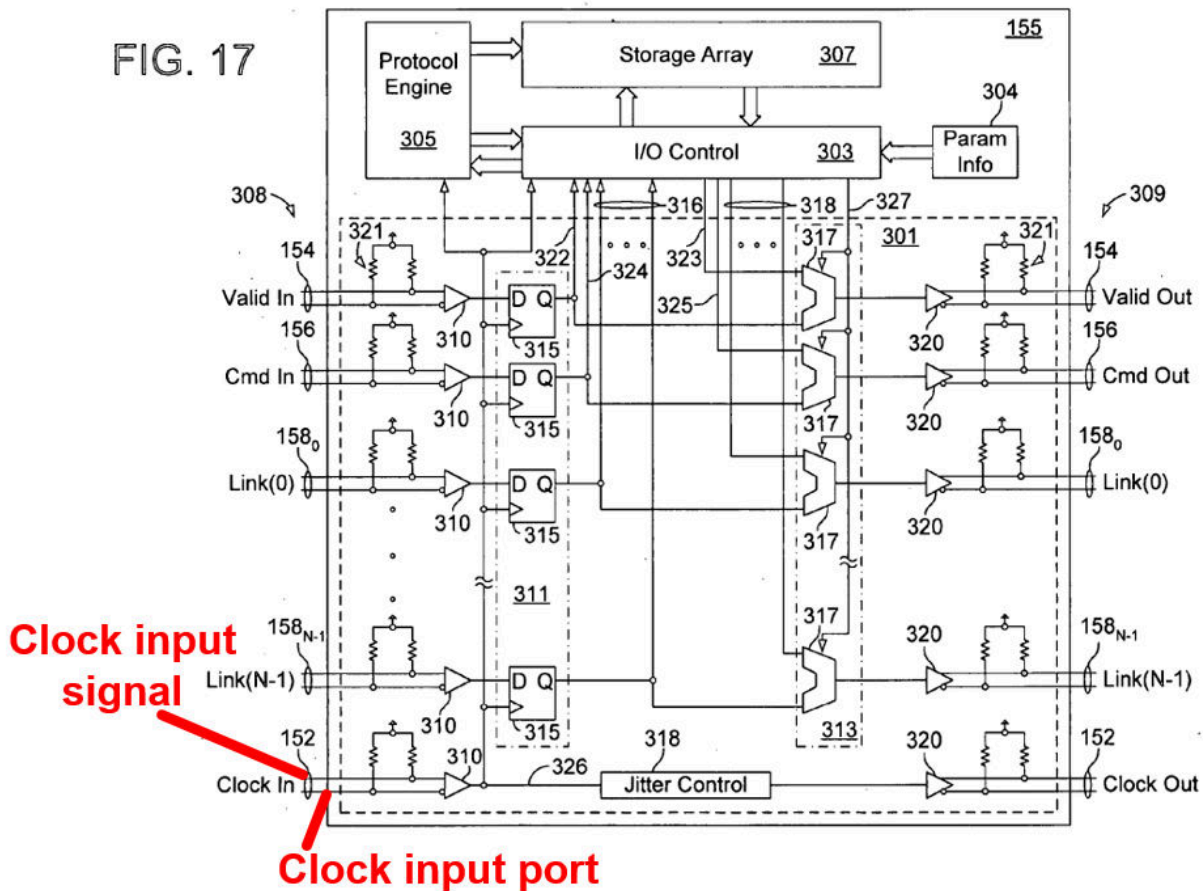
Supra, Ground 1A (§V.A.5) at Element [1a]. EX1003, ¶152. Grundy further underscores the obviousness of [1a]. EX1003, ¶¶152-153. For example, Grundy explains that a “*memory device*” includes an “actual storage array.” EX1009, [0084], *see also id.*, [0033], [0035], [0062], [0073], [0079], [0081], [0082], [0090]-[0094], FIGs. 3, 17. Grundy also explains that the storage array can “include multiple sub-arrays.” *Id.* Referring to storage arrays, Grundy explains that “block size” and a “number of memory banks” is one aspect of the storage array in the

Element [1b]

Supra, Ground 1A (§V.A.5) at Element [1b]. EX1003, ¶154.

Element [1c]

Supra, Ground 1A (§V.A.5) at Element [1a]. EX1003, ¶155. Grundy further underscores the obviousness of [1c]. EX1003, ¶¶155-157. For example, Grundy discloses a **non-volatile memory device** that is “coupled to [an] input-side clock line.” EX1009, [0088], *see also id.*, [0043], [0047], [0054], FIG. 17. Therefore, Grundy’s **non-volatile memory device** includes a **clock input port** that receives a **clock input signal**. *Id.* EX1003, ¶155.



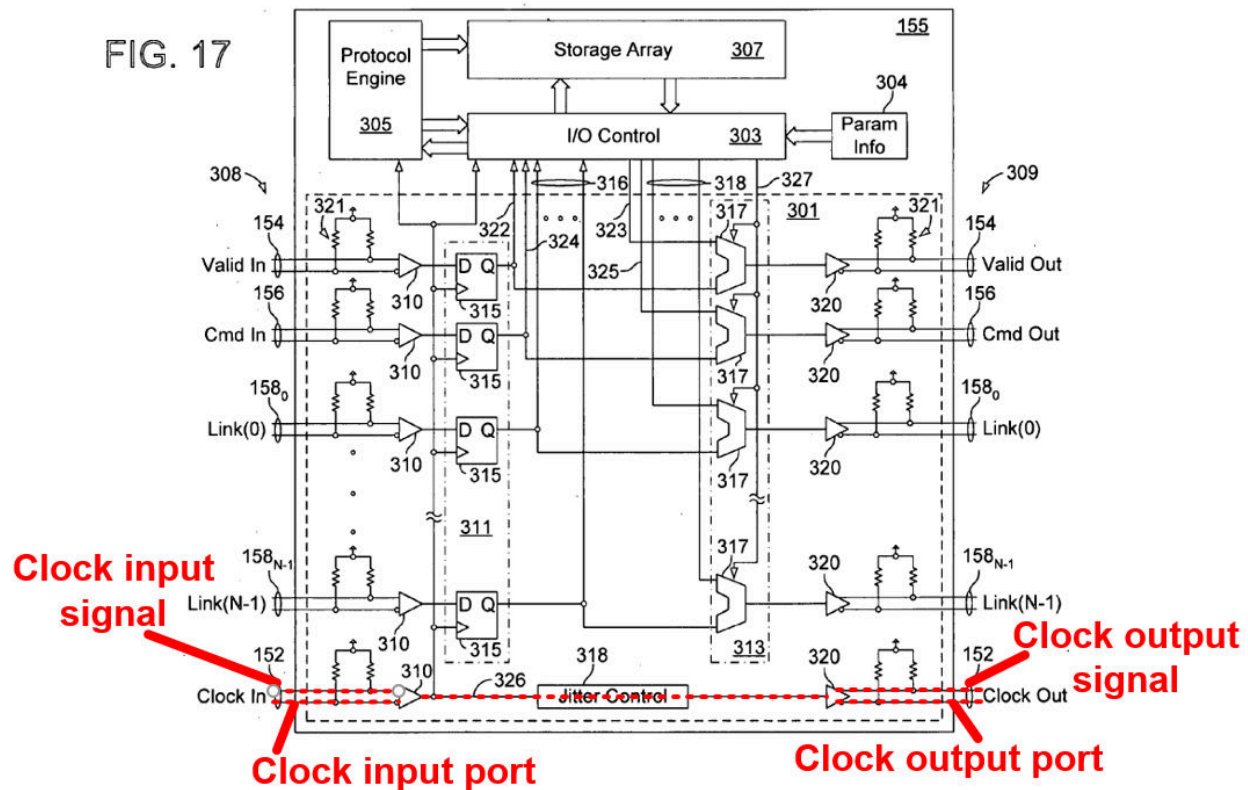
EX1009, FIG. 17 (annotated).

Grundy explains that the *memory device* 155 uses this *clock input signal* received via the *clock input port* to control storage elements 315 to capture data on lines 154, 156, and 158 in “double-data rate” configuration in response to rising edges and falling edges of the *clock input signal*. EX1009, [0088], FIG. 17. The Ryu-Cole-Arcoleo combination of Ground 1A provides input ports for receiving a pair of complementary input strobe signals 12 (e.g., xxStbP, xxStbN). *Supra*, §V.A.5 at [1c]. As described above in the overview of the Ryu-Cole-Grundy-Arcoleo combination, it would have been obvious in view of Grundy to transform these input strobe signals 12 to continuous clock input signals such that the combination renders obvious a *first clock input port* configured to receive a *first clock input signal* and a *second clock input port* configured to receive a *second clock input signal*. EX1009, [0047], FIG. 6; EX1003, ¶¶156-157; *supra*, §IV.A.4.

Element [1d]

Supra, Ground 1A (§V.A.5) at Element [1d]. EX1003, ¶158. Grundy further underscores the obviousness of [1d]. EX1003, ¶¶158-161. For example, Grundy explains that the memory device 155 is coupled to an “input-side clock line” and an “output-side clock line,” with a “logic level clock signal” passing between a clock input and a clock output. EX1009, [0088], *see also id.*, [0043], [0047]-[0054], [0084], [0085], FIG. 17; EX1003, ¶¶158-159. Grundy expressly discloses

that the “logic level clock signal 326 is generated by the signal receiver 310 coupled to the input-side clock line 152,” and that “[t]he clock signal 326 is additionally provided to the output driver 320 coupled to the output-side clock line 152 to drive the outgoing clock signal.” *Id.* This means that according to Grundy, the memory device 155 includes a **clock output port** configured to transfer a **clock output signal** that is referenced to a **clock input signal**. *Id.*



EX1009, FIG. 17 (annotated).

Grundy also explains that the memory device 155 represents one of a set of “chained memory devices” of a “chained memory system.” EX1009, [0043], *see also id.*, [0044]-[0083], FIGs. 5A-16; EX1003, ¶160. A “clock line 152” passes

through each of these chained memory devices. *Id.* This is because each memory device in the chain includes a clock input port for receiving a clock input signal and a clock output port for transferring the clock output signal. *Id.*

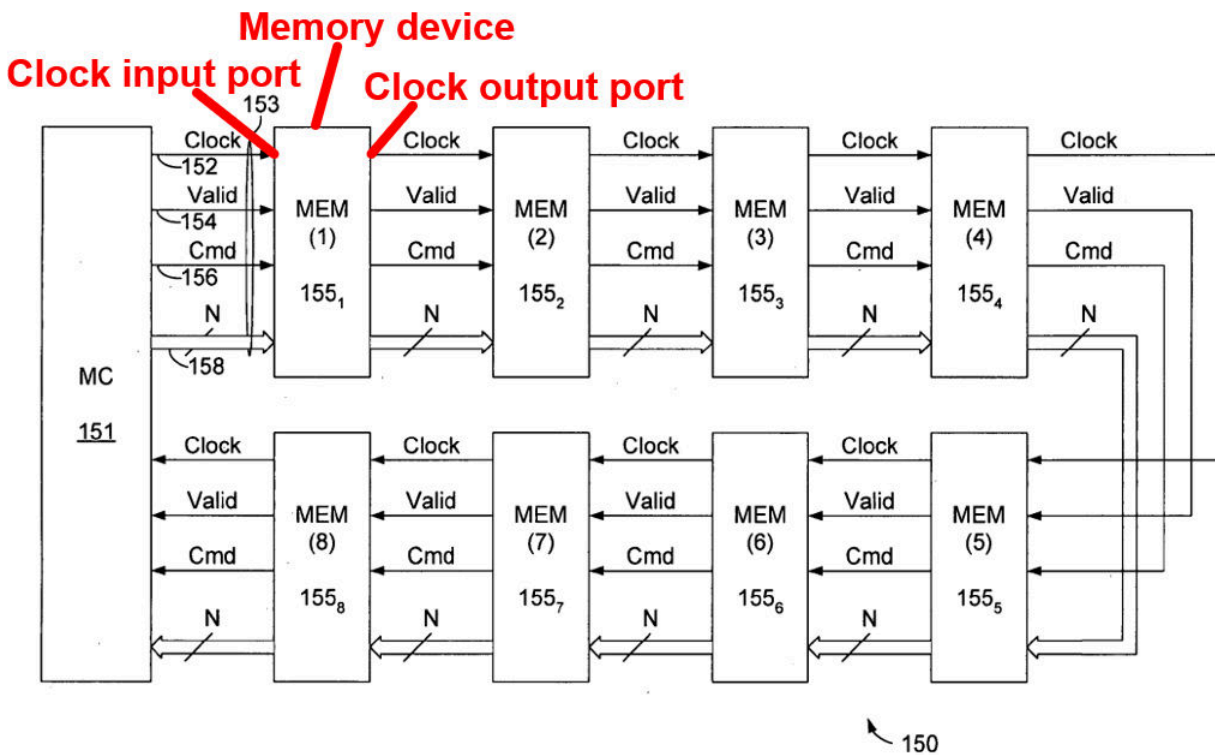


FIG. 5A

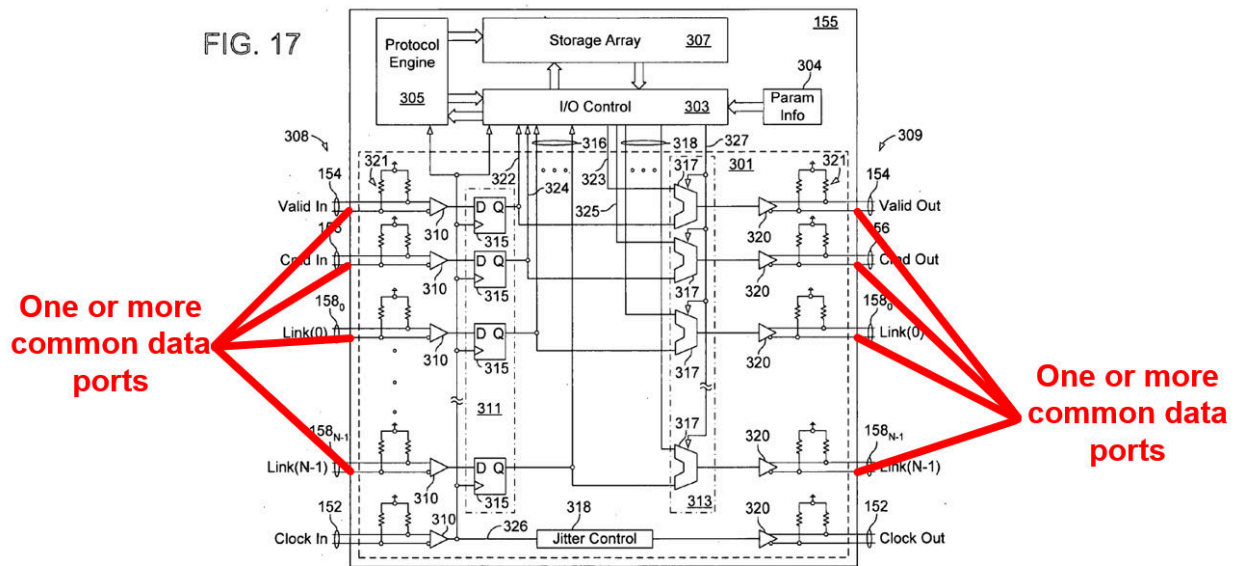
EX1009, FIG. 5A (annotated).

When the non-volatile memory device of the Ryu-Cole-Arcoleo combination is implemented to include a clock line that passes through the device, as suggested by Grundy, the resulting non-volatile memory device includes a **clock output port** configured to transfer a **clock output signal** that is referenced to a **first clock output signal**. EX1003, ¶161; §V.B.2. As another example, as described

above, it would have been obvious to further modify Ryu's D_STRB to be a continuous clock output signal based on Grundy's teaching to use a continuous clock signal for synchronizing data transfer. APPLE-1009, [0047], FIG. 6; EX1003, ¶161; *supra*, §IV.A.4.

Element [1e]

Supra, Ground 1A (§V.A.5) at Element [1e]. EX1003, ¶162. Grundy further underscores the obviousness of [1e]. EX1003, ¶¶162-164. For example, Grundy explains that the ***memory device*** 155 is connected to a clock line, a valid line, and a command line that are “used to conduct a clock signal, a valid signal, and a command signal, respectively.” EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17. EX1003, ¶¶162-163. Grundy also explains that memory device 155 is connected to “a set of N multi-purpose lines” that are “used at alternate times to transfer N-bit wide data values and command values and are referred to collectively herein as a bus.” *Id.* According to Grundy, the command signal is used to “indicate whether a valid ***command*** or ***data*** value is being transmitted on the multi-purpose lines,” and the command signal is used to indicate that “the value transmitted on the multipurpose lines is a ***command*** (which may include ***address*** information).” *Id.*



EX1009, FIG. 17 (annotated).

As depicted in FIG. 17 of Grundy, the clock line, the valid line, and the command line, and the multi-purpose lines each pass through the memory device from an input to an output. EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17. EX1003, ¶164. When memory device 155 is part of a chain of serially connected memory devices, these lines each transfer a **common data signal** from a device preceding memory device 155 in the chain to a device following the memory device 155 in the chain. *Id.* Consequently, memory device 155 includes **one or more common data ports** configured to transfer **common data signals**.

Element [1f]

Supra, Ground 1A (§V.A.5) at Element [1f]. EX1003, ¶165.

Element [1g]

Supra, Ground 1A (§V.A.5) at Element [1g]. EX1003, ¶166.

Claim [4]

Supra, Ground 1A (§V.A.5) at Element [1g]. EX1003, ¶167. Grundy further underscores the obviousness Claim [4]. EX1003, ¶¶167-168. For example, Grundy discloses ***one or more common data ports*** including ports for a “valid line,” ports for a “command line,” and ports for “multipurpose lines,” among other ports. EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17; EX1003, ¶167. Grundy explains that memory device includes “a set of N multi-purpose lines” and “multi-purpose lines 158 are used at alternate times to transfer N-***bit*** wide data values and command values.” EX1009, [0043], [0044], *see also id.*, [0051], [0061] . Thus, each of the N multi-purpose lines handle ***1 bit***, and the ***one or more common data ports*** therefore each comprise ***1 bit***. Grundy further discloses that “signals transmitted on the N signal lines that form the bus may alternatively be time-multiplexed onto a smaller number of signal lines” and describes that a serializer circuit can be provided “to serialize an N-bit transmission onto a single differential signal line.” EX1009, [0051].

Furthermore, Grundy explains that the valid signal and the command signal can be asserted at a high logic level or a low logic level, which means that the ***one or more common data ports*** that transfer these signals each comprise ***1 bit*** (e.g., a

“0” for the low logic level and a “1” for the high logic level). EX1009, [0043].

Grundy explains that the valid line, the memory line, and each multi-purpose line is connected to a “differential receiver 310” that judges the logic level of the line and an “output driver 320” that generates a binary signal having a high or low logic value. EX1009, [0086]-[0088], FIG. 17; EX1003, ¶168. Consequently, when the *non-volatile memory device* of the Ryu-Cole-Arcoleo combination is implemented with the *one or more common data ports* of Grundy, the *one or more common data ports* each comprise *1 bit*. *Id.*

Claims [2], [3], and [10]-[17]

The Ryu-Cole-Grundy-Arcoleo combination renders obvious claims [2], [3], and [10]-[17] for at least the reasons described for the Ryu-Cole-Arcoleo combination (Ground 1A (§V.A.5) at [2], [3], and [10]-[17], *supra*); EX1003, ¶169.

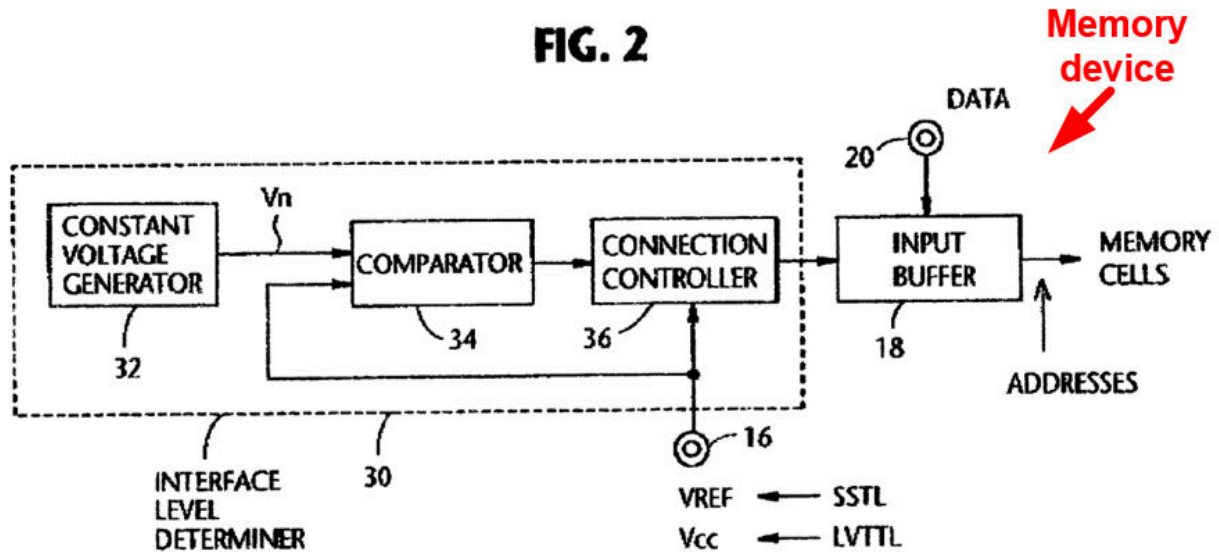
C. GROUND 1C: Obviousness Based on Ryu-Cole-Grundy-Arcoleo-Akashi (Claims 5-9)

1. Akashi

Akashi discloses a memory device comprising a data pin and one or more memory cells. EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2; EX1003, ¶74.

Akashi’s memory device includes an input buffer that judges data received at the data pin as “a high or a low logic level.” EX1008, 2:8-24, *see also id.*, 1:14-25

(“[i]nput buffers or receivers...should recognize whether a voltage is intended to be a high or a low voltage”), 2:41-63, 4:4-34, FIG. 2. After judging the data as a high or low logic level, the input buffer transfers the data to the one or more memory cells. EX1008, FIG. 2.



Akashi’s memory device further includes an “interface level determiner” connected to an “external terminal” for receiving a “reference voltage VREF.” EX1008, 3:49-58, FIG. 2; EX1003, ¶75. The interface level determiner generates an output value based on the reference voltage VREF for sending to the input buffer, and the input buffer can use this output value to compare with the data received via the data input pin to determine whether the data is the high logic level or the low logic level. EX1008, 1:54-2:24, 3:49-4:34, FIG. 2. The input buffer can

use the stub series terminate logic (SSTL) specification to judge the input data, meaning that “all voltages higher than (VREF+0.4) volts are determined as a high voltage, and all voltages lower than (VREF-0.4) volts are recognized as a low voltage.” EX1008, 1:26-43.

2. The Ryu-Cole-Arcoleo-Akashi Combination

A POSITA seeking to implement circuitry to judge inputted signal levels would have looked to references like Akashi for details on known solutions to the problem of judging signal logic levels. EX1003, ¶76. For example, as described above, Akashi describes the conventional option of an input buffer that determines logic levels of inputted data signals according to the SSTL specification. EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2; EX1003, ¶76. Multiple reasons would have prompted a POSITA to implement input buffer circuitry for judging input signal levels in the Ryu-Cole-Arcoleo non-volatile memory device based on Akashi’s teachings. EX1003, ¶76.

First, a POSITA would have been motivated to implement the non-volatile memory device of the Ryu-Cole-Arcoleo combination to include an input buffer that is configured to judge input data as a high logic level or a low logic level as suggested by Akashi, because doing so would readily allow the non-volatile memory device to process binary data such as a bit stream of “1s” and “0s.” EX1003, ¶77. Because memory devices handle large volumes of binary data, a

POSITA would have recognized that it is beneficial for an input buffer to determine the binary values of input data so that the correct data values can be saved to the memory banks or otherwise processed. EX1003, ¶77.

Second, a POSITA would have understood that using a reference voltage and a buffer zone to differentiate between a high logic level and a low logic level, as suggested by Akashi, provides a straightforward solution to identifying data bits while ignoring baseline noise. EX1003, ¶78. For example, Akashi explains that “the SSTL specification dictates that all voltages higher than (VREF+0.4) volts are determined as a high Voltage, and all Voltages lower than (VREF-0.4) volts are recognized as a low voltage.” EX1008, 1:26-44. A POSITA would have appreciated that this would result in baseline noise not being misjudged as a high or low data bit, therefore improving the accuracy of judged data bits received at the device. EX1003, ¶78.

Third, it would have been obvious to implement the non-volatile memory device of the Ryu-Cole-Arcoleo combination such that the input buffer supports terminated signaling including SSTL as taught by Akashi to promote signal integrity in high-speed signaling environments. EX1003, ¶79.

Fourth, a POSITA would have understood that implementing the non-volatile memory device of the Ryu-Cole-Arcoleo combination so that each common data signal received by the memory device is judged by a respective

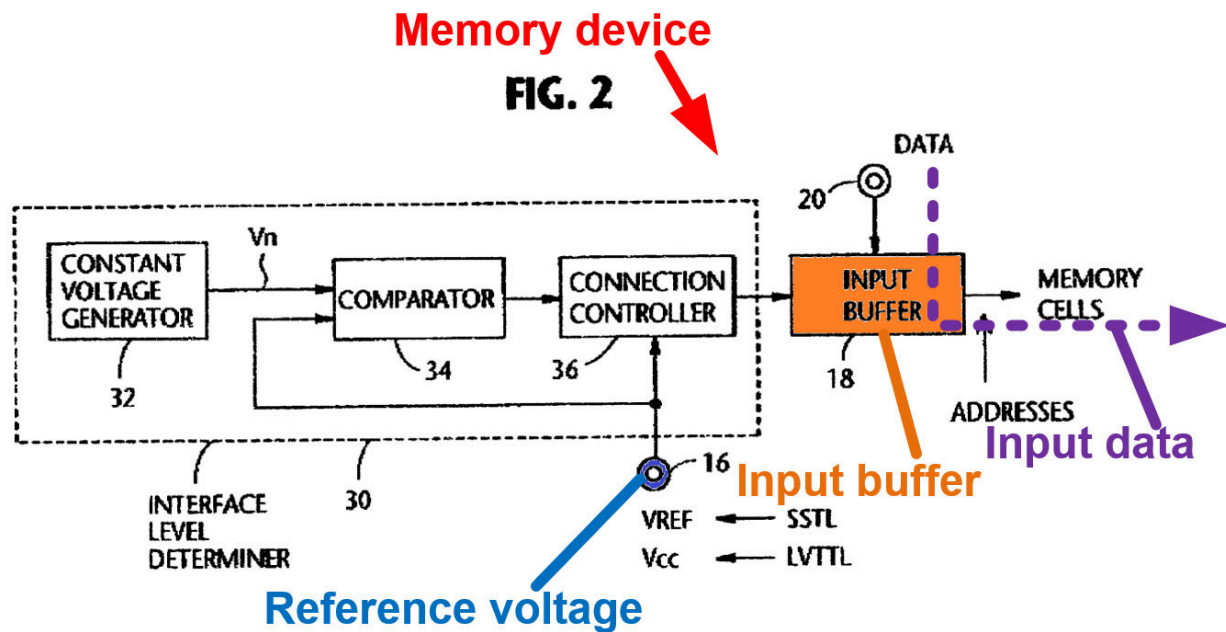
configurable input buffer have a high or low logic level, as taught by Akashi, would yield predictable benefits. EX1003, ¶80.

Fifth, a POSITA would have found it obvious to combine the teachings of Ryu-Cole-Arcoleo with Akashi because the combination merely involves the application of a known technique to a known system to achieve predictable results. *KSR* at 417; *Intel Corp* at 1380-81. A POSITA would have reasonably expected success in making this combination. EX1003, ¶81.

3. Application to Challenged Claims

Claim [5]

The Ryu-Cole-Arcoleo-Akashi combination renders obvious Claim [5]. EX1003, ¶¶170-175. To the extent that Ryu’s “*input/output buffer*” is not configurable to utilize a *reference voltage* for determining logic levels of *common data signals*, Akashi provides these features. EX1004, [0003], [0005]-[0007], [0041]-[0043], [0058]-[0062], [0076]-[0078], [0090], FIG. 5; EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2; EX1003, ¶170. For example, Akashi describes a memory device including an “*input buffer 18*” that receives *input data* via a “data pin 20,” and transfers this input data to “memory cells.” EX1008, 2:8-17, FIGs. 1-2.



EX1008, FIG. 2 (annotated).

The data received by the *input buffer* 18 via data input pin 20 and forwarded to the “memory cells” represents a *common data signal* that is that is substantially similar to data described by the ’028 Patent. EX1008, 1:58-2:25; cf. EX1001, 3:37-67, 5:26-58, 10:42-11:18, FIG. 3B. Akashi’s *input buffer* 18 is connected to an interface level determiner 30 that receives a *reference voltage* (VREF). EX1008, 2:8-34 (“[w]hen the memory chip dedicated to SSTL levels is used, a *reference voltage* VREF is applied to an external terminal 16”), 3:49-34, FIGs. 1, 2; EX1003, ¶171. Akashi also discloses that “it is assumed that a reference voltage VREF utilized for SSTL mode is about 1.5 volts” and “VREF applied to the pin 16 is routed to the input buffer 18 via the connection controller 36.” EX1008, 4:3-21. According to Akashi, the input buffer 18 uses this *reference voltage* VREF for

determining *logic levels* of *common data signals* including input data received by data input pin 20. EX1008, 1:26-43 (“voltages higher than (VREF +0.4) volts are determined as a high voltage, and all voltages lower than (VREF -0.4) volts are recognized as a low voltage”), 2:8-17 (“voltages applied to the buffer 18 via a data input pin 20 are recognized as a high or a low logic level using the reference voltage VREF (viz., at SSTL levels) as mentioned above”). EX1003, ¶172.

The *input buffer* 18 of Akashi is *configurable* to judge a stub series terminated logic (SSTL) signal or a low voltage transistor-transistor logic (LVTTL) signal received by the data input pin 20. EX1008, 1:14-2:34, 2:41-63, 4:3-34, FIG. 2; *cf.* EX1001, 8:8-30, 10:10-27, 13:50-14:24, FIG. 5. EX1003, ¶173. Akashi also explains that “[w]hen the user intends a memory device at SSTL mode in accordance with the manufacture’s (*sic*) instructions, he or she applies VREF to the pin 16” and “when the user intends a memory device at LVTTL mode in accordance with the manufacture’s (*sic*) instructions, he or she applies Vcc to the pin 16,” further confirming that *input buffer* 18 is *configurable*. EX1008, 4:3-22. EX1003, ¶¶174-175.

Claim [6]

The Ryu-Cole-Arcoleo-Akashi combination renders obvious Claim [6]. EX1003, ¶176. Akashi expressly discloses that the *reference voltage* VREF can be set to a *predetermined voltage level* such as 1.5 volts. EX1008, 4:3-14 (“a

reference voltage VREF utilized for SSTL mode is about 1.5 volts...VREF applied to the pin 16 is routed to the input buffer 18 via the connection controller 36”), *see also id.*, 2:8-17. When “the user intends a memory device at LVTTTL mode,” Akashi explains that the user “applies Vcc to the pin 16” and “the power source Vcc is about 3.3 Volts,” meaning that the **reference voltage** is also set to a **predetermined voltage level** in this embodiment. EX1008, 4:3-22; EX1003, ¶176.

Claim [7]

The Ryu-Cole-Arcoleo-Akashi combination renders obvious Claim [7]. EX1003, ¶177. Akashi expressly discloses that “it is assumed that a reference voltage VREF utilized for SSTL mode is about 1.5 volts and that the power source Vcc is about 3.3 Volts.” EX1008, 4:3-14. Akashi also discloses that “the SSTL specification dictates that all voltages higher than (VREF +0.4) volts are determined as a high Voltage, and all Voltages lower than (VREF -0.4) volts are recognized as a low voltage.” EX1008, 1:26-44. This means that a data bit of a **common data signal** having value more than 0.4 volts greater than the **predetermined voltage** is judged to be at the **high logic level**, meaning that any value greater than 1.9 volts is judged to be the **high logic level** when the **predetermined voltage** is 1.5 volts as suggested by Akashi. EX1003, ¶177. In examples where high bits of the **common data signal** have a high value of 3.0

volts, this means that the *predetermined voltage* of 1.5 volts is half of the *high logic level* of the *common data signal*.

Claim [8]

The Ryu-Cole-Arcoleo-Akashi combination renders obvious Claim [8]. EX1003, ¶¶178-179. Akashi expressly discloses a memory device that operates “at SSTL levels,” referring to “stub series *terminated* logic.” EX1008, 1:26-2:34, 2:41-63, 4:3-14, 4:23-34, FIG. 2. When Akashi’s memory device uses *terminated* logic, signals input to the memory device represent a *terminated signal* to improve performance of the device. *Id.* Thus, a POSITA would have been motivated to implement the *non-volatile memory device* of the Ryu-Cole-Arcoleo combination to include *terminated signals* (e.g., according to the SSTL specification) as suggested by Akashi. *Supra*, §V.C.2; EX1003, ¶178. It would have been understood and obvious to a POSITA that a *non-volatile memory device* implementing SSTL as taught in Akashi would use *terminated signals* for the *first clock input signal*, the *second clock input signal*, and the *common data signal* because SSTL calls for *terminated signals*. EX1008, 1:26-43; *supra*, §V.C.2; EX1003, ¶179 (citing corroboration EX1019, 3; EX1020, 13:35-14:48).

Claim [9]

Supra, Claim [8]. EX1003, ¶180.

VI. GROUND 1D: Obviousness Based on Ryu-Cole-Arcoleo-Akashi (Claims 5-9)

For each of the reasons detailed above in Ground 1C that a POSITA would have been motivated and found it obvious to apply Akashi's teachings to the Ryu-Cole-Arcoleo combination of Ground 1A, a POSITA likewise would have been motivated and found it obvious to apply Akashi's teachings to the Ryu-Cole-Grundy-Arcoleo combination of Ground 1B. *Supra*, §V.C.2; EX1003, ¶82. The resulting Ryu-Cole-Grundy-Arcoleo-Akashi combination would have rendered obvious claims 5-9 and each of the additional features recited therein for substantially the same reasons described above in Ground 1C. *Supra*, §V.C.3 at [5]-[9]; EX1003, ¶181.

VII. INSTITUTION SHOULD NOT BE DENIED ON DISCRETION

Petitioner believes that discretionary denial is unwarranted, and yet, Petitioner intends to utilize the bifurcated briefing process contemplated by the March 26, 2025, Stewart Memorandum to rebut contentions if offered by Patent Owner to the contrary.

VIII. CONCLUSION AND PAYMENT OF FEES

The Challenged Claims are unpatentable. Petitioner authorizes charge of fees to Deposit Account 06-1050.

IX. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Infineon Technologies Americas Corp. is the Petitioner. Infineon Technologies AG, Infineon Technologies LLC, and Cypress Semiconductor Corporation are real parties-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any pertinent disclaimers, reexamination certificates, or prior PTAB proceedings involving the '028 Patent. MOSAID Technologies, Inc.—the alleged Patent Owner—filed a complaint asserting the '028 Patent against Petitioner on March 25, 2025 in the U.S. District Court for the Western District of Texas (Civil Action No. 1-25-cv-00436).

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR60246-0008IP1@fr.com.

Respectfully submitted,

Dated: August 29, 2025

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,967 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: August 29, 2025

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on August 29, 2025, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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