

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Filing Date: April 19, 2018
Title: CLOCK MODE DETERMINATION IN A MEMORY SYSTEM

DECLARATION OF DR. CARL SECHEN

I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable under Section 1001 of Title 18 of the United States Code.

Date: 29 August 2025

By: Carl Sechen
Carl Sechen, Ph.D.

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DECLARATION OF DR. CARL SECHEN

I, Carl Sechen, of Dallas, TX, declare that:

I. QUALIFICATIONS AND BACKGROUND INFORMATION

1. My name is Carl Sechen and I have been retained as an expert witness by Petitioner Infineon Technologies Americas Corp. (“Infineon”) to provide assistance regarding U.S. Patent No. 10,140,028 (“the ’028 Patent”). Specifically, I have been asked to consider the validity of claims 1-17 of the ’028 patent (the “Challenged Claims”).

2. I have been retained by Petitioners, as an independent expert in this proceeding before the United States Patent and Trademark Office. Although I am being compensated at my usual and customary rate, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

3. I understand that this proceeding involves the ’028 Patent, and I have been asked to consider the validity of certain claims of the ’028 Patent based on certain prior art references. I have also been asked to consider the state of the art and prior art available as of February 16, 2007. Based on the prior art discussed in this declaration, it is my opinion that claims 1-17 of the ’028 Patent are unpatentable for the reasons provided below.

4. I believe that I am well qualified to serve as a technical expert in this matter based upon my educational and work experience, and specifically, in the field of integrated circuits (ICs), clock signaling, and memory devices. My curriculum vitae (“CV”) is submitted with this declaration as Appendix A.

5. Of note, as shown in my CV, I have extensive experience in the design and implementation of integrated circuits involving clock signals and logic elements.

6. I received a B.S. degree in Electrical Engineering in 1975, an M.S. degree in Electrical Engineering in 1977, and a Ph.D. degree in Electrical Engineering in 1986 from the University of California, Berkeley. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

7. I have been a professor of Electrical Engineering for 39 years. After receiving my Ph.D., I joined the faculty at Yale University as an Assistant Professor of Electrical Engineering in July 1986. In 1990, I was promoted to an Associate Professor of Electrical Engineering, a position I held until June 1992. From July 1992 to August 2005, I was first an Associate Professor and then a Professor of Electrical Engineering at the University of Washington. Since August 2005 to the present, I have been a Professor of Electrical and Computer Engineering at the

University of Texas at Dallas. Over these years, my research has focused on the design and computer-aided design of digital and analog integrated circuits. I have taught numerous students how to design digital, analog, and mixed signal integrated circuits and printed circuit boards, as part of the design courses that I have offered.

8. As a professor, I have developed and taught numerous courses, For example, several courses that teach VLSI integrated circuit design in great detail. I have taught these courses continuously for the past 30 years. I have taught Verilog design to undergraduate and graduate students at the University of Washington and at the University of Texas at Dallas since 2001.

9. I have also been involved in numerous research projects on digital and analog VLSI design. I have taught numerous graduate researchers how to design digital and analog integrated circuits. My research has been funded by many companies over the years, including Intel, AMD, Cadence, LSI Logic, and Texas Instruments. For example, Texas Instruments has funded my work on memory cell research and VLSI design. My VLSI and memory design research has also been supported by governmental agencies such as DARPA and the National Science Foundation. I have authored or coauthored over 200 papers, one book, and four patents, the majority of which concern digital and analog integrated circuit design, as well as computer-aided design. I have also designed, fabricated and tested numerous integrated circuits.

10. I was elected a Fellow of the IEEE in 2002 for contributions to placement and routing of ASICs. Since then I have been promoted to Life Fellow. IEEE stands for Institute of Electrical and Electronics Engineers, which is the leading professional association for electrical engineers. The Board of Directors of the IEEE awards the rank of “Fellow” to individuals with an extraordinary record of accomplishments in any of the IEEE fields of interest. The total number of IEEE members who can be named Fellows in any one year cannot exceed one-tenth of one percent of the total voting IEEE membership.

11. I also received a Distinguished Teaching Award from the University of Texas at Dallas in 2008. I also received a second Distinguished Teaching Award from the University of Texas at Dallas in 2014. In addition, I received the *Graduate Teaching Excellence Award* from the ECE Department at UT Dallas, May 2024. In 2002, I also received the Outstanding Research Advisor Award from the Department of Electrical engineering at the University of Washington and the Best Project Award from the NSF Center for the Design of Digital and Analog ICs. I also received the Semiconductor Research Corporation's Inventor's Recognition Award in 2001 for the development of output prediction logic. I received the 1994 SRC Technical Excellence Award, and I also received the Semiconductor Research Corporation's 1988 SRC Inventor's Award. Additional honors and awards are set forth in my CV. See Appendix A.

12. I have supervised numerous graduate students, and indeed 37 Ph.D. students have graduated under my guidance. A number of doctoral theses that I have supervised relate specifically to integrated circuits, logic design, clock signaling and other circuit technologies. My students and I have published a number of peer-reviewed articles. Several of these articles received accolades in the field. For example, in 2017, we received a best paper award at the prestigious IEEE PhD Research in Microelectronics and Electronics Conference (PRIME).

13. My CV includes a list of publications on which I am a named author. It contains further details regarding my experience, education, publications, and other qualifications to render an expert opinion in connection with this proceeding.

14. In writing this Declaration, I have considered the following: my own knowledge and experience, including my work experience in mobile systems and networks; my experience in teaching those subjects; and my experience in working with others involved in those fields. In addition, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- U.S. Patent No. 10,140,028 (EX1001), and excerpts of its accompanying prosecution history (EX1002)
- U.S. Publication No. 2006/0023499 (“Ryu”) (EX1004)
- U.S. Publication No. 2005/0141666 (“Cole”) (EX1005)
- U.S. Patent No. 5,864,506 (“Arcoleo”) (EX1006)

- U.S. Patent No. 6,337,832 (“Ooishi”) (EX1007)
- U.S. Patent No. 5,917,759 (“Akashi”) (EX1008)
- U.S. Publication No. 2004/0148482 (“Grundy”) (EX1009)
- U.S. Patent No. 5,206,831 (“Wakamatsu”) (EX1010)
- U.S. Patent No. 6,304,497 (“Roohparvar”) (EX1011)
- Wu, *eNVy: A Non-Volatile, Main Memory Storage System* (1994), available at <https://dl.acm.org/doi/pdf/10.1145/381792.195506> (EX1012)
- U.S. Patent No. 6,026,465 (“Mills”) (EX1013)
- U.S. Patent No. 4,970,694 (“Tanaka”) (EX1014)
- Maksimovic, *Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply* (2000), available at <https://www.acsel-lab.com/Publications/Papers/102-IEEE-TVLSI-CAL.pdf> (EX1015)
- U.S. Patent No. 6,943,604 (“Minzoni”) (EX1016)
- U.S. Patent No. 6,972,993 (“Conley”) (EX1017)
- Lee, *Low-Energy Heterogeneous Non-Volatile Memory Systems for Mobile Systems* (2005), available at <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e1f287fa9e15bd88cb14574c4802fd7a6017c449> (EX1018)

- Crisp, *Direct Rambus Technology: The New Main Memory Standard* (1997), available at <https://www.ardent-tool.com/CPU/docs/AMD/anatomy/misc/articles/m6crisp.pdf> (EX1019)
- U.S. Patent No. 7,486,104 (“Oh”) (EX1020)
- U.S. Patent No. 6,937,513 (“Desai”) (EX1021)
- U.S. Patent No. 7,177,190 (“Lee”) (EX1022)
- Yeh, *Flash Memory Built-In Self-Test Using March-Like Algorithms* (2000), available at https://www.researchgate.net/profile/Jen-Chieh-Yeh-2/publication/3943092_Flash_memory_built-in_self-test_using_March-like_algorithms/links/0c9605187311b4193a000000/Flash-memory-built-in-self-test-using-March-like-algorithms.pdf (EX1023)
- U.S. Patent No. 7,804,176 (“Hanawa”) (EX1024)
- U.S. Patent No. 8,085,574 (“Kang”) (EX1025)
- U.S. Publication No. 2008/0016306 (“Min”) (EX1026)
- Palanisamy, *Interfacing Spartan—3 Devices with 166 MHz or 3333 Mb/s DDR SRAM Memories* (2004), available at https://my.eng.utah.edu/~cs3710/xilinx-docs/examples/s3e_starter_revD_mig_ddr/docs/XAPP768c.pdf (EX1027)
- U.S. Patent No. 6,442,644 (“Gustavson”) (EX1028)
- U.S. Patent No. 6,560,669 (“Ryan”) (EX1029)

- U.S. Patent No. 6,240,040 (“Akaogi”) (EX1030)
- Pon, *Technology Scaling Impact on NOR and NAND Flash Memories and Their Applications* (2006), available at https://web.archive.org/web/20080225091210id_/http://www.pentium.pt/design/flcomp/papers/tech_scaling.pdf (EX1031)
- U.S. Patent No. 7,499,323 (“Park”) (EX1032)
- U.S. Patent No. 6,178,518 (“Toda”) (EX1033)
- U.S. Patent No. 6,272,064 (“Wilford”) (EX1034)
- U.S. Patent No. 6,286,077 (“Choi”) (EX1035)

II. LEGAL PRINCIPLES

15. In forming my opinions and considering the subject matter of the ’028 patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

16. I understand that the claims define the invention. I also understand that an unpatentability analysis is a two-step process. First, the claims of the patent are construed to determine their meaning and scope. Second, after the claims are construed, the content of the prior art is compared to the construed claims.

17. I understand that a claimed invention is only patentable when it is new, useful, and non-obvious in light of the “prior art.” That is, the invention, as defined

by the claims of the patent, must not be anticipated or rendered obvious by the prior art.

A. Anticipation

18. I understand that under 35 U.S.C. § 102, a patent claim is invalid if its subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been told that this is referred to as invalidity by anticipation. I have been told that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

B. Obviousness

19. I understand that a patent claim is invalid as obvious if the claimed invention would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time the claimed invention was made. This means that even if all of the elements of the claim cannot be found in a single prior art reference that would anticipate the claim, a person of ordinary skill in the field who knew about all the prior art would have come up with the claimed invention. I understand that in an obviousness determination, the person of ordinary skill in the art is presumed to have knowledge of all material prior art. I understand that whether a claim is obvious is based upon the determination of several factual issues.

20. I understand that obviousness is a determination of law based on underlying determinations of fact. I understand that these factual determinations

include the scope and content of the prior art, the level of ordinary skill in the art, the differences between the claimed invention and the prior art, and secondary considerations of non-obviousness.

21. In considering obviousness, I understand that one must determine the scope and content of the prior art. I understand that, in order to be considered as prior art to a patent being considered, a prior art reference must be reasonably related to the claimed invention of that patent. A reference is reasonably related if it is in the same field as the claimed invention or is from another field to which a person of ordinary skill in the art would look to solve a known problem.

22. I understand that one must determine what differences, if any, existed between the claimed invention and the prior art.

23. I understand that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art. In evaluating whether such a claim would have been obvious, one may consider whether a reason has been identified that would have prompted a person of ordinary skill in the art to combine the elements or concepts from the prior art in the same way as in the claimed invention. There is no single way to define the line between true inventiveness on the one hand (which is patentable) and the application of common sense and ordinary skill to solve a problem on the other hand

(which is not patentable). For example, market forces or other design incentives may be what precipitated a change, rather than true inventiveness.

24. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art at the time of the alleged invention. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would employ are also relevant to the determination of obviousness.

25. I understand that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been told that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

26. I understand that one may consider, e.g., whether (1) the change was merely the predictable result of using prior art elements according to their known functions, or whether it was the result of true inventiveness; (2) there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; (3) the claimed innovation applies a known technique that had been used to improve a similar device or method in a similar way; (4) the claimed invention would have been obvious to try, meaning that the claimed innovation was one of a relatively small number of possible approaches to the problem with a reasonable expectation of success by those skilled in the art; (5) the invention merely substituted one known element for another known element in order to obtain predictable results; (6) the invention merely applies a known technique to a known device, method, or product to yield predictable results; or (7) known work in the field may have prompted variations of use of the same inventions in the same or different fields due to market forces or design incentives that would have been predictable to a person of ordinary skill in the art.

27. I understand that any assertion of secondary considerations of non-obviousness must be accompanied by a nexus between the merits of the invention and the evidence offered.

III. OVERVIEW OF CONCLUSIONS FORMED

28. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-3 and 10-17 of the '028 patent are obvious over Ryu, in view of Cole, and further in view of Arcoleo.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 1-4 and 10-15 of the '028 patent are obvious over Ryu, in view of Cole, further in view of Arcoleo, and further in view of Grundy.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 5-9 of the '028 Patent are obvious over Ryu, in view of Cole, further in view of Arcoleo, and further in view of Akashi.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 5-9 of the '028 Patent are obvious over Ryu, in view of Cole, further in view of Arcoleo, further in view of Grundy, and further in view of Akashi.

IV. BACKGROUND KNOWLEDGE ONE OF SKILL IN THE ART WOULD HAVE HAD PRIOR TO THE PRIORITY DATE OF THE '028 PATENT

29. I am informed that patentability must be analyzed from the perspective of “one of ordinary skill in the art” in the same field as the ’028 patent at the time of the invention. As previously discussed, the relevant time of invention is the patent’s priority date, which is no earlier than February 16, 2007. Moreover, I understand that whether or not a patent application provides “written description” support for patent claims must also be assessed from the perspective of a person of ordinary skill in the art.

30. I am also informed that several factors are considered in assessing the level of ordinary skill in the art, including (1) the types of problems encountered in the art; (2) the prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the field.

31. Based on the foregoing and upon my experience in this area, a person of ordinary skill in the art (“POSITA”) relating to the subject matter of the ’028 patent by the Critical Date (Feb. 16, 2007) would have had would have had a bachelor of science degree in electrical engineering, computer engineering, or a related field, and three years of experience in the research, design, or development of electronic memory circuits. Additional education could substitute for experience and vice versa.

32. Based on my experiences, I have a good understanding of the capabilities of a POSITA as I was such an individual at the time of the Critical Date. Moreover, I have taught, participated in organizations, and worked closely with many such persons over the course of my career.

33. Although I surpass this definition of one of ordinary skill in the art now and at the priority date of the '028 patent, my analysis regarding the '028 patent has been based on the perspective of one ordinary skill in the art as of the priority date of the '028 patent.

34. I am also familiar with the knowledge of the person of ordinary skill in the art as of the priority date of the '028 patent. I am able to opine on how the person of ordinary skill in the art would have understood the disclosure and claims of the '028 patent, the disclosures of the prior art, the motivation to combine the prior art, and what combinations would have been obvious to one of ordinary skill in the art.

V. INTERPRETATIONS OF THE '028 PATENT CLAIMS AT ISSUE

35. For purposes of my analysis in this IPR proceeding, I understand that the terms that appear in the claims of the '028 patent should be interpreted according to their “ordinary and customary meaning,” which is sometimes called the *Phillips* standard. In determining the ordinary and customary meaning, I understand that the words of a claim are first given their plain meaning that those words would have had

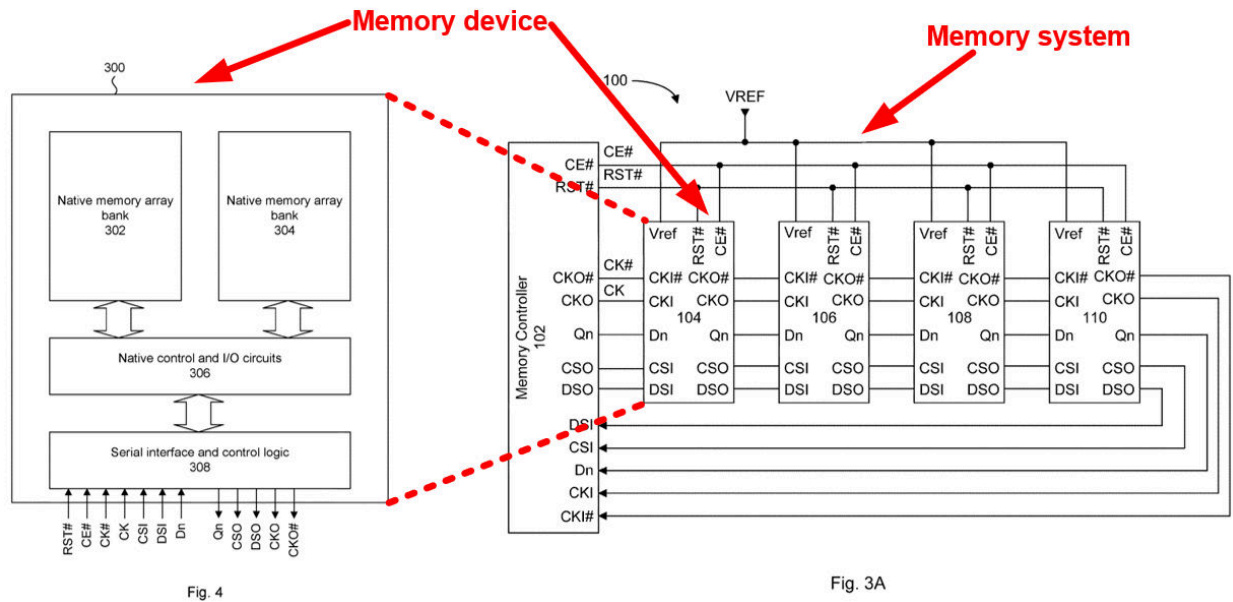
to a POSITA at the time. I also understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, I understand that even treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in interpreting terms of the Challenged Claims herein. As described further below, I have applied an interpretation of “clock” signal in Ground 1A as encompassing a discontinuous “strobe” signal based on Patent Owner’s infringement contentions in co-pending litigation involving the ’028 Patent. EX1100, 52-53; EX1101, 21-28; EX1102, 17-21. However, a “clock” signal is distinguished from a discontinuous “strobe” signal, and Ground 1B applies this interpretation in showing how the claims would have been obvious.

VI. THE ’028 PATENT

A. Overview of the ’028 patent

36. According to the ’028 Patent, a memory system includes a set of non-volatile memory devices arranged in a series configuration and a memory controller for operating the memory devices. EX1001, 1:37-2:57, 3:37-6:30, 9:3-12:49, FIGs. 3A, 3C. Each non-volatile memory device receives multiple inputs. EX1001, 2:37-5:58, 9:3-10:41, 11:19-12:49, FIGs. 3A, 3C. These inputs include, among others, a chip enable signal CE#, complementary clock signals CK and CK#, and a data input

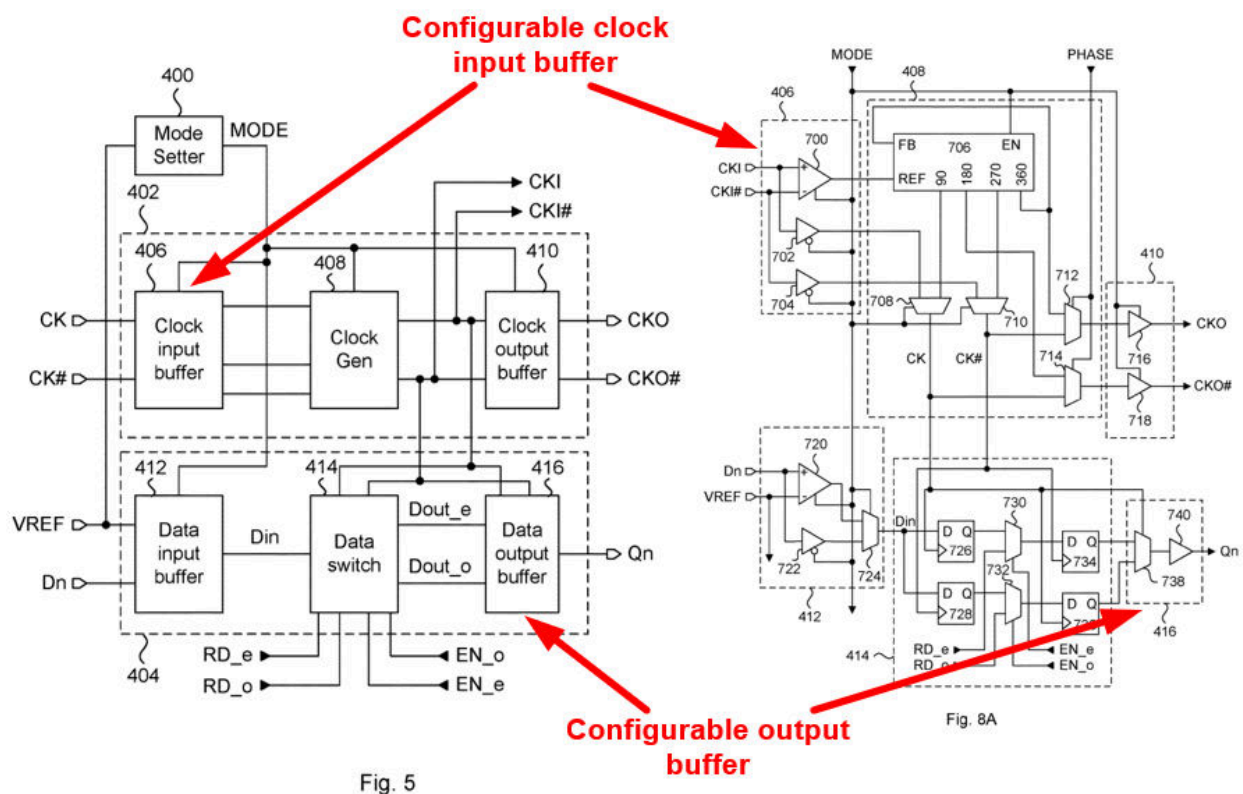
Dn. *Id.* The '028 Patent explains that in one example, each individual non-volatile memory device includes one or more memory banks and control circuitry for managing one or more operational aspects memory banks. EX1001, 12:50-13:49, FIG. 4.



EX1001, FIG. 4, FIG. 3A (annotated).

37. As noted above, two of the inputs received by the clock input buffer of the non-volatile memory device include complementary clock input signals CK and CK#. EX1001, 4:46-5:5, 14:41-63, 17:32-51, FIG. 5, FIG. 8A. These clock signals complementary to one another, because when CK is a high value CK# is a low value and vice versa. EX1001, 4:46-5:5, 14:41-63, 17:32-51, FIG. 5, FIG. 8A. A mode signal (MODE) that can indicate either of a first logic state or a second logic state, meaning that the clock input buffer is configurable between a differential signaling mode and a single ended signaling mode. EX1001, 4:1-25, 4:46-5:5, 14:25-63,

15:38-62, 17:32-51, 18:26-51, 22:36-56, FIG. 5, FIG. 8A. In one logic state of the MODE signal, the clock input buffer is configured to generate “a single ended clock signal based on [the] two differential clock inputs CK and CK#.” *Id.*, 14:41-49. In the second logic state of the MODE signal, the clock input buffer is configured to generate “separate buffered versions of CK and CK#.” *Id.*



EX1001, FIG. 5, FIG. 8A (annotated).

38. I noticed that the '028 Patent expressly discloses that the “clock mode configuration circuit ... is provided for allowing the configurable memory device to be used in both a parallel clocked memory system and a serially clocked memory

system.” EX1001, 8:31-9:3. However, parallel and serial clock signal modes are noticeably missing from the claims of the '028 Patent. Instead of referring to parallel and serial clock signal modes, the claims describe the clock input buffer as being configurable “to one of a *single ended signaling configuration* and a *differential signaling configuration*.” EX1001, 23:26-61. I did not notice the terms “single ended signaling configuration” and “differential signaling configuration” appearing anywhere in the specification of the '028 Patent. As I describe below in my analysis of Grounds 1A-1D (*infra*, §VIII), clock input buffers that achieved the claimed configurability were well known before the Critical Date.

39. The non-volatile memory device described by the '028 Patent also includes a data input buffer (e.g., data input buffer 412) and a data output buffer (e.g., data output buffer 416). EX1001, 5:26-40, 14:64-15:18, 19:4-67, FIG. 5, FIG. 8A. The data input buffer and the data output buffer are connected to one or more common data lines (e.g., D_n and Q_n, respectively). EX1001, 5:26-40, 14:64-15:18, 19:4-67, FIG. 5, FIG. 8A. In addition, the output buffer is configured so that a drive strength is controllable (e.g., by a user). EX1001, 19:56-67. The non-volatile memory device also includes a clock output buffer that drives at least one clock output signal that is generated based on one or both of the complementary clock signals. EX1001, 4:46-5:5, 14:41-63, 18:26-51, 20:47-21:37, FIGs. 5, 8A-8B. The clock output signal is synchronized in a double data rate configuration with output

data produced at the output buffer. EX1001, 4:46-5:5, 14:41-63, 18:26-51, 20:47-21:37, FIGs. 5, 8A-8B. The '028 Patent explains that the configurable data output buffer can “optimize performance and power in the multi-drop bus and point-to-point ring topologies.” EX1001, 19:56-67.

B. Prosecution History of the '028 patent

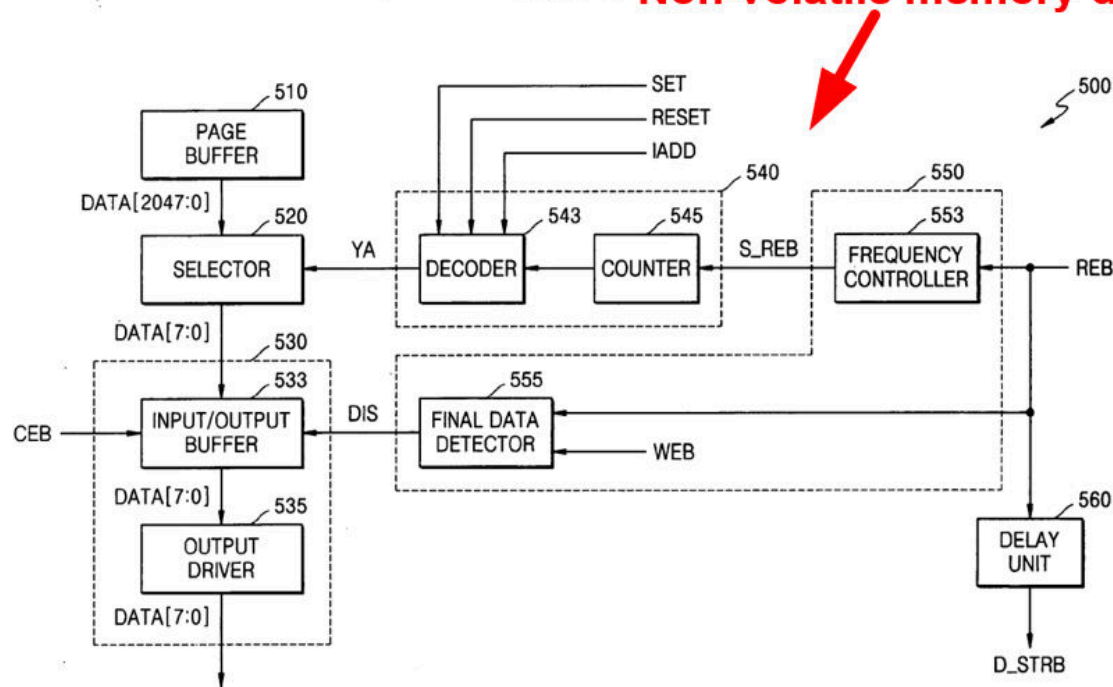
40. I noticed that the Examiner never issued any rejections of the claims of the '028 Patent based on prior art references, and the claims were promptly allowed. *See generally*, EX1002. The Examiner stated in the response for allowance that “[t]he prior art fails to disclose or suggest ‘a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration...” and “one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths.” EX1002, 102. To the contrary, the features of a “configurable clock input buffer” and “one or more configurable output buffers” as claimed were well-known in the art by the Critical Date of the '028 Patent. This is demonstrated by references such as Cole, which discloses a configurable clock input buffer, and Arcoleo, which discloses a configurable clock output buffer. *Infra*, §VII. The file history contains no indication that the Examiner had ever considered these references, or the particular prior art combinations advanced in Grounds 1A-1C, when the application that issued as the '028 Patent was allowed. *See generally*, EX1002.

VII. OVERVIEW AND COMBINATIONS OF PRIOR ART REFERENCES

A. Overview of Ryu

41. Ryu explains that a “non-volatile memory device” “receive[s] or output[s] data through an input/output pin...when reading or writing data.” EX1004, [0003], *see also id.*, [0005], [0041]-[0043], [0059], [0060], [0076], FIG. 5, FIG. 11. The non-volatile memory device includes several features, including “a non-volatile memory array” that stores data, a “page buffer” that receives a portion of this data, and a “selector” that selects data for sending to an “output unit” based on address data. EX1004, [0041]-[0043], [0058]-[0060], [0076]-[0078], FIG. 5, FIG. 11. The output unit includes an input/output buffer that receives an enable signal (CEB) and a disable signal (DIS) and controls the input and output of data from the non-volatile memory device based on these signals. EX1004, [0043], [0059]-[0061], [0063], [0078], FIG. 5, FIG. 11.

FIG. 5 **Non-volatile memory device**



EX1004, FIG. 5 (annotated).

42. The non-volatile memory device described by Ryu includes a “system clock” (SCLK). EX1004, [0003], FIGs. 1A-1B, 4A, 7, 12. To control read and write operations of the non-volatile memory device, the system clock receives a read control signal (REB) and a write control signal (WEB). EX1004, [0003]-[0008], [0045], [0047]-[0049], [0051], [0061]-[0064], [0066]-[0070], FIGs. 5, 7. A “delay unit” of the non-volatile memory device generates a D_STRB signal that is output from the device. EX1004, [0064], [0068], [0092], [0095], FIGs. 5, 7, 11, 12. This D_STRB signal indicates a timing of the data output from an input/output pin of the device, meaning that the D_STRB signal acts as a “clock.” EX1004, [0064], [0067]-

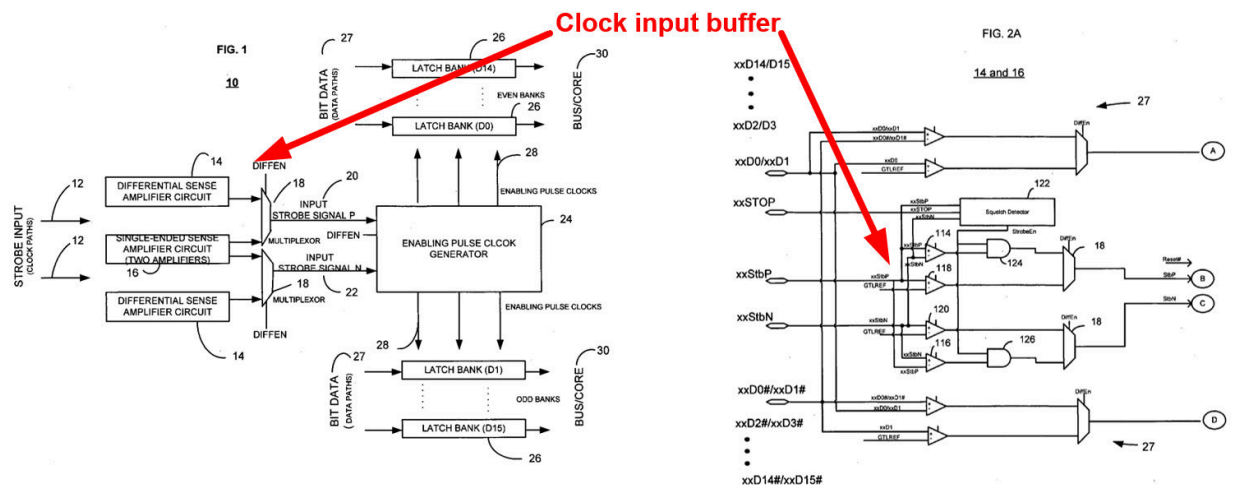
[0068], [0092], [0095], FIGs. 5, 7, 11, 12. The D_STRB signal is synchronized with the data output in a double data rate configuration. *Id.*

B. Overview of Cole

43. I noticed that Cole describes “a micro-architecture for an input section of an integrated circuit (IC)[] ... that may be configured to support either differential or single-ended signaling mode of source synchronous data transfer/signaling. EX1005, [0013]. Cole explains that “there are at least two types of data input signaling modes, single-ended signaling mode and differential signaling mode.” EX1005, [0002]. A difference between these two signaling modes, according to Cole, is that “[c]urrently, for a variety of reasons, the former [signaling mode] tends to be favored by the lower speed, higher voltage integrated circuits, while the later [*sic*] tends to be favored by the higher speed, lower voltage integrated circuits.” *Id.* Cole also explains that “[t]he differences between the two signaling modes create[s] difficulties for designing the Input sections of the integrated circuits of the different types, especially since they often have to co-exist and co-operate with each other in the same system” *Id.* Like the '028 Patent, Cole proposes solutions to address these problems through a configurable IC that supports different signaling modes.

44. Cole explains that an input section of an IC receives a first strobe input signal (xxStbP) and a second strobe input signal (xxStbN) to control latching operations. EX1005, [0013]-[0020], [0023]-[0028], FIGs. 1 (disclosing strobe input

“CLOCK PATHS” 12), 2A-2C. For example, I noticed that the input section controls data flow through latch banks 26 in a plurality of data paths using the complementary strobe input signals by generating two internal strobe signals (sometimes referred to as “StbP” and “StbN”). EX1005, [0017], [0019]-[0021], [0026], [0027], FIG. 1, FIG. 2A. Each one of the two strobe signals can be generated using one or both of the strobe inputs. *Id.*



EX1005, FIG. 1 (annotated).

45. The input section of Cole represents a configurable input buffer that uses a control signal (DIFFEN) for configuring the integrated circuit to operate in a “differential signaling mode” or a “single-ended signaling mode.” EX1005, [0018], [0022]-[0023], [0034]; *see also* [0013], [0017]-[0019], [0021], [0025], [0028], FIGs. 1, 2A. Cole explains that the input buffer includes “sense amplifiers 114 and 116” that each receive the complementary strobe input signals xxStbP and xxStbN as

differential signals and “sense amplifiers 118 and 120” that each receive one of the complementary strobe input signals as a single ended signal. EX1005, [0026], [0028], *see also id.*, [0019], [0021], [0021], FIGs. 1, 2A. The sense amplifiers 114 and 116 are activated when the DIFFEN control signal has a value “1,” thereby causing the integrated circuit to operate in the differential signaling mode, and the sense amplifiers 118 and 120 are activated when the DIFFEN control signal has a value “0,” thereby causing the integrated circuit to operate in the single ended signaling mode. EX1005, [0023].

C. Overview of Arcoleo

46. Arcoleo describes a memory device that manages data output from a memory chip using an output buffer. EX1006, 1:6-10, 2:66-3:6, 3:43-4:28, 6:10-65, 8:1-46, 8:47-10:5, FIGs. 4-6. Arcoleo explains that a “drive strength selector (*sic*)” of the output buffer “enables control of the operation of the output buffer” to select “one of a set of possible output buffer drive strengths.” EX1006, 6:10-7:23, FIG. 4. It is apparent this output buffer of Arcoleo is configurable to one of a plurality of drive strengths. *Id.*

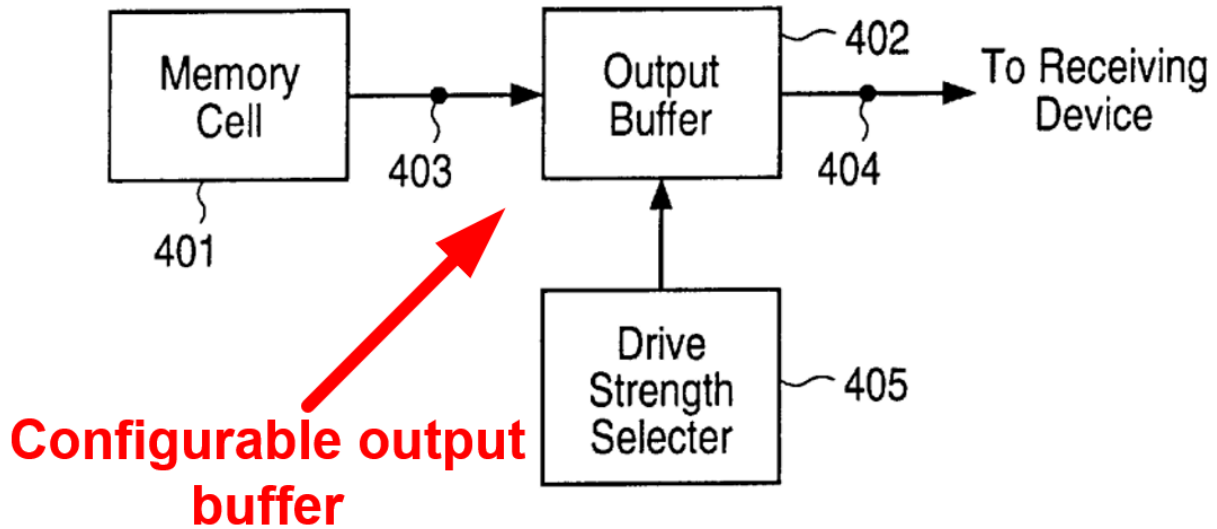


FIG. 4

EX1005, FIG. 4 (annotated).

47. One reason that Arcoleo provides for making the drive strength from the output buffer configurable is that “the drive strength of the output buffers of a memory device” is “appropriately matched” with the electrical load at an output of the output buffer. EX1006, 1:37-51. For example, “an impedance mismatch between the output buffer and the transmission line electrical load” can occur when the output drive strength is too strong, and “the data can be supplied from the memory device to the receiving device more slowly than desired” when the output drive strength is too weak. EX1006, 1:52-2:11. Using a configurable output buffer can prevent these issues from occurring.

D. Combination of Ryu, Cole, and Arcoleo

Combining Ryu with Cole

48. As I discussed above in the overview of Ryu (*Supra*, §VII.A), the non-volatile memory device of Ryu controls operations to read and write data from a non-volatile memory array in a synchronous fashion. EX1004, [0003], [0005], [0041]-[0043], [0059], [0060], [0066]-[0070], [0076], [0094], [0095], FIGs. 5, 7, 11, 12. Even though Ryu's device incorporates use of a system clock signal, I noticed that Ryu describes few details about this clock signal or how a particular type of signaling configuration is implemented on the device based on the clock signal. For example, Ryu does not expressly address which configuration its device employs or how its device would communicate with other devices that use different signaling configuration even though a POSITA would have known that ICs commonly employed either a single-ended signaling configuration or a differential signaling configuration. It is clear, therefore, that a POSITA would have turned to Cole for details of a known and beneficial technique for implementing a configurable input section of an IC capable of selectively switching between a single ended signaling configuration and a differential signaling configuration. *Supra*, §VII.B. Multiple reasons would have prompted a POSITA to integrate a configurable input section that can be selectively configured to a single ended signal mode or a differential signaling mode as suggested by Cole in the non-volatile memory device of Ryu.

49. **First**, a POSITA would have sought to make Ryu's memory device compatible with other devices in many different contexts so that the memory device is versatile in application. For example, a POSITA would have pursued the combination to achieve interoperability between Ryu's device and other devices regardless of the type of signaling employed (e.g., single ended signaling or differential signaling). Cole explains that the single ended signaling mode "tends to be favored by lower speed, higher voltage integrated circuits" and the differential signaling mode "tends to be favored by higher speed, lower voltage integrated circuits." EX1005, [0002]. To ensure that the differential signaling mode and the single ended signaling mode "co-exist and co-operate with each other in the same system," the configurable clock input buffer as taught in Cole would have been beneficial to allow Ryu's non-volatile memory device to toggle between these modes. EX1005, [0002]; *see also id.*, [0001], [0013], [0043], FIG. 8, Abstract. This enables the system to operate in a variety of different environments.

50. **Second**, to include a configurable input section as suggested by Cole to allow the memory device to receive data signals according to either a single-ended or differential mode signaling configuration in an efficient manner using common circuit components that were well known before the Critical Date, a POSITA would have implemented Ryu's non-volatile memory device to include a configurable input section as suggested by Cole. I noticed that the input section 10 of Cole includes two

multiplexors 18, each of these multiplexors 18 receiving a respective input from one of the differential sense amplifier circuits 14 and one of the single-ended sense amplifier circuits 16. EX1005, [0019]-[0022], [0026], FIGs. 1, 2A. The multiplexors 18 each receive a control signal “Diffen” that controls whether the clock input buffer operates in the differential signaling mode or the single ended signaling mode by passing outputs from single ended amplifiers in one mode and passing outputs from differential amplifiers in another mode. *Id.* It is apparent that a POSITA therefore would have understood that multiplexors provide configurability between modes by readily selecting outputs from appropriate amplifiers to provide configurability between modes in an efficient manner based on a single “Diffen” control signal. *Id.*

51. ***Third***, a POSITA would have sought to efficiently latch received data regardless of whether the data is signaled using either a single-ended or differential signaling scheme by implementing Ryu’s memory device with a configurable input section as suggested by Cole. Implementing Ryu’s memory device with Cole’s configurable input section in this way would allow the non-volatile memory device to more efficiently receive data through I/O pins of the device using either single-ended or differential signaling. EX1005, [0025] (“[T]o achieve at least the same data transfer rate for a given set of pins ..., the embodiment is designed to allow the data to be transmitted on each data path at twice the speed while operating in a differential signaling mode (as compared to the speed of transmission while operating in the

single-ended mode).”). Indeed, Cole explains that “[l]atch banks 26 may be employed to latch and temporarily store the data being transferred,” and “[t]he latch banks 26 may operate in accordance with enabling pulse clocks 28” that are generated based on complementary clock signals, and “[a]n enabling pulse clock generator 24 may be employed to provide latch banks 26 with enabling pulse clocks 28 to control their operations,” which means that the enabling pulse clocks 28 generated by the input section drive the latch banks 26 in the differential signaling mode having a higher transmission speed. EX1005, [0016], [0017]; *see also id.*, [0015]-[0018], [0023]-[0025], FIGS. 1, 2B.

52. ***Fourth***, to enable generation of internal strobe signals according to either of a single-ended or differential signaling mode, a POSITA would have been motivated to implement the memory device of Ryu with a configurable input section that receives two complementary strobe input signals as taught by Cole (e.g., xxStbP, xxStbN). For example, Cole’s input section 10 generates internal strobes based on the complementary strobe inputs in the differential signaling mode. EX1005, [0026] (“each of sense amplifiers 114 and 116 receives both two strobe signals, and generates StbP/StbN based on the received signals”). Cole’s input section 10 likewise generates internal strobes in the single ended signaling mode, but each of the internal strobes is generated based on a respective one of the complementary

strobe inputs. EX1005, [0026] (“each of sense amplifiers 118/120 receives one of the two strobe signals...and generates StbP/StbN based on the received signals”).

53. ***Fifth***, a POSITA would have found it obvious to combine the teachings of Ryu with Cole because the combination merely involves the application of a known technique to a known system to achieve predictable results.. It is clear that Cole recognized a problem in reconciling speed and power requirement tradeoffs between ICs that implement differential or signal-ended signaling modes, and Cole described a straightforward solution to address this problem. A POSITA would have reasonably expected success implementing Ryu with Cole. This is especially true given that the combination involves well-known data transfer techniques and conventional logic circuitry that was also well known before the Critical Date. The clock input buffer of Cole and the non-volatile memory device of Ryu would be compatible, because Ryu and Cole both describe techniques for controlling data outputs based on one or more clock signals. EX1004, [0003] (“SCLK represents a system clock”); EX1005, FIG. 2A (depicting “clock paths”). Cole also expressly confirms that its configurable input section can be implemented in a wide range of ICs including memory devices like those disclosed in Ryu. EX1005, [0043]-[0044], [0046]-[0047], [0045] (“system 800 may include other components, including but [] not limited to non-volatile memory” and “[o]ne or more of these components may also include input section 10”), FIG. 8.

Combining Ryu-Cole with Arcoleo

54. As I described above in my analysis of the Ryu-Cole combination, it would have been obvious for a POSITA to implement Ryu's memory device to include an input section configurable between a single ended signaling configuration and a differential signaling configuration as suggested by Cole. I notice that Ryu expressly discloses that an "input/output buffer 533 outputs or blocks the data DATA[7:0]" and "output driver 535 outputs the data DATA[7:0] from the input/output buffer 533 to the external source through [an] input/output pin." EX1005, [0060]. But neither Ryu nor Cole describe in detail electrical requirements of devices that are connected to an input/output pin of the memory device. To implement an output driver for outputting data from the memory device, a POSITA would have turned to Arcoleo. One reason is that Arcoleo discloses "[a]n output buffer drive strength selector [*sic*] 405 enables control of the operation of the output buffer 402 so that the output buffer 402 has a selected one of a set of possible output buffer drive strengths," which means that Arcoleo provides providing a solution to configure an output drive strength based on the electrical load of the outputs. EX1006, 6:19-65, 14:10-21, FIG. 4; §VII.C. A POSITA would have been motivated to further augment the Ryu-Cole memory device with the features disclosed in Arcoleo for multiple reasons.

55. **First**, because techniques for tailoring the drive strength of an output buffer to fit the needs of a system were well known by the Critical Date of the '028 Patent, a POSITA would have implemented Ryu-Cole's non-volatile memory device with a configurable output buffer as taught by Arcoleo. More than eight years before the Critical Date of the '028 Patent, Arcoleo acknowledged that "[i]n many current electronic [s]ystems...SRAMs must drive and switch electrical loads that are more accurately modelled as distributed capacitive loads (i.e., as transmission lines), rather than as lumped capacitive loads, thus *necessitating output buffers having different drive characteristics*." EX1006, 1:45-51. Arcoleo also confirms that its techniques can be applied to a range of different memories including non-volatile memory devices like those described in Ryu. EX1006, 5:30-33 ("The invention can be implemented with any type of memory device, such as, for example, SRAM, ... flash memory ..."), 5:22-29.

56. **Second**, the output buffer of Arcoleo is implemented simply using two parallel inverters, one of which can be connected and disconnected by a switch to control the drive strength. EX1006, 6:37-65; FIGs. 5A-5B. Because connecting and disconnecting an inverter using a switch can be done using well-known components that are easy to control, a POSITA would have understood that this configuration is a straightforward and effective way to control drive strength. A POSITA therefore

would have been motivated to modify the non-volatile memory device of Ryu-Cole with the output buffer of Arcoleo.

57. **Third**, to promote use of the non-volatile memory devices in a wider range of systems while allowing a system designer to more flexibly incorporate the device in a larger computer/memory system, a POSITA would have been motivated to implement the non-volatile memory device of Ryu with an output buffer having a user-selectable drive strength, as taught by Arcoleo. Arcoleo explains that “[w]hile output buffers having selectable drive strength have previously been used with other devices...selectable drive strength output buffers that allow a user to adjust the output buffer drive strength have not heretofore been used with...memory devices.” EX1006, 3:7-40. This allows “the output buffer drive strength to be easily selected by a user of the memory device...from the multiple possible drive strengths.” EX1006, 3:43-65. A POSITA would have understood that allowing a user to configure the output drive strength would be beneficial to permit a user to integrate a memory device in a custom system having other components.

58. **Fourth**, a POSITA would have found it obvious and beneficial to promote use of the non-volatile memory devices in a wider range of systems while allowing a system designer to more flexibly incorporate the device in a larger computer/memory system, thus ensuring that the device is versatile for use in many different contexts and applications. Implementing the memory device of the Ryu-

Cole combination with a configurable output buffer for each common data signal that is output by the memory device is beneficial because the configurable output buffer of Arcoleo receives a bit stream of output data from an input/output pin. To match the needs of the system, this would result in the memory device being able to configure the drive strength of every output signal independently. For example, when outputs from the memory device interface with different capacitive loads, it is beneficial to independently control the drive strength of each output to account for these differences.

59. *Fifth*, a POSITA would have found it obvious to further combine the teachings of Ryu-Cole with Arcoleo because the combination merely involves the application of a known technique to a conventional system to achieve predictable results. Here, Arcoleo recognized a problem with existing output buffers and described a straightforward method to address it. In this context, combining the teachings of Ryu-Cole with Arcoleo would have been obvious, and a POSITA would have reasonably expected success, especially considering that the combination merely implicates conventional techniques for transmitting common data and conventional circuitry. The Ryu-Cole memory device would be fully compatible with a configurable output buffer as taught in Arcoleo. For example, the device of Ryu-Cole and the device of Arcoleo both involve outputting data stored by memory cells via an output buffer. EX1004, [0060], [0061]; EX006, 6:10-36.

E. Overview of Grundy

60. Grundy discloses a “memory system” that includes a “set of memory devices” that are “coupled to one another in chain.” EX1009, [0035], *see also id.*, [0030], [0036]-[0059], FIGs. 3-7E. According to Grundy, every memory device in the chain includes a “signaling interface” and a “storage array,” and it is clear that the storage arrays of the memory devices collectively provide memory for storing data bits. The signaling interface of Grundy can be “used to receive and transmit data and commands propagating through the chain of memory devices.” *Id.* Grundy expressly discloses that the storage arrays can include “nonvolatile storage arrays.” *Id.* Grundy also explains that the chain of memory devices communicate by “signaling links” that connect each memory device to other memory devices and a memory controller. EX1009, [0043], *see also id.*, [0030], [0044], [0047]-[0059], [0084], [0085], FIGs. 5A-7E, 17. These signaling links include a “clock line” that carries clock signals, a “command line” that carries command signals, “multi-purpose lines” that carry data stored by or to be stored by the storage arrays, and a “valid line” indicating whether a valid command or data signal is being transmitted. *Id.*

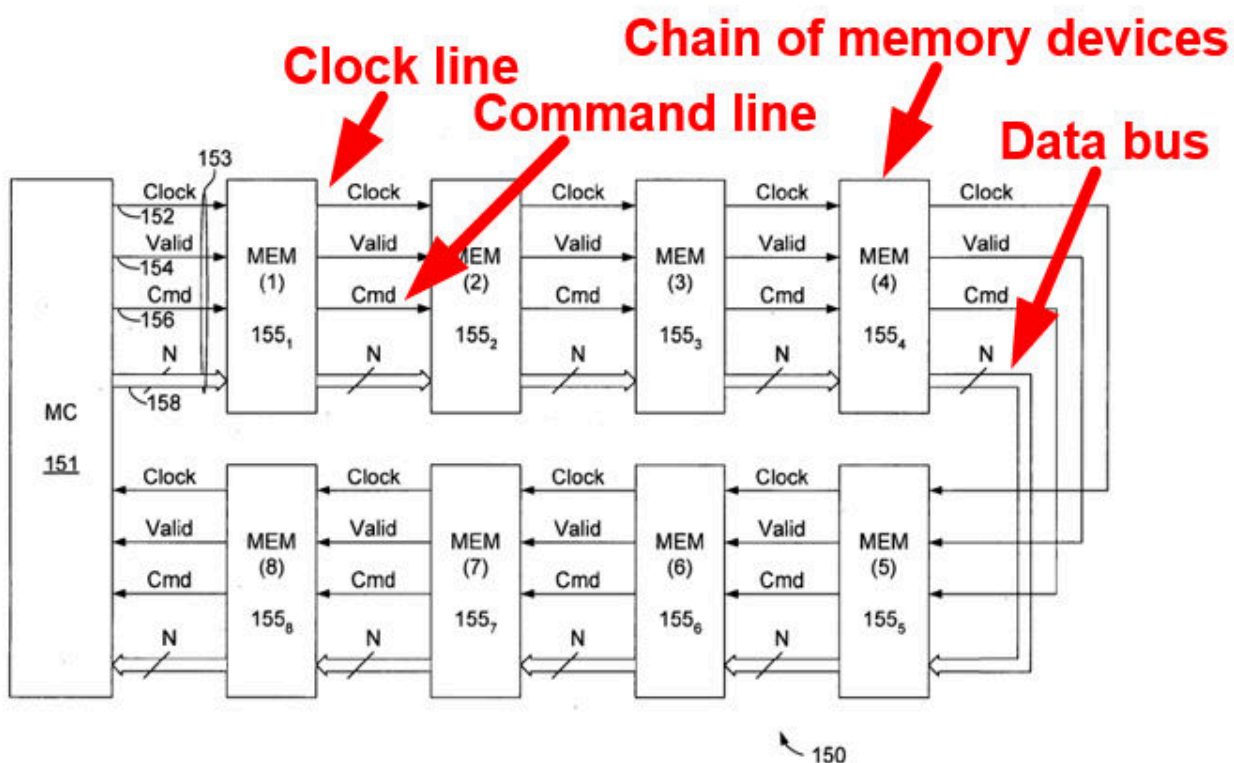


FIG. 5A

EX1009, FIG. 1 (annotated).

61. Every memory device in Grundy's chain includes a clock input ("Clock In") that receives a clock signal from a prior device in the chain and a clock output ("Clock Out") that forwards clock signals to the next device in the chain, which means that the clock signals cycle through the chain of memory devices such that each memory device both receives and outputs a clock signal. EX1009, [0084]-[0091], FIG. 17. The clock signal in Grundy is a free-running signal that provides a steady stream of clock pulses. This clock signal is used to control latching operations in the command lines and data lines, which likewise have inputs and outputs on each memory device. *Id.*

F. Combination of Ryu, Cole, Arcoleo, and Grundy

62. As I described above in my analysis of the Ryu-Cole-Arcoleo combination (§VII.D, *supra*), it would have been obvious to implement Ryu's memory device to include an input section that receives complementary strobe input signals as taught by Cole. Ryu also explains that "[a] controller...for controlling the non-volatile memory device applies a read control signal REB to the non-volatile memory device to receive data during a read operation" and "a D_STRB signal may be created by delaying the read control signal REB by a predetermined delay time and output at the same time with the data DATA[7:0] to the external source," meaning that D_STRB represents an output signal that is referenced to an input signal REB. EX1009, [0005], [0064], FIG. 5.

63. I have been informed that in co-pending litigation involving the '028 Patent, the Patent Owner asserted that a "strobe" signal represents "clock" signal in its infringement contentions against Petitioner. *See* EX1100, 52-53; EX1101, 21-28; EX1102, 17-21; *supra*, Footnote, 2. However, the term "clock" signal is distinguished from a "strobe" signal in that a "clock" signal represents a *continuous* periodic signal for synchronizing timing, whereas a "strobe" signal is only active at certain times (e.g., during data transfer). Strobe signals are not "clock" signals under this interpretation because the periodic behavior of "strobe" signals is not ordinarily continuous. *Id.* A "strobe" signal often alternates periodically only when data is

present on a corresponding input or output line to which the strobe signal is synchronized. *Id.* The periodic strobe signal is discontinued (e.g., it is held at a constant signal level) during times when no data is transferred. *Id.*

64. The claimed clock input and output signals would have been obvious to a POSITA when the Ryu-Cole-Arcoleo combination is further considered in view of Grundy, even if this interpretation of the “clock” signal is applied. This is because instead of teaching a discontinuous strobe signal, Grundy discloses the conventional alternative option of synchronizing data input to and outputted by a memory device to a continuous clock signal. For example, Grundy discloses the following:

[T]he memory controller 151 outputs a **free-running clock signal 172₁** on the clock line 152 coupled between the memory controller 151 and the initial memory device 155₁. **The clock signal 172₁ may also be a strobe signal that is toggled only when data and/or commands are being transmitted on the point-to-point link 153.** When command or data values are to be transmitted on the signaling queue ..., the memory controller 151 simultaneously asserts a valid signal 174₁ on the valid line 154 (and a command signal 176₁ on command line 156 if a command is being transmitted) and drives a first value, A, onto the bus 158, both in response to an edge 167 of the clock signal 172₁. The memory controller 151 continues to assert the valid signal 174₁ (and command signal if appropriate) as subsequent values B, C, D, E, and F are transmitted on to the bus 158 in successive transmit intervals.

65. EX1009, [0047].

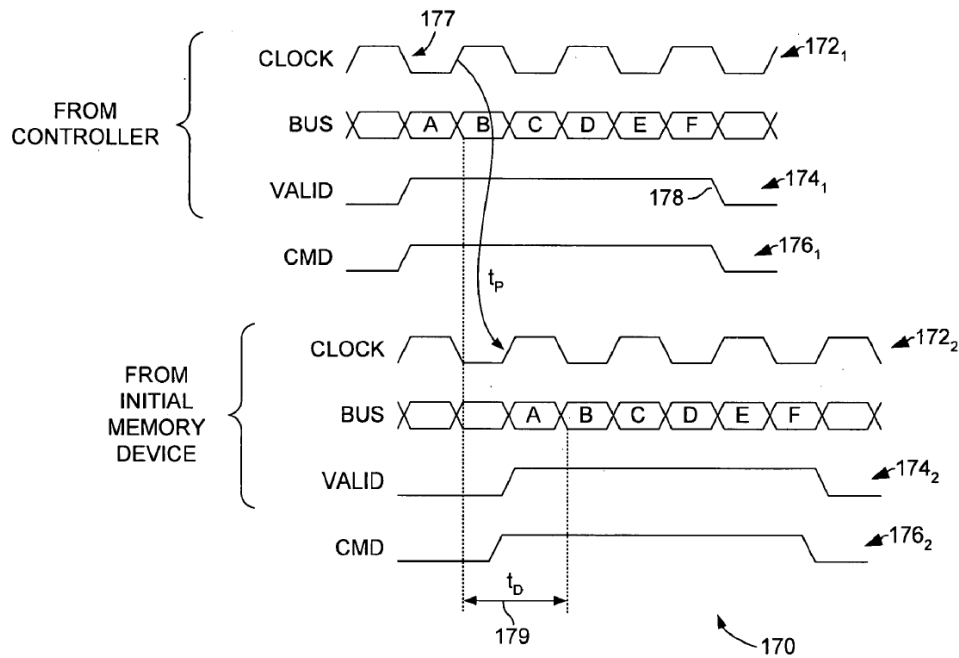


FIG. 6

EX1009, FIG. 6.

66. The free-running clock signal of Grundy can be used in place of a discontinuous strobe signal if separate control lines (such as the VALID or CMD lines) are provided to indicate when data is and is not present on the bus, and a POSITA would have understood this. A POSITA would have found it obvious and would have been motivated to further modify the Ryu-Cole-Arcoleo combination to implement a timing scheme for data transfers using continuous clock signals rather than discontinuous probe signals for multiple reasons. In the resulting Ryu-Cole-Arcoleo-Grundy combination, the discontinuous strobe inputs (e.g., xxStbP and xxStbN) and strobe output signal (e.g., D_STRB) in the resulting combination would

be implemented as continuous clock signals where the presence/absence of data is separately indicated on separate control lines (e.g., VALID and/or COMMAND lines).

67. To the extent neither Ryu nor Cole expressly describes a clock output port configured to transfer a continuous “*clock* output signal” that is referenced to a first clock input signal and synchronized with output data in a double data rate configuration, a POSITA would have turned to Grundy for additional teachings that would have rendered this feature obvious. Grundy explains that every memory device in the memory device chain includes an “input-side clock line” that receives a clock input signal from a prior device in the chain and an “output-side clock line” that transfers an output clock signal to a subsequent device in the chain, meaning that Grundy expressly describes clock input ports and clock output ports. EX1009, [0088]. It is apparent, therefore, that a POSITA would have looked to Grundy for details of a known and beneficial technique for receiving clock input signals and generating clock output signals. *Supra*, §VII.E. Multiple reasons, taken together or independently, would have prompted a POSITA to apply Grundy’s suggested use of clock input port and clock output ports in the non-volatile memory device of Ryu.

68. ***First***, implementing a memory device either with continuous clock signals having corresponding control lines or implementing the memory device with discontinuous strobe signals would have been an obvious design choice and simple

substitution, and a POSITA would have understood this. Grundy explains free-running clock signals and strobe signals that are transmitted only during data transfers were primarily two known, predictable alternatives for signaling data timing information, and a POSITA would have selected one alternative or the other to meet the demands of a given application or design, as both were obvious to try. EX1009, [0047] (“the memory controller 151 outputs a free-running clock signal 172 on the clock line 152...[t]he clock signal 172, may also be a strobe signal that is toggled only when data and/or commands are being transmitted”), FIG. 6. A continuous clock signal can be often beneficial when the memory device is already configured to receive and transfer the clock signal as part of a serially chained memory system like Grundy’s, as this scheme obviates a need for separate (semi) periodic strobe signals, which can reduce cost and complexity in the circuitry. Discontinuous strobe signals, beneficially reduce the number of signaling lines needed for timing data transfers because strobe signals do not require separate control signal lines (e.g., VALID, COMMAND signals) to indicate when data is being transferred. *Id.*

69. ***Second***, because Ryu and Cole invite alternative timing schemes, a POSITA would have found it obvious to implement continuous clock signals for data timing according to Grundy’s suggestion. For example, Ryu discloses alternative embodiments in which D_STRB is already a delayed version of a “flash

clock signal” rather than the discontinuous REB signal. EX1004, [0072]-[0082], FIGs. 9-11. Cole also describes alternatives for the strobe inputs 12 to be provided “in parallel with the data (requiring no extraction) or interleaved with the data (requiring extraction).” EX1006, [0020]. These examples indicate that the substitution of discontinuous strobe signals for a continuous clock is fully compatible with the range of timing schemes contemplated by each of Ryu and Cole.

70. **Third**, a POSITA would have been motivated to implement Ryu’s non-volatile memory device with clock input ports and clock output ports as taught by Grundy because Grundy discloses a memory system having a chain of serially connected memory devices. This would ensure that every memory device in the chain receives a clock signal to govern internal latching operation. According to Grundy, a high-speed interface of each memory device “is designed to work seamlessly with the incoming and outgoing point-to-point links and operates at the clock rate provided in the incoming link clock signal.” EX1009, [0084]. It helps a memory device to work with other memory devices in a chain by implementing the non-volatile memory device with clock input ports and a clock output port.

71. **Fourth**, to improve processing speed and scalability of the memory system, a POSITA would have understood the value of implementing Ryu’s non-volatile memory device as one of a chain of memory devices connected to a controller as taught by Grundy. I noticed Grundy explains that “each additional

memory device is coupled to the system via a point to-point link, thereby enabling high-integrity, high-speed signaling” in a way that “does not compromise data throughput or consume additional pins on the memory controller.” EX1009, [0030]. To provide an ability to scale the number of memory devices based on the needs of the system, a POSITA would have configured Ryu’s non-volatile memory device to interface with other memory devices in a chain as taught by Grundy.

72. ***Fifth***, to enable the non-volatile memory device to process data at a higher rate, a POSITA would have been motivated to implement the non-volatile memory device of Ryu-Cole-Arcoleo with multiple common data ports as taught by Grundy. Grundy describes a memory device including “a set of N multi-purpose lines” that are “used at alternate times to transfer N-bit wide data values and command values,” which means that multiple bits are input to the memory device at any given time. EX1009, [0043], [0044]. The resulting non-volatile memory device can receive and/or output multiple data bits at any one point in time, thus improving data processing rates.

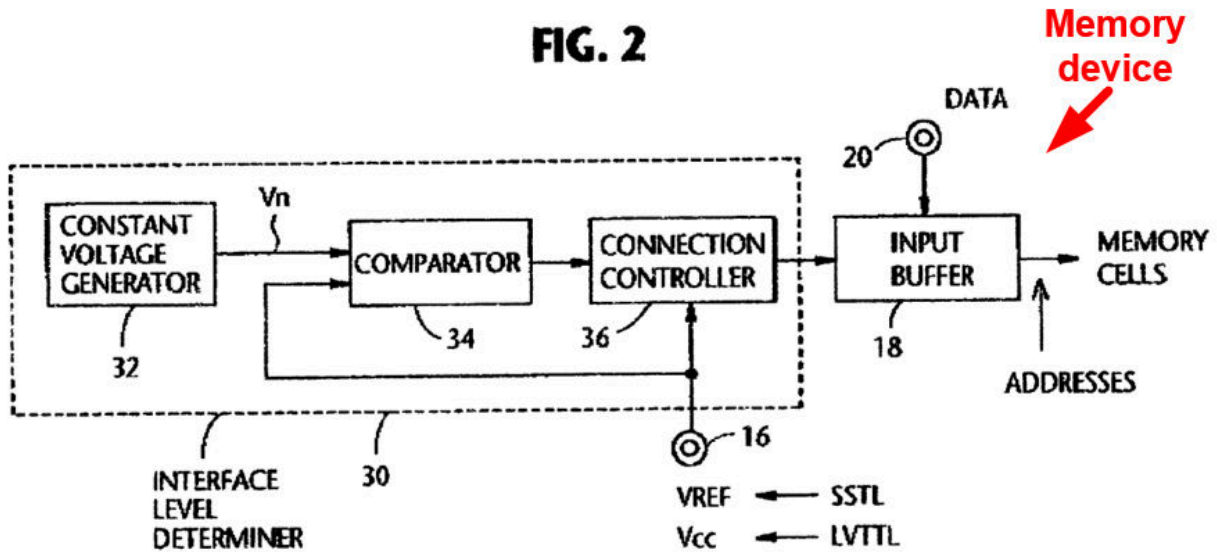
73. ***Sixth***, because the combination merely involves the application of a known technique to a known system to achieve predictable results, a POSITA would have found it obvious to combine the teachings of Ryu-Cole-Arcoleo with Grundy. Here, Grundy recognized a problem with scalability of memory systems involving multiple memory devices and described a straightforward technique to address it.

Combining the teachings of Ryu-Cole-Arcoleo and Grundy would have been obvious to a POSITA, and a POSITA would have reasonably expected success in this combination. This is especially true because the combination involves well-known techniques for transferring clock signals and data signals using memory devices and standard memory device and data logic hardware that was well known before the Critical Date. The memory device of Grundy would be compatible with the non-volatile memory device of Ryu-Cole-Arcoleo because Grundy and Ryu-Cole-Arcoleo both describe techniques and hardware for transferring common data signals and clock signals. EX1004, [0003] (“SCLK represents a system clock”); EX1005, FIG. 2A (depicting “clock paths”).

G. Overview of Akashi

74. According to Akashi, a memory device can include a data pin and one or more memory cells. EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2. Akashi’s memory device includes an input buffer that determines whether data received at the data pin is “a high or a low logic level,” which means that the input buffer judges a binary bit value of an incoming signal. EX1008, 2:8-24, *see also id.*, 1:14-25 (“[i]nput buffers or receivers...should recognize whether a voltage is intended to be a high or a low voltage”), 2:41-63, 4:4-34, FIG. 2. The input buffer drives the data to the one or more memory cells after judging the data as a high or low logic level. EX1008, FIG. 2.

FIG. 2



EX1008, FIG. 2 (annotated).

75. The memory device disclosed by Akashi also includes an “interface level determiner” connected to an “external terminal” for receiving a “reference voltage VREF.” EX1008, 3:49-58, FIG. 2. Based on the reference voltage VREF, this interface level determiner generates an output value for sending to the input buffer. EX1008, 1:54-2:24, 3:49-4:34, FIG. 2. The input buffer compares this output value with the data received via the data input pin to determine whether the data is the high logic level or the low logic level. EX1008, 1:54-2:24, 3:49-4:34, FIG. 2. In the memory device of Akashi, “all voltages higher than (VREF+0.4) volts are determined as a high voltage, and all voltages lower than (VREF-0.4) volts are recognized as a low voltage” because the input buffer uses the stub series terminate logic (SSTL) specification to judge the input data. EX1008, 1:26-43.

H. Combination of Ryu, Cole, Arcoleo, and Akashi

76. Ryu explains that a non-volatile memory device includes an “output unit” comprising an “input/output buffer.” EX1004, [0041]-[0043], [0058]-[0061], [0076]-[0078], [0090], FIG. 5, Cls. 5, 8, 17, 21. According to Ryu, the “non-volatile memory device may receive or output data through an input/output pin.” EX1004, [0003]. Although Ryu does not expressly describe how Ryu’s non-volatile memory device determines signal levels of incoming data received by the input/output buffer, a POSITA would have recognized that Ryu’s non-volatile memory device somehow determines the levels of signals received by the device (e.g., REB, WEB, DATA[7:0]). EX1004, [0045], [0047]-[0049], [0051], [0056], [0057], [0061]-[0064], [0066]-[0070], FIG. 7. A POSITA would have looked to references like Akashi for details on known solutions to determine signal levels of input data received by an input buffer. One reason for this is because Akashi describes the conventional option of an input buffer that determines logic levels of inputted data signals according to the SSTL specification, which provides a convenient way to discriminate between high logic levels and low logic levels. EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2. Multiple reasons would have prompted a POSITA to implement input buffer circuitry for judging input signal levels in the Ryu-Cole-Arcleo non-volatile memory device based on Akashi’s teachings.

77. **First**, to readily allow the non-volatile memory device to process binary data such as a bit stream of “1s” and “0s,” a POSITA would have been motivated to

implement the non-volatile memory device of the Ryu-Cole-Arcoleo combination to include an input buffer that is configured to judge input data as a high logic level or a low logic level as suggested by Akashi. A POSITA would have recognized that it is beneficial for an input buffer to determine the binary values of input data so that the correct data values can be saved to the memory banks or otherwise processed because memory devices handle large volumes of binary data.

78. **Second**, a POSITA would have understood that it provides a straightforward solution to identify data bits while ignoring baseline noise to implement the non-volatile memory device of Ryu with Akashi's suggestion of a reference voltage and a buffer zone to differentiate between a high logic level and a low logic level. For example, Akashi explains that "the SSTL specification dictates that all voltages higher than ($V_{REF}+0.4$) volts are determined as a high Voltage, and all Voltages lower than ($V_{REF}-0.4$) volts are recognized as a low voltage," which means that no determination is made in an 0.8 volt buffer zone surrounding the reference voltage. EX1008, 1:26-44. A POSITA would have appreciated that this would result in baseline noise not being misjudged as a high or low data bit, therefore improving the accuracy of judged data bits received at the device.

79. **Third**, it would have been obvious to implement the non-volatile memory device of the Ryu-Cole-Arcoleo combination such that the input buffer supports terminated signaling as taught by Akashi, including SSTL. This would

promote signal integrity in high-speed signaling environments. For example, terminated signaling decreases an extent to which signals oscillate and overshoot through resistors that absorb signals instead of reflecting signals. A POSITA would have understood that separation can be maintained between buses, as such terminated signaling would improve an ability of the non-volatile memory device to handle greater volumes of data in a short amount of time. EX1008, 1:26-43.

80. ***Fourth***, a POSITA would have understood that implementing the non-volatile memory device of the Ryu-Cole-Arcoleo combination so that each common data signal received by the memory device is judged by a respective configurable input buffer have a high or low logic level, as taught by Akashi, would yield predictable benefits. A POSITA would have understood that it is beneficial for a configurable input buffer to judge the logic level of each signal independently when a memory device receives more than one common data signal, which would be the predictable result of implementing the non-volatile memory device of Ryu-Cole-Arcoleo with the configurable input buffer of Akashi that judges the logic level of one bit stream.

81. ***Fifth***, a POSITA would have found it obvious to combine the teachings of Ryu-Cole-Arcoleo with Akashi because the combination merely involves the application of a known technique to a known system to achieve predictable results.. Here, Akashi recognized a problem with judging logic levels of data in terminated

signaling platforms and described a straightforward technique to address it. In this context, combining the teachings of Ryu-Cole-Arcoleo and Akashi would have been obvious and a POSITA would have reasonably expected success, especially since the combination involves well-known techniques for using input buffers to receive input data at a memory device and standard hardware/software present in input buffers that was well known before the Critical Date.

I. Combination of Ryu, Cole, Arcoleo, Grundy, and Akashi

82. For each of the reasons I described above in my analysis of the Ryu0Cole-Arcoleo-Akashi combination (*Supra*, §VII.H) that a POSITA would have been motivated and found it obvious to apply Akashi’s teachings to the Ryu-Cole-Arcoleo combination, a POSITA likewise would have been motivated and found it obvious to apply Akashi’s teachings to the Ryu-Cole-Arcoleo-Grundy combination.

VIII. MANNER IN WHICH THE PRIOR ART REFERENCES RENDER THE ’028 CLAIMS UNPATENTABLE

A. GROUND 1A: The Ryu-Cole-Arcoleo Combination Renders Claims 1-3 and 10-17 Obvious

Element [1pre]: A configurable non-volatile memory device comprising:

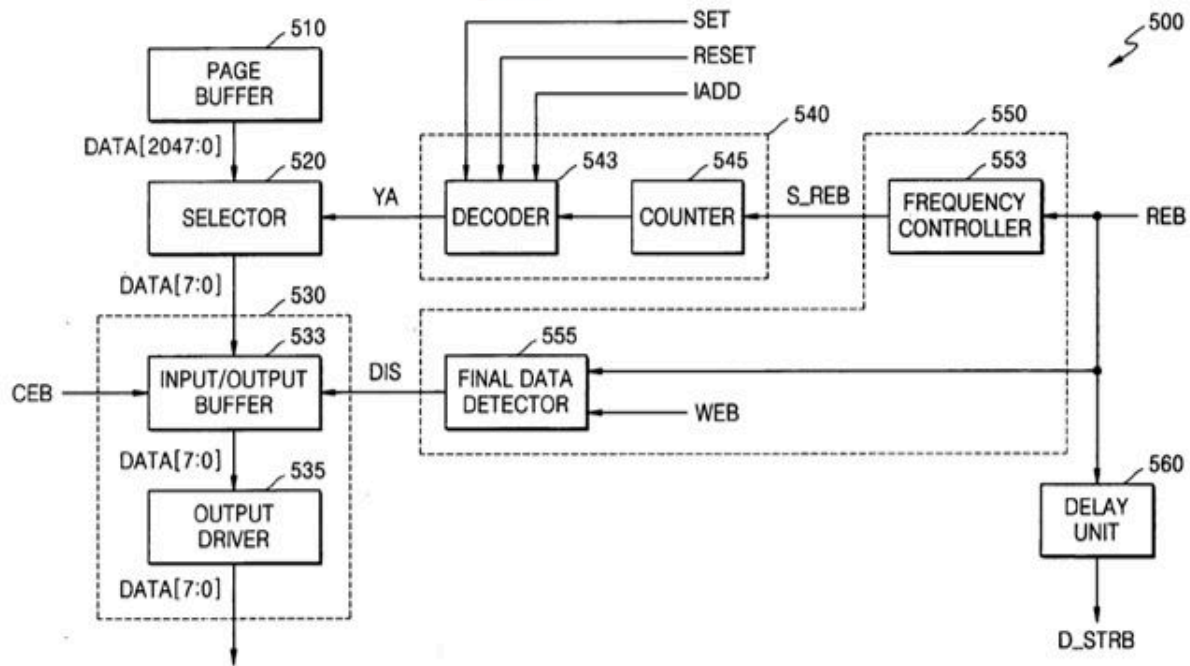
83. The Ryu-Cole-Arcoleo combination renders obvious a “configurable non-volatile memory device,” even to the extent that the preamble is considered a limitation. I noticed that very prominently in the “SUMMARY OF THE INVENTION” and the “DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS,” Ryu expressly discloses a “*non-volatile memory device*.”

EX1004, [0009] (“According to some embodiments of the present invention, a non-volatile memory device is operated by ...”), [0036] (“Exemplary embodiments of the present invention are described herein in the context of a NAND flash memory. It will be understood, however, that the present invention can be embodied in various nonvolatile memory devices ...”); *see also id.*, [0002]-[0005], [0007], [0009], [0012]-[0014], [0042], [0046], [0047], [0062], [0064], [0065], [0069], [0070], [0072], [0076], [0077], FIGs. 5, 11.

84. The Ryu-Cole-Arcoleo ***non-volatile memory device*** is also ***configurable***. For example, Ryu discloses that an “output unit” of the non-volatile memory device can be “activated in response to an enable signal (CEB) and....deactivated in response to a disable signal (DIS),” which means that the ***non-volatile memory device*** is ***configurable***. EX1004, [0043], [0059]-[0061], [0078], FIGs. 5, 11. Further, as I described above in my analysis of the Ryu-Cole-Arcoleo combination, the ***memory device*** includes a ***configurable*** input section as taught in Cole and a ***configurable*** output buffer as taught in Arcoleo. *Supra*, §§VII.A-D. The ***configurable*** input section and the ***configurable*** output buffer both independently provide ways to configure the non-volatile memory device. Ryu also expressly discloses that the non-volatile memory device includes a “non-volatile memory array” that is “not shown” in FIGs. 5 and 11, further confirming my opinion that Ryu’s device is a ***non-volatile memory device***. EX1005, [0042], [0077].

Non-volatile memory device

FIG. 5



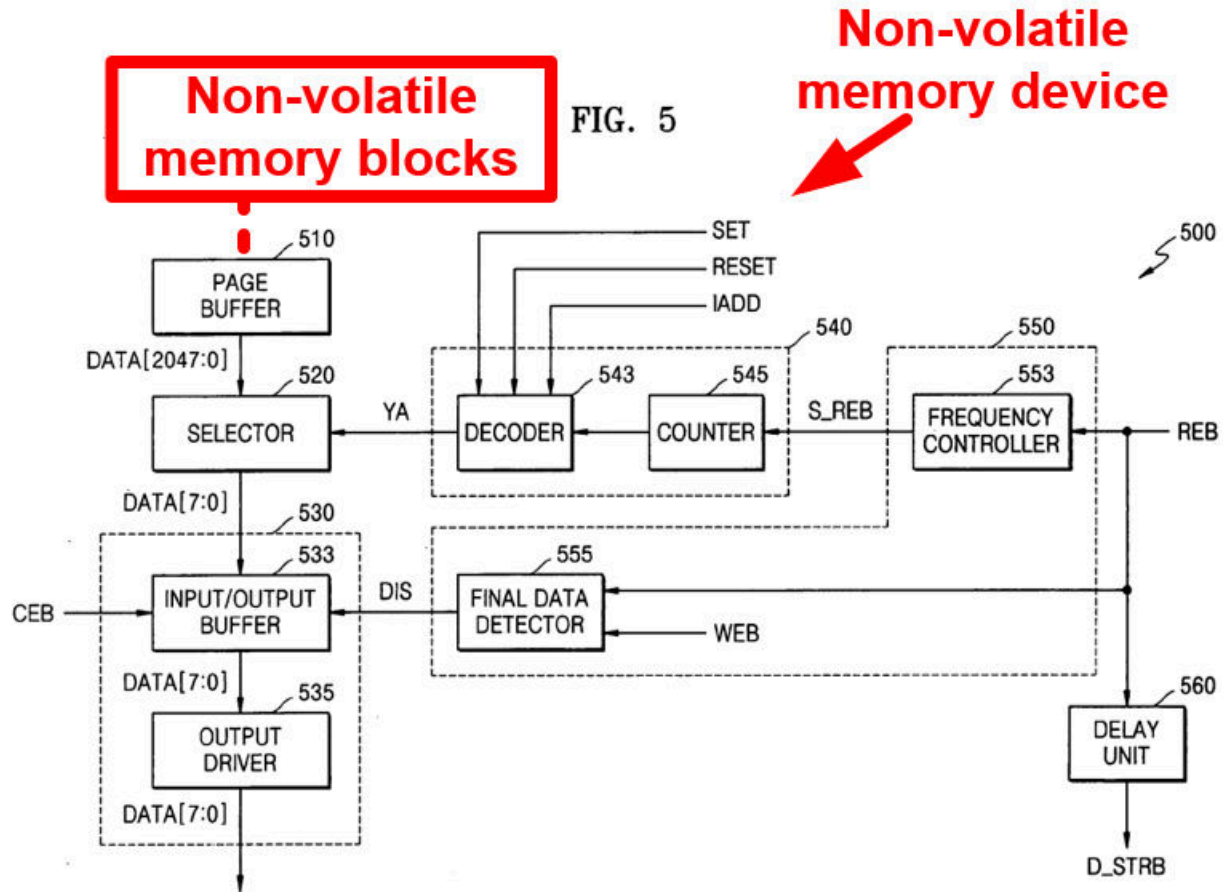
EX1004, FIG. 5 (annotated).

Element [1a]: plurality of non-volatile memory blocks;

85. It is apparent that the Ryu-Cole-Arcoleo combination renders obvious [1a]. For example, the ***non-volatile memory device*** includes a “page buffer.” Ex1004, [0042], [0046], [0047], [0055], [0058], [0076], [0077], [0081]. This page buffer “stores a portion of data stored in a non-volatile memory array (not shown).” EX1005, [0042]; *see also id.*, [0042] (“DATA[2047:0] stored in the page buffer 510”), [0046] (“page buffer... receives and stores data from a non-volatile memory array”), [0077], Cls. 5, 17. It is apparent that the non-volatile memory array described by Ryu includes a ***plurality of non-volatile memory blocks***. My opinion

here is supported by the fact that Ryu's memory array is implemented "in the context of a NAND flash memory" in one embodiment, and in other embodiments can be implement in "a NOR device, an AND device, a DINOR (Divided bit-line NOR) device, a OneNAND device, and a FRAM (Ferroelectric RAM)." EX1004, [0036]. Each of these embodiments of memory devices involve memory devices that have a ***plurality of non-volatile memory blocks*** for storing data.

86. My opinion is also supported by the fact that according to the '028 Patent, a POSITA would have understood that flash memory is conventionally "organized into blocks." Cf. EX1001, 17-24 ("organized into blocks to facilitate block erasure"), FIG. 4; *see also* EX1010, 15:15-34 (corroborating that "memory cell arrays" are "divided into...blocks"); EX1011, 1:45-54 (corroborating that cells in a flash memory array are "grouped into blocks"); EX1012, 4 (corroborating that a "bank of flash memory" includes a plurality of blocks). This means that the '028 Patent concedes a ***non-volatile memory device*** includes a ***plurality of non-volatile memory blocks***. The '028 Patent also explains that "[m]ost commercially available NAND flash memory devices are configured to have two banks of memory." EX1001, 2:22-24. According to the '028 Patent, therefore, a POSITA would have understood that the embodiment of Ryu's ***non-volatile memory device*** involving a NAND flash memory includes at least two memory banks each organized into blocks, resulting in a ***plurality of non-volatile memory blocks***. *Id.*



EX1004, FIG. 5 (annotated).

87. Furthermore, the '028 Patent uses the term “memory *array* bank” and “memory bank” interchangeably. EX1001, 12:50-67 (describing techniques for “accessing the memory array banks 302 and 304” and explaining that “the memory array can be organized as a single memory bank or more than two memory banks”), FIG. 4. Because the '028 Patent acknowledges that “[t]hose skilled in the art will understand that flash memory is organized into banks, and *each bank is organized into blocks*,” a POSITA would have understood that Ryu’s non-volatile memory array is likewise organized into memory blocks. EX1001, 2:20-22; EX1004, [0042],

[0077]. It is also clear that a POSITA would have understood Ryu's non-volatile memory array to include a ***plurality of non-volatile memory blocks*** by the Critical Date of the '028 Patent. *See also* EX1010, 15:15-34 (describing "memory cell arrays" that are "divided into...blocks"); EX1011, 1:45-54 ("describing flash memory array including cells that are "grouped into blocks"); EX1012, 4 (depicting a "bank of flash memory" including a plurality of blocks). It would have been obvious at a minimum for a POSITA to implement Ryu's memory device with a plurality of non-volatile memory blocks to attain well-known benefits of such an organization, including to facilitate block erasure.

Element [1b]: a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;

88. It is clear that The Ryu-Cole-Arcoleo combination renders obvious [1b]. As I described in my analysis of Element [1pre], *supra*, the ***non-volatile memory device*** of Ryu includes an "output unit" (e.g., output unit 530, output unit 1130) that "is activated in response to an ***enable signal*** CEB."¹ EX1004, [0043], *see also id.*, [0059]-[0051], [0078], FIGs. 5, 11. More specifically, Ryu explains that "[t]he input/output buffer 533 outputs or blocks the data DATA[7:0] in response to the enable signal CEB." EX1004, [0060]. This disclosure makes it apparent that a Ryu's

¹ All emphasis added unless otherwise indicated.

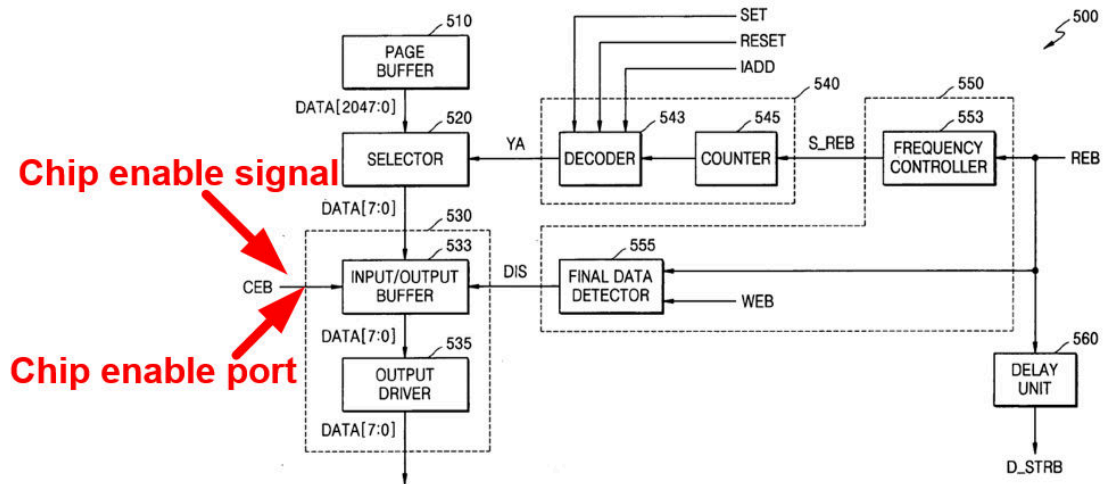
enable signal CEB to represents a *chip enable signal* for enabling the *configurable non-volatile memory device*.

89. I noticed that Ryu's *enable signal* CEB activates the output unit of the *non-volatile memory device* which includes a memory *chip*, and this is consistent with conventional functionality of chip enable signals by the Critical Date of the '028 Patent. My opinion here is corroborated by multiple references that use the acronym "CEB" to refer to an active low chip enable signal, and specifically, an active low chip enable signal where 'B' (for "bar" or complement) indicates active low. EX1026, [0036] (describing a chip enable signal "CEB" that "enables [a] semiconductor memory device"); EX1032, 4:5-14 (describing a "chip enable signal CEB" that enables a buffer to receive signals). Multiple references make it clear that the notation "CEB" was also commonly used as a shorthand for a chip enable signal in the field of circuit design by the Critical Date. EX1023, 3 (describing a chip enable signal "CEB"); EX1024, 5:34-63 ("CEB indicates a chip enable terminal"); EX1025, 4:56-5:5 (describing a "chip enable signal buffer 10" that receives a chip enable signal "CEB")). Although the acronym "CEB" is often used to refer to an active low chip enable signal, this is not the only way to refer to a chip enable signal. Other acronyms and symbols that can be used to refer to a chip enable signal include "CE#" and " $\overline{CE}$." EX1013, 13:54-67 (using "CE#"); EX1014, FIG. 1 (using " $\overline{CE}$ "). A

POSITA would have understood that the “#,” “B,” and over-bar symbols represent means to indicate a complement (or active low) signal.

90. A POSITA would have understood that Ryu’s *non-volatile memory device* would receive the *chip enable signal* CEB via a *chip enable port*, because this would permit the *non-volatile memory device* to receive the CEB signal from an external source. At the very least, this providing a physical interface for the non-volatile memory device would have been obvious to a POSITA. My opinion here is corroborated by multiple references that describe memory devices receiving chip enable signals from external sources. EX1013, 13:54-67 (describing each “flash chip” as including a chip enable port receiving a chip enable (CE#) signal); EX1013, 3:20-50 (describing a memory device that receives two chip enable signals, including a signal for “stand-by mode/operative mode”). This understanding is also consistent with the depiction of the CEB signal originating from an external source as illustrated in FIG. 5 of Ryu. *Id.*

FIG. 5



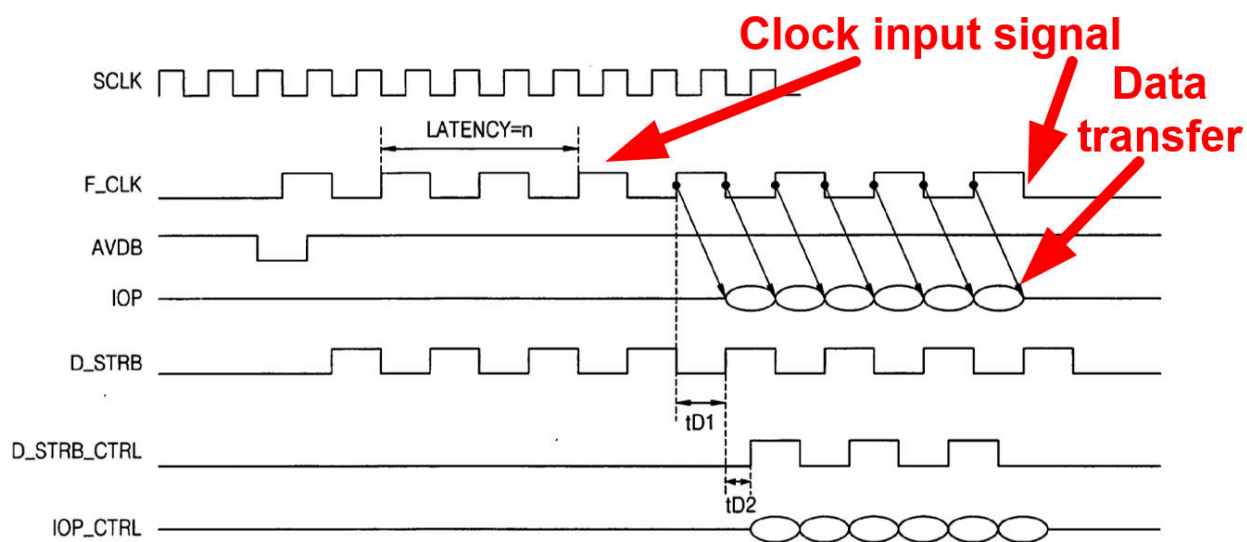
EX1004, FIG. 5 (annotated).

91. The '028 Patent also acknowledges that chip enable signals were known in “*prior art* flash memory system[s]” for a memory device to include a chip enable port configured to receive a chip enable signal. EX1001, 1:54-2:16, 2:36-52, FIG. 1. The '028 Patent explains that such prior art memories commonly included a *plurality of memory devices* that each receive a *chip enable signal* (CE#) via a *chip enable port*. EX1001, 1:54-2:52, FIG. 1. Consequently, the '028 Patent acknowledges that “a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device” was known by the Critical Date of the '028 Patent. *Id.*

Element [1c]: a first clock input port configured to receive a first clock input signal; a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;

92. The Ryu-Cole-Arcoleo combination renders obvious [1c]. The *non-volatile memory device* of Ryu discloses a system clock to synchronize operations of the memory device. EX1004, [0003] (“SCLK represents a system clock”), [0062], [0063], FIGs. 1A-1B, FIG. 7. The read control signal (REB) of Ryu represents a timing signal that synchronizes read operations on the device. *Id.* One cycle of the system clock is equal to one half cycle of the read control signal, because the read control signal is exactly half the frequency of the system clock. *Id.* Ryu describes another embodiment where a flash clock signal (F_CLK) is exactly half the frequency of the system clock and synchronizes read operations by the memory device. EX1004, [0080], [0083]-[0088], [0091], [0092], [0094], FIGs. 11, 12. In this embodiment, F_CLK represents a free-running clock signal that operates before and after data transfer events at Ryu’s input/output pin, as demonstrated below in FIG. 12. EX1004, [0080], [0083], [0094], FIGs. 11-12.

FIG. 12

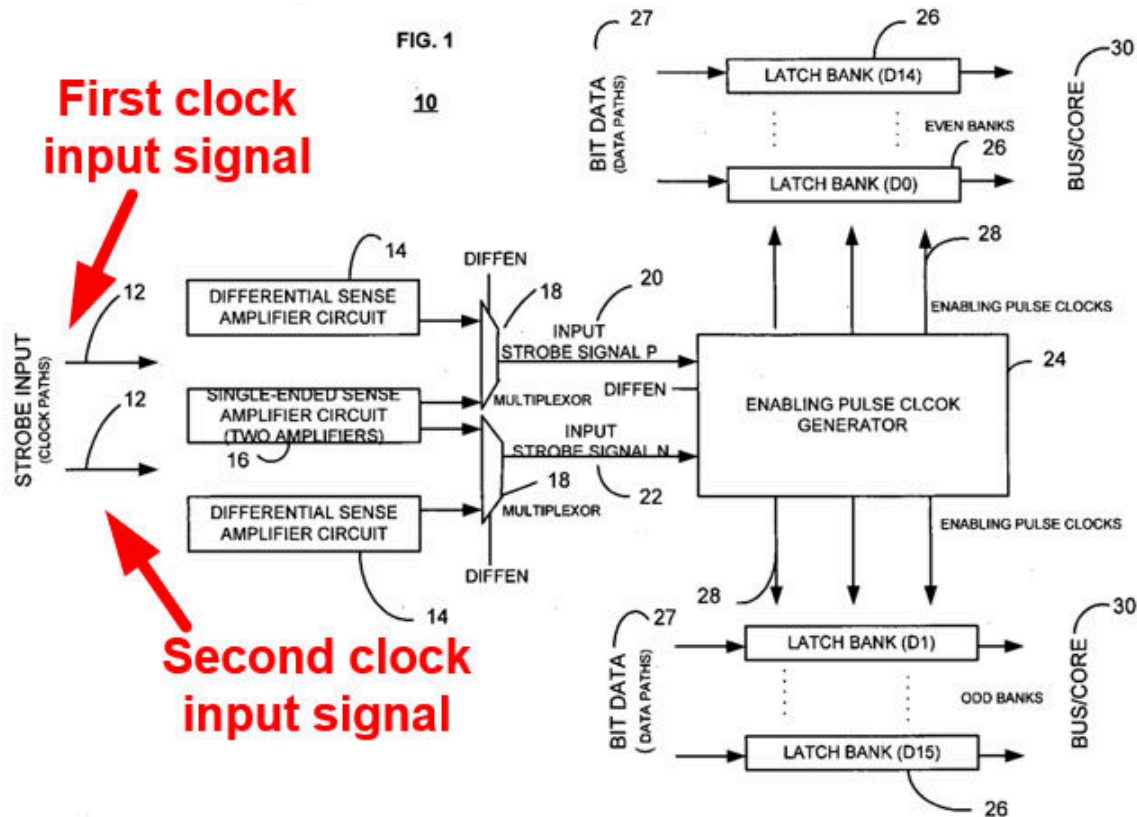


EX1004, FIG. 12 (annotated).

93. As I explained in my analysis of the Ryu-Cole-Arcoleo combination (*Supra*, §VII.D), a POSITA would have been motivated to modify Ryu’s *non-volatile memory device* to include an “input section” as described by Cole. EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, §VII.B, §VII.D. Cole explains that this input section receives “strobe inputs” for controlling “latch banks” to cycle data through one or more “input data paths.” EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, §VII.B, VII.D. According to Cole, the “strobe inputs 12 are provided by the source of the data being transferred” such that “the data may be transferred source synchronously.” EX1005, [0020]; *see also id.*, (“strobe inputs 12 may be provided in parallel with the data”), [0019], FIGs. 1, 2A, 2C.

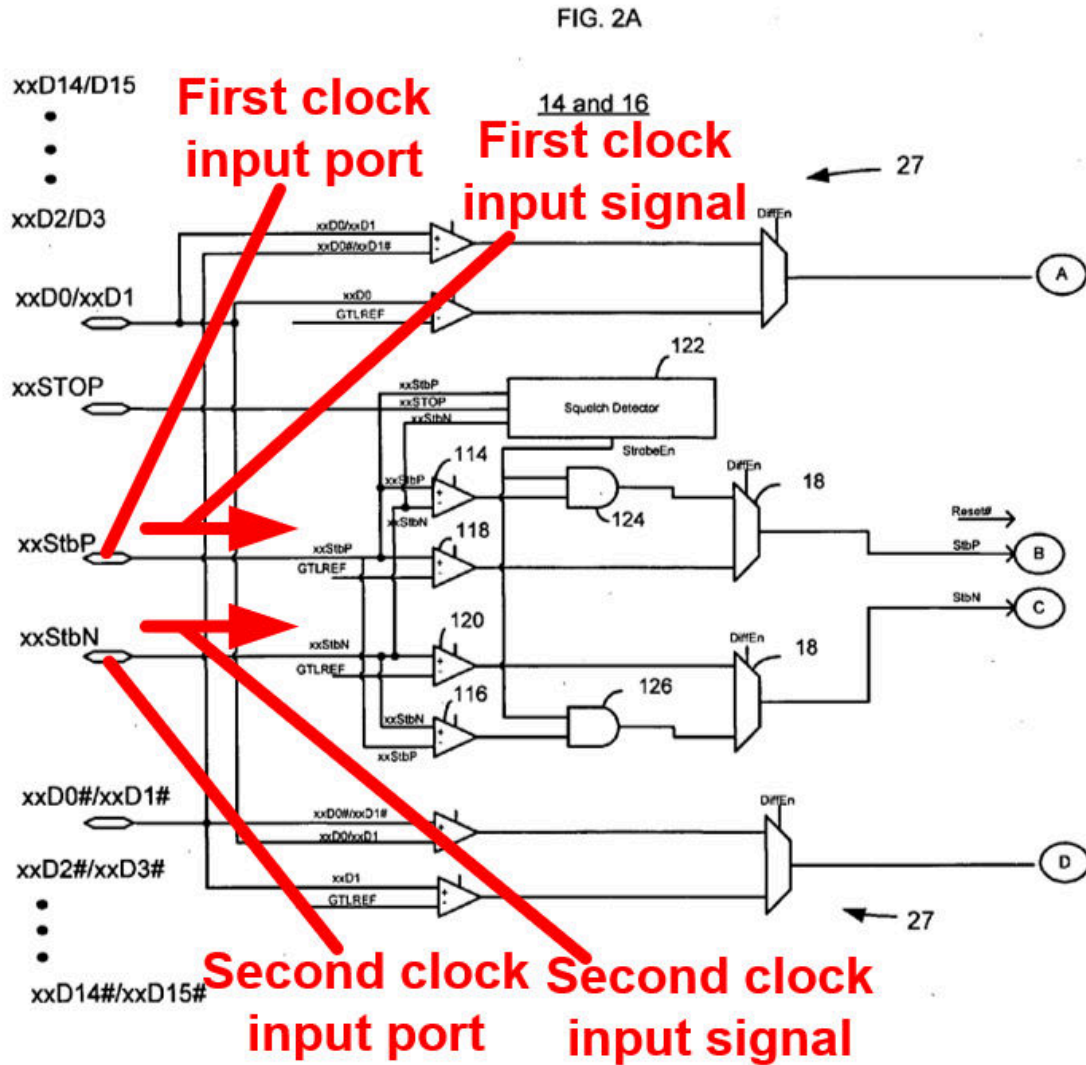
94. Cole uses the terms “strobe inputs” and “CLOCK PATHS” interchangeably to refer to inputs 12. EX1005, FIG. 1 (“STROBE INPUT (CLOCK PATHS)”). The “xxStbP” signal of Cole represents a first of these strobe inputs or clock paths 12 that provides a *first clock input signal*. EX1005, [0026], FIG. 2A, FIG. 2C. The “xxStbN” signal represents a second of these strobe inputs or clock paths 12 that provides a *second clock input signal*.² *Id.*

² I have been informed that Patent Owner made allegations of infringement in a district court proceeding that equate a data strobe with a clock signal. EX1100, 52-53; EX1101, 21-28; EX1102, 17-21. My analysis here (which involves mapping data strobe inputs to clock input signals) is based on Patent Owner’s interpretation of clock signals as encompassing data strobes. In my analysis of Ground 1B, I provide additional obviousness arguments addressing another interpretation. *Infra*, §VIII.B.



EX1005, FIG. 1 (annotated).

95. As taught in Cole, the input section of the Ryu-Cole-Arcoleo memory device predictably includes a *first clock input port* for receiving the *first clock input signal* “xxStbP” and a *second clock input port* for receiving the *second clock input signal* “xxStbN.” EX1005, [0019], [0020], [0026], [0027], FIG. 2A, FIG. 2C. The port symbols on the left-hand side of FIG. 2A clearly demonstrate this, as one port is labeled with “xxStbP” and another port is labeled with “xxStbN.” *Id.*



EX1005, FIG. 2A (annotated).

96. It is clear, therefore, that the strobe inputs 12 of Cole can be represented as “xxStbP” and “xxStbN.” EX1005, FIG. 2A. Although in one embodiment, the *first input signal* of Cole can be a positive strobe input “xxStbP” and the *second input signal* of Cole can be a negative strobe input “xxStbN,” this can be reversed in an alternative embodiment where the *first input signal* is represented by the negative strobe input and the *second input signal* is represented by the positive

strobe input. EX1005, [0019], [0020], [0026], FIG. 1, FIG. 2A. In any case, the strobe signals of Cole together represent a first *clock input signal* and a *second clock input signal* that are received by the input section. *Id.*

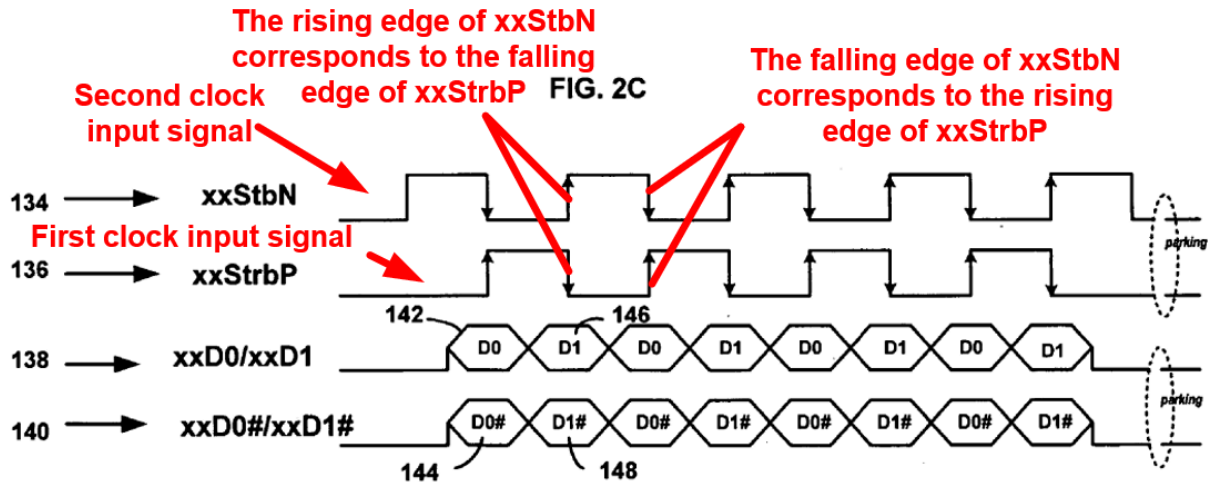
97. Cole explains that “sense amplifier circuits...provide strobe signals...in accordance with at least strobe inputs 12.” EX1005, [0019]. These sense amplifier circuits include “sense amplifiers 118/120” that each receive “one of the two strobe signals” and “sense amplifiers 114 and 116” that each receive “both...strobe signals.” EX1005, [0026]. I noticed that FIG. 2A of Cole depicts sense amplifier 118 as receiving strobe input “xxStbP,” the *first clock input signal*, and depicts sense amplifier 120 as receiving strobe input “xxStbN,” the *second clock input signal*. EX1005, [0026]. FIG. 2A also depicts sense amplifiers 114 and 116 receiving both *clock input signals* “xxStbP” and “xxStbN.” *Id.* It is clear that when the *non-volatile memory device* of Ryu is implemented with the input section of Cole, the device includes a *first clock input port* for receiving the *first clock input signal* “xxStbP” and a *second clock input port* for receiving the *second clock input signal* “xxStbN.” EX1005, [0019], [0020], [0026], [0027], FIG. 2A, FIG. 2C. My opinion here is supported by the fact that port symbols on the left-hand side of FIG. 2A indicate the inputs for *clock input signals* “xxStbP” and “xxStbN.” *Id.*

98. The *first clock input signal* “xxStbP” and the *second clock input port* for receiving the *second clock input signal* “xxStbN” ultimately drive latching

operations of data through input data paths of the input section. EX1005, [0016]-[0022], FIG. 1. In the context of these data paths, Cole expressly discloses that “to achieve at least the same data transfer rate for a given *set of pins* (16 for the embodiment), the embodiment is designed to allow data to be transmitted on each data path.” EX1005, [0025], FIG. 2A. The input section of Cole includes two pins for each pair of “data paths.” (i.e., xxD0, xxD1, and so on). *Id.* This results in “two streams of data bits” being “multiplexed on each pair of data paths, xxD0/xxD1, xxD0#/xxD1#, xxD2/xxD3, xxD2#/xxD3#, and so forth.” *Id.* The prefix “xx” is commonly understood to be a universal symbol for a port on an integrated circuit. Each of these pins disclosed by Ryu represents a **port** for receiving input data. *Id.* I noticed that Cole uses the same “universal port” symbol to depict the ports (inputs) for the **first clock input signal** (xxStbP) and the **second clock input signal** (xxStbN), and these port symbols are also used by Cole for the data input pins, which means that the inputs for the **clock input signals** in Cole are **ports**. *Id.* Consequently, it is clear that Cole’s pin for receiving xxStbP represents a **first clock input port** and the pin for receiving xxStbN represents a **second clock input port**. *Id.*

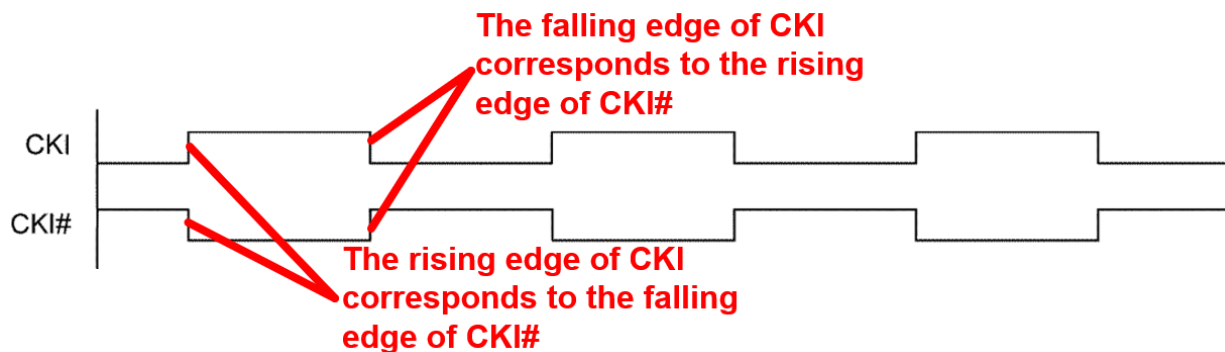
99. The **first clock input signal** represented by “xxStbP” and the **second clock input signal** represented by “xxStbN” are clearly **complementary**, and a POSITA would have understood this. This is supported by the fact that “xxStbP” and “xxStbN” are the inverse of one another such that the rising edges of xxStbN

are aligned with falling edges of xxStbP and falling edges of xxStbN are aligned with rising edges of xxStbP. EX1005, [0019], [0020], [0026], [0027], FIGs. 2A, 2C.



EX1005, FIG. 2C (annotated).

100. I noticed that the complementary strobe input signals disclosed in Cole are strikingly similar to the complementary strobe input signals described by the '028 Patent, which also include contemporaneous pairs of rising and falling edges.



EX1001, FIG. 2B (annotated).

101. My opinion here is supported by multiple references confirming that it was well known by the Critical Date of the '028 Patent for complementary clock signals to have aligned pairs of rising edges and falling edges. *See, e.g.*, EX1015, 2 (describing two complementary clock signals having aligned rising and falling edges; EX1016, FIG. 3A (depicting two complementary clock signals). The ***non-volatile memory device*** of the Ryu-Cole combination therefore includes a ***first clock input port*** configured to receive a ***first clock input signal*** and a ***second clock input port*** configured to receive a ***second clock input signal*** that is ***complementary*** to the ***first clock input signal***, when the memory device of Ryu is implemented with the complementary clock signals of Cole. EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, §VII.D.

Element [1d]: a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;

102. It is apparent that the Ryu-Cole-Arcoleo combination renders obvious [1d]. I noticed, for example, that Ryu's ***non-volatile memory device*** includes a "delay unit" that receives the read control signal REB. EX1004, [0064], [0068], [0092], [0095], FIGs. 5, 12. This delay unit generates a D_STRB signal to be "output at the same time with the data DATA[7:0] to the external source." EX1004, [0064], *see also id.*, [0065]-[0070], [0092], [0095], FIGs. 5, 7, 11, 12, Cls. 10, 22. Ryu explains that in some examples, the D_STRB signal "is generated by delaying the read control signal by a predetermined delay time" and the D_STRB signal "is output with the

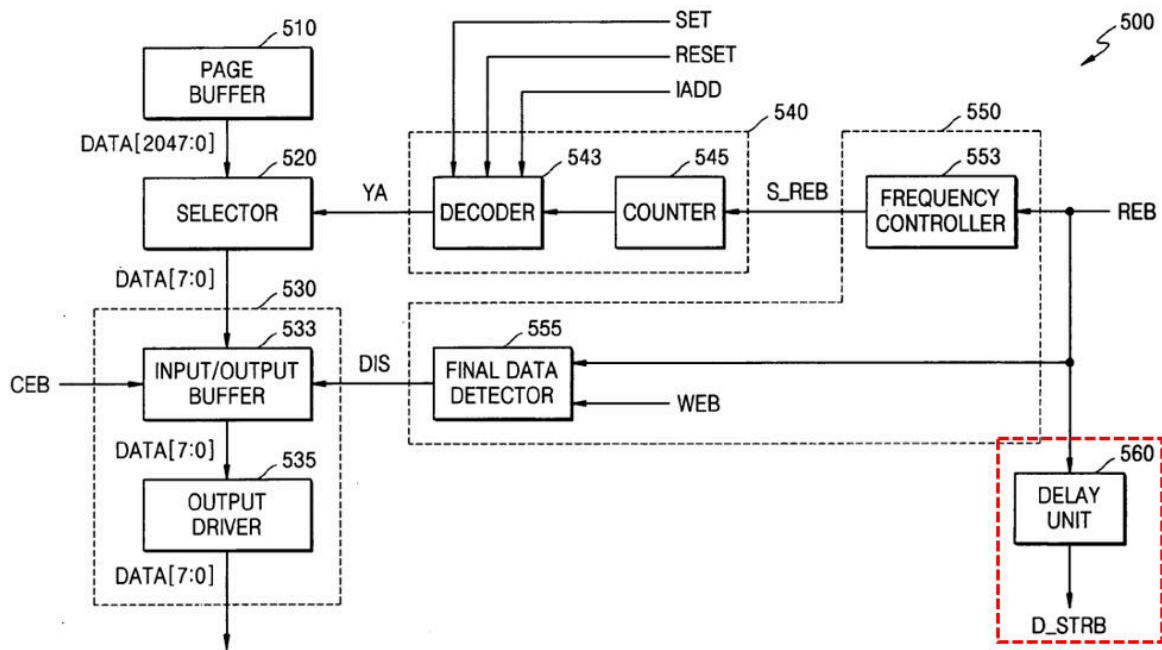
data concurrently to an external source.” EX1004, [0011], [0016], *see also id.*, [0064], [0091], Cls. 10, 22. In some examples, the D_STRB signal “is created by delaying the flash clock signal F_CLK by a predetermined time and [is] output at the same time with the data DATA[7:0] to an external source.” *Id.*, [0091]-[0095].

103. Because the D_STRB signal indicates a timing of data output from the *non-volatile memory device*, it is clear that Ryu’s D_STRB is an *output signal* that indicates the exact timing of output data presented at an input/output pin (IOP) of the device. Again, I have been informed that Patent Owner made infringement allegations in district court that rely on an interpretation of “clock signal” as including strobe signals. *See infra*, Ground 1B at [1d] (addressing an interpretation of *clock output signal*). Based on this interpretation, it is clear that Ryu’s D_STRB signal provides a *clock output signal* as claimed. *Id.*

104. The *non-volatile memory device* comprises an *output port* configured to transmit D_STRB to a downstream device, and this is confirmed by the fact that D_STRB is “output” from the *non-volatile memory device*. *See* EX1004, [0064]-[0070], [0091]-[0095] (data “is transmitted from the non-volatile memory device 1100 to the external controller” and the non-volatile memory device 1100 outputs a D-STRB signal “for indicating the time when the controller fetches the data”). According to Ryu, transmission of D_STRB and transmission of data (e.g., DATA[7:0]) occur synchronously and in parallel. EX1005, [0022] (“[s]trobe ...

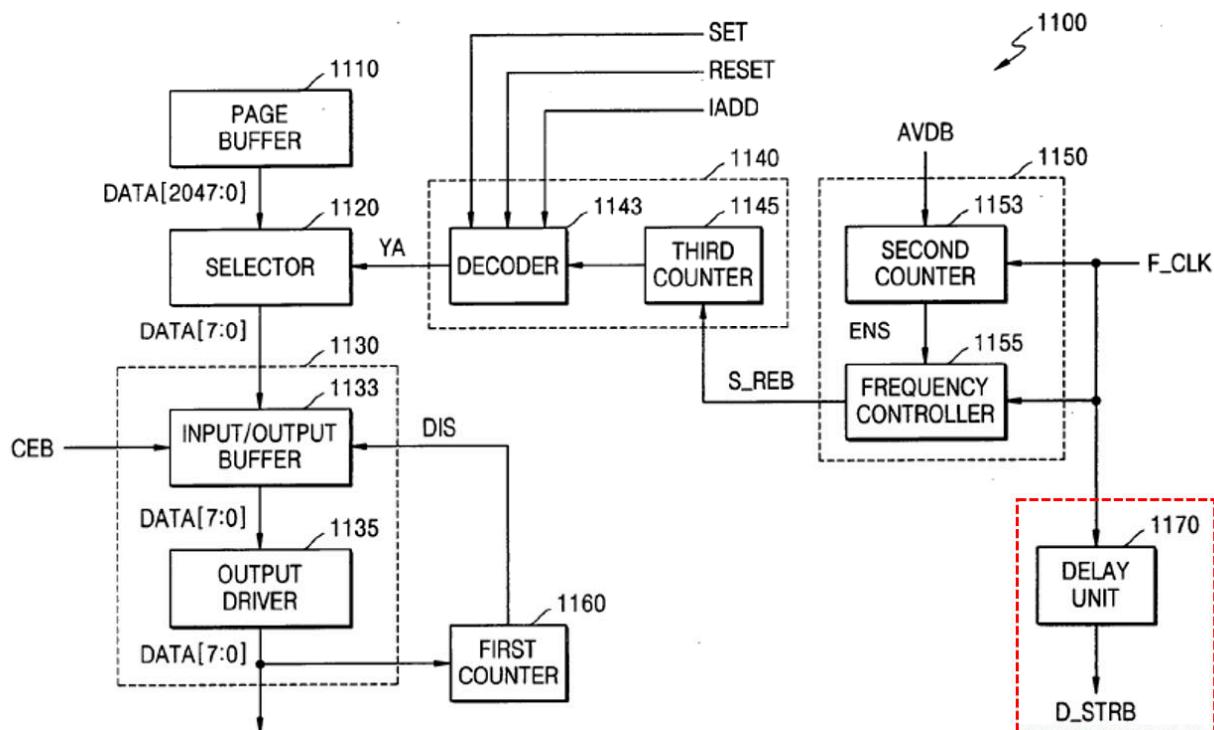
provided in parallel with the data”). It is clear that D-STRB would be transmitted from an *output port* in parallel with output data transmitted from the input/output pin (IOP), and a POSITA would have understood this. My opinion here is consistent with the fact that separate output arrows for D_STRB and output data are depicted in FIGs. 5 and 11 of Ryu. EX1004, [0011] (“The data strobe signal is output with the data concurrently to an external source.”), FIGs. 5, 11; Multiple references corroborate the fact that it was well known for memory devices to have separate data and strobe output ports. EX1007, 7:18-9:34 (describing terminals including ports for data outputs and strobe outputs); EX1009, [0084]-[0091] (describing ports of a memory device for outputting clock signals, data signals, and signals indicating timing of data and commands). Transmitting D_STRB in parallel with the data on a distinct output port also would have been obvious to eliminate the need for D_STRB to be extracted from the data by the downstream device that receives the signals. EX1005, [0020].

FIG. 5



EX1004, FIG. 5 (annotated).

FIG. 11



EX1004, FIG. 11 (annotated).

105. Referencing the the D_STRB signal of Ryu (which represents a *clock output signal*)³ to a *first clock input signal* would have been obvious to a POSITA in the context of the Ryu-Cole-Arcoleo memory device. Because Ryu expressly discloses “delaying the flash *clock signal* F_CLK by a predetermined time” to generate D_STRB, it is clear that Ryu specifically contemplates D_STRB being referenced to a flash clock signal. EX1004, [0094], FIG. 11; *see also id.*, [0091]-

³ *Supra*, Footnote 2.

[0095], [0064] (“D_STRB may [be] created by delaying the read control signal REB”). The flash clock signal (F_CLK) of Ryu is one example of a ***first clock input signal***, because F_CLK is a free-running signal that is active even when data transfer is not occurring. EX1004, [0080], [0083], [0094], FIGs. 11-12.

106. Furthermore, Cole describes an input section of an integrated circuit that receives complementary input signals xxStbP and xxStbN, where xxStbP provides another example of a first clock input signal.⁴ *Supra*, [1c]. Referencing Ryu’s D_STRB signal (which represents a ***clock output signal***⁵) to one of Cole’s complementary strobe input signals, such as xxStbP, would have been obvious to a POSITA. One reason for this is because D_STRB would then indicate an exact timing of values in the output data presented at the input-output pin (IOP). Another reference published before the Critical Date of the ’028 Patent confirms that it would have been obvious to reference a data strobe signal to a clock input signal. EX1009, [0047]-[0048]). For example, a POSITA would have appreciated that memory devices like Ryu’s are commonly chained together and configured to pass data/commands from one device to another until the data/commands reach a target memory device in the chain where the data/commands are to be processed. EX1009,

⁴ *Supra*, Footnote 2.

⁵ *Supra*, Footnote 2.

[0030] (“memory devices are chained to one another” and “[c]ommands and data received within a given memory device are retransmitted to a subsequent memory device ... By this operation, commands and data propagate rapidly through the chain...”), FIG. 3 (depicting chained memory devices), FIG. 5A (same), FIG. 17 (depicting clock output signal referenced to clock input signal used in passing data/commands from one device to another). It would have been obvious for the output timing information (e.g., D_STRB) to be referenced to the input timing information (e.g., xxStbP) so that the output timing information (e.g., D_STRB) would match the input timing information (e.g., xxStbP) for the same data but delayed by an amount corresponding to the propagation delay of the input data. This would ensure efficient passing of input data and timing information (e.g., xxStbP) received from a prior memory device to a next device in the chain. EX1009, [0048] (corroborating that “each of the signals retransmitted by the initial memory device 155₁ is delayed by the same (or substantially the same) propagation delay, t_p ”). This would have been obvious to ensure the output timing information (e.g., D_STRB) was synchronized with the data being passed to the next device in the chain. *Id.*

Element [1e]: one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;

107. The Ryu-Cole-Arcoleo combination renders obvious [1e]. One thing I noticed is that the '028 Patent acknowledges several features recited in element [1e] to be prior art. EX1001, 1:53-2:16, FIG. 1. This includes “one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data, and output data.” *Id.* The '028 Patent expressly concedes that a “prior art” flash memory system illustrated in FIG. 1 includes a “[c]hannel 18 includ[ing] a set of common buses, which include data and control lines that are connected to all its corresponding memory devices,” the memory system including memory controller that transmits “commands and data, via the channel 18” and “[d]ata read from the memory devices is transferred via the channel 18.” *Id.*; *see also id.*, 2:20-22 (“Those skilled in the art will understand that flash memory is organized into banks, and each bank is organized into blocks to facilitate block erasure.”).

108. My opinion that Element [1e] would have been rendered obvious is confirmed by the teachings of Ryu and Cole. For example, Ryu explains that a ***non-volatile memory device*** can “receive or output ***data*** through an input/output pin in synchronization with rising edges and/or falling edges of a read control signal and/or write control signal when reading or writing ***data***.” EX1004, [0003], *see also id.*, [0005]-[0007], [0009], [0037] (“a write control signal for controlling a write of the data”) [0038], [0041]-[0043], [0059], [0060], [0062], [0067], [0069], [0072], [0078],

FIGs. 5, 7, 11, 12. When the *non-volatile memory device* receives data via the “input/output pin” and writes this data to the non-volatile memory array, this represents *input data*. *Id.* When the *non-volatile memory device* reads data from the non-volatile memory and outputs this data from an “input/output pin,” this represents *output data*. It is clear, therefore, that Ryu’s “input/output pin” provides one example of a *common data port* configured to transfer *common data signals* carrying at least *input data* and *output data*. *Id.*

109. My opinion here is confirmed by the fact that Cole describes the input section of the IC to include input/output ports for receiving data from a bus and to transmit data over the bus. EX1005, [0016], [0023], FIGS. 1, 2A-2B (disclosing data paths 27 including latch banks 26 and corresponding data ports), [0043]-[0044], FIG. 8 (bus 808). A POSITA would have understood that the one or more common data ports can also include separate input ports and output ports, and this is corroborated by a reference that includes such ports. *Id.*; EX1009, [0030], FIGS. 3, 5A, 17. Cole also explains that each of latch banks 26 includes “deskewing latches” that capture “bit data received via data paths 27.” EX1005, [0023], *see also id.*, [0016] (“[l]atch banks 26 may be employed to latch and temporarily store the data being transferred to the IC”). Cole also discloses that “data are provided to the 16 latch banks 26 via 16 corresponding data paths 27.” EX1005, [0025].

110. The *non-volatile memory device* further includes a *port* for transferring data signals carrying *command data* (e.g., REB_CTRL, WEB_CTRL) to control read and write operations. EX1004, [0005], [0066]. For example, Ryu discloses that “REB_CTRL is a read control signal generated from the controller...and is applied to the nonvolatile memory device” and “WEB_CTRL is a write control signal generated from the controller...and is applied to the nonvolatile memory device.” EX1004, [0066], *see also id.*, [0005] (“[a] controller...for controlling the non-volatile memory device applies a read control signal...to the non-volatile memory device”), FIG. 5, FIG. 7. Additional control signals applied to the memory device include SET, RESET, and WEB. EX1004, [0055] (“[t]he decoder 453 is set or reset by a set signal SET or a reset signal RESET”), FIG. 5 (depicting SET, RESET, and WEB as inputs to the memory device).

111. Ryu also explains that the *non-volatile memory device* receives an initial address (IADD) and “generates an address signal YA,” and explains that a selector “outputs data corresponding to an address value of an address signal YA.” EX1004, [0042], [0044], *see also id.*, [0054], [0055] (“[t]he initial address IADD can be set by a designer through an external source”), [0057], [0058], [0077], [0079], [0087], [0088], FIGs. 5, 11. Thus, the *non-volatile memory device* also includes a *data port* for receiving data signals carrying *address data*. *Id.* It was well known by the Critical Date of the '028 Patent for memory devices to include data ports for

carrying address data, as confirmed by multiple references. EX1011, 4:60-5:4 (describing “address inputs” that receive address data); EX1013, 13:48-67 (describing a flash memory device including twenty “address pins” each carrying address data); EX1029, 7:66-8:21 (describing “input terminals” that receive address signals).

112. The *non-volatile memory device* receives *command data* (e.g., WEB) and *address data* (e.g., initial address IADD) during a read operation. EX1004, [0042]-[0046], [0053]-[0062], FIG. 5. The *non-volatile memory device* can use the *command data* and the *address data* to access data stored in the non-volatile memory array. EX1004, [0042]-[0046], [0053]-[0062], FIG. 5. Ryu explains that “[t]he data is output in response to the first and second edges of the read control signal REB for controlling the output of the data. EX1004, [0048], *see also id.*, [0044], [0045], [0049], [0051], [0057], [0061], [0067], FIG. 5. It is clear that in the memory system of Ryu, the *non-volatile memory device* selects data for output based on the *address data*. EX1004, [0042] (“[t]he selector 520 outputs data corresponding to an address value of an address signal YA”), [0043] (“[t]he output unit 530...outputs data DATA[7:0] received from the selector 520 through an input/output pin”), [0060] (“[t]he output driver 535 outputs the data DATA[7:0] from the input/output buffer 533 to the external source through the input/output pin”), FIG. 5.

113. Because the *non-volatile memory device* retrieves the *output data* from the non-volatile memory array based on *address data* and *command data*, it is apparent that the *output data* is retrievable from a *plurality of non-volatile memory blocks* based on this data. *Id.*; *supra*, Element [1a] (describing how Ryu’s disclosure of a non-volatile memory array renders obvious the claimed plurality of non-volatile memory blocks). For example, Because Ryu’s *non-volatile memory device* outputs data from the page buffer during a read operation, the page buffer storing “a portion of data in a non-volatile memory array,” a POSITA would have understood and it would have been obvious that the *output data* is retrievable from the non-volatile memory array and thus from the *plurality of non-volatile memory blocks* (*Supra*, [1a]). EX1004, [0042], [0046], [0077]. It is clear that the page buffer itself retrieves data from the non-volatile memory array. EX1004, [0042] (“page buffer 510 stores a portion of data stored in a non-volatile memory array”), [0046] (“page buffer 510...receives and stores data from a non-volatile memory array”), [0077].

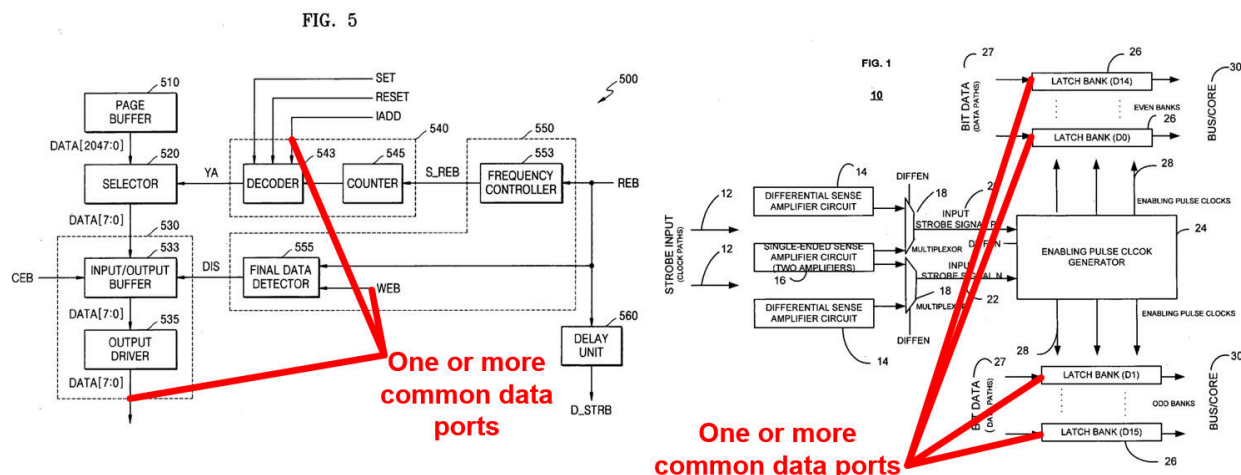
114. In addition to providing a *common data port* configured to transfer *common data signals* carrying *output data*, Ryu’s “input/output pin” also provides a *common data port* configured to transfer *common data signals* carrying *input data*. EX1004, [0004], [0009], [0037], [0045], [0060]-[0062], [0066]. This *input data* is to be written and thus stored to the non-volatile memory array of the *non-volatile memory device* according to a write operation. *Id.* A POSITA would have

understood that this *input data* would be programmed into one of the *plurality of non-volatile memory blocks* based on *command data* and *address data*, because it was well known by the Critical Date of the '028 Patent for memory devices to use address data and command data during write operations to store data in particular locations of the memory. *Id.*; EX1034, 5:43-6:6 (describing a memory device that uses addresses to write data to a memory); EX1029, 6:54-7:6 (disclosing write operations involving address data). For example, in Ryu's *non-volatile memory device*, the *command data* can include a write control signal indicating that the *input data* is to be written to memory and the *address data* can specify the location in memory where the input data is to be programmed and thus stored. *Id.*

115. A POSITA would have understood that the use of *command data* and *address data* to program data in memory was conventional and exceedingly common before the Critical Date of the '028 Patent, and multiple references support my opinion here. EX1028, 4:59-6:56 (describing "command/address lines" that control data operations in a memory device); EX1029, 1:24-35 (describing a memory device that latches command and address signals); EX1030, 4:50-5:5 (describing a flash memory that receives address signals and control signals). To ensure the memory device executes the correct operation (e.g., a write operation based on the command data) and allows a memory controller or other external device to specify which memory device or where in the memory blocks the data should be stored, a POSITA

would have found it obvious to program input data into a *plurality of non-volatile memory blocks* based on *command data* and *address data*. Because it was well known to use of command and address data in similar memory devices before the alleged invention of the '028 Patent, a POSITA would have reasonably expected success implementing these features in the non-volatile memory device of the Ryu-Cole-Arcoleo combination, and this is corroborated by multiple references. EX1028, 4:59-6:56; EX1029, 1:24-35; EX1030, 4:50-5:5).

116. In the Ryu-Cole-Arcoleo combination, the non-volatile memory device includes *one or more common data ports* configured to transfer *common data signals* carrying at least one of *command data*, *address data*, *input data* and *output data*, including Ryu's input/output pin (IOP), and optionally ports for receiving address and command data (e.g., IADD, SET, RESET, CEB, WEB signals) and/or ports for a data bus like that described in Cole. EX1005, [0016], [0023], FIGS. 1, 2A-2B (disclosing data paths 27 and corresponding data ports), [0043]-[0044], FIG. 8 (disclosing bus 808 and corresponding interface for receiving/transmitting data on bus 808).



EX1004, FIG. 5 and EX1005, FIG. 1 (annotated).

117. The term “DATA[7:0]” refers to an output that includes eight bits numbered “0” to “7.” EX1004, [0043], [0058]-[0062], [0064], [0065], [0067], [0078], [0079], [0089]-[0093], FIGs. 5, 11. Specifically, Ryu explains that “[t]he address signal YA is used as a control signal of the selector 520 for selecting *eight data* DATA[7:0] among the data output from the page buffer 510.” EX1004, [0058]. Because Ryu uses the term “DATA[7:0]” to refer to the output data that is output from an “input/output pin” of the non-volatile memory device, the “input/output pin” described by Ryu can include eight separate pins in some cases, to simultaneously output eight bits of data. This interpretation is consistent with my opinion that Ryu describes *one or more common data ports* configured to transfer *common data signals*.

Element [1f]: a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and

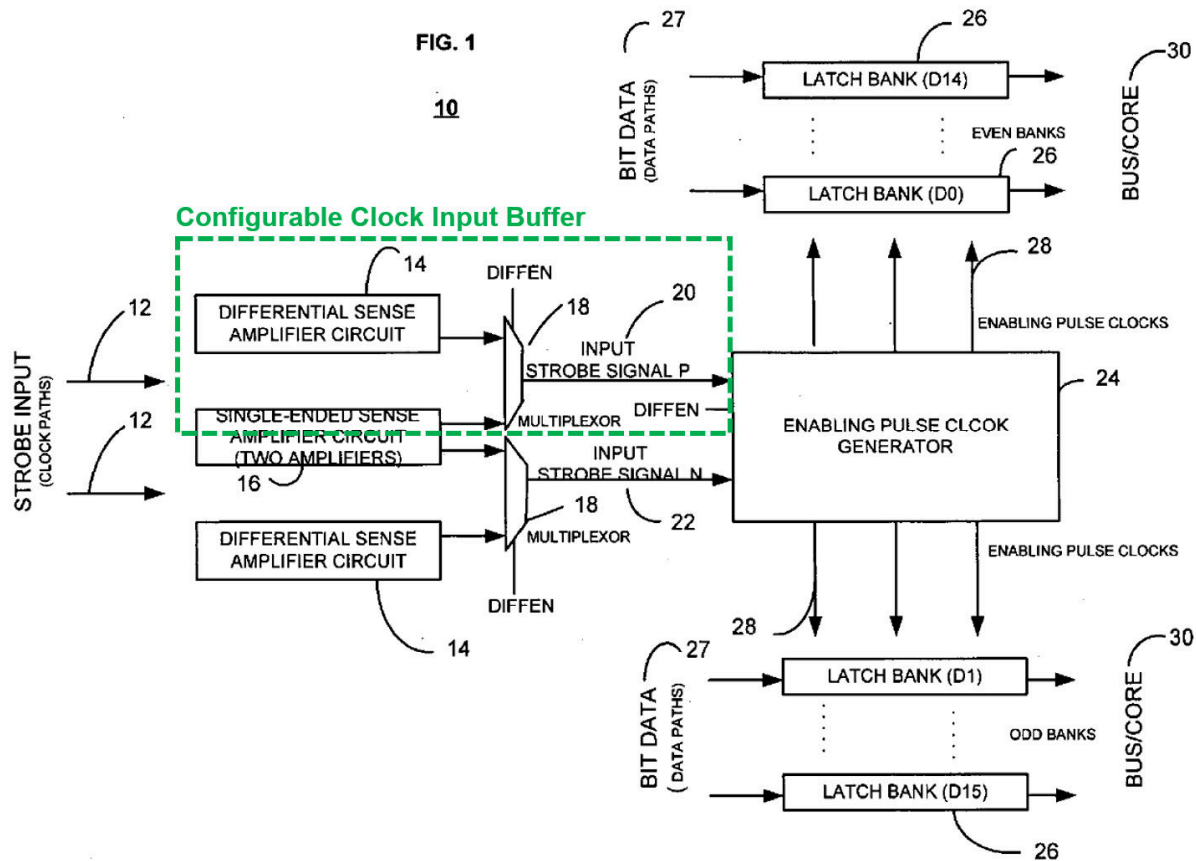
the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

118. It is apparent that the Ryu-Cole-Arcoleo combination renders obvious [1f]. As I described above in my analysis of Element [1c], *supra*, a POSITA would have been motivated to implement Ryu’s *non-volatile memory device* to include an input section that serves as a *configurable clock input buffer* as taught by Cole. *Supra*, §VII.B, §VII.D. For example, Cole’s input section includes a *clock input buffer* including a *first clock input port* that receives a positive strobe input “xxStrbP” representing a *first clock input signal* and a *second clock input port* that receives a negative strobe input “xxStrbN” representing a *second clock input signal*. EX1005, [0019], [0020], [0026], FIG. 1, FIG. 2A; *supra*, [1c]. For example, the *clock input buffer* includes a “differential sense amplifier” circuit 14 that includes amplifier 114 which receives both of the first and second clock input signals (xxStrbP and xxStrbN). EX1005, [0019], [0020], FIG. 1. The *clock input buffer* also includes a “single-ended sense amplifier circuit 16” that includes a first single-ended sense amplifier 118 receiving only first clock input signal (xxStrbP).⁶ EX1005,

⁶ Alternatively, the *clock input buffer* can include sense amplifiers 116 and 120 and the second multiplexor 18. In this case, single-ended sense amplifier 120

[0019], [0020], FIG. 1. Sense amplifier circuits 14 and 16 are coupled to a first multiplexor 18, which selectively passes the output of either sense amplifier 114 or 118 depending on the configuration mode. EX1005, [0021], *see also id.*, [0015], FIG. 1.

receives xxStbN (rather than xxStbP) as a single ended signal and the differential sense amplifier 120 receives both the first and the second clock input signals. EX1005, [0019], [0020], [0026], FIGs. 1, 2A. Another possibility is that the claimed *clock input buffer* can include both differential sense amplifier circuits 14 (including amplifiers 114 and 116), single-ended sense amplifier circuit 16 (including both amplifiers 118 and 120), and both multiplexors 18. The fact that xxStbP is received by amplifier 118 and xxStbN is received by amplifier 120 aligns with the preferred embodiments disclosed in the '028 Patent in which CKI and CKI# are also both utilized as single-ended signals by respective buffer circuits in the single-ended configuration. *Cf.* EX1001, 14:41-63, 17:32-51, FIGs. 5, 8A.



EX1005, FIG. 1 (annotated).

119. In the Ryu-Cole-Arcoleo combination, the *clock input buffer* of Cole’s configurable input section is *configurable* to operate in a “*single-ended signaling mode*” or a “*differential signaling mode*,” which means that the combination provides a configurable clock input buffer configurable to one of a *single ended signaling configuration* and a *differential signaling configuration*. EX1005, [0002] (“[s]ingle-ended signaling mode and differential signaling mode”), [0018] (“input section 10 may...be configurable to support either single-ended or differential signaling”), [0019], [0021]-[0023], [0028], FIGs. 1, 2A. A control signal (DIFFEN)

is used to select one of the *single ended signaling configuration* and the *differential signaling configuration*. EX1005, [0017], [0021], [0022], FIGs. 1, 2A. Cole also explains that the differential signaling mode is enabled when DIFFEN has a value “1” and the single ended signaling mode is enabled when DIFFEN has a value “0” and expressly discloses that multiplexors 18 use DIFFEN “to configurably select...the outputs of sense amplifier circuits 14 and 16...for the differential signaling mode and the single-ended signaling mode respectively.” EX1005, [0021], [0022], FIG. 1.

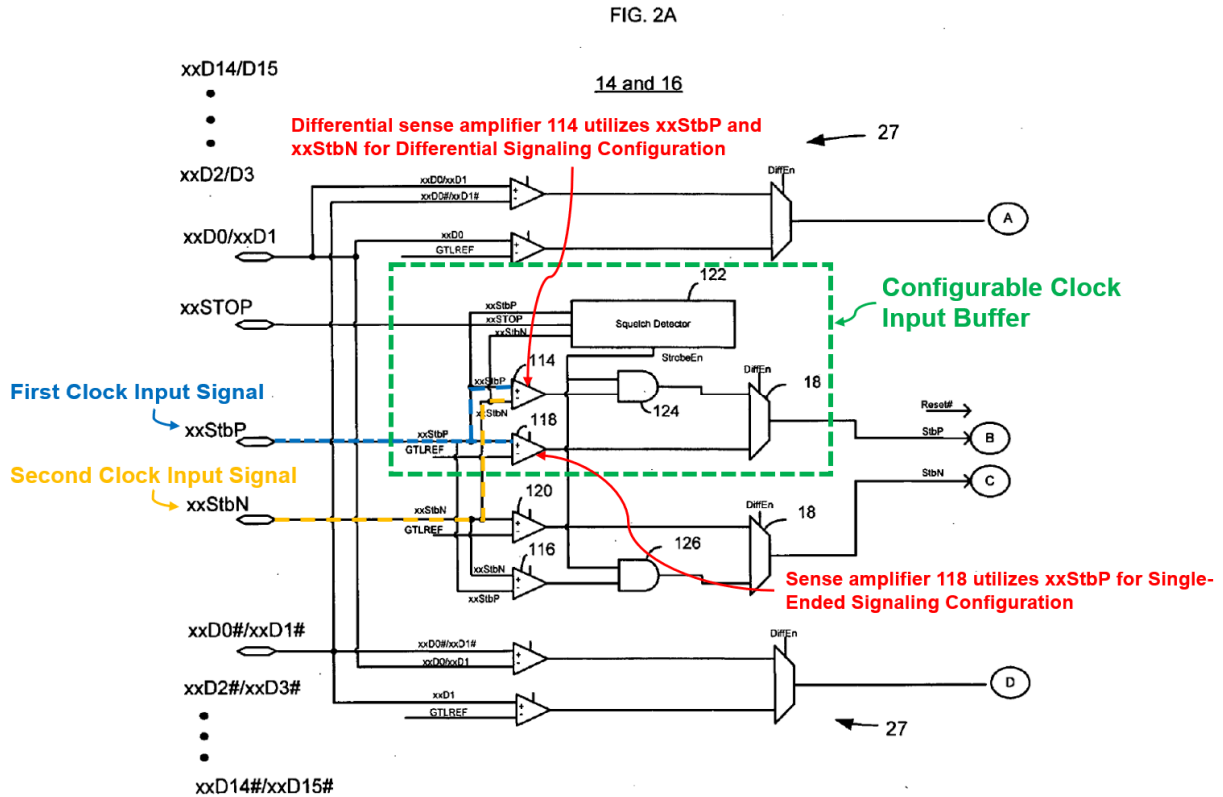
120. The differential sense amplifier circuit 14 utilizes both of the input signals 12 as *differential signals* in the *differential signaling configuration*. EX1005, [0015], [0019], [0021]-[0022], [0040]-[0041], FIGs. 1, 7. This is supported by the fact that Cole describes the first differential sense amplifier circuit 14 as including a “sense amplifier 114” that receives both of the *first clock input signal* represented by the positive strobe input “xxStrbP” and the *second clock input signal* represented by the negative strobe input “xxStrbN.”⁷ EX1005, [0023], [0026], [0028], FIG. 2A. It is apparent that sense amplifier 114 produces a first timing signal based on comparison of the input signals xxStrbP and xxStrbN. EX1005, [0026], [0028], FIG. 2A, FIG. 2C. One reason for this is because FIG. 2A clearly depicts

⁷ *Supra*, Footnote 2.

sense amplifier 114 as receiving xxStrbP in a positive input and xxStrbN in a negative input.

121. The single-ended sense amplifier circuits 16 each utilize one of the input signals 12 as a *single ended signal* in the *single ended signaling configuration*. EX1005, [0015], [0019], [0021]-[0022], [0040]-[0041], FIGs. 1, 7. This is supported by the fact that Cole explains that the single-ended sense amplifier circuit 16 includes a “sense amplifier 118” that receives the the *first clock input signal* “xxStrbP.”⁸ EX1005, [0023], [0026], [0028], FIG. 2A. Sense amplifier 118 produces a first timing signal based on xxStrbP as a single-ended signal. EX1005, [0026], [0028], FIG. 2A, FIG. 2C. One reason for this is because FIG. 2A clearly depicts sense amplifier 118 as receiving xxStrbP in a positive input.

⁸ *Supra*, Footnote 2.



EX1005, FIG. 2A (annotated).

122. The configurable clock input buffer circuitry of Cole and the configurable clock input buffer circuitry of the '028 Patent are strikingly similar. For example, I noticed that the clock input circuit 406 depicted in FIG. 8A of the '028 Patent “includes a comparator 700 for receiving complementary clock signals from clock input ports CKI and CKI#, a first buffer circuit 702 for receiving a clock signal from clock input port CKI and a second buffer circuit 704 receiving a complementary clock signal from clock input port CKI#.” EX1001, 17:32-51. Much like the circuitry of the '028 Patent, Cole’s circuitry includes a comparator (e.g., sense amplifier 114 or 116) that compares the complementary input clock signals as

differential signals and additional circuitry (e.g., sense amplifiers 118 or 120) that utilize one of the first clock input signal and the second clock input signal as a single ended signal. *Id.*

Configurable clock input buffer

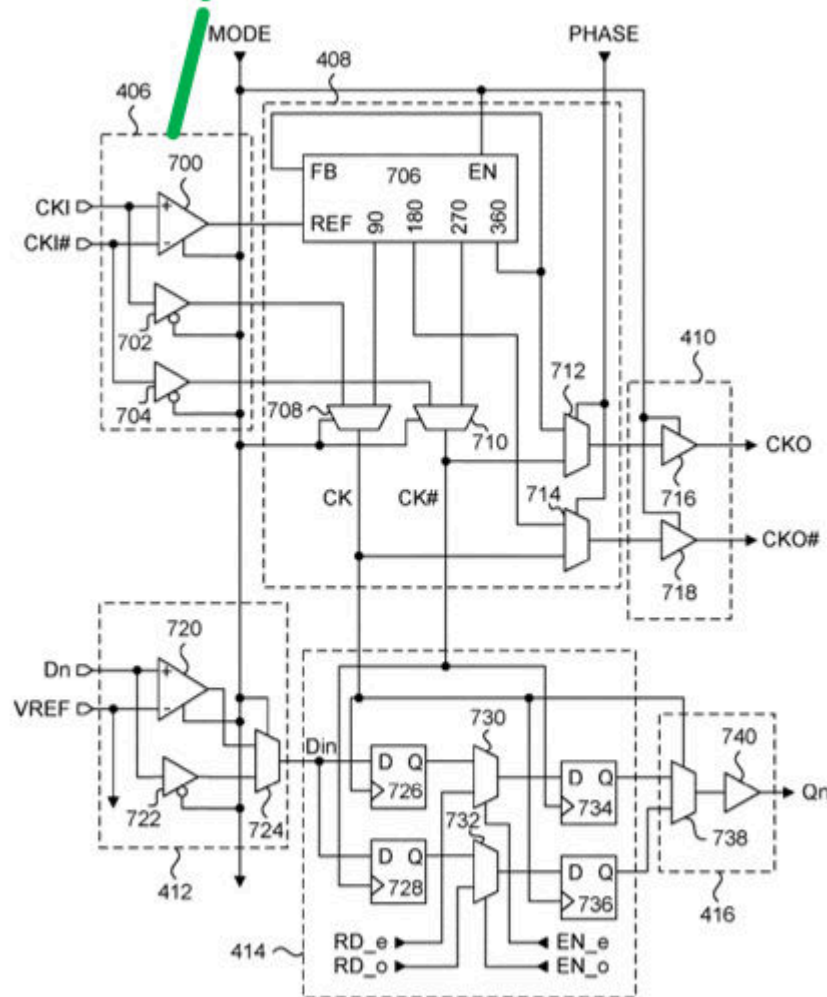


Fig. 8A

EX1001, FIG. 8B (annotated).

123. It is clear that the Ryu-Cole combination therefore provides a ***non-volatile memory device*** including a ***configurable clock input buffer*** configurable to

one of a *single ended signaling configuration* utilizing one clock signal as a *single ended signal* and a *differential signaling configuration* utilizing two clock signals as *differential signals*. *Supra*, §VII.D.

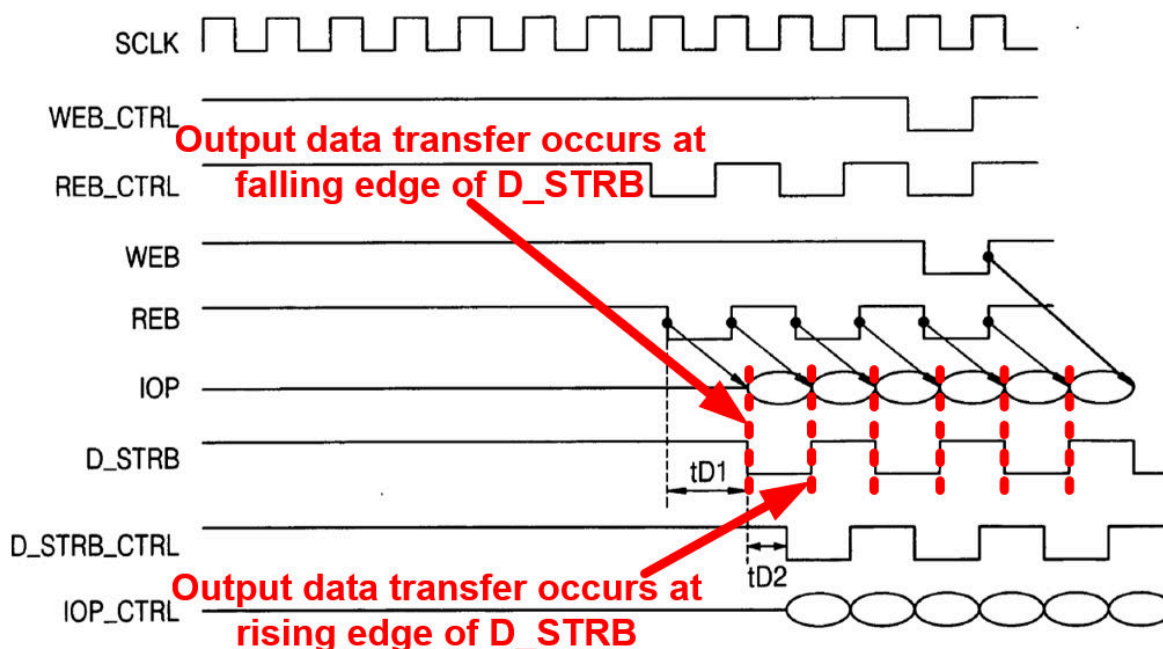
Element [1g]: one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

124. It is apparent that the Ryu-Cole-Arcoleo combination renders obvious [1g]. For example, the output unit of Ryu's *non-volatile memory device* includes an "input/output buffer" and an "output driver" that collectively provide an *output buffer* as claimed. EX1004, [0060] ("[t]he output unit 530 includes an input/output buffer 533 and an output driver 535...the output driver 535 outputs the data DATA[7:0] from the input/output buffer 533 to the external source through the input/output pin"), [0061], [0078], [0090], FIG. 5, FIG. 11, Cls. 9, 21; *supra*, Element [1e]. To control transfer of *output data* ("Data[7:0]") to be outputted via an input/output pin (IOP), Ryu's *output buffer* receives an enable signal CEB and a disable signal DIS. *Id.* I noticed that a selector retrieves *output data* from data in a page buffer. *Id.* This *output data* represents a portion of data stored in Ryu's non-volatile memory array representing a *plurality of non-volatile memory blocks*, and sends the *output data* to Ryu's output unit for transfer via the input-output pin. EX1004, [0042], [0043], [0046], [0060], [0061], [0076]-[0078], [0090], FIG. 5, FIG. 11.

corresponds to one output data unit at the input output pin (IOP), a POSITA would have recognized that Ryu's *output data* is both edge aligned and *synchronized* with the *clock output signal* ("D_STRB")⁹ in a *double data rate* configuration. EX1004, [0067] ("[t]he data DATA[7:0] is output through the input/output pin IOP in response to the rising and falling edges of the read control signal REB and simultaneously the...D_STRB is output"), *see also id.*, [0066], [0094], [0095], FIGs. 7, 12. An additional unit (comprising eight data bits) is output from the IOP at each rising edge and at each falling edge of the D_STRB signal, as depicted below in FIG. 7. *Id.*

⁹ *Supra*, Footnote 2, Element [1d].

FIG. 7



EX1004, FIG. 7 (annotated).

126. It would have been obvious and provided in the Ryu-Cole-Arcoleo combination for the *output buffer* to be *configurable* to one of a *plurality of output buffer drive strengths*, even if Ryu does not expressly disclose this feature. EX1006, 1:12-25, 1:37-2:11, 3:43-4:28, 6:10-65, 7:24-8:46, FIG. 4; *supra*, §VII.D. For example, Arcoleo discloses a “memory device.” EX1006, 3:43-65 (“[a]ccording to the invention, an output buffer circuit of a semiconductor memory device can produce multiple output buffer drive strengths”), 3:66-4:28, 6:10-36, FIG. 4. The memory device includes a “memory cell” and an “output buffer circuit.” *Id.* at 6:10-36 (“[a] memory cell 401 provides a signal representing data stored in the memory

cell 401 as an input signal (e.g., a voltage having a particular magnitude) to the output buffer 402”). Arcoleo discloses that the output buffer circuit includes an “output buffer 402” and an “output buffer drive strength selector (*sic*) 405” that “enables control of the operation of the output buffer 402 so that the output buffer 402 has a selected one of a set of possible output buffer drive strengths.” EX1006, 6:10-65, *see also id.*, 8:1-10:5, FIG. 4.

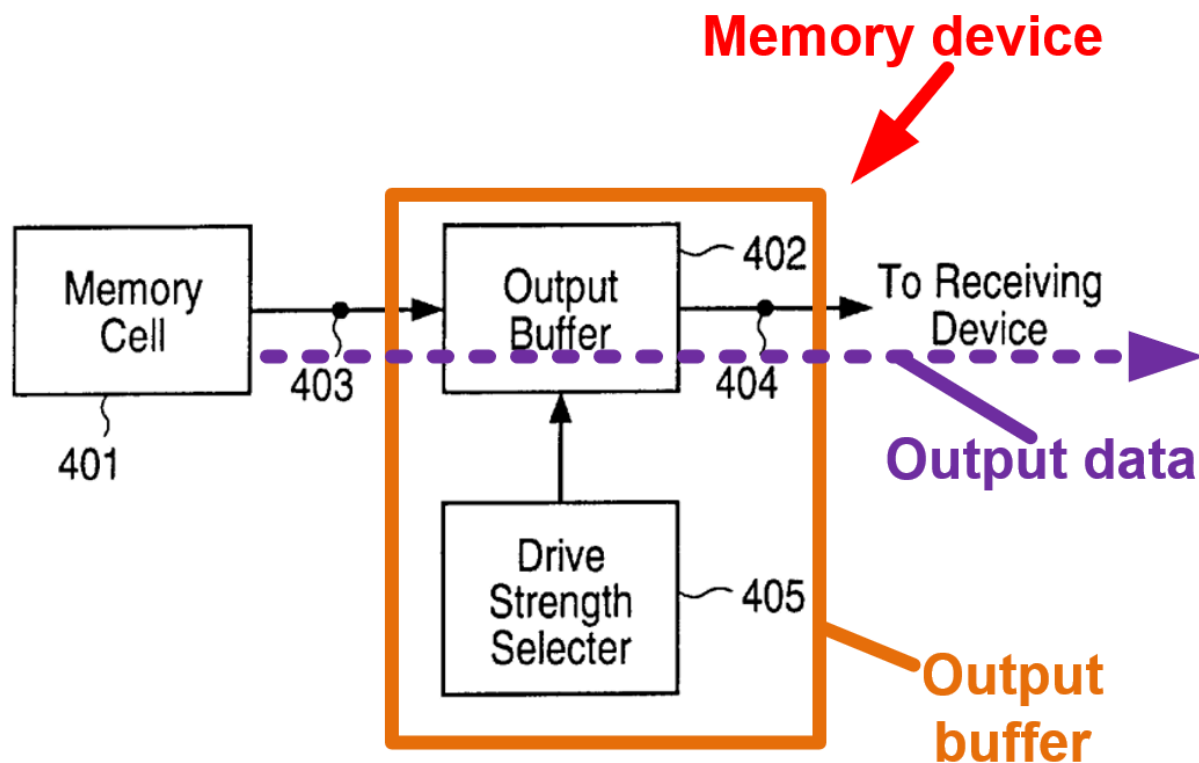


FIG. 4

EX1006, FIG. 4 (annotated).

127. Arcoleo describes a *configurable output buffer* that is configurable to one of a plurality of output buffer drive strengths because the “drive strength selector (*sic*) 405” controls “output buffer 402” to operate at one of a set of possible output

buffer drive strengths. EX1006, 6:10-65, FIG. 4; *cf.* EX1001, 19:64-67 (limited disclosure of a configurable buffer drive strength in the '028 Patent). It would have been obvious to apply these teachings from Arcoleo to the non-volatile memory device in the Ryu-Cole-Arcoleo combination for the reasons described above (*supra*, §§VII.C-D). The *non-volatile memory device* of the resulting Ryu-Cole-Arcoleo combination therefore includes a *configurable output buffer* that is configurable to one of a *plurality of output buffer drive strengths* to transfer *output data* synchronized with the *clock output signal* in a *double data rate configuration*.

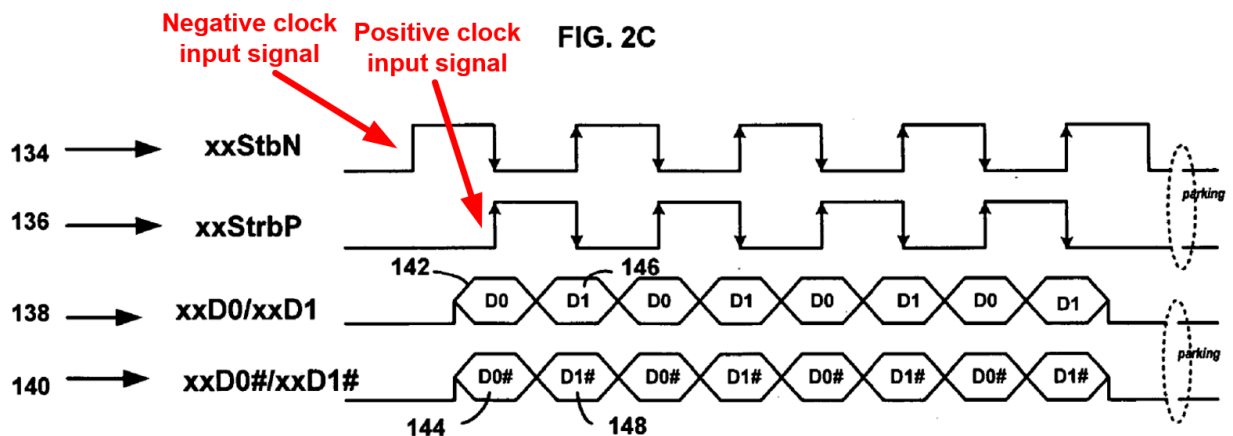
Claim [2]: The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively.

128. As I described in my analysis of Element [1c], *supra*, Cole describes an IC input section having a *configurable clock input buffer* that receives two strobe inputs 12 representing a *first clock input signal* represented by a strobe input “xxStbP” and a *second clock input signal* represented by a strobe input “xxStbN.”

¹⁰ EX1005, [0019], [0020], [0026], FIGs. 1, 2A, 2C. Because Cole generally refers to *positive* signals using the letter “P” and *negative* signals using the letter “N,” including the positive and negative strobe inputs xxStbP and xxStbN received by the *configurable clock input buffer* and the positive and negative strobe signals P and

¹⁰ *Supra*, Footnote 2.

N generated by the *configurable clock input buffer*, it is clear that the first and second clock input signals represent positive and negative clock input signals. EX1005, [0017], [0019], [0026], [0027], FIGs. 2A, 2C. For example, it is clear that the *first clock input signal* “xxStbP” represents a *positive clock input signal* and the *second clock input signal* “xxStbN” represents a *negative clock input signal*. *Id.* My opinion here is confirmed by the fact that FIG. 2C of Cole depicts xxStbP and xxStbN as complementary signals of opposite polarity. *Id.* In FIG. 2C, where xxStbP is at a high value when xxStbN is at a low value and xxStbP is at a low value when xxStbN is at a high value. *Id.*



EX1005, FIG. 2C (annotated).

Claim [3]: *The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal and the second clock input signal are data latching clock signals.*

129. As I described in my analysis of Element [1c], *supra*, the *non-volatile memory device* of Ryu that is governed by a system clock (SCLK). EX1004, [0003],

[0041]-[0045], [0064], [0065], [0076]-[0079], FIGs. 4A-4B, 7, 12. I also explained in my analysis of Element [1c] that the Ryu-Cole combination provides a ***first clock input port*** configured to receive a ***first clock input signal*** and a ***second clock input port*** configured to receive a ***second clock input signal***. EX1005, [0019], [0020], [0026], FIGs. 1, 2A. The ***non-volatile memory device*** of Ryu performs one or more read or write operations using an output unit by receiving and/or transmitting ***data*** via an input/output pin. EX1004, [0003]-[0008], [0038], [0041]-[0043], [0059]-[0063], FIGs. 5, 11. The teachings of Cole demonstrate that it was known and would have been obvious before the Critical Date of the '028 Patent for the ***first clock input signal*** and a ***second clock input signal*** to represent ***data latching clock signals***, even if Ryu does not expressly disclose these features. EX1005, [0015]-[0028], FIGs. 1, 2A, 2C.

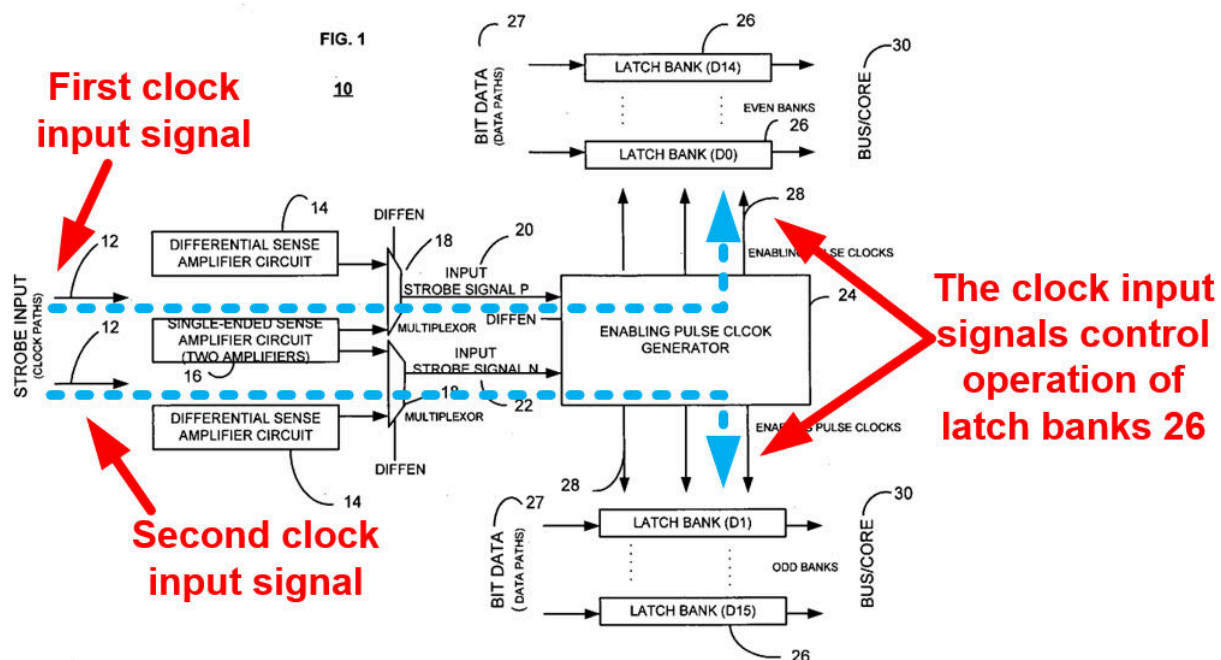
130. The input section 10 of Cole includes “latch banks 26” and Cole explains that the latch banks 26 “may be employed to latch and temporarily store the data being transferred to the IC.” EX1005, [0016]-[0020], [0023], [0024], [0026], [0029], FIGs. 1, 2B, 3. Cole discloses an IC input section having a ***configurable clock input buffer*** that receives two strobe inputs 12 including a positive strobe signal “xxStbP” representing a ***first clock input signal*** and a negative strobe signal “xxStbN” representing a ***second clock input signal***. *Id.* To ensure that data can be

properly latched in latch banks 26,¹¹ strobe inputs indicate the timing of bit data defined in the signals received through data paths 27. *Id.* Cole expressly discloses that input section 10 includes “sense amplifier circuits 14 and 16” that “provide strobe signals P and N 20 and 22 to enabling pulse clock generator 24 for the differential signaling mode and the single-ended signaling mode respectively...in accordance with at least strobe inputs 12.” EX1005, [0019]; *see also id.*, [0015]-[0018], [0023], FIGs. 1, 2B.

131. Cole explains that the pulse clock generator 24 “may be employed to provide latch banks 26 with enabling pulse clocks 28 to control their operations...in accordance with at least strobe signals P and N 20 and 22,” which means that the strobe signals P and N generated based on strobe inputs 12 are used for latching operations EX1005, [0017], FIG. 1. I noticed that strobe signal P 20 is also referred to by Cole as “StbP” and strobe signal N 22 is also referred to by Cole as “StbN.” EX1005, [0026], [0027], [0036], [0037], [0038], [0039], FIGs. 1-2B, 3. Because Cole explains that strobe signals including the positive strobe signal “xxStbP” representing the *first clock input signal* and the negative strobe signal “xxStbN” and the *second clock input signal* can be used to perform *data latching* of the latch banks 26, these clock input signals represent *data latching clock signals*. EX1005, [0029]

¹¹ *Supra*, Footnote 2.

(“enabling pulse clock generator 24 is employed to provide enabling pulse clocks to latch banks 26 to control their data latching operations”), *see also id.*, [0015]-[0018], [0023]-[0025], [0031], FIGs. 1-2B, 3.



EX1005, FIG. 1 (annotated).

132. When the *non-volatile memory device* of Ryu is implemented with a *configurable clock input buffer* as suggested by Cole, the resulting device therefore receives a *first clock input signal* and a *second clock input signal* that serve as *data latching clock signals*. *Supra*, §VII.D.

Claim [4]: *The configurable non-volatile memory device as claimed in claim 1, wherein each of the one or more common data ports comprises 1 bit.*

133. It is apparent that The Ryu-Cole-Arcoleo combination renders obvious [4]. For example, Ryu discloses that “output unit 530 is activated in response to an

enable signal CEB” and “outputs DATA[7:0] received from the selector 520 through an input/output pin,” an input/output pin used for each of the *one or more common data ports*. EX1004, [0043], FIGS. 4A, 5, 7, 10B, 11. A POSITA would have understood that the “DATA[7:0]” output from the input/output pin comprises eight individual bits of data numbered “0” through “7.” *Id.* Ryu’s input/output pin therefore comprises at least eight *common data ports* each comprising *1 bit*, so that the input/output pin can simultaneously output eight bits of data. *Id.* According to Grundy, “signals transmitted on the N signal lines that form the bus may alternatively be time-multiplexed onto a smaller number of signal lines” and a serializer circuit can be provided “to serialize an N-bit transmission onto a single differential signal line.” EX1009, [0051].

134. A POSITA would have understood that each individual *common data port* of Ryu’s input/output pin comprises *1 bit* because Ryu’s timing diagrams show that just one data transfer event occurs at the IOP at a time. *Id.* This confirms my opinion that the input/output pin comprises eight individual *common data ports* each comprising *1 bit*, because eight *1 bit common data ports* would be required to simultaneously transfer an eight bit segment “DATA[7:0].” EX1004, FIGs. 7, 12. Furthermore, it is clear that a POSITA also would have recognized that each of the other *common data ports* for receiving input data, command data, and address data (e.g., including IADD, SET, RESET, REB, CEB) would likewise comprise *1 bit*

because Ryu's timing diagrams consistently depict signaling in which 1 bit of data is transmitted per line at a time. *See e.g.*, EX1004, FIGS. 4A, 7, 10B, 12.

135. Cole also describes common data input ports 27 that each comprise 1 bit, confirming that a POSITA would have implemented the ***non-volatile memory device*** of Ryu with ***1 bit*** data ports. EX1005, [0016] ("latch bit data off input data paths 27"), [0023] ("capturing bit data received via data paths 27"), FIGs. 1, 2A-2C, 4. This supports my opinion that it would have been obvious in the Ryu-Cole combination for the ***common data ports*** of the memory device to each comprise ***1 bit***.

Claim [10]: The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration.

136. It is apparent that the Ryu-Cole-Arcoleo combination renders obvious [10]. As an initial matter, I noticed that the delay unit of Ryu's ***non-volatile memory device*** generates the strobe signal D_STRB "by delaying the read control signal REB by a predetermined delay time tD1," and "delay time t1 is adjusted in a digital format *using internal registers* in accordance with various embodiments." EX1004, [0067], [0068]. Consequently, Ryu explains that the ***non-volatile memory device*** includes one or more ***registers*** that define parameters according to which the device operates. *Id.* To the extent that Ryu does not expressly disclose that the ***non-volatile memory***

device includes a configuration register configured to store configuration information indicating whether the *configurable clock input buffer* is configured as the *single ended signaling configuration* or the *differential signaling configuration*, Cole provides this feature.

137. When the *non-volatile memory device* of Ryu is modified to include an IC input section as described in Cole, the *non-volatile memory device* includes a *configuration register*. EX1005, [0015]-[0028], FIGs. 1, 2A-2C. I noticed that the input section of Cole includes a “configuration register” that stores “one or more control bits.” EX1005, [0022] (“Configuration of input section 10 may be effectuated in any one of a number of manners, including but [] not limited to the setting of one or more control bits in a configuration register...”); see also EX1005, [0002], [0013], [0015]-[0028], FIGs. 1, 2A-2C; *supra*, Elements [1c] and [1e]. Cole explains that the one or more control bits can “cause the control signal Diffen to assume a value of ‘1’ to configure input section 10 to operate in a differential signaling mode, and a value of ‘0’ to configure input section 10 to operate in a single-ended signaling mode.” *Id.* The *non-volatile memory device* of the Ryu-Cole combination therefore includes a *configuration register* that indicates whether the *configurable clock input buffer* is configured as the *single ended signaling configuration* or the *differential signaling configuration*. *Supra*, §VII.D.

Claim [11]: The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store the plurality

of output buffer drive strengths to be utilized by the one or more configurable output buffers.

138. As I described in my analysis of Element [1g], *supra*, it is apparent that the Ryu-Cole-Arcoleo combination provides a ***non-volatile memory device*** including an ***output buffer*** configurable to one of a plurality of ***output buffer drive strengths*** to transfer output data. EX1006, 1:12-25, 1:37-2:11, 3:43-4:28, 6:10-65, 7:24-8:46, FIG. 4; *supra*, §VII.D. Arcoleo explains that a memory device includes an “output buffer circuit.” EX1006, 6:10-36, *see also id.*, 6:37-8:46, FIGs. 4, 5A-5B; *supra*, Element [1g]. This output buffer circuit includes an “output buffer 402” and a “drive strength selector (*sic*) 405” that can select “one of a set of possible output buffer drive strengths.” *Id.* Thus, it is clear that the Ryu-Cole-Arcoleo combination provides ***one or more configurable output buffers*** that utilize a plurality of ***output buffer drive strengths***. *Id.*

139. Arcoleo expressly discloses that “[e]ach possible drive strength can be associated with a particular series of signals so that...a ***register*** or registers can be set, for example, in the memory device to identify a specified drive strength.” EX1006, 11:3-17. This means that Arcoleo explains that the ***configurable output buffer*** comprises a ***configuration register*** that stores a ***plurality of output buffer drive strengths***. *Id.* Consequently, in the Ryu-Cole-Arcoleo combination, the resulting ***non-volatile memory device*** includes a ***configuration register*** that stores a

plurality of output buffer drive strengths to be utilized by the *output buffer*. *Supra*, §VII.D.

Claim [12]: The configurable non-volatile memory device as claimed in claim 1, wherein the output data is edge aligned with the clock output signal.

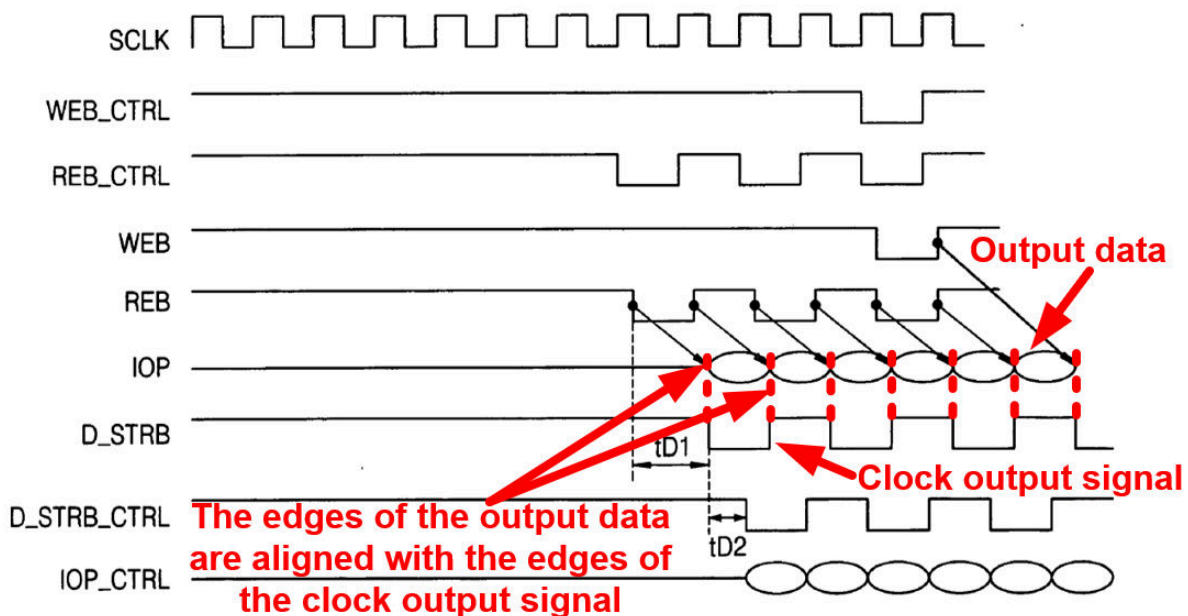
140. The Ryu-Cole-Arcoleo combination would have rendered Element [12] obvious for the reasons I discussed above with respect to Element [1g]. *Supra*, Element [1g].

141. Ryu describes a *non-volatile memory device* including a *clock output port* that drives a *clock output signal*. EX1004, [0041]-[0046], [0058]-[0065], [0076]-[0078], FIG. 5, FIG. 11; *supra*, [1e], [1g]. The *non-volatile memory device* also includes *one or more common data ports* configured to transfer *output data* that is synchronized with the *clock output signal* in a *double data rate configuration*. *Id.* Ryu discloses that the *non-volatile memory device* includes a *clock output signal* represented by the data strobe signal D_STRB that is *edge aligned* with *output data* transferred from an input/output pin (IOP). EX1004, [0064]-[0070], [0091]-[0095], FIGs. 5, 7, 11, 12.

142. For example, every rising edge or falling edge of the D_STRB signal signifies a beginning of a data transfer event at an input/output pin IOP that continues until a subsequent rising or falling edge of D_STRB. *Id.* Furthermore, the fact that the *output data* and the *clock output signal* are *edge aligned* is further confirmed by Ryu expressly disclosing that “a...signal D_STRB” is generated “by delaying the

read control signal REB by a predetermined delay time and output at the same time with the data DATA[7:0] to the external source.” EX1005, [0064], *see also id.*, [0067] (“[t]he data DATA[7:0] is output through the input/output pin IOP... simultaneously the...signal D_STRB is output”), [0094] (“the...D_STRB is output at the same time when data is output through the input/output pin in response to the rising and falling edges of the flash clock signal F_CLK”), FIGs. 7, 12.

FIG. 7

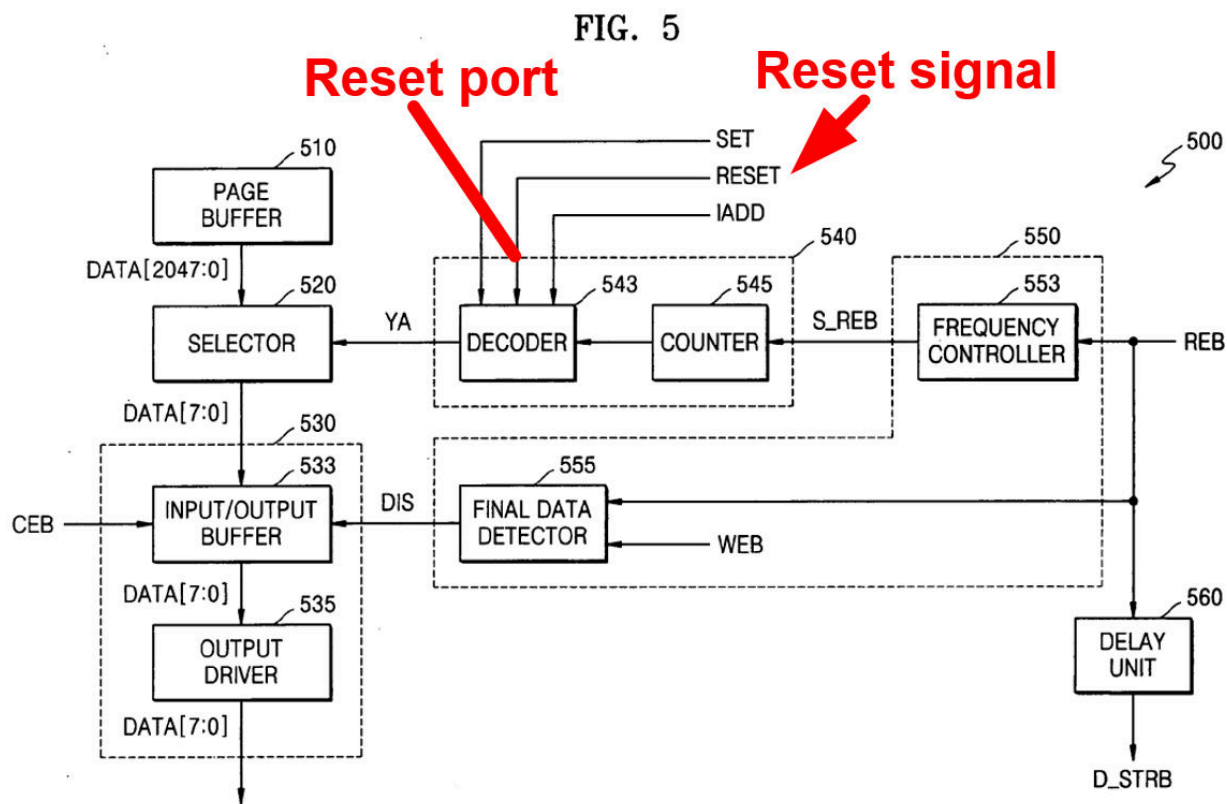


EX1005, FIG. 7 (annotated).

Claim [13]: *The configurable non-volatile memory device as claimed in claim 1, further comprising a reset port configured to receive a reset signal for resetting the configurable non-volatile memory device to a default configuration.*

143. It is clear that Ryu’s *non-volatile memory device* includes a *reset port* configured to receive a *reset signal* (RESET). EX1004, [0055], FIGs. 5, 11. For

example, the *non-volatile memory device* includes a decoder 543 that receives a *reset signal* (RESET) and also receives a “set signal” (SET). *Id.* Ryu expressly discloses that “[t]he decoder...is set or reset by a set signal SET or a reset signal RESET.” *Id.* Because the “decoder” of Ryu is part of the *non-volatile memory device*, the *non-volatile memory device* receives a *reset signal*. EX1004, [0054], [0055], [0057], FIGs. 5, 11. This means that the *reset signal* is for resetting the *non-volatile memory device* to a *default configuration*. *Supra*, §VII.D.



EX1005, FIG. 5 (annotated).

144. As I described above in my analysis of Claim [12], *supra*, Cole explains that “[c]onfiguration of input section 10 may be effectuated in any one of a number

of manners, including but [] not limited to the setting of one or more control bits in a configuration register ... of the IC, or fusing of one or more fuses ... of the IC.” EX1006, [0022]. Cole also explains that “the configuration register or the fuses may be configured to cause the control signal Diffen to assume a value of ‘1’ to configure input section 10 to operate in a differential signaling mode, and a value of ‘0’ to configure input section 10 to operate in a single-ended signaling mode,” which means that the configuration register is used to control whether the *non-volatile memory device* is operating in a *single ended signaling configuration* or a *differential signaling configuration*. *Id.* Either one of these configurations can serve as part of a *default configuration* of the *non-volatile memory device*. *Id.*

145. Moreover, it is clear that a POSITA would have understood that configuration registers or fuses in an IC are commonly set based on signals received via a corresponding *port* and it would have been obvious for the Ryu-Cole-Arcoleo *non-volatile memory device* to receive Diffen or another signal for setting registers/fuses that define a value of the Diffen signal via a port to allow Diffen to be set by an external source such as a user, memory controller, or other device sending data to the non-volatile memory device. *Id.* As an example, if the device is initially set to the single-ended signaling configuration (Diffen=0) but has been subsequently changed to the differential signaling configuration (Diffen=1), a POSITA would have understood a received signal that causes Diffen to revert to 0

for the single-ended signaling configuration to be a “reset signal” that resets the non-volatile memory device to a default single-ended signaling configuration. *Supra*, §VII.D.

Claim [14]: The configurable non-volatile memory device as claimed in claim 13, wherein the default configuration comprises the single ended signaling configuration.

146. The Ryu-Cole-Arcoleo combination discloses and renders obvious Claim [14] for at least the same reasons that I addressed above in connection with Claim [13]. *Supra*, Claim [13].

Claim [15]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a flash memory device.

147. Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of...***flash memory***,” which means that the ***non-volatile memory device*** is a ***flash memory device*** in these embodiments. EX1006, [0036]. Furthermore, it was well known by the Critical Date of the ’028 Patent that ***flash memory*** is a common kind of ***non-volatile memory***, and multiple references corroborate this fact. EX1012, 2 (describing “non-volatile, flash memory”); EX1017, 17:4-17 (claiming a “non-volatile memory device comprising: an array of multi-state non-volatile storage units... wherein [s]aid storage units comprise flash memory cells”); EX1018, 1 (explaining that “semiconductor non-volatile memory devices such as flash memory have been announced to replace the magnetic disk”). Therefore, it is clear that Ryu explains that that the ***non-volatile***

memory device can be a *non-volatile flash memory device* in some embodiments.

Supra, §VII.D.

Claim [16]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NOR flash memory device.

148. As I described above in my analysis of Claim [15], *supra*, Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of a...*flash memory*.” EX1004, [0036]. Ryu also discloses that “the present invention can be embodied in various *nonvolatile memory devices* including, but not limited to, a *NOR device*.” *Id.* A POSITA therefore would have understood that Ryu discloses implementations of the configurable *non-volatile memory device* as a *NOR flash memory device*. *Id.*; *supra*, §VII.D. To the extent that Ryu does not disclose the “NOR device” as being a flash memory device, a POSITA would have understood that Ryu is referring to a *NOR flash memory device* at least because Ryu also describes the *non-volatile memory device* as including a *flash memory* in some cases. *Id.*

149. A POSITA also would have found it obvious to use *NOR flash memory* in many cases, because NOR flash memory has comparatively faster read speeds, higher endurance (e.g., capacity for higher number of write/erase cycles), and lower susceptibility to errors as compared with other configurations such as NAND flash memory. EX1031, 1 (describing NOR flash memory as having “faster read and

programming”). It was well known by the Critical Date of the ’028 Patent for a ***non-volatile memory device*** to include a ***NOR flash memory device***, and my opinion here is corroborated by multiple references. EX1021, 3:20-31 (describing a non-volatile memory device including “an integrated circuit that embodies...a flash NOR array”); EX1022, 5:18-30 (explaining that “nonvolatile memory is formed of a plurality of nonvolatile memory arrays” including “NOR configured flash memory”); *supra*, §VII.D.

Claim [17]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NAND flash memory device.

150. I noticed that Ryu expressly discloses that “[e]xemplary embodiments of the present invention are described herein in the context of a ***NAND flash memory***” and Ryu also expressly discloses that “the present invention can be embodied in various ***nonvolatile memory devices***.” EX1004, [0036]. It was also well known by the Critical Date of the ’028 Patent for a ***non-volatile memory device*** to include a ***NAND flash memory device***, and my opinion here is corroborated by multiple references. EX1021, 3:20-31 (describing a non-volatile memory device including “an integrated circuit that embodies...a flash NAND array”); EX1022, 5:18-30 (explaining that “nonvolatile memory is formed of a plurality of nonvolatile memory arrays” including “NAND configured flash memory”). Consequently, the ***non-***

volatile memory device of the Ryu-Cole-Arcoleo combination includes a *NAND flash memory device* in some embodiments.

B. GROUND 1B: The Ryu-Cole-Arcoleo-Grundy Combination Renders Claims 1-4 and 10-17 Obvious

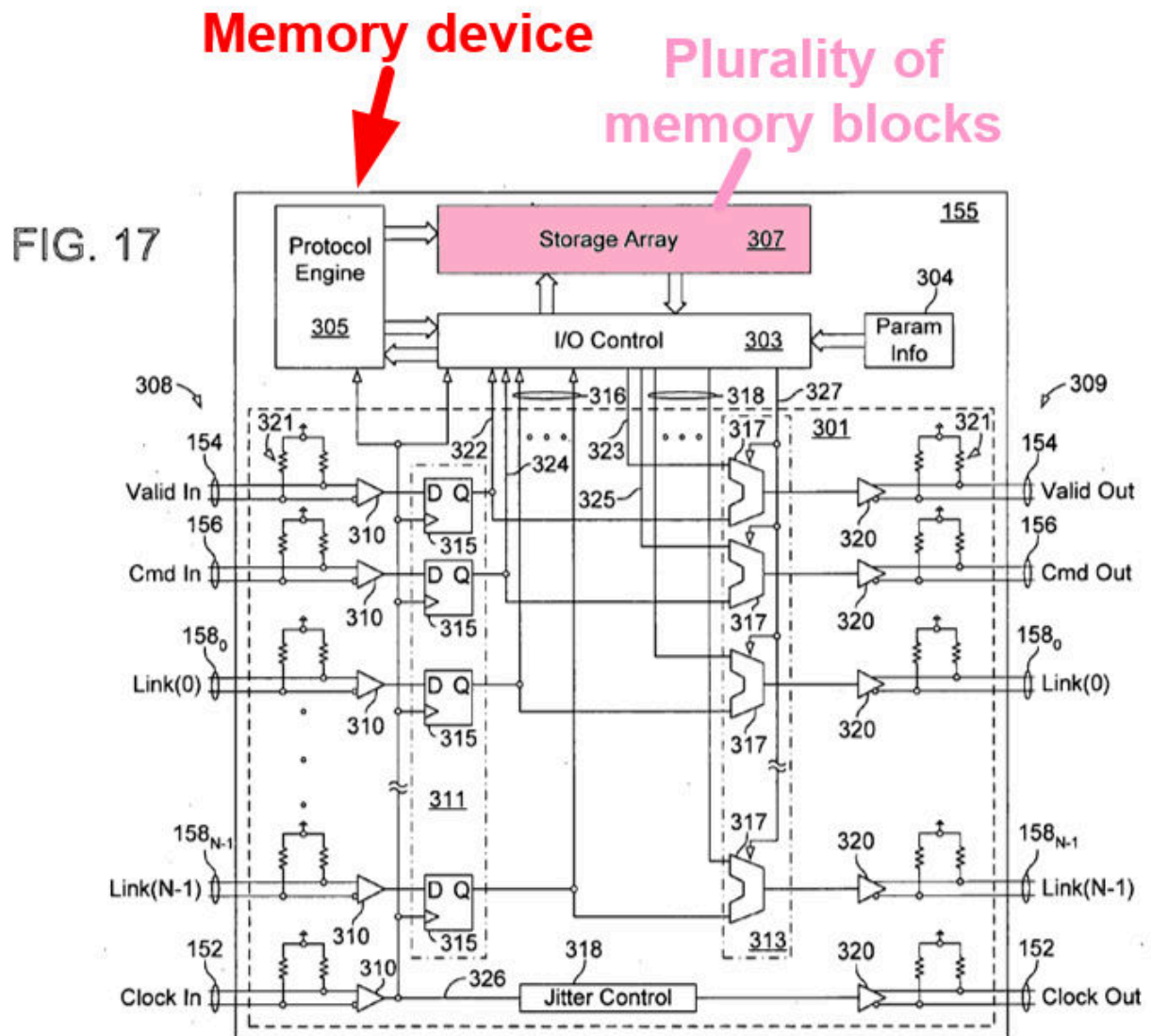
Element [1pre]: A configurable non-volatile memory device comprising:

151. The Ryu-Cole-Arcoleo-Grundy combination discloses and renders obvious Element [1pre] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Element [1pre]. *Supra*, Ground 1A (§VIII.A) at Element [1pre].

Element [1a]: plurality of non-volatile memory blocks;

152. As I described above in my analysis of Ground 1A, Element [1a] (*Supra*, §VIII.A), Ryu explains that the non-volatile memory device includes a “page buffer” that “stores a portion of data stored in a non-volatile memory array” and a “selector” that “outputs data corresponding to an address value...among data...stored in the page buffer.” EX1004, [0042], [0046], [0077], Cls. 5, 17. Grundy makes it even more clear that Element [1a] would have been obvious to a POSITA. Grundy describes a “*memory device*” that includes an “actual storage array,” which clearly represents a *plurality of non-volatile memory blocks*. EX1009, [0084], *see also id.*, [0033], [0035], [0062], [0073], [0079], [0081], [0082], [0090]-[0094], FIGs. 3, 17. According to Grundy, the storage array can “include multiple sub-arrays,” which further reinforces that the storage array comprises a plurality of memory blocks. *Id.*

Referring to storage arrays, Grundy explains that “block size” and a “number of memory banks” is one aspect of the storage array in the *memory device*. EX1009, [0062].



EX1007, FIG. 1 (annotated).

153. A POSITA would have understood Ryu’s non-volatile memory array to include a *plurality of non-volatile memory blocks*, as I described above in my

analysis of Ground 1A (§VIII.A), Element [1a], *supra*. The resulting ***non-volatile memory device*** therefore includes a ***plurality of non-volatile memory blocks*** when the ***non-volatile memory device*** of Ryu is implemented with a storage array (e.g., storage array 307) as suggested by Grundy. EX1009, [0084], *see also id.*, [0033], [0035], [0062], [0073], [0079], [0081], [0082], [0090]-[0094], FIGs. 3, 17.

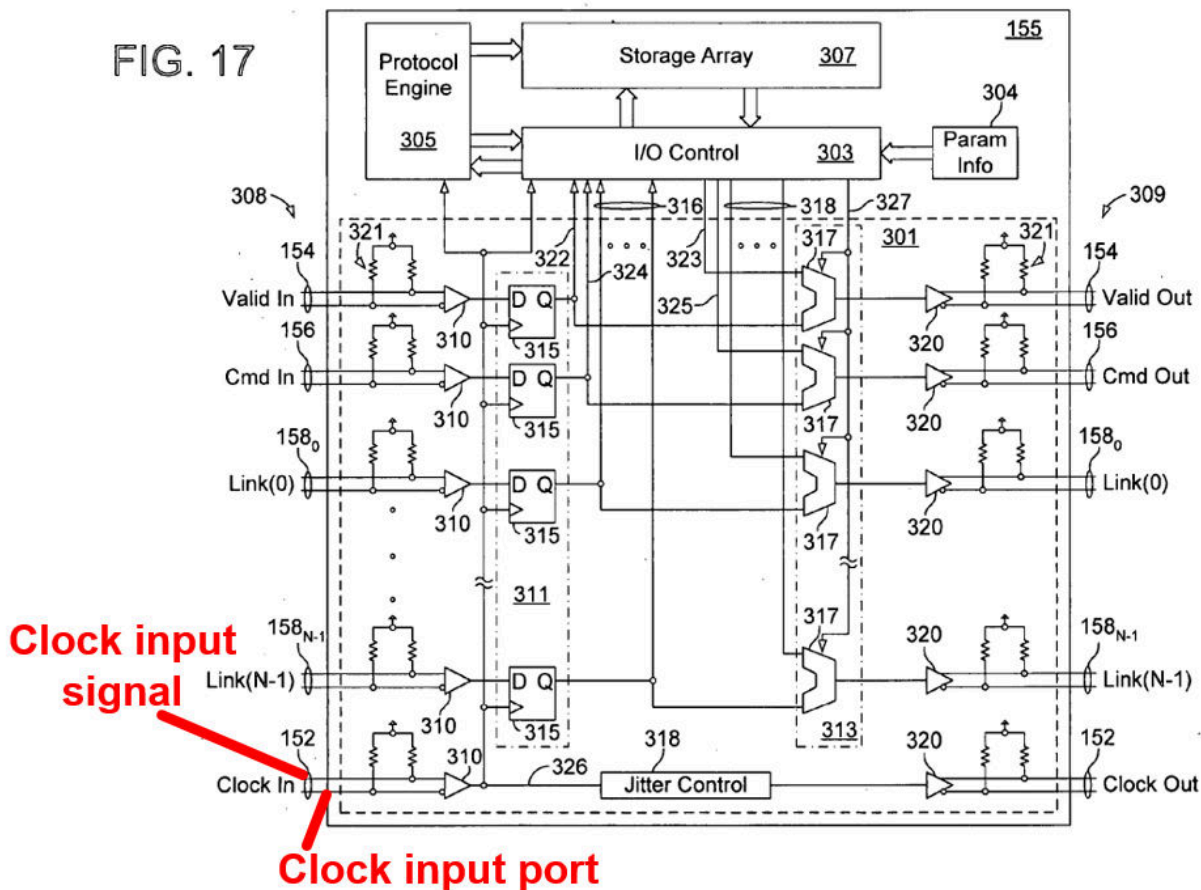
Element [1b]: a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;

154. The Ryu-Cole-Arcoleo-Grundy combination discloses and renders obvious Element [1b] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Element [1b]. *Supra*, Ground 1A (§VIII.A) at Element [1b].

Element [1c]: a first clock input port configured to receive a first clock input signal; a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;

155. As I described above in my analysis of Ground 1A (§VIII.A), Element [1c], *supra*, Ryu describes a ***non-volatile memory device*** and Cole describes an input section of an integrated circuit including a ***first clock input port*** that receives a ***first clock input signal*** represented by a positive strobe input “xxStrbP” and receives a ***second clock input port*** that receives a ***second clock input signal*** represented by a negative strobe input “xxStrbN.” EX1004, [0041]-[0065], [0076]-[0095], FIGs. 5, 11; EX1005, [0019], [0020], [0026], FIGs. 1, 2A. The obviousness of Element [1c]

would have been even more apparent in light of Grundy's disclosure of memory devices that receive clock signals through clock input ports. Grundy explains that a *non-volatile memory device* is "coupled to [an] input-side clock line" that supplies a "logic level clock signal." EX1009, [0088], *see also id.*, [0043], [0047], [0054], FIG. 17. This means that Grundy's *non-volatile memory device* includes a *clock input port* that receives a *clock input signal*, because the memory device clearly includes a clock input port for receiving the clock signal. *Id.*



EX1009, FIG. 17 (annotated).

156. To capture data on lines 154, 156, and 158 in “double-data rate” configuration in response to rising edges and falling edges of the *clock input signal*, Grundy explains that the *memory device* 155 uses this *clock input signal* received via the *clock input port* to control storage elements 315. EX1009, [0088] (“In one implementation, such double-data rate capture is achieved by providing a first set of storage elements 315 to capture outputs of the differential receivers 310 in response to each rising edge of the clock signal 326, and a second set of storage elements 315 to capture outputs of the differential receivers 310 in response to a falling edge of the clock signal 326.”), FIG. 17. It is clear, therefore, that Grundy’s memory device receives a *clock signal* and uses this signal to control latching operations. *Id.*

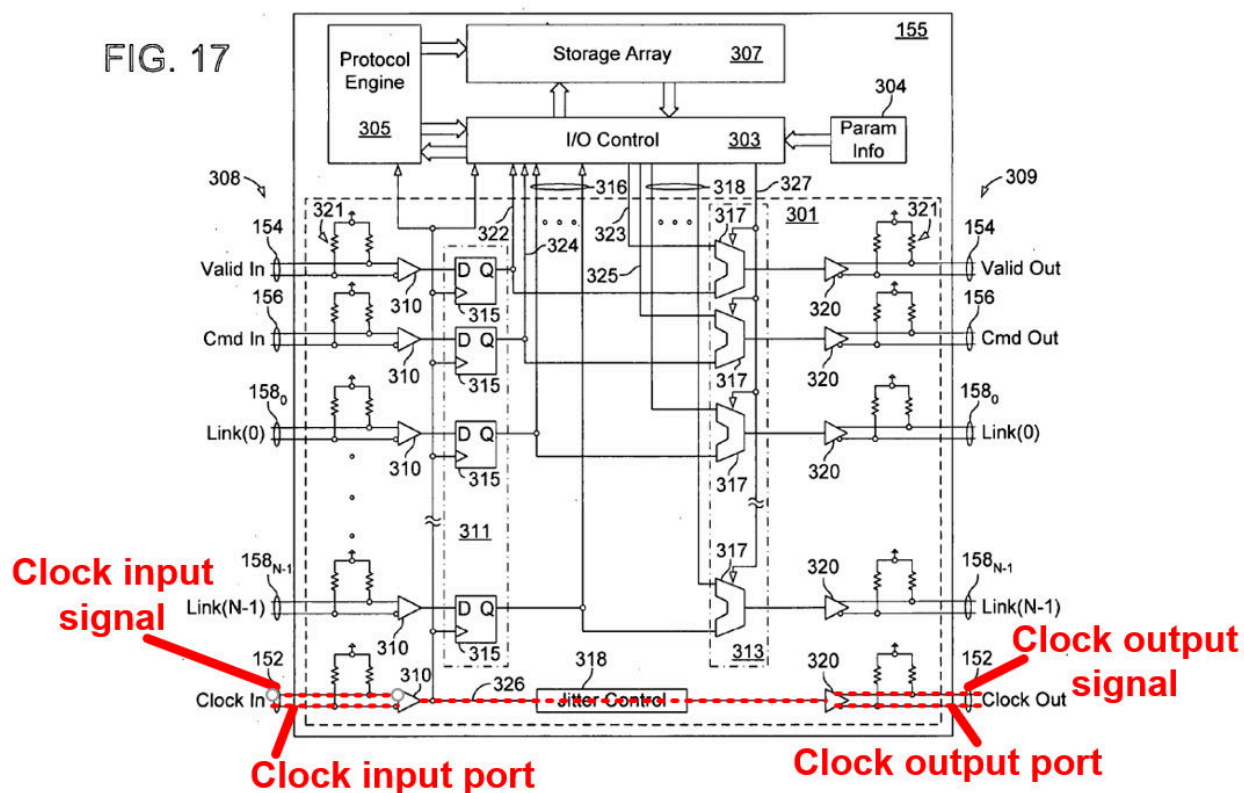
157. The Ryu-Cole-Arcoleo combination of Ground 1A provides a memory device that includes input ports for receiving a pair of complementary input strobe signals 12 (e.g., xxStbP, xxStbN). *Supra*, §VIII.B at [1c]. As I described above in my analysis of the Ryu-Cole-Grundy-Arcoleo combination, it would have been obvious to transform these input strobe signals 12 to continuous clock input signals as suggested by Grundy such that the combination renders obvious a *first clock input port* configured to receive a *first clock input signal* and a *second clock input port* configured to receive a *second clock input signal*. EX1009, [0047], FIG. 6; *supra*, §VII.E-F.

Element [1d]: a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;

158. As I described in my analysis of Ground 1A (§VIII.A), Element [1d], *supra*, Ryu explains that the ***non-volatile memory device*** generates an ***output signal*** referred to as a “data strobe signal D_STRB.” EX1005, [0011], [0016], [0064]-[0067], [0069], [0070], [0091]-[0095], FIGs. 5, 7, 11, 12, Cls. 10, 22. The ***non-volatile memory device*** generates this ***clock output signal*** “by delaying [a] read control signal REB by a predetermined delay time.” EX1005, [0064], *see also id.*, [0068], [0091] (“generating a...signal D_STRB, which is created by delaying the flash clock signal F_CLK by a predetermined time) [0092], [0095], FIGs. 5, 7, 11, 12, Cls. 10, 22.

159. It is even more apparent that Element [1d] is obvious in view of Grundy’s express disclosure of a clock output port. For example, Grundy explains that the memory device 155 is coupled to an “input-side clock line” and an “output-side clock line” that are each connected to the memory device at a respective port. EX1009, [0088], *see also id.*, [0043], [0047]-[0054], [0084], [0085], FIG. 17. A “logic level clock signal” can pass between a the port connected to the input-side clock line and the port connected to the output-side clock line. EX1009, [0088], *see also id.*, [0043], [0047]-[0054], [0084], [0085], FIG. 17. Grundy expressly discloses that the “logic level clock signal 326 is generated by the signal receiver 310 coupled to the input-side clock line 152,” and that “[t]he clock signal 326 is additionally provided to the output driver 320 coupled to the output-side clock line 152 to drive

the outgoing clock signal,” which means that Grundy expressly discloses a *clock output port* that drives a *clock output signal*. *Id.* According to Grundy, therefore, the memory device 155 includes a *clock output port* configured to drive a *clock output signal* that is referenced to a *clock input signal*. *Id.* In some cases, the clock output signal can be transferred to a subsequent memory device in the chain.



EX1009, FIG. 17 (annotated).

160. The fact that the memory device 155 represents one of a set of “chained memory devices” of a “chained memory system” further supports my opinion that it was obvious to include *clock input ports* and *clock output ports* on *non-volatile memory devices*. EX1009, [0043], *see also id.*, [0044]-[0083], FIGs. 5A-16. A

“clock line 152” passes through each of these chained memory devices, passing into each device through a clock input port and out of each device through a clock output port. *Id.* This is because each memory device in the chain includes a clock input port for receiving a clock input signal and a clock output port for transferring the clock output signal. *Id.*

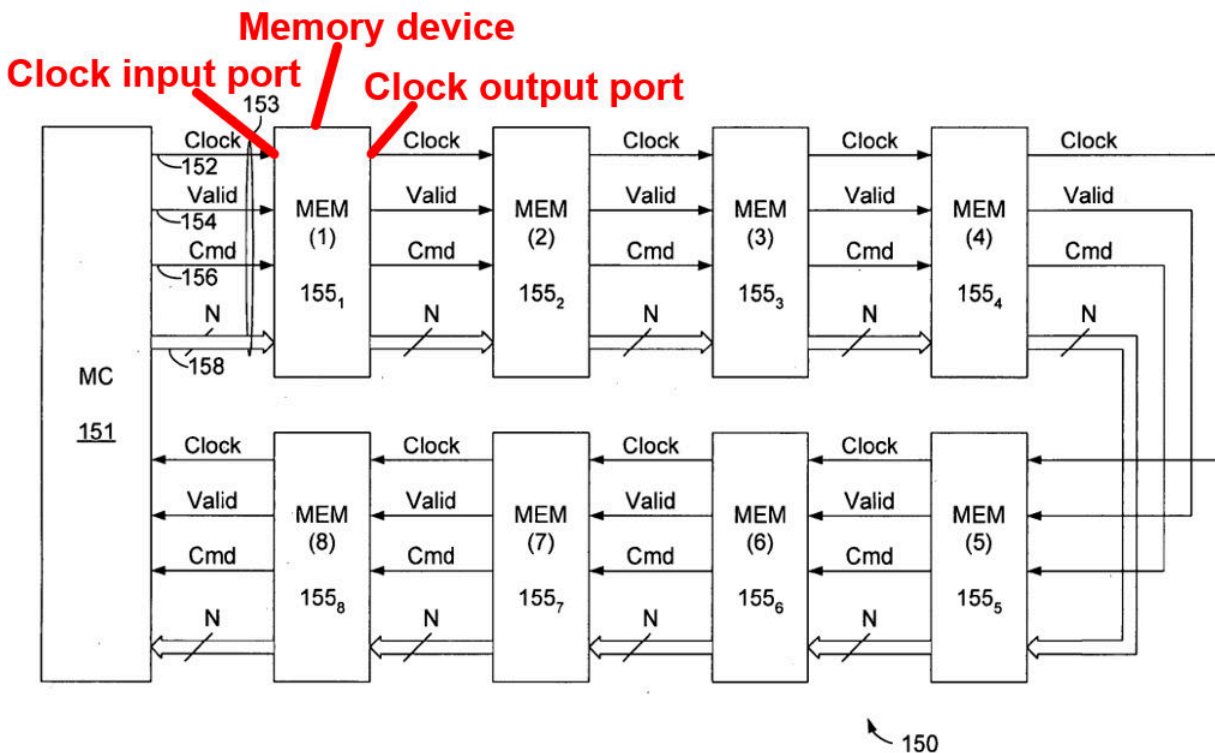


FIG. 5A

EX1009, FIG. 5A (annotated).

161. It is clear that the resulting non-volatile memory device includes a **clock output port** configured to transfer a **clock output signal** that is referenced to a **first clock input signal** when the non-volatile memory device of the Ryu-Cole-Arcoleo combination is implemented to include a clock line that passes through the device,

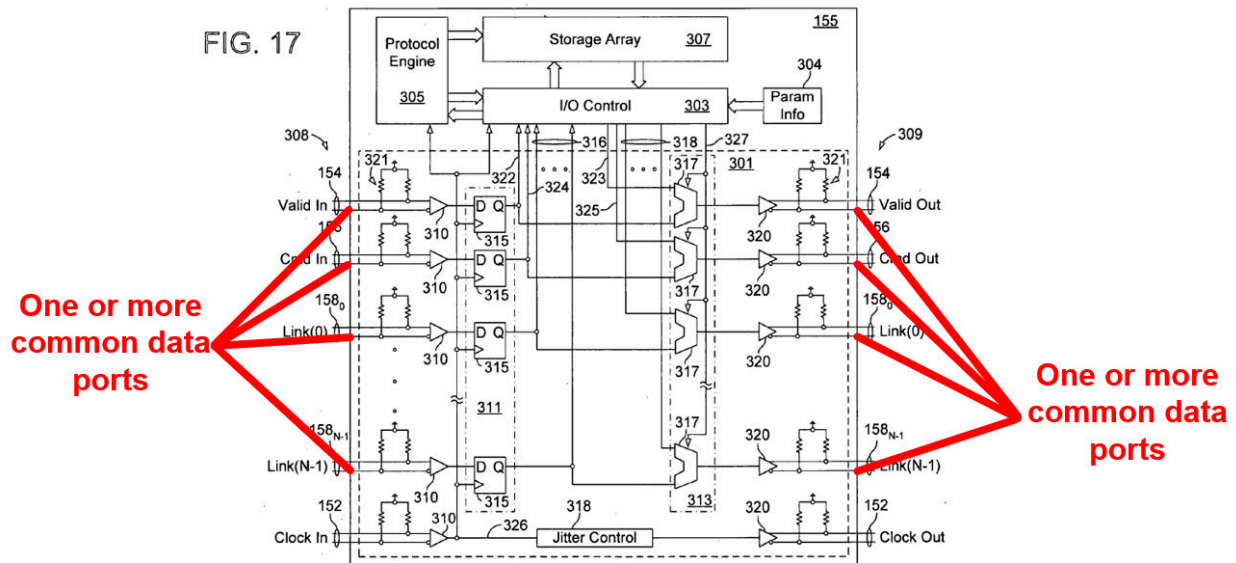
as suggested by Grundy. *Supra*, §VII.F. As I described above in my analysis of the Ryu-Cole-Arcoleo-Grundy combination, it would have been obvious to further modify Ryu's D_STRB to be a continuous clock output signal based on Grundy's teaching to use a continuous clock signal for synchronizing data transfer. *Supra*, §VII.F.

Element [1e]: one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;

162. As I described in connection with my analysis of Ground 1A (§VIII.A), Element [1e], *supra*, Ryu discloses that the ***non-volatile memory device*** includes an input/output pin that receives ***input data*** and sends ***output data***. EX1004, [0003], [0005]-[0007], [0009], [0038], [0041]-[0043], [0059], [0060], [0062], [0067], [0069], [0072], [0078], FIGs. 5, 7, 11, 12. Ryu also explains that a controller applies ***command data*** to the ***non-volatile memory device***, and the ***non-volatile memory device*** receives ***address data*** including an initial address (IADD) from an external source EX1004, [0003]-[0008], [0042], [0044], [0045], [0047]-[0049], [0051], [0053]-[0057], [0061]-[0064], FIGs. 5, 7. To the extent that Ryu does not describe how the ***non-volatile memory device*** receives this ***command data*** and ***address data***, Grundy describes a ***memory device*** 155 including ***one or more common data ports***

carrying *command data*, *address data*, *input data*, and *output data*. EX1009, [0043], [0044], [0047], [0048], [0054], [0084]-[0091], FIGs. 5A-5B, 17.

163. Element [1e] would have been even more obvious in view of the teachings of Grundy. For example, the *memory device* 155 of Grundy is connected to a clock line, a valid line, and a command line that are “used to conduct a clock signal, a valid signal, and a command signal, respectively.” EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17. I noticed that Grundy also explains that memory device 155 is connected to “a set of N multi-purpose lines” that are “used at alternate times to transfer N-bit wide data values and command values and are referred to collectively herein as a bus,” which means that *command data*, *input data*, and *output data* are driven by the memory device *Id*. According to Grundy, the command signal is used to “indicate whether a valid *command* or *data* value is being transmitted on the multi-purpose lines,” and the command signal is used to indicate that “the value transmitted on the multipurpose lines is a *command* (which may include *address* information).” *Id.*



EX1009, FIG. 17 (annotated).

164. The clock line, the valid line, and the command line, and the multi-purpose lines each pass through the memory device from an input to an output as depicted in FIG. 17 of Grundy. EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17. This further confirms my opinion that the ports associated with these lines are **common data ports**. These lines each transfer a **common data signal** from a device preceding memory device 155 in the chain to a device following the memory device 155 in the chain when memory device 155 is part of a chain of serially connected memory devices. *Id.* Consequently, memory device 155 includes **one or more common data ports** configured to transfer **common data signals**.

Element [1f]: a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended

signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

165. The Ryu-Cole-Arcoleo-Grundy combination discloses and renders obvious Element [1f] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Element [1f]. *Supra*, Ground 1A (§VIII.A) at Element [1f].

Element [1g]: a multi-user detector decision unit coupled to said parameter estimator and said received signals, wherein said multi-user detector decision unit selects a multi-user detector based upon at least one threshold;

166. The Ryu-Cole-Arcoleo-Grundy combination discloses and renders obvious Element [1g] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Element [1g]. *Supra*, Ground 1A (§VIII.A) at Element [1g].

Claim [4]: The configurable non-volatile memory device as claimed in claim 1, wherein each of the one or more common data ports comprises 1 bit.

167. The Ryu-Cole-Arcoleo-Grundy combination discloses and renders obvious Claim [4] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Claim [4]. *Supra*, Ground 1A (§VIII.A) at Claim [4]. Grundy further reinforces the obviousness Claim [4]. For example, Grundy discloses a ***memory device*** that includes ***one or more common data ports*** including ports for a “valid line,” ports for a “command line,” and ports for “multipurpose lines,” among other ports. EX1009, [0043], *see also id.*, [0047], [0048], [0054], [0085], FIGs. 5A-5B, 17. The “a set of N multi-purpose lines” and “multi-purpose lines 158,” as

described by Grundy, are used at alternate times to transfer N-**bit** wide data values and command values.” EX1009, [0043], [0044], *see also id.*, [0051], [0061]. This means that it is clear that each of the N multi-purpose lines handle **1 bit**, and the **one or more common data ports** therefore each comprise **1 bit**.

168. The **one or more common data ports** that transfer these signals each comprise **1 bit** (e.g., a “0” for the low logic level and a “1” for the high logic level), because Grundy also explains that the valid signal and the command signal can be asserted at a high logic level or a low logic level. EX1009, [0043]. The valid line, the memory line, and each multi-purpose line of Grundy are connected to a “differential receiver 310” that judges the logic level of the line and an “output driver 320” that generates a binary signal having a high or low logic value, which reinforces my opinion that these lines are associated with common data ports. EX1009, [0086]-[0088], FIG. 17. Consequently, when the **non-volatile memory device** of the Ryu-Cole-Arcoleo combination is implemented with the **one or more common data ports** of Grundy, the **one or more common data ports** each comprise **1 bit**. *Id.*

Claims [2], [3], and [10]-[17]

Claim [2]: The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively.

Claim [3]: The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal and the second clock input signal are data latching clock signals.

Claim [10]: The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration.

Claim [11]: The configurable non-volatile memory device as claimed in claim 1, further comprising a configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers.

Claim [12]: The configurable non-volatile memory device as claimed in claim 1, wherein the output data is edge aligned with the clock output signal.

Claim [13]: The configurable non-volatile memory device as claimed in claim 1, further comprising a reset port configured to receive a reset signal for resetting the configurable non-volatile memory device to a default configuration.

Claim [14]: The configurable non-volatile memory device as claimed in claim 13, wherein the default configuration comprises the single ended signaling configuration.

Claim [15]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a flash memory device.

Claim [16]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NOR flash memory device.

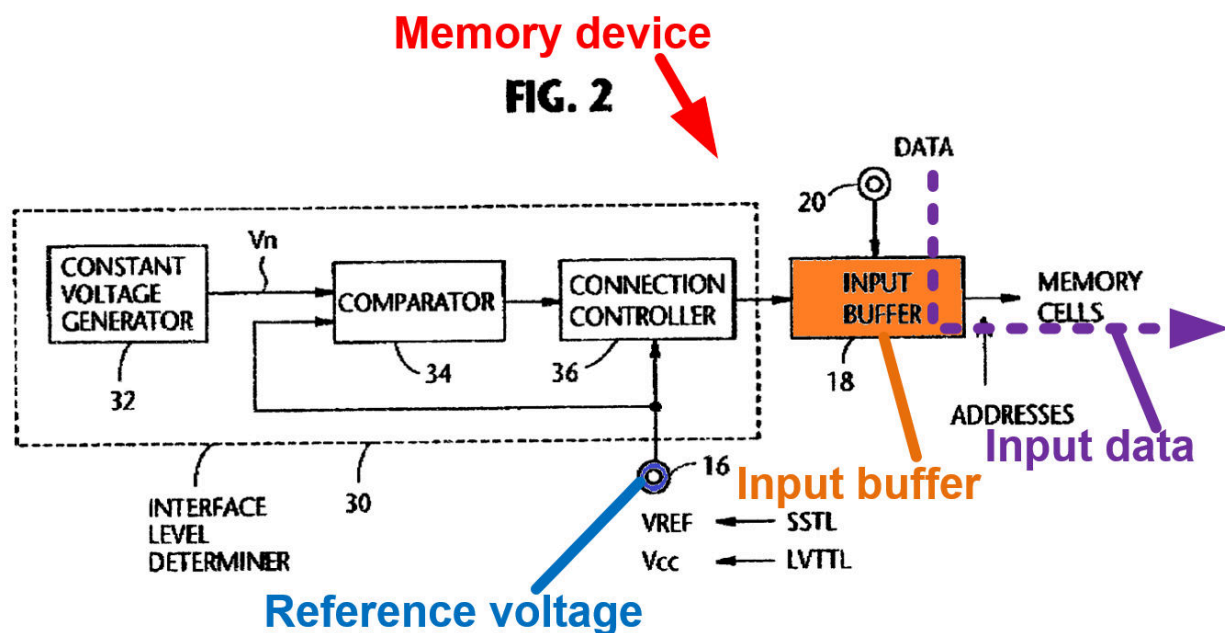
Claim [17]: The configurable non-volatile memory device as claimed in claim 1, wherein the configurable non-volatile memory device is a NAND flash memory device.

169. The Ryu-Cole-Arcoleo-Grundy combination renders obvious Claims [2], [3], and [10]-[17] for at least the same reasons that I addressed above in connection with Ground 1A (§VIII.A) at Claims [2], [3], and [10]-[17]. *See supra*, Ground 1A (§VIII.A) at Claims [2], [3], and [10]-[17].

C. GROUND 1C: The Ryu-Cole-Arcoleo-Akashi Combination Renders Claims 5-9 Obvious

Claim [5]: *The configurable non-volatile memory device as claimed in claim 1, further comprising one or more configurable data input buffers configured to utilize a reference voltage for determining logic levels of the common data signals.*

170. The *non-volatile memory device* of Ryu receives data “through an input/output pin” of an “*input/output buffer*.” EX1004, [0003], [0005]-[0007], [0041]-[0043], [0058]-[0062], [0076]-[0078], [0090], FIG. 5. Even if Ryu does not describe the *input/output buffer* as being configurable to utilize a *reference voltage* for determining logic levels of *common data signals*, Akashi provides these features. EX1008, 1:7-2:34, 2:41-3:24, 3:46-4:34, FIG. 2. For example, the memory device of Akashi includes an “*input buffer 18*” having a “data pin 20” that receives *input data* and drives this *input data* to “memory cells.” EX1008, 2:8-17, FIGs. 1-2.



EX1008, FIG. 2 (annotated).

171. A *common data signal* that is substantially similar to data described by the '028 Patent that includes data received by the *input buffer* 18 via data input pin 20 and forwarded to the “memory cells” is substantially similar to data described by the '028 Patent. EX1008, 1:58-2:25, FIG. 2; *cf.* EX1001, 3:37-67 (“[t]he differential input buffer is coupled to the data input pin for receiving the input data, and is enabled in the first mode for sensing logic levels of the input data relative to the voltage”), 5:26-58, 10:42-11:18, FIG. 3B.

172. Akashi’s *input buffer* 18 is connected to an interface level determiner 30 that receives a *reference voltage* (VREF) via an external terminal 16. EX1008, 2:8-34, 3:49-34, FIGs. 1, 2. For example, Akashi discloses that “[w]hen the memory chip dedicated to SSTL levels is used, a *reference voltage* VREF is applied to an external terminal 16.” EX1008, 2:8-17. Akashi also discloses that “it is assumed that a reference voltage VREF utilized for SSTL mode is about 1.5 volts” and “VREF applied to the pin 16 is routed to the input buffer 18 via the connection controller 36.” EX1008, 4:3-21. To determine *logic levels* of *common data signals* including input data received by data input pin 20, Akashi explains that the input buffer 18 uses this *reference voltage* VREF including input data received by data input pin 20. EX1008, 1:26-43 (“voltages higher than (VREF +0.4) volts are determined as a high voltage, and all voltages lower than (VREF -0.4) volts are recognized as a low

voltage”), 2:8-17 (“voltages applied to the buffer 18 via a data input pin 20 are recognized as a high or a low logic level using the reference voltage VREF (viz., at SSTL levels) as mentioned above”).

173. When the input data represents a stub series terminated logic (SSTL) signal or when the input data represents a low voltage transistor-transistor logic (LVTTL) signal, the input buffer 18 of Akashi is configurable to judge input data received by the data input pin 20. EX1008, 1:14-2:34, 2:41-63, 4:3-34, FIG. 2. In the SSTL mode, Akashi explains that “comparator 34 generates a high logic” and “VREF...is routed to the input buffer 18,” whereas in the LVTTL mode, Akashi explains that “comparator 34 generates a low logic level” and “no voltage is transferred to the input buffer 18.” EX1008, 4:3-22. This means that VREF serves as a signal for configuring the input buffer to operate in the SSTL mode or the LVTTL mode.

174. The input buffer 18 of Akashi is therefore strikingly similar to the data input buffer of the '028 Patent, which is configurable to operate according to a high speed transceiver logic (HSTL) signaling format where the buffer receives a reference voltage or an LVTTL signaling format where no reference voltage is used. Cf. EX1001, 8:8-30, 10:10-27, 13:50-14:24, FIG. 5. Because the input buffer 18 of Akashi is configurable in a way that is strikingly similar to how the input buffer of the '028 Patent is configurable, it is clear that Akashi provides a *configurable data*

input buffer. Id. Akashi also explains that “[w]hen the user intends a memory device at SSTL mode in accordance with the manufacture’s (*sic*) instructions, he or she applies VREF to the pin 16” and “when the user intends a memory device at LVTTL mode in accordance with the manufacture’s instructions, he or she applies Vcc to the pin 16,” further confirming that input buffer 18 is configurable. EX1008, 4:3-22.

175. As I described above in my analysis of the Ryu-Cole-Arcoleo-Akashi combination (*Supra*, §VIII.H), a POSITA would have applied Akashi’s teachings in the combination with Ryu, Cole, and Arcoleo for the reasons discussed above (*Supra*, §VIII.H), and the resulting *non-volatile memory device* would predictably include a *configurable data input buffer* that utilizes a *reference voltage* for determining *logic levels of common data signals* as taught in Akashi.

Claim [6]: The configurable non-volatile memory device as claimed in claim 5, wherein the reference voltage is set to a predetermined voltage level.

176. The *reference voltage* VREF of Akashi can be set to a *predetermined voltage level* such as 1.5 volts. EX1008, 4:3-14 (“a reference voltage VREF utilized for SSTL mode is about 1.5 volts...VREF applied to the pin 16 is routed to the input buffer 18 via the connection controller 36”), *see also id.*, 2:8-17 (“a reference Voltage VREF is applied to an external terminal 16...relays or transfer the reference voltage VREF to an input buffer 18 which typically takes the form of a differential transistor pair”). According to a second embodiment described by Akashi, “the user intends a memory device at LVTTL mode” and the user “applies Vcc to the pin 16.”

EX1008, 4:15-22. The second embodiment also involves a reference voltage being set to a *predetermined voltage level* because Akashi explains that “the power source Vcc is about 3.3 Volts.” EX1008, 4:3-14.

Claim [7]: The configurable non-volatile memory device as claimed in claim 5, wherein the reference voltage is set to half of the common data signal's high logic level.

177. Akashi explains that “it is assumed that a reference voltage VREF utilized for SSTL mode is about 1.5 volts and that the power source Vcc is about 3.3 Volts.” EX1008, 4:3-14. Akashi also discloses that “the SSTL specification dictates that all voltages higher than (VREF +0.4) volts are determined as a high Voltage, and all Voltages lower than (VREF -0.4) volts are recognized as a low voltage.” EX1008, 1:26-44. This means that a data bit of a common data signal having value more than 0.4 volts greater than the predetermined voltage is judged to be at the high logic level, meaning that any value greater than 1.9 volts is judged to be the high logic level when the predetermined voltage is 1.5 volts as suggested by Akashi. The predetermined voltage of 1.5 volts is half of the high logic level of the common data signal in examples where high bits of the common data signal have a high value of 3.0 volts.

Claim [8]: The configurable non-volatile memory device as claimed in claim 1, wherein the first clock input signal, the second clock input signal and the common data signal are terminated signals.

178. Akashi expressly discloses a memory device that operates “at SSTL levels,” referring to “stub series *terminated* logic.” EX1008, 1:26-2:34, 2:41-63, 4:3-14, 4:23-34, FIG. 2. Signals input to the memory device represent a *terminated* signal to improve performance of the device when Akashi’s memory device uses *terminated* logic. *Id.* For example, Akashi explains that “[t]he SSTL specification is particularly intended to improve operations in situations where buses must be isolated from relatively large stubs.” EX1008, 1:26-2:34. To improve signal accuracy and allow buses to be isolated from relatively large stubs, a POSITA would have been motivated to implement the *non-volatile memory device* of the Ryu-Cole-Arcoleo combination to include *terminated signals* (e.g., according to the SSTL specification) as suggested by Akashi. *Supra*, §VII.H.

179. In the combination, it would have been understood and obvious to a POSITA that a non-volatile memory device implementing SSTL as taught in Akashi would use *terminated signals* for the *first clock input signal*, the *second clock input signal*, and the *common data signal* because that is what SSTL calls for, namely terminated signals. EX1008, 1:26-43; *supra*, §VII.H. Multiple references also corroborate that it was well known by the Critical Date of the ’028 Patent to use *terminated signals*, including signals according to the SSTL specification, for *clock signals* and *data signals* like those recited in claim 8. *See, e.g.*, EX1019, 3 (describing a memory device including a terminated clock signal “RClk[2]” and a

terminated data signal “bus data [18:0]”); EX1020, 13:35-14:48 (describing “termination circuits” for terminating data signals).

Claim [9]: The configurable non-volatile memory device as claimed in claim 8, wherein the first clock input signal, the second clock input signal and the common data signals are SSTL signals.

180. The Ryu-Cole-Arcoleo combination discloses and renders obvious Claim [8] for at least the same reasons that I addressed above in connection with Claim [8]. *Supra*, Claim [8].

D. GROUND 1D: The Ryu-Cole-Arcoleo-Grundy-Akashi Combination Claims 5-9 Obvious

181. The Ryu-Cole-Arcoleo-Grundy-Akashi combination renders obvious Claims [5]-[9] for at least the same reasons that I addressed above in connection with Ground 1C (§VIII.C) at Claims [5]-[9]. *See supra*, Ground 1C (§VIII.C) at Claims [5]-[9].

IX. CONCLUSION

182. For all the reasons I have noted in the foregoing paragraphs, claims 1-17 of the '028 Patent are obvious in view of the references discussed above.

183. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

APPENDIX A

Carl Sechen

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Research Interests

My research interests center primarily on the design and computer-aided design of digital and analog integrated circuits. Ongoing projects include the design of secure ICs that cannot be reverse engineered. We are continuing the development of the TRAP (TRAnsistor-level Programmable) fabric that implements 10X more logic in the same area compared to lookup-table based FPGAs and eFPGAs, making it the first practical approach to secure hardware via IC redaction.

Education

Ph.D., Electrical Engineering, University of California, Berkeley, 1986
Thesis: *Placement and Global Routing of Integrated Circuits Using Simulated Annealing*
Advisor: Prof. Alberto Sangiovanni-Vincentelli
M.S., Electrical Engineering, Massachusetts Institute of Technology, 1977
Advisor: Prof. Stephen Senturia
B.E.E., Electrical Engineering, University of Minnesota, 1975

Employment history

Professor, University of Texas at Dallas August 15, 2005 – present
Professor, University of Washington July 1999 – August 14, 2005
Associate Professor, University of Washington July 1992 – June 1999
Associate Professor, Yale University July 1990 – June 1992
Assistant Professor, Yale University July 1986 – June 1990

University Administrative Positions

Director of ECS Tech Support Services, UTD, June 2012 – February 2014

Honors and Awards

- *Best Paper Award* at the 2017 IEEE PhD Research in Microelectronics and Electronics Conference (PRIME), for the paper “Improved Lagrangian Relaxation-based Gate Size and VT Assignment for Very Large Circuits”, Bariloche, Argentina, February 2017.
- Nominated for a *Best Paper Award* for: “A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration”, *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 27-31, 2017, Lausanne, Switzerland.
- Nominated for UTD’s President’s Teaching Excellence Award for Graduate/Professional Instruction, 2020.
- Received the *Graduate Teaching Excellence Award* from the ECE Department at UT Dallas, May 2024.
- Received the *Distinguished Teaching Award* for the Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2014.
- Received the *Distinguished Teacher of the Year Award*, Dept. of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, 2008.
- Elected *IEEE Life Fellow* in 2002

- Elected a Fellow of Asia-Pacific Artificial Intelligence Association (AAIA)
- Received the *Outstanding Research Advisor Award*, Department of Electrical Engineering, University of Washington, 2002.
- Received the *Best Project Award*, NSF Center for the Design of Digital and Analog ICs (CDADIC), July 2002.
- Received the Semiconductor Research Corporation's 2001 *SRC Inventor's Recognition Award*
- Received the Semiconductor Research Corporation's 1994 *SRC Technical Excellence Award*
- Received the Semiconductor Research Corporation's 1988 *SRC Inventor's Recognition Award*

Litigation Support Experience

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Hsuanyeh Law Group PC
Case Name:	<i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-259 (W.D. Tex., filed June 2, 2023)
Services Provided:	Expert Reports
Disposition:	Ongoing
Date:	April 2024 to present

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Akin Gump Strauss Hauer & Feld LLP
Case Name:	<i>Vervain, LLC v. Kingston Technology Corp., et al.</i>
Services Provided:	Declarations filed
Disposition:	Ongoing
Date:	February 2025 to present

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Latham Watkins
Case Name:	Vervain v. Western Digital Civil Action No. 6:21-cv-00488-ADA
Services Provided:	Expert Reports for Western Digital; one deposition
Disposition:	settled
Date:	August 2021 to July 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Orrick, Herrington, and Sutcliffe
Case Name:	Godo Kaisha IP Bridge 1 v. Micron Technology, Inc., et al., Civil Action No. 6:20-cv-00178-ADA (W.D. Tex.)
Services Provided:	Two expert reports on behalf of Micron
Disposition:	Case dismissed
Date:	August 2020 – July 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Arnold & Porter
Case Name:	Taiwan Semiconductor Manufacturing Co. v. Silicon Storage Tech., Inc. AAA Case No. 01-21-0002-5445
Services Provided:	None yet
Disposition:	pending
Date:	Started July 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Arnold & Porter
Case Name:	Intel v. BeSang

Services Provided:	Work on IPRs on behalf of Intel
Disposition:	pending
Date:	March 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Anova Law Group, PLLC
Case Name:	Chongqing HKC Optoelectronics Technology Co., Ltd. v. 138 East LCD Advancements Limited
Services Provided:	Two IPRs on behalf of the Petitioner (Chongqing)
Disposition:	pending
Date:	Started December 2022

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Perkins Coie
Case Name:	Intel v. BitMICRO
Services Provided:	Two IPR declarations on behalf of Intel
Disposition:	pending
Date:	Started October 2021

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Perkins Coie
Case Name:	Impinj v. NXP Civil Action NO. 6:21-cv-00530-ADA
Services Provided:	Expert Reports on behalf of Impinj and one trial testimony in Waco
Disposition:	Complete victory for Impinj; \$45 million settlement, plus \$15 million annually
Date:	October 2021 through November 7, 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Wilmer Cutler Pickering Hale and Dorr LLP (“WilmerHale”)
Case Name:	Civil Action No. 6:19-cv-404-ADA FLASH-CONTROL, LLC, Plaintiff, v. INTEL CORPORATION; IN THE UNITED STATES DISTRICT COURT FOR THE WESTERN DISTRICT OF TEXAS AUSTIN DIVISION
Services Provided:	Expert consultation on behalf of Intel
Disposition:	unkown
Date:	Started January 2020 ended 2022

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	Arigna Technology Limited v. Volkswagen AG et al., Case No. 2:21-cv-00054-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation and testimony
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	<i>Arigna Technology Limited v. Bayerische Motoren Werke AG et al.</i> , Case No. 2:21-cv-00172-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	<i>Arigna Technology Limited v. Porsche AG, et al.</i> , Case No. 2:21-cv-00173-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	<i>Arigna Technology Limited v. General Motors Company, et al.</i> , Case No. 2:21-cv-00174-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	Patent litigation
Law Firm:	Susman Godfrey LLP
Case Name:	<i>Arigna Technology Limited v. Daimler AG, et al.</i> , Case No. 2:21-cv-00175-JRG-RSP (E.D. Tex.)
Services Provided:	Expert consultation
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	ITC Investigation
Law Firm:	Susman Godfrey LLP
Case Name:	<i>In The Matter of Certain Power Inverters and Converters, Vehicles Containing the Same and Components Thereof</i> , Inv. No. 337-TA-1267 (ITC)
Services Provided:	Expert consultation and testimony
Disposition:	Settled
Date:	Started 12/06/2020 ended June 2023

Expert Engagement

Type of Matter:	IPR filing
Law Firm:	Kirkland & Ellis LLP
Case Name:	Case 1:19-cv-01006-UNA IPR PACT XPP Schweiz AG v. Intel Corporation IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE
Services Provided:	Expert consultation toward the filing of an IPR on behalf of Intel
Disposition:	Unknown
Date:	Started December 2019 ended 2022

Expert Engagement

Type of Matter:	IPR filing
Law Firm:	Wilmer Cutler Pickering Hale and Dorr LLP (WilmerHale)
Case Name:	VLSI Technology, LLC v. Intel Corporation, No. 3:17-cv-05671-BLF (N.D. Cal.), VLSI Technology, LLC v. Intel Corporation, No. 1:18-cv-00966-CFC-CJB (D. Del.) VLSI Technology, LLC v. Intel Corporation, No. 6:19-cv-00256-ADA (W.D. Tex.)
Services Provided:	Two declarations in support of an Intel IPR and two depositions
Disposition:	Unknown
Date:	Started May 1, 2019, ended July 30, 2020

Expert Engagement

Type of Matter:	Patent infringement and associated IPR filing
Law Firm:	Baker Botts (DC case) and Sterne, Kessler, Goldstein & Fox P.L.L.C. (IPR case)
Case Name:	Case No. 1:18-cv-555-LY UNITED STATES DISTRICT COURT WESTERN DISTRICT OF TEXAS AUSTIN DIVISION POLARIS INNOVATIONS, LTD., an Ireland limited company, Plaintiff, v. ADVANCED MICRO DEVICES, INC
Services Provided:	Filing a declaration in support of the IPR and planning for the district court case
Disposition:	Case dissolved
Date:	Started February 2019; ended May 2020

Expert Engagement

Type of Matter:	Trade secret case before an Arbitration Panel
Law Firm:	Anova Law Group
Case Name:	TVL International LLC v. Zhejiang Shenghui Lighting Co., Ltd. Case No. 01-17-0004-7802 AMERICAN ARBITRATION ASSOCIATION CHARLOTTE, NORTH CAROLINA

	<i>In the matter of arbitration between</i> TVL INTERNATIONAL LLC, Claimant, v . ZHEJIANG SHENGHUI LIGHTING CO., LTD. and SENGLED USA, INC.
Services Provided:	Three expert reports completed, and testimony before the Arbitration Panel
Disposition:	Ended with TVL declared the winner
Date:	April 9, 2018 through August 31, 2018.

Expert Engagement

Type of Matter:	Challenge of Patent Validity
Law Firm:	Weil, Gotshal and Manges; but in the future: Orrick, Herrington & Sutcliffe
Case Name:	North Star Innovations, Inc. v Micron Technology, Inc., et al., Case 17-cv-506-LPS-CJB, D. Del.
Services Provided:	Research in support of an IPR regarding Patent 5,943,274 on behalf of Micron
Disposition:	In progress but no work performed to date
Date:	March 5, 2018 through present

Expert Engagement

Type of Matter:	Challenge of Patent Validity
Law Firm:	Baker Botts
Case Name:	Advanced Micro Devices v. Broadcom
Services Provided:	One declaration in support of an IPR regarding Patent 7,472,151 Case No. Unassigned Patent 7,472,151 DECLARATION OF DR. CARL SECHEN IN SUPPORT OF PETITION FOR <i>INTER PARTES</i> REVIEW OF U.S. PATENT NO. 7,472,151
Disposition:	Settled not long after the IPR was filed
Date:	December 3, 2016 through March 27, 2017

Expert Engagement:

Type of Matter:	Trade Secret Misappropriation
Law Firm:	Wilson Sonsini Goodrich & Rosati
Case Name:	GSI Technology, Inc. v. United Memories, Inc. and Integrated Silicon Solution, Inc.; Case No. 5:13-cv-1081-PSG in the United States District Court for the Northern District of California, San Jose Division
Services Provided:	One declaration on behalf of ISSI, one deposition and one trial testimony before a jury
Disposition:	ISSI was victorious at trial and upon appeal
Date:	May 2014 through November 2015

Expert Engagement:

Type of Matter:	Patent validity – PTO re-examination proceedings
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Law Firm:	Bruce Itchkawitz, Knobbe Martens Olson & Bear; Rich Kim, Mehran Arjomand, and David Kim, Morrison & Foerster LLP
Case Name:	Netlist, Inc. vs. Google, Inphi Corp., and Smart Modular Technologies <u>Individual cases in the last 5 years:</u> <ol style="list-style-type: none"> 1. <i>Inter Partes</i> Review No. IPR2017-00667 2. <i>Inter Partes</i> Review No. IPR2017-00549 3. <i>Inter Partes</i> Review No. IPR2017-00692 4. <i>Inter Partes</i> Review No. IPR2017-00562 5. <i>Inter Partes</i> Review No. IPR2017-00561 6. <i>Inter Partes</i> Review No. IPR2017-00587 7. <i>Inter Partes</i> Review No. IPR2017-00560 8. Appeal No. 2015-006849 9. Appeal No. 2015-007761 10. <i>Inter Partes</i> Review No. 2015-01021 11. Reexamination Control No.: 95/001,337 12. <i>Inter Partes</i> Review No. IPR2014-0097 13. <i>Inter Partes</i> Review No. IPR2014-00970 14. <i>Inter Partes</i> Review No. IPR2014-01011 15. <i>Inter Partes</i> Review No. IPR2014-00883 16. <i>Inter Partes</i> Review No. IPR2014-00883 17. Appeal No. 2013-009044
Services Provided:	25 declarations, 5 depositions on behalf of Netlist, Inc., filed July 2011 through May 2015 supporting patent validity challenges before the PTO Worked on 6 separate IPR's, each involved writing an expert report and giving a deposition.
Disposition:	Pending
Date:	June 28, 2011 through March 2018

Expert Engagement:

Type of Matter:	Patent invalidity and patent non-infringement
Law Firm:	Wilson Sonsini Goodrich & Rosati (representing the defendant)
Case Name:	HSM Portfolio, LLC, Technology Properties Limited, LLC v. Advanced Micro Devices (defendant) Case: 1:11-cv-00770-RGA (D. Del.)
Services Provided:	Work toward declaration on patent non-infringement
Disposition:	Settled in defendant's favor
Date:	April 2013 through December 2013

Expert Engagement:

Type of Matter:	Patent non-infringement
Law Firm:	Jones Day (representing the defendant)
Case Name:	Intellectual Ventures v. Xilinx (defendant) IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiffs, v.

	ALTERA CORPORATION, MICROSEMI CORPORATION, LATTICE SEMICONDUCTOR CORPORATION and XILINX, INC., Defendants. C.A. No. 10-1065 (LPS) (CONSOLIDATED)
Services Provided:	One declaration on patent non-infringement; one deposition
Disposition:	Settled in defendants' favor
Date:	February 2013 through April 2014

Expert Engagement:

Type of Matter:	Patent non-infringement
Law Firm:	Morrison Foerster (representing the defendant)
Case Name:	Intellectual Ventures v. Altera (defendant) IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, Plaintiffs, v. ALTERA CORPORATION, MICROSEMI CORPORATION, LATTICE SEMICONDUCTOR CORPORATION and XILINX, INC., Defendants. C.A. No. 10-1065 (LPS) (CONSOLIDATED)
Services Provided:	One declaration on patent non-infringement; one deposition
Disposition:	Settled in defendant's favor
Date:	February 2013 through December 2013

Expert Engagement:

Type of Matter:	Patent validity and patent infringement
Law Firm:	Antonelli, Harrington & Thompson LLP
Case Name:	Guardian Media Technologies, Ltd., Plaintiff, v. Acer America Corp, et al., Defendants. <u>Cases:</u> CIVIL ACTION NO. 6:10-CV-597-LED Case No. 2:13-CV-08369 PSG (PLAx)
Services Provided:	One declaration on patent validity and two declarations on patent infringement
Disposition:	Settled in Plaintiff's favor
Date:	February 2013 through March 2015

Expert Engagement:

Type of Matter:	Patent infringement
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Law Firm:	Winston & Strawn (Nanya)
Case Name:	On Technologies vs. Nanya
Services Provided:	Work on claim term definitions
Disposition:	Case was transferred from East. Dis. Texas to No. Calif. in late 2010; then settled
Date:	March 2010 through October 2010

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	White and Case (Panasonic)
Case Name:	Freescall Semiconductor vs. Panasonic
Services Provided:	Invalidity and non-infringement expert reports filed November 2010; deposition December 2, 2010
Disposition:	ITC case settled January 2011
Date:	April 2010 through January 2011

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	Weil, Gotshal and Manges (Samsung)
Case Name:	Rambus vs. Samsung
Services Provided:	<p>One Declaration, One Deposition, and one trial testimony for Samsung</p> <p><u>Declaration:</u> This report overviewed Rambus technology and patents, their alleged “steering” of patent claims, and Samsung’s subsequent DDR products.</p> <p><u>Deposition:</u> Dr. Sechen was asked to consider whether Samsung’s subsequent DDR products, DDR2, DDR3, GDDR, GDDR2, GDDR3, and GDDR4 fell within the scope of their 2000 license agreement with Rambus. Representing attorney: Matt Antonelli.</p> <p><u>Trial Testimony:</u> Dr. Sechen testified before Judge Ronald Whyte, San Jose, CA, that Samsung’s subsequent DDR products, DDR2, DDR3, GDDR, GDDR2, GDDR3, and GDDR4 fell within the scope of their 2000 license agreement with Rambus. Representing attorney: Matt Antonelli.</p>
Disposition:	Dr. Sechen’s involvement completed on 30 September 2008 with the conclusion of the trial.
Date:	May 2008 through September 2008

Expert Engagement:

Type of Matter:	Patent infringement
Law Firm:	O’Melveny & Myers (Magma)
Case Name:	Synopsys vs. Magma Design Automation
Services Provided:	<p>Two Declarations, One Supplemental Declaration and Two Depositions for Magma</p> <p><u>Declaration:</u></p>

	<p>June 10, 2005: Dr. Sechen illustrated that the material in the Synopsys patents (originally patented by Magma, but awarded to Synopsys by the court) were put into the public domain by Magma. In addition, he illustrated that the material in the Synopsys patents were generally in the public domain prior to the patents.</p> <p><u>Declaration:</u> Dr. Sechen wrote a declaration supporting Magma’s proposed claim constructions for the two patents involved on July 21, 2005.</p> <p><u>Supplemental Declaration:</u> July 13, 2005 Dr. Sechen had a supplemental declaration showing that Synopsys’ expert report in fact was consistent and in agreement with his first declaration.</p> <p><u>Deposition:</u> Aug. 10, 2005: Dr. Sechen was deposed on the July 21, 2005 declaration. Representing attorney: Mark Miller.</p> <p><u>Deposition:</u> Dec. 16, 2005: Dr. Sechen was deposed on the June 10, 2005 declaration and on the supplemental declaration of July 13, 2005. Representing attorney: Mark Miller.</p>
Disposition:	Settled after court made several rulings in Magma’s favor
Date:	Started January 2005; Ended January 2006

Expert Engagement:

Type of Matter:	Trade Secret Misappropriation and Patent Enforcement
Law Firm:	Susman Godfrey
Case Name:	UniRAM Technology vs. Monolithic System Technology and TSMC
Services Provided:	<p>3 Expert Reports, 1 Declaration and 2 Depositions, and 2 trial testimonies for UniRAM.</p> <p><u>Expert Report:</u> May 19, 2005: Expert report covered claim construction issues</p> <p><u>Declaration:</u> May 19, 2005: Declaration in support of plaintiff UniRAM’s response to TSMC’s motion for summary judgment of inequitable conduct. (Subject of the 2nd trial testimony.)</p> <p><u>Expert Report:</u> May 31, 2007: Expert report that concluded that the UniRAM trade secrets were not and are not generally known, and that the UniRAM trade secrets created significant value for the defendants.</p> <p><u>Expert Rebuttal Report:</u> Expert rebuttal report filed on June 13, 2007.</p>

	<p><u>Deposition:</u> June 21, 2005: Deposition concerning expert report of May 19, 2005. Representing attorney: Russ Chorush.</p> <p><u>Deposition:</u> June 28, 2007: Deposition regarding expert report of May 31, 2007 and to a lesser degree the May 19, 2005 declaration. Representing attorney: Russ Chorush.</p> <p><u>Trial Testimony:</u> September 2007 trial concerning Dr. Sechen's expert report of May 31, 2007. Representing attorneys: Russ Chorush (Heim, Payne and Chorush) and Joseph Grinstein (Susman Godfrey).</p> <p><u>Trial Testimony:</u> January 2008 regarding my declaration of May 19, 2005. Representing attorneys: Russ Chorush (Heim, Payne and Chorush) and Joseph Grinstein (Susman Godfrey). The presiding judge specifically commented on Dr. Sechen's credibility in his final judgment.</p>
Disposition:	\$32 million judgment for UniRAM
Date:	Started February 2005; Ended January 15, 2008

Expert Engagement:

Type of Matter:	Patent validity and infringement (both to PTO and trial)
Law Firm:	Squire, Sanders and Dempsey (Hitachi)
Case Name:	Translogic vs. Hitachi
	<p>4 expert reports, 2 declarations, 1 deposition and trial testimony for Hitachi</p> <p><u>Expert Disclosure Statement:</u> Expert disclosure statement of July 25, 2003. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively "Hitachi") to compare claims of U.S. Patent No. 5,162,666 ("the '666 Patent") with certain technical references which were prior art to the '666 Patent. Plaintiff Translogic Technology, Inc. ("Translogic") asserted claims of the '666 Patent against Hitachi.</p> <p><u>Supplemental Expert Disclosure:</u> Supplemental expert disclosure statement of September 19, 2003. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively "Hitachi") to compare claims of U.S. Patent No. 5,162,666 with certain technical references which were prior art. Dr. Sechen supplemented the Expert Disclosure Statement he previously submitted in this case based on</p>

	<p>his review of the Report and Recommendation of Special Master Regarding Claim Construction.</p> <p><u>Expert Disclosure Statement:</u> Expert disclosure statement of February 9, 2004. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively “Hitachi”) to analyze certain circuits in Hitachi microprocessors that Translogic Technology, Inc. (“TTI”) accuses of infringing Patent No. 5,162,666 (“the ‘666 Patent”). Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products.</p> <p><u>Supplemental and Restated Expert Disclosure Statement:</u> Supplemental and restated expert disclosure statement of September 20, 2004. Dr. Sechen was retained by Squire, Sanders & Dempsey LLP, counsel for defendants Hitachi, Ltd., Hitachi America, Ltd. and Renesas Technology America, Inc. (collectively “Hitachi”) to analyze certain circuits in Hitachi microprocessors that Translogic Technology, Inc. (“TTI”) accuses of infringing Patent No. 5,162,666 (“the ‘666 Patent”). Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products. This report supplements my earlier expert disclosure statement, however, it is written as a substitute for that earlier report. This revision now uses the multiplexer drawing convention used by Hitachi, which is different from the standard U.S. convention.</p> <p><u>Declaration in Opposition to Plaintiff’s Motion for Summary Judgment:</u> Declaration in opposition to plaintiff’s motion for summary judgment, April 2004. Dr. Sechen was asked to analyze certain circuits in Hitachi microprocessors that Translogic Technology accused of infringing their patent No. 5,162,666. Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products.</p> <p><u>Second Declaration in Opposition to Plaintiff’s Motion for Summary Judgment:</u> Second declaration in opposition to plaintiff’s motion for summary judgment, September 20, 2004. Dr. Sechen was asked to analyze certain circuits in Hitachi microprocessors that Translogic Technology accused of infringing their patent No. 5,162,666. Dr. Sechen was also asked to review aspects of the design and design process for these Hitachi products.</p> <p><u>Deposition:</u> Aug. 18, 2003: Dr. Sechen was deposed on all of the above-mentioned expert disclosures and declarations. Representing attorneys: Nathan Lane and David Elkins of Squire, Sanders and Dempsey, as well as Alan Loudermilk of Loudermilk Associates.</p> <p><u>Trial Testimony:</u> January 2004: Representing attorneys: Nathan Lane and David Elkins of Squire, Sanders and Dempsey, as well as Alan Loudermilk of Loudermilk Associates.</p>
Disposition:	Concluded, PTO ruled in favor of Hitachi but court ruled in favor of Translogic.

Date:	July 2003 to September 2004
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Expert Engagement:

Type of Matter:	Trade Secret Theft
Law Firm:	Keker and Van Ness (Cadence)
Case Name:	Cadence vs. Avanti
Services Provided:	Two Declarations and One Deposition for Cadence <p><u>Declaration:</u> Short declaration that verified and substantiated the findings of other Cadence experts.</p> <p><u>Declaration:</u> Dr. Sechen submitted a very long reply declaration that compared an Avanti software product to a Cadence software product, and showing that the products were not in the public domain.</p> <p><u>Deposition:</u> Deposition focused primarily on the reply declaration. Representing attorney: Michael Page.</p>
Disposition:	Concluded
Date:	July 1995 to July 1996

Graduated Ph.D. Students

1. Kai-Win Lee (Yale May 1990) "Global Routing of Row-Based Integrated Circuits".
2. Dahe Chen (Yale May 1992) "Mickey: A Graph-Based Macro-Cell Global Router".
3. Mark Chiang (Yale May 1992) "A Perturbation Approach to the Symbolic Analysis of Analog Circuits".
4. William Swartz (Yale May 1993) "Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits".
5. Ted Stanion (Yale May 1994) "Boolean Algorithms for Combinational Synthesis and Test Generation".
6. Kalapi Roy (University of Washington June 1994) "A Timing-Driven Multi-Way Partitioning System for Integrated Circuits and Multi-Chip Systems".
7. Jer-Jaw Hsu (University of Washington December 1994) "Fully Symbolic Analysis of Large Analog Integrated Circuits".
8. Wern-Jieh Sun (University of Washington December 1994) "Effective and Efficient Placement for Very Large Integrated Circuits".
9. Qicheng Yu (University of Washington March 1995) "Approximate Symbolic Analysis of Large Analog Integrated Circuits".
10. Bingzhong David Guan (University of Washington August 1996) "Automatic Layout Generation of Static CMOS Combinational Cells and Blocks".
11. Eugene Liu (University of Washington, December 1997) "Global Routing and Pin Assignment for Multi-layer Chip-level Layout".
12. Hsiao-Ping Tseng (University of Washington, December 1997) "Detailed Routing Algorithms for VLSI Circuits".

13. Gin Yee (University of Washington, June 1999) “Dynamic Logic Design and Synthesis Using Clock-Delayed Domino”.
14. Tyler Thorp (University of Washington, December 1999), “Design and Synthesis of Dynamic Circuits”.
15. Tatjana Serdar (University of Washington, December 2000), “Automatic Datapath Tile Placement and Routing”.
16. Jovanka Ciric (University of Washington, August 2001), “Boolean Matching and Level-Based Technology Mapping”.
17. Yi Han (University of Washington, December 2004), “A High-Performance CMOS Programmable Logic Core for System-on-Chip Applications”.
18. Hiran Tennakoon (University of Washington, August 2005), “Efficient and Accurate Gate Sizing With Piecewise Convex Delay Models”.
19. Miodrag Vujkovic (University of Washington, March 2006), “Efficient Fully-Automated, Refinement-Based Power-Delay Optimization Design Flow for Standard Cell Designs”.
20. Kian Hour (Alfred) Chong (University of Washington, June 2006), “Self-Calibrating Differential Output Prediction Logic”.
21. Xinyu (Sunny) Guo (University of Washington, June 2006), “A High-Throughput Divider Based on Output Prediction Logic”.
22. Sheng Sun (University of Washington, August 2006), “High Performance and Energy Efficient Adder Design”.
23. Mohammad Rahman (UT-Dallas, December 2011), “Power and Leakage Minimization for Digital ICs”.
24. Chiu-Wei Pan (UT-Dallas, August 2012), “High Speed and Power Efficient Compression of Partial Products”.
25. Zhao Wang (UT-Dallas, October 2012), “Accurate Wire Endpoint Delay Estimation”.
26. Akshay Sridharan (UT-Dallas, October 2015), “STARK: Synchronous to Asynchronous Re-design Kit”.
27. Anitha Yella (UT-Dallas, January 2016), “Power Optimization in ICs”.
28. Meisam Roshan (UT-Dallas, September 2016), “A MEMS-Assisted Dual-Resonator Temperature-to-Digital Converter”.
29. Huihua (Helen) Huang (UT-Dallas, May 2018), “A 0.1ps Resolution Coarse-Fine Time-to-Digital Converter with 2.21ps Single-Shot Precision”.
30. Jingxiang (Amelie) Tian (UT-Dallas, December 2019), “Transistor-level Programmable Fabric”.
31. Bo Hu (UT-Dallas, March 2021), “Thermal-Aware Placement and High Level Synthesis For Hardware Security”.
32. Lubaba Nahar, (UT-Dallas, July 2022), “CAD Tools for PCB Reverse Engineering and IC Interconnect”.
33. Qiongdan (Olivia) Huang, (UT-Dallas, July 2022), “Toward Accurate Timing Analysis of Transistor-Level Programmable Fabric”.
34. Xiangyu Xu, (UT-Dallas, December 2022), “Routing Methods for Transistor-level Programmable Fabrics”.
35. Vibhav Kumarswami Salimath, (UT-Dallas, December 2023), “Standard Cell Library Composition Optimization for Advanced Process Nodes”.
36. Apurva Jain, (UT-Dallas, January 2024), “Addressing Testing and Verification Challenges in a Transistor-level Programmable Fabric”.
37. Thomas Broadfoot (UT-Dallas, December 2025), “Transistor-level Programmable Fabrics for Cost-Effective IC Redaction”.

Current Ph.D. Students

1. Jinkun Feng, Ph.D. expected 06/27
2. Nazia Bushra, Ph.D. expected 06/28

Teaching Activities

<i>Yr</i>	<i>Qtr</i>	<i>Course</i>	<i>Brief Title, Credits, #students</i>	<i>Stud. Opin. Survey</i>
1992	Aut	EE538	Auto Layout, 4 credits, 20 students	4.38/4.08
1993	Win	EE356	Analog ICs, 4 credits, 55 students	3.21/3.00
1993	Spr	EE535	VLSI Design, 4 credits, 25 students	4.27/4.47
1993	Sum	EE332	Analog ICs, 5 credits, 35 students	3.57/3.48
1993	Aut	EE538	Auto Layout, 4 credits, 15 students	3.60/3.50
1993	Aut	EE332	Analog ICs, 5 credits, 40 students	3.93/3.90
1994	Win	EE433	Analog MOS ICs, 4 credits, 65 students	3.96/4.08
1994	Spr	EE476	Digital ICs, 5 credits, 55 students	3.89/3.89
1994	Aut	EE538	Auto Layout, 4 credits, 15 students	3.63/3.63
1994	Aut	EE433	Analog MOS ICs, 4 credits, 55 students	4.32/4.30
1995	Win	EE476	Digital ICs, 5 credits, 85 students	3.75/3.85
1995	Spr	EE473	Adv. Analog MOS, 5 credits, 45 students	3.53/3.59
1995	Aut	EE476	Digital ICs, 5 credits, 85 students	4.40/4.20
1996	Win	EE535	VLSI Design, 4 credits, 55 students	4.10/4.00
1996	Spr	EE538	Auto Layout, 4 credits, 15 students	4.30/4.50
1996	Aut	EE476	Digital ICs, 5 credits, 125 students	3.40/3.40
1997	Win	EE477	Custom Dig ICs, 4 credits, 45 students	4.30/4.10
1997	Win	EE541	Auto Layout, 4 credits, 20 students	4.70/4.70
1997	Spr	EE535	VLSI Design, 4 credits, 20 students	3.83/4.00
1997	Aut	EE476	Digital ICs, 5 credits, 60 students	3.88/3.89
1998	Win	EE477	Custom Dig ICs, 4 credits, 60 students	3.66/3.61
1998	Spr	EE476	Digital ICs, 5 credits, 60 students	3.39/3.50
1998	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.57/3.94
1998	Aut	EE476	Digital ICs, 5 credits, 35 students	4.15/4.50
1999	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.00/3.94
1999	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	3.79/4.13
1999	Aut	EE476	Digital ICs, 5 credits, 50 students	4.70/4.70
2000	Win	EE477	Custom Dig ICs, 4 credits, 55 students	4.53/4.27
2000	Spr	EE535	Digital VLSI Design, 4 credits, 35 stud.	4.35/4.44
2000	Aut	EE476	Digital ICs, 5 credits, 125 students	4.20/4.19
2001	Win	EE477	VLSI II, 5 credits, 75 students	4.30/4.37
2001	Win	EE525	VLSI II, 5 credits, 25 students	4.25/4.50
2001	Spr	EE526	VLSI III, 4 credits, 50 students	4.35/4.50
2001	Aut	EE476	VLSI I, 5 credits, 150 students	4.1/4.2
2002	Win	EE477	VLSI II, 5 credits, 75 students	4.1/4.1
2002	Win	EE525	VLSI II, 5 credits, 25 students	4.1/4.1
2002	Spr	EE526	VLSI III, 4 credits, 50 students	3.6/3.3

2002	Aut	EE476	VLSI I, 5 credits, 150 students	3.7/3.6
2003	Win	EE477	VLSI II, 5 credits, 55 students	3.4/3.8
2003	Win	EE525	VLSI II, 5 credits, 25 students	3.6/3.3
2003	Spr	EE526	VLSI III, 4 credits, 32 students	3.3/3.5
2003	Aut	EE476	VLSI I, 5 credits, 30 students	4.5/4.6
2004	Win	EE477	VLSI II, 5 credits, 12 students	3.2/3.7
2004	Win	EE525	VLSI II, 5 credits, 7 students	2.2/2.2
2004	Spr	EE526	VLSI III, 4 credits, 12 students	3.2/3.2
2004	Aut	EE476	VLSI I, 5 credits, 65 students	3.8/3.9
2005	Fall	EE6325	VLSI Design, 3 units, 42 students	4.4/4.6
2006	Spr	EE7325	Advanced VLSI Design, 3 units, 20 students	4.5/4.3
2006	Fall	EE6325	VLSI Design, 3 units, 66 students	4.4/4.2
2007	Spr	EE7325	Advanced VLSI Design, 3 units, 15 students	4.5/4.2
2007	Fall	EE6325	VLSI Design, 3 units, 40 students	4.8/4.6
2008	Spr	EE4325	Introduction to VLSI Design, 40 students	3.5/3.4
2008	Spr	EE7325	Advanced VLSI Design, 3 units, 19 students	4.6/4.4
2008	Sum	EE6325	VLSI Design, 3 units, 36 students	4.0/3.7
2008	Fall	EE6325	VLSI Design, 3 units, 40 students	4.1/4.1
2009	Spr	EE4325	Introduction to VLSI Design, 22 students	4.2/3.9
2009	Spr	EE7325	Advanced VLSI Design, 3 units, 37 students	3.7/3.6
2009	Sum	EE6325	VLSI Design, 3 units, 17 students	4.1/4.0
2009	Fall	EE6325	VLSI Design, 3 units, 67 students	4.3/4.0
2010	Spr	EE4325	Introduction to VLSI Design, 25 students	4.6/4.5
2010	Spr	EE7325	Advanced VLSI Design, 3 units, 35 students	4.4/4.4
2010	Sum	EE6325	VLSI Design, 3 units, 17 students	4.7/4.5
2010	Sum	EE3320	Digital Circuits, 3 units, 17 students	4.1/3.8
2010	Fall	EE6325	VLSI Design, 3 units, 77 students	4.4/4.2
2011	Spr	EE4325	Introduction to VLSI Design, 37 students	4.0/4.1
2011	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.2/4.2
2011	Sum	EE6325	VLSI Design, 3 units, 16 students	4.14
2011	Sum	EE3320	Digital Circuits, 3 units, 26 students	4.13
2011	Fall	EE6325	VLSI Design, 3 units, 91 students	4.73
2012	Spr	EE4325	Introduction to VLSI Design, 27 students	4.25
2012	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.90
2012	Sum	EE6325	VLSI Design, 3 units, 35 students	4.46
2012	Sum	EE3311	Electronic Circuits, 3 units, 22 students	3.62
2012	Fall	EE6325	VLSI Design, 3 units, 144 students	4.76
2013	Spr	EE6325	VLSI Design, 3 units, 41 students	4.85
2013	Spr	EE4325	Introduction to VLSI Design, 7 students	4.75
2013	Sum	EE7325	Advanced VLSI Design, 3 units, 67 students	4.38
2013	Sum	EE3311	Electronic Circuits, 3 units, 46 students	4.58
2013	Fall	EE6325	VLSI Design, 3 units, 129 students	4.64
2014	Spr	EE4325	Introduction to VLSI Design, 25 students	4.69
2014	Sum	EE7325	Advanced VLSI Design, 3 units, 74 students	4.53
2014	Sum	EE3311	Electronic Circuits, 3 units, 40 students	4.75
2014	Fall	EE6325	VLSI Design, 3 units, 139 students	4.79
2015	Spr	EE4325	Introduction to VLSI Design, 25 students	4.72
2015	Sum	EE7325	Advanced VLSI Design, 3 units, 49 students	4.25
2015	Sum	EE3311	Electronic Circuits, 3 units, 25 students	4.80
2015	Fall	EE6325	VLSI Design, 3 units, 142 students	4.73
2016	Spr	EE4325	Introduction to VLSI Design, 25 students	3.67

2016	Sum	EE7325	Advanced VLSI Design, 3 units, 70 students	4.77
2016	Sum	EE3311	Electronic Circuits, 3 units, 35 students	4.88
2016	Fall	EE6325	VLSI Design, 3 units, 140 students	4.79
2017	Spr	EE4325	Introduction to VLSI Design, 32 students	4.10
2017	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2017	Sum	EE3311	Electronic Circuits, 3 units, 32 students	4.50
2017	Fall	EE6325	VLSI Design, 3 units, 80 students	4.82
2018	Spr	EE4325	Introduction to VLSI Design, 32 students	4.63
2018	Sum	EE7325	Advanced VLSI Design, 3 units, 30 students	4.88
2018	Fall	EE6325	VLSI Design, 3 units, 80 students	4.88
2019	Spr	EE4325	Introduction to VLSI Design, 43 students	4.33
2019	Sum	EE3311	Electronic Circuits, 3 units, 61 students	4.23
2019	Fall	EE6325	VLSI Design, 3 units, 60 students	4.84
2020	Spr	EE4325	Introduction to VLSI Design, 33 students	4.75
2020	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.30
2020	Fall	EE6325	VLSI Design, 3 units, 43 students	4.65
2020	Fall	EE7325	Advanced VLSI Design, 3 units, 16 students	4.17
2021	Spr	EE4325	Introduction to VLSI Design, 41 students	3.40
2021	Sum	EE3311	Electronic Circuits, 3 units, 29 students	4.20
2021	Fall	EE6325	VLSI Design, 3 units, 72 students	4.75
2022	Spr	EE7325	Advanced VLSI Design, 3 units, 17 students	4.17
2022	Spr	EE4325	Introduction to VLSI Design, 46 students	4.13
2022	Sum	EE3311	Electronic Circuits, 3 units, 29 students	-----
2022	Fall	EE6325	VLSI Design, 3 units, 111 students	4.20
2023	Spr	EE4325	Introduction to VLSI Design, 48 students	4.00
2023	Fall	EE6325	VLSI Design, 3 units, 76 students	4.00
2024	Fall	EE6325	VLSI Design, 3 units, 42 students	4.75

Course Development

U. of Washington: EE 541 Automatic Layout of Integrated Circuits (first offering: Fall 1992)
U. of Washington: EE 477 Custom Digital CMOS Circuit Design (first offering: Win 1997)
U. of Washington: EE 476 Digital Integrated Circuit Design (first offering: Spr 1994)

Yale University: EE 880 Automatic Layout of Integrated Circuits.
Yale University: EE 877 Introduction to VLSI CAD Tools
Yale University: EE 878 Introduction to VLSI Synthesis
Yale University: EE 988 Analog Integrated Circuits II

Journal Publications

1. A. Fowler, S. Mohammed, M. Shihab, T. Broadfoot, P. Beerel, C. Sechen, and Y. Makris, "A TRAP for SAT: On the Imperviousness of a Transistor-Level Programmable Fabric to Satisfiability Attacks", *Transactions on Cryptographic Hardware and Embedded Systems* 2025, Issue 2.

2. A. Jain, T. Broadfoot, Y. Makris and C. Sechen, "Modeling Bidirectional Switches for Enabling Logic Equivalence Checking in a Transistor-Level Programmable Fabric," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, January 2025, Vol. 44, No. 1, pp. 385-389.
3. Roshan, C. Sechen, *et al.*, "A MEMS-Assisted Temperature Sensor with 20 μ K Resolution, Conversion Rate of 200S/s and FOM of 0.04pJK", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 185-197, January 2017.
4. Z. Wang, X. He, and C. Sechen, "A New Approach for Gate-Level Delay-Insensitive Asynchronous Logic", *Journal of Circuits, Systems & Signal Processing*, October 2014.
5. Z. Wang, C. Pan, Y. Song, and C. Sechen, "High-Throughput Digital IIR Filter Design", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 2, pp. 15-27, April 2014.
6. C. Pan, Z. Wang and C. Sechen, "High Speed and Power Efficient Compression of Partial Products and Vectors," *Journal of Algorithms and Optimization (JAO)*, Vol. 1, No. 1, pp. 39-54, October 2013.
7. Z. Wang and C. Sechen, "A New Algorithm for Accurate Wire Endpoint Delay Estimation", *Journal of Algorithms and Optimization (JAO)*, Vol. 2, No. 1, pp. 30-43, Jan. 2014.
8. M. Rahman, H. Tennakoon, and C. Sechen, "Library-Based Cell-Size Selection using Extended Logical Effort", *IEEE Trans. on Computer-Aided Design*, July 2013.
9. H. Tennakoon and C. Sechen, "Non-convex Gate Delay Modeling and Delay Optimization," *IEEE Trans. on Computer-Aided Design*, Vol. 27, No. 9, September 2008, pp. 1583-1594.
10. Don Bouldin, Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees, Carl Sechen, and Wayne Dai, "Automated Design of Digital Signal Processing ASICs," *IEEE Circuits and Devices*, vol. 20, n. 4, pp. 17-21, July 2004.
11. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *IEEE Trans. on Computer-Aided Design*, Vol. 22, No. 5, May 2003, pp. 535-544.
12. T. Thorp and C. Sechen, "Design and Synthesis of Dynamic Circuits," *IEEE Transactions on VLSI Systems*, Vol. 11, No. 1, February 2003, pp. 141-149.
13. G. Hoyer, G. Yee and C. Sechen, "Locally-Clocked Pipelines and Dynamic Logic," *IEEE Transactions on VLSI Systems*, Vol. 10, No. 1, February 2002, pp. 58-62.
14. H. P. Tseng, L. Scheffer and C. Sechen, "Timing- and Crosstalk-Driven Area Routing," *IEEE Transactions on Computer Aided Design*, vol. 20, no. 4, pp. 528-544, April 2001.
15. G. Yee and C. Sechen, "Clock-Delayed Domino for Dynamic Circuit Design," *IEEE Transactions on VLSI Systems*, Vol. 8, No. 4, August 2000, pp. 425-431.
16. L. Liu and C. Sechen, "Multi-layer Chip-level Global Routing Using an Efficient Graph-based Steiner Tree Heuristic," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
17. L. Liu and C. Sechen, "Multi-layer Pin Assignment for Macro Cell Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999.
18. H. P. Tseng and C. Sechen, "A Gridless Multi-Layer Router for Standard Cell Circuits using CTM Cells," *IEEE Transactions on Computer Aided Design*, Vol. 18, No. 10, October 1999.
19. W. Sun and C. Sechen, "A Parallel Standard Cell Placement Algorithm," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 11, November 1997, pp. 1342-1357.
20. Q. Yu and C. Sechen, "Efficient Approximation of Symbolic Network Functions Using Matroid Intersection Algorithms," *IEEE Transactions on Computer Aided Design*, vol. 16, no. 10, October 1997, pp. 1073-1081.

21. Q. Yu and C. Sechen, "Generation of Color-Constrained Spanning Trees with Application in Symbolic Analysis," *Int. Journal of Circuit Theory and Applications*, Vol. 24, No. 5, pp. 597-603, 1996.
22. Q. Yu and C. Sechen, "A Unified Approach to the Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 8, pp. 656-669, August 1996.
23. K. Roy and C. Sechen, "A Timing-Driven Partitioning System for Multiple FPGAs," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 309-328, 1996.
24. K. Roy, D. Guan and C. Sechen, "A Sea-of-Gates Style FPGA Placement Algorithm," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 293-307, 1996.
25. T. Stanion, D. Bhattacharya, and C. Sechen, "An Efficient Method for Generating Exhaustive Test Sets," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 12, December 1995.
26. W. Sun and C. Sechen, "Efficient and Effective Placement for Very Large Circuits," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 3, pp. 349-359, March 1995.
27. J. J. Hsu and C. Sechen, "DC Small Signal Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I*, Vol. 41, No. 12, pp. 817-828, December 1994.
28. T. Stanion and C. Sechen, "Boolean Division and Factorization Using Binary Decision Diagrams," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, September 1994, pp. 1179-1184.
29. C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro Cell Integrated Circuits Using Simulated Annealing," *Int. J. Computer-Aided VLSI Design*, vol. 2, no. 2, 1990, pp. 127-158.
30. C. Sechen, D. Braun, and A. Sangiovanni-Vincentelli, "ThunderBird: A Complete Standard Cell Layout Package," *IEEE J. of Solid State Circuits*, vol. 23, n. 2, pp. 410- 420, April 1988.
31. C. Sechen and A. Sangiovanni-Vincentelli, "The TimberWolf Placement and Routing Package," *IEEE J. of Solid State Circuits*, vol. 20, n. 2, April 1985, pp. 510-522.
32. C. Sechen, "An Improved Lock Layer Transistor," *Solid State Electronics*, Vol. 21, No. 6, June 1978, pp. 911-913.
33. S. Senturia and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Transactions on Electron Devices*, vol.24, no.9, p.1207, September 1977.
34. S. Senturia, C. Sechen, and J. Wishneusky, "The Charge-Flow Transistor: A New MOS Device," *Applied Physics Letters*, Vol. 30, No. 2, Jan. 1977, p. 106-108.

Fully Refereed Conference Proceedings

1. A. Fowler, C. Sechen and Y. Makris, "An SMT-Based Method for Identifying State-Holding Elements in Extracted Netlists", Submitted to the International Test Conference (ITC), Sept. 21-26, 2025, San Diego, CA.
2. S. Chaitaligajanan, A. Fowler, B. Schaefer, Y. Makris, C. Sechen, M. Zaman, and R. Narumi, "Trusted, Assured and Cyber-secure Microelectronics", Proc. GOMACTech-25 (Government Microcircuit Applications & Critical Technology Conference), March 17-20, 2025, Pasadena, CA.

3. T. Broadfoot, Y. Makris, and C. Sechen, "TRAPv4: A Transistor-Level Programmable Fabric for "Blacked-Out" ASIC Redaction", *Proc. GOMACTech-25 (Government Microcircuit Applications & Critical Technology Conference)*, March 17-20, 2025, Pasadena, CA.
4. A. Jain, T. Broadfoot, Y. Makris, and C. Sechen, "Testing a Transistor-Level Programmable Fabric: Challenges and Solutions", *Proc. IEEE VLSI Test Symposium (VTS)*, Tempe, AZ, April 22-24, 2024.
5. A. Jain, T. Broadfoot, Y. Makris, and C. Sechen, "Quo Vadis Signal? Automated Directionality Extraction for Post-Programming Verification of a Transistor-Level Programmable Fabric", *Proc. Design Automation and Test in Europe (DATE) Conference*, Antwerp, Belgium, April 17-19, 2023.
6. V. Salimath and C. Sechen, "Essential Standard Cell Library Composition", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
7. L. Nahar, J. Rajendran, Y. Makris and C. Sechen, "MTBoM: Metal Trace to Bill of Materials Generation for PCB Reverse Engineering", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
8. Q. Huang, J. Tian, T. Broadfoot, X. Xu, B. Hu, M. Shihab, A. Jain, V. Salimath, Y. Makris and C. Sechen", *Proc. 15th IEEE Dallas Circuits and Systems Conference (DCAS 2022)*, June 17-19, 2022, Dallas, TX.
9. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.
10. V. Salimath and C. Sechen, "Optimal Standard Cell Library Composition for 7nm", *Proc. IEEE International Symposium on Circuits & Systems (ISCAS)*, May 17-20, 2020, Seville, Spain.
11. M. Shihab, B. Ramanidharan, S. Tellakula, G. Reddy, J. Tian, C. Sechen, and Y. Makris, "ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric", *Proc. 8th IEEE VLSI Test Symposium (VTS'20)*, April 5-8, 2020, San Diego, CA.
12. M. Shihab, J. Tian, G. Reddy, B. Hu, W. Swartz Jr., B. Schaefer, C. Sechen and Y. Makris, "A Transistor-Level Fabric for Design Obfuscation", *Proc. Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, March 16-19, 2020, San Diego, CA.
13. B. Hu, M. Shihab, Y. Makris, B. Schaefer and C. Sechen, "An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs", *Proc. Design Automation in Europe Conference (DATE)*, March 9-13, 2020, Grenoble, France.
14. B. Hu, M. Shihab, Y. Makris, B. Schaefer and C. Sechen, "Extending the Lifetime of Coarse-grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage", *2019 International Conference on Field-Programmable Technology (FPT'19)*, December 9-13, 2019 Tianjin, China.
15. S. Reda, M. Saligane, S. S. Sapatnekar, C. Sechen, *et al.*, "Toward an Open-Source Digital Flow: First Learnings from the OpenROAD Project", *Proc. ACM/IEEE Design Automation Conference (DAC)*, June 4-6, 2019, Las Vegas, NV.
16. B. Hu, J. Tian, M. Shihab, G. Reddy, W. Swartz, Y. Makris, B. Schaefer, and C. Sechen, "Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA", *Proc. Great Lakes Symposium on VLSI (GLSVLSI)*, Washington, D.C., USA, May 9-11, 2019.
17. S. Sapatnekar, L. Saul, C. Sechen, *et al.*, "OpenROAD: Toward a Self-Driving, Open-Source Digital Layout Implementation Tool Chain", *Proc. Government Microcircuit Applications*

- and Critical Technology Conference (GOMACTech), March 25-28, 2019, Albuquerque, NM, pp. 1105-1110.
18. M. Shihab, G. Reddy, J. Tian, B. Hu, W. Swartz, B. Carrion Schaefer, C. Sechen, Y. Makris, "Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming," *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 25-29, 2019, Florence, Italy.
 19. A. Yella, S. Gunturi and C. Sechen, "Are Standalone Gate Size and VT Optimization Tools Useful?", *Proc. IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE), Devices, Circuits, and Systems Track*, Windsor, ON, Canada, April 30 - May 3, 2017.
 20. T. Broadfoot, C. Sechen and J. Rajendran, "On Designing Optimal Camouflaged Layouts", *Proc. IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, May 1-4, 2017, McLean, VA.
 21. A. Yella and C. Sechen, "Improved Lagrangian Relaxation-based Gate Size and VT Assignment for Very Large Circuits, *Proc. IEEE PhD Research In Microelectronics and Electronics Conference Latin America (PRIME)*, Bariloche, Argentina, February 20-23, 2017. **BEST PAPER AWARD**
 22. J. Tian, G. Reddy, J. Wang, W. Swartz, Y. Makris and C Sechen, "A Field Programmable Transistor Array Featuring Single-Cycle Partial/Full Dynamic Reconfiguration", *Proc. of Design Automation and Test in Europe (DATE) Conference*, March 27-31, 2017, Lausanne, Switzerland. **NOMINATED FOR BEST PAPER AWARD**
 23. M. Roshan, C. Sechen, *et al.*, "Dual-MEMS Resonator Temperature-to-Digital Converter with 39 μ K Resolution and a FoM of 0.11pJK²", *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2016, San Francisco, CA.
 24. M. Jain and C. Sechen, "Chip Design: Matrix Multiplier Based on Systolic Architecture", *IEEE Computer Society 6th International Conference on Computing, Communications and Networking Technologies (ICCCNT)*, July 13-15, 2015, Dallas, TX.
 25. Z. Wang, X. He and C. Sechen, "TonyChopper: A Desynchronization Package", *Proc. Int. Conf. on Computer Aided Design (ICCAD)*, Nov. 2-6, 2014, San Jose, CA. (20% accepted)
 26. H. Huang and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS", *2014 Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.
 27. A. Sridharan and C. Sechen, "Minimum Energy Operation using Robust Asynchronous Logic with Sleep Transistors", *Proc. Dallas Circuits and Systems Conference (DCAS)*, Oct 12-13, 2014, Dallas, TX.
 28. Yashaswini Prathivadi, Carl Sechen, and Roozbeh Jafari, "A Swarm of Wearable Sensors at the Edge of the Cloud for Robust Activity Recognition", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13)*, Sept. 29, 2013, Montreal, Canada.
 29. Mohammad-Mahdi Bidmeshki, Carl Sechen, and Roozbeh Jafari, "Low Power Programmable Architecture for Periodic Activity Monitoring", *Proc. SRC Techcon*, 2013, Austin, TX.
 30. Thomas Broadfoot, Jingxiang Tian, HeeEun Choi, Mohammad-Mahdi Bidmeshki, Roozbeh Jafari, and Carl Sechen, "Platform Design for Swarm Wearable Computing", *Proc. First International Workshop on the Swarm at the Edge of the Cloud (SEC'13)*, Sept. 29, 2013, Montreal, Canada.
 31. A. Sridharan, C. Sechen, and R. Jafari, "Low-Voltage Low-Overhead Asynchronous Logic", *Int. Symp. on Low Power Electronics and Design (ISLPED)*, Beijing, China, Sept. 4-6, 2013. (25% accepted)
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33. Hee-Eun Choi, C. Sechen and R. Jafari, "24kb, 11T Subthreshold SRAM for Ultra-Low Power Medical and Health Monitoring Embedded Systems," *IEEE Texas Workshop on Integrated System Exploration (TexasWISE)*, 8 March 2013, Round Top, Texas.
34. M. Rahman, and C. Sechen, "Post-Synthesis Leakage Power Minimization", *Design Automation and Test in Europe (DATE) Conference*, March 12-16, 2012, Dresden, Germany.
35. M. Rahman, H. Tennakoon, R. Afonso and C. Sechen, "Power Reduction via Separate Synthesis and Physical Libraries", *Proc. Design Automation Conference (DAC)*, June 2011, San Diego, CA.
36. C. Pan and C. Sechen, "Power Efficient Partial Product Compression", *Proc. Great Lakes Symposium on VLSI*, Lausanne, May 2-4, 2011, Switzerland.
37. M. Rahman, H. Tennakoon, and C. Sechen, "Power Reduction via Near-Optimal Library-Based Cell-Size Selection", *Design Automation and Test in Europe (DATE) Conference*, March 14-18, 2011, Grenoble, France.
38. M. Rahman, H. Tennakoon, R. Afonso, and C. Sechen, October 17-18, "Design Automation Tools and Libraries for Low Power Digital Design", *Proc. IEEE Dallas Circuits and Systems Conference (DCAS)*, Oct. 17-18, 2010, Richardson, TX.
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40. H. Huang and C. Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.
41. E. Kiefer, W. Swartz, and C. Sechen, "Low Skew Automated Clock Tree Generation", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, Oct. 26-27, 2009, Austin, TX.
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46. E. Kiefer, W. Swartz, and C. Sechen, "Low Power Automated Clock Tree Generation", *Proc. IEEE Dallas Circuits and Systems Society Workshop*, Oct. 4-5, 2009, Dallas, TX.
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48. S. Sun and C. Sechen, "Post-Layout Comparison of High Performance 64b Static Adders in Energy-Delay Space," *Proc. IEEE Int. Conf. on Computer Design (ICCD)*, Lake Tahoe, CA, October 2007.
49. M. Rahman, H. Tennakoon, and C. Sechen, "Optimal Area-versus-Delay Circuit Sizing Using Extended Logical Effort", *Proc. Austin Conf. on Integrated Circuits and Systems (ACISC)*, May 14-15, 2007, Austin, TX.
50. K. H. Chong, L. McMurchie and C. Sechen, "A 64b Adder Using Self-calibrating Differential Output Prediction Logic," *Proc. Int. Solid-State Circuits Conference (ISSCC)*, February 2006, San Francisco, CA.

51. J. Zhang, M. Vujkovic, D. Wadkins, and C. Sechen, "Post-Layout Energy-Delay Analysis of Parallel Multipliers," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 2006, Greece.
52. M. Vujkovic, D. Wadkins and C. Sechen, "Efficient Post-Layout Power-Delay Curve Generation," *Prof. 15th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 21-23 September 2005, Leuven, Belgium. In: *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation*, Series: Lecture Notes in Computer Science, Vol. 3728 Paliouras, Vassilis; Vounckx, Johan; Verkest, Diederik (Eds.) 2005, XV, 753 p., Softcover ISBN: 3-540-29013-3.
53. X. Guo and C. Sechen, "High Throughput Divider Using Output Prediction Logic," *Proc. PRIME (Ph.D. Research in Microelectronics) Conf.*, July 25-28, 2005, Lausanne, Switzerland.
54. X. Guo and C. Sechen, "A High Throughput Divider Implementation," *Proc. Custom Integrated Circuits Conference (CICC)*, 18-21 September 2005, San Jose, CA.
55. H. Tennakoon and C. Sechen, "Efficient and Accurate Gate Sizing with Piecewise Convex Delay Models," *Proc. Design Automation Conference (DAC)*, Anaheim, CA, June 13-17, 2005.
56. S. Sun, Y. Han, X. Guo, K. Chong, L. McMurchie and C. Sechen, "409ps 4.7 FO4 64b Adder Based on Output Prediction Logic in 0.18um CMOS," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.
57. X. Guo and C. Sechen, "High Speed Redundant Adder and Divider in Output Prediction Logic," *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, May 11-12, 2005, Tampa, FL.
58. J. Kim, L. McMurchie and C. Sechen, "Mitigation of Single- and Multiple-Cycle-Duration SETs using Double-Mode Redundancy (DMR) in Time", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.
59. J. Lan, D. Lam, L. McMurchie, and C. Sechen, "SEE-Hardened-by-Design Area-Efficient SRAMs", *Proc. IEEE Aerospace Conference*, Big Sky, Montana, Mar. 5-12, 2005.
60. Y. Han, L. McMurchie and C. Sechen, "A High Performance CMOS Programmable Logic Core," *Proc. Custom Integrated Circuits Conference (CICC)*, October 3-6, 2004, Orlando, FL.
61. V. Tang, J. Lan, D. Lam, L. McMurchie, and C. Sechen, "High-Performance SEE-Hardened Programmable DSP Array," *Proc. 2004 Military and Aerospace Programmable Logic Device (MAPLD) Conference*, Washington, DC, Sept. 8-10, 2004.
62. D. Lam, J. Lan, L. McMurchie, and C. Sechen, "Radiation-Hardened-by-Design Area-Efficient SRAMs," *Proc. Hardness by Design (HBD) Workshop*, Albuquerque, NM, August 24-25, 2004.
63. M. Vujkovic, D. Wadkins, B. Swartz and C. Sechen, "Efficient Timing Closure Without Timing Driven Placement and Routing," *Proc. Design Automation Conference (DAC)*, San Diego, CA, June 7-11, 2004.
64. Y. Lam, L. McMurchie, and C. Sechen, "SEU Hardening of Peripheral Circuitry in Self-Scrubbing SRAMs," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.
65. V. Tang, J. Lan, D. Lam, L. McMurchie and C. Sechen, "Low-Overhead SEE-Hardened Programmable DSP Array," *Proc. Single Event Effects Symposium*, Manhattan Beach, CA, April 27-29, 2004.
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67. Y. Han and C. Sechen, "A Novel High Speed FPGA Architecture, *Proc. SRC Techcon*, Dallas, TX, Aug. 25 – 28, 2003.

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69. S. Kio, K. Chong, and C. Sechen, "A Low Power Delayed-Clock Generation and Distribution System," *Proc. Int. Symp. on Circuits and Systems (ISCAS)*, May 25-28, 2003, Bangkok, Thailand.
70. Warren Snapp, Paul Haug, Dave Sunderland, Roger Brees Don Bouldin, Wayne Dai, and Carl Sechen, "MSP Liberator ASIC Design Flow Produces Full Custom Performance Required for Next Generation Military Electronics," *Proc. Government Microelectronics and Applications Conference (GOMAC)*, April 1-3, 2003, Tampa, FL.
71. H. Tennakoon and C. Sechen, "Gate Sizing Using Lagrangian Relaxation Combined with a Fast Gradient-Based Preprocessing Step," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.
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73. L. McMurchie and C. Sechen, "WTA – Waveform-Based Timing Analysis for Deep Submicron Circuits," *Proc. Int. Conf. on Computer-Aided Design (ICCAD)*, Nov. 2002, San Jose, CA.
74. M. Vujkovic and C. Sechen, "Optimized Power-Delay Curve Generation for Standard Cell ICs," *Proc. Int. Workshop on Logic Synthesis (IWLS)*, June 4-7, 2002, New Orleans, LA.
75. Yi Han, Larry McMurchie, Jovanka Ciric, and Carl Sechen, "Giga hertz-Speed FPGA Architecture based on Output Prediction Logic", *Tenth ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2002)*.
76. J. Ciric and C. Sechen, "Efficient Canonical Form for Boolean Matching of Complex Functions in Large Libraries," *Proc. of IEEE Int. Conf. on Comp. Aided Design (ICCAD)*, San Jose, CA, November 5-7, 2001.
77. R. Rutenbar, M. Baron, T. Daniel, R. Jayaraman, Z. Or-Bach, J. Rose and C. Sechen, "When Will FPGAs Kill ASICs?" *Proc. Design Automation Conference (DAC)*, June 18-22, 2001, Las Vegas, NV.
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79. S. Kio, L. McMurchie, and C. Sechen, "Application of Output Prediction Logic to Differential CMOS," *Proc. of IEEE Computer Society Annual Workshop on VLSI*, Orlando, FL, April 19-20, 2001.
80. S. Sun, L. McMurchie, and C. Sechen, "A High-Performance 64-bit Adder Implemented in Output Prediction Logic," *Proc. 19th Conference on Advanced Research in VLSI*, March 14-16, 2001, Salt Lake City, UT.
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Patents

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Research Funding

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- “Cost-Effective IC Redaction through a CMOS/MRAM Transistor-Level Programmable Fabric”, PI: C. Sechen, Co-PIs: J. Friedman, Y. Makris. NSF CHEST I/UCRC. June 1, 2023 – May 31, 2024. \$100,000.
- NSF Proposal: SaTC: TTP: Medium: Hardware Intellectual Property Protection through Hybrid ASIC/TRAP Integrated Circuit Design, 8/15/22-7/31/26, \$900,000 (PI: Y. Makris, co-PI: C. Sechen).
- “CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)”, Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, \$150,000. NSF CHEST I/UCRC. March 1, 2022 – February 28, 2023.
- “CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP)”, Dr. Yiorgos Makris, Dr. Carl Sechen, Dr. Benjamin Carrion Schaefer, Dr. William Swartz Jr., ECE Department, UT Dallas, 800 W. Campbell Rd., ECSN 4.914, Richardson, TX 75080, \$150,000. NSF CHEST I/UCRC. March 1, 2021 – February 28, 2022.
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- “Optimal Gate Size and Vt Selector, and Innovative Approach to Path-Based Timing Analysis”, PI: Carl Sechen, Texas Instruments, Jan. – Dec., 2012, \$50,000. Current status: completed.
- “Optimal Gate Size and Vt Selection”, Texas Instruments, Wireless Division, Jan. – Dec., 2011, \$50,000, PI: Carl Sechen.
- “Power Minimization Research”, Texas Instruments, ASIC Division, Jan. – Dec., 2011, \$50,000, PI: Carl Sechen.
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- “Low Power HD Video Decoder Research”, Texas Instruments, Wireless Division, Jan. – Dec., 2010, \$50,000, PI: Carl Sechen.
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- “Power Optimization and Circuit Hardening”, MARCO Focus Center Research Program (C2S2), \$155,000, September 2005 – August 2008.
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- “Power Minimization and Yield Optimization in Digital IC’s”, Carl Sechen, Semiconductor Research Corporation TxACE, \$150,000, August 2007 – July 2010.
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- “Low Power HD Video Decoder Research”, Carl Sechen, Texas Instruments, Wireless Division, \$45,000, Jan. – Dec., 2007.
- “Three-Transistor Memory Cell Research”, Carl Sechen, Texas Instruments, \$35,000, Jan. – Dec., 2007.
- “Power Minimization Research”, Carl Sechen, Texas Instruments, ASIC Division, \$37,000, Jan. – Dec., 2007.
- “Low Power HD Video Decoder Research”, Carl Sechen, Texas Instruments, Wireless Division, \$30,000, Sept. – Dec., 2006.
- “DRAM-Density SRAM”, Carl Sechen, Honeywell, \$105,000, January 2006 – April 2007.
- “RADHARD by Design,” DARPA/Boeing, Phase I, \$45,000 (co-PI, my portion), November 2004 – August 2005).
- “CLASS: Clockless Logic, Analysis, Synthesis, and Systems,” DARPA/Boeing, Phase II/III, \$709,000 (co-PI, my portion), (Sept. 2004 – August 2006).
- “MSP Phase 2: Digital IC Optimization Techniques,” DARPA/Boeing, \$285,000 (co-PI, my portion), (September 2004 – August 2006).
- “Power Optimization and Circuit Hardening,” MARCO FCRP C2S2 Center, \$100,000, PI (Oct. 04 – Sep. 05).
- “High Speed and Low Power Digital IC Design,” NSF ITR, \$350,000 (my portion) co-PI, (Sept. 00 – Aug. 05).
- “Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits,” Air Force Research Lab, \$110,000, PI (Sep 04 – Aug 05).
- “High Speed & Low Power Digital Circuit Synthesis and Design,” MARCO FCRP C2S2 Center, \$100,000, PI (Oct. 03 – Sep. 04), full indirect.
- “CLASS: Clockless Logic, Analysis, Synthesis, and Systems,” DARPA/Boeing, Phase I, \$135,000 (co-PI, my portion), (Oct. 2003 – May 2004).
- “Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits,” Air Force Research Lab, \$105,000, PI (Sep 03 – Aug 04), full indirect.
- “Low Power Digital IC Design,” NSF Center for the Design of Analog and Digital ICs (CDADIC), \$55,000, PI (Sep 03 – Aug 04), no indirect.
- “Reconfigurable RF, Analog and Digital Array for Radiation-Hardened Wireless Communication Circuits,” DARPA/SPAWAR, \$150,000, PI (April 03 – May 04), full indirect.
- “Development of Pulse-Based Logic,” DARPA, \$100,000, PI (March 03 – May 04), full indirect.

- “High Performance and Power Efficient Digital IC Optimization Techniques,” MSP Phase 1: Boeing/DARPA, \$400,000, PI (April 02 – August 03), full indirect.
- Unrestricted grant, Intel Corporation, \$60,000, PI (May 03 – April 04).
- “High Performance Digital IC Design,” MARCO/DARPA C2S2 Center, \$170,000, PI (Jan. 01 – Aug. 03), full indirect.
- “Ultra High Performance Digital Circuit Design and Synthesis,” National Science Foundation, \$180,000, PI, (Sep 02 – Aug 05).
- “Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits,” Air Force Research Lab, \$95,000, PI (Sep 02 – Aug 03), full indirect.
- “PLL Design, Clock Generation and High-Speed/Low-Power DSP-block Design,” NSF Center for the Design of Analog and Digital ICs (CDADIC), \$55,000, PI (Sep 02 – Aug 03), no indirect.
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- “High Performance Digital IC Design,” Semiconductor Research Corporation (SRC), June 1, 2000 – May 31, 2003, \$525,000 (full indirect).
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- Unrestricted grant, Intel Corporation, \$60,000, PI (Mar 01 – Feb 02).
- Unrestricted grant, Sun Microsystems, \$30,000, PI (Feb 00 – Mar 01).
- Unrestricted grant, Compaq Computer Corp., \$25,000, PI (Oct. 99 – Sep. 00).
- Unrestricted grant, Cadabra, Inc., \$20,000, PI (Feb. 00 – Mar 01).
- “Ultra High Speed Digital Circuit Synthesis and Layout NSF Center for the Design of Analog and Digital ICs (CDADIC), \$55,000 (no indirect), PI (Sep. 99-Aug. 00).
- “Ultra High Speed Digital Circuit Synthesis and Layout”, National Science Foundation, \$255,000 (full indirect), PI (Sep 99 – Aug 02).
- “Ultra High Speed Digital Circuit Synthesis and Layout”, Semiconductor Research Corporation, \$154,000 (full indirect), PI (Mar 99-Mar 00).
- “Ultra High Speed Digital Circuit Synthesis and Layout”, , Semiconductor Research Corporation, \$154,000 (full indirect), PI (Mar 99-Mar 00).
- “Synthesis of Ultra High Speed Random Logic Blocks”, Semiconductor Research Corporation, \$132,000, PI (Mar 98-Feb 99).

- “Ultra High Speed Digital Circuit Synthesis and Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$65,000, PI (Sep. 98-Aug. 99).
- “Radiation-hard High Speed Digital Circuit Synthesis”, Boeing, \$35,000, PI (Sep. 98-Aug. 99).
- “Datapath Cell Layout”, Compaq/Digital Equipment, \$25,000, PI (Sep. 98 – Aug. 99).
- Unrestricted grant, Sun Microsystems, \$8,000, PI (June 99 – May 00).
- Unrestricted grant, Compaq Computer Corp., \$25,000, PI (Oct. 98 – Sep. 99).
- Unrestricted grant, Sun Microsystems, \$30,000, PI (Jan. 99 – Dec. 99).
- Unrestricted grant, TimberWolf Systems, Inc., \$20,000, PI (Apr. 98 – Mar. 99).
- Unrestricted grant, Sun Microsystems, Inc., \$8,000, PI (June 98 – May 99).
- Various industrial gifts, \$65,000, PI (Sep 97-Aug 98).
- “High Speed Digital Circuit Design”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$50,000, PI (Sep. 97-Aug. 98).
- “Automatic Layout Research”, Semiconductor Research Corporation, \$132,000, PI (Mar 97-Feb 98).
- Various industrial gifts, \$112,000, PI (Sep 96-Aug 97).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$50,000, PI (Sep. 96-Aug. 97).
- “Symbolic Analysis of Large Analog Circuits”, National Science Foundation, \$90,000, PI (Sep 94-Aug 97).
- “Automatic Layout Research”, Semiconductor Research Corporation, \$132,000, PI (Mar 96-Feb 97).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$45,000, PI (Sep. 95-Aug. 96).
- Various industrial gifts, \$117,000, PI (Sep 95-Aug 96).
- “Automatic Layout Research”, Semiconductor Research Corporation, \$132,000, PI (Mar 95-Feb 96).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$45,000, PI (Sep. 94-Aug. 95).
- Various industrial gifts, \$208,000, PI (Sep 94-Aug 95).

- “Automatic Layout Research”, Semiconductor Research Corporation, \$144,000, PI (Mar 94-Feb 95).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$45,000, PI (Sep. 93-Aug. 94).
- Various industrial gifts, \$343,000, PI (Sep 93-Aug 94).
- “Automatic Layout Research”, Semiconductor Research Corporation, \$140,000, PI (Mar 93-Feb 94).
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), \$45,000, PI (Sep. 92-Aug. 93).
- Various industrial gifts, \$312,000, PI (Sep 92-Aug 93).
- “Automatic Layout Research”, Semiconductor Research Corporation, \$140,000, PI (Mar 92-Feb 93).
- Various industrial gifts, \$306,000, PI (Sep 91-Aug 92).
- Yale University, Various Industrial Gifts, \$1.65 million, PI (1986-1992).

Conference Service Activities

- Session Chairman for the Design Automation and Test in Europe Conference, 2012-2014.
- Session Chairman for the IEEE Design Automation Conference, 1987, 1990, 1991, 1997.
- Session Chairman for the International Symposium on Physical Design, 1997, 1998.
- Session Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1988, 89, 90, 91, 92.
- Session Chairman for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989, 1990, 1991, 1992, 1993, 1998.
- Elected Chairman for the Placement and Floorplanning sub-committee for the 2004 Design Automation Conference (DAC), 2004.
- Elected to the Placement and Floorplanning sub-committee for the 2003 Design Automation Conference (DAC), 2003.
- Elected Program Chair for the 2000 ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU).
- Elected chairman of the placement and floorplanning committee of the 2001 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 2000 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and routing committee of the 1999 Int. Conf. On Computer Aided Design (ICCAD).
- Elected chairman of the placement and floorplanning committee of the 1998 Int. Conf. On Computer Aided Design (ICCAD).
- Elected Program Chairman of the ACM Physical Design Workshop, Lake Arrowhead, CA, April 1993.
- Elected Chairman of the 1992 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- Elected Chairman of the 1990 Int. Workshop on Layout Synthesis, May, MCNC, Research Triangle Park, NC.
- CAD Track Chairman for the IEEE Int. Conf. on Computer Design (ICCD), 1991.

Service as a Referee

- Technical Program Committee for the Design Automation Conference, 2014, 2015.
- Technical Program Committee for the Design Automation and Test in Europe Conference, 2012-2014.
- Technical Program Committee for the IEEE Int. Symposium on VLSI Design, 2010-2011.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Aided Design (ICCAD), 1989-93, 98.
- Technical Program Committee for the IEEE Int. Conf. on Comp. Design (ICCD), 1987-97.
- Technical Program Committee for the European Design and Test Conference (EDTC), 1995, 96, 97, 98.
- Technical Program Committee for the Design Automation and Test in Europe (DATE) Conference, 1998, 99, 00, 01, 02, 03.
- Technical Program Committee for ACM International Physical Design Workshop, 1996.
- Technical Program committee for the International Symposium on Physical Design, 1997, 98.
- Technical Program Committee for the International Workshop on Layout Synthesis, 1988, 90, 92.
- IEEE/ACM Design Automation Conference, 1986-1998.
- National Science Foundation, 1986-present.

- IEEE Transactions on Computer Aided Design, 1986-present.
- IEEE Transactions on VLSI Systems, 1992-present.
- ACM Transactions on Design Automation of Electronic Systems, 1995-present.

University Service

UTD

Academic Affairs Committee 2022-2024

Director of ECS Tech Support Services, June 2012 – February 2014

Information Technology Planning and Policy Committee, Sept. 1, 2016 – August 31, 2019

UW

Faculty Council on Research, 1994-1997

Faculty Senate, 2002-2004

Department Service

UTD

Chair of the TA Assignment Committee, Spring 2024-2025, and ongoing

Chair of Adhoc Committee for a possible promotion to Associate Professor with Tenure (Prof. Kanad Basu), 2024.

Chair of the Computer Resources Committee, ECE Dept., 2007-2021

Advisory Committee to TxACE (SRC Texas Analog Center of Excellence) 2008-2009

Chair of the Analog Search Sub-Committee, EE Dept., 2007-2008

Faculty Search Committee (computer engineering) 2010-11

Teaching Assistant (TA) Selection Committee, 2021-23

UW

Faculty Search Committee, 2005-2006

Group Chair, VLSI and Digital Systems Group, 1997-2005

Faculty Search Committee, 98-99.

Graduate Studies and Research Committee, 1992-93, 96-97, 97-98.

Group Chair, Electronics, 94-95.

Graduate Admissions Committee, Electrical Engineering Dept., 1992-93.

Qualifying Examination Subcommittee, 1992-93.

Computer Resources Committee, 1992-93.

Outside University Service

Selected by the NSF to serve as a panelist for (invited) full proposals submitted to the CISE Expeditions in Computing (Expeditions) program, NSF 08-568, April 6-7, 2010.

Selected by the NSF to serve on the 2008 proposal review panel (April 14-15, 2008) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2009 funding.

Selected by the NSF to serve on the 2007 proposal review panel (January 8-9, 2007) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2008 funding.

Selected by the NSF to serve on the 2005 proposal review panel (October 20-21, 2005) to review a number of proposals that were submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2006 funding.

Selected by the NSF to serve on the 2004 proposal review panel (May 5-6, 2004) to review a number of proposals that have been submitted to the Computing Processes and Artifacts (CPA) cluster of the Computer, Information Sciences & Engineering (CISE) directorate of the National Science Foundation for Fiscal Year 2004 funding.

Selected by the NSF to serve on the 2002 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Selected by the NSF to serve on the 1999 CAREER proposal evaluation panel for the Design Automation Program (Division of Communications-Computer Research or C-CR) of the National Science Foundation.

Co-Director of the NSF Center for the Design of Analog and Digital ICs (CDADIC), 1997-2005; this center provides about \$450,000 annually to the University of Washington.

Professional Society Memberships

Eta Kappa Nu
Tau Beta Pi
Sigma Xi
IEEE Fellow
ACM