UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

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Case IPR2025-01456
Patent 10,140,028

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**PETITIONER'S UPDATED LIST OF EXHIBITS**

## LIST OF EXHIBITS

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| EX1001 | U.S. Patent No. 10,140,028 to Gillingham ("the '028 Patent") |
| EX1002 | Excerpts from the Prosecution History of the '028 Patent ("the Prosecution History") |
| EX1003 | Expert Declaration and Curriculum Vitae of Carl Sechen, Ph.D. |
| EX1004 | U.S. Publication No. 2006/0023499 ("Ryu") |
| EX1005 | U.S. Publication No. 2005/0141666 ("Cole") |
| EX1006 | U.S. Patent No. 5,864,506 ("Arcoleo") |
| EX1007 | U.S. Patent No. 6,337,832 ("Ooishi") |
| EX1008 | U.S. Patent No. 5,917,759 ("Akashi") |
| EX1009 | U.S. Publication No. 2004/0148482 ("Grundy") |
| EX1010 | U.S. Patent No. 5,206,831 ("Wakamatsu") |
| EX1011 | U.S. Patent No. 6,304,497 ("Roohparvar") |
| EX1012 | Wu, *eNVy: A Non-Volatile, Main Memory Storage System* (1994), *available at* https://dl.acm.org/doi/pdf/10.1145/381792.195506 |
| EX1013 | U.S. Patent No. 6,026,465 ("Mills") |
| EX1014 | U.S. Patent No. 4,970,694 ("Tanaka") |
| EX1015 | Maksimovic, *Clocked CMOS Adiabatic Logic with Integrated Single-Phase Power-Clock Supply* (2000), *available at* https://www.acsel-lab.com/Publications/Papers/102-IEEE-TVLSI-CAL.pdf |

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| EX1016 | U.S. Patent No. 6,943,604 ("Minzoni") |
| EX1017 | U.S. Patent No. 6,972,993 ("Conley") |
| EX1018 | Lee, *Low-Energy Heterogeneous Non-Volatile Memory Systems for Mobile Systems* (2005), *available at* https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e1f287fa9e15bd88cb14574c4802fd7a6017c449 |
| EX1019 | Crisp, *Direct Rambus Technology: The New Main Memory Standard* (1997), *available at* https://www.ardent-tool.com/CPU/docs/AMD/anatomy/misc/articles/m6crisp.pdf |
| EX1020 | U.S. Patent No. 7,486,104 ("Oh") |
| EX1021 | U.S. Patent No. 6,937,513 ("Desai") |
| EX1022 | U.S. Patent No. 7,177,190 ("Lee") |
| EX1023 | Yeh, *Flash Memory Built-In Self-Test Using March-Like Algorithms* (2002), *available at* https://www.researchgate.net/profile/Jen-Chieh-Yeh-2/publication/3943092_Flash_memory_built-in_self-test_using_March-like_algorithms/links/0c9605187311b4193a000000/Flash-memory-built-in-self-test-using-March-like-algorithms.pdf |
| EX1024 | U.S. Patent No. 7,804,176 ("Hanawa") |
| EX1025 | U.S. Patent No. 8,085,574 ("Kang") |
| EX1026 | U.S. Publication No. 2008/0016306 ("Min") |
| EX1027 | Palanisamy, *Interfacing Spartan—3 Devices with 166 MHz or 3333 Mb/s DDR SRAM Memories* (2004), *available at* https://my.eng.utah.edu/~cs3710/xilinx-docs/examples/s3e_starter_revD_mig_ddr/docs/XAPP768c.pdf |

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| EX1028 | U.S. Patent No. 6,442,644 ("Gustavson") |
| EX1029 | U.S. Patent No. 6,560,669 ("Ryan") |
| EX1030 | U.S. Patent No. 6,240,040 ("Akaogi") |
| EX1031 | Pon, *Technology Scaling Impact on NOR and NAND Flash Memories and Their Applications* (2006), *available at* https://web.archive.org/web/20080225091210id_/http://www.pentium.pt/design/flcomp/papers/tech_scaling.pdf |
| EX1032 | U.S. Patent No. 7,499,323 ("Park") |
| EX1033 | U.S. Patent No. 6,178,518 ("Toda") |
| EX1034 | U.S. Patent No. 6,272,064 ("Wilford") |
| EX1035 | U.S. Patent No. 6,286,077 ("Choi") |
| EX1036-1099 | RESERVED |
| EX1100 | Complaint, *Mosaid Techs. Inc. v. Infineon Techs. AG et al.*, 1-25-cv-00436 (W.D. Tex.) (Mar. 25, 2025) |
| EX1101 | Mosaid Technologies Inc.'s Preliminary Infringement Contentions, Exhibit 028-A *MOSAID Technologies, Inc. v. Infineon Technologies AG, et al.*, 1-25-cv-00436 (W.D. Tex.) (Jun. 20, 2025) |
| EX1102 | Mosaid Technologies Inc.'s Preliminary Infringement Contentions, Exhibit 028-B *MOSAID Technologies, Inc. v. Infineon Technologies AG, et al.*, 1-25-cv-00436 (W.D. Tex.) (Jun. 20, 2025) |
| EX1103 | September 24, 2025 Stipulation |

Respectfully submitted,

Dated: September 24, 2025

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**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §42.6(e)(4), the undersigned certifies that on September 24, 2025, a complete and entire copy of this Petitioner's Updated List of Exhibits were provided via email, to the Patent Owner by serving the email correspondence addresses of record as follows:

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