

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

MOSAID TECHNOLOGIES INC.,

Plaintiff,

v.

**INFINEON TECHNOLOGIES AG and
INFINEON TECHNOLOGIES AMERICAS
CORP.,**

Defendants.

Civil Action No. 1:25-cv-436-ADA

DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Plaintiff MOSAID Technologies Inc. (“Plaintiff” or “MOSAID”) asserts three patents against Defendants Infineon Technologies AG and Infineon Technologies Americas Corp. (together, “Defendants” or “Infineon”): U.S. Patent Nos. 10,140,028 (“the ’028 Patent”), 9,972,381 (“the ’381 Patent”), and 7,685,393 (“the ’393 Patent”) (collectively, the “Asserted Patents”). Infineon propose constructions that adhere to the proper scope of the Asserted Patents’ claims. The parties competing construction proposals are set forth in Addendum A.

II. LEGAL STANDARDS

As this Court no doubt knows, claim construction is a pivotal procedure where the Court determines the meaning of the words used in the asserted patent claims as a matter of law, and those definitions are then used to determine infringement and validity. *See Wavetronix LLC v. EIS Elec. Integrated Sys.*, 573 F.3d 1343, 1354 (Fed. Cir. 2009); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 996 n.7 (Fed. Cir. 1995). By resolving disputes as to the meaning and scope of the asserted claims, the Court will allow the parties to enter discovery with increased certainty as to what is needed for each party to prove their case. *See, e.g., Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996).

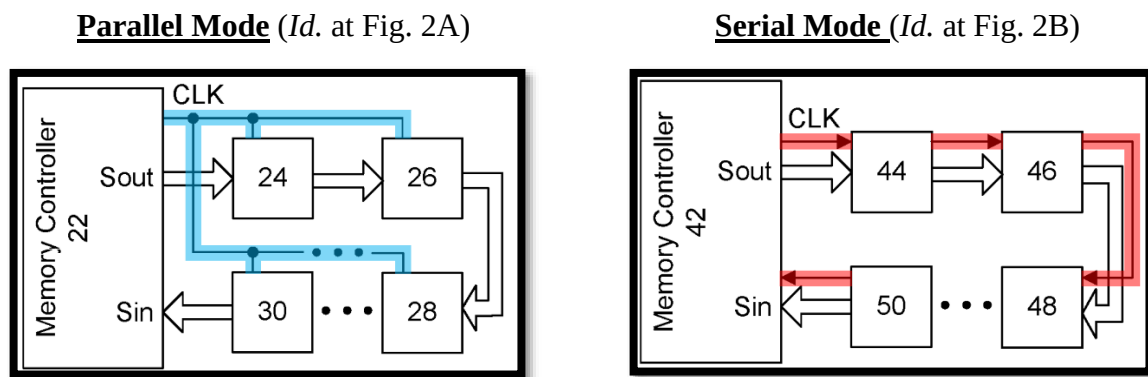
Claim construction requires examining the words of the claims to determine the scope of a patented invention. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). The words of the claims are generally given the “ordinary and customary meaning” that they “would have to a person of ordinary skill in the art in question at the time of the invention” “in the context of the entire patent, including the specification.” *Id.* The specification—the part of the patent preceding the claims describing the invention—provides the “single best guide to the meaning of a disputed term” and is usually dispositive of a term’s meaning. *Id.* at 1315. The entire intrinsic record, including the specification and prosecution history, must be examined when determining the

meaning of a claim term. *Id.* at 1315–16; *see also E.I. du Pont De Nemours & Co. v. Unifrax I LLC*, 921 F.3d 1060, 1068 (Fed. Cir. 2019). And, where necessary, the Federal Circuit has endorsed the use of extrinsic evidence to “help educate the court regarding the field of the invention and can help the court determine what a person of ordinary skill in the art would understand claim terms to mean.” *Phillips*, 415 F.3d at 1318–19.

III. THE '028 PATENT

A. Overview of the Asserted Patent

The '028 Patent concerns a purported improvement to a memory system. Ex. 1 ('028 Patent) at Abstract. According to the specification, in the prior art, a “clock signal” was “provided either in parallel to all the memory devices or serially from memory device to memory device through a common clock input.” *Id.* The '028 Patent purports to improve on this prior art with a memory device that does both. Namely, as shown below, the '028 Patent lets one memory device work in both a parallel clock mode (the blue clock path) and a serial clock mode (the red clock path). *Id.*



The '028 Patent describes memory devices that have the ports for operating in either parallel or serial mode. *Compare id.* at Fig. 3A (depicting memory devices operating in a serial clock configuration) *with id.* at Fig. 3C (depicting the same memory devices in a parallel clock configuration). When “the clock signals are provided in parallel,” each memory device gets the

clock signal directly from the controller—“therefore the clock output ports . . . of each memory device are unconnected.” *Id.* at 11:23–25.

In contrast, clock outputs are needed in serial mode. In serial mode, a “clock signal CLK is provided serially *to each* memory device *from* [a] memory controller 42 configured for providing the source synchronous clock signal CLK.” *Id.* at 8:8–14 (emphasis added). “Each memory device 44, 46, 48 and 50 will be configured *to receive and pass* the source synchronous clock CLK.” *Id.* at 8:12–14 (emphasis added). Though the patent does not define “source synchronous clock,” timely technical dictionaries explain that a “source-synchronous” clock is a “forwarded clock,” which is merely a “copy of the clock” input to the memory device. Ex. 2 (Athavale et al., *High-Speed Serial I/O Made Simple*, 2005) at 6.

B. “Clock output signal” means a synchronous periodic signal used to synchronize system operations, not any arbitrary timing

This Court should construe a “clock output signal” to mean “a periodic signal that synchronizes system operations,” consistent with the definition from both the intrinsic and extrinsic record.

First, the claimed function of the “clock output signal” is synchronizing system operations. Claim 1 states this in no uncertain terms—“the output data [is] **synchronized** with the clock output signal.” Ex. 1 (’028 Patent) at Cl. 1 (emphasis added). While an output signal could be asynchronous from the rest of the memory system, *id.* at 2:9–10, that’s not the case here—the “clock output signal is **referenced to** the first clock input signal.” *Id.* (emphasis added). And as explained in one embodiment, “the clock is used by each memory device . . . for **synchronizing** internal memory device operations.” *Id.* at 7:58–61 (emphasis added). Given that the claims require system operations be “synchronized with the clock output signal” and given that the clock

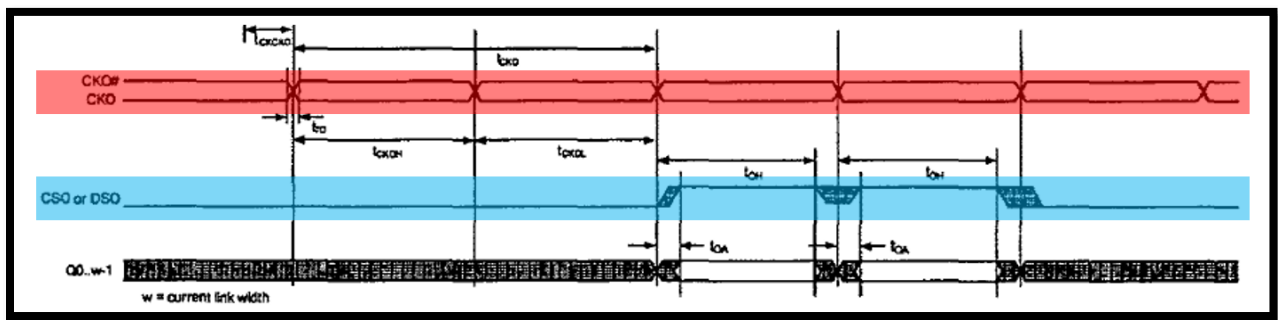
output signal is “referenced to” a signal used for synchronizing—the “clock output signal” must be synchronous for the claims to make sense.

Second, this synchronous interpretation comports with every embodiment in the specification that has a clock output port. According to the specification, memory devices use clock output ports to forward “source synchronous clock signals” in serial mode. *Id.* at 8:13–15. In serial mode, the “clock signal CLK is provided serially **to each** memory device **from** an alternate memory controller **42** configured for providing the source synchronous clock signal CLK.” *Id.* at 8:8–14 (emphasis added). “Each memory device **44, 46, 48 and 50** will be configured **to receive and pass** the source synchronous clock CLK.” *Id.* at 8:12–15 (emphasis added). The point is clear: clock outputs forward the same periodic clock from one device to the next to maintain synchronized timing.

Plaintiff’s contrary interpretation will sweep broadly enough to encompass control signals like data strobes, rewriting the claims. But if the claimed “clock output signal” could mean “strobe,” the specification would not have consistently referred to them by different terms. When a specification uses different terms at “different points in the specification,” it “suggests that the patent applicants were aware of their separate meanings,” and those separate meanings should apply in the claims. *See Horizon Pharma, Inc. v. Dr. Reddy’s Lab’ys Inc.*, 839 F. App’x 500 (Fed. Cir. 2021). Here, the specification repeatedly and consistently uses the term “clock” to refer to regular, repeating signals that helps memory systems keep time. *See* Ex. 1 (’028 Patent) at Figs. 3B, 3D, 7, 8B (depicting output clocks as periodic signals). The specification distinguishes clocks from data strobes by depicting data strobe ports separately from clock ports in numerous figures. *See, e.g., id.* at Figs. 3A, 3C, 4, 9. Even a data strobe’s function differs completely from that of a clock. For instance, a data strobe is “used for enabling the output port . . . and has a pulse duration

corresponding to the length of the read data being requested.” *Id.* at 10:8–9. If the plain meaning of “clock output signal” included “data strobes,” the specification would not have used the terms to refer to different components that perform different functions.

The embodiments in the provisional application maintain this distinction. There, the “clock output” is for “source-synchronous clocking,” which use “output clocks” for “which the output data is phase and frequency synchronous.” Ex. 3 (Provisional) at MOSAID_INF_436_00000245; *Trs. of Columbia Univ. in City of New York v. Symantec Corp.*, 811 F.3d 1359, 1365 (Fed. Cir. 2016) (looking to provisional application that “similarly defined” term for corroboration). Each memory device “repeat[s] the clocks to maintain the phase synchronous relationship between the arriving clocks **and** the arriving strobes and data.” Ex. 3 (Provisional) at MOSAID_INF_436_00000255 (emphasis added). In contrast, the “[d]ata strobe” input and output are described as “mark[ing] the start of an incoming Read Data packet.” *Id.* at MOSAID_INF_436_00000245. The provisional application’s timing diagram illustrate this distinction between the periodic nature of clocks and erratic nature of strobes, showing the clock output signals (**CKO#** and **CKO**) and data strobe output (**DSO**) alongside each other:



Id. at MOSAID_INF_436_00000256, Fig. 13 (annotated).

Finally, to the extent necessary, dictionary definitions comport with the meaning evident in the claim language, the specification, and the provisional’s use of the terms *clock* and *strobe*.¹ “Because dictionaries, and especially technical dictionaries, endeavor to collect the accepted meanings of terms used in various fields of science and technology, those resources have been properly recognized as among the many tools that can assist the court in determining the meaning of particular terminology to those of skill in the art of the invention.” *Phillips*, 415 F.3d at 1318. These dictionaries distinguish clocks (which “generate periodic signals for synchronization”) from strobes (which “triggers a data reading, transfer of information or sampling”). Ex. 4 (Newton’s Telecom Dictionary, 22d ed. 2006) at 334, 863. Clocks involve a “periodic *signal* used to synchronize digital data transfers or circuit actions,” whereas a strobe is an “electronic timing signal that . . . may inform a second device that data is present and stable on the input/output (I/O) port.” Ex. 5 (Hargrave’s Communications Dictionary, 2001) at 100, 498. Moreover, another dictionary defines *clock signal* itself—“periodic signals used for synchronizing events.” Ex. 6 (The Authoritative Dictionary of IEEE Standards Terms, 7th ed. 2000) at 177. Contrast that with the same dictionary’s definition of *strobe*—“pulse used to cause a register to assume and retain the state indicated by its data inputs” and a “pulse used as an input to a trigger circuit.” *Id.* at 1117.²

Contrary to MOSAID’s apparent assertion from its infringement contentions, a “clock output signal” does not encompass *all* timing. Not all timing signals are the same, even intuitively.

¹ *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1584 (Fed. Cir. 1996) (“As compared to expert testimony, which often only indicates what a particular expert believes a term means, prior art references may also be more indicative of what all those skilled in the art generally believe a certain term means.”).

² See also Ex. 7 (Newton’s Telecom Dictionary, 20th ed. 2004), 184 (“[A] clock has two functions . . . [t]o generate periodic signals for synchronization on a transmission facility[.]”);

For example, there are many ways to determine when one needs to leave. They could wear a watch that pulses and count the pulses to know what time it is. Alternatively, they could have someone tap them on the shoulder and tell them that it is time to leave. Here, “clock” aligns with the former method of keeping time—it aligns with (1) the language of the claims, (2) every embodiment in the intrinsic record, and (3) the understanding of a person of ordinary skill in the art (POSITA). Thus, the Court should adopt Infineon’s plain meaning construction: that “clock output signal” means “synchronous periodic signal.”

C. Indefiniteness: The terms “positive” and “negative clock input signal[s]” render claim 2 indefinite because they lack definition in the specification and make no sense in the context of an oscillating clock signal

This Court should find the terms “positive” and “negative clock input signals” indefinite because POSITAs lack reasonable certainty about what dependent claim 2’s “positive” and “negative clock input signal[s]” are. Those terms are nowhere defined—the specification never uses them, nor do the other claims—which suggests they are indefinite. *Mantissa Corp. v. First Fin. Corp.*, No. 2022-1963, 2024 WL 607717, at *3 (Fed. Cir. Feb. 14, 2024) (noting that the disputed “term . . . does not appear in the specification” when finding it indefinite). Instead, claim 2 merely explains that “the first clock input signal is a **positive** clock input signal, and the second clock input signal is a **negative** clock input signal,” without further explanation.

Beyond the lack of definition, the words “positive” and “negative” make little sense in the context of a clock signal. A clock signal does not carry a “positive” or “negative” designation; it toggles between high (voltage present) and low (no voltage present). At most, one might attempt to infer from the specification a “positive” clock signal (high) and a “zero” clock signal (low). But Claim 2 explicitly refers to a “negative clock input signal,” and the patent never explains what that means. Even if “negative” were read to mean “low,” claim 2 still cannot be reconciled with the nature of a clock signal. A clock does not remain at high or low indefinitely—it oscillates. Claim

2, therefore, is internally incoherent: it assigns static labels (“positive” and “negative”) to a signal whose essence is dynamic.

Because the claim language is ambiguous and the specification fails to clarify, a POSITA could not determine with reasonable certainty the scope of Claim 2. The Court should hold dependent claim 2 indefinite.

IV. THE '381 PATENT

A. Overview of the Asserted Patent

The '381 Patent relates to flash memory devices. Ex. 8 ('381 Patent) at 1:43–46. Specifically, the alleged invention addresses a need for memory devices “that have increased memory capacities and/or operating speeds while minimizing the number of input pins and wires required to access the memory modules.” *Id.* at 2:56–58. To achieve this purported advance, the '381 Patent recites variants of “flash memory device[s]” that have one or more “serial data links” and “control input ports” that “enable the memory device to transfer the serial data to a serial data output port” or “receiv[e] output enable signals.” *Id.* at Abstract.

B. Disputed Terms

1. The claims’ plain meaning requires that the control signal’s transition be *contemporaneous* with “*a beginning of command data being received*”

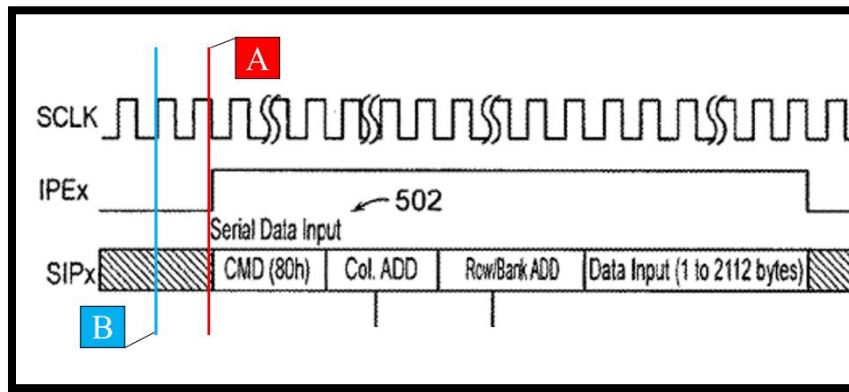
The parties dispute whether the control signal’s transition must be *contemporaneous* with “*a beginning of command data being received*.”³ Here, the plain language requires that the control signal transition contemporaneously with the *beginning* of data *being* received—nothing earlier,

³ Claim 1 and claim 17 both contain the disputed phrase, with the sole difference being claim 17’s use of “command data being *provided*” as opposed to “received.” Defendants provide the terms “received” and “provided” for context but will discuss received for purposes of this brief. Defendants reserve the right to address Plaintiff’s arguments based on this term.

nothing later. The claim’s grammar and word choice require a specific timing for the claimed data transfer—resulting in “indicates a beginning of” meaning “is contemporaneous with.”

The claim language is clear—the transition of the control signal relates to command data that is “**being** received.” That is—being received *right now*. The control signal’s transition does not indicate that command data “was being received” or “will be received.” The applicant did not use the past or future tense; instead, it discusses the data being received in the present, which is the only tense that gives operative effect to the claim’s surrounding terms.

Indeed, a construction of contemporaneity is the only one that gives “beginning” operative effect in the claims. “In construing claims . . . we must give each claim term the respect that it is due.” *Pause Tech., LLC v. TiVo, Inc.*, 419 F.3d 1326, 1334 (Fed. Cir. 2005). Here, data transfers are not instantaneous events—as the claim acknowledges, they have a “beginning,” middle, and end. The specification’s figures illustrate various data transfers that show many clock (SCLK) transitions before, during, and after a transfer of command (CMD), address (Col. ADD and Row/Bank ADD), and input data (Data Input):



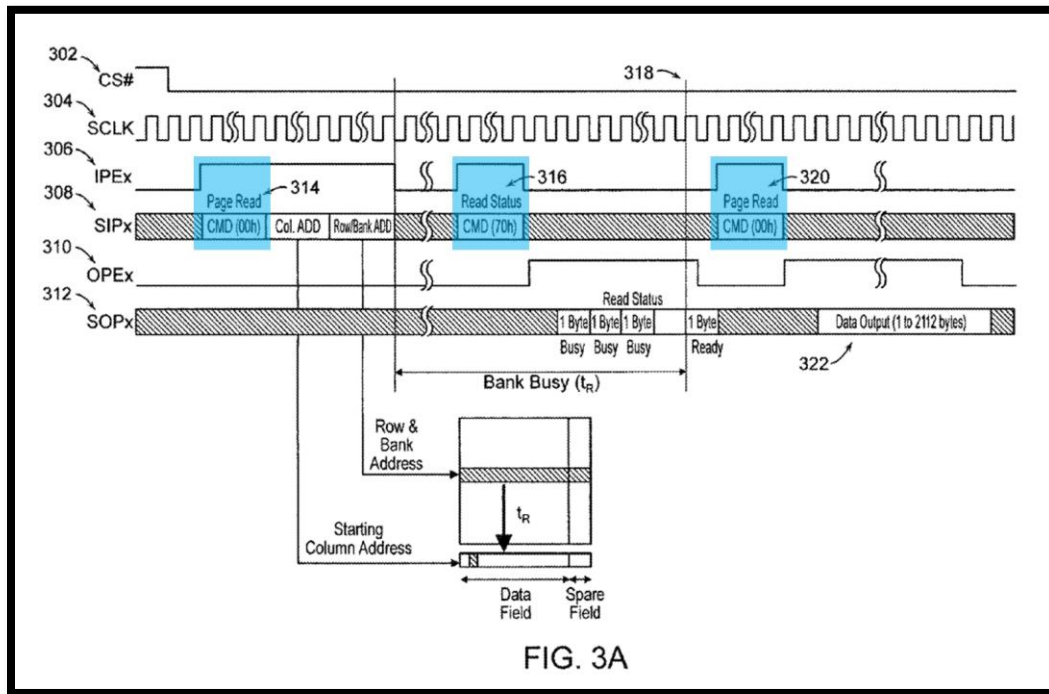
Ex. 8 ('381 Patent) at Fig. 5A (annotated). The “*beginning* of command data being received” occurs at point A, where a control signal’s (IPEX) transition indicates a *beginning* of command

data “being received.” In contrast, a control signal transition at the point labeled **B** would indicate that command data “will be received.”

Suppose that’s what the claim means—that the control signal’s transition “indicates a beginning of command data that *will be received*”—what work would the term “beginning” do? If the transition merely meant that command data would be received at some point in the future, there would be no reason to refer to the *beginning* at all. Such a reading would render “beginning” superfluous and reduce the claim to meaning “indicates . . . command data being received.” But every data transfer necessarily has a beginning, and if the whole data transfer is in the future (as it is at point **B**) then the “beginning” necessarily is, too. Here, given that it “is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous,” *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 810 (Fed. Cir. 2021) (quoting *Wasica Finance GmbH v. Continental Automotive Systems, Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017)), the applicant’s inclusion of the word “beginning” must be given effect.

Moreover, this effect—that the control signal transitions contemporaneously with “*a beginning of command data being received*”—is evidenced in every one of the patent’s embodiments. For instance, the specification discusses “two control signals, IPE (Input Port Enable) and OPE (Output Port Enable)” that transition contemporaneously with data being received. Ex. 8 (’381 Patent) at 3:41–43. “**When** IPE goes to ‘High’ . . . the SIP port **starts to receive** consecutive serial input stream bytes.” *Id.* at 3:49–57 (emphasis added). And “[i]f IPE goes to a ‘Low’ state, the SIP port **stops receiving** input signal streaming bytes.” *Id.* (emphasis added). The specification leaves in no uncertain terms the contemporaneous relationship between the control signal’s transition and the received data: “in response to the input port enable (IPEX) signal **306** set high, the serial input (SIPx) port **308 is sampled on the first rising edge of the serial**

clock (SCLK) signal 304.” *Id.* at 14:42–45. Figure 3A depicts one such example with multiple control signal transitions, wherein the transition aligns with the beginning of command data being received:



Id. at Fig. 3A (annotated). This same alignment of contemporaneous control signal transitioning and command data occurs again, (*id.* at Fig. 4), and again, (*id.* at Fig. 5A), and again, (*id.* at Fig. 6A), and again, (*id.* at Fig. 7), and again, (*id.* at Fig. 8A), and again, (*id.* at Fig. 8B), and again, (*id.* at Fig. 8C), in every timing diagram in the specification. Given that “[t]he only meaning that matters in claim construction is the meaning in the context of the patent,” *Trs. of Columbia Univ.*, 811 F.3d at 1363, the control signal’s transition be *contemporaneous* with *a beginning of* command data *being* received. *Cf. also id.* at 1364 (“[T]he patentee’s choice of preferred embodiments can shed light on the intended scope of the claims.”) (quoting *Astrazeneca AB, Aktiebolaget Hassle, KBI-E, Inc. v. Mut. Pharm. Co.*, 384 F.3d 1333, 1340 (Fed. Cir. 2004)).

2. **As before, “clock output signal” means a synchronous periodic signal used to synchronize system operations, not any arbitrary timing**

Like for the '028 Patent, *see supra* Section III.B, a “clock output signal” is “a periodic signal that synchronizes system operations.” It does not encompass *all* timing signals as MOSAID’s infringement contentions impliedly advance.

As with the '028 Patent, the claim language is clear. Claim 4 states that the “clock output signal” “transmit[s] a clock output signal **synchronized** with the output data.” Ex. 8 ('381 Patent) at Cl. 4 (emphasis added). While an output signal could be asynchronous from the rest of the memory system, *id.* at 14:61–66, that’s not the case here—the clock output signal is synchronized with the output data, *id.* at Cl. 4, and the “output data is transferred in synchronization with both rising and falling edges of the clock signal, *id.* at Cl. 1. If the output clock signal is synchronized with the output data, and the output data is synchronized with the input clock, then the output clock must be synchronized with the input clock. Indeed, claim 5 even prescribes a particular method for “synchroniz[ing] the clock output signal with the clock signal.” *Id.* at Cl. 5. Given that the claims require system operations be “synchronized” with the “clock output signal,” the “clock output signal” must be synchronous for the claims to make sense.

This synchronous interpretation comports with the embodiments from the specification. For instance, one of the provisional applications notes that the “serial clock output will be used **only if** clock signals are point-to-point connected in daisy-chain cascade configuration.” Ex. 9 (Provisional) at MOSAID_INF_436_00000395 (emphasis added). Figure 13B from the specification is consistent, explaining that in a “cascade configuration a serial clock output port (SCLKO) is added in every device.” Ex. 8 ('381 Patent) at 24:35–39. The specification also refers to “[a]dditional circuitry” that “may be used in every device in order to match (**or synchronize**) any phase difference between SCLKI and SCLKO signals.” *Id.* at 24:39–42 (emphasis added).

These embodiments only have an output clock signal so that another memory device can receive an input clock signal, meaning these signals must have the same qualities—that is, they must be synchronous periodic signals.

Third, and finally, dictionary definitions comport with the meaning evident in the claim language, the specification, and the provisional’s use of the terms *clock* as being a synchronous, periodic signal. *See supra* Section III.B (discussing pertinent dictionary definitions for clocks).

V. THE ’393 PATENT

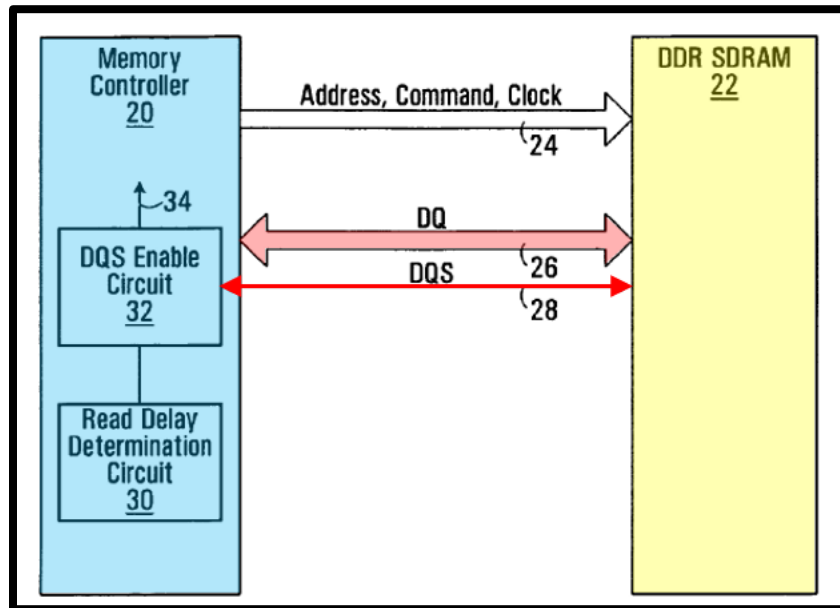
A. Overview of the Asserted Patent

The ’393 Patent purports to describe methods for controlling and transferring read and write data between a memory controller and a specific class of synchronous memories—those that employ “a bidirectional read/write bus with source-synchronous clocking, and a bidirectional data strobe.” Ex. 10 (’393 Patent) at 1:8–11. The patent repeatedly emphasizes this architecture as the context and focus of “the present invention.” *Id.* at 1:8–11, 3:9–11, 13:33–38, Fig. 1.

The specification explains that the described “synchronous memory” is not any generic synchronous device, but one having “a bidirectional read/write bus with source synchronous clocking, and a bidirectional data strobe.” *Id.* at 13:36–38; *see also id.* at 1:8–11, 3:9–11, Fig. 1. As a result, the patent expressly states that the invention is “applicable to all industry standard [Double Data Rate] DDR [Dynamic Random Access Memory] DRAMs that use bidirectional data strobes.” *Id.* at 13:33–36. One example of such memory is “DDR [Synchronous Dynamic Random-Access Memory] SDRAM.” *Id.* at 3:9–11, 3:24–25, 5:16–33, Fig. 1.

In the disclosed architecture (replicated below), a memory controller connects to a DDR SDRAM using three busses: (1) a unidirectional bus to send addressees, commands, and clock signals; (2) a bidirectional write/read bus (“DQ”); and (3) a bidirectional bus for data strobe clock (“DQS”). *Id.* at 5:16–33. The controller includes a read delay determination circuit “that

determines the read delay between the memory controller . . . and the DDR SDRAM” and a DQS enable circuit that “produces a gated DQS signal” as a function of the read delay. *Id.*



Id. at Fig. 1 (annotated).

To determine the delay, the controller writes an initialization sequence (for example, a Gray code) to the memory, issues a read command, and generates an “initialization sample” by sampling contents of data input latches.” *Id.* at 5:46-50, 6:25-27, 7:6-51, 9:16-34. One embodiment “sampl[es] each bit of the [initialization sequence] with four clock phases” (i.e., obtains 0°, 90°, 180°, 270° samples) at predetermine time “to determine what the read delay is.” *Id.* at 7:25-43, 9:16-34, 10:25-37, 10:52-67. “Having determined the read delay, DQS enable circuit . . . enables/disables the incoming DQS and/or DQS90” in accordance with the read delay. *Id.* at 8:10-23, 11:1-19. In short, the purported invention of the ’393 Patent attempts to determine “the optimum timing of the DQS enable signal in a single read operation.” *Id.* at Abstract, 4:7-15.

B. Disputed term: “a synchronous memory” (claim 1)

The Court should construe “a synchronous memory” in the preamble of claim 1 as “a memory that has a bidirectional read/write bus with source-synchronous clocking and a

bidirectional data strobe,” and hold the preamble limiting, because (1) the preamble supplies the antecedent structural context for every step of the claimed method; (2) the specification expressly excludes *single data rate* synchronous memories from the scope of claims, and instead repeatedly limits all embodiments to a memory with bidirectional data (read/write) bus with source-synchronous clocking and bidirectional data strobe; and (3) the parallel independent claims define the same memory while implementing the same method sequence. MOSAID’s “plain and ordinary meaning” construction would improperly encompass memory types expressly excluded by the specification.

1. The preamble is limiting

Claim 1 is written as “[a] method for controlling a synchronous memory comprising” followed by a five-step sequence that repeatedly refers to “the memory”—a term whose only antecedent is the “synchronous memory” in the preamble. That preamble therefore “recites essential structure [and] is necessary to give life, meaning, and vitality to the claim.” *Catalina Mktg. Int’l, v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (internal quotation marks and citation omitted).

The prosecution record reinforces that the preamble frames the invention being claimed. In responding to an anticipation rejection, the applicant characterized “Claim 1 of the subject application” as “involv[ing] controlling a **synchronous memory** by establishing a read data path delay,” then reproduced the claim text with the same preamble and four-step body. Ex. 11 (Applicant’s Remarks) at MOSAID_INF_436_00001454 (emphasis added). That clear reliance on the preamble’s statement of the invention supports treating it as limiting. *See Catalina*, 289 F.3d at 808 (when a claim preamble is “essential to understand . . . terms in the claim body, the preamble limits claim scope.”).

2. Intrinsic evidence supports Infineon’s construction

MOSAID’s “plain and ordinary meaning” theory—under which any synchronous memory would satisfy the claim—is contrary to the intrinsic record. The ’393 Patent specification is unequivocal that the invention does not encompass all synchronous memories.

The ’393 Patent explicitly states that “the present invention” applies only to certain types of synchronous memories. “When a patent . . . describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.” *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1308 (Fed. Cir. 2007); *Honeywell Int’l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006) (statements in the specification characterizing “the present invention” limited the scope of claims); *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) (“We have found disavowal or disclaimer based on clear and unmistakable statements by the patentee that limit the claims, such as “the present invention includes . . .” or “the present invention is . . .” or “all embodiments of the present invention are . . .”).

The specification opens by stating that the invention of the ’393 Patent “relates to the control and transfer of read and write data between a memory controller and a synchronous memory using bidirectional databusses and bidirectional data strobe signals.” Ex. 10 (’393 Patent) at 1:7-11 (emphasis added). Later it generalizes: “More generally still, embodiments of the invention are applicable to a memory that has a bidirectional read/write bus with source synchronous clocking, and a bidirectional data strobe.” *Id.* at 13:33–38.

The specification distinguishes synchronous memory types to which the invention does not apply because the underlying timing problem does not exist there. The Federal Circuit recognizes that “an inventor may disavow claims lacking a particular feature when the specification distinguishes or disparages prior art based on the absence of that feature.” *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016); *see also Hill-Rom Servs., Inc. v. Stryker Corp.*,

755 F.3d 1367, 1372 (Fed. Cir. 2014) (“Disavowal requires that the specification or prosecution history make clear that the invention does not include a particular feature or is clearly limited to a particular form of the invention.”) (internal quotation marks and citations omitted). The background section of the specification distinguishes “single data rate” SDRAMs, which “do not have a DQS clock.” Ex. 10 (’393 Patent) at 1:55–67. These statements confirm that the claimed “synchronous memory” excludes such technologies and is limited to memories with a bidirectional data bus (DQ), source-synchronous clocking, and a bidirectional data strobe (DQS)—such as a Double Data Rate (DDR) SDRAM. *See, e.g., id.* at 13:33–36, Fig. 1.

Finally, independent claims 17, 18, 21, and 22 each recite a memory “that has a bidirectional read/write bus with source synchronous clocking and a bidirectional data strobe.” The “memory controller ... for implementing a method” in claim 17 recites the same method sequence as claim 1. *Compare id.* at Cl. 17 (a method claim) *with id.* at Cl. 1 (at apparatus claim). That parallel claim structure confirms that the “synchronous memory” of claim 1 is the same type of memory described explicitly in those other independent claims.

3. MOSAID’s proposed “plain and ordinary meaning” does not resolve the dispute

“Synchronous memory” is not a single, settled term of art that, standing alone, resolves whether SDR SDRAM can qualify. The patent’s background section explains why it does not—because it lacks a bidirectional data strobe (DQS)—underscoring the need for a construction anchored in the intrinsic record. *See id.* at 1:55–57.

Because the parties dispute the scope of “synchronous memory” and MOSAID’s “plain and ordinary meaning” position would leave that dispute to the jury, the Court must construe the term based on the intrinsic record. *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008) (“A determination that a claim term ‘needs no construction’ or has

the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.”). None of MOSAID’s identified extrinsic evidence materials defines “synchronous memory.” See generally Ex. 12. And the fact that the component words—“synchronous” and “memory”—are generally known does not render the combined phrase self-defining to a POSITA when its scope is contested. *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1319 (Fed. Cir. 2016) (holding it was an error to give terms’ plain and ordinary meaning to the jury where scope of the term was disputed by the parties). Accordingly, MOSAID’s bare appeal to “plain and ordinary meaning” is insufficient to resolve the parties’ controversy over claim scope.

For the reasons above, the Court should construe “a synchronous memory” (Claim 1) as “a memory that has a bidirectional read/write bus with source synchronous clocking and a bidirectional data strobe.”

C. Indefiniteness

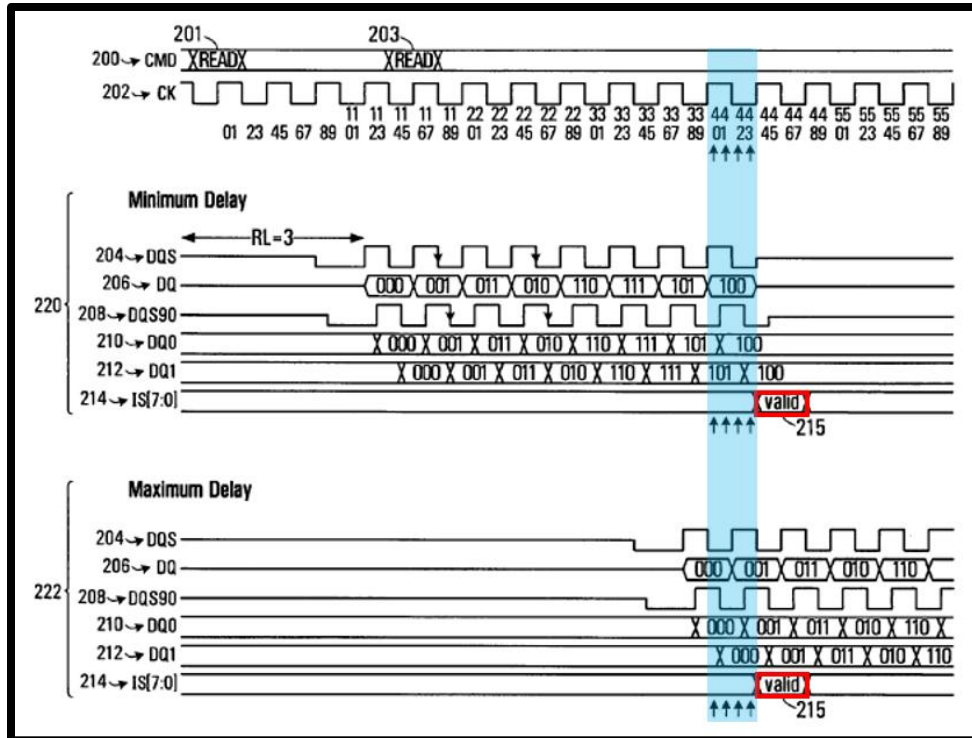
1. The term “a single initialization sample” (claim 1) is indefinite because the specification fails to define what is meant by “single”

The claim term “a single initialization sample”⁴ is indefinite because the intrinsic record provides no objective boundary for what “single” means in this context—indeed the specification describes an “initialization sample” as continuously changing and only “valid” after an unspecified delay—leaving a POSITA without “reasonable certainty” as to the scope of “a single initialization sample.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 899 (2014).

Claim 1 requires “sampling the returned data signals to produce *a single initialization sample*.” Ex. 10 (’393 Patent) at Cl. 1 (emphasis added). But the specification explains the

⁴ This claim language also appears in unasserted independent claims 17-18 of the ’393 Patent.

“initialization sample output is changing continuously as a function of the input” and is only “valid a predetermined time after the initial READ command” such as after “clock counts=40, 41, 42, 43”—with no teaching of how such a predetermined time is selected and what makes “initialization sample” “valid.” *Id.* at 9:35–40, 10:30–33. Figure 5, replicated below, illustrates this arbitrary selection point for sampling “single initialization sample”:



Id. at Fig. 5 (annotated).

The specification also discloses that the “initialization sample” is generated by aggregating samples of content of multiple latches at a defined instance. *Id.* at 7:17–19. The specification also states that the disclosed method can be performed using “a single read operation” and “single burst.” *Id.* at Abstract. The body of the specification consistently refers to “the initialization sample” but never to a “*single* initialization sample.” The document nowhere cabins “single” to a moment, a transaction, or a data structure. These teachings of the ’393 Patent therefore leave a POSITA with several plausible readings of “single.” *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 789

F.3d 1335, 1341 (Fed. Cir. 2015) (holding that a term, such as “molecular weight,” is indefinite when multiple plausible methodologies yield different results and the intrinsic record didn’t choose among them).

Notably, the term “single” is not in the original claims. After the August 10, 2009, Notice of Allowance, after raising new prior art and discussing it with the applicant, the examiner entered an Examiner’s Amendment adding “a single initialization sample” to claims 1, 17, and 18. See Ex. 11 (Notice of Allowability) at MOSAID_INF_436_00001575–78. But the amendment is not based on the specification. That is classic indefiniteness: adding a new, undefined claim modifier to avoid prior art, without tethering it to the disclosure. *Halliburton Energy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1250 (Fed. Cir. 2008) (finding a claim term indefinite when “[a] proposed definition nor any other possible construction resolve the ambiguity in the scope of the term.”).

2. The terms “the read delay” / “read delays” (claims 9, 13) lack antecedent bases, and are therefore indefinite

The phrases “the read delay” (claims 9 and 13) and “read delays” (claim 9)⁵ are indefinite because the claims never supply a unique antecedent basis for those terms and the intrinsic record discloses multiple, different “delay” concepts—leaving a POSITA without reasonable certainty as to claim scope. *Nautilus*, 572 U.S. at 910.

Claim 9’s text presents two antecedent-basis problems. The Federal Circuit has held that a claim term may be indefinite when it lacks proper antecedent basis and its meaning is not otherwise reasonably ascertainable. *Energizer Holdings, Inc. v. Int’l Trade Comm’n*, 435 F.3d 1366, 1370–71 (Fed. Cir. 2006). Claim 9 first introduces only a set of delays—“for each of a plurality of read delays, storing an expected initialization sample”—but then requires “looking up

⁵ The terms “read delay” and “read delays” also appear in unasserted claims 2, 10 and 17-18 of the ’393 Patent.

the read delay stored for the initialization sequence.” Ex. 10 (’393 Patent) at Cl. 9 (emphasis added). The claim never previously “stores” any read delay (only an expected initialization sample), and it provides no singular antecedent for “the read delay” to which the definite article could refer. The result is a mismatch and, more importantly, a reference to a stored delay that the claim never introduced. A POSITA cannot tell which delay—among the plurality, or something else entirely—is being “looked up.” That is classic antecedent-basis indefiniteness.

Likewise, claim 13’s “the read delay” has no antecedent in its claim chain and conflicts with the term used in claim 1 (from which claim 13 depends). Indeed, claim 13 recites “updating the read delay,” but neither claim 13 nor claim 1 (its base) first introduces a “read delay.” Claim 1 repeatedly uses the different term “**read data path delay**.” *Id.* at Cl. 1 (emphasis added). The patentee deliberately amended claim 1 to change “the read delay” to “read data path delay,” but left dependent claims (including claim 13) using “the read delay.” Ex. 11 (September 10, 2008 Claim Amendments) at MOSAID_INF_436_00001446. A POSITA is now left to guess whether claim 13’s “read delay” means the “read data path delay” of claim 1 or some other controller timing (e.g., is it a loop-around read delay measured from a memory controller to a memory, and back, or a delay only between the memory controller and memory).

Here, the ’393 Patent never anchors “the read delay” or “read delays” to any clear antecedent, and it compounds the ambiguity by using a different amended term—“read data path delay”—elsewhere in the claim set. These phrases therefore lack objective boundaries and are indefinite.

3. The term “an expected initialization sample” (claim 9) is undefined and indefinite

“An expected initialization sample” is indefinite because the ’393 Patent never defines what makes an “initialization sample” “**expected**,” uses internally inconsistent claim language, and

decouples what is stored from what is later looked up—leaving a POSITA without reasonable certainty about the term’s scope. *Nautilus*, 572 U.S. at 910.

First, claim 9 itself is self-contradictory and internally misaligned. Claim 9 recites “for each of a plurality of read delays, storing an **expected initialization sample**,” and then states that determining the read delay “comprises looking up the read delay stored for the **initialization sequence**.” Ex. 10 (’393 Patent) at Cl. 9 (emphasis added). The claim thus (i) stores an “expected ... sample,” yet (ii) looks up a read delay “for the ... sequence.” *Id.* The very next claim switches this term again—Claim 10 recites “storing an expected initialization **sequence**.” *Id.* at Cl. 10 (emphasis added). This sample/sequence toggle across adjacent dependent claims creates ambiguity as to what artifact is “expected” and what is actually stored and later consulted. And because the specification distinguishes between “initialization sample” and “initialization sequence,” the use of “expected initialization sample” in Claim 9 renders the claim indefinite.

Second, “an expected initialization sample” is also indefinite for an independent reason: the specification never uses—let alone defines—this term. *Mantissa Corp.*, 2024 WL 607717, at *3 (noting that the disputed “term . . . does not appear in the specification” when finding it indefinite). The intrinsic record consistently uses “initialization sample” without the “expected” modifier. Nothing in the specification or prosecution history describes an “expected” sample, how to compute it, or what reference it is “expected” relative to.

As explained above, *see supra* Section V.C.1, the specification explains the “initialization sample” is changing continuously and generated during several clock counts, and can be assembled across separate read operations. With all such variables, a POSITA cannot tell what is an “expected initialization sample” for any given delay.

Based on the foregoing, the term “an expected initialization sample” is indefinite.

VI. CONCLUSION

For these reasons, the Court should adopt (i) the parties' agreed constructions and (ii) Defendants' proposed constructions for the disputed terms in the Asserted Patents.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a) on October 27, 2025, and was served via electronic mail on all counsel of record.

/s/ David M. Hoffman

David M. Hoffman