

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

MOSAID TECHNOLOGIES INC.,

Plaintiff,

v.

**INFINEON TECHNOLOGIES AG and
INFINEON TECHNOLOGIES AMERICAS
CORP.,**

Defendants.

Civil Action No. 1:25-cv-436-ADA

INFINEON’S PRELIMINARY INVALIDITY CONTENTIONS

Defendants Infineon Technologies AG and Infineon Technologies Americas Corp., collectively (“Infineon”) provide the following disclosure of Preliminary Invalidity Contentions to Plaintiff MOSAID Technologies Inc. (“MOSAID”) regarding United States Patent No. 7,685,393 (the “’393 Patent”), United States Patent No. 9,972,381 (the “’381 Patent”), and United States Patent No. 10,140,028 (the “’028 Patent”) (collectively, the “Patents-in-Suit” or “Asserted Patents”).

These preliminary contentions are made only as to the claims of the Patents-in-Suit that MOSAID has identified in its Preliminary Infringement Contentions dated June 20, 2025:

Patent	Asserted Claims	MOSAID Alleged Priority Date(s)	Chart Prefix
’393 Patent	1, 9, 13	April 28, 2005, or, in the alternative, January 3, 2006, or, in the alternative, January 6, 2006, or, in the alternative, January 18, 2006, or, in the alternative, February 8, 2006, or, in the alternative, June 30, 2006	393

'381 Patent	1–6, 8–21	August 29, 2005, or, in the alternative, November 25, 2005, or, in the alternative, May 12, 2006, or, in the alternative, September 30, 2005, or, in the alternative, December 30, 2005, or, in the alternative, September 27, 2006, or, in the alternative, October 19, 2006, or, in the alternative, November 21, 2008, or, in the alternative, September 15, 2010, or, in the alternative, May 3, 2012 April 22, 2013, or, in the alternative, January 15, 2014, or, in the alternative, December 30, 2015, or, in the alternative, November 8, 2016, or, in the alternative, August 31, 2017, or, in the alternative, January 11, 2018	381
'028 Patent	1–4, 8, 10–16	February 16, 2007, or, in the alternative, February 15, 2008, or, in the alternative, January 13, 2011, or, in the alternative, April 26, 2013, or, in the alternative, January 17, 2014, or, in the alternative, September 19, 2014, or, in the alternative, May 22, 2015, or, in the alternative, January 15, 2016, or, in the alternative, December 14, 2016, or, in the alternative, July 20, 2017, or, in the alternative, April 19, 2018	028

Infineon reserves the right to supplement these preliminary invalidity contentions at least per the parties' agreement and/or to the extent MOSAID is allowed to change their Asserted Claims.

These preliminary invalidity contentions are being made before fact discovery opens and before claim construction. The parties have not yet started general discovery and document production, and no depositions have been noticed or taken. No third-party discovery of any underlying issue has been taken. Accordingly, Infineon reserves the right to supplement and amend these preliminary contentions to the extent additional information becomes available during discovery, including the deadline for serving Final Invalidity Contentions. Infineon may serve third-party discovery on companies that it is informed and believes have relevant prior art. Infineon will also be taking third-party discovery from the individuals named as inventors on MOSAID patent filings and associated companies. Infineon may also serve additional third-party discovery in the future including, but not limited to, based on discovery received from MOSAID, the inventor, and/or the above-referenced third parties. Infineon reserves the right to supplement and/or amend its invalidity contentions to include new prior art discovered from MOSAID, from the named inventors, from these third-party sources, or other sources.

I. RESERVATIONS

A. General Reservation of Right

The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any claim terms. In certain instances, Infineon has applied the claims to the prior art in view of MOSAID's allegations, admissions, or positions for purposes of these preliminary invalidity contentions only, to the extent Infineon can discern MOSAID's allegations. This disclosure of preliminary invalidity contentions is not intended to be, and is not, an admission that any Asserted Claim is infringed by any of Infineon's products, any particular feature or aspect of any of the accused products practices any limitations of the Asserted Claims, or any of the constructions implicit in MOSAID's Preliminary Infringement Contentions is reasonable, supportable, or proper. Rather, in some instances, Infineon's

application of the claims to the prior art is intended to apply MOSAID's apparent interpretation of the claims.

B. The Intrinsic Record

Infineon reserves the right to rely on applicable industry standards and prior art cited in the file histories of the Patents-in-Suit and any related U.S. and foreign patent applications as invalidating references or to show the state of the art. Infineon further reserves the right to rely on the patent applicant's admissions concerning the scope of the prior art relevant to the Patents-in-Suit found in, *inter alia*: the patent prosecution history for the Patents-in-Suit and any related patents and/or parent applications or reexaminations (or *inter partes* review or post-grant review proceedings); any deposition testimony of the named inventor or inventors whose names were removed during prosecution of the Patents-in-Suit; any deposition testimony or other admissions by MOSAID; and the papers filed and any evidence submitted by MOSAID in connection with this or any related litigation or proceeding.

C. Rebuttal Evidence

Prior art not included in these preliminary invalidity contentions, whether known or not known to Infineon, may become relevant. In particular, Infineon is currently unaware of the extent, if any, to which MOSAID will contend that limitations of the Asserted Claims of the Patents-in-Suit are not disclosed in the prior art identified herein or otherwise contend the Patents-in-Suit are not invalid. To the extent that such an issue arises, Infineon reserves the right to identify other references that would render obvious the allegedly missing limitation(s) or the disclosed device or method, or otherwise rebut MOSAID's argument(s).

D. Contextual Evidence

Infineon's claim charts cite particular teachings and disclosures of the prior art as applied to the limitations of each of the Asserted Claims. However, persons having ordinary skill in the

art generally may view an item of prior art in the context of his or her experience and training, other publications, literature, products, and understandings. Moreover, common sense may be employed as part of the obviousness analysis. As such, Infineon may rely on the uncited portions of the prior art references and on other publications, expert testimony, and common sense as aids in understanding and interpreting the cited portions, as providing context thereto, and as additional evidence that the prior art discloses a claim limitation or the claimed subject matter as a whole. Infineon further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony, including expert testimony, to establish bases for combinations of certain cited references that render the Asserted Claims obvious. The references discussed in the claim charts may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. The suggested obviousness combinations are provided in the alternative to anticipation contentions and are not to be construed as suggesting that any reference included in the combinations is not by itself anticipatory.

II. IDENTIFICATION OF PRIOR ART

The following patents, publications, systems, and admitted prior art are prior art to the Asserted Claims of the Patents-in-Suit under at least 35 U.S.C. §§ 102(a), (b), (d), (e) and/or (g). Infineon also incorporates as if fully set forth in these Preliminary Invalidity Contentions the complete prosecution histories for the Patents-in-Suit and related patents, including the prior art and supporting documents cited in those prosecution histories. Infineon may cite or rely upon the prosecution histories, the examiner's findings, and the prior art cited therein to support or provide context for these Preliminary Invalidity Contentions.

Infineon not only relies upon the prior art disclosed in these Preliminary Invalidity Contentions, but also relies on any commercial embodiments and accompanying literature (or

other evidence and/or witness testimony) of the various assignees that correspond to the respective disclosures found within the prior art disclosed in these contentions. The assignees' various and respective commercial embodiments and/or corresponding literature (or other evidence and/or witness testimony) anticipate and/or render obvious the claims of the Asserted Patents for at least the reasons disclosed in these Preliminary Invalidity Contentions, as well as for other independent reasons found within the commercial embodiments and corresponding literature. Infineon also reserves the right to rely on related patents, published applications, foreign patents or publications, and other patent documents as necessary to establish prior art status or clarify the disclosures cited. Infineon further reserves the right to rely on the earliest publication or priority dates to which each of the prior art references are entitled, including dates on which a claim of priority may be based for patent references that are any of a divisional, continuation, or continuation-in-part of an earlier filed patent application.

Infineon reserves the right to revise its claim charts to rely on any of these references to prove the invalidity of the claims of the Patents-in-Suit in a manner consistent with the Federal Rules of Civil Procedure, the Court's Local Rules, and this Court's Orders.

A. Patents and Published Patent Applications

1. '393 Patent

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 5,917,760 ("Millar '760")	Bruce Millar	September 19, 1997	June 29, 1999
U.S. 6,182,253 ("Lawrence '253")	Archer R. Lawrence, Jack C. Little	July 16, 1997	January 30, 2001
U.S. 6,615,345 ("LaBerge '345")	Paul A. LaBerge	July 29, 1999	September 2, 2003
U.S. 6,617,842 ("Nishikawa '842")	Katsumi Nishikawa, Kazuo Shibata	December 22, 2000	September 9, 2003

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 6,629,225 ("Zumkehr '225")	John F. Zumkehr	May 31, 2001	September 30, 2003
U.S. 6,674,378 ("Johnson '378")	Brian Johnson, Brent Keeth	February 13, 2003	January 6, 2004
U.S. 6,763,444 B2 ("Thomann '444")	Mark R. Thomann, Christopher K. Morzano, Wen Li	May 8, 2001	July 13, 2004
U.S. 6,950,350 ("Kerl '350")	Daniel L. Kerl	April 4, 2002	September 27, 2005
U.S. 6,982,922 ("Stark '922")	Donald C. Stark	March 11, 2003	January 3, 2006
U.S. 7,310,752 ("Jeddeloh '752")	Joseph M. Jeddeloh	September 12, 2003	December 18, 2007
U.S. 2005/0047192 A1 ("Matsui '192")	Shigezumi Matsui, Takashi Sato, Kazuyuki Sakata, Tsuyoshi Yaguchi, Kenzo Kuwabara, Atsushi Nakamura, Motoo Suwa, Ryoichi Sano, Hisashi Shiota	July 21, 2004	March 3, 2005
U.S. 2005/0135167 A1 ("Manabe '167")	Takashi Manabe	September 28, 2004	June 23, 2005

2. '381 Patent

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 6,654,307 ("Widmer '307")	Kevin C. Widmer, Cliff Zitlaw, Frankie Fariborz Roohparvar	Mar 21, 2002	Nov. 25, 2003
U.S. 2004/0243909 ("Roohparvar '909")	Frankie Roohparvar	May 8, 2003	Dec. 2, 2004
U.S. 6,570,791 ("Roohparvar '791")	Frankie Fariborz Roohparvar, Kevin C. Widmer	Aug. 30, 2001	May 27, 2003
U.S. 7,831,794 ("Ito '794")	Takafumi Ito	Jun. 29, 2006	Nov. 9, 2010
U.S. 2004/0148482 ("Grundy '482")	Kevin Grundy, Para Segaram	Jan. 13, 2004	Jul. 29, 2004

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 2004/0081005 ("Garrett '005")	Billy Garrett, Frederick Ware, Craig Hampel, Richard Barth, Donald Stark, Abhijit Abhyankar, Catherine Chen, Thomas Sheffler, Ely Tsern, and Steven Woo	Oct. 20, 2003	Apr. 29, 2004
U.S. 7,376,020 ("Sorrells '020")	Peter H. Sorrells, David L. Wilkie, Christopher A. Parris, Martin S. Kvasnicka, Martin R. Bowman	Dec. 13, 2005	May 20, 2008
U.S. 6,266,273 ("Conley '273")	Kevin M. Conley, Daniel C. Guterman, Carlos J. Gonzalez	Aug. 21, 2000	Jul. 24, 2001
U.S. 2006/0023499 ("Ryu '499")	Dong-ryul Ryu	Nov. 24, 2004	Feb. 2, 2006
U.S. 2005/0204091 ("Kilbuck '091")	Kevin Kilbuck, David Eggleston	Mar. 11, 2004	Sep. 15, 2005
U.S. 6,452,431 ("Waldrop '431")	William C. Waldrop	Aug. 28, 2000	Sep. 17, 2002
U.S. 6,892,270 ("Roohparvar '270")	Frankie F. Roohparvar	Feb. 25, 2004	May 10, 2005
U.S. 7,558,900 ("Jigour '900")	Robin J. Jigour, Eungjoon Park, Joo Weon Park, Jong Seuk Lee	Mar. 11, 2005	Jul. 7, 2009

3. '028 Patent

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 2006/0023499 ("Ryu '499")	Dong-ryul Ryu	Nov. 24, 2004	Feb. 2, 2006
U.S. 6,337,832	Tsukasa Ooishi, Masatoshi Ishikawa	Mar. 18, 1999	Jan. 8, 2002

Number	Inventor(s)	Date Filed	Date Issued / Published
U.S. 2006/0139068	Ying Cole, Songmin Kim, Robert Greiner	Feb. 21, 2006	Jun. 29, 2006
U.S. 5,864,506	Mathew R. Arcoleo, Raymond M. Leong, Derek R. Johnson	Jan. 14, 1998	Jan. 26, 1999
U.S. 5,917,759	Shunichi Akashi	Aug. 14, 1998	Jun. 29, 1999
U.S. 6,654,307 ("Widmer '307")	Kevin C. Widmer, Cliff Zitlaw, Frankie Fariborz Roohparvar	Mar 21, 2002	Nov. 25, 2003
U.S. 2003/0201804	William Waldrop	May 6, 2003	Oct. 30, 2003
U.S. 7,221,617	Bjorn Flach, Monica De Castro Martins, Wolfgang Ruf, Martin Schnell	May 12, 2005	May 22, 2007
W.O. 2002/029581	Brian L. Smith	Sep. 17, 2001	Apr. 11, 2002
U.S. 6,570,791 ("Roohparvar '791")	Frankie Fariborz Roohparvar, Kevin C. Widmer	Aug. 30, 2001	May 27, 2003
U.S. 7,831,794 ("Ito '794")	Takafumi Ito	Jun. 29, 2006	Nov. 9, 2010
U.S. 2004/0148482 ("Grundy '482")	Kevin Grundy, Para Segaram	Jan. 13, 2004	Jul. 29, 2004
U.S. 2006/0220683	Jun-Hyun Chun	Jul. 8, 2005	Oct. 5, 2006
U.S. 6,892,270 ("Roohparvar '270")	Frankie F. Roohparvar	Feb. 25, 2004	May 10, 2005
U.S. 7,376,020 ("Sorrells '020")	Peter H. Sorrells, David L. Wilkie, Christopher A. Parris, Martin S. Kvasnicka, Martin R. Bowman	Dec. 13, 2005	May 20, 2008
U.S. 2005/0204091 ("Kilbuck '091")	Kevin Kilbuck, David Eggleston	Ma. 11, 2004	Sep. 15, 2005
U.S. 2004/0243909 ("Roohparvar '909")	Frankie Roohparvar	May 8, 2003	Dec. 2, 2004
U.S. 2004/0081005 ("Garrett '005")	Billy Garrett, Frederick Ware, Craig Hampel, Richard Barth,	Oct. 20, 2003	Apr. 29, 2004

Number	Inventor(s)	Date Filed	Date Issued / Published
	Donald Stark, Abhijit Abhyankar, Catherine Chen, Thomas Sheffler, Ely Tsern, and Steven Woo		
U.S. 6,266,273 ("Conley '273")	Kevin M. Conley, Daniel C. Guterman, Carlos J. Gonzalez	Aug. 21, 2000	Jul. 24, 2001
U.S. 6,452,431 ("Waldrop '431")	William C. Waldrop	Aug. 28, 2000	Sep. 17, 2002
U.S. 7,558,900 ("Jigour '900")	Robin J. Jigour, Eungjoon Park, Joo Weon Park, Jong Seuk Lee	Mar. 11, 2005	Jul. 7, 2009

B. Publications

1. '393 Patent

Title	Author / Publisher	Pub. Date
Xcell Journal, Virtex V4, Issue 52, First Quarter 2005 (available at: https://www.xilinx.com/publications/archives/xcell/Xcell52.pdf) (last accessed Aug. 13, 2025)	Xilinx	2005

2. '381 Patent

Title	Author / Publisher	Pub. Date
Jim Cooke, Flash Memory 101: An Introduction to NAND Flash, EE Times (Mar. 20, 2006), available at https://www.eetimes.com/flash-memory-101-an-introduction-to-nand-flash/ (last accessed Aug. 3, 2025) [hereinafter "Cooke"]	Jim Cooke	Mar. 20, 2006
JESD79-2B	JEDEC Solid State Technology Association	January 2005

3. '028 Patent

Title	Author / Publisher	Pub. Date
Jim Cooke, Flash Memory 101: An Introduction to NAND Flash, EE Times (Mar. 20, 2006), available at https://www.eetimes.com/flash-memory-101-an-introduction-to-nand-flash/ (last accessed Aug. 3, 2025) [hereinafter “Cooke”]	Jim Cooke	Mar. 20, 2006
JESD79-2B	JEDEC Solid State Technology Association	January 2005

Infineon additionally identifies and relies on patent or publication references that describe or are otherwise related to the prior art systems identified below. Infineon’s investigation into prior art patent and publication references remains ongoing, and Infineon reserves the right to identify and rely on additional patent or publication references that are identified through further investigation or discovery. Infineon reserves the right to supplement as further prior art is identified through investigation or discovery.

C. Systems

The following systems¹ are prior art to one or more of the Asserted Claims.

1. '393 Patent

Item	Person or Entity	Date of Knowledge, Use, Sale, or Offer for Sale
Xilinx “Virtex” series of products, including, without limitation, Virtex-II, Virtex-II Pro, Virtex-II Pro X, Virtex-4, and Virtex-5	Xilinx	At least January 2001
Altera “Cyclone” series of products, including, without limitation, Cyclone (1 st gen.) and Cyclone II	Altera	At least 2003
Infineon DDR Mobile-RAM products, including, without limitation,	Infineon	At least 2002

¹ Infineon may subpoena one or more of these entities to obtain additional information on the system identified herein. To the extent those subpoenas result in the production of relevant documents or testimony, Infineon will supplement these Preliminary Invalidity Contentions as necessary.

Item	Person or Entity	Date of Knowledge, Use, Sale, or Offer for Sale
HYB18M512160AF-6, HYE18M512160AF-6, HYB18M512160AF-7.5, HYE18M512160AF-7.5, HYB18M512160AF-8, and HYE18M512160AF-8		

2. '381 Patent

Item	Person or Entity	Date of Knowledge, Use, Sale, or Offer for Sale
Samsung K9F Series (e.g., K9F1G08Q0A/ K9F1G08U0A) ("Samsung")	Samsung Electronics	At least May 2004
Spansion S25FL Series	Spansion LLC	At least Mar. 2005
Spansion S29NS-N Series	Spansion LLC	At least Apr. 2005
Hynix HY27UF084G2M Series ("Hynix")	Hynix	At least Dec. 2004

3. '028 Patent

Item	Person or Entity	Date of Knowledge, Use, Sale, or Offer for Sale
Micron MT28S4M16B1LL	Micron Technology, Inc.	At least May 2002
Hynix HY27UF084G2M Series	Hynix	At least Dec. 2004
Spansion S29NS-N Series	Spansion LLC	At least Apr. 2005
JESD79-2B	JEDEC Solid State Technology Association	At least Jan. 2005

III. CHARTS SETTING FORTH WHERE IN THE PRIOR ART REFERENCE EACH ELEMENT OF THE ASSERTED CLAIMS ARE FOUND

Exhibits A1 to C9 provide detailed claim charts showing where each claim element may be found in the prior art identified above. Each of these Exhibits is without prejudice to Infineon's indefiniteness positions under 35 U.S.C. § 112(b) and assume that such positions have been rejected by the Court. Nothing in the Exhibits should be taken as a concession that the claims are not indefinite.

Infineon relies on all portions and aspects of each item of prior art in support of Infineon's contention that such prior art satisfies each limitation of the Asserted Claims. Infineon has provided specific supporting citations to the prior art, but these citations do not necessarily represent every location, instance, or manner in which a particular claim limitation is satisfied by the prior art. Even where limitations are disclosed at multiple locations within a single item of prior art, Infineon has not necessarily identified every iteration of every such disclosure. Infineon therefore reserves the right to rely on additional, or different, portions/aspects of the prior art other than those specifically cited in the claim charts provided herewith.

For those references for which detailed claim charts are provided in the Exhibits, the Exhibit Number is listed next to the prior art reference in Section IV.A. Prior art references which are not associated with an Exhibit Number are additional prior art references that are pertinent to the invalidity of the Patents-in-Suit, either alone or in combination with other references. At this time, Infineon has not provided claim charts for each of these additional references, either because they are cited in conjunction with references for which charts have already been provided, are cited in these contentions, and/or because these references have similar disclosures to the prior art references for which invalidity charts have been provided and/or may be used to show the state of the art.

IV. INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

Exhibits A1 to C9 provide detailed claim charts showing where each claim element may be found in the prior art identified above. Each of these Exhibits is without prejudice to Infineon's indefiniteness positions under 35 U.S.C. § 112(b) and assume that such positions have been rejected by the Court. Nothing in the Exhibits should be taken as a concession that the claims are not indefinite.

The charts include both art that teaches each limitation according to MOSAID apparent construction of its claims based on its infringement contentions as well as art that teaches each limitation according to a proper understanding of the asserted claims. That Infineon has relied on MOSAID apparent constructions in mapping the exemplary teachings of the prior art to the limitations of the asserted claims does not mean that Infineon agrees with those interpretations. Infineon reserves the right to advocate for constructions of the asserted claims that limit them to their proper scope. Moreover, nothing in the asserted charts is an admission that any assertion expressly or impliedly made in MOSAID infringement contentions is correct. Infineon maintains that it does not infringe any asserted claim, and nothing in these charts discounts from that position.

Infineon relies on all portions and aspects of each item of prior art in support of Infineon's contention that such prior art satisfies each limitation of the Asserted Claims. Infineon has provided specific supporting citations to the prior art, but these citations do not necessarily represent every location, instance, or manner in which a particular claim limitation is satisfied by the prior art. Even where limitations are disclosed at multiple locations within a single item of prior art, Infineon has not necessarily identified every iteration of every such disclosure. Infineon therefore reserves the right to rely on additional, or different, portions/aspects of the prior art other than those specifically cited in the claim charts provided herewith.

For those references for which detailed claim charts are provided in the Exhibits, the Exhibit Number is listed next to the prior art reference in Section IV.A. Prior art references which are not associated with an Exhibit Number are additional prior art references that are pertinent to the invalidity of the Patents-in-Suit, either alone or in combination with other references. At this time, Infineon has not provided claim charts for each of these additional references, either because they are cited in conjunction with references for which charts have already been provided, are cited

in these contentions, and/or because these references have similar disclosures to the prior art references for which invalidity charts have been provided and/or may be used to show the state of the art.

Each of the prior art references identified below anticipates and/or renders obvious one or more of the Asserted Claims alone and/or when viewed in combination with other prior art references. Infineon's contentions that the references described in these Preliminary Invalidity Contentions, in various combinations, render the Asserted Claims obvious under 35 U.S.C. § 103 are in no way an admission or suggestion that each reference does not independently anticipate the Asserted Claims under 35 U.S.C. § 102. Furthermore, the specific combinations described in these Preliminary Invalidity Contentions are not intended to be exhaustive, as there are many possible combinations of these references, and it is not practical, particularly at this early stage before further factual investigation and claim construction proceedings, to identify and list all potentially relevant combinations. Infineon reserves the right to identify additional combinations in its final invalidity contentions, during expert discovery, and in later stages of the case.

Infineon provides additional information regarding these combinations below. Each of these exemplary combinations is listed for purposes of explaining and exemplifying which references would be combined under the motivations to combine described in the paragraphs below. These combinations are not intended to be exclusive or limiting but rather intended to provide notice of the reasoning behind the motivations to combine and the references that would be combined thereunder. In many instances, multiple different motivations would apply to a particular combination (for example, if multiple references were both authored by the same person and referred to the same product/system, then both of those motivations would apply) and the specific combinations were not duplicated.

Should any prior art cited above be deemed not to disclose, explicitly or inherently, any limitation of a claim, Infineon reserves the right to argue that any such difference between that prior art and the corresponding claim would have been obvious to one of ordinary skill in the art. To the extent that such an argument is deemed a “combination” analysis for purposes of obviousness, Infineon discloses its present intention to rely on the separate combination of the knowledge of a person of ordinary skill in the art with each item of prior art identified above. The knowledge of a person of ordinary skill in the art is demonstrated by the full list of references above, the prior art produced, the state of the art, and common sense.

1. '028 Patent

Ex. #	Reference
A-1	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 5,917,759
A-2	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 5,864,506
A-3	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 2006/0139068
A-4	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 7,221,617
A-5	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 2004/0148482
A-6	Invalidity of U.S. Pat. No. 10,140,028 in view of Hynix HY27UF084G2M
A-7	Invalidity of U.S. Pat. No. 10,140,028 in view of JESD79-2B
A-8	Invalidity of U.S. Pat. No. 10,140,028 in view of Micron MT28S4M16B1LL
A-9	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 2006/0023499
A-10	Invalidity of U.S. Pat. No. 10,140,028 in view of W.O. 2002/029581
A-11	Invalidity of U.S. Pat. No. 10,140,028 in view of Spansion S29NS-N
A-12	Invalidity of U.S. Pat. No. 10,140,028 in view of U.S. 6,654,307
A-13	Invalidity of U.S. Pat. No. 10,140,028 in view of Secondary References

2. '381 Patent

Ex. #	Reference
B-1	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 2004/0148482
B-2	Invalidity of U.S. Pat. No. 9,972,381 in view of Hynix HY27UF084G2M Series
B-3	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 7,831,794
B-4	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 6,570,791
B-5	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 2006/0023499
B-6	Invalidity of U.S. Pat. No. 9,972,381 in view of Samsung K9F1G08Q0A
B-7	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 7,376,020
B-8	Invalidity of U.S. Pat. No. 9,972,381 in view of Spansion S25FL System
B-9	Invalidity of U.S. Pat. No. 9,972,381 in view of Spansion S29NS-N and S72NS-N
B-10	Invalidity of U.S. Pat. No. 9,972,381 in view of U.S. 6,654,307
B-11	Invalidity of U.S. Pat. No. 9,972,381 in view of Secondary References

3. '393 Patent

Ex. #	Reference
C-1	Invalidity of 7,685,393 in view of Altera Cyclone
C-2	Invalidity of 7,685,393 in view of Infineon DDR Mobile-RAM Products
C-3	Invalidity of 7,685,393 in view of Kerl '350
C-4	Invalidity of 7,685,393 in view of LaBerge '345
C-5	Invalidity of 7,685,393 in view of Lawrence '253
C-6	Invalidity of 7,685,393 in view of Thomann '444
C-7	Invalidity of 7,685,393 in view of Xilinx Virtex
C-8	Invalidity of 7,685,393 in view of Zumkehr '225

Ex. #	Reference
C-9	Invalidity of 7,685,393 in view of Secondary References

B. Motivation to Combine

In general, a claimed invention is unpatentable if the differences between it and the prior art “are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.” 35 U.S.C. § 103(a); *Graham v. John Deere Co.*, 383 U.S. 1, 13-14 (1966). In view of the Supreme Court’s *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) (“KSR”) decision, the USPTO issued a set of Examination Guidelines setting forth a number of potential rationales for combining prior art references. See Examination Guidelines for Determining Obviousness under 35 U.S.C. § 103 in view of the Supreme Court Decision in *KSR*. Those rationales include:

- Combining prior-art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices (methods, or products) in the same way;
- Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;
- “Obvious to try”—choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market

forces if the variations would have been predictable to one of ordinary skill in the art; and

- Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art or to combine prior-art teachings to arrive at the claimed invention.

These rationales are consistent with the Supreme Court’s emphasis in *KSR* that “the results of ordinary innovation” from the perspective of a person of ordinary skill are not patentable, and further that “[a] person of ordinary skill is also a person of ordinary creativity, not an automaton.” 550 U.S. at 421. Infineon contends that one or more of these rationales apply in considering the obviousness of the Asserted Claims.

For example, a person of ordinary skill in the art at the time of the alleged invention of each of the Patents-in-Suit would have been motivated to combine or adapt known or familiar methods in the art, especially where market forces prompted such variations. Moreover, each of the above-identified references describes methods that were known to offer improvements and benefits to the art, and, accordingly, one of skill in the art would have been motivated to combine or modify the references as identified in each of the combinations above.

Furthermore, since there were a finite number of predictable solutions, a person of ordinary skill in the art had a good reason to pursue the known options. The above-identified prior art references merely use those familiar elements for their primary or well-known purpose in a manner well within the ordinary level of skill in the art. Accordingly, common sense and the knowledge of the prior art render the claims invalid under Section 102 or Section 103.

A person of ordinary skill would also have been motivated to combine the above prior art based on his/her knowledge, the nature of the problem to be solved, and the teachings of the prior

at. The identified prior art addresses the same or similar technical issues and suggests the same or similar solutions to those issues. Moreover, some of the prior art refer to or discuss other prior art, illustrating the close technical relationship among the prior art. As one example, the references listed above are directed to the same or similar technology.

One of skill in the art would have been further motivated to look at all of the available documentation for a particular product/system to understand the operation. One of skill in the art would have combined that knowledge from the various related references because it would be clear that the references were related. For at least this reason, one of skill in the art could consider it obvious to combine the references that collectively teach a product or system. The references were identified in the charts for each such system/product, and Infineon intends to rely upon the combination of references in each of the system/product charts.

One of skill in the art would have been further motivated to combine the different publications and patents that were authored by employees of the company or assigned to the same assignee and related to the same subject matter.

One of skill in the art would have been further motivated to combine different references that were authored, developed, or invented by the same individual(s) related to the same subject matter. The common inventor/author/architect references themselves demonstrate that they relate to continued work in a common field of effort and continued related developments in that field. One of skill in the art would, therefore, combine the references related to each individual. Similarly, based on the teachings of the references and/or the knowledge of one of ordinary skill, one of skill in the art would have been further motivated to combine different references from the same company.

Finally, as explained below and in the attached charts, all concepts recited in the Asserted Claims of the Patents-in-Suit represent well-known techniques and apparatuses. Thus, the Asserted Claims of the Patents-in-Suit are invalid under 35 U.S.C. § 103 because they do nothing more than combine known techniques and apparatuses according to their known and ordinary uses to yield predictable results.

1. '393 Patent

(a) Single Sample References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a method for controlling a synchronous memory in which the read data path delay between the memory and the memory controller is determined using a single initialization sample, such a reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Single Sample References”) to render obvious claims that may require such or similar features.

- Manabe '167
- Stark '922
- Jeddeloh '752
- Millar '760
- Zumkehr '225
- Matsui '192
- Xilinx Virtex

A person of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above Single Sample References to improve the function and utility of the system, and such a

combination would have been within that person's skill. As shown in the teachings of the foregoing Single Sample References, designing memories and memory controllers configured to determine a read data path delay based on a single initialization sample—or a single read operation—was well known in the art by the time of the '393 Patent's alleged invention. Combining an anticipatory reference or exemplary combination with any one of the above Single Sample References would have amounted to applying a known technique to a known device ready for improvement, yielding predictable results. Furthermore, given the design needs (e.g., designing synchronous memories and memory controllers configured to determine a read data path delay based on a single initialization sample) and the finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to make such a combination.

(b) Look Up References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a method for controlling a synchronous memory in which the initialization sequence is used to determine the read delay between the memory and the memory controller by looking up the read delay stored for the initialization sequence, such a reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Look Up References") to render obvious claims that may require such or similar features.

- Stark '922
- Manabe '167
- Nishikawa '842
- Johnson '378
- Zumkehr '225
- Thomann '444

- Xilinx Virtex

A person of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above Look Up References to improve the function and utility of the system, and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Look Up References, designing memories and memory controllers configured to determine the read delay between the memory and the memory controller by looking up the read delay stored for the initialization sequence using the initialization sequence was well known in the art by the time of the '393 Patent's alleged invention. Combining an anticipatory reference or exemplary combination with any one of the above Look Up References would have amounted to applying a known technique to a known device ready for improvement, yielding predictable results. Furthermore, given the design needs (e.g., designing memories and memory controllers configured to determine the read delay between the memory and the memory controller by looking up the read delay stored for the initialization sequence using the initialization sequence) and the finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to make such a combination.

(c) Ongoing Update Read Delay References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a method for controlling a synchronous memory in which the read delay is updated upon detecting clock drift (e.g., due to PVT variations), such a reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Ongoing Update Read Delay References") to render obvious claims that may require such or similar features.

- LaBerge '345
- Manabe '167
- Matsui '192
- Johnson '378
- Thomann '444
- Kerl '350
- Xilinx Virtex
- Altera Cyclone

A person of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above Ongoing Update Read Delay References to improve the function and utility of the system, and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Ongoing Update Read Delay References, designing memory controllers configured to control a synchronous memory in which the read delay is updated upon detecting clock drift was well known in the art by the time of the '393 Patent's alleged invention. Combining an anticipatory reference or exemplary combination with any one of the above Ongoing Update Read Delay References would have amounted to applying a known technique to a known device ready for improvement, yielding predictable results. Furthermore, given the design needs (e.g., designing memories and memory controllers configured to control a synchronous memory in which the read delay is updated upon detecting clock drift) and the finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to make such a combination.

(d) Writing To Predetermined Locations References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a method for controlling a synchronous memory in which the read delay is updated upon detecting clock drift (e.g., due to PVT variations), such a reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Writing To Predetermined Locations References”) to render obvious claims that may require such or similar features.

- Zumkehr '225
- Thomann '444
- Lawrence '253
- Matsui '192
- Manabe '167
- Johnson '378
- Nishikawa '842
- Xilinx Virtex
- Altera Cyclone
- Infineon DDR Mobile-RAM

A person of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above Writing To Predetermined Locations References to improve the function and utility of the system, and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Writing To Predetermined Locations References, designing memory controllers which write an initialization sequence to predetermined locations of the memory was well known

in the art by the time of the '393 Patent's alleged invention. Combining an anticipatory reference or exemplary combination with any one of the above Writing To Predetermined Locations References would have amounted to applying a known technique to a known device ready for improvement, yielding predictable results. Furthermore, given the design needs (e.g., designing memory controllers which write an initialization sequence to predetermined locations of the memory) and the finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to make such a combination.

(e) Sampling Returned Data Signals References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a method for controlling a synchronous memory in which a predetermined time after sending the read command, the memory controller samples the returned data signals to produce a single initialization sample, such a reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Sampling Returned Data Signals") to render obvious claims that may require such or similar features.

- Matsui '192
- Millar '760
- Johnson '378
- Zumkehr '225
- Manabe '167
- Johnson '378
- Xilinx Virtex
- Altera Cyclone
- Infineon DDR Mobile-RAM

A person of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above Sampling Returned Data Signals References to improve the function and utility of the system, and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Sampling Returned Data Signals References, designing memory controllers which write controlling a synchronous memory in which a predetermined time after sending the read command, was well known in the art by the time of the '393 Patent's alleged invention. Combining an anticipatory reference or exemplary combination with any one of the above Sampling Returned Data Signals References would have amounted to applying a known technique to a known device ready for improvement, yielding predictable results. Furthermore, given the design needs (e.g., designing memory controllers which write an initialization sequence to predetermined locations of the memory) and the finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to make such a combination.

2. '381 Patent

(a) Flash Memory References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a flash memory comprising a plurality of erasable blocks, each erasable block comprising a plurality of pages, each page comprising a plurality of flash memory cells, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Flash Memory References") to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273

- Garrett '005
- Ito '794
- Roohparvar '791
- Roohparvar '909
- Ryu '499
- Samsung
- Sorrells '020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop '431
- Widmer '307
- Hynix
- Jigour '900
- Roohparvar '270

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Flash Memory References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Flash Memory References, designing non-volatile memory systems using flash memory techniques was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Flash Memory References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design

needs—*e.g.*, designing non-volatile memory systems such that computer systems could have memory stored despite losing power to the system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(b) Clock Input References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a clock input port configured to receive a clock signal, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Clock Input References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Ryu ’499
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop ’431
- Widmer ’307
- Hynix
- Jigour ’900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Clock Input References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Clock Input References, designing a clock input port was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Clock Input References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, synchronizing memory system operations—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(c) Common Data Interface References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose at least one common data interface configured to transfer command data, address data, input data and output data, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Common Data Interface References") to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273
- Garrett '005
- Ito '794
- Roohparvar '791

- Ryu '499
- Samsung
- Sorrells '020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop '431
- Widmer '307
- Hynix
- Jigour '900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Common Data Interface References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Common Data Interface References, designing ports and busses for transferring data of various kinds in a single memory system was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Common Data Interface References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, transferring command, address, and input/output data while minimizing the number of ports on a device—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(d) Double-Data Rate References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose command data, address data, input data and output data being transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Double-Data Rate References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Ryu ’499
- Widmer ’307

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Double-Data Rate References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Double-Data Rate References, designing data transfer systems that operate on both the rising and falling edge of a clock signal was well-known in the art by the time of the ’381 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Double-Data Rate References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore,

given the design needs—*e.g.*, transferring more data without increasing the operating frequency of the system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(e) Control Signal References²

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a control input port configured to receive a control signal wherein a transition of the control signal from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Control Signal References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Conley ’273
- Roohparvar ’791
- Ryu ’499
- Samsung
- Spansion S25FL
- Spansion S29NS-N
- Waldrop ’431

² Plaintiff accuses a chip-select signal and port of being a control signal and port, respectively, in its infringement contentions. Defendants maintain that the accused chip-select signal and port are not a control signal and port. Although Defendants do not concede or adopt Plaintiff’s point of view, Plaintiff also cannot credibly challenge a mapping of the control signal and port limitations to the prior art’s disclosure of chip-select or chip-enable ports and signals. Any identification of chip-select or chip-enable limitations in Defendants’ invalidity contentions or prior art charts is not an admission that chip-select or chip-enable signals or ports are control signals or ports.

- Widmer '307
- Hynix
- Jigour '900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Control Signal References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Control Signal References, designing a port that indicates when command data is being sent to a memory device was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Control Signal References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, indicating the type of data being sent to a device to ensure that it is latched into the proper register and/or utilized appropriately—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(f) Page Program and Read References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose control circuitry configured to execute a page program operation to store the input data on a selected page and to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface, such reference can be combined with the corresponding disclosures from

any one or more of the following prior art references (“Page Program and Read References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Conley ’273
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Roohparvar ’909
- Ryu ’499
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop ’431
- Widmer ’307
- Hynix
- Jigour ’900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Page Program and Read References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Page Program and Read References, designing memory devices with circuitry that is

capable of both reading and writing (i.e., programming) from their memory arrays was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Page Program and Read References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, the need to both store and retrieve data from the memory arrays of a device—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(g) Status Register References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a status register configured to indicate a status of the flash memory device, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Status Register References”) to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273
- Garrett '005
- Ito '794
- Roohparvar '791
- Ryu '499
- Samsung
- Sorrells '020

- Spansion S25FL
- Spansion S29NS-N
- Hynix
- Jigour '900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Status Register References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Status Register References, designing registers that can indicate the status of a memory device (e.g., operations being performed, whether the last operation was successful, whether the device is ready to perform another operation) was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Status Register References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, ensuring that a device is in the proper state and capable of beginning an operation, whether that be read, write, program, reading and writing, resetting, erasing, or otherwise—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(h) Latching Command Data References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose command data being latched at the first rising edge of the clock signal after the transition of the control signal, such reference can be combined with the corresponding disclosures

from any one or more of the following prior art references (“Latching Command Data References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Latching Command Data References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Latching Command Data References, designing latching command data after receiving an indication from the control signal that command data was imminent was well-known in the art by the time of the ’381 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Latching Command Data References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, minimizing the wasted clock cycles in between an indication that command data was coming and processing

said command data—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(i) Page Program Result References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose the status register is further configured to provide a result of the page program operation after the page program operation is completed, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Page Program Result References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Ito ’794
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Page Program Result References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Page Program Result References, designing a status register that indicates when a page program operation was successful and that the device can perform its next operation was well-known in the art by the time of the ’381 Patent’s claimed invention. Combining an anticipatory

reference or exemplary combination with any one of the above exemplary Page Program Result References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, a system that indicates when it has completed operations and is ready to begin another operation—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(j) Clock Output Port References³

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a clock output port configured to transmit a clock output signal synchronized with the output data when the flash memory device is in the double data rate configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Clock Output Port References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Ryu ’499
- Samsung

³ Plaintiff accuses a data strobe of being a clock in its infringement contentions. Defendants maintain that a data strobe is not an output clock. Although Defendants do not concede or adopt Plaintiff’s point of view, Plaintiff also cannot credibly challenge a mapping of the output clock limitations to the prior art’s disclosure of data strobe ports and signals. Any identification of such limitations in Defendants’ invalidity contentions or prior art charts are not admissions that a data strobe is an output clock.

- Sorrells '020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop '431
- Widmer '307

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Clock Output Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Clock Output Port References, designing a memory device with a port that outputs a clock signal was well-known in the art by the time of the '381 Patent's claimed invention. Even if the foregoing references do not disclose a clock output port (and instead disclose a data strobe), designing a memory system with a clock signal still would have been obvious given the benefits from converting an intermittent strobe into a continuous clock signal to synchronize memory operations. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Clock Output Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, synchronizing memory operations across multiple memory devices in series or a cascading fashion—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(k) Delay Lock Loop References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a delay lock loop (DLL) to synchronize the clock output signal with the clock signal, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Delay Lock Loop References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Ryu ’499
- Waldrop ’431

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Delay Lock Loop References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Delay Lock Loop References, designing a delay system to control the offset timing of a memory device was well-known in the art by the time of the ’381 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Delay Lock Loop References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, accommodating the delays inherent in timing from a signal being processed in a memory device—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(l) End of Transfer Signal References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a transition of the control signal from the active state to the inactive state indicates

an end of the transfer of the at least one of command data, address data, input data and output data, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“End of Transfer Signal References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Conley ’273
- Garrett ’005
- Ito ’794
- Roohparvar ’791
- Roohparvar ’909
- Ryu ’499
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Waldrop ’431
- Widmer ’307
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary End of Transfer Signal References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the

foregoing End of Transfer Signal References, designing a control signal that transitions at the conclusion of a data transfer process was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary End of Transfer Signal References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, communicating to a memory device that the transfer of data to is ending—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(m) NOR Flash Memory

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a system wherein the flash memory device is a NOR flash memory device, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“NOR Flash References”) to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273
- Ito '794
- Roohparvar '909
- Ryu '499
- Sorrells '020
- Widmer '307
- Jigour '900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary NOR Flash References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing NOR Flash References, designing flash memory systems with NOR flash memory was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary NOR Flash References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, enabling fast, random-access reads, direct code execution reads, or otherwise high reliability reads—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(n) Single- and Multi-Level Cell References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose the flash memory cell is a single-level-cell or a multi-level-cell, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Single- and Multi-Level Cell References”) to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273
- Ito '794
- Roohparvar '909

- Ryu '499
- Sorrells '020
- Widmer '307
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Single- and Multi-Level Cell References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Single- and Multi-Level Cell References, designing flash memory cells that can store one or more bits per cell was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Single- and Multi-Level Cell References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, prioritizing maximum endurance, fastest performance, and highest reliability (single-level cell) memory devices or prioritizing higher storage density and lower cost per bit for consumer or data-centric applications (multi-level cell)—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(o) Multi-/Single-Bit Serial I/O References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the at least one common data interface comprises multi-bit serial data input and output, such reference can be combined with the corresponding disclosures

from any one or more of the following prior art references (“Multi-/Single-Bit Serial I/O References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Kilbuck ’091
- Garrett ’005
- Ito ’794
- Samsung
- Sorrells ’020
- Spansion S25FL
- Spansion S29NS-N
- Hynix
- Jigour ’900

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Multi-/Single-Bit Serial I/O References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Multi-/Single-Bit Serial I/O References, designing a system that minimizes the number of serial I/O references or uses several was well-known in the art by the time of the ’381 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Multi-/Single-Bit Serial I/O References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, minimizing the number of physical ports on a device, including minimizing it to a single port—combined with a finite number of identified, predictable

solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(p) Read While Write References⁴

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the control circuitry is configured to perform the read operation during a time period that overlaps with a time period for the page program operation, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Read While Write References References”) to render obvious claims that may require such or similar features.

- Grundy ’482
- Conley ’273
- Ito ’794
- Spansion S25FL
- Spansion S29NS-N
- Widmer ’307

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Read While Write References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the

⁴ Plaintiff accuses program, suspend, and resume operations in its infringement contentions. Defendants maintain that the accused features do not amount to an “overlap[]” in time periods as recited by the claims. Although Defendants do not concede or adopt Plaintiff’s point of view, Plaintiff also cannot credibly challenge a mapping of this limitation to the prior art’s disclosure of program, suspend, and resume operations. Any identification of such limitations in Defendants’ invalidity contentions or prior art charts is not an admission that program, suspend, and resume operations satisfy this limitation.

foregoing Read While Write References, designing a system that can perform simultaneous operations was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Read While Write References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, maximizing efficiency by performing as many operations in a period of time as possible—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(q) Reset Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a second control input port configured to receive a reset signal, wherein the status register is configured to be reset when the reset signal is received at the second control input port, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Reset Port References”) to render obvious claims that may require such or similar features.

- Grundy '482
- Ito '794
- Ryu '499
- Sorrells '020
- Spansion S29NS-N
- Widmer '307
- Roohparvar '270

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Reset Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Reset Port References, designing a port that can receive a reset signal was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Reset Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, having a port capable of resetting the status register and other device operations upon interruption or other errors—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(r) Error Correcting Code References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose error correcting code (ECC) configured to be utilized during the page program operation, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Error Correcting Code References”) to render obvious claims that may require such or similar features.

- Grundy '482
- Kilbuck '091
- Conley '273
- Garrett '005
- Roohparvar '909

- Samsung
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Error Correcting Code References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Error Correcting Code References, designing systems that (when information is stored or sent) are capable of spotting mistakes and, in many cases, automatically fix them was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Error Correcting Code References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, ensuring data integrity in environments where stored or transmitted bits may get flipped or corrupted—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(s) Internal Verification References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose control circuitry is configured to automate the page program operation including an internal verification, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Internal Verification References”) to render obvious claims that may require such or similar features.

- Kilbuck '091
- Conley '273

- Roohparvar '909
- Samsung
- Sorrells '020
- Spansion S29NS-N
- Hynix

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Internal Verification References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Internal Verification References, designing systems that, after programming or erasing data, read back the previously written data to confirm it matches the intended values was well-known in the art by the time of the '381 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Internal Verification References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, guaranteeing that every program or erase operation actually succeeded before the system moves on—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

3. '028 Patent

(a) Non-Volatile Memory Device References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a non-volatile memory device with a plurality of non-volatile memory blocks, such reference can be combined with the corresponding disclosures from any one or more of the

following prior art references (“Non-Volatile Memory Device References”) to render obvious claims that may require such or similar features.

- Ryu ’499
- Widmer ’307
- Flach ’617
- Roohparvar ’791
- Cole ’068
- Hynix
- Grundy ’482
- Spansion S29NS-N
- Smith ’581
- Arcoleo ’506
- Ito ’794
- Micron
- Waldrop ’804
- Kilbuck ’091
- Roohparvar ’270

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Non-Volatile Memory Device References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Non-Volatile Memory Device References, designing non-volatile memory devices was well-known in the art by the time of the ’028 Patent’s claimed invention. Combining

an anticipatory reference or exemplary combination with any one of the above exemplary Non-Volatile Memory Device References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, designing non-volatile memory systems such that computer systems could have memory stored despite losing power to the system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(b) Chip Enable Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Chip Enable Port References”) to render obvious claims that may require such or similar features.

- Ryu '499
- Widmer '307
- Roohparvar '791
- Hynix
- Grundy '482
- JESD79-2B
- Spansion S29NS-N
- Ito '794
- Micron
- Roohparvar '270

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Chip Enable Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Chip Enable Port References, designing a port on a memory device that turns on the chip's internal circuitry was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Chip Enable Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, having a way of turning memory chips on in a system with serially connected memory chips—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(c) Clock Output Port References⁵

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Clock Output Port References") to render obvious claims that may require such or similar features.

- Ryu '499

⁵ Plaintiff accuses a data strobe of being a clock in its infringement contentions. Defendants maintain that a data strobe is not an output clock. Although Defendants do not concede or adopt Plaintiff's point of view, Plaintiff also cannot credibly challenge a mapping of the output clock limitations to the prior art's disclosure of data strobe ports and signals. Any identification of such limitations in Defendants' invalidity contentions or prior art charts are not admissions that a data strobe is an output clock.

- Widmer '307
- Roohparvar '791
- Hynix
- Grundy '482
- JESD79-2B
- Smith '581
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Clock Output Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Clock Output Port References, designing a memory device with a port that outputs a clock signal was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Clock Output Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, synchronizing memory operations across multiple memory devices in series or a cascading fashion—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(d) Configurable Clock Input Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose first and second clock input ports, and a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling

configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Configurable Clock Input Port References”) to render obvious claims that may require such or similar features.

- Flach ’617
- Cole ’068
- Smith ’581

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Configurable Clock Input Port References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Configurable Clock Input Port References, designing clock inputs that can operate in a single-ended configuration and a differential-signaling configuration was well-known in the art by the time of the ’028 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Configurable Clock Input Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, creating memory devices that are backward compatible with earlier memory standards or deploying disparate memory devices in a single memory system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(e) Common Data Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose one or more common data ports configured to transfer common data signals

carrying at least one of command data, address data, input data and output data, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Common Data Port References”) to render obvious claims that may require such or similar features.

- Ryu ’499
- Widmer ’307
- Flach ’617
- Roohparvar ’791
- Hynix
- Grundy ’482
- JESD79-2B
- Spansion S29NS-N
- Ito ’794
- Micron
- Kilbuck ’091
- Roohparvar ’270
- Sorrells ’020
- Garrett ’005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Common Data Port References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Common Data Port References, designing ports and busses for transferring data of

various kinds in a single memory system was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Common Data Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, transferring command, address, and input/output data while minimizing the number of ports on a device—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(f) Page Program and Read References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and output data to be retrievable from the one of the plurality of non-volatile memory blocks, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Page Program and Read References”) to render obvious claims that may require such or similar features.

- Ryu '499
- Widmer '307
- Flach '617
- Roohparvar '791
- Hynix
- Grundy '482
- JESD79-2B

- Spansion S29NS-N
- Ito '794
- Micron
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Page Program and Read References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Page Program and Read References, designing memory devices with circuitry that is capable of both reading and writing (i.e., programming) from their memory arrays was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Page Program and Read References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, the need to both store and retrieve data from the memory arrays of a device—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(g) Variable Drive Strength Output Buffer References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, such reference can be combined with the corresponding disclosures from

any one or more of the following prior art references (“Variable Drive Strength Output Buffer References”) to render obvious claims that may require such or similar features.

- Widmer ’307
- Grundy ’482
- JESD79-2B
- Spansion S29NS-N
- Arcoleo ’506
- Waldrop ’804
- Chun ’683

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Variable Drive Strength Output Buffer References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Variable Drive Strength Output Buffer References, designing output buffers that can operate with various output buffer drive strengths was well-known in the art by the time of the ’028 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Variable Drive Strength Output Buffer References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, changing the output buffer drive strength to ensure compatibility in different signaling environments, ensure backwards compatibility with earlier standards, and maximizing power efficiency in different system deployments—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(h) Double-Data Rate References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose the output data synchronized with the clock output signal in a double data rate configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Double-Data Rate References”) to render obvious claims that may require such or similar features.

- Ryu ’499
- Widmer ’307
- Flach ’617
- Roohparvar ’791
- Grundy ’482
- JESD79-2B
- Smith ’581
- Ito ’794
- Garrett ’005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Double-Data Rate References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Double-Data Rate References, designing data transfer systems that operate on both the rising and falling edge of a clock signal was well-known in the art by the time of the ’028 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Double-Data Rate References would have amounted to applying a known

technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, transferring more data without increasing the operating frequency of the system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(i) Differential Clock Signal References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose use of two clock signals, including clock signals wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Differential Clock Signal References”) to render obvious claims that may require such or similar features.

- Widmer ’307
- Flach ’617
- Roohparvar ’791
- Cole ’068
- Grundy ’482
- JESD79-2B
- Smith ’581

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Differential Clock Signal References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Differential Clock Signal References, designing memory systems with two clock

signals, where one is positive and the other is negative (an inverse of the positive) was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Differential Clock Signal References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, ensuring signal integrity by reducing noise and interference and allowing faster, more reliable data transfer—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(j) Data Latching Clock Signal References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose clock signals wherein the first clock input signal and the second clock input signal are data latching clock signals, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Data Latching Clock Signal References”) to render obvious claims that may require such or similar features.

- Widmer '307
- Roohparvar '791
- Cole '068
- Grundy '482
- JESD79-2B
- Spansion S29NS-N
- Smith '581
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Data Latching Clock Signal References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Data Latching Clock Signal References, designing systems that latch data on the edges of clock signals (both rising and falling edges) was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Data Latching Clock Signal References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, operating memory systems with a precise, predictable alignment between incoming data and the moment it is recorded—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(k) One-Bit Data Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose common data ports wherein each of the one or more common data ports comprises 1 bit, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“One-Bit Data Port References”) to render obvious claims that may require such or similar features.

- Widmer '307
- Roohparvar '791
- Hynix
- Grundy '482

- Spansion S29NS-N
- Smith '581
- Ito '794
- Micron
- Kilbuck '091
- Roohparvar '270
- Sorrells '020
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary One-Bit Data Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing One-Bit Data Port References, designing a system that minimizes the number of serial I/O references or uses several was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary One-Bit Data Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, minimizing the number of physical ports on a device, including minimizing it to a single port—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(I) Terminated Data Signal References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose signaling configurations wherein the first clock input signal, the second clock input signal and the common data signal are terminated signals, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Terminated Data Signal References”) to render obvious claims that may require such or similar features.

- Ryu '499
- Cole '068
- Grundy '482
- JESD79-2B
- Waldrop '804
- Akashi '759
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Terminated Data Signal References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Terminated Data Signal References, designing signal lines that include a resist, an impedance matching element, or some other method of terminating clock and data signals was well-known in the art by the time of the '028 Patent’s claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Terminated Data Signal References would have amounted to applying a known technique to a known device

ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, preventing electrical reflections that can distort the signal and maintaining signal integrity over high-speed interconnects to ensure accurate data transmission—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(m) Clock Buffer Configuration Register References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Clock Buffer Configuration Register References”) to render obvious claims that may require such or similar features.

- Flach ’617
- Cole ’068
- Smith ’581

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Clock Buffer Configuration Register References to improve the function and utility of the same and such a combination would have been within that person’s skill. As shown in the teachings of the foregoing Clock Buffer Configuration Register References, designing registers to store configuration data like clock input buffer configurations was well-known in the art by the time of the ’028 Patent’s claimed invention. Combining an anticipatory reference or exemplary

combination with any one of the above exemplary Clock Buffer Configuration Register References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, storing various clock configurations to align the system with older standards (*i.e.*, backwards compatibility) or the needs of a particular system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(n) Drive Strength Configuration Register References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Drive Strength Configuration Register References”) to render obvious claims that may require such or similar features.

- Widmer ’307
- Grundy ’482
- JESD79-2B
- Arcoleo ’506
- Ito ’794
- Micron
- Waldrop ’804
- Chun ’683

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above

exemplary Drive Strength Configuration Register References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Drive Strength Configuration Register References, designing registers to store configuration data like drive strength configurations was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Drive Strength Configuration Register References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, storing various drive strength configurations to align the system with older standards (*i.e.*, backwards compatibility) or the needs of a particular system —combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(o) Edge-Aligned Output Data References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the output data is edge aligned with the clock output signal, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Edge-Aligned Output Data References”) to render obvious claims that may require such or similar features.

- Widmer '307
- Roohparvar '791
- Cole '068
- Grundy '482
- Garrett '005

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Edge-Aligned Output Data References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Edge-Aligned Output Data References, designing outputting data so that it is edge aligned with the clock output (or at the very least, data strobe outputs that would have rendered clock outputs obvious) was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Edge-Aligned Output Data References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, operating memory systems with a precise, predictable alignment between outgoing data and the moment it is read—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(p) Reset Port References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a reset port configured to receive a reset signal for resetting the configurable non-volatile memory device to a default configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Reset Port References”) to render obvious claims that may require such or similar features.

- Ryu '499
- Widmer '307
- Roohparvar '791

- Cole '068
- Grundy '482
- Spansion S29NS-N
- Roohparvar '270

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Reset Port References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Reset Port References, designing a port that can receive a reset signal was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Reset Port References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, having a port capable of resetting the status register and other device operations upon interruption or other errors—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(q) Default Single-Ended Configuration References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the default configuration comprises the single ended signaling configuration, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“Default Single-Ended Configuration References”) to render obvious claims that may require such or similar features.

- Flach '617

- Cole '068
- Smith '581

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Default Single-Ended Configuration References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Default Single-Ended Configuration References, designing memory systems that default to single-ended mode was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Default Single-Ended Configuration References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, designing a system that can work with older standards and systems as well as newer ones or more complex ones—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(r) Flash Memory References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the configurable non-volatile memory device is a flash Memory device, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references ("Flash Memory References") to render obvious claims that may require such or similar features.

- Ryu '499
- Widmer '307

- Roohparvar '791
- Hynix
- Grundy '482
- Spansion S29NS-N
- Arcoleo '506
- Ito '794
- Micron
- Kilbuck '091

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary Flash Memory References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing Flash Memory References, designing non-volatile memory systems using flash memory techniques was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary Flash Memory References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, designing non-volatile memory systems such that computer systems could have memory stored despite losing power to the system—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

(s) NOR Flash Memory References

To the extent MOSAID contends that an anticipatory reference or exemplary combination fails to disclose a memory device wherein the configurable non-volatile memory device is a NOR flash memory device, such reference can be combined with the corresponding disclosures from any one or more of the following prior art references (“NOR Flash Memory References”) to render obvious claims that may require such or similar features.

- Ryu '499
- Widmer '307
- Flach '617
- Roohparvar '791
- Cole '068
- Hynix
- Grundy '482
- JESD79-2B
- Spansion S29NS-N
- Smith '581
- Arcoleo '506
- Ito '794
- Micron
- Waldrop '804
- Chun '683
- Akashi '759
- Kilbuck '091

One of ordinary skill in the art would have been motivated to combine any one or more of the anticipatory references or exemplary combinations with any one or more of the above exemplary NOR Flash Memory References to improve the function and utility of the same and such a combination would have been within that person's skill. As shown in the teachings of the foregoing NOR Flash Memory References, designing flash memory systems with NOR flash memory was well-known in the art by the time of the '028 Patent's claimed invention. Combining an anticipatory reference or exemplary combination with any one of the above exemplary NOR Flash Memory References would have amounted to applying a known technique to a known device ready for improvement to yield predictable results. Furthermore, given the design needs—*e.g.*, enabling fast, random-access reads, direct code execution reads, or otherwise high reliability reads—combined with a finite number of identified, predictable solutions, a person of ordinary skill in the art would have been motivated to combine the teachings of these references.

V. INVALIDITY UNDER 35 U.S.C. § 112

A. Indefiniteness

Section 112(b) includes a definiteness requirement: “[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.” 35 U.S.C. § 112(b). “[A] patent is invalid for indefiniteness if its claims, read in light of the patent's specification and prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014).

The definiteness requirement requires that the claim must set forth what the applicant regards as the invention and do so with sufficient particularity and definiteness. *Allen Eng'g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002). Where it would be apparent to one of skill

in the art, based on the patent specification, that the “invention” set forth in a claim is not what the patent applicant regarded as the invention, the claim is invalid. *Id.*

Based on Infineon’s present understanding of the Asserted Claims and MOSAID’s apparent interpretation of these claims as reflected in its Preliminary Infringement Contentions, the following limitations of the Asserted Claims fail to satisfy the requirements of § 112(b) because the precise scope of at least the terms listed below cannot be determined with reasonable certainty by a POSITA when reading the claims in light of the specification and prosecution history.

1. ’393 Patent

- “[A] single initialization sample” (Claim 1). The ’393 Patent specification does not explain what the term “single” in this phrase means or how it applies in the context of the disclosed embodiments. The specification describes generating an “initialization sample” by sampling multiple latches (*see, e.g.*, ’393 Patent at 7:6-24), and also states that the same technique can be applied to a system using an iterative approach (*see, e.g.*, ’393 Patent at Abstract, 4-16-24). When an iterative approach is used, the resulting “initialization sample” is obtained over multiple iterations rather than in one capture event, and thus would not be “single” under the plain meaning of that term. The absence of any guidance as to what “single” refers to in such context leaves a POSITA without reasonable certainty as to the scope of the claim.
- “[A]n expected initialization sample” (Claim 9). The term “expected initialization sample” does not appear anywhere in the ’393 Patent specification and is not a recognized term of art. The claim and specification provide no explanation of what makes a sample “expected,” how such an expectation is generated, or in what form it

is stored. As a result, a POSITA would lack reasonable certainty as to the scope of this term.

2. '381 Patent

- “[C]ommon data interface” (Claims 1, 11, 12, 17). A POSITA lacks reasonable certainty as to the scope of these claims. The term “common data interface” is not used nor defined in the specification, and this does not appear to be a common term of art that had accepted boundaries in the field at the time of invention. Though interfaces for sending data are referenced in the specification multiple times, it is ambiguous to which kind of interface or interfaces the term “common data interface” refers.

3. '028 Patent

- “[C]ommon data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data.” (Claims 1, 4, 8). A POSITA lacks reasonable certainty as to the scope of these claims. The terms “common data interface” and “common data signals” are not used nor defined in the specification, and they do not appear to be a common term of art that had accepted boundaries in the field at the time of invention. Though ports for sending data are referenced in the specification multiple times, it is ambiguous to which kind of port or ports the term “common data ports” refers. Similarly, though data signals are referenced multiple times throughout the specification, it is ambiguous to which kinds of signals the term “common data signals” refers. Finally, it is ambiguous whether the “common data signals” carry all of the command, address, input, and output in a single signal, or if they need only carry some of this data in a given signal.
- “The configurable non-volatile memory device as claimed in claim 1, wherein each of the one or more common data ports comprises 1 bit.” (Claim 4). A POSITA lacks

reasonable certainty as to the scope of this claim. It is unclear how a “common data port[]” can “comprise[] 1 bit.” A port is a physical structure that cannot store data, and a bit is a measure of data. Given that POSITAs generally understand “comprise” to mean “includes at least” in the context of patent claims, it is unclear how a physical structure that cannot store data would include at least one bit of data. Therefore, a POSITA lacks reasonable certainty as to the scope of this claim.

B. Written Description

35 U.S.C. § 112 includes a written description requirement: “The specification shall contain a written description of the invention” 35 U.S.C. § 112(a). “To satisfy the written description requirement, a patent applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention.” *ICU Medical Inc. v. Alaris Medical Systems, Inc.*, 558 F.3d 1368, 1377 (Fed. Cir. 2009) (internal quotation marks and citations omitted); *see also Synthes USA, LLC v. Spinal Kinetics, Inc.*, 734 F.3d 1332, 1340 (Fed. Cir. 2013). “The test [for written description support] requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art. Based on that inquiry, the specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (*en banc*).

The specification must describe the claimed invention in sufficient detail so that a POSITA can recognize what is claimed. “The appearance of mere indistinct words in a specification or a claim, even an original claim, does not necessarily satisfy that requirement.” *University of Rochester v. G.D. Searle & Co.*, 358 F.3d 916, 923 (Fed. Cir. 2004) (internal quotation marks and citations omitted).

Based on Infineon's present understanding of the Asserted Claims and MOSAID's apparent interpretation of these claims as reflected in its Preliminary Infringement Contentions, the following limitations of the Asserted Claims fail to satisfy the requirements of Section 112 for at least the following limitations:

1. '393 Patent

- “[A] read data path delay between the memory and a memory controller” (Claim 1). The '393 Patent specification never uses or defines “read data path delay.” Instead, it refers to “loop-around delay” and “read delay.” To the extent MOSAID argues that the claimed “read data path delay between the memory and a memory controller” denotes only the data read portion of that timing (i.e., from the memory to the controller), the specification does not demonstrate possession of that subject matter.
- “[F]or each of a plurality of read delays, storing an expected initialization sample” (Claim 9). The phrase “expected initialization sample” does not appear anywhere in the '393 Patent specification. The disclosure does not explain what such an “expected” sample is, who or what generates the expectation, or how such a sample is determined or stored.

2. '381 Patent

- “[D]ouble data rate configuration.” (Claims 1, 4, 17, 19). The written description does not show that the applicant was in possession of a configurable memory device with respect to data latching. The written description does not describe any kind of configurability with respect to the method of data latching. Moreover, the written description does not show that the applicant was in possession of a memory device that could transfer command data, address data, input data, and output data in a double-data rate configuration.

- “[A] transition of the control signal from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface”; “a transition of the control signal from the active state to the inactive state indicates an end of the transfer of the at least one of command data, address data, input data and output data.” (Claim 1, 6). Based on Plaintiff’s flawed-apparent construction (which Defendants believe is wrong), Plaintiff appears to contend that a chip select/chip enable signal qualifies as a “control signal” as described in this limitation. Plaintiff appears to point to timing diagrams of the chip select/enable signal to show that this limitation is met. Defendants reject Plaintiff’s flawed apparent construction. But if Plaintiff’s construction were correct, then this claim would be invalid due to the lack of a sufficient written description. The written description does not show that the applicant was in possession of the idea that a transitioning chip select/enable signal could be used to indicate the beginning of data being provided at the at least one common data interface.
- “[A] first transition of the control signal from an inactive state to an active state indicates a beginning of command data being provided at the at least one common data interface”; “a second transition of the control signal from the active state to the inactive state indicates an end of the transfer of the at least one of command data, address data, input data and output data.” (Claim 17, 20). Based on Plaintiff’s flawed-apparent construction (which Defendants maintain is wrong), Plaintiff appears to contend that a chip select/chip enable signal qualifies as a “control signal” as described in this limitation. Plaintiff appears to point to timing diagrams of the chip select/enable signal to show that this limitation is met. Defendants reject Plaintiff’s flawed apparent construction. But if Plaintiff’s construction were correct, then these claims would be

invalid due to the lack of a sufficient written description. The written description does not show that the applicant was in possession of the idea that a first transition of a chip select/enable signal could be used to indicate the beginning of data being provided at the at least one common data interface.

- “[A] clock output port configured to transmit a clock output signal synchronized with the output data when the flash memory device is in the double data rate configuration.” (Claim 4). Based on Plaintiff’s flawed-apparent construction (which Defendants maintain is wrong), Plaintiff appears to contend that a data strobe or a read-write data strobe qualify as an output clock. Defendants reject Plaintiff’s flawed apparent construction. But if Plaintiff’s construction were correct, then this claim would be invalid due to the lack of a sufficient written description. The written description does not show that the applicant was in possession of the idea that an intermittent data strobe could serve as an output clock.
- “The flash memory device as claimed in claim 4, further comprising a delay lock loop (DLL) to synchronize the clock output signal with the clock signal.” (Claim 5). The written description does not show that the applicant was in possession of a memory device comprising a delay lock loop. The specification does not discuss a delay lock loop at all.

3. ’028 Patent

- “[A] configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration.” (Claim 1). The written description does not show that the applicant was in possession of a configurable clock input buffer. The written description does not describe any kind of configurability with

respect to the method of data latching. Moreover, the written description does not show that the applicant was in possession of a memory device that could transfer command data, address data, input data, and output data in a double-data rate configuration.

- “[O]ne or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks.” (Claim 1). The written description does not show that the applicant was in possession of the claimed configurable clock output buffer. While the specification notes that the output buffer drive strength can also be configured, it does not explain how nor that there this could be done for a plurality of buffer drive strengths. Moreover, the configurable output buffer drive strength is disclosed in relation to features of a presently unclaimed embodiment.
- “The configurable non-volatile memory device as claimed in *claim 1*, wherein the first clock input signal, the second clock input signal and the common data signal are terminated signals.” (Claim 8). The written description does not show that the applicant was in possession of a terminated signals for the clock inputs and common data signal. The written description does not discuss the use of terminated signals for all these signals, and instead, only specifies when signals are “un-terminated.”
- “[A] configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended signaling configuration or the differential signaling configuration.” (Claim 10). The written description does not show that the applicant was in possession of a configuration registering storing information relating to the configuration of the clock input buffer.

The written description does not describe any kind of register for storing single-ended as opposed to differential signaling configurations for the clock input buffer.

- “[A] configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers.” (Claim 11). The written description does not show that the applicant was in possession of a configuration registering storing information relating to the output drive strength. The written description does not describe any kind of register for storing single-ended as opposed to differential signaling configurations for the clock input buffer.
- “[T]he default configuration comprises the single ended signaling configuration.” (Claim 14). The written description does not show that the applicant was in possession of a default configuration register for the input clock buffer. The written description does not describe a default configuration for the input clock buffer.

VI. INVALIDITY UNDER 35 U.S.C. § 101

To be patentable subject matter under § 101, a claim must be directed to one of four eligible subject matter categories: “new and useful process, machine, manufacture, or composition of matter.” 35 U.S.C. § 101. “Claims that fall within one of the four subject matter categories may nevertheless be ineligible if they encompass laws of nature, physical phenomena, or abstract ideas.” *Digitech Image Techs., LLC v. Elecs. for Imaging, Inc.*, 758 F.3d 1344, 1350 (Fed. Cir. 2014) (citing *Diamond v. Chakrabarty*, 447 U.S. 303, 309 (1980)). The Supreme Court established a two-step test for deciding the subject matter eligibility of claims under § 101. *Alice Corp. Pty. Ltd. v. CLS Bank Int’l*, 134 S. Ct. 2347, 2355 (2014). First, the claims must be analyzed to determine whether they are drawn to one of the statutory exceptions, *i.e.*, a patent ineligible concept: an abstract idea, a law of nature, or a natural phenomenon. *See id.* Second, the elements

of the claims must be viewed both individually and as an ordered combination to see if there is an “inventive concept.” *Id.*; see also *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327, 1335-36 (Fed. Cir. 2016). The claims are examined to determine if they merely invoke well-understood, routine, conventional components and activity to apply an abstract idea. See, e.g., *Elec. Comm’n Techs. v. ShoppersChoice.com*, 958 F.3d 1179, 1180-82 (Fed. Cir. 2020).

The Asserted Claims of the ’028 Patent are directed to ineligible subject matter under 35 U.S.C. § 101 and applicable case law authority.⁶ The ’028 Patent’s claims are directed to the abstract idea of compatibility with different kinds of signals. The recited components of the invention—e.g., non-volatile memory blocks, chip enable port, two clock input ports, a clock output port, common data ports, and a configurable output buffer—are all conventional either as shown in the prior art or as admitted by the patent itself. See *supra*. Once these conventional components are set aside, see *Broadband iTV, Inc. v. Amazon.com, Inc.*, 113 F.4th 1359, 1369

⁶ See, e.g., *Alice Corp. Pty. Ltd. v. CLS Bank Int’l*, 134 S. Ct. 2347 (2014); *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 132 S. Ct. 1289 (2012); *Trading Techs. Int’l, Inc. v. IBG, LLC*, 921 F.3d 1084 (Fed. Cir. 2019); *ChargePoint, Inc. v. SemaConnect, Inc.*, 920 F.3d 759 (Fed. Cir. 2019); *SAP America, Inc. v. InvestPic, LLC*, 898 F.3d 1161 (Fed. Cir. 2018); *Interval Licensing LLC v. AOL, Inc.*, 896 F.3d 1335 (Fed. Cir. 2018); *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121 (Fed. Cir. 2018); *Two-Way Media Ltd. v. Comcast Cable Commc’ns, LLC*, 874 F.3d 1329 (Fed. Cir. 2017), *cert. denied*, 139 S. Ct. 378 (2018); *Intellectual Ventures I LLC v. Capital One Fin. Corp.*, 850 F.3d 1332 (Fed. Cir. 2017); *Infineon, Inc. v. Ameranth, Inc.*, 842 F.3d 1229 (Fed. Cir. 2016); *Affinity Labs of Texas, LLC v. DIRECTV, LLC*, 838 F.3d 1253 (Fed. Cir. 2016); *Elec. Power Grp., LLC v. Alstom S.A.*, 830 F.3d 1350 (Fed. Cir. 2016); *Enfish, LLC v. Microsoft Corp.*, 822 F.3d 1327 (Fed. Cir. 2016); *Genetic Techs. Ltd. v. Merial L.L.C.*, 818 F.3d 1369 (Fed. Cir. 2016); *Intellectual Ventures I LLC v. Capital One Bank (USA)*, 792 F.3d 1363 (Fed. Cir. 2015); *Internet Patents Corp. v. Active Network, Inc.*, 790 F.3d 1343 (Fed. Cir. 2015); *OIP Techs., Inc. v. Amazon.com, Inc.*, 788 F.3d 1359 (Fed. Cir. 2015); *Content Extraction & Transmission LLC v. Wells Fargo Bank, Nat’l Ass’n*, 776 F.3d 1343 (Fed. Cir. 2014); *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245 (Fed. Cir. 2014); *buySAFE, Inc. v. Google, Inc.*, 765 F.3d 1350 (Fed. Cir. 2014); *Digitech Image Techs., LLC v. Elecs. for Imaging, Inc.*, 758 F.3d 1344 (Fed. Cir. 2014); *CyberSource Corp. v. Retail Decisions, Inc.*, 654 F.3d 1366 (Fed. Cir. 2011); *Automated Tracking Sols., LLC v. Coca-Cola Co.*, 723 F. App’x 989 (Fed. Cir. 2018); *EasyWeb Innovations, LLC v. Twitter, Inc.*, 689 F. App’x 969, 971 (Fed. Cir. 2017); *Yu v. Infineon Inc.*, 1 F.4th 1040 (Fed. Cir. 2021).

(Fed. Cir. 2024), all that remains as the “claimed advance” is the configurable clock input buffer, *AP Am., Inc. v. InvestPic, LLC*, 898 F.3d 1161, 1167 (Fed. Cir. 2018) (focus of Step 1 is on the “claimed advance”); *Finjan, Inc. v. Blue Coat Sys., Inc.*, 879 F.3d 1299, 1303 (Fed. Cir. 2018) (same). However, the recited configurable clock input buffer does not claim any particular structure, configuration, or explanation as to how it actually operates. Indeed, the recited configurable clock input buffer amounts to little more than a device capable of achieving the desired result—a clock input that can operate in either a single-ended or differential clock input. This kind of results-oriented claiming is routinely held invalid under 35 U.S.C. § 101. *See, e.g., O’Reilly v. Morse*, 56 U.S. 62, 100 (1853); *USAA v. PNC Bank N.A.*, 139 F.4th 1332 (Fed. Cir. 2025).

There is no inventive concept that saves this claim at *Alice*’s second step. As noted, all the recited components are conventional, arranged in a conventional order, and performing their conventional functions. Even if the patentee points to the purported “configurable clock input buffer” as being the inventive, this argument fails—the abstract idea cannot supply the inventive concept. Moreover, none of the dependent claims recite inventive concepts that render them patentable. Each recites narrowing limitations that merely cabins the abstract idea to a narrower technological environment, but this does not make the invention inventive nor render the abstract idea any less abstract. *See Bilski v. Kappos*, 561 U.S. 593, 612 (2010); *Alice*, 573 U.S. at 223. Further, the remaining dependent claims recite post-solution steps that do not change the character of the claimed advance (a device capable of configuring its clock input from single ended to differential) nor supply anything but conventional components performing their conventional functions. Such limitations are insufficient to convey patentability. *See Diamond v. Diehr*, 450

U.S. 175, 191–92 (1981) (“[I]nsignificant post-solution activity will not transform an unpatentable principle into a patentable process.”). Thus, the ’028 Patent’s claims are invalid under § 101.

VII. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

Infineon is producing and/or making available for inspection the documents required under the Court’s Standing Order Governing Patent Proceedings.

Infineon reserves the right to produce and rely on additional documents relating to its products in view of, for example, additional information revealed during discovery regarding MOSAID’s allegations and/or amendments to MOSAID’s preliminary infringement contentions.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the foregoing document was served electronically on August 15, 2025, to all counsel of record.

/s/ David M. Hoffman

David M. Hoffman